

# Random-Telegraph-Noise by Resonant Tunnelling at Low Temperatures

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## Abstract

We have found a systematic way to identify the bias conditions to observe the Random-Telegraph-Noise (RTN) in advanced Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs). We measured a *p*-type MOSFET at 2K, and found narrow bias conditions to observe the RTN presumably caused by charge trapping and de-trapping, which were only observed at low temperatures. It will pave the way to address the nature of a trap, which will be useful to understand the mechanism of RTN to secure the reliability. (Keywords: Random-telegraph-noise, charge trap, low temperatures)

## Introduction

The RTN is becoming one of the major concerns to secure reliabilities in MOSFETs, when the technology node is scaled down to sub-20nm [1-2]. The RTN would be caused by the threshold voltage fluctuations due to the trapping/de-trapping process of carriers at charge traps near the Si/SiO<sub>2</sub> interface [3]. However, it is difficult to identify the nature of these processes, since it is difficult to find a typical MOSFET statistically showing the RTN at room temperatures. The low temperature measurement of the RTN was reported previously [4], but the precise conditions under which bias conditions are required for the RTN, were missing. We measured MOSFET devices at low temperatures and identified the narrow bias conditions to observe the RTN.

## Experimental Data and Discussion

The measured device was a standard *p*-type MOSFET with the width of 10 $\mu$ m and the length of 75nm. The device with a large width was chosen to increase the chance to find the RTN. The gate electrode was made of doped poly-Si, and the gate oxide was 2.4nm-thick SiO<sub>2</sub>. Subthreshold characteristics are shown in Fig. 1. The subthreshold slope was 80.8mV/decade at 300K, 48.4mV/decade at 150K, and 9.8mV/decade at 2K,

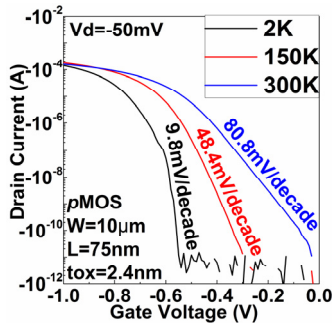


Fig. 1. Subthreshold properties at 2, 150, and 300K.

respectively. The background noise was less than 10pA.

We measured drain current ( $I_d$ ) by changing the gate voltage ( $V_g$ ) and drain voltage ( $V_d$ ) to observe single-hole

charging events. We found Coulomb diamonds [5], as shown in Fig. 2.

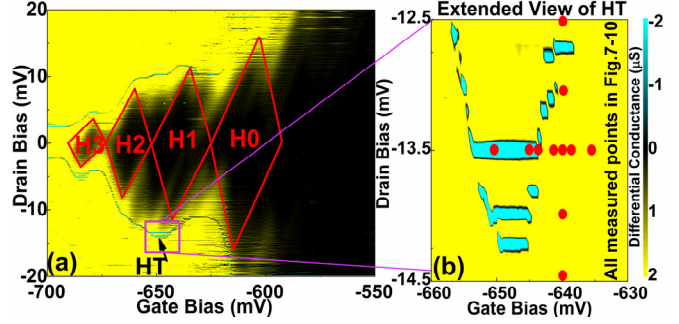


Fig. 2. (a) Current stability diagram of the device at 2K. An expanded diagram is shown in (b).

We extracted the capacitance of the quantum dot related to single-hole transistor characteristics (Table 1). The estimated diameter of the quantum dot is about 25nm, which might be coming from the poly-Si grains of the gate electrode or the surface roughness. The charging energies of the quantum dot were 14meV, 11meV, 8.5meV, and 4.1meV for H0, H1, H2, and H3 states, depending on the number of holes trapped in the quantum dot (Fig. 2(a)), respectively.

Tab. 1. Extracted capacitance of different hole states in the quantum dot.

	$C_g$ (aF)	$C_d$ (aF)	$C_s$ (aF)
H0	4.8	2.6	4.0
H1	6.5	2.8	4.6
H2	7.6	3.8	6.5
H3	8.5	17.2	13.6

Near the edge of Coulomb diamonds, we observed sharp current peaks in the stability diagram. We measured the time domain characteristics of  $I_d$  under the bias conditions for the sharp peaks, and observed RTN, as shown in Fig. 4 (a). We identified the switching with large and small amplitudes, respectively. We investigated on the temperature dependence of the RTN, as shown in Fig. 3. The RTN was observed at 2K, while it was not observed

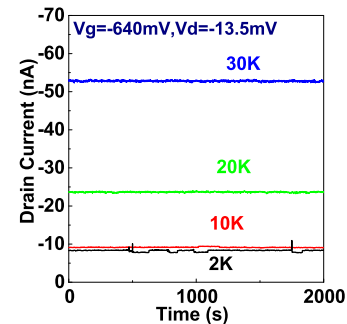


Fig. 3. RTN behaviour at 2, 10, 20, and 30K.

above 20K. This implies that the thermal assisted transport hinder the observation of the RTN.

We have analysed the frequency to observe the current within a certain range of a fixed step of 4pA, which is actually the quantum mechanical probability,  $P(I_d)$ , to find the system under a certain current state, which should contain some information about the wave function of the traps. We found 4 different current levels, which are shown in Fig. 4 (b). From 4 levels, we can clearly identify 2 amplitudes; the small one was 71pA, and the large one was 528pA. The RTN with 2 different amplitudes implies that 2 traps were responsible. The schematic potential diagram across the channel is shown in Fig. 5.

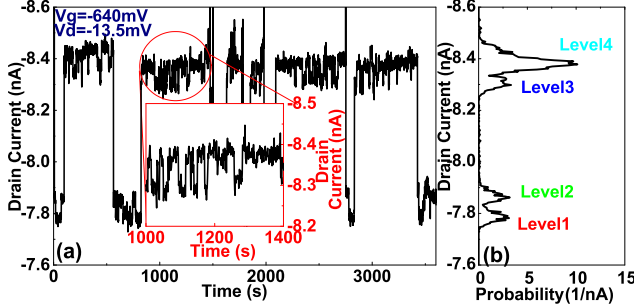


Fig. 4. RTN behaviour of  $I_d$  at HT. (a) shows the time domain measurement result of  $I_d$ . (b) shows the probability of current obtained from frequency counting.

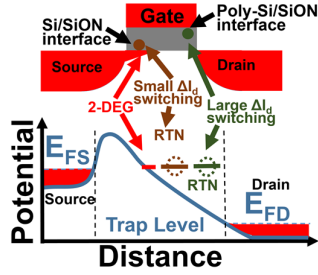


Fig. 5. Schematic potential diagram across the channel.

The current shows different correlation behaviours in time domain with different time lag [6]. The autocorrelation of  $I_d$  was strong if the time lag is 1s (Fig. 6(a)). This means that the switching was not frequently observed in this time scale. At the lag of 10s, the autocorrelation was weaker, and we started to observe switching with the small amplitude. At the lag of 100s, the autocorrelation was almost random (Fig. 6(c)), and we can recognize both small and large amplitudes.

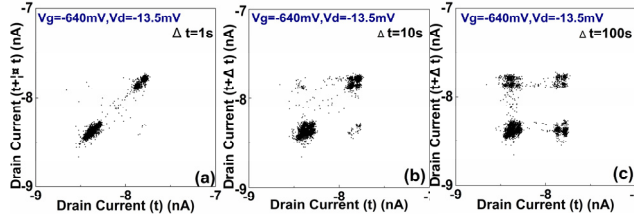


Fig. 6. lag plot of RTN under certain bias conditions. The shape of lag plot shows the correlation behaviour of current in time domain with different time lag.

We studied the  $V_g$  dependence of the RTN at  $V_d$  of -13.5mV (Figs. 7 and 8). We can explain these by assuming that the traps responsible for the large amplitude was located at the poly-Si/SiON interface, while the trap

responsible for the small amplitude was located at the SiON/Si interface (Fig. 5). We observed switching with both small and large amplitudes at  $V_g$  between -645mV and -640mV, since the trap level at the top interface is aligned with the Fermi level of the poly-Si, while the trap level at the bottom interface was aligned to the 2D hole-inversion layer. At  $V_g$  of -635mV, only the bottom trap was trapped/de-trapped through resonant tunnelling and the top trap was occupied, so that the switching of the small amplitude was observed.

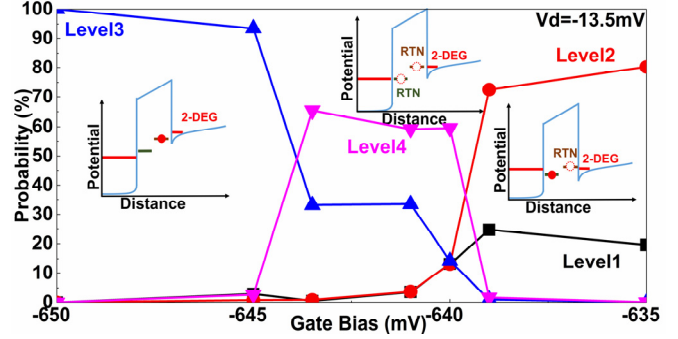


Fig. 7. Gate modulation of probability to find  $I_d$ . Schematic potential diagram under each bias condition is shown.

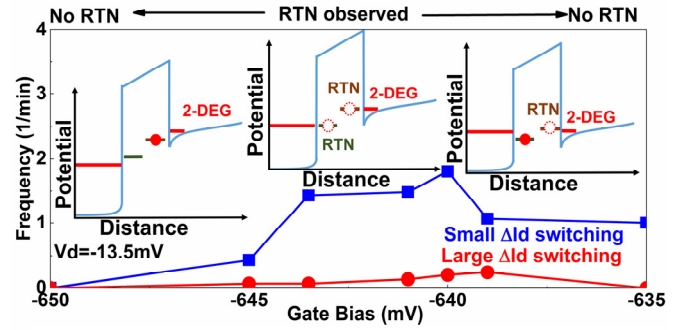


Fig. 8. Gate modulation of the RTN frequency. Schematic potential diagram under each bias condition is shown.

Finally, we examined the  $V_d$  dependence of the RTN at  $V_g$  of -640mV (Figs. 9 and 10). The switching of the small amplitude was observed in the entire  $V_d$  range, which implies that the bottom trap did not change significantly upon the change of  $V_d$ . This means that the bottom trap was presumably located at the source edge. On the other hand, the switching of the large amplitude was observed only at  $V_d$  between -13.0mV and -14.0mV, which means that the top trap level was resonated to the gate in the very narrow bias window. Considering the sensitivity of the top trap on  $V_d$ , we think that the top trap is located near the drain edge. The narrow bias condition

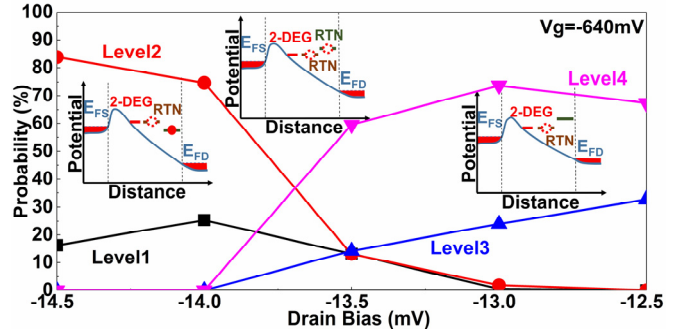


Fig. 9. Drain modulation of probability to find  $I_d$ . Schematic potential diagram under each bias condition is shown.

to observe the RTN implies resonant tunnelling was responsible for the trapping/de-trapping process.

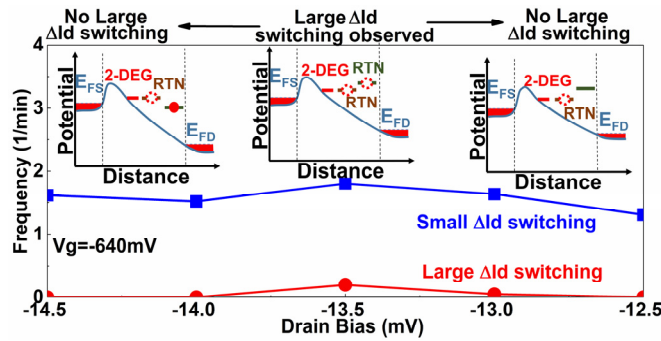


Fig. 10. Drain modulation of the RTN frequency. Schematic potential diagram under each bias condition is shown.

### Conclusion

We have found resonant peaks in  $I_d$  under narrow bias conditions and observed the RTN at 2K. We addressed the 2 traps are responsible for the switching of large and small amplitudes. By measuring the current stability diagram, we can systematically identify bias conditions to find shallow traps through resonant tunnelling. We can apply this technique to investigate the reliability of MOSFETs in more detail for understanding the mechanism of the RTN for the future.

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