Direct Off-Line Two-Switch Forward Converter with a Boost PFC Converter for Powering of DC Electromagnet Systems

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***Abstract* – In this paper a switch mode power supply design for electromagnet systems is presented. It is based on a boost converter with power factor correction and a two-switch forward converter. The powered electromagnetic systems in this research are part of various electrical contact apparatus such as electromagnetic contactors, relays, circuit breakers etc. The proposed schematic works in a wide input voltage range which solve the problem with the voltage sag occurring in the energy distribution system. The proposed solution ensures stable operation of the contact equipment and the relay circuits in their industrial application.**

***Keywords* – Switch Mode Power Supply, Boost converter, Power Factor Correction, Forward Converter, Electromagnetic System.**

1. Introduction

The voltage sag is a process that occurs in the electrical distribution system due to different transient processes such as switching operations associated with a temporary disconnection of supply, short circuits, inrush currents coursed of induction motors etc. It is defined as the decrease in the RMS voltage under 90% of the nominal value for a duration greater than 0.5 sec. but less than 1 min. Comprehensive descriptions of this process are given in [1, 2, 3, 4] and different methods for its measurement and mitigation are proposed in [5, 6, 7, 8]. Despite the proposed solutions the voltage sag is still a problem which broadly affects all electrical loads.

The proposed system is presented in Fig.1A. The electromagnet is part of an electromagnetic contactor which is powered from a switch mode power supply (SMPS), complete with the following elements: input rectifier and filter, boost converter with power factor correction (PFC) and forward converter. The input voltage can vary in the range 85-265V which covers the standards 110V and 230V without additional switching and prevents the voltage sag (Fig.1B) if the system works on 230V.

A two-switch forward converter is used here as it has some desirable advantages: galvanic disconnection between the primary and secondary side; the voltage across the MOSFETs is equal to the input voltage; simple driver circuit as the two transistors operate synchronously; operation in the power range around 1kW is possible.

The forward two-switch converter has been the object of significant research. In [9, 10] applications with multiple and variable outputs are presented. Some approaches for improving the efficiency based on zero voltage switching are given in [11, 12, 13]. The potential use as micro inverter [14] shows that an application for AC electromagnet systems is also possible with this schematic. A comparison between forward and flyback converters is shown in [15]. In this research the two-switch forward converter has been chosen because of its greater power rating. Several different specific applications are studied from [16, 17, 18, 19, 20, 21], respectively battery chargers, photovoltaic systems, supercapacitors power supply sources, hybrid electrical vehicle and arc welding power supplies. These applications show a significant flexibility and applicability of this type of forward converter.

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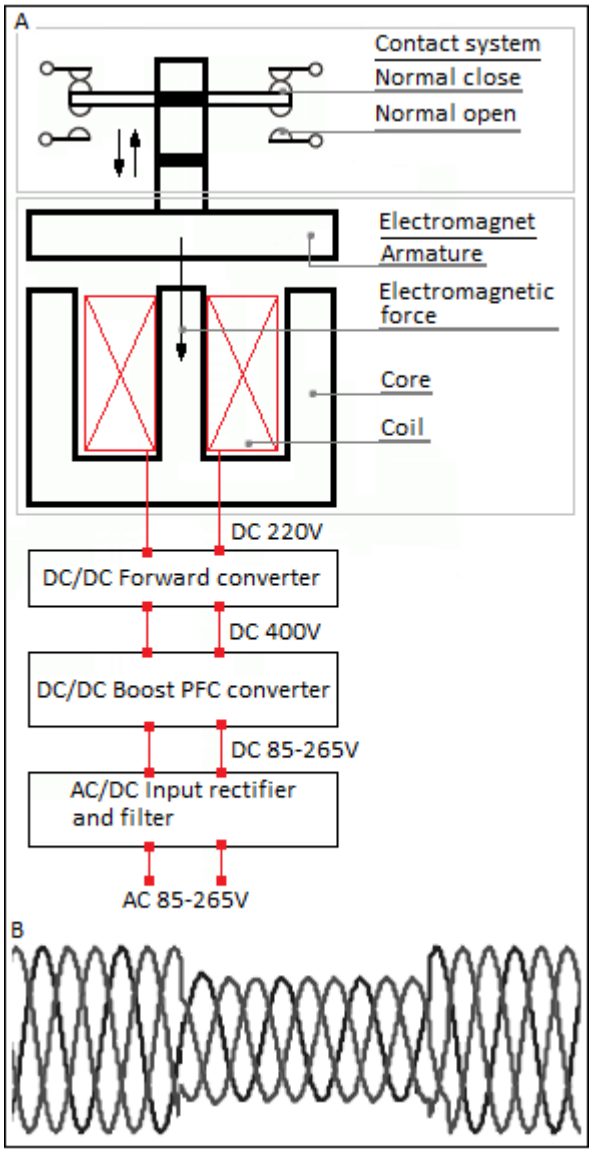

Figure 1. A. Electromagnet system powered form switch mode power supply; B. Voltage sag.

For the experimental verification two platforms [22, 23] are used and the design is based on several established procedures and application manuals [24, 25, 26, 27, 28, 29]. The basic requirement to the input filter, the rectifier and the boost converter is operation in the proposed above voltage range with power factor correction. The design procedures are given in [30, 31, 32] which are applied for the proposed power supply system. Although the design of the powered electromagnet is not an object of this research its parameters have been considered according to [33, 34, 35].

The aim of this research is to propose a SMPS specifically designed for electromagnetic systems which are part of electrical apparatus. The wide input voltage range must prevent the voltage sag seen commonly occurred in any electrical distribution network.

The paper is organised as follows: part 2 gives an analysis of the proposed schematic where the basic parts of the proposed SMPS are described; part 3 presents the basic design of the proposed converter where the most important of the calculation procedure is given; the experimental verification of the entire system based on PFC boost converter, two-switches forward converter and electromagnet as a load is shown in part 4; the conclusions are formulated in part 5.

2. Analysis of the proposed schematic

The basic parts of the proposed schematic are given in Fig.2 as follows:

- *Module 1. Input common mode filter*. It is comprised from X capacitors C1 and C2, Y capacitors C3 and, C4 and input filter Lf.
- *Module 2. Input rectifier*. The full bridge rectifier is comprised from diodes D1-D4 and filter capacitor C5. This capacitor is not the normal electrolytic boost capacitor because of the power factor correction operations. Normally here a ceramic capacitor is used with value between 220nF - 470nF.
- *Module 3. Boost converter*. The boost converter schematic is comprised of transistor Q3, inductor L1 and diodes D5, D10 is an object of design. The input divider R1-R2 is connected directly to the input rectifier for zero detection in the input half wave voltage. The current sense resistor R3 measures the current through Q3. Respectively, the points 1 and 2 are voltage and current signals to the microcontroller and point 11 is the gate drive signal.
- *Module 4. Forward two-switch converter*. The schematic can be divided into the primary (transistors Q1, Q2, diodes D6, D7, the transformer Tr1) and secondary side (the rectifier D8, D9 and the filter L2, C7).
- *Module 5. DC Electromagnet as load of the power supply system.* An electromagnet has a significant inductance which must be taken into consideration in the design procedure. The maximum power of the proposed power supply system is 500W which can power a considerable range of low voltage contactors or circuit breakers. Examples are given in Tabl.1 according to [36, 37].

Table 1. Power of electric DC contactors.

Type of DC contactors	Power of the electromagnet system [W]
AL 9, 12, 16	3
AL 26, 30, 40	3,5
AE 45, 50, 63, 73	200
AF 45, 50, 63, 75	190
AE 95, 110	400
AF 95, 110	400
AF 145, 185	500
AF 210, 260, 300	520
AF 400, 460	990

- *Module 6. Gate driver for the forward converter*. The gate drive schematic provides the pulse width modulation (PWM) signal to transistors Q1 (point 3) and Q3 (point 5).
- *Module 7. Feedback circuit*. The feedback circuit is based on a linear operational amplifier combined with an optocoupler X1 and additional active filter X2. The schematic gives the precise measurement of the output voltage over the divider R4-R5 (point 6) and options for its software digital control.
- *Module 8. Control system based on an STM32 Cortex microcontroller*. The control system is beyond the scope of the presented paper, but information about these types of microcontrollers can be found in [38, 39].

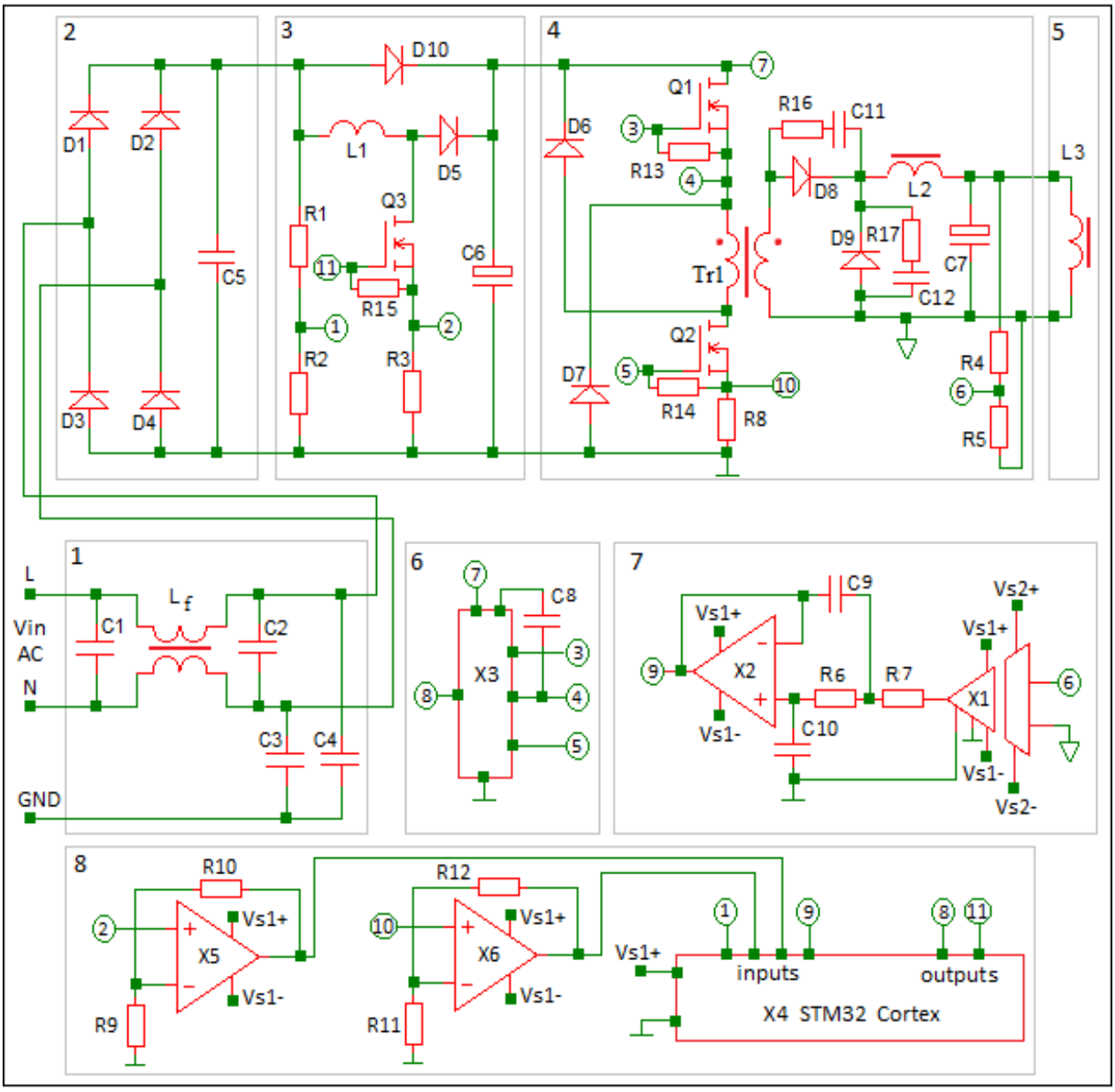

Figure 2. Schematic of of-line switch mode power supply for DC electromagnets

3. Basic design of the power part of the proposed converter

The power stage of the boost converter follows the design procedures shown in [30, 31, 32], and the design of the forward converter is given in [21, 22, 23, 24, 25]. However, only a specific example is provided here in order to show the feasibility of the proposed schematic.

The parameters used in the design procedure are as follows:

- $I_{IN.nom.rms}$, $I_{IN.max.rms}$, $I_{IN.min.rms}$ are the input nominal, maximum and minimum RMS currents.
- $I_{OUT.avg}$, $I_{OUT.min}$, $I_{OUT.max}$, $I_{OUT.ripple}$ are the average, minimum, maximum and ripple output DC currents.
- $I_{D.rms.Q3}$ is the Drain-Source current through the boost MOSFET transistor Q3.
- $I_{D.Q1Q2.avg}$, $I_{D.Q1Q2.min}$, $I_{D.Q1Q2.max}$ are the Drain-Source average, minimum and maximum current through the primary side MOSFET transistors Q1 and Q2.
- P_{IN}, P_{OUT} are the input and output power.
- P_{BR1} is the dissipated power from the rectifier.
- $V_{IN.nom.rms}$, $V_{IN.min.rms}$, $V_{IN.max.rms}$, $V_{IN.pk}$ are the nominal, minimum, maximum and peak input RMS voltages.
- V_{out} is the output DC voltage.
- V_{csR2}, V_{csR8} are the voltages across the current sense resistors R2 and R8.
- V_F is the forward drop over the input diodes;
- V_{bus} is the voltage from the boost PFC converter.
- $V_{bus.min}$ is the minimum voltage from the boost PFC converter.
- η is the efficiency.
- DC_{boost} is the duty cycle of the boost converter.
- $DC_{forward}$ is the duty cycle of the forward converter.
- $t_{hold-up} = 20ms$ is the standard SMPS hold-up time of 20 ms.
- ΔI_{L2} is the current ripple through the inductor L2.
- $\Delta V_{out\%}$ is the output voltage ripple over the load.

The input parameters of the designed converter are given in Tabl.2.

Table 2. Input parameters of the converter.

Input voltage AC (minimum)	85 V
Input voltage AC (maximum)	265 V
Input voltage AC (nominal)	230 V
Output voltage DC	230 V
Voltage after the boost converter	400 V
Output power	500 W
Maximum switching frequency of the boost and forward converters	100 kHz

The input power P_{IN} depends on the efficiency. For this design a reasonable assumption is $\eta = 0.85$:

$$P_{IN} = \frac{P_{OUT}}{\eta} \quad (1)$$

The input current is at a maximum when the input voltage is at a minimum $V_{IN.min.rms}$:

$$I_{IN.max.rms} = \frac{P_{IN}}{V_{IN.min.rms}} \quad (2)$$

From the same equation the nominal current is:

$$I_{IN.max.rms} = \frac{P_{IN}}{V_{IN.nom.rms}} \quad (3)$$

The power dissipated from the input bridge rectifier depends on the forward voltage drop V_F. If it is assumed $V_F = 0.7V$ the power P_{BR1} is given from:

$$P_{BR1} = 2.V_F.I_{IN.max.rms} \quad (4)$$

The boost PFC converter must be designed at minimum input voltage $V_{IN.min.rms}$, maximum output power P_{OUT} and maximum input voltage.

The inductor L1 is chosen in order to provide 20% output ripples. The boost PFC converter operates at a constant frequency of 100 kHz, and variable duty cycle DC_{boost}:

$$DC_{boost} = 1 - \frac{V_{IN.min.rms} \times \eta}{V_{out}} \quad (5)$$

The inductor L1 value is calculated on the nominal values with 20% current ripple:

$$L_1 = \frac{V_{in.nom.rms} \times (V_{out} - V_{in.nom.rms})}{0.2 \times I_{in.nom.rms} \times F_{sw.boost} \times V_{out}} \quad (6)$$

The maximum current peak value $I_{L1.max.pk}$:

$$I_{L1.max.pk} = \frac{P_{out} \cdot \sqrt{2}}{V_{IN.min.rms}} \quad (7)$$

The Q3 current can be calculated from:

$$I_{D.rms}^2 = \frac{2}{T}\int_0^{\frac{T}{2}} DC_{boost}(t).I_{IN.max.rms}^2(t)dt =$$

$$I_{D.rms}^2 = \frac{2}{T}\int_0^{\frac{T}{2}} \left(1 - \frac{V_{IN.pk}.\sin(\omega t)}{V_{bus}}\right) \times \quad (8)$$

$$\times I_{IN.max.rms}^2.sin^2(\omega t)dt$$

Eventually, the current $I_{D.rms.Q3}$ is:

$$I_{D.rms.Q3} = I_{in.max.rms}\sqrt{\frac{1}{2} - \frac{4}{3\pi}\frac{V_{IN.pk}}{V_{bus}}} \quad (9)$$

The PFC current sense resistor R2 is:

$$R2 = \frac{V_{csR2}}{I_{L1.max.pk} + \frac{0.2 \times I_{L1.max.pk}}{2}}, \quad (10)$$

but because in this design a standard value of 0.01 Ohm is chosen, the voltage over the resistor is:

$$V_{csR2} = R2.\left(I_{L1.max.pk} + \frac{0.2 \times I_{L1.max.pk}}{2}\right) \quad (11)$$

This voltage requires an additional operational amplifier X5 connected as a non-inverting amplifier.

In this case the power dissipation over R2 is:

$$P_{R2} = V_{csR2}.I_{D.rms.Q3} \quad (12)$$

The last result shows that a 1W SMD resistor would be a possible choice.

The boost capacitor C6 must be calculated according to the standard hold-up time of 20ms. where the minimum capacitance can be derivated from:

$$\frac{1}{2}C_6\left(V_{bus}^2 - V_{bus.min}^2\right) \geq P_{out}.t_{hold-up} \quad (13)$$

It has been experimentally tested that during $t_{hold-up}$ the bus voltage V_{bus} must not drop under 385V. In order to allow for stable operation, the fluctuation must not be greater than 15V. In this case the minimum capacitance is:

$$C_6 = \frac{P_{out}.t_{hold-up}}{V_{bus}^2 - V_{bus.min}^2} \quad (14)$$

Two capacitors rated at $470\mu F, 450V$ in parallel are a possible solution.

The forward converter also works with a constant switching frequency of 100 kHz. Normally, this type of converter works under a 50% duty cycle but here a safety margin of 10% is applied in order to stabilise the output voltage during the input voltage sag. With this assumption the maximum duty cycle is $DC_{forward} = 40\%$. The transformer turn ratio would be:

$$\frac{N_{sec}}{N_{prim}} = \frac{V_{out}}{V_{bus}.DC_{forward}} \quad (15)$$

The output secondary average current is given from:

$$I_{OUT.avg} = \frac{P_{out}}{V_{out}} \quad (16)$$

If 20% output current ripple is assumed:

$$I_{OUT.ripple} = 0.2 \times I_{OUT.avg} \quad (17)$$

From these values the primary side average current is given from:

$$I_{D.Q1Q2.avg} = I_{OUT.avg}.\frac{N_{sec}}{N_{prim}} \quad (18)$$

If the current sense resistor R8 is a standard 0.01 Ohm 1% SMD, the voltage over it would be:

$$V_{csR8} = R8 \times I_{D.Q1Q2.max} \quad (19)$$

which must be amplified from the operational amplifier X6. The dissipated power is 0.12W.

The output inductor ripple is

$$\Delta I_{L2} = \frac{V_{out}}{L_2}.\frac{(1-DC_{forward})}{f_{sw}} \quad (20)$$

or if the ΔI_{L2max} is the maximum output current:

$$L_2 = \frac{V_{out}}{\Delta I_{L2max}}.\frac{(1-DC_{forward})}{f_{sw}} \quad (21)$$

The output capacitor C_7 is calculated from:

$$C7 = \frac{1}{8}.\frac{1-DC_{forward}}{L_s * f_{sw}^2}.\frac{1}{\Delta V_{out\%}}, \quad (22)$$

where, as a first assumption is taken the voltage output ripple 10% of the nominal output voltage.

The results according to the input parameters are given in Tabl.2.

Tabl.3 Results according to the input parameters given in Tabl.2.

Equation	Parameter	Value
1	P_{IN}	558 W
2	$I_{IN.max.rms}$	6.9 A
3	$I_{IN.max.rms}$	2.55 A
4	P_{BR1}	8.3 W
5	DC_{boost}	0.55
6	L_1	2.5 mH
7	$I_{L1.max.pk}$	8.32 A
9	$I_{D.rms.Q3}$	5.1 A
11	V_{csR2}	0.092 V
12	P_{R2}	0.47 W
14	C_6	849 μF
15	$\frac{N_{sec}}{N_{prim}}$	1.5
16	$I_{OUT.avg}$	2.17 A
17	$I_{OUT.ripple}$	0.43 A
	$I_{OUT.min}$	1.95 A
	$I_{OUT.max}$	2.39 A
18	$I_{D.Q1Q2.avg}$	3.2 A
	$I_{D.Q1Q2.min}$	2.8 A
	$I_{D.Q1Q2.max}$	3.5 A
19	V_{csR8}	0.035 V
21	L_2	550 μH
22	C_7	1.5 μF

4. Experimental results

The experimental results are shown as follows:

- *Fig. 3. The primary side of the forward converter*. Transistors Q1 and Q3 are switched-on simultaneously with the gate drive signal (1). The current through (2) begins each cycle at zero value before reaching the peak. The voltages of the Drain-Source (Fig. 3A, graphics 3, 4) over Q1 and Q2 are equal to the bus voltage. During the gate drive OFF period the transformer is fully demagnetised through diodes D6 and D7. The time of the demagnetisation process is shown on fig. 3B as t_{demag}. It finishes before the next ON period which prevents the saturation of the transformer. This shows that the design is correct for the given frequency.
- *Fig. 4. The secondary side of the forward converter*. The output current through the load i.e. the electromagnetic system (Fig. 4A, graphic 4) shows the assumed 10% ripple, and the voltage over the electromagnet is filtered from the output filter. The current through D8 meets its maximum value. Moreover, the provided experiments showed that the two additional snubbers over the diodes D8 (R15, C11) and D9 (R17, C12) are mandatory (30 Ohm, 1nF, 400V). Their design requires experimental measurements and has been done according to [23].
- *Fig. 5. The boost converter with PFC and Fig.6 test of the PFC operation mode*. The input full wave voltage (Fig. 5A, graphic 2) must have a clear zero crossing point. This means that the capacitor C5 must not smooth the input waveform. For the designed converter, this capacitor can be ceramic with a capacitance in the range 220-330nF. For this module, it was experimentally found that an additional diode D10 is necessary in order to mitigate the inrush current during the start-up transient process. The reason is that the designed converter for this specific application cannot have soft start and input inrush current limitation as such functions could affect the start-up time of the electromagnetic system. The PFC operation mode is checked and depicted in three points of the input waveform: zero crossing point (Fig. 5B), 50% (Fig. 6A) and maximum point of the input waveform (Fig. 6B). The modulation of the gate drive PWM (graphic 1) shows that the boost converter works with PFC. Eventually, the power factor is 0.98.

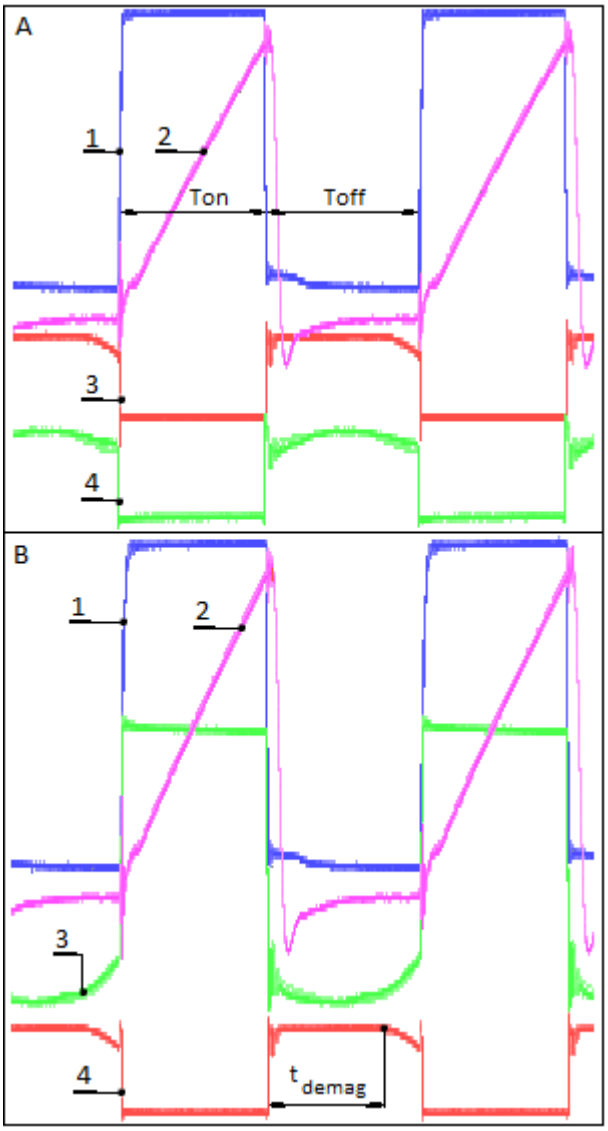

Figure 3. The primary side of the forward converter.
A: 1 Gate drive PWM; 2 Primary side current through the transformer; 3, 4, Voltages of the Drain-Source across Q1, Q2;
B: 3 Voltage across the primary side on the transformer.

- *Fig. 7. Experiment with an input voltage sag*. The voltage sag is within 37% of the nominal voltage. If the voltage sag decreases below that value the PFC stage must be switched-off from the microcontroller. Fig. 7A shows the input waveform after the rectifier on the minimum input and Fig. 7B the same waveform on the nominal input. The average currents and PWM are also depicted. During the sag time the output voltage (Fig. 4A, graphic 3) has remained constant which shows the stable operation of the entire system. The presented experiments have been done with several types of electromagnets functioning as a propulsion system of electromagnetic contactors. A switching ON-OFF process on the contact system (Fig. 1A) has not been mentioned.

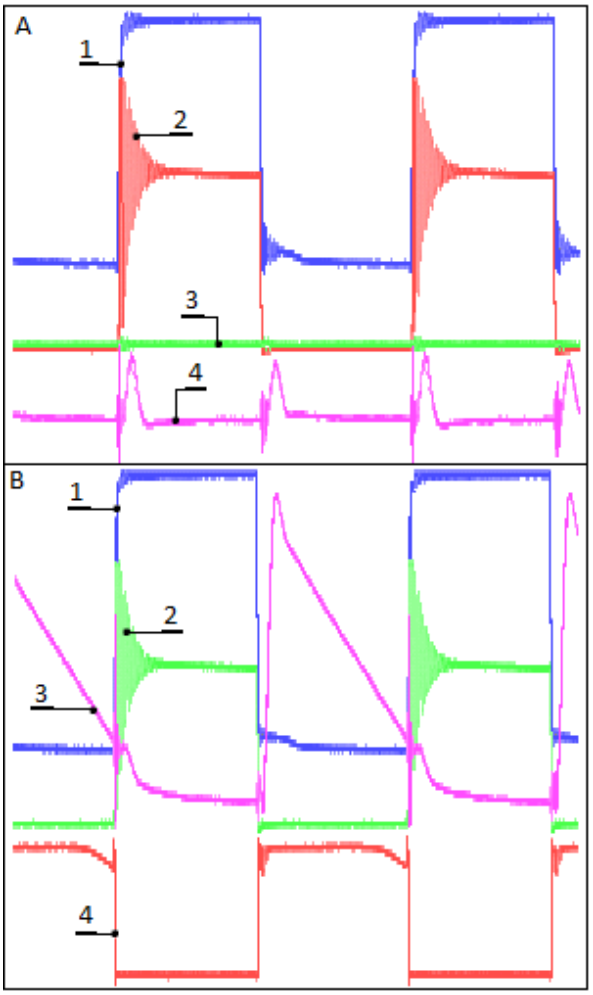

Figure 4. The secondary side of the forward converter. A: 1. Gate drive PWM; 2. Voltage across the inductor L2; 3. Output voltage across the electromagnet; 4. Output current through the electromagnet. B: 1. Gate drive signal, 2. Voltage across the inductor L2, 3. Current across D9 during the freewheeling cycle, 4. Voltage across Q1.

The conducted experiments showed that a stable operation under the minimum under voltage is also possible but these several additional steps must be considered: the boost converter stops the PFC operation and stabilises the bus voltage on the maximum possible value; the forward converter works with 50% duty cycle instead of the assumed (eq. 15) 40%. Alternatively, in the design procedure even smaller nominal duty cycle can be applied along with a higher transformer turn ratio. This would give an additional voltage margin.

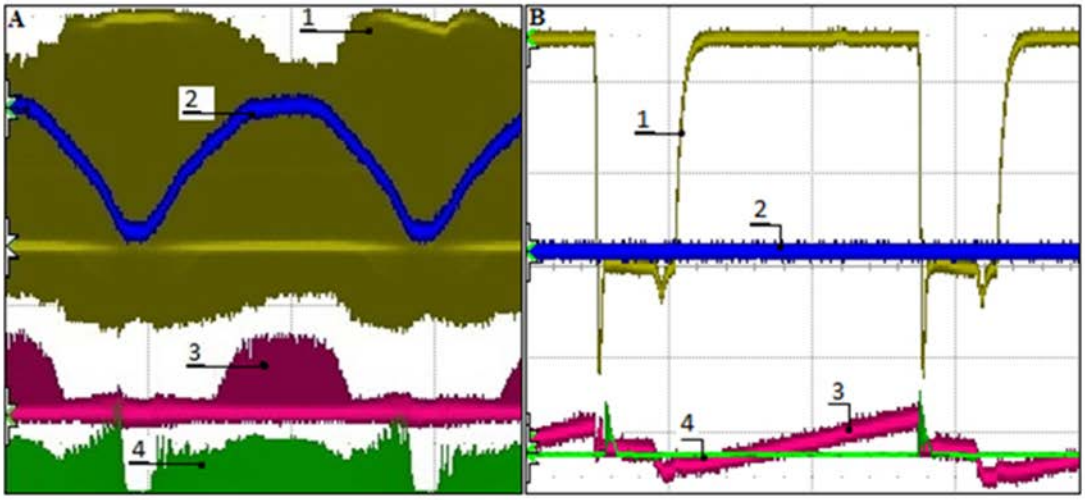

Figure 5. The boost converter with PFC. A: 1. Gate drive signal on Q3 (100 kHz), 2. Input full-wave voltage after the rectifier (100 Hz). 3. Current through the Drain-Source of the transistor Q3. 4. Current through the diode D5. B: Testing the PFC. 1 Maximum duration of the gate drive signal (1) when the input voltage (2) is at zero point. 3. Current through Q3. 4. Current through D5.

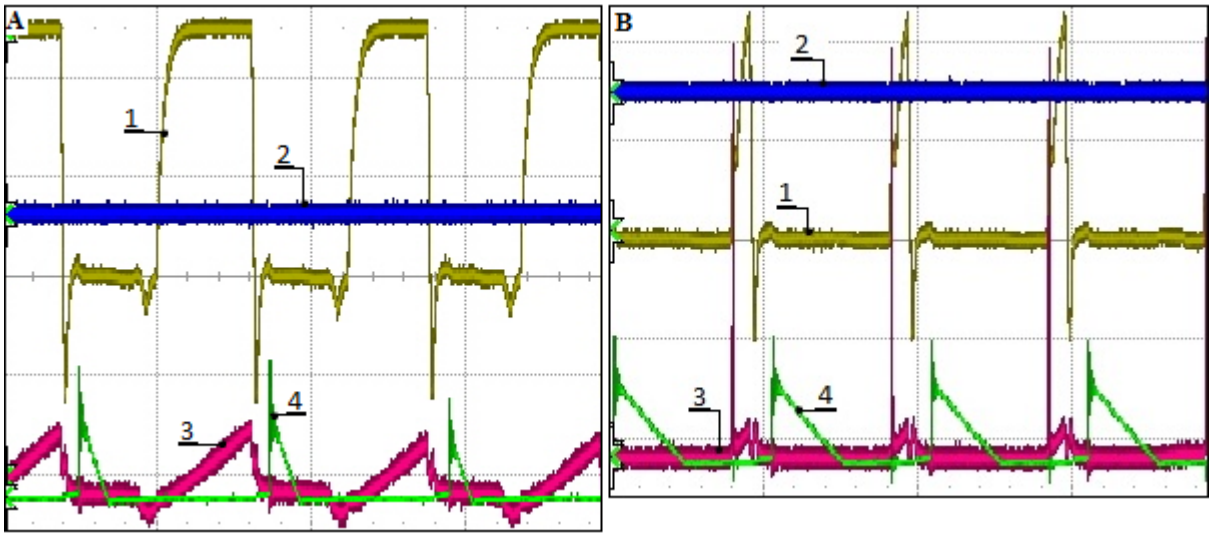

Figure 6. Test of the PFC operation mode (continuation of Fig. 6). A: 1. 50% duration of the gate drive signal (1) when the input voltage (2) is at 50%. B: 1. Minimum duration of the gate drive signal (1) when the input voltage (2) is at maximum point. 3. Current through Q3. 4. Current through D5.

5. Conclusion

Generally, the designed and experimentally tested converter works steadily in the proposed application. The input boost converter stabilised the bus voltage on 400V during the PFC operation in the proposed input voltage range. The experimental verification shows that the PFC stage works normally (Fig. 5, Fig. 6) under the nominal input voltage and should be switched-off during the voltage sag.

The output boost voltage provides a safety margin for the next two-switch forward converter. This converter works steadily (Fig. 3, Fig. 4) under nominal condition with a safety margin on the maximum duty ratio.

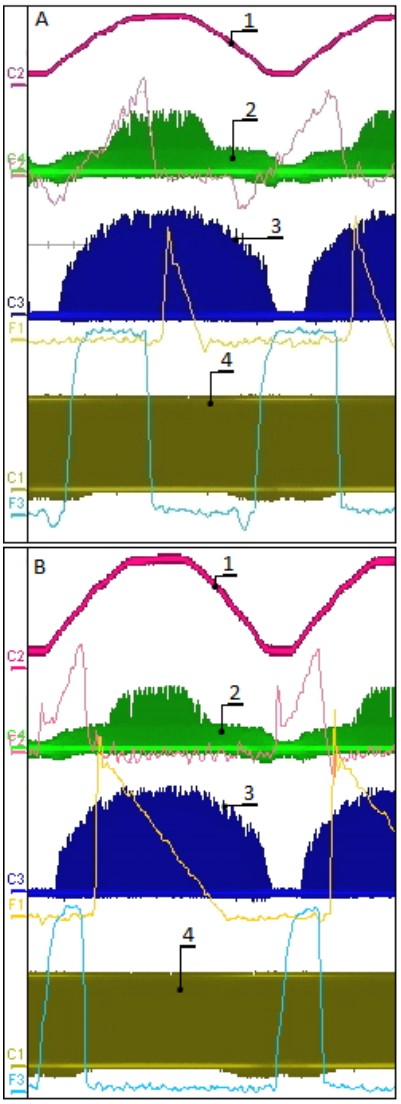

Figure 7. A. Experiment with an input voltage sag voltage. B. Nominal input voltage. 1 Input voltage after the rectifier; 2 Current through boost transistor Q3; 3. Current through boost diode D5; 5. Gate drive on Q3.

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