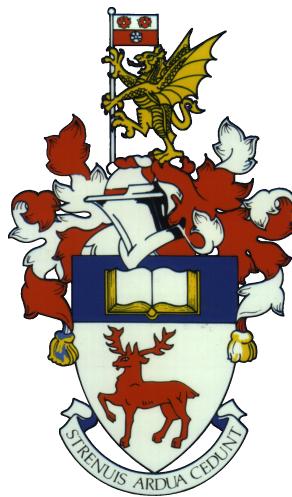


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**Kelvin Probe Force Microscopy (KPFM) for Nanoelectronic Device
Characterisation**

by

Sheng Ye

Thesis for the degree of Doctor of Philosophy

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ABSTRACT

FACULTY OF PHYSICAL SCIENCE AND ENGINEERING

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KELVIN PROBE FORCE MICROSCOPY (KPFM) FOR NANOELECTRONIC
DEVICE CHARACTERISATION

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This project is to develop a new method of characterization for Silicon-nano-wire (SiNW) FET and SET devices by using KPFM technology to derive the information of local surface potential change on the channel of SiNW devices. The surface potential is related to many important parameters on material's surface, e.g. fixed surface charge, doping profile variation, distribution of charge carriers under applied bias, and individual dopant atoms near the surface. Those parameters are strongly related to the characteristics of SiNW devices.

The KPFM equipment is designed to extract the contact potential difference (CPD) between tip and sample. The change of CPD is related to the Fermi energy level in materials. Therefore any factors which induce Fermi energy level change inside material are detectable. The significantly improved lateral resolution (sub-nanometer) gives us confidence for the measurement of local surface potential variation.

Much of the time has been dedicated for the KPFM equipment calibration and optimization. By the end of PhD project the surface potential characterisation of three different types of the silicon-nano-wire (SiNW) devices (uniformly doped SiNW, n-p-n SiNW Field-Effect-Transistor (FET), and n-p-n-p-n SiNW Single-Electron-Transistor (SET)) has been achieved. By using surface potential information the surface trapped charge and change in local resistivity in SiNW is successfully estimated and the result is confirmed well agreed with the characterisation of other conventional method. This characterisation result also suggest the accuracy of local surface potential measurement. In-situ potential mapping and profiling of n-p-n FET channel under device operation has been successfully performed. By comparing the data with simulation and electrical characterisation of the same device, correspondence between the line-shape of the surface potential and electrical field profiles and device parameters has been clarified for the first time. An attempt has been made to observe the surface potential of the channel of SET devices which have shown clear Coulomb oscillation at low temperature (5K). The formation of a conductive channel in 330-nm-wide SiNW channel by the side gate modulation is successfully observed.

Four main achievements can be claimed at the end of this project. First, the metallurgic p-n junction in thin (50nm) SOI has been first time ever detected by E_x curve extraction from measured potential profile and the E_x curve was used to study the charge transport in the n-p-n structure under different biasing condition. Secondary, the novel single side gate doping modulated single electron transistors was fabricated and shown Coulomb oscillations which was consistent with theoretical predictions. Furthermore, the operation of FET/SET was investigated by scanned high resolution surface potential profile which revealed the status of p-n junction under biasing. In the end, this study discovered a new method to investigate nano-electronic devices by KPFM scan and more information such as change in build-in voltage at low temperature, and charge in charge state of island can be extracted if the high vacuum and low temperature is applied.

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Declaration of Authorship

I, **Sheng Ye**, declare that the thesis entitled *Kelvin Probe Force Microscopy (KPFM) for Nanoelectronic Device Characterisation* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as: International Conference [1], [2], [3].

Signed:.....

Date:.....

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Nomenclature

A	Area
A_{tip}	KPFM tip apex area
A_o	Amplitude of resonance without interaction
A_{res}	Reference amplitude value which is set in AM-mode feedback system
B	Band width of resonator
C	Capacitance
d	Distance
C_d	Depletion capacitance
E_c	Energy of bottom conduction band
E_{bi}	Build in energy in p-n junction
E_f	Fermi Energy Level
E_i	Intrinsic Fermi Energy Level
E_v	Energy of top valance band
E_{res}	Energy stored in cantilever
E	Electric field
E_{max}	Maximum electric field
E_x	Electric field in x direction
E_y	Electric field in y direction
ϵ_o	Permittivity of vacuum
ϵ_{ox}	Permittivity of Oxide
ϵ_{si}	Permittivity of Silicon
f	Frequency
ω	Angular frequency
F	Force
I	Current
J	Current density
k	Spring constant
k_B	Boltzmann constant
L	Length
L_d	Diffusion length
μ	Mobility
μ_e	Mobility of electrons

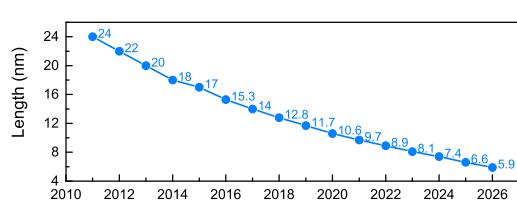
μ_h	Mobility of holes
m	Mass
n	Density of electrons
n_i	Intrinsic electron density
N_a	Density of acceptors
N_c	Effective density of state in conduction band
N_d	Density of donors
N_v	Effective density of state in valance band
p	Density of holes
p_i	Intrinsic hole density
ψ	Potential
ψ_b	Potential between Fermi level and intrinsic Fermi level
ψ_{bi}	Build in potential in p-n junction
ψ_f	Fermi potential (potential from Fermi energy level to vacuum)
ψ_i	Intrinsic potential (potential from intrinsic Fermi energy level to vacuum)
$q\psi$	Work function
$q\psi_n$	Work function of n-type silicon
$q\psi_p$	Work function of p-type silicon
ϕ_s	Surface potential
ϕ_{sn}	Surface potential of n-type Si
ϕ_{sp}	Surface potential of p-type Si
q	Electron charge ($=1.6 \times 10^{-19}$ C)
Q	Quality factor of cantilever
R	Resistance
R_c	Connection Resistance
R_s	Sheet Resistance
R_{total}	Total Resistance
ρ	Resistivity
ρ_{net}	net charge density
S_R	Linear Fitting Slope of $R - L$ curve
t	Thickness/ time
T	Kelvin temperature
V	Voltage
V_{cpd}	Contact potential
V_d	Drain voltage
V_{fb}	Flat Band Voltage
V_g	Gate voltage
V_{th}	Threshold voltage
ΔV	Oscillation period of Single-Electron-Transistor
W	Width
W_d	Depletion width

W_s Width of space change region
 z Tip-sample distance

Chapter 1

Introduction

Silicon-nano-wire (SiNW) is popular building block in various applications, such as highly scalable transistor [4, 5, 6], highly sensitive sensors [7, 8, 9], and quantum information processing devices [10, 11]. First of all, the semiconductor industry get benefits from scaling according to Moore's Law. ITRS2011 (Figure 1.1(a)) predicted the gate size of transistor will be below 18nm since 2014 [12]. However planar field-effect-transistors (FET) present its difficulty to be scaled below 20nm due to the short channel effect, unavoidable significant parameter variations in manufacturing process, and quantum effects [13, 14]. On the other hand, high scalability (<20 nm) and enhanced performance have been realized by full depletion in SiNW transistors [4, 5, 6]. Moreover, by changing the gate structure and modifying SiNW surface, SiNW transistor can be used for sensing applications [7, 8, 9]. With different target materials covered on the SiNW surface, it can be extended for various sensing applications, such as bio-medical and gas sensors. Moreover, even though quantum effects prevent scaling but it can be used for quantum information processing in intentionally designed SiNW quantum information devices [10, 11]. Quantum confinement in SiNW can be defined by gate-induced electrical potential barrier or by introducing physical constriction. In carefully designed SiNW quantum devices the electron spin is able to be controlled and read out by ultra charge sensitive SET based electrometer [15].



(a) Scaling trend

Table PIDS1. Process Integration Difficult Challenges

Near-Term 2011-2018	Summary of Issues
Scaling Si CMOS	Scaling planar bulk CMOS
	Implementation of fully depleted SOI and multi-gate (MG) structures
	Controlling source/drain series resistance within tolerable limits
	Further scaling of EOT with high k materials ($k > 30$)
	Threshold voltage tuning and control with metal gate and high- k stack
	Inducing adequate strain in new structures

(b) Fabrication difficulties

Figure 1.1: ITRS2011 prediction for physical L_{gate} and fabrication process challenge [12]

The challenges of fabricating SiNW devices are also pointed out by ITRS2011 (Figure 1.1(b)). The electrical characteristics of nano-electronic-devices are easily affected in many ways e.g. gate potential distribution on devices channel [8], surface charge distribution [9], dopant atoms distribution [16, 17] etc. As the number of atoms are significantly reduced in highly-scaled nanodevices, even single or a few electrons around the channel largely affect the device characteristics and its stability. The SiNW transistor is still field effect transistor. The charge distribution in the SiNW channel and its transport behaviour heavily depend on how the surface potential is distributed. As the size of SiNW transistor is further shrank below 20 nm, the surface potential is able to influence charge carriers in whole channel. In some cases, the trapped surface charge and ionized dopants could assist with gate voltage together to influence charge transfer properties of the device channel [16, 18]. Therefore for further understanding of how nanodevices work, not only conventional electrical characterisation but also microscopic observation of device structure would provide useful information. In particular, if there is a way to measure the potential distribution and randomly distributed charge in the SiNW channel it could facilitate the understanding of SiNW devices behaviour.

The Kelvin Probe Force Microscopy (KPFM) is an ideal tool to map surface potential with high sensitivity and lateral resolution. It was born in IBM T. J. Watson Research Centre in 1991 [19]. At the beginning it is able to distinguish 50 nm feature size minimum 0.1 mV potential variation [19]. In the short time after the KPFM's resolution is improved into atomic level [20, 21, 22, 23]. However only few KPFM studies are related to electronic devices. The purpose of this project is to relate high quality surface potential image to the electric characteristic of SiNW devices and then to understand the effect of nanoscale local surface potential distribution on the electrical characteristics of silicon nanowire devices by looking at the build-in potential change, strength of lateral electric field (E_x), and width change of space charge region under different biasing condition. In this project, the KPFM equipment is modified to supply bias to the devices and the measured devices is specifically designed, *e.g.* PtIr coated sharp Nanosensor ATEC tip to improve both quality and lateral resolution of KPFM scan, fully and uniformly doped SiNW to test the accuracy of KPFM measurement, ultra thin SOI for fully depletion operation and enable to see the potential change from the top scan, side/back gate structure for the accessibility to the channel of devices by KPFM tip.

This thesis is organized as follows. In the following literature review chapter, two very important terms in this project, SiNW devices and KPFM technology are featured. The up-to-dated development of those technologies will be reviewed. Development of SiNW devices will be reviewed from three different application aspects: field effect transistors for LSI, chemical and biological molecular sensors, and single electron transistors for quantum information technology. For the KPFM technology the review will start from the historical development and technological progress part are reviewed first and then

some recent attempts related to electronic devices are introduced. My motivation of this work is shown with respect to the recent trend of this research area. Chapter 3 will introduce the relevant theory which is used in this PhD project. The relevant theoretical background on the silicon nanowire device operation and KPFM measurement is described in this chapter. In the SiNW devices part, charge carriers transport properties in planar, SiNW, and single electron transistor are learned. The experiment result will be presented in the flowing three chapters. The local resistance and trapped surface charge characterisation in exposed silicon-nano-wire (SiNW) by KPFM will be shown in Chapter 4. The charge redistribution and charge transport in multiple n-p-n structure are studied by both simulated and KPFM scanned surface potential mapping in Chapter 5. So far the position of metallurgical p-n junction and change in depletion width under gate modulation has been successfully observed. In Chapter 6 the low temperature coulomb oscillation and room temperature surface potential mapping of fabricated doping modulated side gate n-p-n-p-n SiNW SET is illustrated. The results obtained strongly suggest that the KPFM is able to applied for the characterisation of nano FET and SET devices. The final conclusion will be made in the last chapter.

Chapter 2

Literature Review

2.1 Introduction

The conventional planar CMOS devices are near their scaling limitation while multiple gate and SiNW transistors demonstrate superior advantage against the channel effect. The multiple gate structure has already been employed for fabricating high performance and low power consumption digital signal processor. The multiple gate FET is claimed having higher scalability than planar structure and ideal subthreshold slope. However problems, for example threshold voltage and current variation [24, 16] and influence of impurity atoms [25], in SiNW devices are noticed and it is believed that the quantum effect would finally prevent further scaling. Here in this chapter the development of multiple gate devices is reviewed to identify their advantage and limitation from different aspects. Because the single electron transistor could be the ultimate solution the SiNW based single electron transistor will also be reviewed.

As the size of SiNW devices is shrunk into nano scale, nanoscale imaging of local device structure becomes more important in order to fully understand the characteristics of devices. Except for the electron microscope technology such as scanning electron microscopy (SEM) and transmission electron microscopy, the SPM technology is able to derive various physical information with high special resolution. In particular KPFM is the technology to be able to observe the local potential variation of the channel in SiNW field effect transistors [26].

The literature review in this chapter is separated into two main parts. The first part focuses on the history of development of the SiNW devices and introduces their advantages and problems. The second part is dedicated to reviewing the development of the KPFM technology and its application for device imaging. The SiNW devices are reviewed by application categories: multigate SiNW transistors, SiNW sensors, and single electron transistors. The KPFM technology will be discussed from its first invention

to final improvement. The following description concentrates on applications relevant to characterisation of specific materials, then applications on nanoscale devices. The motivation of this project is shown in Section 2.4.

2.2 Silicon nanowire devices

2.2.1 Multi-gate/GAA SiNWs for Advanced CMOS

Various critical problems are reported on scaled planar MOSFETs. When MOSFET channel length goes into less than 100 nm, the short channel effect (SCE) emerges [13]. Further scaling down to less than 25 nm causes further serious problems. Firstly the reduction of the operational voltage results in the demand for thinner insulator thickness (few Å) to maintain same level of charge density in the conductive channel [27] meanwhile the thinner (<2 nm) insulating layer causes larger gate leakage current [28]. In addition it raises up the ratio of the operation voltage to the thermal voltage, so that thermal diffusion of electrons increases source-drain (S-D) leakage current [13]. Consequently standby power consumption becomes larger. Furthermore scaled planer CMOS requires more complicated and strict doping profile for precise control of the energy barrier height and depletion length in device operation. Non-uniform doping is required for 25 nm CMOS technology but the SCE cannot be solved even with the advanced doping-profile control [29]. These issues prevent to further scaling planer CMOS from going under 25 nm technology.

The multi-gate devices started from double gate FET [30, 31, 32] (Figure 2.1(a)) in 1990s and have shown immunity to SCE and high scalability. Generally it can be scaled down less than 20 nm because of the following reasons. As was pointed out by Suzuki *et al.* [32] the double gate FETs show steep subthreshold slope, high transconductance, and short channel immunity. These features are caused by full depletion and both side inversion [30] instead of surface inversion/depletion in the planar MOSFET. It also means the gate has better control over the channel.

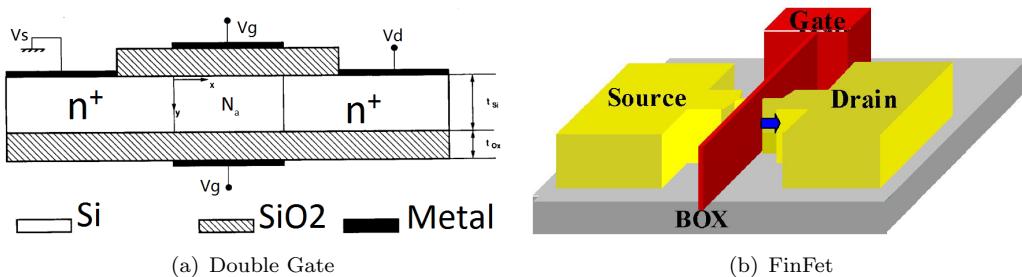


Figure 2.1: multi-gate FET (a) Double Gate FET. back gate is based on SOI BOX layer [32] (b) FinFET device. gate is wrapped on SiNW channel except back side

Hisamoto *et al.* [33] revealed that the double gate FET suppressed SCE however also showed that its fabrication was complicated and its threshold voltage control was not easy. New structures called FinFET [33] (Figure 2.1(b)) and Gate-All-Around (GAA) FETs [4, 6] were developed to solve problems in double gate FETs. To fabricate the FinFET the Fin structure is firstly defined on a Si wafer and then poly Si is deposited around the Fin structure as a gate electrode [33]. In Hisamoto *et al.* report the smallest FinFET with the feature size of 17 nm was fabricated [33]. In the GAA FET fabrication process the FET channel is made suspended on SOI first and then the gate electrode is wrapped all around the channel [4].

The FinFET/GAA structure is successful not only because of its compatible fabrication but also of its high device performance [30, 33, 4, 6]. Singh *et al.* [4] reported that their fully depleted GAA SiNW showed almost ideal subthreshold slope (~ 63 mV/dec) and low DIBL (~ 10 mV/V), and high I_{on}/I_{off} ratio ($\sim 10^{16}$) (Figure 2.2). The subthreshold slope in conventional MOSFETs is larger than 80 mV/dec while an idea value is 60 mV/dec at 300 K. The high performance contributed by fully depletion of FET channel [4].

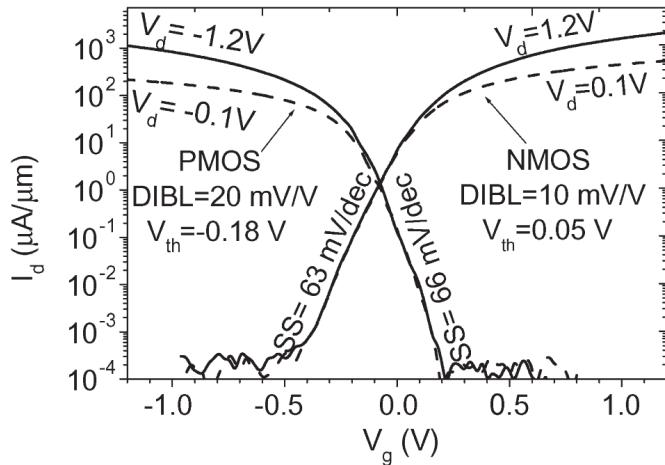


Figure 2.2: High performance GAA SiNW FET I_d - V_g curve [4].

The operation of conventional MOSFETs heavily depends on modulated doping profile along the channel and the gate voltage to control the current flow in the channel. However as the channel length of devices shrinks into 25 nm the junction doping modulation may not be easily built up due to hard controlability of the position of individual impurity atoms in such a small size [13]. An idea of junction-less transistors was proposed by Colinge *et al.* [6]. The junctionless transistor consists of a Si nanowire channel and multiple gates but instead of using doping modulation in the MOSFET channel, uniformly doped source, channel and drain structures are used. The key point for the junction-less FET is that the SiNW should be thin enough to be able to be fully depleted. Colinge *et al.* [6] mentioned the full depletion also happened even for the SiNW with the doping concentration of 1×10^{19} cm $^{-3}$ doped SiNWs and also ideal SS slope would be expected.

Due to its simple structure and easy fabrication process this structure is considered as an alternative transistor after the 25 nm era.

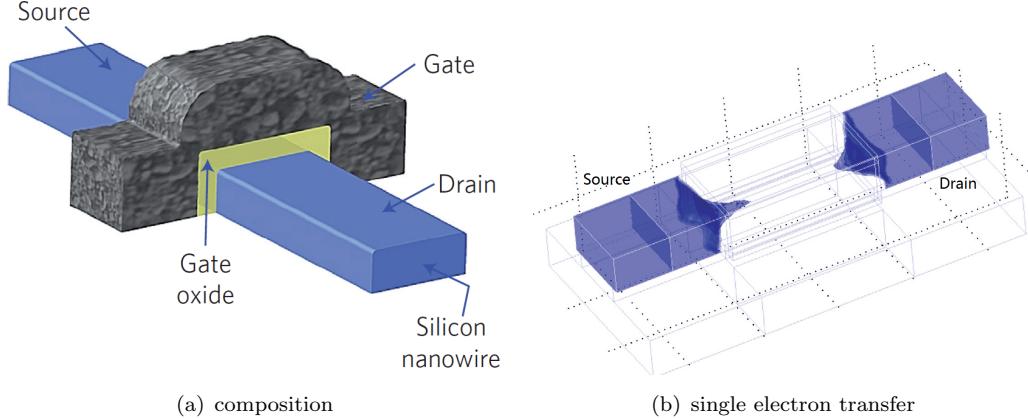


Figure 2.3: Junction-less transistor (a) Structure. Body of transistor is made of uniformly doped SiNW and the gate electrode is wrapped around it. (b) Depletion of SiNW. No need for junction the gate electrode fully deplete SiNW so that current is pinch-off [6].

The multi-gate FETs now in production in industry, however, when the size of device shrinks further, serious issues in relation to individual dopants are also to be considered. In highly-scaled devices, the number of dopants in the channel of the devices is significantly reduced. In a 1- μm long channel the number of dopants is a few thousands while in 32-nm-long channel the number is largely reduced down to only less than 100 (Figure 2.4) [34]. In the long channel device, we only need to consider the impurity concentration that determines the resistivity of the channel and how the channel is formed by gate voltage. On the other hand, in the highly scaled devices, this simple consideration is no longer valid. So, we must take account of the dopants individually, i.e. not only the number but also the position of the dopants should be considered. As the number of reports suggested dopant distribution in the device channel is one of the reasons for large variation of the threshold voltage [16, 34, 35, 36]. The standard deviation of the threshold voltage related to the stochastic variation of the number of dopants in the depletion region is estimated by Equation 2.1 [24]

$$\sigma V_t = \frac{1}{3} \frac{t_{\text{ox}}}{\varepsilon_{\text{ox}}} \sqrt[4]{4q^3 \varepsilon_{\text{si}} \psi_b} \frac{\sqrt[4]{N_B}}{\sqrt{W_{\text{eff}} L_{\text{eff}}}} \quad (2.1)$$

Where $\psi_b = (k_b T/q) \ln(N_B/n_i)$ is the potential difference from the Fermi level to intrinsic Fermi level caused by doping, t_{ox} is the thickness of insulator layer. ε_{ox} and ε_{si} is permittivity for silicon oxide and silicon respectively, N_B is the doping concentration. W_{eff} , and L_{eff} are the effective length and width of channel respectively. Equation 2.1 suggests that the threshold variation would become larger when the channel is shorter and the doping concentration is larger.

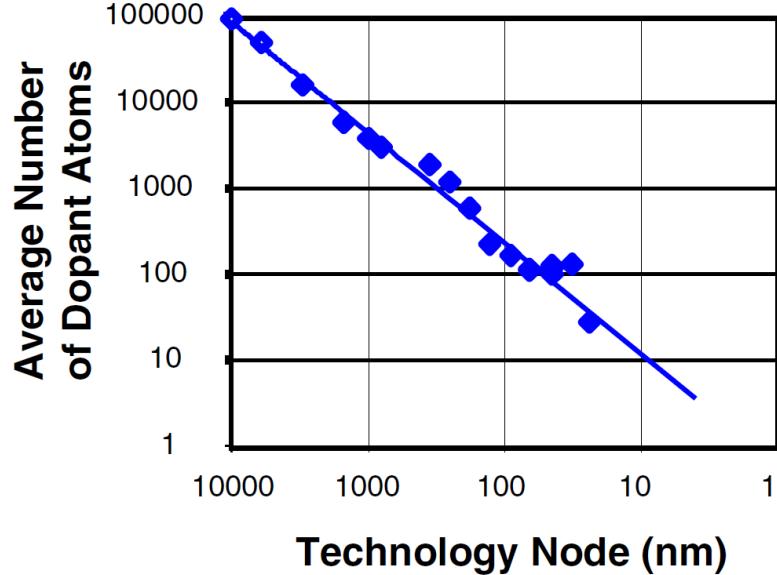


Figure 2.4: Dopants number in FET channel as node size [24]

Shinada *et al.* [16] reported that the regularly distributed dopant array in a FET channel showed high capability to suppress the variation of threshold voltage. Assuming the same number of dopants in comparison, the device with the regular dopant array shows narrower threshold voltage variation whereas large threshold voltage variation is observed in the channel with randomly distributed dopants as shown in Figure 2.5. The reason is attributed to difference of the potential valley distribution induced by the ionized dopants in bulk silicon. The potential distribution determines conduction properties of the channel. While the periodically distributed dopants cause better stability of the threshold voltage, randomly distributed dopants either enhance or suppress local conductivity therefore the global threshold voltage is increased or reduced so that the variation becomes larger.

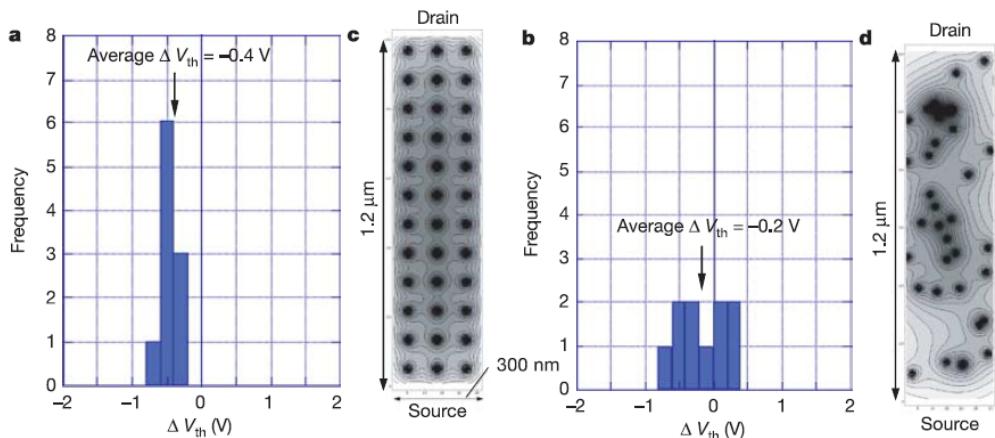


Figure 2.5: Dopants array suppress threshold variation dopants induced potential valley [16].

In addition, the sub-threshold current in the FET with the nanoscale channel length is

also found to be related to individual dopant atoms distributed in the channel. In nano devices the tunnelling effect will become more significant. The sub-threshold current could be increased by resonant tunnelling which happens on coupled dopant atoms in the source and drain regions. In those devices the dopant atoms act as stepping stones which allow electrons tunnelling through them at room temperature as demonstrated by Pierre *et al.* [36]. In their simulation only a few dopant atoms are presented in the 30-nm-long FET channels, however, the measured three devices at room temperature show different sub-threshold characteristics as shown in Figure 2.6. This behaviour has been later confirmed by the low temperature resonant electron tunnelling measurement [36]. Each tunnelling peak represents the ionisation energy of individual dopants. The ionisation energy difference could explain the variation of sub-threshold behaviour. It is noteworthy that the ionisation energy is related to how far the dopants are away from the gate dielectric material. Dopants just under the gate dielectric material tend to have large ionisation energy [37].

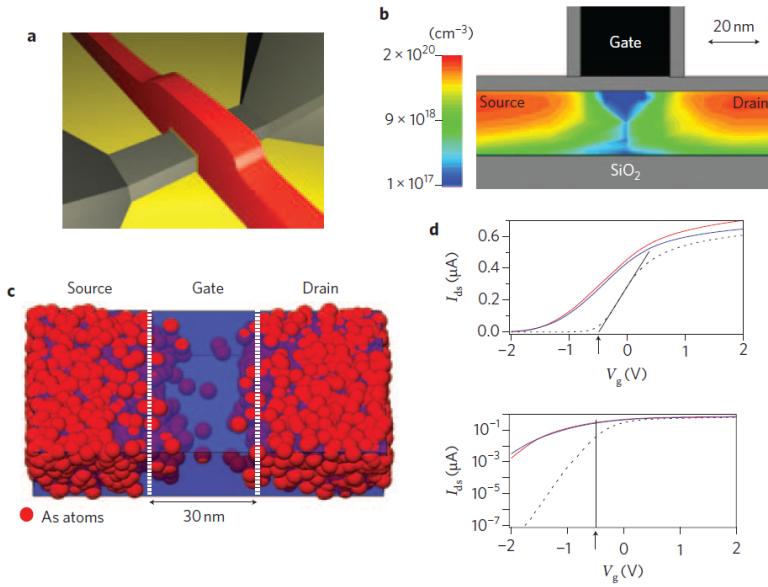


Figure 2.6: Dopants in nano-FET and its sub-threshold current curve [36].

To sum up, the physical limitation makes planar MOSFETs difficult to be scaled down to 25 nm. Thanks to 3D multi-gate/GAA technology the silicon CMOS devices can go along with the Moore's Law. However, characteristics of multi-gate FETs SiNW have not been fully studied. As the size of devices becomes much smaller, electrical characteristics of the devices become more sensitive to the local physical parameter variation such as impurity atom distribution, surface charge distribution, and surface roughness. Therefore in order to get insight to improve the performance of SiNW devices the local physical parameter characterization of multi-gate SiNW devices is very important.

2.2.2 SiNW for sensing applications

The channel conductance of FETs is well modulated by the gate bias which is capacitively coupled with the channel. This suggests that any capacitive coupling to the channel could affect the channel conductance. For logic MOSFET application the trapped charge should be minimized to avoid any degradation of MOSFET performance. On the other hand, we can use this high sensitivity of the FETs for sensing application.

Cui *et al.* have demonstrated that the SiNW sensor shows high sensitivity and selectivity to biological and chemical species [9]. The high sensitivity is contributed by high surface volume of SiNW channel. The high selectivity depends on the surface modification. An example in Figure 2.7(a) shows pH sensing where both NH_2 base and SiOH base play an important role to sense H^+ . Stepwise change of the conductance of the SiNWs was demonstrated with changing pH of the solution (Figure 2.7(b)). By changing the attached molecules the SiNW FET can be various sensors such as gas sensors [38], DNA sensors [39], medical sensors [7]. The reported sensitivity has been drastically improved from 10 nM in 2000 [9] to and recently minimum 10 fM [8].

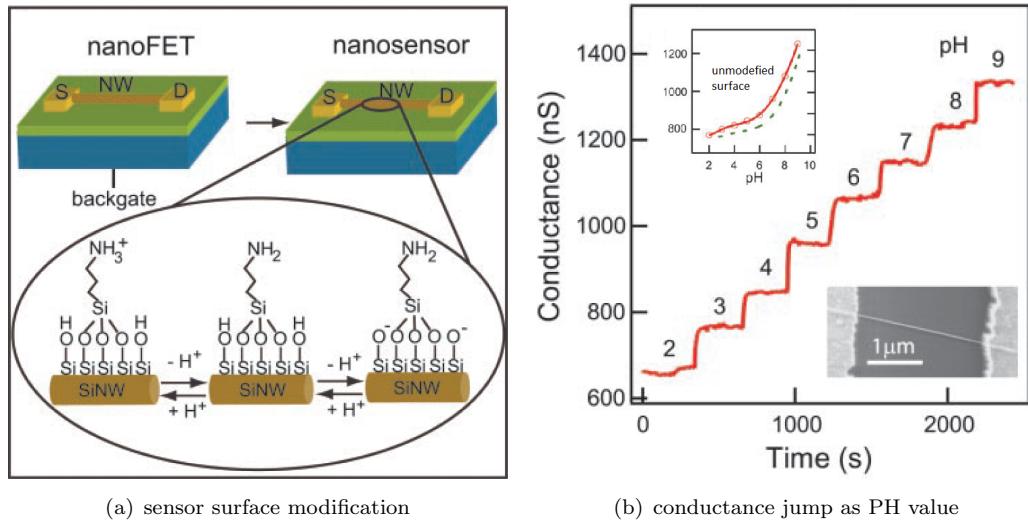


Figure 2.7: SiNW sensor construction and testing result (a) surface modification on SiNW FET. The attached molecule is targeted to H^+ ion (b) The transconductance change response to the change of pH value. Top left insert is conductance change to pH change for unmodified devices. The conductance response to the H^+ concentration change quickly [9]

The fabrication of SiNW sensor was started from the bottom-up technology [9], where the SiNW was grown by Chemical Vapor Deposition (CVD) with metal catalyst. After that the SiNWs dispersed in solution are located on to insulator substrate by spin coating or fluid flow assisted technology [40]. And then the electrodes are fabricated with respect to the position of the NWs. The advantages for this method are low cost, size uniformity, and good crystal quality. However the position of SiNWs cannot be

controlled precisely. To lower the fabrication cost, SiNW based on polycrystalline thin film was developed and their high performance was reported [7]. However, to achieve relatively lower cost and high performance and high-level integration at the same time, the best way is to use top-down silicon device fabrication technology.

Recently multiple-gate SiNW FETs are being investigated for sensing applications. The early SiNW sensors were gated only from the backside, showing weak controllability of the threshold voltage of the FET, and therefore the sensitivity was limited. In order to enhance the sensitivity of SiNW sensor, Ahn *et al.* proposed a double-gate structure (Figure 2.8(a)) [41] measured threshold voltage shifts are illustrated in Figure 2.8(b). An improvement is made that when V_{G2} is set larger than the threshold voltage of the double-gate sweep, even a small amount of immobilized charge could shift the threshold voltage of the V_{G1} sweep significantly therefore the sensor's sensitivity is dramatically enhanced. It also means the sensitivity of double-gate SiNW sensors is tunable.

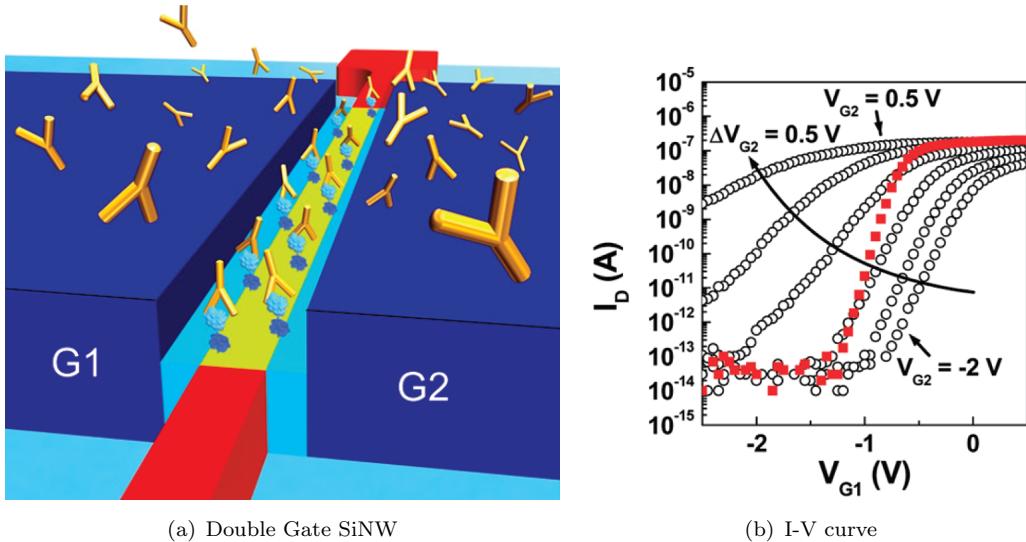


Figure 2.8: Double gate SiNW sensor and tunable threshold voltage curve (a) Double gate SiNW sensor structure. The gate is positioned at both left and right side and the top side of SiNW is functioned for sensing purpose (b) Measured tunable threshold voltage effect by double gate. G1 voltage is continuously swept and G2 is changed step by step. Significant threshold voltage shift can be seen after V_{G2} bigger than its threshold voltage [41].

Although Ahn *et al.*'s double-gate devices present tunable sensitivity successfully, their sensors only use the top side of the SiNW. To enhance the sensitivity an idea of the suspended double-gate SiNW sensors was proposed [8]. The full expose of the surface of the SiNW will largely increase the sensitivity thanks to the larger ratio of the surface to volume of the SiNW. Under an appropriate condition, it was claimed that this suspended sensor could have 20 times higher sensitivity than previous non-suspended ones [8].

This is an interesting result but switching characteristics are not consisted with what was predicted by simulation. It might be interesting if we could measure the surface

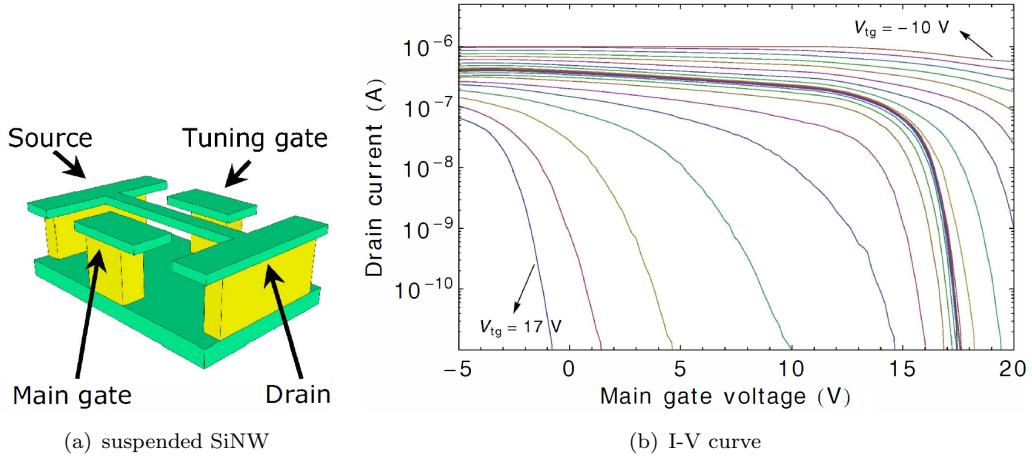


Figure 2.9: Suspended SiNW sensor and its electrical characteristics. (a) Suspended structure. Double side gate is air isolated from channel and bottom of SiNW is released from SOI (b) Tunable threshold voltage by tuning gate [8].

electrical potential directly and make a comparison with electrical characteristics of the devices.

To sum up, in developing SiNW devices for sensing applications, many effort has been made to reduce the fabrication costs and to improve their performance. The bottom-up technology enables us to achieve very thin nanowires but has difficulty to control the position, indicating yet to be suitable for mass production. double-gate structure is appeared to be useful in order to control the threshold voltage of the SiNWFETs and then to enhance the sensitivity. The idea of suspended SiNW sensors could ultimately explore the potential of high sensitivity. Mapping the surface potential distribution on SiNW will be also helpful to optimise the device structure and to understand the sensing mechanism of molecules.

2.2.3 Si single electron transistors

Once the conventional transistor finally encounter its physical limitation, a novel device, the single electron transistor could be an elementary device in future IC due to the extremely low operation current. Various kinds of applications of SETs have been investigated such as the voltage state logic, charge state logic, a few electron memory, and electron static charge memory [42]. The SET is not only considered as a substitute of the conventional FET logic devices but also a ultrasensitive charge sensor which will be applicable for quantum information processing. The quantum computer is believed to be more powerful than the current binary solid state computer because of using the superposition of the quantum states. A advantages of silicon-based quantum information devices are long phosphorus nuclear coherence time in Si, compatibility while current

advanced semiconductor fabrication technology, *etc*. However again the random dopant distribution would affect the performance of the Si-based single electron devices. [11, 43].

The world first single electron transistor was born in Bell Laboratories in 1987 [44]. The SET shows different behaviour from conventional FETs. As increasing the gate voltage the conductance shows oscillating behavior with a certain period rather than monotonic change (Figure 2.10(b)). The first SET was based on metal and the structure is illustrated in Figure 2.10(a), where tunnel junctions are induced by the overlapped electrodes.

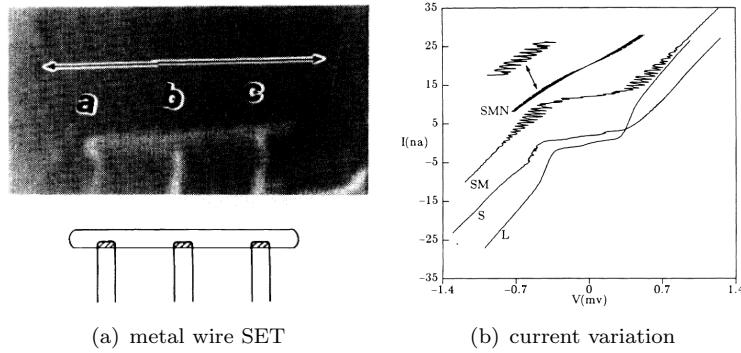


Figure 2.10: world first single electron transistor and measured current curve. (a) three junction single electron transistor. a,b,c is the position of junction made by electrodes vertical overlap. (b) nonlinear current change as function of voltage at low temperature. [44]

Similar conductance oscillation behaviour was found in a narrow channel MOSFET at low temperature by Kastner *et al.* [18]. A narrow 70-nm-wide Al gate was fabricated to induce 1D electron gas in MOSFET to study the conduction resonance behaviour at low temperature (Figure 2.11(a)). This conductance fluctuation was explained by the theory of the electron resonant tunnelling. The resonance takes place in the presence of localized states along the MOSFET channel and electron path shown in Figure 2.11(b). The period of the tunnelling events depends on the position of the local states and the channel length. The observed random resonance period (Figure 2.11(c)) was the outcome of the overlap of individual resonances [18].

Based on the discovery described above, Scott-Thomas *et al.* developed the first semiconductor SET in 1989 [45]. Later Kastner *et al.* found that the resonance period is not reproducible and also changes from at room temperature to low temperature [46]. This was considered to be a common phenomenon after confirmation by many similar experiments. Then Kastner *et al.* suggested that the change of frequency was due to the change of the number of the trapped charges which induce potential barrier in the MOSFET channel (Figure 2.12(a)) [46]. In each cycle the position of trapped charges would be changed so that the period is changed. On the other hand, the device with the gate defined two potential barrier is fabricated as shown in Figure 2.12(b) shows good reproducibility of the resonant frequency.

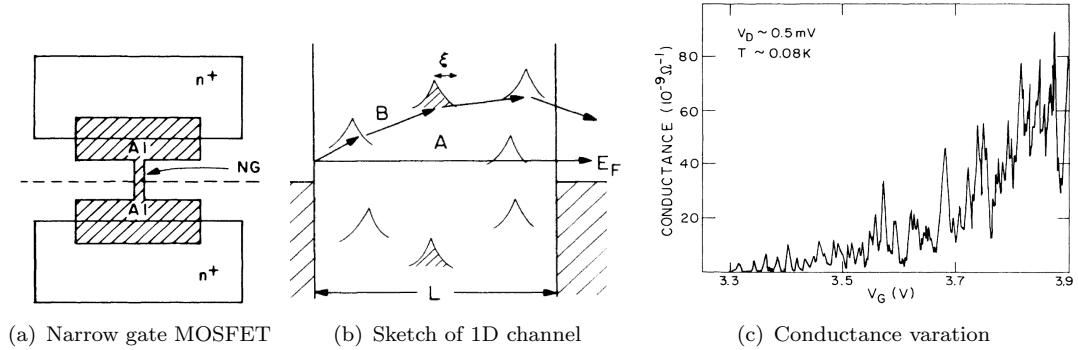


Figure 2.11: Conductance variation in narrow gate MOSFET at low temperature. (a) structure of narrow gate MOSFET. 1D narrow inversion layer is defined by Al gate electrode. (b) Sketch of 1D MOSFET channel, localized states and electron path. Path A electron resonant tunneling, Path B phonon assisted tunneling. (c) The electron current various as gate potential (electron Fermi energy) [18]

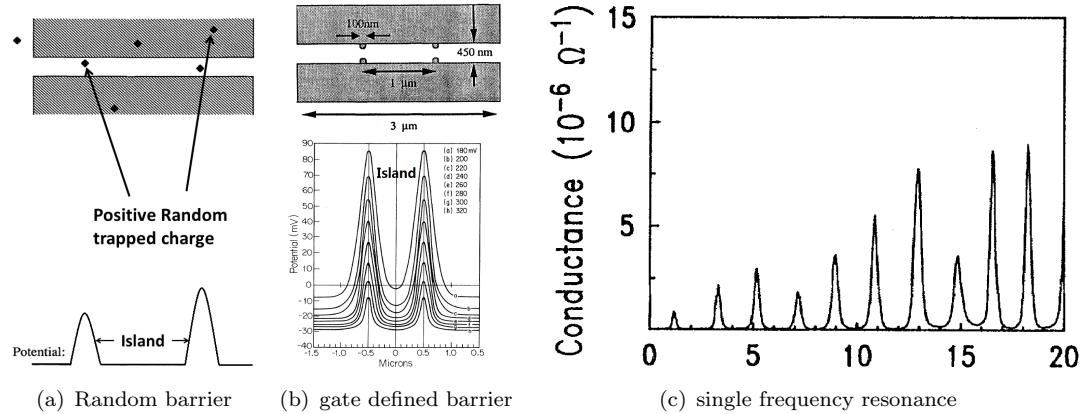


Figure 2.12: Potential confined SET island (a) random surface charge and its induced confined potential well (b) intentionally fabricated gate electrode (top view) and confined potential well as change of gate voltage. The distance of this potential determine resonant period (c) The measurement of conductance as function of gate voltage. [46]

Previous studies show the SET devices should be operated at extremely low temperatures ($\sim 1\text{K}$) and its size is normally larger than 100 nm. The other studies demonstrate that the operation temperature depends on the size of the coulomb island and is closely related to the ratio of the electron coupling and thermal energy. Likharev pointed out that if the SET behaviour was needed to be observed at room temperature the island size should be smaller than 10 nm [42]. Obviously it is not easy to control the characteristics of scaled SET devices in particular due to large influence of randomly distributed surface charges, resulting in unwanted potential barriers for electrons [46]. Not only the trapped surface charges but also the impurity atoms play an important role in SET to build unintentional potential barriers [47].

The SET shows great advantages to construct quantum information devices and also possible low power consumption binary logic devices. In order to get high operation temperature the size of the Coulomb island in the SET should be as small as possible. To construct an SET, the tunnelling barrier is one of the key components. However as the SET is in the small size, the tunnelling barrier is fragile. Ionized impurity atoms play an important role in nano scale devices. Studying the surface potential distribution is surely helpful for deep understanding and performance improvement of SET devices.

2.3 KPFM technology

The KPFM is a tool to draw a map of the surface potential of materials with high lateral resolution of down to atomic level and high sensitivity of the surface potential (~ 5 mV). It is widely used for characterising materials or molecules. Recently it is also applied to the investigation of doping profile, potential distribution, surface defects, even individual impurity atoms [48]. The following sections introduce the development of KPFM technology and relevant investigation on electronic devices via KPFM.

2.3.1 Brief history: from STM/AFM to KPFM

The invention of Scanning tunnelling Microscopy (STM) in 1982 [49] was a dawn of nanotechnology. It allows the three dimensional atomic level investigation of the surface of materials and also manipulation of individual atoms. The resolution of STM is better than Scanning Electron Microscopy (SEM). The height resolution is based on the high distance sensitivity of tunnelling current (stabilized at the distance of 0.2 Å), which is three orders of magnitude larger than tip-sample distance change. The first STM demonstrated the highest resolution of 2 Å in height and 1 μ m in lateral. Binnig *et al.* [49] reported that lateral resolution was improved by significant reduction of tip radius. In the following year the atomic lateral resolution on (111) Si surface was reported by the same group in IBM Zurich Research Laboratory (Figure 2.13(a)) [50]. This was the first time people have observed individual atoms arranged on material's surface. Except for the observation of the atom arrangement, the STM was later applied for manipulating individual atoms to assemble the quantum corrals [51]. Importantly STM is also used to assemble single atom transistor by positioning individual dopant atom in an FET channel [52].

The STM is only able to measure surface topography change in relation to the change of tunnelling resistance, therefore the measurement ability of STM is restricted by the conductivity of specimens. To solve this problem the tunnelling current is then substituted by the other distance sensitive signal which is called the atomic force. Combining STM with stylus profilometer technology, the Atomic Force Microscopy (AFM) was then

developed in 1986 by the same group in IBM [53]. The AFM is able to work in the air. The first AFM image shows vertical resolution of less than 1 Å and lateral resolution of 30 Å. The AFM's resolution is soon improved into atomic level [54, 55] (Figure 2.13(b)). The image of the atom arrangement on the Si (111) surface was taken by AFM.

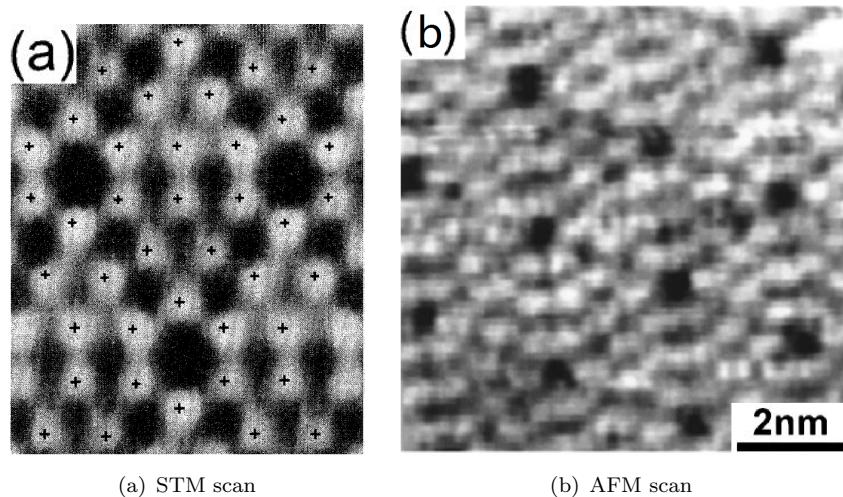


Figure 2.13: Atomic resolution STM and AFM scan on 7×7 Si (111) surface
 (a) STM scan, the brightness indicates altitude and the cross mark points the atoms position [50] (b) AFM scan, similar atomic arrangement information as in STM image [55]

The AFM is a kind of force sensor with the sensitivity as small as 10^{-18} N. By choosing an appropriate tip, AFM is easily expanded to multiple microscopic force sensing application such as magnetic force microscopy (MFM) [56], electro-static force microscopy (EFM) [57], and Kelvin Probe Force microscopy (KPFM) [19]. Those group of STM/AFM based microscopy are called Scanning Probe Microscopy (SPM). With proper force modulation technology, SPMs are able to measure both topography and physical quantity simultaneously. It has been used also for device characterization to study charge state of quantum dots, and potential distribution on FET channel.

For the purpose of studying electrical properties the high resolution Electric Static Force Microscopy (EFM) was developed [57]. Martin *et al.* [57] reported that the capacitance force microscopy is able to detect electric force smaller than 10^{-10} N and minimum capacitance 8×10^{-22} F. Stern *et al.* [58] pointed that this Force Microscopy is assumed to be able to detect charge in order of 100 electrons. Afterwards, detection of single charge carrier on insulator by Force Microscopy was reported by Schönenberger and Alvarado (1990) [59]. The coupling capacitance change in nano-scale could significantly vary device parameters or even dominate devices characteristics.

The EFM is sensitive to the electric static force however this static force is not only decided by the surface charge state/potential but also the capacitance between the tip and sample. The capacitance depends on dielectric material which covering sample

surface and also on the tip-sample distance. Therefore quantitative study of the surface potential of the sample is difficult with EFM. To solve this problem the Kelvin Probe Force Microscopy was developed [19]. By combining the EFM and Kelvin measurement method, the signal originated from the surface potential can be accurately extracted in KPFM. The first KPFM is demonstrated to be able to detect potential difference of 0.1 mV with the lateral special resolution of smaller than 50nm.

2.3.2 Development of KPFM technology

2.3.2.1 Doping profile measurement

Determination of doping profile in devices is of paramount importance to understand the device operation, in particular nano-scale SiNW devices. Typical method to study the doping profile are the secondary ion mass spectroscopy (SIMS) [60], spreading resistance profiling (SRP), and scanning spreading resistance microscopy (SSRM) [61]. While those methods are lack of lateral special resolution, KPFM is advantageous with high lateral resolution doping of detecting profile.

The KPFM is designed to measure the CPD (contact potential difference) change between the tip and sample surface with high lateral resolution. The first KPFM measurement result is shown in Figure 2.14 [19]. In the left-hand-side AFM image the height step is consistent with the fabrication process where Pd thin film was evaporated on the Au substrate. The shape of potential step in the right-hand-side image is also delicately matched with the sample topography contour. This is the concrete evidence that the CPD is associated with the work function of various materials.

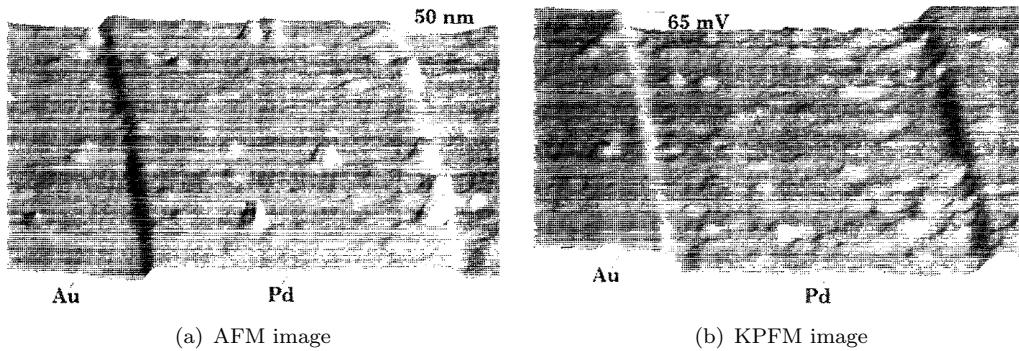


Figure 2.14: First literature KPFM measurement of CPD contrast on metal film (a) AFM image for 50nm Pd metal film on Au (b) CPD image for Pd film on Au for 65mV contrast and small local variation can be seen [19]

However, the quantitative study of CPD in two different materials by KPFM is difficult. In literature the work function is in between 4.68 and 6.24eV for Au [62] and 4.64 to 5.4 eV for Pd [63] while the measured CPD is 65 mV. The decay of CPD was reported in Ref. [64], where the 65 mV difference was reduced to 35 mV after four days. This was

attributed to the adhesion of bipolar molecules especially water molecule, these results suggest that KPFM image is severely affected by the surface condition of the sample.

Effects of water molecule layers on KPFM were investigated by Sugimura *et al.* [64]. Their experimental result is shown in Figure 2.15. The p- and n-type doping patterns were made as a square array which was prepared on the n-type wafer with the P doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$. For the purpose of hydrophilic surface preparation, about 2-nm-thick, was grown on the sample surface so that the contact angle of almost 0 degree against water was achieved. No CPD contrast can be observed in the high relative humidity (RH) environment in KPFM measurement while clearly 50 mV difference was observed on the sample in nitrogen environment after annealing at 100 °C. This experiment demonstrate clear evidence of shielding effect by addition of bipolar molecules. In other words, the CPD measurement via KPFM is easily impacted by the surface condition. Quantitative evaluation of the magnitude of the CPD shift by water molecule adsorption has not been reported yet.

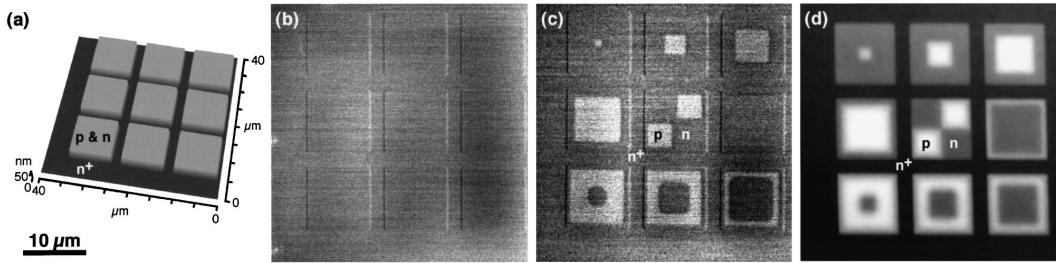


Figure 2.15: CPD shield by water molecule layer (a) height image of sample surface (b) CPD measurement for sample expose in 54% RH, no CPD contrast. (c) CPD measurement taken after 3h 100 annealing in air. (d) measurement in $< 0.6\%$ RH nitrogen [64]

An attempt for quantitative two-dimensional surface doping profile analysis has been made by Henning *et al.* [65]. In their report the measured potential value was expressed by

$$U_{DC} = (E_c - E_f)_{\text{tip}} - (E_c - E_f)_{\text{substrate}} . \quad (2.2)$$

This equation is valid only if the tip material is the same as that of the sample surface. The actual measured potential difference between two different doping region is independent of the tip-sample CPD because the surface potential of the tip is used as the standard reference level. However in Henning's measurement the result of build in potential in p-n junction was small than theoretical calculation (Figure 2.16). The reason of scaling effect has not been explained clearly. It would be caused by perturbation of the stray capacitance between the cantilever tip and sample surface and also due to the surface condition. The scaling effect is the common problem of the quantitative analysis of doping profile from the KPFM measurement results. In the other p-n junction

investigation by KPFM the potential difference in between was 130 mV for the junction formed by thermal diffusion process and 260 mV for that by ion implantation process [66]. In that study the doping concentration should exceed $1 \times 10^{20} \text{ cm}^{-3}$ and the CPD contrast should be larger than 800 mV. To sum up, KPFM is able to probe the difference the surface potential but quantitative doping profile by KPFM is a challenge work.

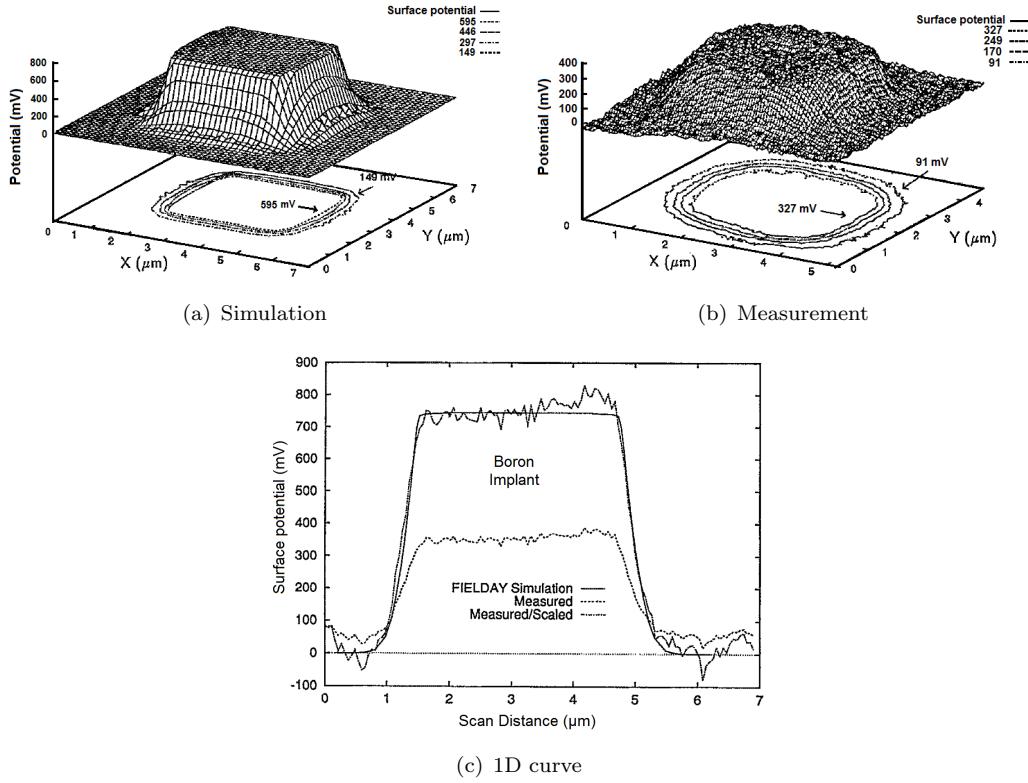


Figure 2.16: 2D doping profile analysis by KPFM. (a)FIELDAY simulation using Gaussian-derived dopant profiles. Over 800 mV difference for doping profile change (b)Actual KFM measurement result. Only ~ 350 mV difference can be observed. (c)1D curve comparison between simulation and scaled measurement value. The transition edge is acceptable [65].

A dipole model was build by Baumgart *et al.* in Figure 2.17(a) to explain scaling factor [67]. Baumgart *et al.* [67] proposed that the dipole which is induced by sample surface states and resulting minority charge carriers injecting into sample surface. During the KPFM measurement the overshoot DC bias is required to cancel the charge injection therefore the KPFM does not record the actral workfunction difference between tip and scanned materials. As result the work function difference in KPFM result which was suggested by Nonnenmacher *et al.* [19] was then replaced by $[E_c - E_f(n)]/e$ for n-type and $[E_v - E_f(p)]/p$ Figure 2.17(b). In this situation the real KPFM measured value is instead by the potential difference between conduction band to Fermi level in n-region and Fermi level to valance band in p-region separately. By using the KPFM correction model, the KPFM measured CPD result for $N_a = 2 \times 10^{16}$ $N_d = 2 \times 10^{17}$ p-n junction

should be 310 mV which is consistent with measured value 300 mV [67]. Referring to the measurement in Ref. [65] (Figure 2.16(c)) this model is applicable.

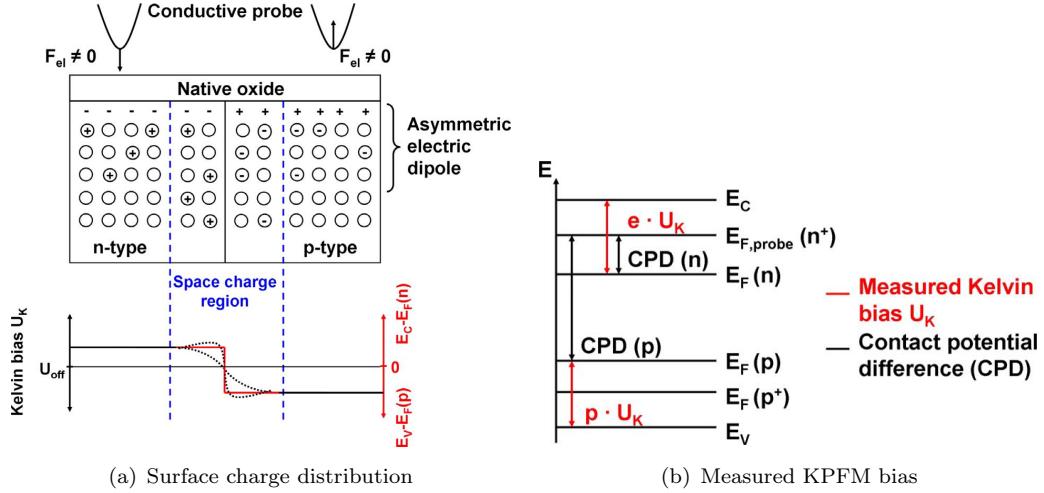


Figure 2.17: Charge distribution at near surface and KPFM measured bias
 (a) Tip-sample interaction force F_{el} caused by amount of mobile charge is trapped on surface and same amount un-screened ionised dopants at near surface. This amount trapped surface charge is caused by CPD between and sample. In measurement the F_{el} is eliminated by injecting majority charge (b) The measured KPFM value compare to CPD [67].

The doping profile measurement results shown above suggest that to quantitative detect doping profile variation by KPFM equipment will heavily depends on sample surface states. Both Baumgart's [67] and Henning's *et al.* [65] doping profile studies were carried in ambient environment. The measured CPD value along doping profile change could also be affected by attraction of charge molecules from atmosphere. The vacuum measurement [23] can be suggested to improve the accuracy of CPD measurement.

2.3.2.2 Nano-scale doping profile mapping

While the macroscopic doping concentration is a principal parameter for large scale p-n junctions as discussion in section 2.2.1 in nanoscale devices, the variation of devices parameter will depends on uniformity of doping profile random distribution of individual dopants affects the key device parameters such as the threshold voltage [16]. Even though the conventional KPFM detection method is claimed to be able to detect doping profile with high lateral resolution, the nano scale doping profile measurement is a big challenge work. In other words, the CPD does not change if doping profile change in short range due to free carrier screening [68, 69, 70, 48]. The screening length can be derived by solving the following Poisson equation, [69]

$$\frac{d^2\psi_i}{dx^2} = -\frac{q}{\varepsilon_{si}}[N_d(x) - n_i e^{q(\psi_i - \psi_f)/k_b T}] , \quad (2.3)$$

$$\frac{d^2(\Delta\psi_i)}{dx^2} - \frac{q^2 N_d}{\varepsilon_{si} k_b T} \Delta\psi_i = -\frac{q}{\varepsilon_{si}} \Delta N_d(x) , \quad (2.4)$$

Where the ψ_i is potential change induced by net charge, ψ_f is Fermi potential, x is the screening length which defines the diffusion length of free charge carriers. The solution is

$$x = \sqrt{\frac{\varepsilon_{si} k_b T}{q^2 N_d}} . \quad (2.5)$$

The doping variation that happens within this length is not detectable without depleting free charge carriers [70, 48].

The nano-scale doping profile has been observed by scanning transmission electron microscopy (STEM) [71] and STM [72] (Figure 2.18). However both technology has its limitation. The STEM technology requires specific sample preparation including ultra thin (<5 nm) contact-less film and small thickness variation. Therefore it would be difficult to characterise the device structure without any damage. On the other hand, STM is a non-destructive measurement but is only able to detect atoms near the surface (less than 10 atomic layers) [73].

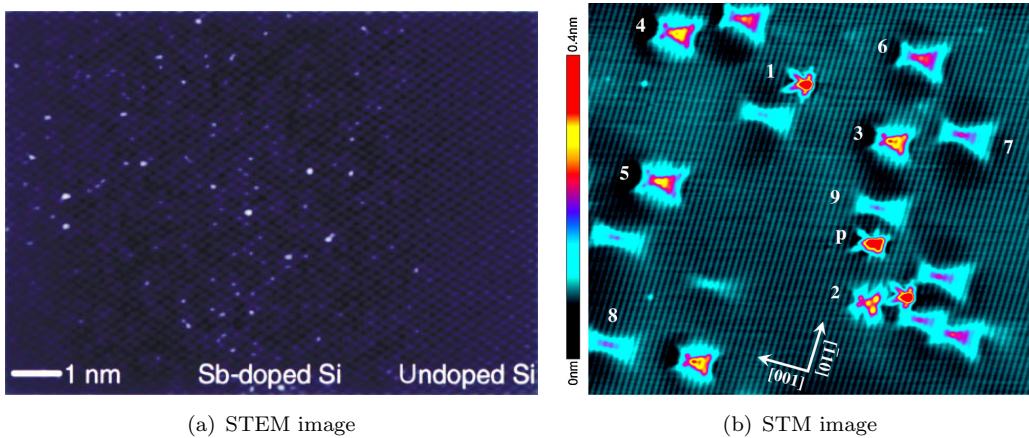


Figure 2.18: Nano scale dopant atoms observation by STEM and STM. (a) The brighter dots indicates single or more Sb dopant atoms. Otherwise The undoped area shows uniform colour [71]. (b)STM image for number of Mn acceptors in GaAs [72].

The distribution of the dopant atoms distribution located much deeper was detected by measuring the electric field/potential caused by which is induced by ionised dopant atoms located in the depth of up to 20 nm from the surface [70, 48]. Usually the ionised

dopants potential is screened by freely moving charge carriers. However the free charge carriers are able to be depleted by applied voltage. To achieve this task the free charge carriers on the measured surface where depleted and low temperature was helpful to stabilize the surface potential.

Ligowski *et al.* [48] detected single dopant atoms in thin Si layer at temperature of 13 K. In their experiment the charge carrier is depleted by the back gate electrode (Figure 2.19(a)) and the the local potential well in the CPD image under back gate biasing (Figure 2.19(b)). At zero back-gate biasing, the KPFM image is more uniform, which is consistent with the charge screening effect.

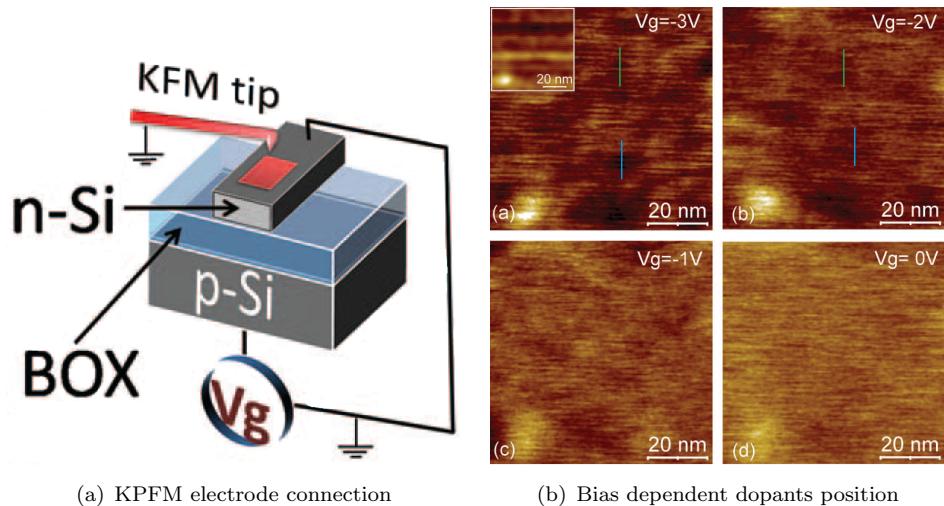


Figure 2.19: KPFM position dopants in thin Si. (a) Sample and measurement setting (b) measurement result. Large contrast appears on large back gate voltage due to stronger depletion effect. Dopant atoms supposed in marked region [48].

The dopant cluster potential overlap could blur the boundary of each individual dopants. Assuming the uniform doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$, only one dopant is expected to be in the area of $10 \text{ nm} \times 10 \text{ nm}$. Therefore in nano-scale devices the doping profile measurement by KPFM would turn into single dopant detection rather than evaluating the doping concentration.

2.3.3 Recent attempts of Si nanodevice characterization

The KPFM is designed to measure the CPD of the material surface, thus it is also expected to be able to measure the change of the position of the Fermi energy by externally applied bias. In 1999, Shikler *et al.* [74] measured the build-in-potential in p-n junction of light-emitting devices. In that experiment the n-region is grounded while p-region biased. The resulting CPD image is shown in Figure 2.20(a) with different forward bias. The CPD is fixed in n-region due to ground connection. In contrast the

CPD in the p-region is gradually reduced with increasing forward bias. This trend of the CPD change is consistent with expectation. However the measured potential step at the p-region is much larger than the externally applied potential step value. In Figure 2.20(a) for KPFM measured potential change on biased p-n junction, the maximum CPD on p-Si shifted from 0.7 to 1.9 V (1.2 V in total), however, the applied bias only changed from 1.78 to 1.5 V (0.28 V shift in total). Meanwhile the measured build-in potential for p-n junction is 800 mV which is smaller than the theoretical calculation. The scaling factor is common phenomenon [67] in the KPFM measurement and it was attributed to the light absorption, or change of surface charge states [74].

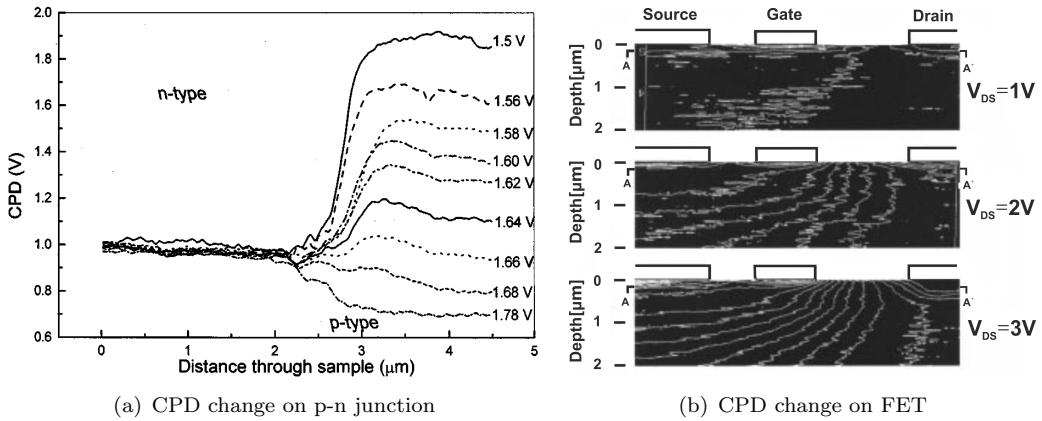


Figure 2.20: In vitro KPFM measurement for micro-scale devices (a) p-n junction under different forward bias [74] (b) potential distribution in FET under different S-D potential [75].

The potential measurement at a cross-sectional surface of an FET device was reported in 1999 [75]. In Figure 2.20(b) equal potential lines are represented by the contour map and the potential difference between adjacent lines is 100 mV. With small applied source-drain bias V_{DS} the density of the potential lines is small while the contour lines are much intense under larger applied voltage. Particularly the density is high near the electrode.

SiNW devices have been studied recently by KPFM by several group, such as the measurement of dopant variation along the SiNW [76], deep charge traps [77], and potential distribution with current [26]. The potential distribution in SiNW is associated with transport of charge carriers in the channel. The measured potential map and potential curve along SiNW under different applied bias are shown in Figure 2.21. Under S-D bias where the current goes through the SiNW channel, and the potential drop along the SiNW is clearly seen in the KPFM image. In addition the three dark spots indicated by the white arrows suggest the defects on SiNW channel [26]. In the end the measured CPD change is consistent with change of applied bias on electrode. In Figure 2.21(c) the total potential drop in the scanned region is about 0.65V which is consistent with externally applied 0.75 V bias. In addition, the potential step between SiNW and electrode

which was explained by doping transition form heavily doped p^+ electrode to lightly doped p SiNW [26].

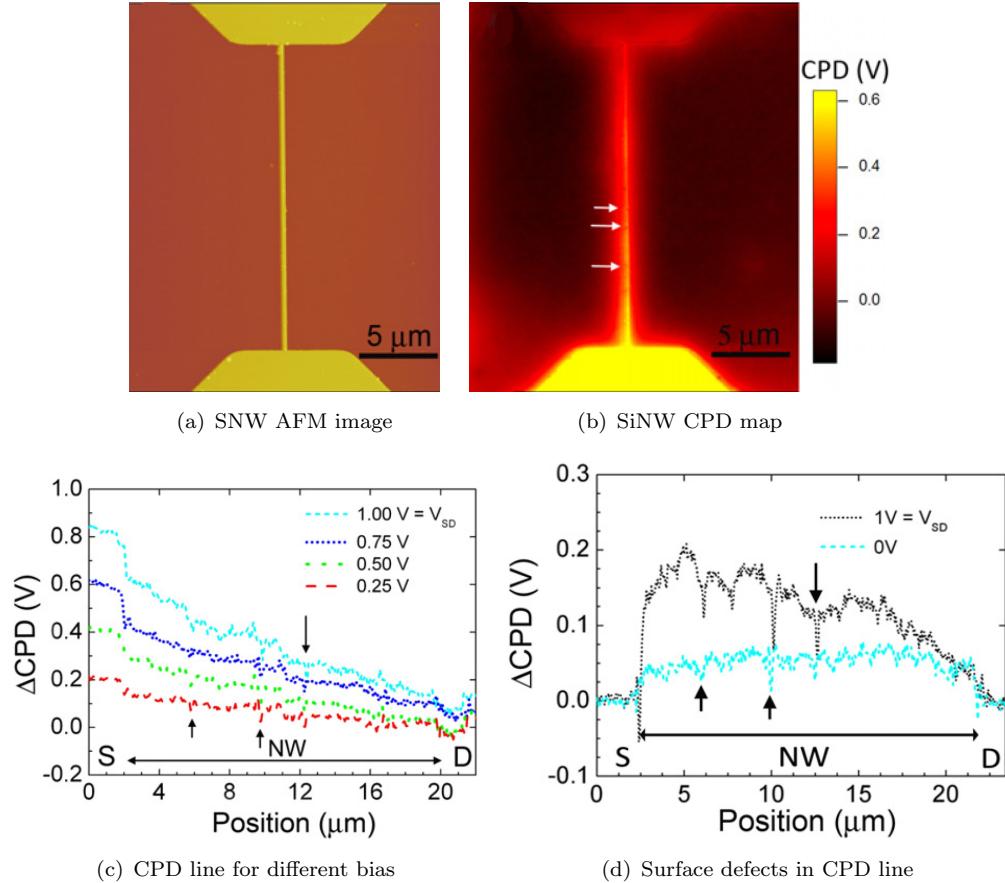


Figure 2.21: In-vitro potential distribution along SiNW by KPFM (a) AFM image of SiNW devices $W=200\text{nm}$ $L=20\mu\text{m}$ $h=115\text{nm}$ (b) KPFM potential map (c) surface potential line along SiNW and electrodes under different V_{DS} bias. (d) zoomed in observation of potential valley which probably induced by surface defects which is indicated by arrow. [26]

In nanoscale devices, any charge traps near the channel could affect the electronic transport properties. [78, 36]. The charge state of quantum dots was measured by Salem *et al.* [79]. The nano crystalline silicon (nc-Si) dots with the diameter of 2-8 nm on the sample surface as shown in fig.2.22(a). A larger CPD contrast is able to be observed between uncharged dots and substrate materials in KPFM image. The dots were charged by largely biased KPFM tip. In contrast the charged dots present opposite CPD state to uncharged dots. This experiment demonstrated that the charge state of quantum dot is measurable. This method is expected to be extend to detect charge states in single electron transistors.

The presence of dopant atoms and its charging state are often estimated by current or conductance spectrum [80, 25, 78, 36]. In recent works, attempts have been made for the direct observation of dopants distribution and dopant states in nano SiNW devices

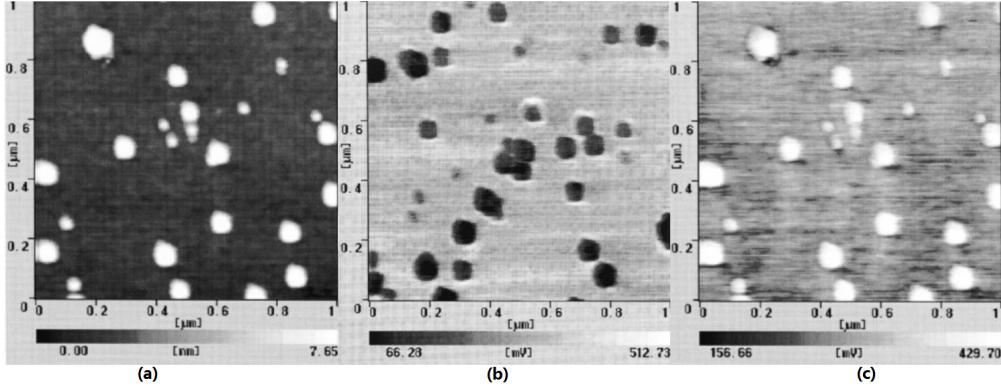


Figure 2.22: Charge state of quantum dots by KPFM (a) AFM image of quantum dots (b) KPFM image of un-charged quantum dots (c) KPFM image of charged quantum dots [79].

[48, 10, 81, 82, 83]. Similar to the single dopant detection technology in ref. [48] the single dopant is detected by KPFM. In contrast the measured sample is changed into double side gate FET transistor (Figure 2.23(a)). For the dopants detection -4 V is applied to the side and back gate to deplete free charge carriers and cancel the screening effect. In the result the dopant position was suggested by the gate voltage dependent black dots in the potential image. In addition, the bleared blacked dots in the potential image for current running condition (Figure 2.23(a)) was explained by ionised dopants trapping electrons when electron current is flowing. The trapping can be related to coulomb oscillation therefore the current spectrum is also measured in similar but top gated devices (Figure 2.23(b)). The short channel tend to have single peak and long channel tend to present multiple resonance. This effect can be explained by few dopants formed single QD in short channel and many QD in long channel.

The in-situ SiNW characterisation studies above demonstrated the KPFM tool is able to detect the local potential change in the p-n junctions due to externally applied bias, accurately follow the potential drop in uniformly doped SiNW, and even the dopant atoms and its charge states under devices operation. Those works suggest a new method of nano-devices characterisation by using surface potential information. However, the fictionalised nano devices such as SiNW FET and SET devices has not been systematically characterised by using this new methods. After reviewing work, a space has been found that the surface potential characterisation method can be extended to reveal the change in charge transport properties in the intentionally designed FET and SET devices by using local potential and electric field informations.

2.4 Motivation of this work

This review has summarized the up-to-date development of nano FET devices and KPFM characterisation technologies. The multigate SiNW devices are promising for

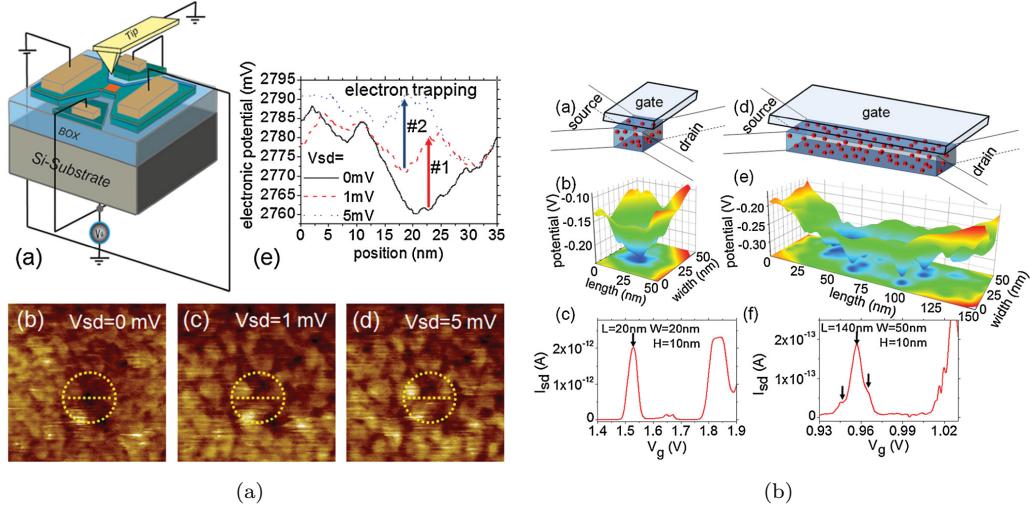


Figure 2.23: Single dopant charge state measurement and current oscillation corresponding simulation. (a) KPFM single dopant charge measurement setting and measurement result. (b) simulation result of dopant atoms formed quantum dots in channel in short and long channel. The measured current oscillation is consistent with simulation: short channel on QD single oscillation long channel multiple QD multiple oscillation peak [10].

further scaling and showing ideal subthreshold behaviour. On the other hand, the problems caused by individual dopants variation has been identified in literature. In the study of SiNW sensing applications we have noticed that the depletion of charge carrier in the channel seriously affects real surface potential distribution. After reviewing the development of SET devices, we have found that for single electron operation, there is more strict requirement in local potential variation. As KPFM is a powerful tool for local surface potential variation mapping, the further in-depth understanding of SiNW devices would be expected by employing KPFM.

In this study, in order to investigate the details of electrical transport properties of silicon nanowire devices, I have developed the original experimental set-up (bias network in Nanonics CV2000 system) to be able to measure the surface potential of the working devices. Various test structures such as simple p-n junctions, uniformly-doped nanowires, and back-gate n-type transistors have been fabricated on SOI by using state-of-the-art nanofabrication technology. The KPFM image and profile along the nanowire channels will be analysed by comparing with the simulation results and discussed by considering charging effects around the nanowire channels.

Chapter 3

Theoretical Background

3.1 Introduction

This chapter introduces theoretical background of device operation and measurements which are used in this project. The first part focuses on the material properties of Si, in particular how the Fermi energy shifted, due to doping, and also the transport properties of SiNW devices. The second part will introduce the principle of KPFM measurement and details of KPFM equipment. Because the KPFM is based on the AFM principle, AFM system is introduced first and then KPFM. Effects of vacuum environment on the KPFM measurement are also introduced.

3.2 Fermi energy shift in Si by doping

In semiconductor devices, electrical potential to the charge carriers is controlled by doping. In large-scale devices the doped region is considered to be uniform and the doping concentration is the parameter needed for describing device characteristics. On the other hand in nano-scale devices as a total number of atoms in the channel are significantly reduced so that individual dopant atoms should be considered independently. In other words local potential distribution induced by the randomly distributed dopants would affect the device characteristics. Here, key equations that represent the relationship between the doping concentration and Fermi energy shift with respect to the vacuum level are derived.

3.2.1 Doping and Fermi energy level shift

Operation principle of semiconductor electronic devices are closely related to the electronic structure of the material that is in general tuned by impurity doping. Actually the

electron transport in the devices are controlled by electric potential. The doping is often used to enhance the conductivity or to build up p-n junction which is a fundamental element for various application *e.g.* diodes for current rectification, bipolar transistors (BJT), and field effect transistors (FETs) for switches and logic applications.

One of the key role of the dopants is to generate charge carriers in semiconductor materials. Without dopants the conductivity of intrinsic semiconductor is very low; *e.g.* 10^{-4} S/cm for Si, 10^{-8} S/cm for GaAs, and 10^{-2} S/cm for Ge [68]. The conductivity of materials expressed by Equation 3.1,

$$\sigma = \frac{1}{\rho} = q\mu_n n + q\mu_p p , \quad (3.1)$$

Where the μ_n and μ_p are the electron and hole mobility, and n and p represent concentrations of electron and hole. In intrinsic semiconductors the electron-hole pair must be excited over the energy band gap of the materials *e.g.* 1.11 eV for Si, 1.43 eV for GaAs, and 0.67 eV for Ge. The fermi distribution function of electrons [69] is

$$f_D(E) = \frac{1}{1 + e^{(\frac{E-E_f}{k_B T})}} , \quad (3.2)$$

where E_f is the Fermi energy and $k_B T$ is the thermal energy (k_B is the Boltzmann's constant, and T is the temperature). The probability of electron distribution is exponentially reduced. Therefore large energy band gap results in low charge carrier density in intrinsic materials. However the charge carrier density can be adjusted by doping impurity atoms into semiconductor materials. For example, in Si, excess electrons are supplied by phosphorus doping while excess holes by boron. electron donor phosphorus in Si and electron acceptor boron. The impurity atoms substitute host atoms in lattice. For different dopant atoms the excitation energy is different; *e.g.* 39 mV for Sb, 45 mV for P and 54 mV for As in Si. The carriers are almost fully activated at room temperature so the doping concentration corresponds to the carrier density. In general, the conductivity of semiconductor materials can be largely enhanced by doping.

The charge carrier density n is calculated by integrating the product of $f_D(E)$ chance of electrons stay at energy E and $N(E)$ the number of electrons stay at energy E , as shown in Equation 3.3

$$n = \int_{E_c}^{\infty} N(E) f_D(E) dE . \quad (3.3)$$

The solution of Equation 3.3 for electron density n is

$$n = N_c e^{-(E_c - E_f)/k_B T} , \quad (3.4)$$

and for hole density p is

$$p = N_v e^{-(E_f - E_v)/k_B T}, \quad (3.5)$$

where the N_c is the density of state in conduction band and the N_v is the density of states in valence band. In Si at room temperature 300 K, the value of N_c is $1.05 \times 10^{19} \text{ cm}^{-3}$ and value of N_v is $3.92 \times 10^{18} \text{ cm}^{-3}$. The intrinsic electron concentration n_i is equal to intrinsic hole concentration p_i and it is $1.45 \times 10^{10} \text{ cm}^{-3}$. The intrinsic Fermi energy level E_i is then derived by equalling Equation 3.4 and Equation 3.5 and solve E_f as

$$E_f = E_i = \frac{E_c + E_v}{2} - \frac{k_B T}{2} \ln \frac{N_c}{N_v}, \quad (3.6)$$

Equation 3.4 and Equation 3.5 are also valid for doped semiconductors where the number of electrons and holes are not balanced. We can simplify those expressions which reference of to the intrinsic carrier concentration n_i which is derived by substituting Equation 3.6 into Equation 3.4 or Equation 3.5:

$$n_i = \sqrt{N_c N_v} e^{-E_c - E_v / 2k_B T}, \quad (3.7)$$

Therefore the charge carrier concentrations are rewritten as

$$n = n_i e^{(E_f - E_i)/k_B T}, \quad (3.8)$$

$$p = n_i e^{(E_i - E_f)/k_B T}, \quad (3.9)$$

And another important expression showing the relationship among n , p and n_i are derived as

$$n_i^2 = np \quad (3.10)$$

The majority carrier concentration is considered as the doping concentration as the minority carrier concentration is negligible compared with the majority one. The shift of Fermi energy level is from the intrinsic one finally expressed as

$$E_{fn} - E_{in} = k_B T \ln \frac{N_d}{n_i} , \quad (3.11)$$

$$E_{fp} - E_{ip} = k_B T \ln \frac{n_i}{N_a} . \quad (3.12)$$

Where the N_d and N_a are the n-type donor and p-type acceptor concentrations respectively. These equations show how the shift of Fermi energy level is related to the doping concentration quantitatively. While n-type doping moves E_f closer to the edge of the conduction band, p-type doping shifts to the edge of valence band (Figure 3.1). When the two types of materials are contacted the Fermi energy level of both sides are aligned at the same level due to the carrier diffusion between two regions and as a result the energy barrier is formed in both conduction and valence band as shown in Figure 3.1.

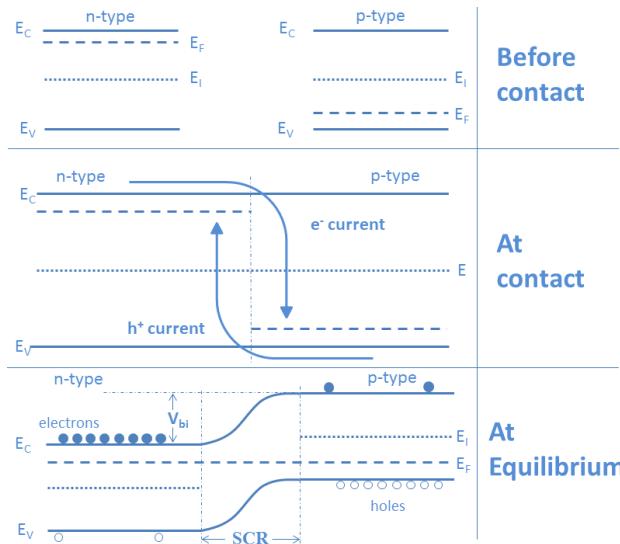


Figure 3.1: Doping induced energy shift and energy barrier in a p-n junction.

The energy barrier height E_{bi} is defined by subtracting Equation 3.12 from Equation 3.11,

$$E_{bi} = k_B T \ln \frac{N_d N_a}{n_i^2} , \quad (3.13)$$

Where the Fermi level in both p- and n-type material is aligned and the energy barrier height is the intrinsic Fermi energy difference between contact p- and n-type material. Corresponding to the energy barrier there is voltage step which is called build in potential ψ_{bi} formed in p-n junction is derived from Equation 3.13 as

$$\psi_{bi} = \frac{k_B T}{q} \ln \frac{N_d N_a}{n_i^2} . \quad (3.14)$$

In p-n junction, the build-in potential prevent the drift of the carriers from the p-region to n-region for electrons and the other way around for holes.

3.2.2 Charge carriers depletion in p-n junction

Once the FET channel length becomes less than 10 nm, fabrication of well-defined two pn junctions at the both sides of the channel junction barriers becomes challenging because the effect of diffusion and random distribution of dopant atoms. Junctionless transistors [6], are advantageous in fabrication and shows almost ideal sub-threshold characteristics, and high on/off current ratio (10^6) [6].

The depletion length under biasing is estimated by solving Poisson's equation (Equation 3.15 [68]).

$$\frac{d^2\psi}{dx^2} = -\frac{d\epsilon}{dx} = -\frac{qN}{\epsilon_{si}} \quad (3.15)$$

By integrating Poisson's equation twice, the depletion width W is calculated as follows:

$$\begin{aligned} \psi &= \iint_W^0 \frac{d^2\psi}{dx^2} dx \\ &= \iint_W^0 -\frac{qN}{\epsilon_{si}} dx \\ &= \frac{1}{2} \frac{W^2 qN}{\epsilon_{si}} \end{aligned} \quad (3.16)$$

$$W = \sqrt{\frac{2\psi_{bi}\epsilon_{si}}{qN}} \quad (3.17)$$

For full depletion of the SiNW channel towards low off-current, the smaller doping concentration and higher voltage are preferable. However lower doping concentration significantly reduces the channel conductivity so the device operation speed is reduced. In addition the inversion layer is formed once the applied gate voltage makes the Fermi energy level at interface crosses the intrinsic Fermi level. Due to the creation of the inversion layer, the depletion width cannot exceed the maximum depletion width W_m defined as the width when the applied voltage reaches $2\psi_b = 2(\psi_f - \psi_i)$. If the doping concentration of a SiNW is assumed $1 \times 10^{17} \text{ cm}^{-3}$, the value for $2\psi_b$ is approximately 0.8 V. By using this estimated value in Equation 3.17, the maximum depletion width is estimated around 73 nm. Therefore if the thickness or diameter of the nanowire is less than W_m , it is possible to deplete whole SiNW by applying voltage.

3.3 Charge transport in SiNW devices

Two complementary components of the current should be considered to describe the charge carrier transport in semiconductors. The first one is the drift current which is driven by electric field inside the semiconductors i.e. charge carriers move under the force of electric field. The large current in semiconductor devices is normally contributed by drift current. The drift current density is expressed in Equation 3.18

$$J_{\text{drift}} = q\mu n E , \quad (3.18)$$

where q is charge of single charge, μ is mobility of charge carries, n is charge carrier density, and E is electric field.

The other one is caused by charge carrier diffusion due to the gradient of carrier concentration which is driven by . In semiconductor devices the formation of p-n junction and small minority charge carrier current is the result of diffusion process which is driven by thermal energy. In semiconductor p-n junctions a small amount of minority charge carrier current is the result of diffusion process. The diffusion current density $J_{\text{diffusion}}$ is expressed by

$$J_{\text{diffusion}} = k_B T \mu \frac{dn(x)}{dx} , \quad (3.19)$$

where $n(x)$ is the charge carrier density at the position x .

3.3.1 Planar FETs

First let me outline the theory for conventional planar MOSFETs. The concentration of charge carriers in the channel is modulated by gate biasing. When the FET devices is on a thin inversion layer is formed near the oxide interface for current conducting. In literature the value of gate voltage V_g which drive the current to appear is called threshold voltage V_{th} . V_{th} is related to the energy band bending near the gate oxide interface. The V_{th} is associated with the formation of the inversion layer at $\psi = 2\psi_b$. The total amount of spatial charge in the depletion region is

$$Q_{\text{sc}} = qN_a W_m \quad (3.20)$$

$$= \sqrt{2q\epsilon_{\text{si}} N_a (2\psi_b)} . \quad (3.21)$$

At $\psi = 2\psi_b$, the ideal (without surface charge) threshold voltage is expressed as

$$V_{\text{th}} = 2\psi_b + \frac{Q_{\text{sc}}}{C_{\text{ox}}} \quad (3.22)$$

$$= 2\psi_b + \frac{\sqrt{2q\epsilon_{\text{si}}N_a(2\psi_b)}}{C_{\text{ox}}} . \quad (3.23)$$

The bulk MOSFET is constructed by a n-p-n/p-n-p structure. The p-n junctions which are formed at two terminals of MOSFET channel are the fundamental element in the MOSFET to contribute the transconductance behaviour of MOSFET devices. In the off state ($V_g < V_{\text{th}}$) the p-n junction is strong and one of the reversed back-to-back p-n junctions prevent current running through the channel. After large voltage is applied ($V_g < V_{\text{th}}$) the junction is significantly weaken by injecting exceed minority charge carriers large current is allowed. Therefore the change in transconductance is related to the potential induced free charge carrier density change. As previous discussion the applied surface potential is able to deplete free charge carrier away and also inverse the type of free charge carriers *e.g.* free electron density is larger than hole density in p-type channel. The total amount inversion charge carriers is expressed by

$$-Q_i = C_{\text{ox}}(V_g - V_t) , \quad (3.24)$$

where C_{ox} is the gate capacitance per unit area, V_g and V_t are the applied gate voltage and threshold voltage, respectively. It is notably that in this equation the conductive charge carrier density can be increased infinitely with increasing V_g as Equation 3.24, however in real situation Q_i is limited by various factors such as density of state, break down voltage, and tunnelling effect.

Equation 3.25 is the drain current for small V_d and Equation 3.26 for large V_d [68].

$$I_d = \mu \frac{W}{L} C_{\text{ox}}(V_g - V_t) V_d, \text{ at linear region} \quad (3.25)$$

$$I_{\text{Dsat}} = \mu \frac{W}{2L} C_{\text{ox}}(V_g - V_t)^2, \text{ at saturation region.} \quad (3.26)$$

According to Equation 3.26 in the saturation region, the drain current is independent of the drain voltage. This is because of the pinch off effect under the large drain voltage. The pinch-off state and current saturation curve are shown in Figure 3.2 (a) and (b), respectively. The MOSFET operation time is expressed by the RC products as

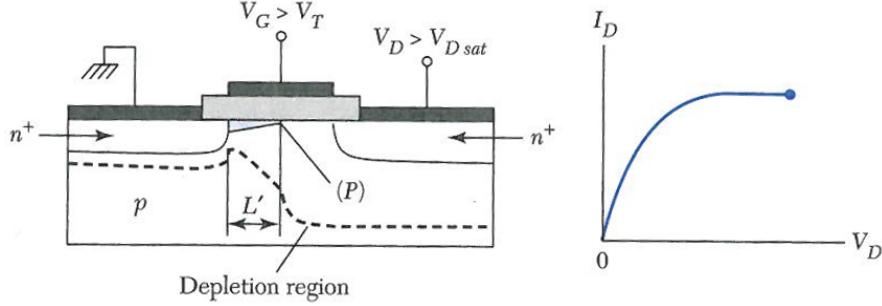


Figure 3.2: Pinch off and current saturation state [68].

$$\begin{aligned}
 \tau &= RC \\
 &= \frac{V}{I}C \\
 &= \frac{V_g}{\mu \frac{W}{L} C_{\text{ox}} V_g^2} C_{\text{ox}} W L \\
 &= \frac{L^2}{\mu V_g} .
 \end{aligned} \tag{3.27}$$

According to Equation 3.27, the operation speed depends on the gate voltage, channel length and charge carrier mobility in the channel. It is clear that in order to enhance MOSFET's switching speed, larger mobility and shorter channel length are desired. However as the devices are scaled down into nanoscale, the short channel effect appears. The short channel effect appears in the following four aspects. First the threshold voltage starts to depend on the source/drain voltage. Secondary, the subthreshold current starts to increase. Thirdly, the velocity saturation happens earlier due to earlier appear of high electric field ($E_x = V_d/L$). The velocity saturation makes the saturation current smaller than that of the pinch-off point therefore reduce operation speed. Finally hot charge carriers and tunnelling effect become serious in devices. It results in large leakage current and also breaking charge neutrality in the insulators therefore gradually changes device operational parameters.

In the sub-threshold region, due to the weak inversion of the channel, subthreshold current is mainly the diffusion current which is expressed by [68]

$$\begin{aligned}
 I_d &= -qAD_n \frac{\partial n}{\partial y} \\
 &= -qAD_n \frac{n(0) - n(L)}{L} \\
 &= \frac{qAD_n n_i e^{-q\phi_b/k_B T}}{L} \left(1 - e^{-qV_d/k_B T}\right) e^{q\phi_s/k_B T}
 \end{aligned} \tag{3.28}$$

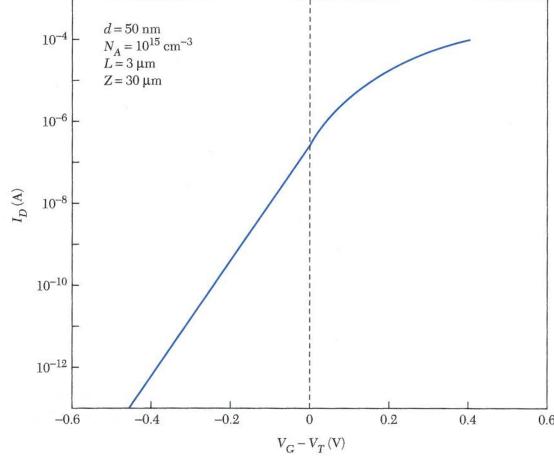


Figure 3.3: Subthreshold voltage I-V curve [68].

where ψ_b is the potential difference between Fermi level and intrinsic Fermi level, ϕ_s is surface potential at Si-SiO₂ interface, and A is cross-sectional area of the channel which is the product of the depth and width of the channel. The $I_d - V_d$ curve is illustrated in Figure 3.3. Obviously below the threshold voltage the source-drain current increase exponentially. The subthreshold swing (SS) defined as $[\partial(\ln I_d)/\partial V_g]^{-1}$ is important value to assess leakage current in the OFF states. Smaller SS value means fast cutting off speed and also small leakage. At room temperature the ideal SS value is 60 mV/decade.

The SCE is a crucial issue of the scaling of planar MOSFETs. Novel SiNW devices have SCE immunity and are able to show a SS value much closer to the ideal SS. In the following discussion the charge transport in the sub-threshold region is investigated by the combination of $I - V$ characteristics and surface potential profile.

3.3.2 SiNW MOSFETs

In order to overcome the SCE, the thin SiNW devices with multigates are being developed. At early stage of the double gate structure with the front and backside gate were developed [30, 31, 84, 32]. At on state an inversion layer is formed on both the front side and back side. The double gate devices demonstrate nearly ideal threshold slope [32].

3.3.3 Si single electron transistors

As was mentioned in the in previous review, the SiNW transistors could behave as single electron transistors (SETs) if the single dopant dominate the charge transport in device operation. Here key theoretical points on single electron transistors are introduced. The simplified SET model is presented in Figure 3.4(a). Two tunnelling junctions isolate one electron island in the middle and the gate electrode is capacitively coupled to the island to control the energy state and the number of electrons in the island. The total

charge presented in the island can be estimated by using the gate capacitance C_g and gate voltage V_g as shown in Figure 3.4(b) [46].

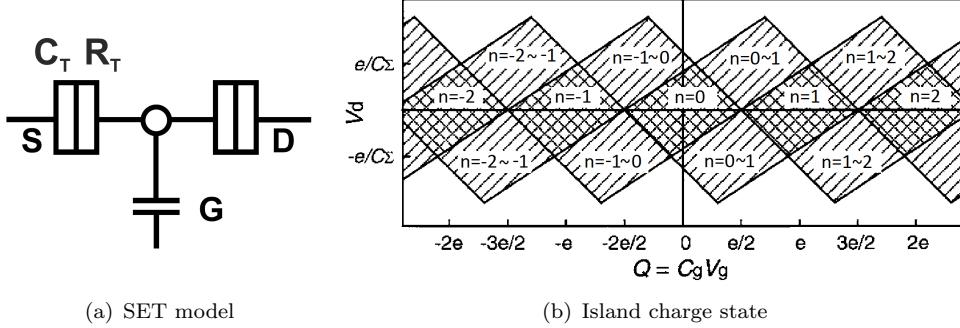


Figure 3.4: Construction of single electron transistor and its island charge state diagram (a) SET model, two tunneling junction and one isolated island coupling with gate capacitance (b) gate voltage controlled number of electrons in island. single electron add or left island at $(n + \frac{1}{2}e)/C_g$ [46]

In SET devices the source/drain current is oscillated according to the gate voltage as shown in Figure 3.5(c). The period of conductivity oscillation is related to single electron charging energy. The charging energy is the energy which is required to move a single electron from the source or drain into the island. Figure 3.5 (a) and (b) present the energy which is required for removing an electrons to or from island. When $Q = Ne$, this state is at the minima of the energy curve as shown in Fig. 3.6 (a), and this graph suggests that additional energy of $Q = (N + \frac{1}{2})e$ is required to move to the nearest state, either $(N + 1)e$ or $(N - 1)e$. On the other hand, when $Q = (N + \frac{1}{2})e$ the N and $N+1$ states are degenerated, so that the energy gap between the states is disappeared even at zero temperature [46]. As a result the peak conductance appears at $Q = (N + \frac{1}{2})e$ and the conductance is minimized at $Q = Ne$ (Figure 3.5(c)). From the gate capacitance the oscillation period is estimated as

$$\Delta V_g = e/C_g . \quad (3.29)$$

There are many restrictions to design SETs. To be able to clarify each single charge is one of the important criteria. This can be achieved by shrinking the island size and the gate capacitance. According to the equation $V = e/C$, if C becomes small enough and single charge is distinguishable. In the aspects of individual electron confinement, the resistance of the tunneling barrier R_t should be large enough (Equation 3.30) [18] and the thermal energy should be much smaller than charging energy e^2/C_Σ .

$$R_t \gg R_Q = h/e^2 \approx 30 \text{ k}\Omega \quad (3.30)$$

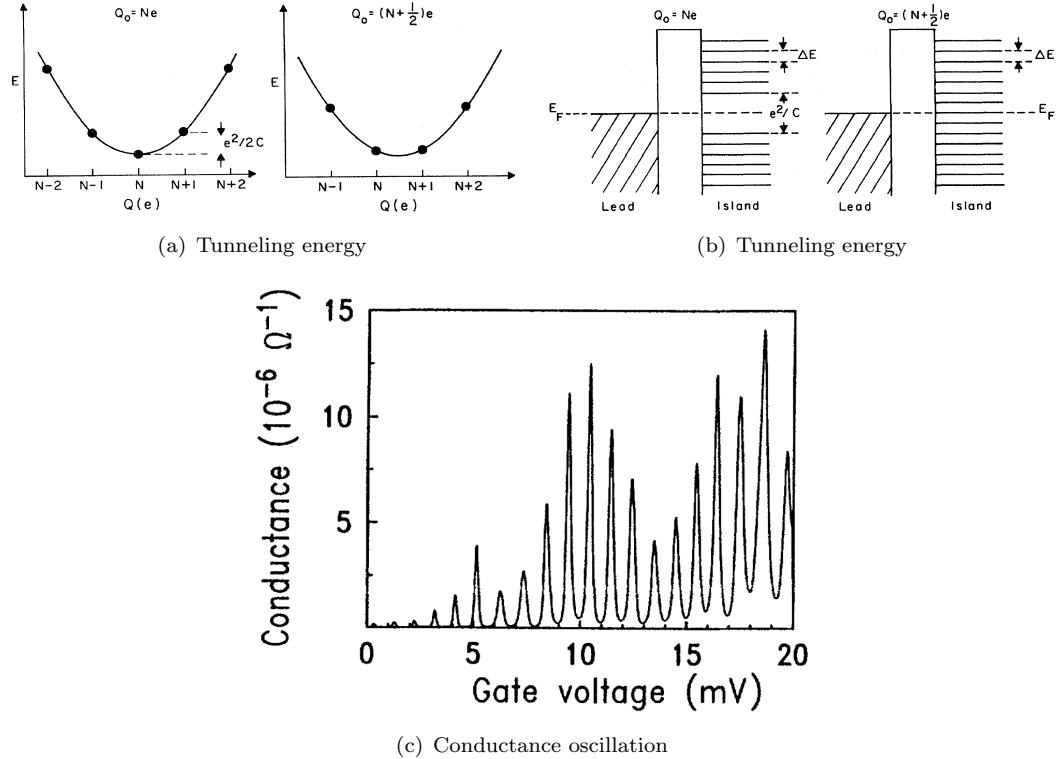


Figure 3.5: Single electron transistor charging energy conductance fluctuation diagram (a,b) Charging energy for one and two electrons, larger demand energy for Ne state than $(N + \frac{1}{2})e$ state, but for second electron the demand energy is much larger than the first one. (b) conductance fluctuation as function of gate voltage, peak conductance appears at $(N + \frac{1}{2})e$ state and minimum at Ne state. [46]

3.4 Kelvin Probe Force Microscopy

Electrical characteristics of the SiNW devices are strongly related to the surface potential and individual charge distribution. Therefore if there is a method which is able to measure the surface potential variation and charge distribution in the SiNW channel the SiNW devices electrical characteristics can be further understood. The requirement for this kind of measurement should be highly sensitive and non-disruptive. Kelvin Probe Force Microscopy presents high capability for this application.

3.4.1 Contact potential difference (CPD)

The CPD is the quantity measured in KPFM. The CPD between two materials is due to the difference of the work function. The work function is defined as the energy which is required for removing an electron from the material to the vacuum level. The work function is expressed by

$$q\psi = (E_c - E_f) + q\chi , \quad (3.31)$$

where χ is called the electron affinity which is the potential required to remove an electron from the bottom of the conduction band to vacuum [69]. The electron affinity of Si is 1.39 eV, Ge 1.23 eV and Al 0.43 eV. The Equation 3.32 is used for the estimation of work function of n-type semiconductor and Equation 3.32 is used to estimate the work function in p-type and p-type semiconductor.

$$q\psi_n = \left(\frac{E_g}{2} - k_B T \ln \frac{N_d}{n_i} \right) + \chi . \quad (3.32)$$

$$q\psi_p = \left(\frac{E_g}{2} + k_B T \ln \frac{n_i}{N_a} \right) + \chi . \quad (3.33)$$

On the other hand, for metals Fermi level is in the conduction band [69], therefore the work function defined as the difference between the Fermi level and the vacuum level.

Without electrical connection, two material are just isolated as shown in Figure 3.6(a) when they are electrically connected, the free charge carriers are moved to level the Fermi energy of the materials and finally an equilibrium state is reached in Figure 3.6(b) [69].

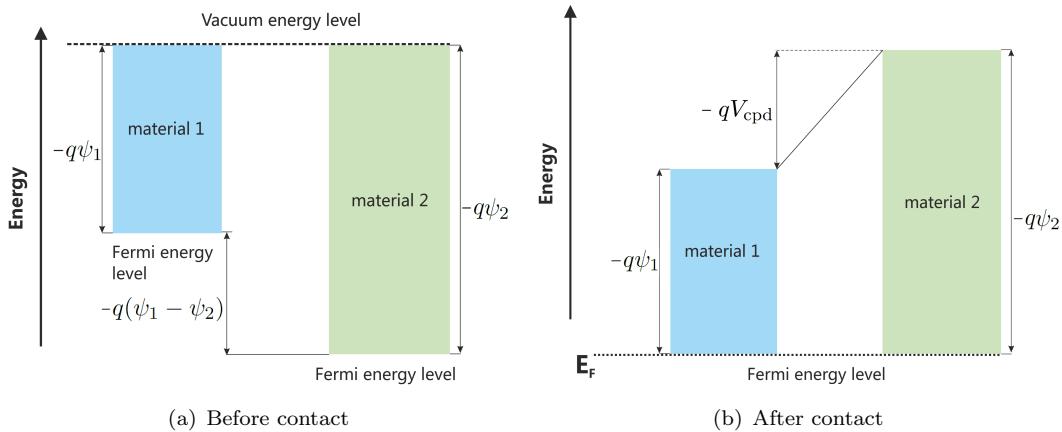


Figure 3.6: (a) Before contact two material is neutral and equal potential body
(b) after contact the electrons will move from Fermi energy higher to lower material and finally align the Fermi energy at same level in both materials

It is notable that the charge transfer can be in multiple ways *e.g.* direct contact, wire connection, even tunnelling etc. Once the equilibrium state is build up there is no net current between them. The value of CPD is expressed by the work function potential difference as

$$V_{cpd,12} = \psi_1 - \psi_2 , \quad (3.34)$$

where the ψ_1 and ψ_2 is the work function potential of material 1 and 2 in Figure 3.6.

3.4.2 KPFM measurement principle

The contact potential difference (V_{CPD}) between tip and sample surface is recorded during KPFM scan. The processes of V_{CPD} measurement are shown in Figure 3.7 (a) and (b)) for formation of V_{CPD} between tip and sample, and Figure 3.7(c) for V_{CPD} measurement. Without electrical contact (Figure 3.7(b)) the Fermi energy in both tip and sample is not aligned and no charge is accumulated in the tip apex. After the electrical connection is build, the Fermi energy in both tip and sample is aligned and V_{CPD} is induced between tip and sample as previous discussion and the potential between tip and sample is

$$V_{\text{ts}} = \psi_t - \psi_s , \quad (3.35)$$

where the ψ_s is the work function potential of sample and ψ_t is the work function potential of tip. Under the influence of V_{ts} the charges is then accumulated in sample surface and tip apex as result the charge accumulation in tip-sample capacitor C_{ts} . The capacitance force is also induced in C_{ts} by V_{ts} and expressed as

$$F(V_{\text{ts}}) = \frac{V_{\text{ts}}^2 C_{\text{ts}}}{2z} \quad (3.36)$$

$$= \frac{\varepsilon_0 A_{\text{tip}} V_{\text{ts}}^2}{2z^2} , \quad (3.37)$$

where the z is the tip-sample distance, ε_0 is the permittivity of vacuum, and A_{tip} is the area of tip apex. The capacitance force $F(V_{\text{cpd}})$ is the crucial signal which is monitored by KPFM system for the measurement of V_{cpd} by applying opposite DC bias

$$V_{\text{DC}} = -V_{\text{ts}} , \quad (3.38)$$

to the conductive KPFM tip via KPFM feedback system to eliminate the $F(V_{\text{cpd}})$. The details of $F(V_{\text{cpd}})$ monitoring and KPFM feedback system will be illustrated in the flowing KPFM measurement system section.

The discussion above shows the principle of KPFM measurement for the work function difference between tip and sample. This is what the KPFM designed for the materials characterisation. Nowadays the KPFM characterisation methods has been extended to dynamic in-situ nano-electronic-devices characterisation as discussed in literature review. Based on the dynamic characterising application the work function potential

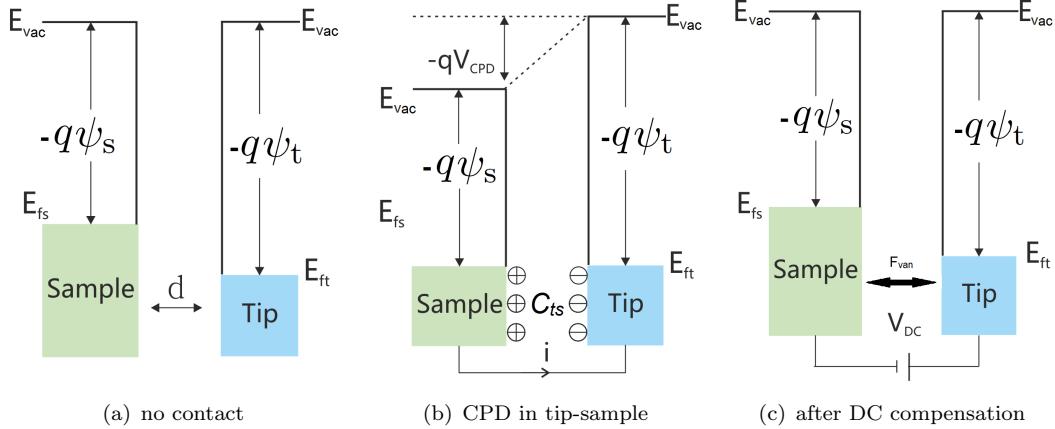


Figure 3.7: CPD measurement in KPFM (a) before tip electrical connected to sample the vacuum energy level E_{vac} for tip and sample material at the same line (b) after electrical connection CPD if formed and the Fermi energy level is at the same line $V_{\text{ts}} = \psi_t - \psi_s$ (c) after applying DC bias the potential difference is eliminated and only Van der Waals' force F_{van} is presented.

difference in Equation 3.37 is able to be extended to any potential difference between tip and sample surface so that not only local work function variation on sample but the local potential distribution under externally applied and surface trapped charge are also measurable.

3.4.3 KPFM measurement system

The KPFM is based on AFM measurement system as in previous review. The AFM is actual a force microscopy which monitors the force change on tip cantilever to sense both topography and tip-sample voltage induced force change to record both topography and voltage change on sample surface during scanning. The schematic diagram of our KPFM measurement system is shown in Figure 3.8. According to the diagram the AFM and KPFM have separate signals and measurement systems (in the dash line frames) but share the same tip cantilever and PSD detector which is used to monitor the vibration of tip cantilever. The tip cantilever is vibrated at certain frequency under the drive by inputting $\sin(\omega_1)$ signal on piezo and the amplitude of tip cantilever vibration is used to monitor the tip-sample interaction during the scan. The AFM feedback system automatically adjust the tip height to follow the change in sample contour by monitoring the change in vibration amplitude. Meanwhile the AFM scan the other AC signal ω_2 is directly applied to the conductive tip and induce the second vibration in tip cantilever due to tip-sample capacitance force. The amplitude of second vibration is mordanted by KPFM system. During the scanning a DC voltage is applied to the tip to follow the change of V_{CPD} . The details of AFM and KPFM measurement will be illustrated in the flowing study for the purpose of optimisation of KPFM measurement.

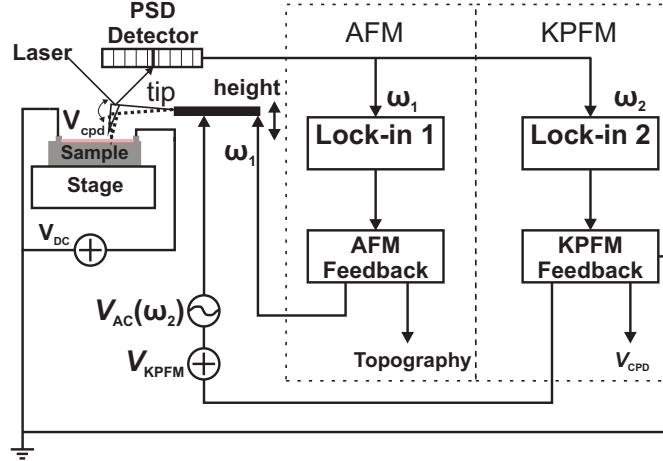


Figure 3.8: Diagram of KPFM measurement system

3.4.3.1 AFM

In the AFM measurement system, the tip sample interaction force is a key parameter for the detection of topography change. The distant dependent force is shown in Figure 3.9(a). If the distance between the tip and the sample surface is about 10 Å [85], the tip-sample interaction is dominated by the attractive force (20 nN), while if the distance becomes less than 4 Å to the sample surface the tip-sample interaction changes to be repulsive force (100 nN) [86]. Three different AFM measurement modes; contact, non-contact, and tapping are shown in Figure 3.9(b). The long range attractive force which induced by permanent dipole, corresponding induced dipole, and instantaneously induced dipole is used in non-contact mode AFM measurement for soft and delicate sample but with low resolution due to weak interaction force. The short range repulsive is used in contact-mode AFM measurement for hard and smooth sample measurement Figure 3.9(b). In contact-mode AFM the tip is strongly engaged with sample surface thus the life time of AFM tip is short. The third AFM measurement mode, tapping mode, is used in our KPFM measurement system. During AFM scan the tip gently tap the sample surface and then lift with certain frequency by using this methods the resolution and life time of tip is improved [73].

The mechanical oscillation method is used to monitor the force change in tip-sample interaction for the topography scan. To get the maximum sensitivity the cantilever is driven under its intrinsic resonant frequency f_o as [88]

$$f_o = \frac{1}{2\pi} \sqrt{\frac{k}{m}} , \quad (3.39)$$

where the k is the spring constant of cantilever and m is the effective mass of tip cantilever. The resonant frequency is changed after the tip-sample is engaged (fig:tipsmod) and the new frequency is expressed as [89]

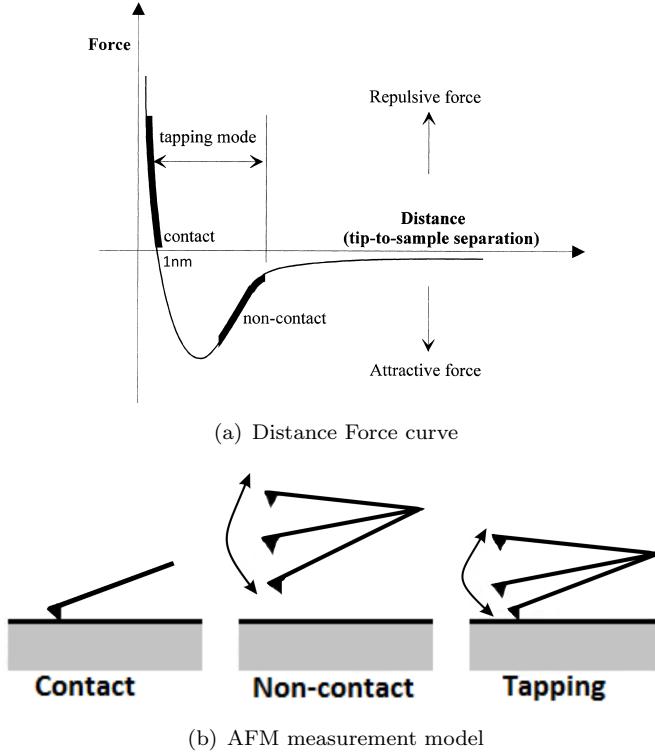


Figure 3.9: (a) Tip sample distance related atomic force curve and force region used in different AFM measurement mode [87]. In the repulsive region the force is sharply response to distance change and for the attractive force the change is relatively steady. (b) tip-sample distance in different AFM mode

$$f_{\text{int}} = \frac{1}{2\pi} \sqrt{\frac{k + k_{\text{ts}}(z)}{m}} , \quad (3.40)$$

where the $k_{\text{ts}}(z)$ is the tip-sample interaction force gradient at height z . The change in resonant frequency results the change in resonant amplitude as in Figure 3.10(b) according to the theoretical estimation [90]

$$A_{\text{res}} = \frac{A_{\text{o}} (\omega_{\text{o}}/\omega)}{\sqrt{1 + Q^2 (\omega/\omega_{\text{o}} - \omega_{\text{o}}/\omega)^2}} , \quad (3.41)$$

where the A_{res} is the resonant amplitude after the tip-sample engagement, the A_{o} is the resonant amplitude in air, the ω_{o} is the angular frequency of intrinsic resonant, the ω is the angular frequency under engagement, and the Q is quality factor of cantilever. As Figure 3.10(b) the peak amplitude at only if $\omega = \omega_{\text{o}}$ when cantilever resonant in air. The amplitude is monitored by feedback system during the sample surface mapping scan.

In our KPFM measurement system the Amplitude Modulation (AM-mode) [88] is used to monitor the amplitude change which is induced by change in z and to adjust the height of cantilever to maintain the constant resonant amplitude thus to follow the contour change

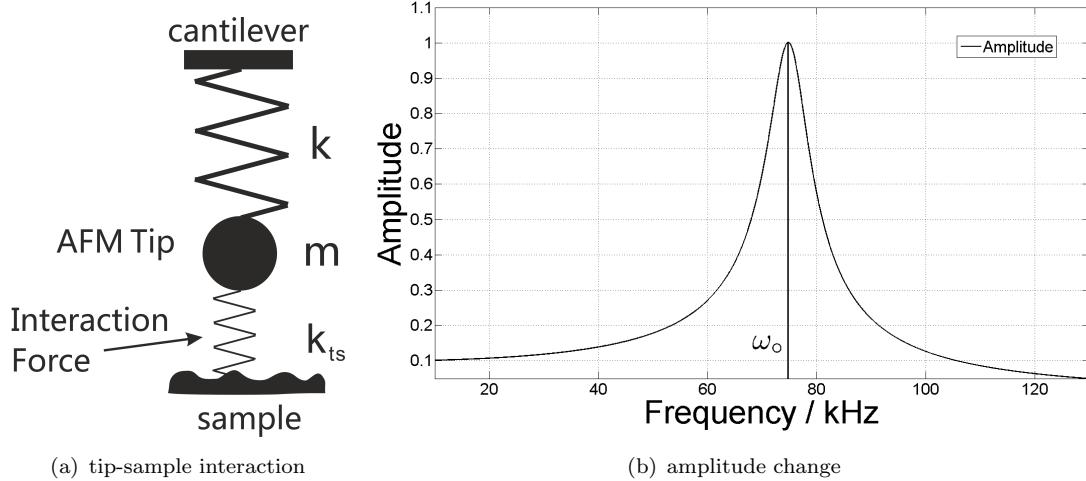


Figure 3.10: Tip sample interaction and amplitude change (a)two spring model for tip-sample interaction, after interaction resonant frequency is changed due to change of total k (b)Frequency related amplitude and phase shift curve. The amplitude peak only appears when cantilever drives at ω_0 .

on sample surface during scan. In actual AFM scan, the cantilever driving frequency is fixed at ω_0 and a reference amplitude value, for example $A_{\text{ref}} = 0.28$ at $\omega = 60$ kHz, is set to feedback system and the close-loop feedback system adjust the tip-sample distance fixed at constant z to maintain the $A_{\text{res}} = A_{\text{ref}}$ thus the change in contour on sample surface is precisely recorded during the scan.

The quality of AFM image by our measurement system is largely depended on the value of A_0 and A_{ref} . Appropriate A_{ref} should be found because both too large or too small A_{ref} all reduce the height resolution of AFM image. During the scan the actual tapping force is decided by the value of A_{ref} . The energy which stored in cantilever is expressed as [73]

$$E_{\text{res}} = \frac{1}{2}kA^2 . \quad (3.42)$$

The energy which is stored in cantilever is related to the resonant amplitude A and spring constant of cantilever k . The energy dissipation during tapping is

$$\Delta E_{\text{res}} = \frac{1}{2}k(A_0 - A_{\text{ref}})^2 . \quad (3.43)$$

Therefore the small A_{ref} value result large energy depletion and also result large tapping force and it is opposite for large A_{ref} value. In the KPFM scan large tapping force could improve the high resolution of AFM scan however too large tapping would break the stability of measurement and also reduce the life time of tip. The value of A_0 and A_{ref} should also adjusted according to different sample for example for soft sample the large

A_o is preferred and it should be small for hard sample surface. The physical oscillation amplitude in the system is between 10~100 nm [73].

3.4.3.2 KPFM

The principle of V_{cpd} detection by KPFM has been introduced by Figure 3.7 and Equation 3.37. In this part we will focus on the details of the V_{cpd} detection to investigate its sensitivity and limitation.

Similar to the AFM measurement, the other osculation amplitude is monitored by the KPFM measurement system to derive V_{cpd} . As diagram of KPFM measurement system in Figure 3.8, the AC signal ω_2 is applied to the cantilever simultaneously during AFM scan and result a second resonant in cantilever. The PSD detector detects converts the mixed mechanical osculation into electronic signal and send it to both AFM and KPFM feedback system. The Lock-in-amplifier in both AFM and KPFM system are able to distinguish only targeted oscillation. For the KPFM measurement the lock-in2 generates ω_2 and only scenes the AC signal with the same frequency and phase in the mixed electric signal from PSD to detect and adjust the mechanical oscillation which is related to the V_{cpd} . The mechanical ω_2 oscillation is expressed by replacing V_{DC} into $V_{DC} + V_{AC}$ in Equation 3.37 and expressed as

$$F(z, t) = \frac{1}{2} \frac{\partial C(z)}{\partial z} [V_{DC} + V_{AC} \sin(\omega_2 t)]^2 , \quad (3.44)$$

where the $C(z)$ is the function of tip-sample capacitance at distance z , t is the time. Due to the mechanical vibration, the tip-sample capacitance is also changing thus the constant C in Equation 3.37 is replaced by dynamic capacitance $C(z)$ in Equation 3.44. After the expansion of square part in Equation 3.44, the force function is expressed as

$$F(z, t) = \frac{1}{2} \frac{\partial C}{\partial z} V_{DC}^2 + \frac{\partial C}{\partial z} V_{DC} V_{AC} \sin(\omega_2 t) + \frac{1}{4} V_{AC}^2 \frac{\partial C}{\partial z} [1 - \cos(2\omega_2 t)] . \quad (3.45)$$

In the Equation 3.45, three different forces are contained; DC constant force, osculating force at frequency ω , and osculating force at frequency 2ω . Those forces are expressed in flowing equations

$$F_{DC} = \frac{1}{2} \frac{\partial C}{\partial z} V_{DC}^2 , \quad (3.46)$$

$$F_{\omega_2} = \frac{\partial C}{\partial z} V_{DC} V_{AC} \sin(\omega_2 t) , \quad (3.47)$$

$$F_{2\omega_2} = \frac{1}{4} \frac{\partial C}{\partial z} V_{AC}^2 [1 - \cos(2\omega t)] . \quad (3.48)$$

The DC bias induced cantilever's deflection is expressed by Equation 3.46, the mechanical oscillation which induced by AC bias between tip and sample at frequency ω_2 is expressed by Equation 3.47, and the other AC bias induced mechanical oscillation at frequency $2\omega_2$ is expressed by Equation 3.48. For V_{cpd} measurement the KPFM the amplitude of F_{ω_2} induced oscillation is monitored and adjusted by KPFM measurement system [19]. Here the amplitude is expressed as

$$A_{\omega_2} = \pi \varepsilon_0 V_{AC} V_{DC} \frac{QR}{kz} , \quad (3.49)$$

where the ε_0 is the permittivity of vacuum, and the R is the tip radius. During the scan KPFM close-loop feedback system always tries to minimise the value of A_{ω_2} by making V_{DC} to be zero. The V_{DC} is composed by

$$V_{DC} = V_{cpd} + V_{KPFM} \approx 0 , \quad (3.50)$$

where the V_{KPFM} is the DC bias applied to cantilever to eliminate the DC bias between tip and sample thus the A_{ω_2} in Equation 3.49 is also minimised. During the KPFM scan the change in local V_{cpd} is recorded by feedback system as V_{KPFM} , which is equal to $-V_{cpd}$ by always adjusting A_{ω_2} to be zero.

To understand the sensitivity of KPFM measurement is important to understand the limitation of KPFM equipment. The noise in KPFM measurement system is mostly contributed by thermal vibration which is [90]

$$N = \sqrt{2k_B T Q B / \pi k f_{res}} , \quad (3.51)$$

where the k_B is Boltzmann constant, the T is Kelvin temperature, the Q is quality factor, B is band width, the k is the spring constant of cantilever, and the f_{res} is resonant frequency. This equation suggests the thermal noise can be reduced by more stiff tip and also high resonant frequency. Based on the estimation of thermal noise the sensitivity (minimum measurable voltage) to V_{CPD} can be estimated by [19]

$$V_{CPD,min} = \sqrt{2k_B T k B / \pi^3 Q f_{res}} (1/\varepsilon_0 V_{AC}) (z/r) , \quad (3.52)$$

where the r is the radius of tip apex. According to Equation 3.52 the KPFM sensitivity is not only depended on the thermal noise but also AC voltage and tip radius. The sensitivity can be improved by increasing the value of AC, however, large AC voltage also

induce large cantilever bending and also large magnitude of second mechanical oscillation which could smear the AFM measurement and also KPFM feedback. Large radius tip could reduce noise however the lateral resolution would be sacrificed. Therefore the parameter setting which is used for KPFM measurement should be balanced. In our measurement, the parameters which used for KPFM scan are; tip radius $r = 20$ nm, spring constant $k = 2.8$ N/m, $f_{\text{res}} = 75$ kHz, $Q = 300$, $B = 1$ Hz, effective tip-sample distance $z = 10$ nm, and applied $V_{\text{AC}} = 1$ V, therefore the optimistic sensitivity is about 0.4 mV. Nonnenmacher et al. [19] mentioned that in ultra high vacuum (UHV) the resolution could be increase 100 times because the increase in Q . As the resolution of AFM can be reached to atomic scale massive atomic resolution LCPD measured by KPFM are reported [20, 21, 22, 23].

3.4.3.3 High vacuum KPFM measurement

The surface potential of devices could be influenced by the surface state of materials. As the adhesive molecules are able to be removed in the vacuum environment, the vacuum is demanded to remove the adhered molecules on sample surface to eliminate the affection from the surface charges. On the other hand, due to the air removing the mechanical resonant property is significantly changed and results the change in both AFM and KPFM feedback system. For the purpose of vacuum measurement optimisation the change difference in vacuum measurement will be studied.

Because less of air damping in vacuum the Q value of the cantilever are largely increased. Normally for 300kHz tip the Q value is 100, however, in high vacuum it is approximately 50,000 [89] therefore better KPFM sensibility is expected for vacuum measurement according to Equation 3.52. Since the Q value is 500 times larger than in air, the minimum measurable V_{cpd} in high vacuum can be 22 times smaller than it in ambient. However the actual resolution of high vacuum measurement is also limited by time scale (τ) which is the time taken for tip cantilever to response the change and back to stable condition. The response in amplitude change is slower than frequency change and it is strongly related to Q value. The time scale for AM mode KPFM is [91]

$$\tau_{\text{AM}} \approx \frac{2Q}{f_{\text{res}}} . \quad (3.53)$$

It is clear that the significant increase in Q value in high vacuum would cause large delay in response time therefore the measurement system is tend to be unstable for vacuum measurement. To solve this problem the high resonant frequency is demand, however it is not available for our measurement system. As an alternative solution the PID controller (proportionalintegralderivative controller) is applied to the feedback system to optimise the vacuum measurement.

3.4.4 KPFM equipment

The KPFM in the University Of Southampton lab is Nanonics CV2000. The CV represents the meaning of Cryo View. It is capable to measure sample in high vacuum (below than 5×10^{-8} Torr) and low temperature (using liquid helium). According to Figure 3.11 there is a spare port at five a clock position. It can be used to connect external electrode into the chamber for measuring the local surface potential change and electrical characteristic at the same time. The maxim scanning range is 50 micron in X-Y-range and 25 micron in Z-range. The minimum scanning step is less than 0.02 nm. That step should be enough for the investigation of minute potential variation at nano scale for nano-devices. The high vacuum and cryo temperature enable us to study SETs.

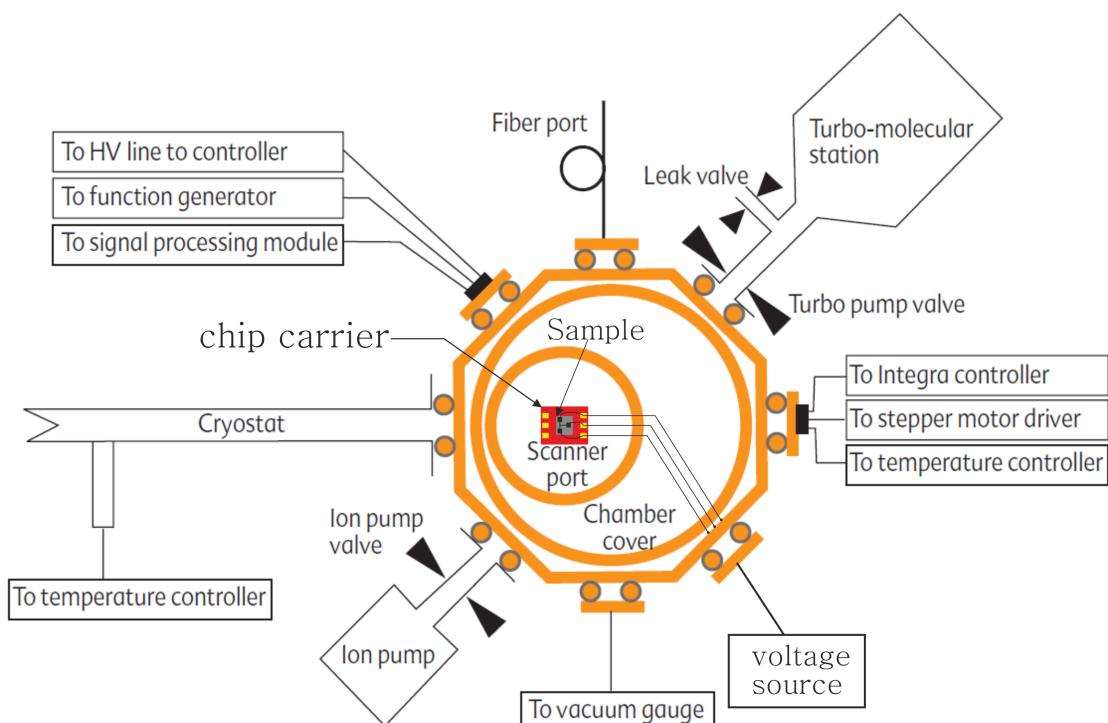


Figure 3.11: The construction of Nanonics CV2000 (top view)

The sensitivity of KFPM system depends on the AFM tip. The highly conductive n^+ silicon with resistivity from $0.01\sim0.02 \Omega\cdot\text{cm}$ Nanosensor ATEC-FM-20 is used (Figure 3.13). According to the manufacturer's specification, this tip has resonant frequency from $50\sim130$ kHz, force constant $0.7\sim9.0$ N/m and particularly the radius of tip is smaller than 10 nm. This tip is capable to measure calibrating sample, however, there is still some space to upgrade the lateral resolution if finer map image is desired.

To be more specific the low pass filter is also called Time Constant Filter. It aims to remove high frequency noise of all types: mechanical, acoustic or electrical. However the smallest position represents smallest time constant. As discussion in background chapter the time consistent determines tip reaction time and as much as small time constant is

Technical Specification CryoView 2000™

Modes of Operation

NFOM	Transmission, reflection, collection, fluorescence
AFM	Contact, non-contact, intermittent-contact
Feedback Mechanism	Tuning Fork Feedback
Confocal Microscopy	Transmission, reflection, fluorescence

Scanning/Sample

Scanner	2 Piezoelectric flat scanners are available: 1. Scan range: 25 micron Z-range, 50 micron XY-range 2. Scan range: 5 micron Z-range, 10 micron XY-range
Step Size	< 1 nm for 50 micron scanner; < 0.02 nm for 10 micron scanner
Sample Positioning	XYZ stepper motors
Maximum Sample Size	16 mm diameter

Probes

NSOM Probes	Cantilevered tapered optical fiber probes
AFM Probes	Cantilevered tapered glass probes
Specialized Probes	Cantilevered probes for electrical or thermal measurements
	Custom probes available on request

Figure 3.12: The technical specification list of CV2000

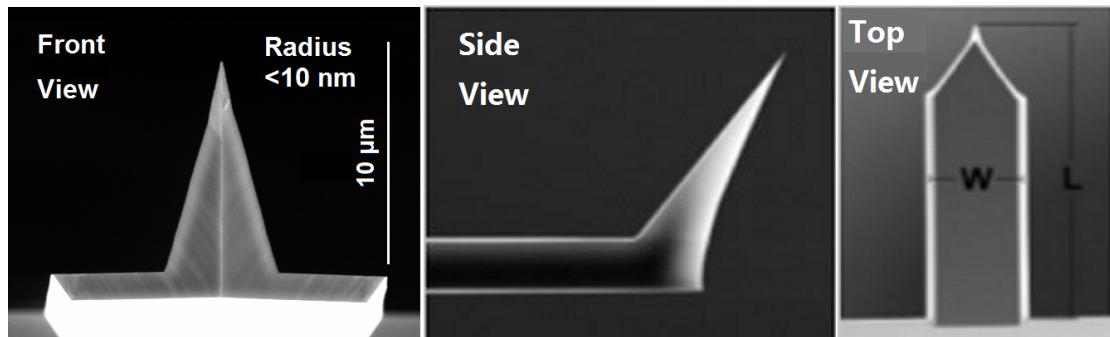


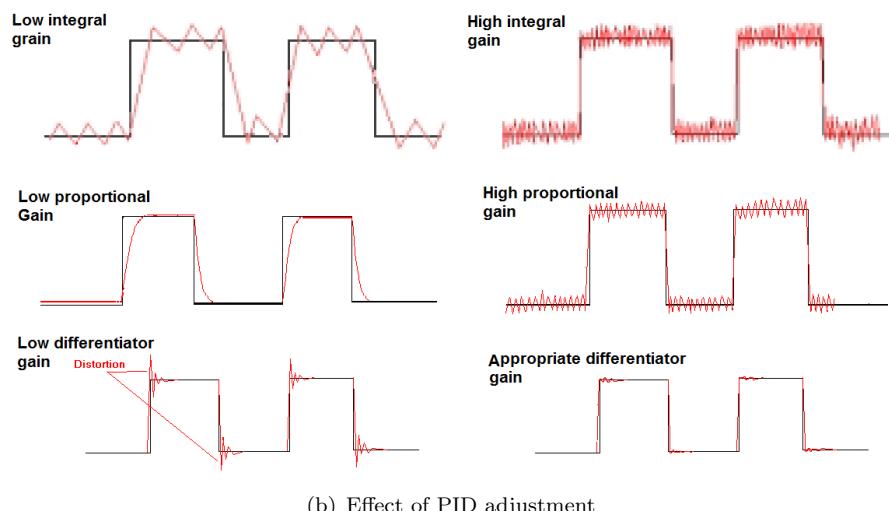
Figure 3.13: SEM image of KPFM tip.

recommend especially for vacuum measurement with AM model (CV2000). In addition the Integrator Gain defines how fast the correction will be applied to the scanner, i.e. the integration time for the Z correction. The Integrator Gain is very sensitive and may significantly affect the quality of the image. Furthermore the Differentiator Gain is useful when the sample combines relatively flat features with relatively sharp topographic features. The problem with this combination is that flat areas need low Proportional Gain and sharp areas need high Proportional Gain. Normally the Proportional Gain is at minimum position. Moreover the Proportional Gain defines the magnitude of the correction signal. It amplifies the Error signal in order to get an appropriate correction signal. The increase of Proportional Gain is useful if hysteresis appears between trace and retrace curve. In order to get the quality image the PID control adjustment

should combine with physical resonant amplitude setting, reference value set up, and also sampling time at each measurement point etc.



(a) CV2000 PID button



(b) Effect of PID adjustment

Figure 3.14: PID control parameter setting and its effect (a) PID adjust button (b) effect of PID parameter setting[92]

Chapter 4

KPFM characterisation of charge transport property in SiNW

4.1 Introduction

Silicon nanowires (SiNWs) have been widely considered as a key building block of nanoelectronics since the report of bottom-up-grown SiNW devices [93, 94]. With the development of top-down nanofabrication technology, SiNWs have been applied not only for the channel of highly-scaled short-channel-effect-free field-effect-transistors (FETs) [4] but also for the core of ultrasensitive molecular sensors [95]. While the surface of the SiNWs is surrounded by insulators and gate electrodes for FET applications, the surface properties are vital for sensing applications where the surface of the nanowire needs to be exposed to the targets to be detected. Therefore, the study of local surface properties and electrical transport properties of the SiNW devices at the same time are beneficial for further understanding of how the surface states and carrier transport in the nanowire are correlated each other.

Kelvin Probe Force Microscopy (KPFM) is a unique method to observe the local surface potential which is directly associated with the electronic state of the materials. Since the pioneering work detecting the potential change across a silicon p-n junction [96], KPFM has been developed as a local potential sensing tool to characterise doping concentration of silicon [64, 66, 67, 97, 98, 99]. Recently KPFM has been applied for studying SiNW devices and local doping variation along the NW length [100] and distribution of the deep traps and defects on the surface [26, 77] have been investigated under the current flow through the nanowire. Motivated by these works, in this paper, I have designed a silicon nanowire device whose surface of the channel is accessible by the KPFM cantilever and systematically studied effects of source-drain biasing on the surface potential around the nanowire channel. I have particularly focused on the behaviour at the junction between

the nanowire and lead region and discussed characteristic features due to the mixture of material-originated and surface-originated effects observed by KPFM.

4.2 Experimental methods

4.2.1 Devices design

The structure of SiNW device is shown in Figure 4.1. There are two different lead design for shorter channels ($\leq 15 \mu\text{m}$) in Figure 4.1(a) and longer channels ($> 15 \mu\text{m}$) in Figure 4.1(b). Both side of the SiNW (insert figure) are connected to the two $200 \times 200 \mu\text{m}$ large contact pads. For the devices with shorter channel the lead length is fixed but the width of the leads changes depending on the width of SiNW, where the ratio of the width of the lead to the SiNW is kept at 10:1. For the long channel devices the lead structure is fixed as shown in the inset of Figure 4.1(b). The lead design for the short channel SiNWs is to increase the gap between the contact pads to make the KPFM scan easier.

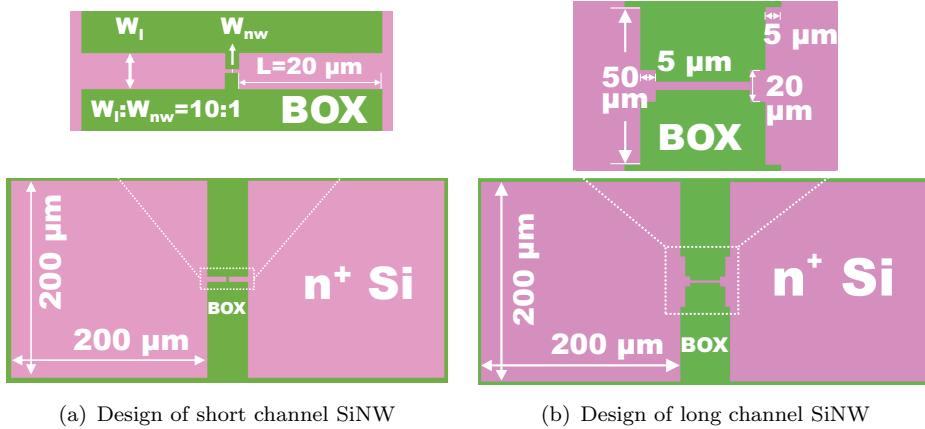


Figure 4.1: Mask design for uniform heavily doped SiNW devices (a) short channel (b) long channel (BOX=buried oxide).

The dimensions of SiNWs channel are listed in Figure 4.2(a). Total 64 devices are arranged in a $1 \times 1 \text{ cm}^2$ chip (Figure 4.2(b)). In the fabrication total 6 chips is made and named from C1-C6. To test the uniformity of doping process.

The other key sample parameters are also listed in the Figure 4.2(a). Prior to the diffusion process, dopant diffusion simulation (Silvaco Athena) was taken to estimate the doping concentration and diffusion depth. The simulation result is shown in Figure 4.3. After 30-min diffusion at 1000°C the doping concentration in the top 50 nm SOI is expect to be $3.5 \times 10^{20} \text{ cm}^{-3}$, corresponding to the resistivity of $2.86 \times 10^{-4} \Omega\cdot\text{cm}$ with refer to the bulk Si doping-resistivity table in Ref. [68]. Meanwhile, the mobility of

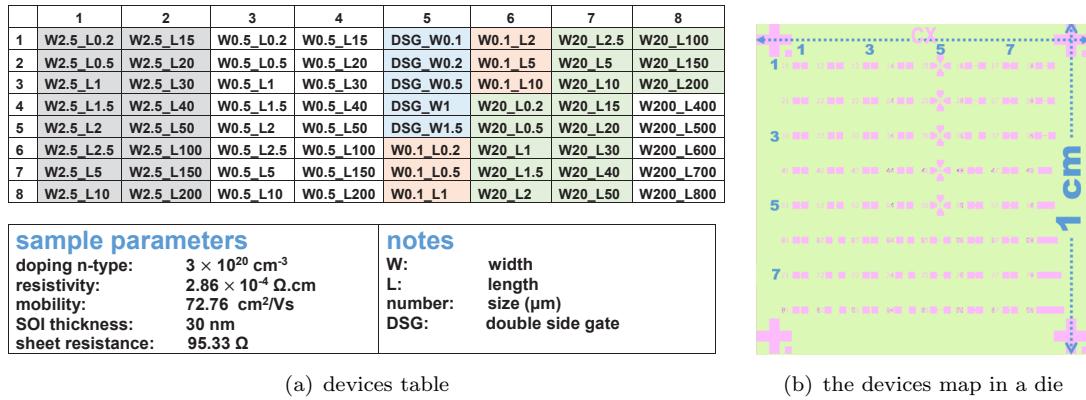


Figure 4.2: Table and map of heavily doped SiNW devices (a) table of SiNW devices. (b) devices range map in chips.

electrons in Si is $72.76 \text{ cm}^2/\text{Vs}$ according to the relationship of $\rho = 1/q\mu n$. For the SOI thickness of 30 nm, $95.33 \Omega/\square$ is expected for the sheet resistance.

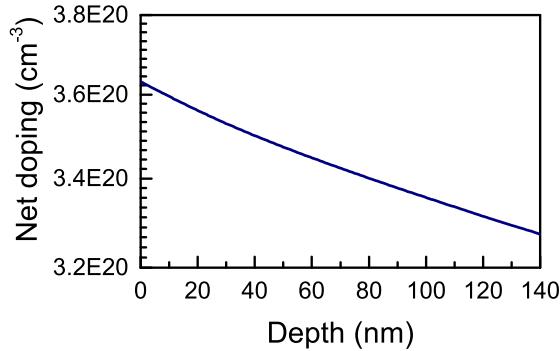


Figure 4.3: Silvaco Athena simulation of dopant diffusion in SOI after $1000 \text{ }^{\circ}\text{C}$ 30 min annealing, concentration figure along depth, the doping concentration on top 60 nm is around $3.5 \times 10^{20} \text{ cm}^{-3}$ (n).

During the fabrication process a dummy SOI chip was processed with the sample chip together for the purpose of process control. The thickness of SOI, resist and thermal oxide, were measured by Ellipsometry (J.A. Woollam M-2000). The resistivity of the wafer after doping was characterised by Four-Probe (Jandel RM3-AR) and Hall effect (Nanometrics HL5550) measurements.

4.2.2 Devices fabrication

The fabrication process is shown in Figure 4.4. There were three main fabrication processes were taken to get the SiNW devices. The first step is to thin the thickness of SOI (Fig.4.4.(a)-(c)), In the thinning process a p-type 100 nm 6" SOI wafer (SOITEC, Ltd) was oxidised in oxygen gas at $1000 \text{ }^{\circ}\text{C}$ for 107 min, where 40-nm-SOI was consumed. After oxidation the oxide was removed by dipping the chip into non-metal tank of 5%

HF solution for 4 min. The second step is doping (Fig. 4.4 (d) - (f)). The spin-on-dopants (Filmtronics P507) was coated on chip immediately after stripping the oxide, and then diffused in a furnace at 1000 °C for 30 min. After diffusion, the remaining dopant material was cleaned by 5% HF solution for 5 min. The final step is the pattern transfer (Fig. 4.4 (g)- (h)). The designed pattern was transferred onto the doped SOI by Electron-beam (E-beam) lithography and then Reactive-ion etching (RIE). After removal of the resist, the device was ready for measurements.

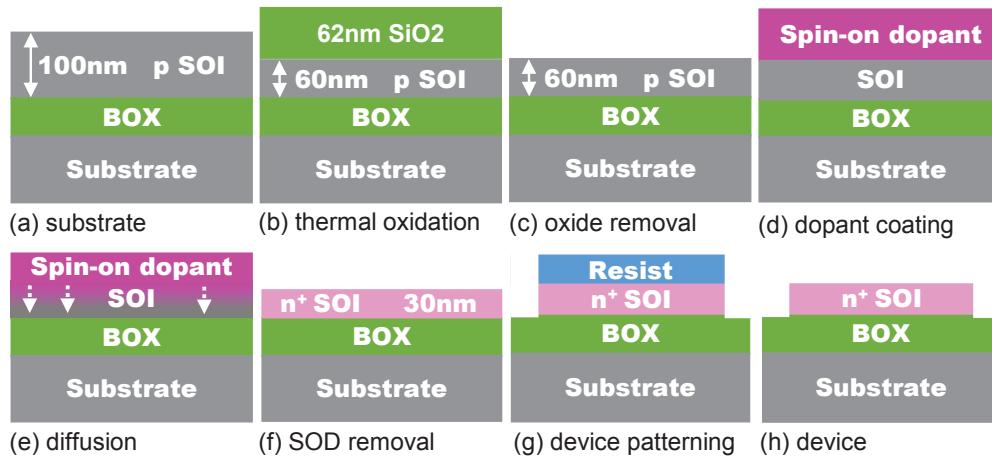


Figure 4.4: Mask design for uniform heavily doped SiNW devices.

SEM imageries in Figure 4.5 shows the plan views of the fabricated devices. The dark region shows the existence of thin SOI while the bright colour region corresponds to the exposure of the BOX layer. The shape and dimensions of the fabricated devices is well agreed with that of the designed mask.

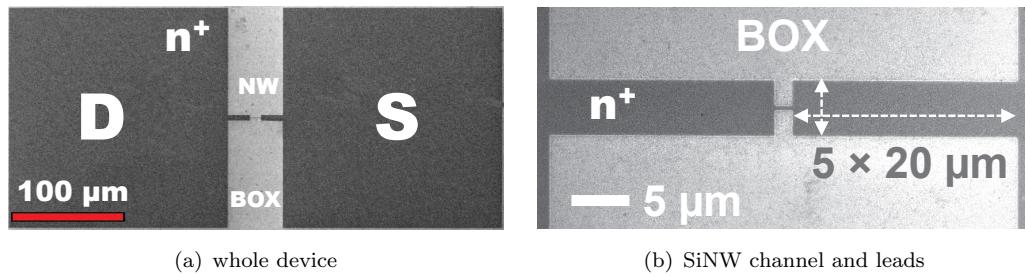


Figure 4.5: SEM image of fabricated uniformly doped SiNW device.

4.2.3 I-V characterisation

The probe station (Cascade M150) and Device Parameter analyser (Agilent B1500) were used for $I - V$ characterisation. Due to the highly conductive nature of the heavily doped SOI the probes were directly contacted without using metal pads to apply voltage and to measure the current through the devices. The resistance of the fabricated Si nanowires were evaluated as follows. First, the drain current I_d was measured by sweeping V_d

from -0.5 V to 0.5 V. The total average resistance R_{total} was extracted from the slope obtained by linear fitting of the $I_{\text{d}} - V_{\text{d}}$ characteristics. $R = V_{\text{d}}/I_{\text{d}}$. The total resistance is shown as

$$\begin{aligned} R_{\text{total}} &= R_{\text{contact}} + R_{\text{pad}} + R_{\text{lead}} + R_{\text{nw}} \\ &= R_{\text{C}} + R_{\text{nw}} , \end{aligned} \quad (4.1)$$

where the R_{contact} is the resistance of the probe-pad interface, R_{pad} is the resistance between the contact point to the lead in the contact pad, R_{lead} is the total resistance of two lead. The sum of R_{contact} , R_{pad} , and R_{lead} is expressed as R_{C} which is the sum of the parasitic resistance except for the nanowire. The value of R_{C} is consider to be constant for the samples whose doping and dimensions of the lead structure are the same.

If R_{total} of the SiNW devices with the same width is plotted against the length of SiNW (L) in the curve $R_{\text{total}} - L$, the resistivity of the nanowire is able to be extracted according to the formula,

$$R_{\text{total}} = \rho \frac{L}{Wt} + R_{\text{C}} \quad (4.2)$$

$$= S_{\text{R}} L + R_{\text{C}} , \quad (4.3)$$

where ρ is the resistivity of doped Si material. L is the length of SiNW channel, W is the width of SiNW, and t is the thickness of SOI. The value of ρ/Wt is expressed as S_{R} which is the slope of the $I_{\text{d}} - V_{\text{d}}$ curve. S_{R} can be used to extract the average resistivity of SiNW according to flowing equations

$$\begin{aligned} S_{\text{R}} &= \frac{R_{\text{nw}}}{L} \\ &= \frac{\rho}{Wt} \end{aligned} \quad (4.4)$$

$$\rho = S_{\text{R}} Wt \quad (4.5)$$

4.2.4 Surface potential simulation

Next, a new set-up of KPFM system that enables to characterise the surface potential of the devices under biasing condition at the same time. The Silvaco Atlas 3D simulator was used to simulate the potential and electric field distribution on the SOI devices

under various drain biasing. In 3D models the n-type uniformly-doped 30-nm-thick SOI layer is designed on top of a 200-nm-thick insulator layer.

In simulation, Poisson's Equation, carrier continuity equation, transport equation, and displacement current equation are used to calculate charge transport property. In addition the Fermi-Dirac and Boltzmann statistics, effective density of states, intrinsic carrier concentration, Passler's model for temperature dependent bandgap, bandgap narrowing, and the universal energy bandgap model are used to estimate charge carriers inside of semiconductor. Furthermore the mobility model is included to calculate the charge carrier's mobility change depends on temperature, high/low field, Impact Ionization, Strain etc.

4.2.5 Surface potential mapping and charge transport characterisation method

The connection diagram is shown in Figure 4.6(a). The Drain and Source electrodes are connected to the DC voltage source (Keithley 2401). In KPFM surface potential scan the common ground is shared between voltage source and KPFM measurement system. A device under test is electrically connected to the system by wire bonding. The Figure 4.6(b) is the image of a sample connection to the measurement system. The sample chip is placed onto the large contact pad which leads to the external electrode, G , in the centre of PCB board by conductive copper tape. The source (S) and drain (D) of the sample are connected to the marked electrodes to marked electrode S and D, respectively by 30 μ m Al wire. The cooper wires are soldered to the chip holder and connected by BNC cables which are connected to the voltage source.

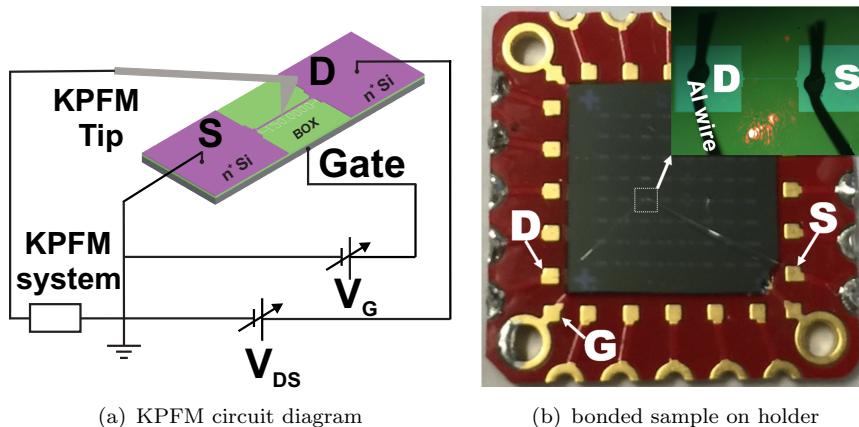


Figure 4.6: The in-situ KPFM measurement electrode connection diagram (a) diagram of KPFM wire configuration. (b) image of sample holder and wire bonding (two black parallel line in top right insert image).

From measured potential profile, the local resistivity is able to be extracted. as the local potential drop along the SiNW channel is measured by KPFM. The flowing equations show how to extract the local resistivity

$$R = \rho \frac{L}{A} , \quad (4.6)$$

$$\rho = \frac{RA}{L} = \frac{V}{I} \frac{A}{L} = \epsilon \frac{A}{I} , \quad (4.7)$$

The ρ is the resistivity of material (n^+ Si), L is the length of SiNW, and the A is the cross-section area of SiNW. Assuming the nanowire is uniformly doped, ρ is expressed in Equation 4.7 with the electric field ϵ which is represented by potential slope along the SiNW. Therefore the local resistivity along the SiNW can be extracted from the slope of the surface potential taken by KPFM scan.

The current density J is expressed by

$$J = \frac{I}{A} = q\mu n\epsilon , \quad (4.8)$$

where the q is the single electron charge, n is free electron density, and μ is electron mobility. Therefore the mobility is then expressed as

$$\mu = \frac{J}{qn\epsilon} = \frac{I}{qn\epsilon A} . \quad (4.9)$$

4.3 Results

4.3.1 Wafer scale resistivity characterisation

After thermal oxidation thinning process the thicknesses of the SOI and the oxide are measured by ellipsometry. The thickness map is shown in Figure 4.7. The SOI thickness map in Figure 4.7(a) shows a circle pattern in the wafer centre and a circular ring pattern round the centre circle. The thickness of centre circle is 62.95 nm and the outer ring is 60.09 nm. The thickness of thermal oxide is more uniformly distributed on wafer in Figure 4.7(b). The average thickness of SiO_2 is 82.27 nm.

Then the 6" wafer was cut into 8 3×4 dies and 4 dummy chip according to the cutting map in Figure 4.8(a). The die1 (D1) is used for the SiNW devices fabrication and its thickness is confirmed by ellipsometry scan with dense sampling points in Figure 4.8(b). The measurement result suggests 3 nm variation in thickness from top to bottom.

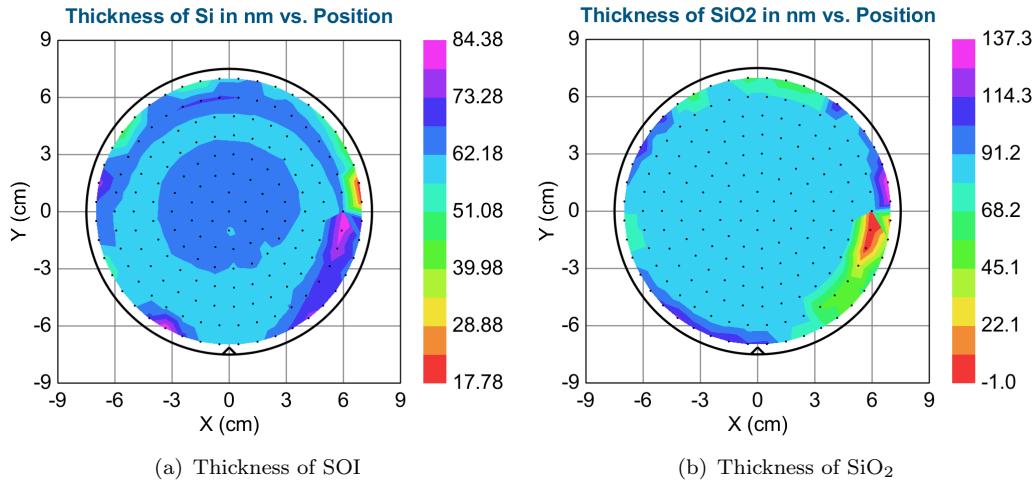


Figure 4.7: SOI wafer thickness mapping after thermal oxidation (a) SiO_2 (b) Si

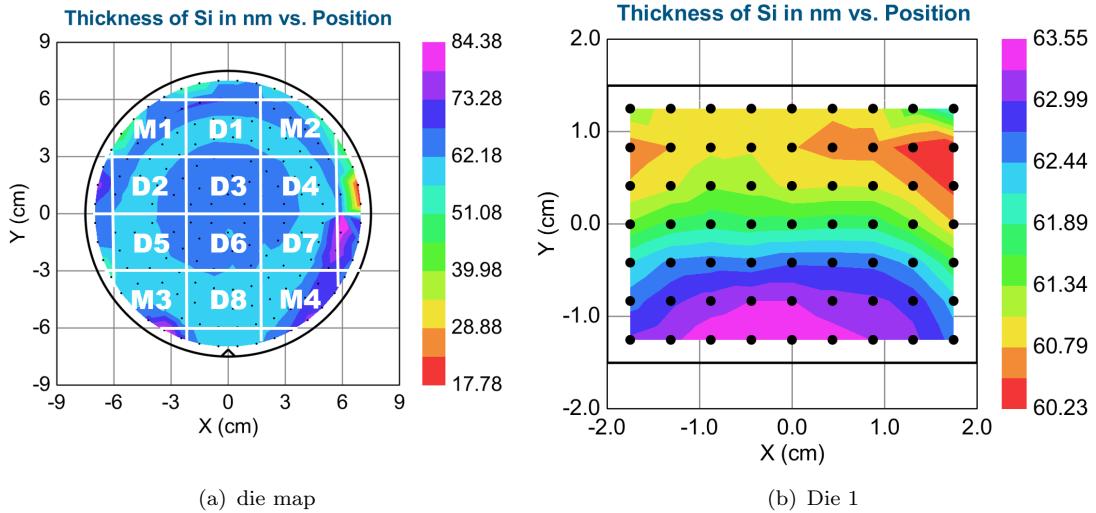


Figure 4.8: Die cutting map and die1 thickness mapping (a) SOI wafer cutting map (b) Thickness map of die1 (D1)

After 30 min diffusion process at $1000\text{ }^{\circ}\text{C}$ and removal of rest SOD the thickness of die was measured again by ellipsometry and the resistivity of dummy SOI chip (M2) was confirmed by both Four Probe and Hall effect measurement. The measurement is shown in Table 4.1. Notice that the Hall measurement shows slightly smaller resistivity value and higher electron concentration which suggests that the value of resistivity can fluctuate in each different measurements.

4.3.2 Resistivity estimation by I-V method

The $I_d - V_d$ curves were taken from total 14 W0.5 SiNW devices in C1 with length from 0.2 to $100\text{ }\mu\text{m}$. Obviously in the same V_d sweeping range the current level decrease as

Table 4.1: Physical parameter of uniformly doped SOI (R_s , ρ , N_d , and μ_e). The values of N_d and ρ from four probe measurement are estimated by bulk Si model in Ref. [68].

	Four Probe	Hall
Thickness t (nm)	30	30
Sheet resistance R_s (Ω/\square)	134.9	84.62
Resistivity ρ ($\Omega\cdot\text{cm}$)	4.047×10^{-4}	2.54×10^{-4}
Doping N_d (cm^{-3})	2.1×10^{20}	1.58×10^{21}
Electron mobility μ_e ($\text{cm}^2/\text{V}\cdot\text{s}$)	73.98	15.6

increasing in SiNW length in Figure 4.9(a). The shortest SiNW has highest slope value and the longest SiNW shows the smallest slope value. The current curve from top to bottom are ranged in the same order as SiNW length L . To extract the accurate value of R_{total} the linear fitting was applied to the SiNW I_d - V_d curve in Figure 4.9(b). The insert residual curve indicate there is small amount error (< 20 nA) between measured value and fitted curve. According to the current level (μA) the error is less than 1%. Notice that the measured I_d start to smaller than fitting when $V_d > 2.5$ V and the difference increases as increasing in V_d . In the end, the value of total resistance R_{total} can be derived by using $R_{\text{total}} = 1/\text{slope}$.

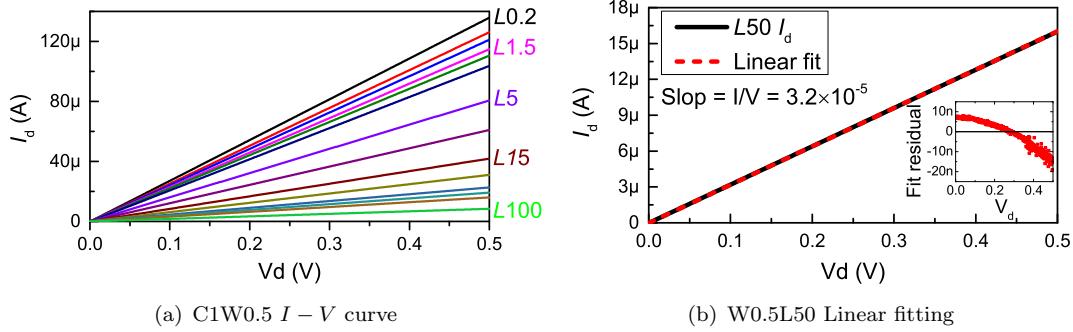


Figure 4.9: $I - V$ curve of C1W0.5 and linear curve fitting (a) $I - V$ curve of C1W0.5 devices (b) linear fitted curve. The fitted slope (I/V) is the average conductivity value in the range of scanned V_d . The fitting accuracy is indicated by insert residual figure ($I_{\text{real}} - I_{\text{fit}}$).

After value of R_{total} fitting by using $I - V$ curve the R_{total} is plotted against SiNW length L in Figure 4.10. The devices with width of 0.5 (Figure 4.10(a)) and 2.5 μm (Figure 4.10(b)) from C1 were measured for three times to check the stability of probing directly on Si surface measurement. In Figure 4.10 the point of R_{total} is well overlapped for repeated measurement to different devices.

The linear fitting of $R_{\text{total}}-L$ was taken to extract the resistivity value ρ and connection resistance R_c . Figure 4.11 shows the fitting curve for both short ($L \leq 10 \mu\text{m}$) and long ($L > 10 \mu\text{m}$) channel SiNW devices. In general the measured R_{total} points is well sitting

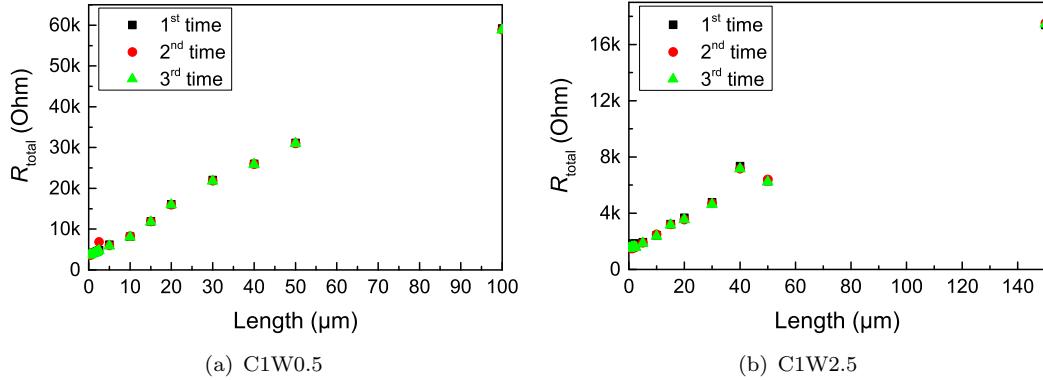


Figure 4.10: $R_{\text{total}}-L$ figure for devices in chip1 (a) figure of short channel devices for both W0.5 and W2.5 (b) figure of long channel devices for both W0.5 and W2.5

around the fitting line. It is worth to notice that resistance fluctuation is relatively large for narrower (W0.5) and shorter devices. This fluctuation was also observed by KPFM scan in the flowing section. In addition, the vale of S_R for both short long channel devices is consistent. The value of S_R is 321.77 and 378.04 $\Omega/\mu\text{m}$ for both short and long W0.5 devices separately and it is 64.95 and 72.74 for short and long W2.5 devices. In the end the fitted R_c values for short channel devices are 2736.29 and 1054.60 Ω for W0.5 and W2.5 separately. On the other hand the R_c for long channel SiNW devices is similar which are 1590.54 and 1189.91 Ω for W0.5 and W2.5. Notice that the lead connection for short channel devices is changing with 1:10 ratio to the width of NW and lead but the lead structure is fixed for long channel devices.

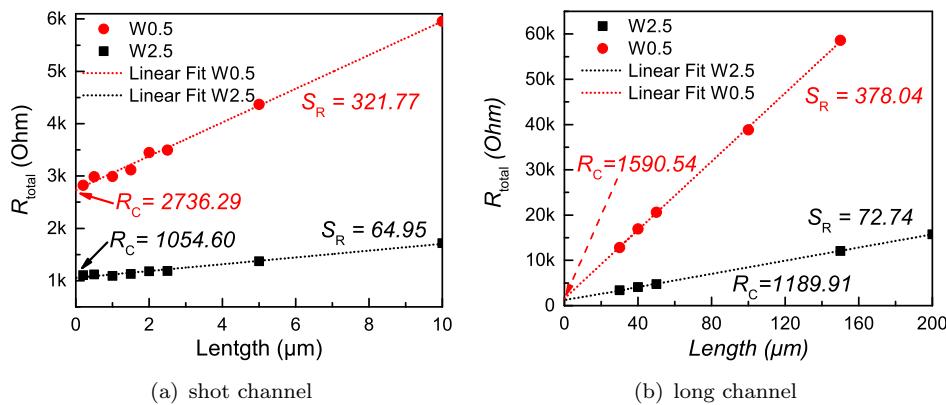


Figure 4.11: Resistivity fitting for both short and long channel (a) figure of W0.5 devices (b) figure of W2.5 devices

The value of S_R can be converted to resistivity by using Equation 4.7. The converted average ρ and fitted average R_c for short channel devices from C1 and C2 are listed in the Table 4.2. The slope value of S_R decreases as the with of SiNW increases for devices in both C1 and C2 chip. After converting the S_R value into sheet resistance by $S_R \times W$ and resistivity you can see the value of R_s is almost equal for all devices in C1.

Meanwhile the value of S_R in C2 for W0.5 and W2.5 is about the same but slightly larger for W20. In addition the resistivity value in the C1 is in the range of $6.73\sim6.91\times10^{-4}$ $\Omega\cdot\text{cm}$ and for C2 is $4.83\sim5.8\times10^{-4}$ $\Omega\cdot\text{cm}$. The value of ρ in C1 is larger than in C6. The ρ in C6 is about 28% to the ρ in C1. In the end, the change in R_c is similar to the change to ρ . The R_c in C6 is about 28% reduction to the R_c in C1.

Table 4.2: Average sheet resistance and resistivity table from $R-L$ linear fitting for short SiNW

Table of short channel ($L \leq 10 \mu\text{m}$) S_R , R_S , and ρ								
	C1 (chip1)				C6 (chip6)			
	S_R ($\Omega/\mu\text{m}$)	R_S (Ω/\square)	$\rho \times 10^{-4}$ ($\Omega\cdot\text{cm}$)	R_c (Ω)	R_S ($\Omega/\mu\text{m}$)	R_S (Ω/\square)	$\rho \times 10^{-4}$ ($\Omega\cdot\text{cm}$)	R_c (Ω)
W0.5	460.55	230.28	6.91	3697.8	321.77	162.38	4.87	2736.3
W2.5	90.2	225.5	6.77	1491.79	64.95	160.89	4.83	1054.6
W20	12.6	224.4	6.73	915.58	9.68	193.51	5.8	731.1

4.3.3 Estimation of charge transport property by simulated and KPFM measured potential

4.3.3.1 Simulated and measured potential map on SiNW

The devices physical model simulation was taken by using Silvaco Atlas. The simulation of surface potential result for 2.5 and -5 V V_d is show in Figure 4.12. The simulated potential is converted to the electron potential which has opposite sign with potential voltage for positive charge carriers. The conversion is for the easy observation of electron moving in SiNW. After conversion the potential value on 2.5 V biased D-lead is lower then potential on the S-lead in Figure 4.12(a). The value of potential also indicates the direction of electron movement e.g. electrons move from S to D through SiNW channel in Figure 4.12(a). In addition the degree of colour change indicates that the gradient of electron potential change is different in wider lead and narrow channel is different which in SiNW channel is larger than in two leads. Particularly there are two semi-circle pattern in the leads at lead-SiNW connection interface at SiNW two ends. What the difference for -5 V V_d is the polarity change of electron potential in lead and scale of potential drop is double.

The short SiNW channel is scanned under different V_d by KPFM. The AFM and surface potential image for $L=2 \mu\text{m}$, $W=0.5 \mu\text{m}$ (W0.5L2) at $V_d=0 \text{ V}$ SiNW is shown in Figure 4.13. In the AFM image (Figure 4.13(a)) the dark red \blacksquare structure which corresponds to the 30 nm SOI devices structure on top of BOX layer. In the AFM image the colour of sample surface is uniform. That suggests the smooth and clean sample surface condition. There are few dots on top of devices can be related to the remaining

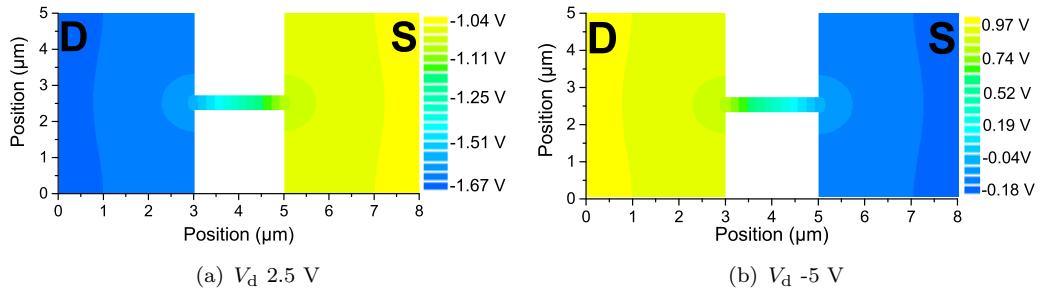


Figure 4.12: Simulation of surface potential distribution for uniformly doped W0.5L2 SiNW devices under 2.5 and -5 V V_d

of resists residue. In addition, the potential of devices emerges from BOX in potential image in Figure 4.13(b). Different from the AFM image the number of spots in devices area is more dense than the number of spots in AFM image. The value of potential change for dots is around 60 mV.

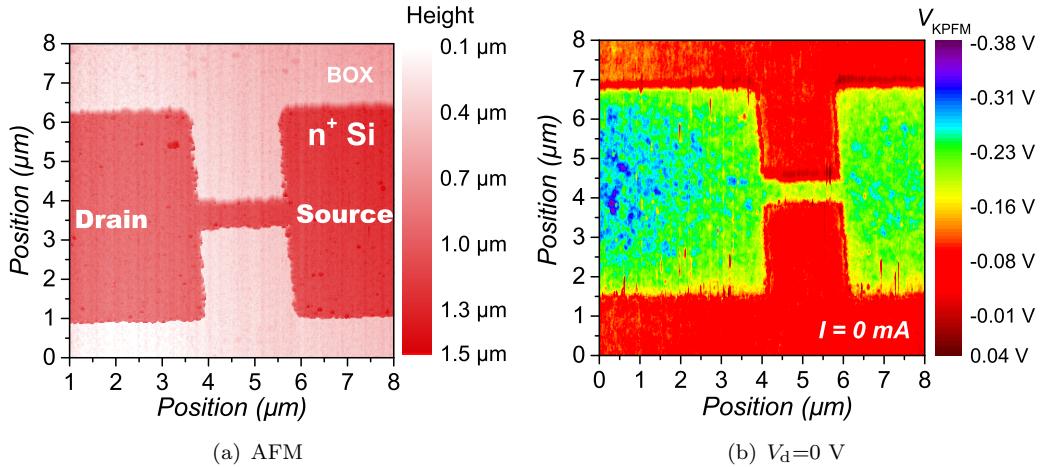


Figure 4.13: AFM and KPFM image of C1W0.5L1.5 SiNW. (a) AFM image. 'D' and 'S' is Drain and Source lead (b) KPFM (relative surface potential) for $V_d = 0$ V.

Different V_d was applied to observe the potential change along the SiNW channel and lead under biasing condition. The scanning result is shown in Figure 4.14 for $V_d = 2.5$ V and $V_d = -5$ V separately. In Figure 4.14(a) for $V_d = 2.5$ V the measured potential value increases from left hand side to right hand side. The gradient of colour change indicate the gradient of potential change on narrow SiNW channel is significantly large than the potential increase gradient in wider lead structure. In addition the density of dot on the lead and SiNW is the same as no biasing condition but the value of potential dots increases from roughly 60 mV to about 200 mV. Further more there is a half circular pattern in the Source lead near the connection area. Once we change the polarity of biasing the direction of potential drop is opposite as well in Figure 4.14. The circular pattern is also moved to the low biased lead side but the size is shrunk as value of voltage

is increased. Meanwhile of V_d changed to -5 V the potential change in dots increased to about 400 mV.

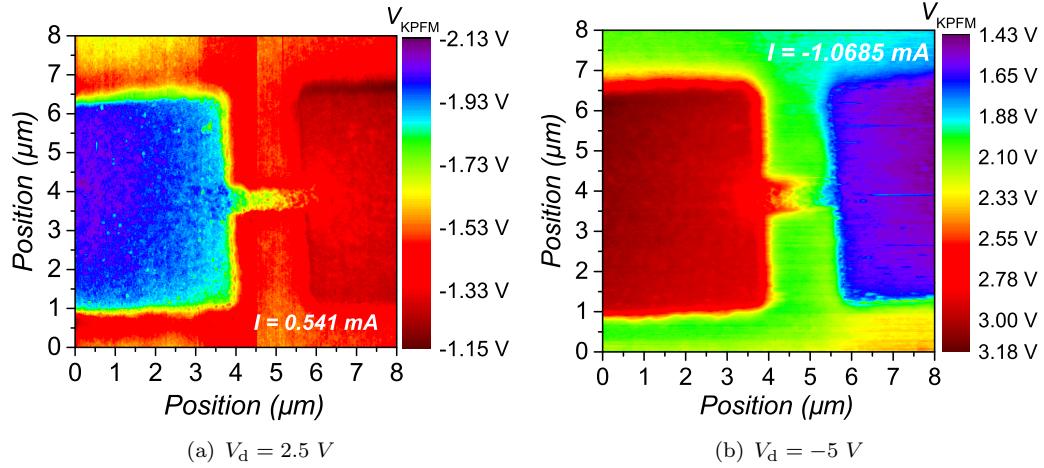


Figure 4.14: Surface potential mapping under 2.5 V and -5 V bias

4.3.3.2 Simulated and measured potential profile on SiNW

The potential (CPD) and electric field profile along X axis direction is extracted from simulated potential map and shown in Figure 4.15. The profile for $V_d = 2.5$ V shows total 0.63 V voltage is dropped in total 8 μm range meanwhile it is 1.15 V for $V_d = -5$ V. The slope of CPD in the SiNW region is obviously larger than that in lead. The value of slope is actually the value of electric field (E) which is equal to dV/dx . The E profile suggests that the E in SiNW is 1923 V/cm ($V_d = 2.5$ V) and 3829 V/cm ($V_d = -5$ V) which about 10 times larger than the value of E which is about 200 V/cm ($V_d = 2.5$ V) and 320 V/cm ($V_d = -5$ V) in leads. The ratio of 1:10 in E can be correspond to the ratio of 10:1 in width for lead and SiNW. In addition the electric field need to take distance to get stable in the connection region. The transition distance inside of the SiNW is around 250 nm for both 2.5 and -5 V V_d meanwhile the transition distance in leads is near 2500 nm for both different V_d . The transition distance ration is 10:1 as well. In the end, the change of E in the connection region is related to the semi-circle pattern in the simulated potential map image in Figure 4.12. That can be related to the charge transport propriety change from wider lead to narrow SiNW.

Scanning probe microscopy imaging results for a SiNW device with $L_{\text{nw}} = 2 \mu\text{m}$ and $W_{\text{nw}} = 500 \text{ nm}$ are summarized in Figure 4.16. Figure 4.16(a) shows topography of the nanowire obtained by AFM scan. The measured thickness of the structure is 35 nm, suggesting the SOI for the area outside the device patterns is well etched out. KPFM surface potential images for the nanowire device under different V_d are shown for $V_d = 0$ (Figure 4.16(b)), $V_d = 2.5$ V (Figure 4.16(c)), and $V_d = -5$ V (Figure 4.16(d)), respectively. At $V_d = 0$, the potential levels of the source and drain leads and the

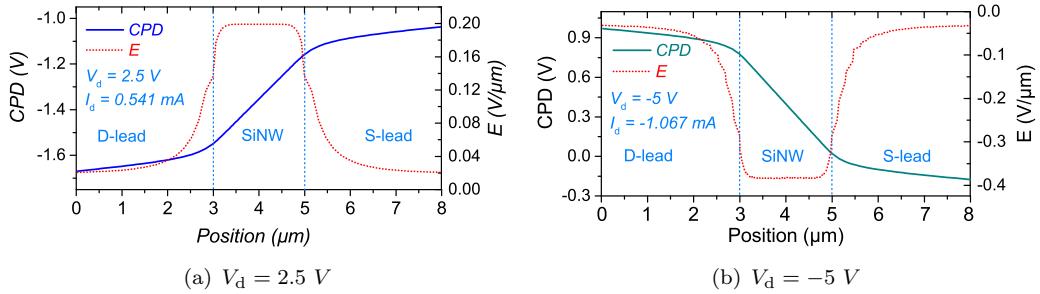


Figure 4.15: Simulated potential and electric field profile along the centre of SiNW and leads for 2.5 and -5 V V_d

nanowire are almost in the same level. The positive V_d makes the potential lower along the channel from the source to drain while the negative V_d offers a flipped potential distribution with respect to the axis across the centre of the nanowire. It is noticeable that characteristic hemispherical pattern of the potential distribution is observed at the both ends of the nanowire in Figure 4.15.

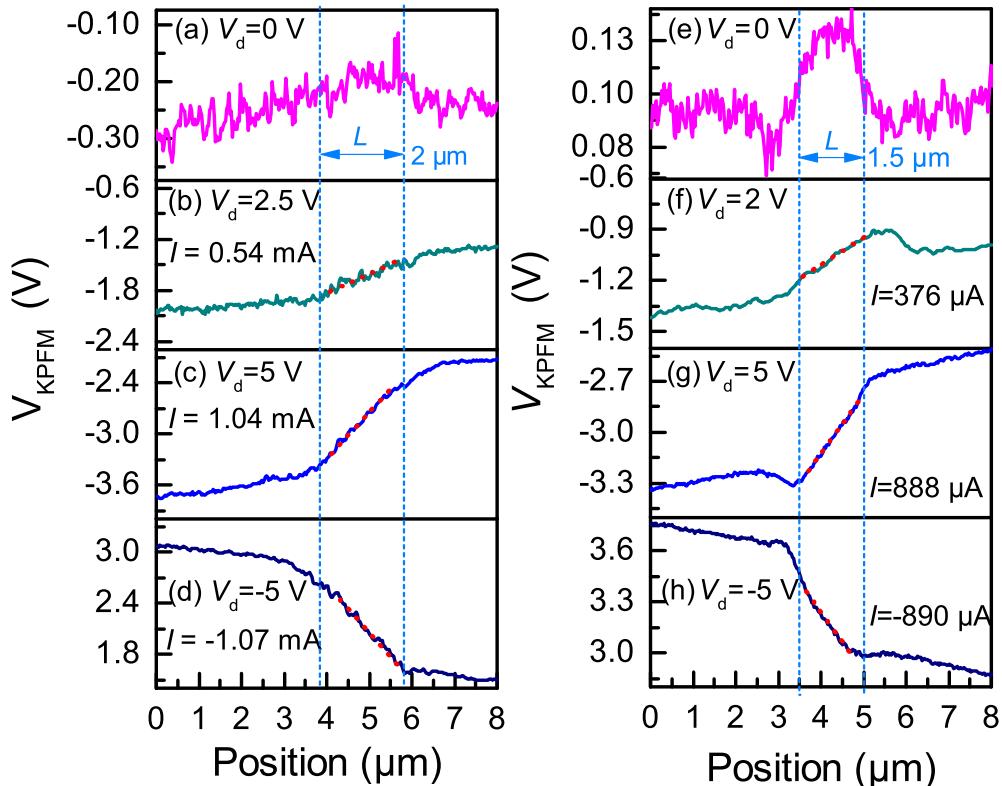


Figure 4.16: Surface potential profile for non-biased C1W0.5L2 SiNW. Left 2 μm channel, right 1.5 μm channel. The red dot line is the liner slope fitting.

For further detailed analysis the potential profiles along the long nanowire axis are extracted in Figure 4.16 (a) - (d) from the surface potential maps in Figure 4.16. At $V_d = 0$ in Figure 4.16(a), whilst a flat profile is expected from a theoretical point of view, a small hump which suggests charge accumulation is identified at the SiNW region.

When the drain voltage of 2.5 V is applied the potential decreases from the source to drain lead through the nanowire as shown in Figure 4.16(b). The slope of the potential profile is steeper at the nanowire than at the leads, as is expected from Equation 4.5 due to the narrower width. When V_d is increased up to 5 V in Figure 4.16(c), the slope becomes much steeper and then almost symmetrical polarity change is confirmed at $V_d = -5$ V in Figure 4.16(d). Note that in particular at $V_d = -5$ V, a kink is observed at the right-hand-side interface between the edge of the nanowire and the lead (at $x = 6 \mu\text{m}$), in spite that a smooth crossover is expected in theoretical calculation shown in Figure 4.16(b).

Samples with different nanowire lengths have been also measured to study size effects. Figure 4.16(e) - (h) shows the KPFM profile along the nanowire with L_{nw} of 1.5 μm . The hump structure with the relative step height of about 50 mV at the nanowire is more prominent in Figure 4.16(e) at $V_d = 0$. For this 1.5- μm -long NW, the potential profiles show clear deviation from the simulations in Figure 4.16. At $V_d = 2$ V in Figure 4.16(f), a clear hump is seen at the right-hand-side edge of the nanowire. When V_d is increased to 5 V in Figure 4.16(g), a characteristic dip and hump structure emerges clearly at the left-hand-side edge. After the polarity changes at $V_d = -5$ V in Figure 4.16(f), this dip and hump is seen at the right-hand-side edge, suggesting this structure is not originated from local inhomogeneity of the structure but associated with how the voltage is applied.

4.4 Discussion

First, the resistivity of the nanowire ρ_{nw} from the KPFM results according to Equation 4.5 is extracted and compare with the wafer-level estimation. The slope in the nanowire region S_{nw} is extracted by linear fitting of the individual potential change at the nanowire. The fitting results are indicated in the Figure 4.16 and the extracted local resistivities are summarised in Table 4.3. First we briefly mention the results of local resistivity estimation of the SiNW devices from the surface potential profile under biasing conditions. The extracted local resistivity is about $5.3 - 7.3 \times 10^{-4} \Omega\cdot\text{cm}$, which are in the same order of the resistivity of $4.02 \times 10^{-4} \Omega\cdot\text{cm}$ from the 4 probe measurement for the doped SOI layer. This coincidence strongly supports that the surface potential measured by KPFM under the current flow directly reflects the bulk transport properties of conductive silicon and shows the usefulness of KPFM to investigate not only static potential profiles but dynamic transport properties of nanodevices.

Next we discuss the difference between the theoretical and experimental surface potential profiles. The hump structure observed at the nanowire region in Figure 4.16(a) and (e) is against theoretical expectation of flat potential distribution through the scan range. This suggests that even at $V_d = 0$, an effective potential barrier is formed against electrons at the nanowire region. The measured contact potential difference V_{KPFM} is primarily

Table 4.3: A summary table of the extracted parameters from KPFM surface potential imaging of the SiNW structure with $W_{\text{nw}} = 0.5 \mu\text{m}$

L_{nw} (μm)	V_d (V)	I (mA)	S_{nw} (V/ μm)	ρ_{nw} ($\Omega\cdot\text{cm}$)
2.0	2.5	0.54	0.192	5.32×10^{-4}
	5	1.04	0.495	7.11×10^{-4}
	-5	-1.07	-0.518	7.27×10^{-4}
1.5	2	0.38	0.161	6.41×10^{-4}
	5	0.89	0.340	5.74×10^{-4}
	-5	-0.89	-0.396	6.68×10^{-4}

associated with the work function which is directly related to the carrier density n in the material. However to explain a 50 mV change of V_{KPFM} , n of the nanowire must be a fifth of the carrier density of the lead region, which is quite unlikely as the samples are fabricated on the uniformly heavily-doped SOI. Excess trapped charges at the surface of the nanowire would be a possible source of this additional potential enhancement. Generally the plasma etching process would introduce charge trap [101] sites at the edge of the fabricated structures since the top surface is covered by 80 nm SiO_2 and 500 nm resists (UVN30) during the etching. In fact KPFM images in Figure 4.13 and Figure 4.14 shows the potential at the edges of the structure is basically higher than that on the bodies. Compared with the lead region, the centre line along the nanowire length is much closer to the edge and as a result, the surface of the nanowire closer to the edge could be exposed to the plasma even through the tiny gap between the surface and the mask. This must be a reason why the nanowire region carries more number of the trapped charges than the lead region. Assuming a simple parallel capacitance model, the tip-sample capacitance is estimated as 1.11 aF by using disk structure of KPFM tip apex with radius of 20 nm and average distance 10 nm from sample surface. According to the relationship, $n = CV/q$, total 0.35 single charge is expected in tip apex area $1.26 \times 10^{-11} \text{ cm}^2$. Therefore the upwards 50 mV electron potential V_{KPFM} shift is expected to be induced by $2.8 \times 10^{10} \text{ cm}^{-2}$ additional negative charge trapped on SiNW channel, which is consistent with a typical value [102] of the charge trap density at the surface of Si.

The deviation of experimental KPFM profile curves from the theory is more remarkable when V_d is applied. The potential hump at the source side and the dip and hump at the drain side interfaces are common feature in this structure. Those anomalies at the edges are most significant at the larger V_d and for the shorter L_{nw} . This can be explained by considering interaction between electric field gradient induced at the nanowire-lead interface and trapped charges. Owing to the abrupt change of the width of the structure, relatively large electric field gradient is induced at the interface by the applied drain voltage. In response to the local electric field gradient, the trapped

charges might be redistributed in the following ways: (1) at the source side, the local dipole is formed with the direction from the nanowire to lead so that negative charges are accumulated on the lead region just outside the nanowire, and (2) at the drain side, the local dipoles with the direction from the lead to nanowire are induced so that positive charges are effectively accumulated on the lead connected to the nanowire. In other words, the mobile trapped charges can work to make the electric field gradient more visible in surface potential measurements. The results suggest that local polarisation is also detectable by applying KPFM for the nanostructure under biasing condition.

4.5 Conclusion

The surface potential profile along the purpose-built surface-exposed conductive silicon nanowire was measured by Kelvin probe force microscopy under source-drain biasing. Local resistivity estimated from the slope of the surface potential at the nanowire is proved well consistent with the wafer-level resistivity evaluation, where we confirm the KPFM can follow the potential drop along the conductive material under biasing. Two remarkable deviations are identified by comparing between the simulation and experimental observation of the potential profile. The potential hump at the nanowire is remained even without biasing and is considered due to the excess trapped charges at the surface. The characteristic hump and dip structures found at the interface between the nanowire and the leads are possibly explained by the additional polarisation induced by mobile surface charges in response to the geometrically formed electric field gradient. To the best of our knowledge, this is the first detailed analysis of the surface potential profile of the conductive silicon nanowire under biasing focusing on the interface with the geometrical change and surface charges. The results would be useful for designing the silicon nanowire sensing devices where the surface and charges around play a vital role for device performance.

Chapter 5

Surface potential characterisation of N-P-N structure

5.1 Introduction

The p-n junction is the fundamental building block of modern semiconductor devices and the n-p-n/p-n-p structure is a key element in MOSFET devices. In the other advanced applications the n-p-n structure is used to construct tunnelling barriers for a single electron transistor [103]. Typically, characteristics of n-p-n structure have been studied by either $I - V$ measurements or simulations. However, considering the advanced scaling down of the channel length and the increasing numbers of opportunities of applications of Si nanowire devices as discussed in Chapter 2, it is important to establish a method observing the formation of physical p-n junction and also the operation of n-p-n structures under changing voltage. This study can be used for optimisation of device fabrication and for designing advanced nano devices.

In this chapter, the charge transport properties through a n-p-n structure is studied through the surface potential information which is obtained by in situ KPFM scan. To help understand the formation of p-n junction, local free charge carrier density change, and local electric field distribution, simulations are conducted by using Silvaco Athena device simulator. How the surface potential behaves depending on the device operational conditions will be demonstrated by comparing the $I - V$ characteristics, simulation, and KPFM observation results for the same device.

5.2 Experimental

5.2.1 Devices design

The structure of devices design is shown in Figure 5.1. In the design, the channel at the centre narrowest with the size of $20 \mu\text{m} \times 20 \mu\text{m}$ is connected by the two leads to the Drain (D) and Source (S) contact pads. The multi-junction in Figure 5.1(b) is formed by doping modulation in the channel area. The pink colour area represents the phosphorous doped n-type SOI and the grey area is lightly doped p-type SOI. By using the substrate as the gate electrode the devices can work as an n-channel FET device.

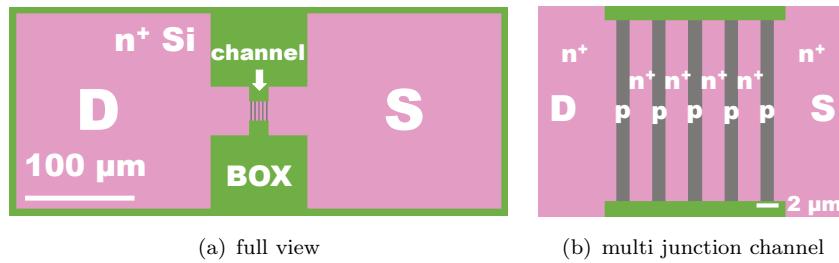


Figure 5.1: Mask design of multi junction devices.

5.2.2 Fabrication

5.2.2.1 Fabrication process overview

Multiple n-p-n junction devices are fabricated on a thinned silicon-on-insulator (SOI) layer. The fabrication process is shown in Figure 5.2. The top SOI layer is thinned down to 60 nm by dry oxidation, resulting in the 80-nm-thick SiO_2 film on the top of SOI. The top SiO_2 is also used as a hard mask to protect the p-type area from dopant diffusion in the subsequent diffusion process. The mask pattern is written by electron-beam (E-beam) lithography in Figure 5.2.b then transferred from the resist onto the SiO_2 hard mask by reactive-ion etching (RIE) process in Figure 5.2.c. After removing the resist the surface is cleaned by 200:1 diluted HF to remove the native oxide on top of the Si surface (Figure 5.2.d). A spin-on-diffusant (SOD) is coated and diffused in furnace (Figure 5.2.e). After diffusion the wafer is dipped in HF to remove the remained diffusant and SiO_2 hard mask in Figure 5.2.f. The device pattern is drawn and transferred to the wafer by using another E-beam lithography (Figure 5.2.g). Figure 5.2.h shows a schematic cross section of the completed devices.

In the following subsections, the detailed devices fabrication processes and characterisation results will be demonstrated. During the fabrication a dummy SOI chip from the same SOI wafer was used to confirm the fabrication conditions by monitoring relevant

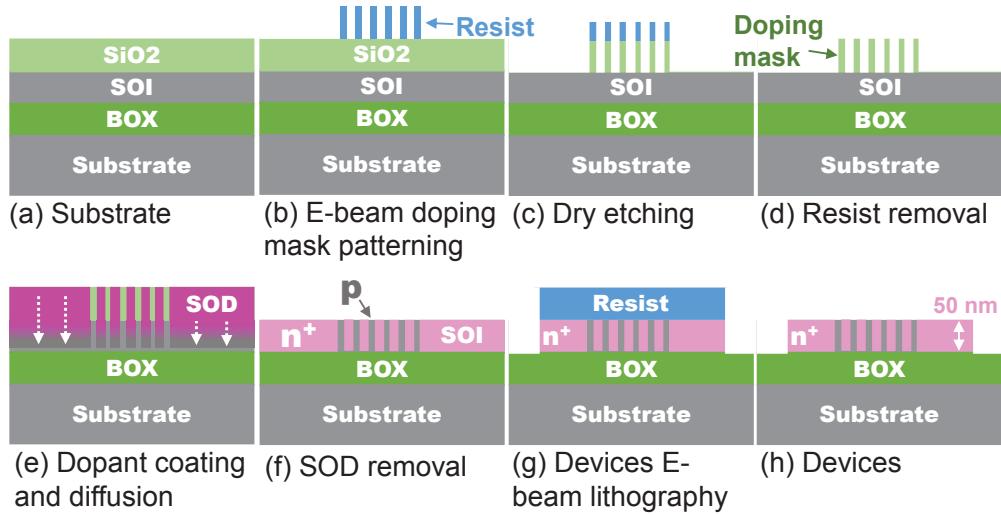


Figure 5.2: Fabrication process of multi-junction devices

physical parameters, *e.g.* etching rate, thickness of oxide, resistivity, thickness of SOI *etc.*

5.2.2.2 Doping mask patterning

The starting wafer was (100) p-type ($N_a \sim 2 \times 10^{14} \text{ cm}^{-3}$) 100 nm Soitec SOI wafer with 200 nm BOX. The device fabrication started from $3 \times 4 \text{ cm}$ chip which is cut from 6" wafer. The die 2 (D2) was used for the devices characterised in this chapter. After cutting the wafer in to the dies the thickness of die 2 is characterised by ellipsometry. The thickness map of the thermal SiO₂ and thinned SOI are shown in Figure 5.3. In the mapping image it is shown that the 82.26-nm-thick SiO₂ film covered uniformly on the central area of the SOI. In addition the thickness of the thinned SOI is around 60.8 to 62-nm-thick in the central area.

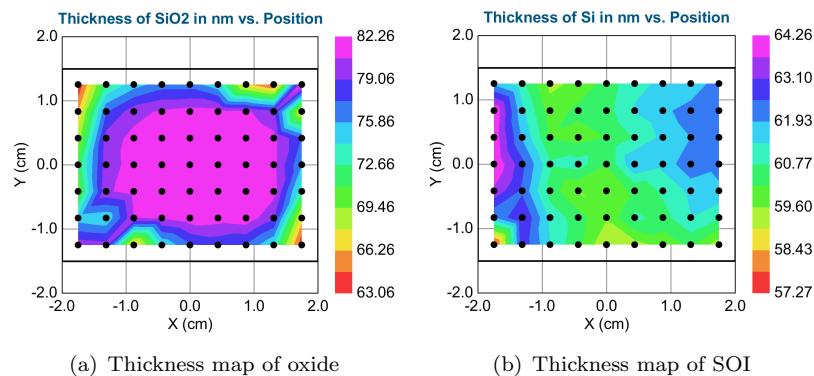


Figure 5.3: Thickness map of starting die for multi n-p-n devices

The electron beam (E-beam) lithography and reactive-ion-etching (RIE) were used to transfer the designed doping mask pattern to the SiO₂ film. In this process, the negative

E-beam resist (Shipley UVN 30) was spun on top of a 3 cm \times 4 cm chip with the spinning speed of 4500 RPM for 30 s. The final resist thickness of 500 nm was confirmed by ellipsometry. Then the resist was exposed by E-beam with the base dose value of 85 $\mu\text{C}/\text{cm}^2$. The acceleration voltage and current level of the E-beam were 100 kV and 25 nA, respectively. After exposing the resist was post-baked at 95 °C for 30 s. The resist was hardened and then developed by immersing the chip in MFCD 26 solution for 30 s then rinsed by DI (deionised) water for 1 min. The pattern of resist after developing was checked by an optical microscope to confirm the success of resist patterning.

After the doping mask was patterned the RIE and wet etching processes by 5% HF were used to transfer the pattern to the SiO_2 film. Three quarters of 80-nm-thick SiO_2 was firstly etched by RIE to get the straight side wall and to avoid further under cut. The etching rate of RIE for SiO_2 was 27 nm/min therefore the etching time of 2.2 min was taken. After that the rest of SiO_2 was etched by 5% HF solution for 30 s. The wet HF etching was selected for final removal of SiO_2 because its high selectivity to Si and minimizing the surface damage. The complete removal of SiO_2 was confirmed by seeing hydrophobic surface and also ellipsometry measurement. The combined process yielded less under cut of the doping mask film under the resist and smoother SOI surface at the same time.

After the pattern was transferred to the SiO_2 film from resist, the remaining resist was removed by a plasma asher with the power of 800 W for 10 min. The size and structure of the pattern were confirmed by an optical microscope (Figure 5.4) after ashing. The exposed SOI shows the bright contrast in the optical images and the area covered by SiO_2 doping mask shows the dark contrast. Figure 5.4(a) shows bar-code-like mask pattern which was used for multiple n-p-n devices.

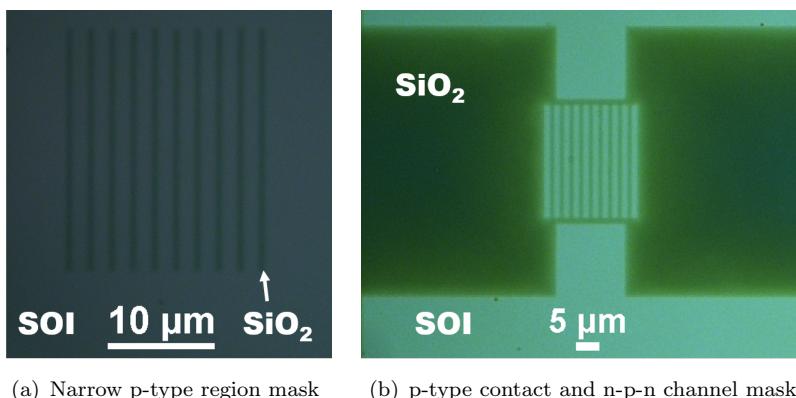


Figure 5.4: Optical image of doping mask for the multiple n-p-n devices.

Before doping, the chip was cleaned to eliminate the metal and organic contamination. In the cleaning process, the chip was firstly immersed in FNA for 10 min to remove the residue of the resist. Then the chip was rinsed by DI water. After rinsing the RCA cleaning process was taken. The 200:1 diluted HF with the SiO_2 etching rate of

1 nm/min was used to remove the 3-nm-thick native oxide which was formed during ashing and cleaning process. The chip was immersed in 200:1 HF for 5 min just before spin-on-dopant coating.

5.2.2.3 Dopant diffusion

The diffusant, Filmtronics P507, was spin-coated on the sample chip just after cleaning process. The P507 was taken out from the stored fridge and warmed up for 12 hrs before use as suggested by the manufacture. Then the diffusant was coated with the spin speed of 2000 RPM for 20 s. After coating the chip was baked at 200 °C for 15 min to drive out the solvents. The film thickness of 200 nm was confirmed by ellipsometry for the dummy chip after baking. Then the chip was put in a drive-in furnace with N₂ gas flow. The drive-in peak temperature was set at 850 °C for 2 min. The furnace started at 200 °C. The temperature ramp rate was set as 5 °C/min, therefore the total process time was 262 min.

The Silvaco Athena simulation was taken to estimate the doping concentration and lateral diffusion length L_d . In the simulator, the diffusant concentration was based on the value of 4% phosphorus in Filmtronics P507. Based on the concentration of phosphorus in P507 the density of dopant concentration is estimated as $4 \times 10^{20} \text{ cm}^{-3}$ and used in the simulation. The temperature setting was the same as the condition we used in the real diffusion process. The doping profile shown in Figure 5.5(a) suggests the exposed SOI was uniformly doped. According to the image, amount of n-type dopants diffused into the region under the mask. The value of L_d is extracted from the doping profile curve in Figure 5.5(b). The simulator suggests 90.63 nm lateral diffusion.

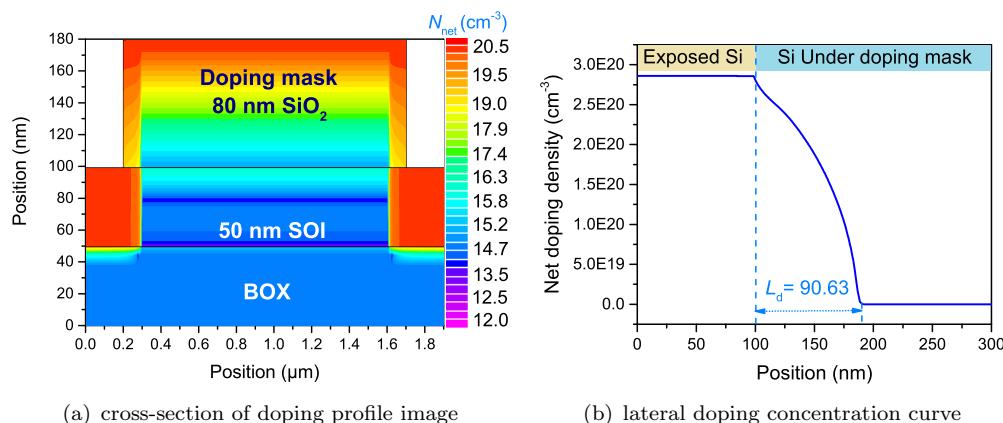


Figure 5.5: Simulation of cross-section doping profile image and lateral doping profile curve.

After diffusion, the sample was observed by the optical microscope. In Figure 5.6(a), the SOD film with the stripe pattern is shown on top of the SOI and doping mask. The stripe might be caused by SOD morphology change under high annealing temperature.

The doping mask marked by an arrow in Figure 5.6(a) under the SOD film is clearly seen. These remained SOD film and SiO_2 doping mask were removed by 5% HF solution for 6 min. The complete removal of the SOD layer and hard mask was confirmed by ellipsometry measurement on the dummy chip. Another optical image in Figure 5.6(b) was taken after surface cleaning. It is seen that the doped and intrinsic area are clearly distinguished by the contrast difference. The undoped area is darker in the optical image.

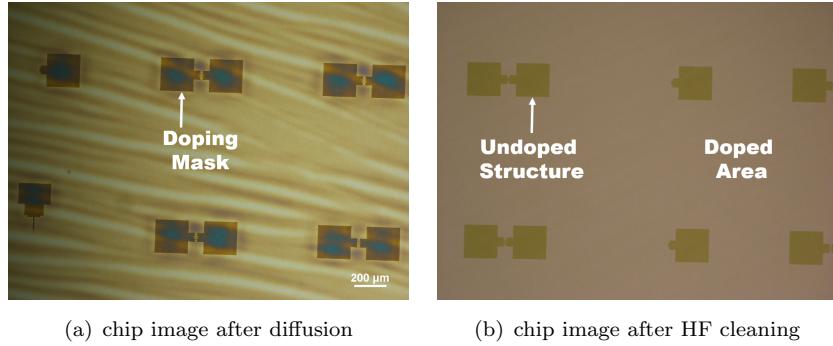


Figure 5.6: Optical image of chip surface after diffusion and remaining SOD removal.

The measured physical parameters from the dummy chip M2 are listed in Table 5.1. The M2 was from the same wafer and also processed together with the device, chip therefore the measured parameters are assumed the same as the devices chip. The thickness t of SOI chip was measured again by ellipsometry. The rest of the parameters were characterised by Hall effect measurement. The contact electrodes were deposited on the M2 after SOD removal and then the chip was annealed by Rapid-Thermal-Annealing (RTA) at 450 °C for 40s. The electrodes were put at four corner of 1 cm × 1 cm chip. In total three small chips were made based on the M2 die to check the uniformity of doping.

Table 5.1: Table of SOI wafer physical parameter after dopant diffusion.

Method	Sample	t (nm)	$N_d \times 10^{19}$ (cm $^{-3}$)	R_s (Ω/\square)	$\rho \times 10^{-3}$ ($\Omega \cdot \text{cm}$)	μ (cm $^2/\text{Vs}$)
Hall Effect	Chip 1	50	1.17	1953	9.77	54.6
	Chip 2	50	1.55	1729	8.65	46.5
	Chip 3	50	1.05	2072	10.36	57.6
Four probe	M2	50	0.1	4500	22.5	276.9

The measurement result of the remained thickness of SOI of 50-nm-thick after dopant diffusion shown in Equation 5.1 suggests that 10-nm-thick SOI was consumed in SOD diffusion. The consumption of 10-nm-thick Si is explained by oxide diffusion from the SOD material under high temperature. In addition, the measured doping concentration

N_d is around $1 \times 10^{19} \text{ cm}^{-3}$. The doping variation from three chips is small so that we can assume the sample is uniformly doped. The sheet resistance R_s and resistivity ρ correspond to the doping concentration. The mobility of doped SOI is estimated to be $55 \text{ cm}^2/\text{Vs}$. The value measured above will be used devices study in the flowing discussion.

5.2.2.4 Fabricated multiple n-p-n devices

After the doping process, the chip was then ready for device patterning. The negative E-beam resist UVN30 was used again for the device patterning. The E-beam resist patterning process is the same as the one used for doping mask patterning. After transferring the designed device pattern was exposed onto the resist the RIE was used to transfer the resist pattern on to the SOI layer. The etching time was 20 s in O_2/SF_6 chemistry with the gas flow rate of 2.0 sccm for O_2 and 18 sccm for SF_6 , respectively, resulting in etching time with 15% over etching. The etching rate of Si which was tested in advance for a dummy chip was 300 nm/min. After etching, complete removal of unwanted SOI was confirmed by ellipsometry measurement.

Optical microscopy images of a final device structure are shown in Figure 5.7. The bright blue colour indicates the existence of an n-type SOI layer and the dark blue is the area where the BOX is exposed after etching. The large areas with the size of $200 \mu\text{m} \times 200 \mu\text{m}$ are the source and drain contact pads. The contact pads are directly proved in the I-V characterisation and wire-bonded for KPFM measurements. The two $40 \mu\text{m} \times 40 \mu\text{m}$ square structures between the S/D pads are the leads which connects the multiple n-p-n channel in the centre to the contact pads. These two leads are used to increase the distance between the contact points for easy excess of the KPFM cantilever. The square with the size of $20 \mu\text{m} \times 20 \mu\text{m}$ at the centre is the multiple n-p-n junction channel. Doping concentration is modulated in this region. A blow-up of the channel is shown in Figure 5.7(b). The area in darker blue colour pointed by arrows with a label 'p' is the undoped area. A part of this area will be scanned by KPFM to study the real potential change under different biasing conditions.

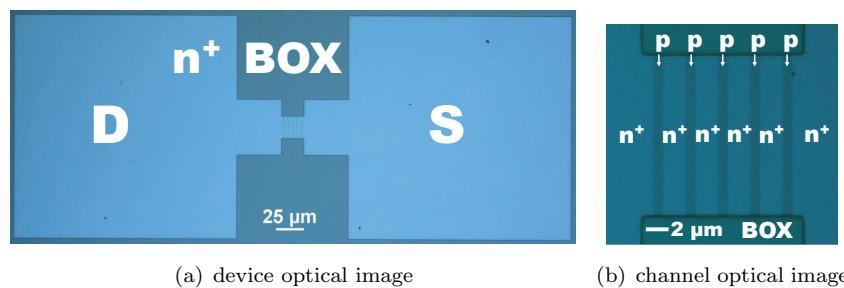


Figure 5.7: Optical image of fabricated multi-junction devices.

5.2.3 I-V characterisation

Prior to KPFM characterisation, we measured electrical characteristics of the device by using a standard probe station (Cascade M150) and device parameter analyser (Agilent B1500). Besides, in-situ $I - V$ characterisation was done by using a source meter (Keithley 2401) which is connected to the source and drain of the device. The bottom substrate is also electrically connected to apply the back-gate voltage. This offers KPFM cantilever to access the surface of the FET channel under different biasing conditions.

5.2.4 Surface potential measurement and electric field extraction

Figure 5.8(b) shows a real optical image in scanning. The Al wire is bonded to the contact pad whereas the KPFM tip cantilever is suspended on top of device to scan the surface to obtain both topography and potential information. The scanned n-p-n channel area which will be discussed in this chapter is shown in Figure 5.8. The two adjacent n-p-n structures showed almost identical behaviour so in the discussion a single n-p-n structure will be focused.

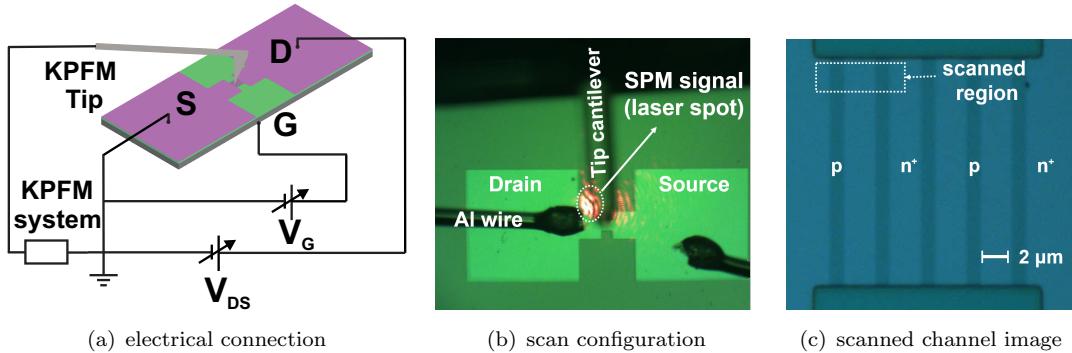


Figure 5.8: KPFM measurement.

5.3 Results

5.3.1 I-V characteristics of multiple n-p-n channel devices

5.3.1.1 Experimental $I - V$

The experimental $I_d - V_g$ characteristics for multiple n-p-n structure FET is shown in Figure 5.9. By eye guide in this figure we can see the device turns on at $V_g = 0.7$ V and the current increases linearly until $V_g = 5.8$ V where the steep slope suddenly turns to be gradual. It suggests the I_d is saturated at this point. By looking at the I_d curve form the threshold voltage $V_{th} = 0.7$ V to the negative direction, relatively subthreshold current

is seen in the range of $-2.5 < V_g < 0.7$ V. The subthreshold current is suppressed below 6×10^{-9} A in the range of $-5.8 < V_g < -2.5$ V. At larger negative voltage, $V_g < -6$ V, the leakage current increases again as is shown in $\log(I_d)$ curve. This current is due to hole conduction in the n-p-n structure. The $I_d - V_d$ characteristics shown in Figure 5.9, also show modulated drain current by back-gate biasing and shows linear behaviour.

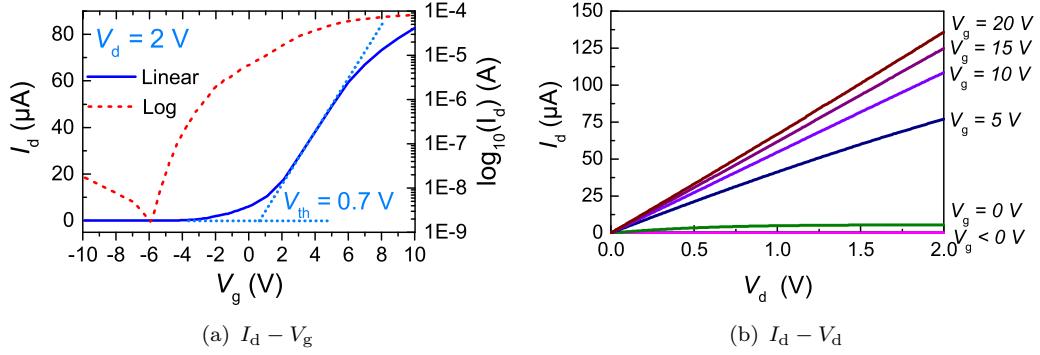


Figure 5.9: Experimental $I_d - V_g$ and $I_d - V_d$ curve. The channel is 50 nm thick, 2 μ m long, and 2 μ m wide.

5.3.1.2 Simulated $I - V$

$I - V$ characteristics shown in Figure 5.10 are numerical results for an FET with single n-p-n structure studied by 2D Silvaco Atlas simulation. According to the $I_d - V_g$ curve in Figure 5.10(a) the V_{th} is 0.9 V which is 0.2 V larger than the experimental value the saturation point is almost consistent with the experimental value at $V_g = 5.8$ V. In addition there is still small amount of sub-threshold leakage current in the range of $-0.5 \leq V_g \leq 0$ V and then is suppressed after $V_g < 0$ V until $V_g = -5.5$ V. Similar to experimental measurement I_d increases at $V_g < -5.5$ V but the current level is relatively smaller (1×10^{-17} A). The $I_d - V_d$ curves in Figure 5.10(b) suggest the current saturation in the model starts at lower V_d .

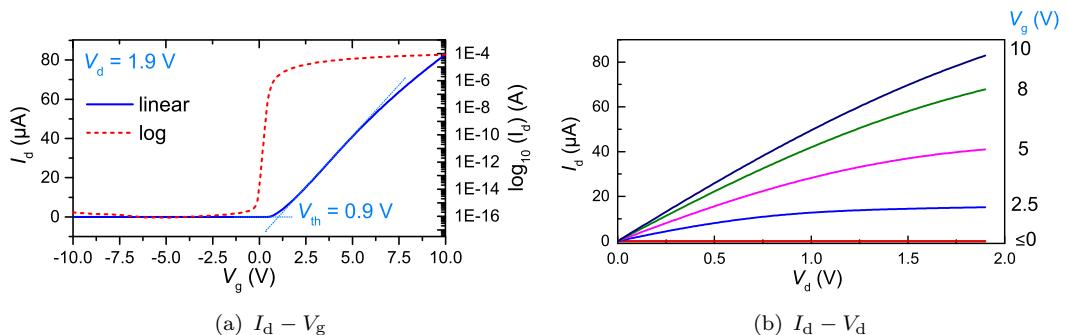


Figure 5.10: Simulated I-V curve of single n-p-n devices. The channel is 50 nm thick, 2 μ m long, and 2 μ m wide.

5.3.2 Surface potential and vertical potential profile of doping modulated 50 nm SOI under static gate biasing

5.3.2.1 Surface potential image of Multiple n-p-n structure by KPFM

The potential change on fabricated devices was scanned under different static gate voltages. Figure 5.11(a) shows a topographic image of the scanned area shown in the inset of Figure 5.7(a) covering two adjacent n-p-n structures. Due to the local oxidation in the diffusion process the doped n-type area is about 10 nm lower than the undoped intrinsic area, where the doping mask was covered. Surface potential imaging via KPFM at $V_g = 0$ V and -5 V are shown in Figure 5.11(b) and Figure 5.11(c). The potential of p region, ϕ_{sp} , is higher than that in n region, ϕ_{sn} , at $V_g = 0$ V, whereas $\phi_{sp} < \phi_{sn}$ at $V_g = -10$ V.

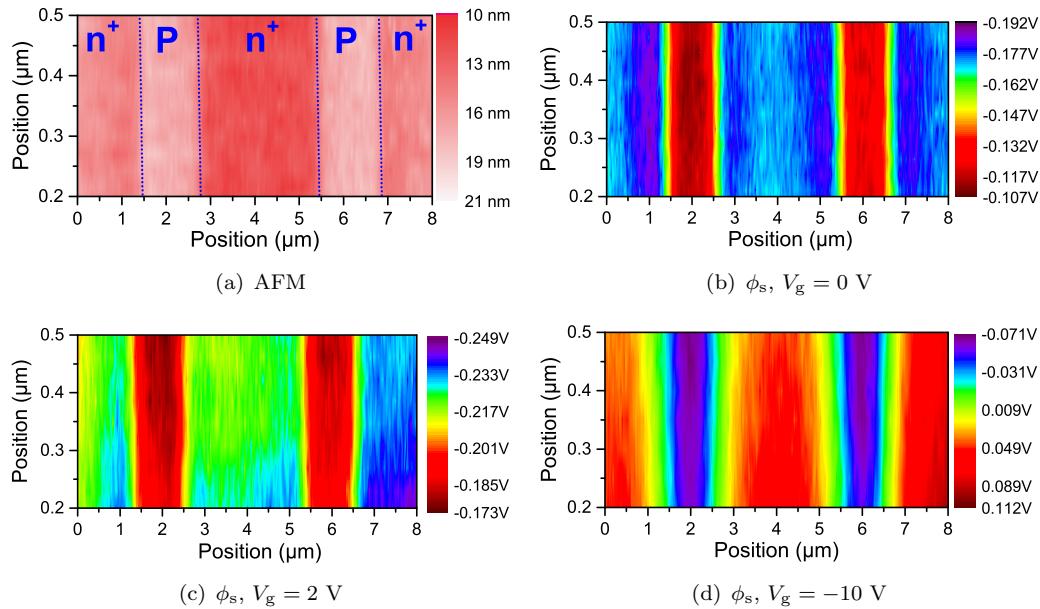


Figure 5.11: The images of measured topography and surface potential under gate biasing.

5.3.2.2 Simulation study of vertical potential and charge density distribution in SOI under gate biasing

To understand the vertical potential distribution in the thin SOI film is important for the purpose of investigating SOI-FET devices by looking with surface potential information. In this section, the potential distribution along the perpendicular axis to in 50-nm-thick SOI film is simulated for the n-p-n structure various V_g . Here, both the vertical potential ϕ and hole density p profiles in the n- ($1 \times 10^{18} \text{ cm}^{-3}$) and p-type ($2 \times 10^{14} \text{ cm}^{-3}$) regions are shown under the 3 different static V_g . For simplicity to eliminate the offset voltage

V_{fb} , the doping concentration of the substrate for gating was set the same as the p-type region in SOI.

The simulated potential (ϕ) and hole concentration (p) along the perpendicular axis to the n-p-n channel in 50-nm-thick SOI are plotted in Figure 5.12. In Figure 5.12(a) both ϕ_p and p shift upwards when V_g decrease. By looking at the vertical distribution (from the position 0 to 50 nm, 0 corresponds to the surface of the SOI and 50 nm corresponds to the interface between SOI and BOX layers) the ϕ and p curve are slightly bended. The bending starts from near the gate side and ends at the surface. The bending direction is different when the polarity of V_g is changed. Here the negative V_g results the near gate side (50 nm) bends up slightly in contrast to the positive V_g results showing bending downwards. The total potential difference $\Delta\phi_{tb} = \phi_{top} - \phi_{bottom}$ from the surface to bottom are -13.7, -0.48 and 14.1 mV for $V_g = -0.5$, 0 and 1 V, respectively. The change in hole concentration follows the trend of change in ϕ in SOI. From the top to bottom, the hole density on the top surface is 0.6, 0.98, and 1.73 times larger than the hole density in the bottom of the SOI at $V_g = -0.5$, 0, and 1 V, respectively. The results here suggest that both the ϕ and p distributions are almost uniform in the p-region from the top to the bottom of the SOI. The magnitude of the hole concentration in the p region is significantly modulated by V_g between $2 \times 10^4 \text{ cm}^{-3}$ and $1.2 \times 10^{16} \text{ cm}^{-3}$ for V_g from 1 V to -0.5 V.

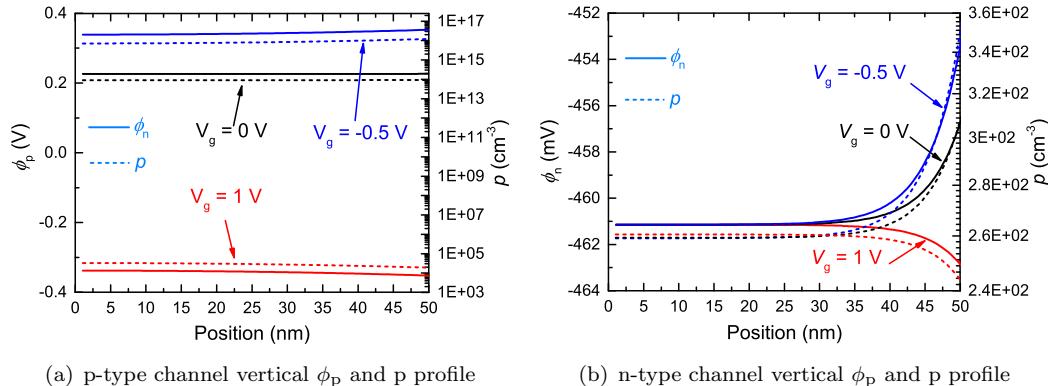


Figure 5.12: Vertical potential and hole density profile in both p and n-type 50 nm SOI under different V_g . The left to right hand side is the surface to BOX direction.

The ϕ and p distribution in the n-type region in Figure 5.12(b) is different from that in p-region. In changing V_g , ϕ is almost fixed near the surface but starts to bend at the depth of 30 nm from the surface for. Note that the bending upwards at $V_g = 0 \text{ V}$ is related to the work function difference between the p-type substrate and the n-type region on SOI. The degree of ϕ bending is related to the polarity and magnitude of V_g . The magnitude of $\Delta\phi_{tb}$ are -7.78, -4.25, and 1.64 mV for $V_g = -0.5$, 0, and 1 V, respectively. The trend of the p change in SOI also follows the change of the ϕ_s profile. The value of p does not depend on V_g on the top surface but starts to bend at the depth

of 30 nm from the surface. Here the p concentration at the surface is 1, 0.8, and 0.7 times of p concentration at the bottom.

By this simulation along the depth direction, conclusion is that in the back gated n-p-n FET, ϕ and p inside the low-doped 50-nm-thick p-type region are almost uniformly distributed. Therefore, the measured surface potential is regarded as the potential change in the p-type SOI film due to back-gate biasing. The surface potential on the grounded heavily doped n-type SOI film should be fixed and the free charge carrier density only changes in the range of 15 nm from the bottom of the SOI film. This information is important for the analysis of surface potential profile for SOI-FET devices via KPFM.

5.3.3 Surface potential profile of FET channel under static gate biasing

5.3.3.1 Experimental surface potential profile

Figure 5.13 shows the surface potential profile across a single n-p-n structure under various gate voltages. At $V_g = 0$ V, the surface potential increases from $\phi_{sn} = -0.13$ V at the left-hand-side n-type region to $\phi_{sp} = -0.08$ V at the central p-type region through the pn junction. This behaviour is common for the right-hand-side p-n junction. In Figure 5.13(a), with increasing positive V_g both ϕ_{sn} and ϕ_{sp} decreases. But the ϕ_{sp} decreases more rapidly than ϕ_{sn} and finally ϕ_{sp} and ϕ_{sn} become almost at the same level at $V_g = 5.2$ V which is corresponded to the current saturation in $I_d - V_g$ figure (Figure 5.9(a)). In addition the change in surface potential profile in Figure 5.13(b) under negative V_g biassing is different from the curves under positive V_g in Figure 5.13(a), which ϕ_{sn} increases with decreasing V_g while ϕ_{sp} shows non-monotonic change. ϕ_{sp} increases until $V_g = -2.2$ V and then turns to decrease. Corresponding to the $I_d - V_g$ curve, the leakage is suppressed at -2.5 V. It is notable that ϕ_{sp} becomes lower than ϕ_{sn} when $V_g = -5.8$ V is applied. Refer to the $I_d - V_g$ curve again the hole current start to increase at $V_g = -5.8$ V.

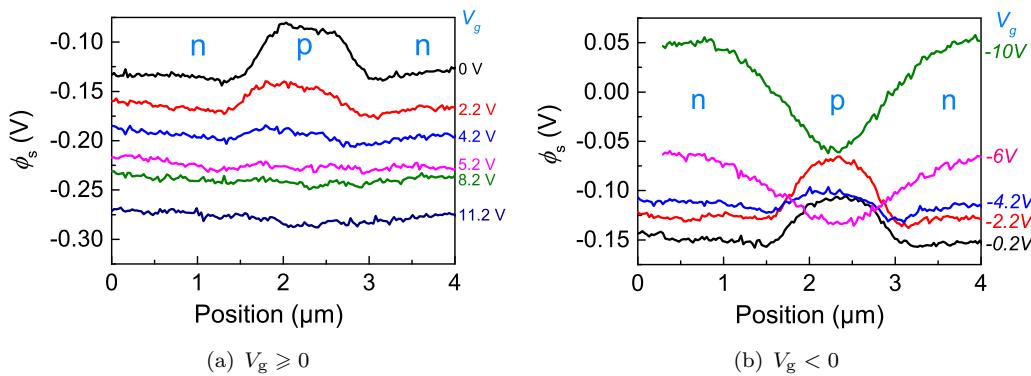


Figure 5.13: Surface potential value against different applied V_g at $V_d = V_s = 0$ V.

In Figure 5.14, ϕ_{sp} , ϕ_{sn} , and $\Delta\phi_{pn}$ are plotted as a function of V_g . The ϕ_s on both p and n-type regions follows the change of V_g . However the simulation suggests in heavily doped n-type regions the change in ϕ is only a few mV for the position 20 nm above the SOI-BOX interface and ϕ_{sn} is always fixed in Figure 5.12(b). In the experiment result the value of ϕ_{sn} goes down monotonically in the V_g scanning range, while ϕ_{sp} shows non-monotonic change. The value of ϕ_{sn} increases when V_g is swept from the positive to negative direction until the current suppression point at $V_g = -2.2$ V, and then suddenly drops down until the hole conduction starts at $V_g = -5.8$ V. At $V_g < -5.8$ V, ϕ_{sn} increases again.

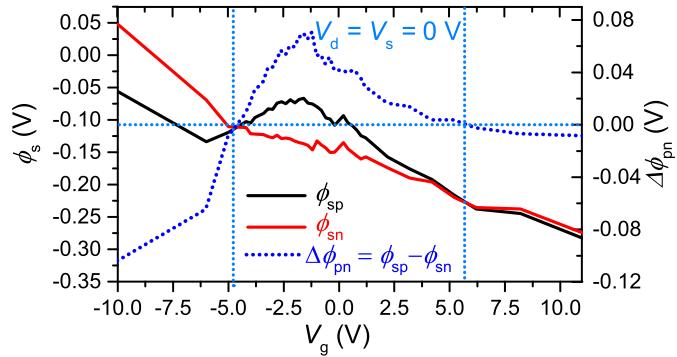


Figure 5.14: The V_g dependent surface potential value ϕ_s form n and p area. The dark blue break line present the value of $\Delta\phi_{sp}$.

To clearly see the potential change in n-p-n structure, $\Delta\phi_{pn}$ is expressed by removing the possible offset in ϕ_{sn} as

$$\Delta\phi_{pn} = \phi_{sp} - \phi_{sn} . \quad (5.1)$$

The $\Delta\phi_{pn}$ curve in Figure 5.14 intercepts the zero line twice, one at $V_g = -4.8$ V and another at $V_g = 5.8$ V. Particularly the one cross over at 5.8 V is close to the current saturation point. The other cross over is close to the hole conduction point which suggest the change in hole density in SOI film. Furthermore, the peak $\Delta\phi_{pn}$ value 70 mV is clearly shown in the $\Delta\phi_{pn}$ figure at $V_g = -2$ V which is corresponded to the leakage current suppression point. Correspondence between these characteristic features in CPD change and the $I_d - V_g$ characteristics in Figure 5.9(a) will be discussed later.

5.3.3.2 Simulated surface potential profile

The surface potential difference $\Delta\phi_{pn}$ between the centre of p-type region (ϕ_{sp}) at the position of 2.25 μm in Figure 5.15(b) and n-type regions is plotted in Figure 5.15(a) and indicates that the value of $\Delta\phi_{pn}$ decreases monotonically as a function of V_g . The $\Delta\phi_{pn}$ figure is able to be divided into three sections according to the change in gradient, indicating the value of ϕ_{sp} changes rapidly in the range of $-0.2 < V_g < 0.9$. Refer to

the simulated $I - V$ curve, the rapid ϕ_{sp} change region corresponds to the sub-threshold region. The change of $\Delta\phi_{pn}$ becomes linear after $V_g > V_{th}$. It is noticeable that the simulation cannot give the the surface potential change when $V_g < -0.5$ V therefore the $\Delta\phi_{pn}$ for $V_g < -0.5$ V is missing. Particularly, $\Delta\phi_{pn}$ shows anomaly twice in changing V_g during the V_g sweeping. On anomaly is at $V_g = -0.2$ V and the other is at $V_g = 0.54$ V.

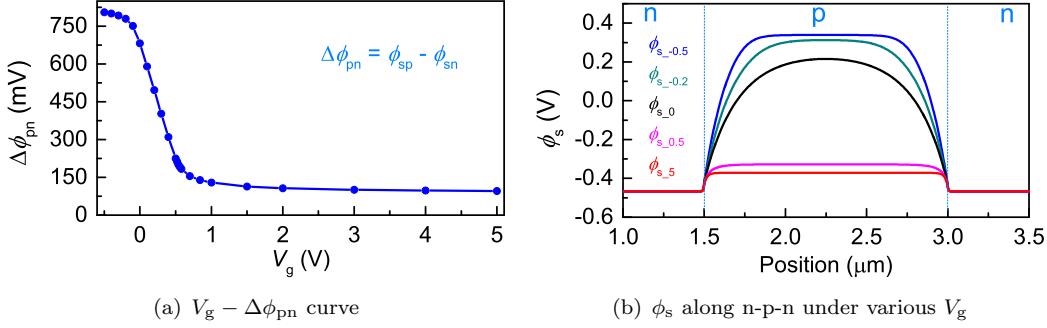


Figure 5.15: Gate voltage dependent (a) surface potential at centre p and (b) potential profile on top SOI. The value in the suffix of the notation represent the value of gate voltage e.g. $\phi_{s,-0.5}$ is the surface potential curve for $V_g = -0.5$ V.

In observing the surface potential profile in Figure 5.15(b), the transition length is defined as the distance for ϕ_s to raise up from the lowest in n-type regions to the maximum peak value in p-type region. The change in the potential profile is used to indicate the change of the density of free charge carriers and also the reformation of depletion region in p-n junction. The ϕ_s is fixed at -467 mV in n-type regions which is away from the p-n interface. The value of ϕ_s starts to increase at the position of 21 nm away from p-n interface until a point in the p-type region and then becomes flat. The peak value ϕ_s and peak position depends on the value of V_g . In the Figure 5.15(b) the ϕ_s goes to maximum (338.8 mV) at $V_g = -0.5$ V and minimum (-371.6 mV) at $V_g = 5$ V. In addition the transition length in n-type region is shorter than in p-type region. Typical transition length is 21 nm in the n-type regions for all V_g . The transition length in the p-type region is related to the value of V_g . The transition length changes from 750 nm (0 V biased centre of p-type region) to 24 nm (positively biased).

To understand the behaviour of free charge carriers under static gate biasing, the surface hole density profile is plotted in a semi-log scale in Figure 5.16(a). $I_d - V_g$ curve in Figure 5.10(a), the current dramatically increases at $V_{th} = 0.9$ V. Here the hole density is reduced from $6 \times 10^{13} \text{ cm}^{-3}$ when $V_g = 0$ V to $1.7 \times 10^5 \text{ cm}^{-3}$ when $V_g = 0.9$ V. According to the relationship $n_i^2 = np$, we know the electron density in the entire channel is increased to $2.9 \times 10^{14} \text{ cm}^{-3}$ for large conductive current by using $n = n_i^2/p$. By further increase in V_g to 5 V, the hole density is reduced to $8.3 \times 10^3 \text{ cm}^{-3}$. This deduction of the hole concentration explains the further increase of I_d and delay the I_d saturation point to larger V_g . The hole concentration is increased by negative V_g . When V_g is reduced to

–0.5 V the hole density in the centre p-type region is increased up to $7.1 \times 10^{15} \text{ cm}^{-3}$. This change can be related to the reduction of sub-threshold current in the range of when $-0.5 \leq V_g \leq 0 \text{ V}$ in Figure 5.10(a). Particularly in simulation results, the length of the flat potential region with the maximum potential value is different depending on V_g . At large positive V_g the hole concentration profile shows the longer flat region whereas p at $V_g = 0 \text{ V}$ shows the shorter length. The maximum p concentration value at $V_g = 0 \text{ V}$ is slightly smaller than the acceptor concentration N_a . Ideally the hole density should follow the equation of $p = N_a$ in a non-degenerated semiconductor without influence of bias at room temperature. The bending of hole density profile and reduction of the maximum value suggest lateral thermal diffusion of electrons from high concentration n-type regions to low concentration p-type region.

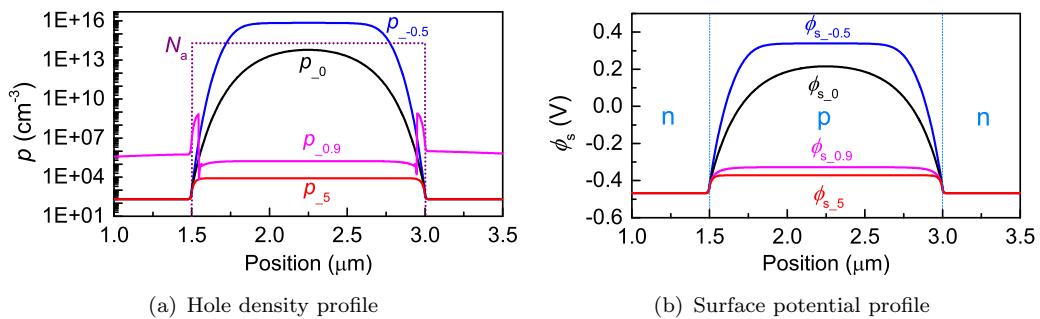


Figure 5.16: V_g dependent surface hole density and potential profile along n-p-n channel. The value in the suffix of the notation represent the value of gate voltage e.g. $p_{-0.9}$ is the hole concentration curve at $V_g = 0.9 \text{ V}$.

The hole density curve in Figure 5.16(a) under various V_g is similar to the potential profile in Figure 5.16(b) V_g . This phenomenon suggests that the charge carrier density is exponential to the potential value. The p density curve at $V_g = 0.9 \text{ V}$ shows particular distribution in the n-type region at the p-n junctions. This might be related to the difficulty of calculation in the simulator. The relationship will be illustrated in the following discussion section.

In the experimental data, the similar monotonic change was only observable in the range of $V_g \geq -2.2 \text{ V}$. The ϕ_{sp} line goes down when $V_g < 2.2 \text{ V}$. In simulation, the change of $\Delta\phi_{pn}$ is monotonic but the slope changes when the polarity of V_g is changed.

5.3.4 Electric field profiling and metallurgical junction

According to Poisson's equation, electric field reveals the change in net charge density and the drift current is also related to the lateral electric field in the device channel. Thus the formation of p-n junction and charge transport behaviour inside the devices is able to be analysed in detail by looking at electric field distribution. The lateral electric field E_x distribution along the FET channel was extracted from the KPFM potential profile by the following equation

$$E_x = \frac{d\phi_s}{dx} , \quad (5.2)$$

where x is the position on x-axis which is along the channel direction. The measurement result was noisy, so that the Loess smoothing function [104] was used to smooth the potential curve. From the profile of E_x the net charge (ρ_{net}) distribution inside of semiconductor is derived from Poisson's equation,

$$\rho_{\text{net}} = \frac{dE_x}{dx} . \quad (5.3)$$

According to Equation 5.3, the non-zero E_x is equivalent to presence of the net charge and the gradient of E_x correspond ρ_{net} at a position x .

5.3.4.1 Experimental electric field profile

Figure 5.17(a) shows the measured topography (dotted line) and surface potential (solid line) profiles cross an n-p-n channel. The ϕ_s curve shows that the measured potential for electron on p-type region is about 50 mV higher than that on the n-type region as a result of electron-hole recombination in the space charge region. ϕ_s takes about 530 nm rise from lower flat level to peak value at both left and right terminal of p-type region. The height difference between the n and p region is indicated by the AFM curve. The p-type area is about 9 nm higher than n-type areas as a result of local oxidation of SOI in diffusion process. This point is also confirmed by ellipsometry measurement. The width of higher region can be used to indicate the actual width of doping mask. The width of the designed doping mask is not guaranteed to be transferred precisely onto the SOI layer due to the under cut and over etching in the actual fabrication process. The actual doping mask width W_m is measured as 1284.3 nm, which is 215.7 nm shorter than the designed length of 1500 nm.

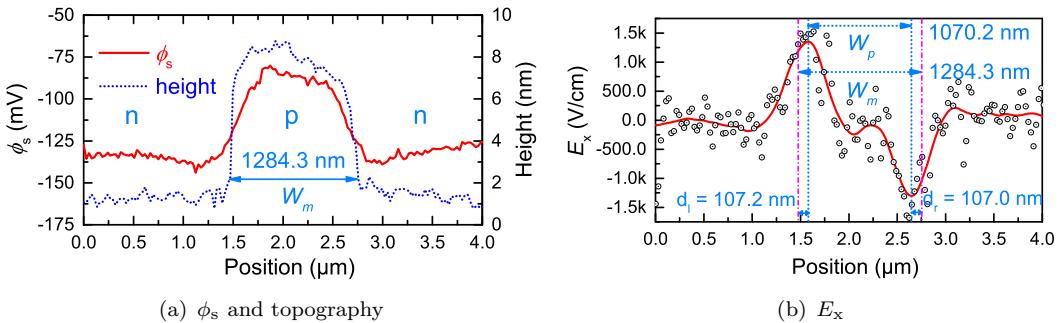


Figure 5.17: (a) The measured surface potential curve and (b) lateral electric field fitting. The dot is the original KPFM data point and the red line is the curve after Loess smoothing.

The space charge region in p-n junction is indicated by distribution of E_x . The extracted E_x curve is shown in Figure 5.17(b). There are two symmetric peaks; In the positive side where E_x is parallel to the x-axis direction and negative side where E_x is antiparallel to the x-axis direction in the E_x profile. The black dots represent the E_x value which was derived from the original non-smoothed potential profile and the smoothed result which is presented by the solid red line. It is clear that the value of E_x line in n-type region is almost equal to zero. The E_x curve starts to rise at $x = 1.0 \mu\text{m}$ and shows the maximum at $x = 1.6 \mu\text{m}$. E_x decreases and turns to the negative between $x = 2.2\text{--}3.2 \mu\text{m}$, and shows the minimum at $x = 2.7 \mu\text{m}$. The distance between the maximum and minimum points is 1070.2 nm which is 214 nm shorter than the length of the doping mask measured by AFM. The position of the maximum or minimum of the electric field is called as the position of metallurgical p-n junction. Therefore, KPFM is the tool that enable us to determine the position of metallurgical p-n junction experimentally. The results suggest that the distance between the edge of the hard mask and the metallurgical junction is about 107 nm. The distance of 107 nm would be due to the lateral diffusion of P dopants.

To observe the lateral charge redistribution in practical devices under the influence of static gate biasing, the V_g dependent E_x is also extracted in Figure 5.18(a) from ϕ_s curve in Figure 5.18(b). Each E_x curve in Figure 5.18(a) shows the peak shape at the same x position in changing the gate voltage, while the height of the peak in E_x is changed as a function of V_g . The maximum E_x value at the peak is peak value keeps is 1.34 kV/cm when $V_g = 0 \text{ V}$ and it moves upwards to 1.4 kV/cm when V_g is reduced to -1.8 V . However it drops down to 1.2 kV/cm when V_g is further reduced to -3 V . It is notable that the reduction of E_x at negative V_g does not cause the increase in I_d . Once the larger negative V_g is applied the both E_{\max} and ϕ_{sp} is reversed. On the other hand, E_{\max} is reduced and large current is allowed under positive V_g . For $V_g = 4 \text{ V}$ E_{\max} is reduced to 372 V/cm which is about 73.4% of E_{\max} at $V_g = 0 \text{ V}$. The line width of the E_{\max} peak with respect to the position x , which is related to the width of space charge region, also changes according to the change of V_g . It is clear that the line width of the E_{\max} peak is largely decreased under the large positive gate voltage of 4 V. As a result, the length where the E_x is kept almost zero in the p-type region increases from the null at $V_g = 0 \text{ V}$ to about 738 nm in the E_x curve for $V_g = 4 \text{ V}$. With refer to the experimental $I - V$ curve in Figure 5.9, larger current is allowed for the shorter depletion width in the p-n junction.

5.3.4.2 Simulated electric field profile

The E_x is also extracted from the simulation results where two abrupt p-n junctions are assumed for the n-p-n structure modelled in the calculation, and shown in Figure 5.19(a). Similar to the fitting results of the KPFM potential profile, there are two E_{\max} peaks corresponding to the left-hand-side and right-hand-side metallurgical p-n junctions. E_{\max}

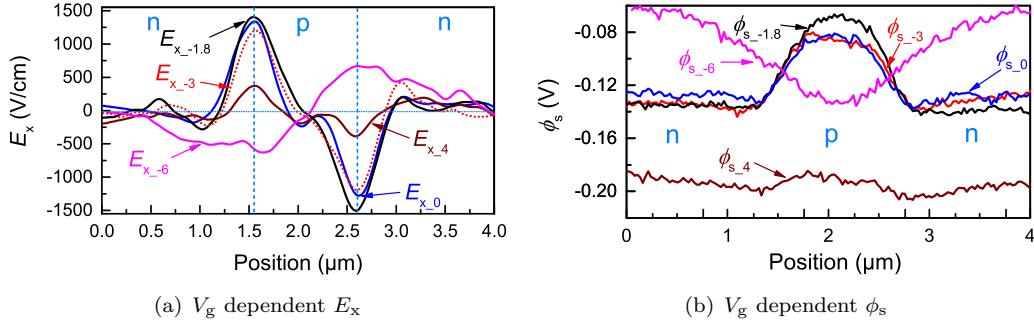


Figure 5.18: Fitted V_g dependent lateral electric field change in n-p-n structure. The value in the suffix of the notation represent the value of gate voltage e.g. E_{x-4} is the electric field curve in x-axis at $V_g = 4$ V.

is adjustable by changing V_g . Here E_{\max} are 67.9, 58.4, and 50.5 kV/cm at $V_g = -0.5$, 0, and 5 V, respectively. In addition, the line shape of the peak is asymmetric due to the assumption of the abrupt junction. The length of the tail of the E_x peak into p-type region is consistent with the transition length where the hole density is changed from the lowest to the maximum value as shown in Figure 5.19(b). The transition length of the hole concentration is 750 nm at $V_g = 0$ V. When V_g is reduced to -5 V the length is down to 390 nm. After the hole concentration is significantly reduced under the large positive V_g , the length becomes 75 nm. This result suggests that in the abrupt junction model, the transition length is much shorter than the experimental observation so the other model should be considered to explain the actual fabricated structure.

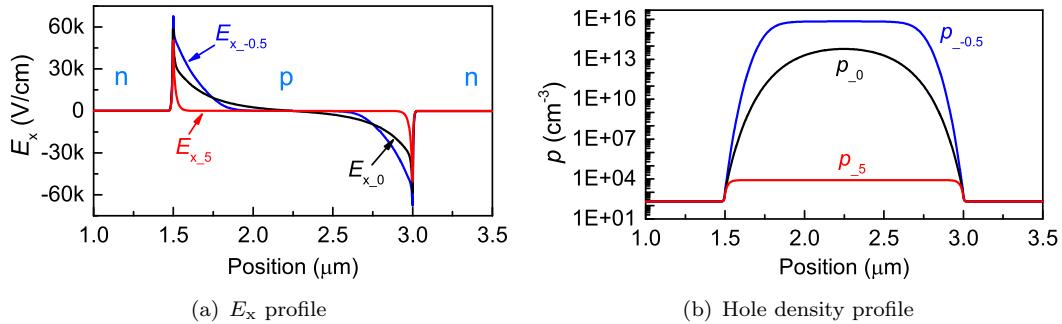


Figure 5.19: V_g dependent surface hole density and potential profile along n-p-n channel. The value in the suffix of the notation represent the value of gate voltage e.g. E_{x-5} is the electric field curve in x-axis at $V_g = 5$ V.

5.3.5 Potential profile under current flow

5.3.5.1 Experimental potential and electric field profile

To investigate the charge transport characteristics in the n-p-n structure the potential profile under fixed $V_d = -2$ V and various V_g (-5, 0, and 5 V) is scanned along n-p-n

structure and shown in Figure 5.20(a). The profile ϕ_{s-5} (current off state) shows that ϕ_{sn} is slightly tilted and large amount of potential drop of 290 mV is observed in the p-type region. The ϕ_s curve is bent in the right-hand-side of the p-type region. It is notable that $\Delta\phi_{pn}$ was flipped to -30 mV in Figure 5.14 but it turns back to the 35 mV hump feature again when $V_d = -2$ V. In addition, at the $V_g = 0$ V ϕ_s the degree of bending for ϕ_s and the magnitude of the potential drop are significantly reduced compare to the case at $V_g = -5$ V, whereas the the current is increased to 200 nA and and the height of potential hump is reduced from 50 mV without V_d to 21 mV at $V_d = -2$ V. When the large positive V_g is applied to turn on the device, the current is dramatically increased to 56 μ A and the surface potential ϕ_{s-5} shows almost monotonic decrease with two bending of the slope. The slope of the straight line in the n-type region in both sides is almost equal but smaller than the slope in the p-type region. the total potential drop in p-type region is further reduced to 100 mV. Particularly the hump structure almost disappeared in the profile.

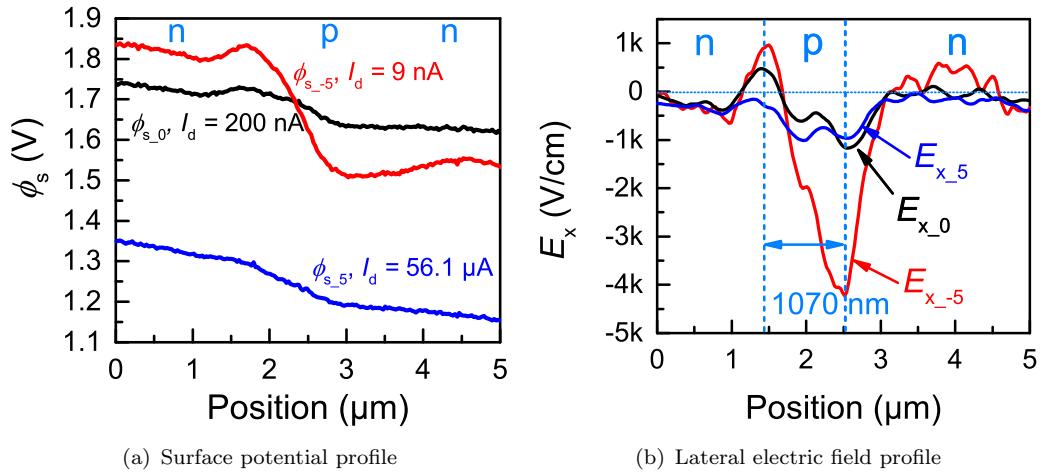


Figure 5.20: Surface potential value against the applied various V_g at $V_d = 2$ V $V_s = 0$ V. The value in the suffix of the notation represent the value of gate voltage e.g. ϕ_{s-5} is the surface potential curve for $V_g = 5$ V.

The E_x profile in Figure 5.20(b) is extracted from the potential curves. Figure 5.20(b) suggests even under the -2 V drain bias, the E_{max} are kept at the same position as it is observed in Figure 5.17(b) at $V_d = 0$ V. On the other hand, the symmetry of the lineshape of the E_x peaks between the left and right-hand-side p-n junctions is broken under the influence of V_d . As a result, the $|E_{max}|$ at the left-hand-side p-n junction is 968 V/cm while the one at right-hand-side is 4200 V/cm. This is the change observed for high channel resistivity condition ($V_g < V_{th}$). Under the large positive gate voltage of 5 V, the E_x peaks disappears and behaves similar to the uniformly doped SiNW devices which were described in previous chapter. Here the absolute value of $|E_x|$ of p-type region is 866 V/cm which is larger than that in n-type regions of 231 V/cm, suggesting that even at hight V_g the resistivity of the inversion layer formed in the p-region is larger than that in n-type region. In addition, the curve E_{x-5} in the Figure 5.20(b), the

left-hand-side E_{\max} peak becomes smaller while the right-hand-side E_{\max} peak becomes larger. The line width of the E_{\max} peak at the left-hand-side is reduced from 535 to 268 nm while the right-hand-side peak is expanded from 535 nm to 802 nm. The change in the peak width suggests the space charge distribution is changed. Overall, the profile at $V_g = 5$ V corresponds to the resistive nature of the channel while the one at $V_g = -5$ V shows capacitive nature dominated by space charges. The profile at $V_g = 0$ V is a kind of crossover between the two distinctive states.

5.3.5.2 Simulated potential and electric field profile

The simulated ϕ_s profiles of a single n-p-n channel at $V_d = -1$ V and various V_g are shown in Figure 5.21(a). Time constraint only allowed me to simulate the model at $V_d = -1$ V but I believe that qualitative comparison would be useful to analyse the experimental results. The simulated surface potential profiles for various V_g (-0.5, 0, and 5 V) are illustrated in Figure 5.21(a). All the potential curves in the p-type region are lifted up near both drain and source side. In addition, the ϕ_s curve in p-type region is bent when $V_g < V_{th}$ and the degree of bending depends on the magnitude of V_g . The curve, $\phi_{s,-0.5}$, in Figure 5.21(a) shows that the potential drop of 1.2 V takes place at the right-hand-side p-n junction and the potential curve at the centre of the p-type region is still flat. After V_g is increased to 0 V, the potential drop in the p-type region of the n-p-n structure is changed. The potential drop in the right-hand-side p-n junction is reduced to 0.8 V and the rest of the drop of 0.26 V is observed as the tilted potential line along the p-type region. When V_g is increased to 5 V, the ϕ_s curve in p-type region turns to be a linear line with well-defined constant slope. It is notable that, in simulation the space-charge-induced potential steps in left-hand-side p-n junction is able to be reduced by increasing V_g but is cannot be eliminated even large current flows through the channel. The value of the potential hump in the left-hand-side p-n junction is reduced by V_d from 806, 683, and 95 mV at $V_d = 0$ V to 209, 92, and 71 mV at $V_d = -1$ for $V_d = -0.5$, 0, and 5 V, respectively.

The E_x profiles are extracted and shown in Figure 5.21(b). Similar to the experimental E_x profiles, under the influence of V_d the left-hand-side E_{\max} peak in the p-n junction is shrunk while the right-hand-side peak is expanded. The degree of expansion depends on the value of V_g . The asymmetry of the E_{\max} peaks is clear for $V_g < V_{th}$ and the symmetry is retrieved by large positive V_g of 5 V. Furthermore, the current level is different under various electric field distribution along the channel. In the profile of $E_{x,-0.5}$, the electric field in the left-hand-side of the p-type region ($x < 2.2$ μm) is close to 0 V/cm while E_x decreased to negative value in the rest of p-type region. At $V_g = 0$ V the leakage current is increased meanwhile the magnitude of the peak at the left-hand-side junction is reduced slightly and the negative E_x in the left-hand-side p-type region is shifted down slightly. After V_g is increased to 5 V the flat E_x line indicates that the antiparallel E_x is uniformly distributed in the p-type region, resulting in the large current.

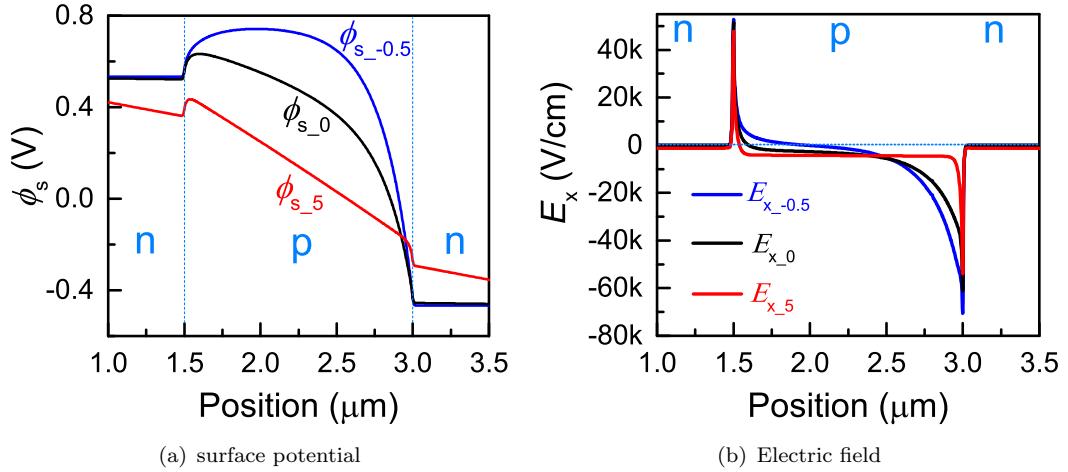


Figure 5.21: Surface potential and electric field on n-p-n channel for $V_d = -1$ V and changing V_g (-0.5, 0, and 5 V). The electric field is derived along drain to source direction. The value in the suffix of the notation represent the value of gate voltage e.g. ϕ_{s_5} is the surface potential curve for $V_g = 5$ V.

5.4 Discussion

The charge transport property ($I - V$ characteristics) of FET devices is revealed by local free charge carrier charge density (Equation 3.8, Equation 3.9) and local electric field distribution (Equation 5.2) which is related to the potential profile inside the device channel. In this section the change in electrical characteristics of the FETs is discussed in relation to the local electrical potential and electric field information. The discussion will firstly start with electric characteristics of the devices and then change of the free carrier density in p-type channel under static V_g is discussed then change of the p-n junction under different biasing condition is addressed, and finally switching of the charge transport properties from capacitive to resistive nature is mentioned in terms of surface potential profile changes.

5.4.1 $I - V$ characteristics of n-p-n structure

The simulated $I_d - V_g$ curve in Figure 5.10(a) suggests the threshold voltage is 0.9 V at $V_d = 1.8$ V, whereas V_{th} (Figure 5.9(a)) in the practical multiple junction n-p-n device is 0.7 V. The theoretical V_{th} calculation by using Equation 3.23 for bulk MOSFET devices suggests V_{th} for an ideal device is 0.88 V. The theoretical calculation result is consistent with V_{th} from the simulated $I - V$ curve. The V_{th} of the practical devices is 0.2 V smaller than that in the simulation. The 0.2 V threshold voltage reduction in the practical device can be explained by the following three factors. The first factor can be the over estimation of the intrinsic doping concentration. $N_a = 2 \times 10^{14} \text{ cm}^{-3}$ is used in the simulation but it could be down to $8.5 \times 10^{13} \text{ cm}^{-3}$ if $V_{th} = 0.7$ V should be realised. The second factor can be the positive 0.2 V offset voltage from the SOI substrate. The

original doping concentration is the same for the SOI and substrate but the small amount of P dopant could diffuse into the substrate during the diffusion process. The diffusion causes the shift of work function of the substrate. Assuming that 0.2 V is all contributed by the additional diffusion into the substrate P dopant concentration of $2 \times 10^{14} \text{ cm}^{-3}$ is expected for the substrate. The last factor could be the offset from trapped charges on the channel surface while the surface of the fabricated devices is exposed for KPFM characterisation.

The physical model for threshold voltage estimation is well developed and it is able to be accurately estimated. On the other hand, the other changes such as current saturation, suppression of leakage current, increase in hole current, and delay of saturation in experimental $I_d - V_d$ have not been discussed in details in literature. The changes in the $I - V$ characteristics are related to the local charge carrier redistribution and also the change of the local electric field caused by externally applied voltage. Based on the surface potential information which is measured by KPFM, the change in electrical characteristics will be discussed in the following sections.

5.4.2 Charge carrier density change in p-type region

The potential profile simulation along the depth direction suggests that in the p-type region of the n-p-n structure the potential is uniformly modulated by V_g while the surface potential is fixed at a certain value at the grounded n-type regions. The uniformity of potential distribution in p-type region is due to relatively low doping concentration, and the thin SOI layer (50-nm-thick). Taking those factors into consideration, the potential change inside of p-type region is able to be probed by the surface potential ϕ_s which is measured by KPFM from the opposite side of the SOI.

The simulation result in Figure 5.19 suggest the free charge carrier density is directly related to the potential profile in the device. The relationship between the hole density and potential profile is expressed by Equation 3.9. The value of ϕ_s we calculated in simulation is equal to $(E_i - E_f)/q$, therefore the hole concentration in Figure 5.19 is calculated by

$$p = n_i e^{\frac{q\phi_s}{k_b T}}, \quad (5.4)$$

and this equation indicates that the change in ϕ_s also results in the change of the free charge carrier density.

Both simulation and measurement results indicate the surface potential difference $\Delta\phi_{pn}$ in the p-n junctions is changed as a function of V_g in Figure 5.14 (measurement) and Figure 5.15(a) (simulation). The change in $\Delta\phi_{pn}$ is also related to the shift of Fermi energy level in p-type region therefore the free charge carriers inside of p-type region is

modulated by the back gate. When V_g is not applied, the $\Delta\phi_{pn}$ (0.68 V in simulation) is already formed in the p-n junction due to the difference of the doping concentration. The $\Delta\phi_{pn}$ at $V_g = 0$ V is slightly smaller than the value of theoretical calculation (0.76 V) according to the doping concentration in Equation 3.14. The reduction of $\Delta\phi_{pn}$ can be attributed to the relatively lower doping level in the p-type region which shows long depletion length without biasing. The depletion length could exceed the length of p-type region if the depletion from the both terminals of p-type region is considered. The longer depletion length is also indicated by both $E_{x,0}$ and $\phi_{s,0}$ profiles in Figure 5.19 where $E_{x,0} \neq 0$ and transition of ϕ_s are almost extended to the centre of p-type region. As a result electrons which is diffused from the adjacent n-type regions are presented in the centre of p-type region and reduce the density of holes by electron-hole recombination, resulting in the reduction of $\Delta\phi_{pn}$. According to the hole density curve $p_{,0}$ in Figure 5.19(b) the hole density of centre p-type region is still larger than the electron density, indicating the region is and not fully depleted yet. The excess electrons in the p-type region could relate to the relative large sub-threshold current.

Based on the discussion above, the potential profile is able to be used for the observation of charge carrier redistribution inside the FET channel under biasing. The simulated $\Delta\phi_{pn}$ (takes from central p-type region) in Figure 5.15(a) changes rapidly in the range of the sub-threshold region ($-0.2 < V_{th} < 0.88$ V) and turns to be gradual in both current suppression and large current regions. This phenomenon suggests the level of modulation of the potential and charge carrier density in the p-type region is weakened when V_g is out of the sub-threshold range.

Here a capacitance model is suggested to make a link between the device structure and observed surface potential profile via KPFM measurements as shown in Figure 5.23. The C_{dl} and C_{dr} are the depletion capacitances which are parallel with the p-n junction capacitance at both the left and right hand side of p-type region, and C_g is the gate capacitance. The gate dependent $\Delta\phi_{pn}$ is then expressed as

$$\Delta\phi_{pn} = -(-\psi_{bi} + V_g \frac{C_{ox}}{C_{ox} + 2C_d}) , \quad (5.5)$$

where the negative sign in front of the built-in voltage ψ_{bi} is due to the the fact that ψ_{bi} is measured from the p-type Si to n-type Si, and the negative sign in front of the bracket is due to the fact that the potential we discuss in our work is for electrons. Based on this model, the change in $\Delta\phi_{pn}$ profile is explained that the rapid potential change in the sub-threshold region is related to reduction of the depletion capacitance (the enhancement of the depletion width) due to electron-hole recombination of electron-hole by excess electrons which are attracted by the positive gate voltage. After the p-type region is strongly inverted at V_{th} , the depletion width becomes the maximum, *i.e.* the depletion capacitance becomes minimum [69] and then $\Delta\phi_{pn}$ becomes linear. Therefore, in the $\Delta\phi_{pn}$ curve, the threshold voltage is defined at the point where $\Delta\phi_{pn}$ starts to be

linear. In the simulated $\Delta\phi_{pn}$ curve the point where $\Delta\phi_{pn}$ starts to be linear is around 0.9 V which is consistent with the threshold voltage extracted from the $I - V$ simulation. The other linear region for $V_g < -0.2$ V is explained by the maximum total capacitance where the depletion capacitance in the p-type region is minimum due to excess holes. This is related to the leakage current suppression.

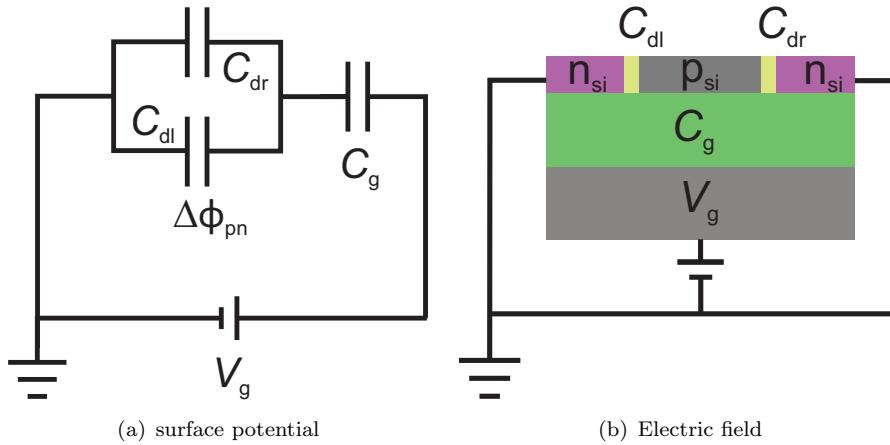


Figure 5.22: Surface potential and electric field on n-p-n channel for $V_d = -1$ V and changing V_g . The electric field is derived along drain to source direction.

The $\Delta\phi_{pn}$ profile in Figure 5.14 for practical devices measured by KPFM indicates that the $\Delta\phi_{pn}$ also decreases rapidly from current suppression point to the threshold point ($-2.2 < V_g < 0.7$ V), however, the $\Delta\phi_{pn}$ line is not linear even after $V_g > V_{th}$ and the $\Delta\phi_{pn}$ finally equal to 0 V at $V_g = 5.8$ V. Furthermore at the other gate voltages where the current is suppressed $\Delta\phi_{pn}$ does not increase any more with decreasing V_g and starts to drop down rapidly. In the $I_d - V_g$ curve the current saturated at $V_g = 5.8$ V thus the crossover could related to the free electron saturation in the p-type region and the number of carriers cannot be increased largely for the further increase of V_g . The other cross over point at $V_g = -4.8$ V is close to the point where the hole conduction stars. This crossover could be related to the spread of the hole carriers into the n-type regions and finally is able to be converted to the hole current when V_g is further reduced.

The link between the experimental $\Delta\phi_{pn}$ and $I - V$ characteristics has been clarified, while the quantitative estimation of the doping concentration and charge carrier density is hard to be made. In this experimental setting by comparing the measured $\Delta\phi_{pn}$ with the theoretical calculation, the scaling factor is estimated to be more than 10. The other capacitance model for KPFM measurement is made as shown in Figure 5.23. Where C_{contact} is the contact capacitance formed at the electrode-SOI contact interface ($C_{\text{contact}} = 0$ in simulation), C_d is the depletion capacitance formed at the p-n junction, C_{tip} is the equivalent tip-sample capacitance, and V_{fb} is the voltage applied to tip KPFM tip for sensing the DC bias between the tip and the scanned point on the sample surface. For the measurement of the surface of p-region, three different capacitances are serially connected. C_{tip} is about 1.1 aF, C_d is roughly 265 aF and C_{contact} is 811 nF.

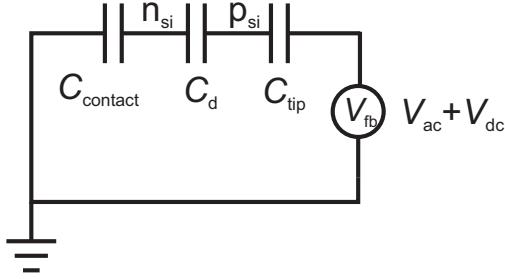


Figure 5.23: KPFM measurement capacitance model.

The shift of ϕ_{sn} in experiment could be possibly related to the capacitance between the Al wire and heavily doped SOI, where the Schottky junction could be formed. As a result, the $C_g + C_{\text{contact}}$ capacitance model are used to estimate the potential drop in n-type regions. The estimated value of contact capacitor is $C_{\text{contact}} = 94C_g$ according to the average linear slope ($\frac{\phi_{sn}}{V_g} = -0.011$ in Figure 5.14) of ϕ_{sn} by using the following equation

$$\begin{aligned}\phi_{sn} &= -V_g \frac{C_g}{C_g + C_{\text{contact}}} \\ C_{\text{contact}} &= -\left(\frac{V_g}{\phi_{sn}} + 1\right)C_g .\end{aligned}\quad (5.6)$$

In addition, the reduction of $\Delta\phi_{pn}$ in the measurement brings us the difficulty of quantitative estimation of actual charge carrier density in the channel of the device. The offset of ϕ_{sn} is not the reason of $\Delta\phi_{pn}$ scaling as the degree of offset is small. The reduction of $\Delta\phi_{pn}$ can be related to the feedback signal $V_{fb} = V_{dc} + V_{ac}$. According to the KPFM measurement principle which is illustrated by Equation 3.48, the V_{fb} applied on between tip and ground. When the tip scanning on p-type region the constant V_{ac} signal is coupled to the p-type region whereas the measurement adjusts V_{dc} to cancel out V_{dc} induced capacitance coupling force, *e.g.*, $\phi_{sp} = 682$ mV when $V_g = 0$ V. The KPFM feedback system apply 682 mV on the tip to keep an equal potential between the tip and sample surface. According to the potential distribution in the serial capacitances, the coupled DC signal could induce about 0.4% charge change in the p-n junction and also possibly cause $\Delta\phi_{pn}$ fluctuation of 0.4%. Therefore the potential of p-n junction is not changed by the KPFM scan, however the coupled AC signal could affect the local state of capacitively connected p-type region. According to Equation 3.48, force signal component of the $\frac{\partial C}{\partial z} V_{ac}^2 [1 - \cos(2\omega t)]$ always exists between tip and sample surface. Therefore the V_{ac} signal is able to induce charge resonant in the p-n junction under 140 kHz. The reduction of $\Delta\phi_{pn}$ could be related to the smear of DC potential in the p-n junction due to a small amount of AC current. In addition, the ϕ_s measurement is sensitive to the sample surface state. Furthermore the scaling factor may be also related to the minority charge carrier injection into the sample surface during KPFM scan [67].

5.4.3 Direct observation of metallurgical junction under biasing

The position of metallurgical p-n junction is useful information for the estimation of effective channel length for nano devices, the size of tunnelling barrier for doping modulated SET devices, and also for a photo-diode. Due to the dopant diffusion, the actual position of metallurgical junction can be shifted. In this study, a procedure to determine the position of the metallurgical junctions is introduced via the surface potential and electric field distribution obtained by KPFM. Not only the position of metallurgical junction but also the width and the magnitude of electric field in the junctions is also able to be directly observed by E_x curve.

The simulated E_x curve for abrupt junction in Figure 5.19(a) suggest E_x appears at the position of p-n contact interface and it is not able to be moved even under changing V_g . The formation of E_x is related to the redistribution of the charges (Figure 5.24(a)) at the interface of the p-n junctions and the magnitude of E_x can be estimated by Poisson's equation Eq.3.15. The charge redistribution is caused by diffusion effect where charge carriers tend to diffuse from a higher density area to lower and the electrons-hole are combined in the space charge region, as result of diffusion the neutrality is broken and electric field is formed crossover the junction region and the strength reached maximum at the metallurgical boundary. As a result of superposition of E_x . After the formation of E_x the diffused majority charge carriers are driven back by E_x . Both diffusion and drift process happens simultaneously and the dynamic balance will be finally achieved and the diffusion length is able to be estimated by Equation 3.17. It is notable that, E_{\max} is only presented at the boundary of metallurgical p-n junction.

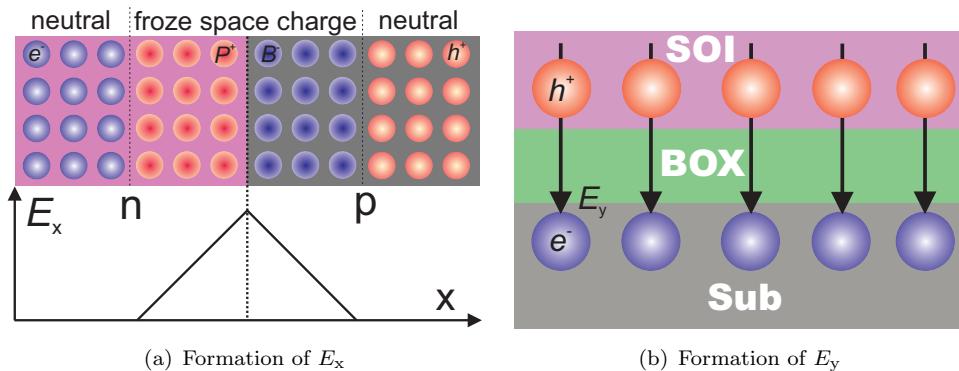


Figure 5.24: The formation of E_x and E_y in back gated SOI devices (a) E_x . e^- is free electron , h^+ is free hole, P^+ is core of phosphorus atom which lost one electron in Si lattice, B^- is the boron atom which accept one extra electron in Si lattice. (b) E_y .

The simulated E_x curves in Figure 5.19(a) under different static V_g suggests the position of E_x is fixed but the width of junction and the strength of E_{\max} can be changed by externally applied bias and also the charge density in the semiconductor materials. Under the applied V_g , the charge carrier density in the channel is changed and how to

change of the charge carrier density also changes the dynamic recombination process in the space charge regions. The amount of diffused and recombined electrons in p-side of p-n junction are reduced by positive V_g increased electron concentration, and vis versa. Therefore, the reduction of $|E_{\max}|$ value and the shrink in width of the space charge region can be explained by reduction of recombination process as the excess electrons are moved in the p-type region by the large positive $V_g = 5$ V and it is opposite under the large negative V_g . It is notable that, the applied V_g does not contribute to the changing value of E_x because V_g only induces the electric field is perpendicular to the channel as shown in Figure 5.24(b). Therefore, the magnitude of E_x is only affected by the diffusion process or applied V_d .

By using E_x profiling, the formation of metallurgical junction is directionally observed in Figure 5.18(a). Together with the AFM results, the lateral dopant diffusion (107 nm) was estimated for the thermal diffusion process (furnace) at peak temperature 850 °C for 2 min. Meanwhile, the thermal diffusion simulation results suggest that the lateral diffusion length is 90 nm which is almost consistent with the experimental observation. The difference of 17 nm would be related to the error for the shape of the doping mask such as the thinned edge of the mask, or the error caused by the relatively large tip radius. In addition, the relatively wider line width if the E_{\max} peak in the n-type regions indicates the doping concentration of the donors in the junction region is diluted possibly due to the lateral diffusion. The E_{\max} height change under the static gate voltage for the diffused p-n junction is much higher than that in the ideal abrupt p-n junction used in the simulation. In the experimental measurements, E_{\max} is reduced about 73.4% at $V_g = 5$ V compared to that in the E_x curve at $V_g = 0$ V.

The space charge redistribution under the influence of applied V_d can be observed via the change of the E_x curves. The simulated curves in Figure 5.22(b) suggests the space charge inside of left-hand-side p-n junction is reduced while the charges is accumulated to the right-hand-side p-n junction under the influence of externally applied E_x with anti-parallel x-axis direction by -1 V V_d . The degree of change in junction is also related to the value of V_g . The simulation result suggests large change in junction happens under the negative V_g which the hole density in p-type region is accumulated and the external E_x is almost shield in the p-type region by space charge ($E_x = 0$ V/cm). On the other hand then influence of V_d is minimised under large positive V_g which the p-type region is full of free electrons. Particularly the change in p-n junction in the practical devices is similar to the change in simulation. It is notable that, in experimental the p-n junction is almost eliminated under 5 V V_g .

5.4.4 Direct observing the transition of in n-p-n structure

The free charge carrier transfer in the semiconductor devices takes place under the presence of the electric field or diffusion as expressed in Equation 3.19. Therefore the

change of the $I-V$ characteristics of devices should be linked with the direct observation of the electric field and charge carrier distribution in the channel. According to the previous discussion the n-p-n structure acts as the capacitors which store space charges and are tuned by the change of the the potential barrier of the two p-n junctions. On the other hand, the current flows in the channel which is also related to the magnitude of electric field in p-n junctions. Based on this understanding, a parallel resistor and capacitor model is built and shown in Figure 5.25 for understanding of the transition behaviour of n-p-n structure between resistive and capacitive natures.

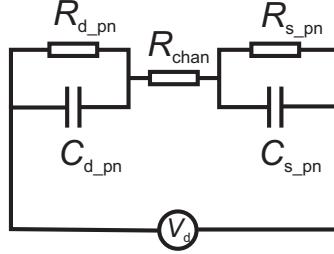


Figure 5.25: Circuit model of n-p-n channel.

The capacitance C_{d_pn} and C_{s_pn} represent the capacitance of the p-n junctions at the drain side and source side, respectively. The capacitance is simply expressed by the depletion width, *i.e.* $C_{d_pn} = \epsilon_{si}/W_d$. The R_{d_pn} and R_{s_pn} is the resistance of the junction which can be derived by Ohm's law $R = V/I$, and the R_{chan} is the resistance of the effective p-channel. The simulation result suggests that C_{s_pn} and C_{d_pn} dominate the device behaviour when $V_g < V_{th}$ as the value of C_{pn} is small, *i.e.* wider depletion width and large junction resistance R_{pn} , *i.e.* larger potential drop but small current. At $V_g > V_{th}$ the junction capacitance is significantly increased (a narrower depletion width) and the junction resistance is largely reduced to allow large current, therefore the $I-V$ characteristics is dominated by junction resistors.

The free charge carriers transport property through the ideal n-p-n structure can be estimated by observing the change of E_x in Figure 5.21(b). At the negative V_d , the majority charge carriers, free electrons, tend to transfer through the Drain electrode to the grounded Source electrode, however there the electric field in the C_{d_pn} is parallel to the x-axis direction and tend to prevent the electron transfer. However, the conduction current is still observed and electrons are still able to transfer through the energy barrier which is built at p-n junction. In the previous discussion, the diffusion current which is driven by thermal energy assists the electrons transfer through the Drain side junction. Once the electrons cross the junction, they are able to be driven by the anti-parallel x-axis electric field to generate the drift current. The change in the current level is related to the quantity of electrons which are transferred through the Drain-side junction and the total potential drop in the p-type region. It is notable that, the height of the energy barrier in the the Drain-side p-n junction can be tunable by V_g so that the height and width of Drain-side p-n junction can be reduced by increasing V_g , making the diffusion

process easier and the current assisted by electric field (anti-parallel x-axis direction) is enhanced. For the $E_{x,-0.5}$ in Figure 5.21(b), the width where the distance of $E_x \approx 0$ becomes longer. This suggests that the n-p-n structure behaves as two serially connected capacitances where the V_d induced E_x is shielded by the two capacitors meanwhile the charges are redistributed in those two capacitors under the influence of V_d and result change in E_{max} . This change is consistent with injecting minority charge carriers which resulting in depletion in the injected area. The depletion is almost extended to the whole p-channel, therefore, the resistance of the channel becomes large. On the other hand, the $E_{x,5}$ profile suggests that the width of the barrier is significantly reduced and the current assistant electric field is uniformly distributed in the p-type region. Due to the short depletion length, R_{pn} is smaller than that in the sub-threshold region, and R_{chan} is low due to the inversion, therefore at $V_g = 5$ V the resistive behaviour is dominant.

Based on the discussion above, the changes of the junction capacitance and resistance are extracted from the experimentally observed profiles. By using the depletion width which is extracted from the $E_{x,-5}$ profile in Figure 5.20 (716 nm in the left p-n junction and 1250 nm in the right p-n junction). The depletion capacitances are estimated as $C_{d,pn} = 1.4 \times 10^{-8}$ F/cm⁻² and $C_{s,pn} = 8.2 \times 10^{-9}$ F/cm⁻², respectively. In addition, according to the total potential drop in the right hand side p-n junction (326 mV) and current level (9 nA) the $R_{s,pn} = 3.6 \times 10^7$ Ω. The potential drop in the drain-side p-n junction is approximately the value of the potential hump of 21mV, therefore, the resistance $R_{d,pn} = -2.3 \times 10^6$ Ω.

At $V_g = 0$ V, the sub-threshold current is increased to 200 nA while the height of E_{max} is significantly reduced. The drain side junction depletion width is reduced to 669 nm and the source side junction depletion width is enhanced to 1297 nm. Based on the change in the depletion width, the capacitance of junctions are adjusted to $C_{d,pn} = 1.6 \times 10^{-8}$ F/cm⁻² and $C_{s,pn} = 8 \times 10^{-9}$ F/cm⁻² at $V_g = 0$ V. In addition the potential drop at drain-side junction is 17 mV while at the source-side junction is 95 mV. For $I_d = 200$ nA the junction resistance is reduced to $R_{d,pn} = -87$ kΩ and $R_{s,pn} = 470$ kΩ.

The measurement result shows that the n-p-n channel is switched to the resistive behaviour when $V_g \gg V_{th}$. The $\phi_{s,5}$ profile in Figure 5.20 shows straight linear line in p-channel and $E_{x,5}$ tends to be levelled straight line in p-type region. By using the resistivity fitting method which we used for resistive devices in the previous chapter, the resistivity of the n and p-type region are estimated as 0.041 and 0.154 Ω·cm, respectively. Here the n-type regions resistivity is close 0.023 Ω·cm in Table 5.1.

5.5 Conclusion

This chapter demonstrated a new devices characterisation method surface potential mapping. By using this method, the charge transport mechanism in n-p-n structure

is revealed. The similarity between practical measurement and simulation suggest well reliability of KPFM characterisation. The study result can be used for the improvement of single electron devices design. On the other hand the reason for large inconsistency for potential difference between n and p channel is given. The p-n junction capacitance in floating p-type region could interact with KPFM feedback AC signal and change the measurement result. For the future improvement, the direct p-type region electrical contact is suggested to improve the KPFM feedback. In addition the vacuum measurement is preferred to remove the influence of moisture or other polarised surface adhesions.

Chapter 6

Doping modulated side gate single electron transistor

6.1 Introduction

The previous study suggest the KPFM equipment is capable to investigate the potential change inside thin SOI devices for the purpose of deep understanding of device electrical characteristics. Nowadays, the scaling is the trend of evolution for semiconductor devices. Moreover, the quantum information devices becomes hot topic for the future solution of powerful computation. However the quantum information devices are still in development. Attempts which have been made to detect the local potential potential distribution for the characterisation of quantum devices, *e.g.* individual dopant observation [48], single electron transfer through two donors [47], and electron transport through dopant induced quantum dots in SiNW channel [105], *etc.* The single electron transport property through dopant atoms has been well investigated by those studies. The possibility of characterising advanced quantum devices has been well demonstrated by those studies. On the other hand, practical fabrication of the single dopant devices is channelling. Inspired by those works the effort of KPFM characterisation of single electron transistors have been made.

To achieve our purpose, the KPFM-tip-accessible surface-exposed doping modulated side gate thin SiNW SET devices were fabricated. The side gate and exposed channel design is for the convenience of surface potential scan. Based on this device the typical coulomb oscillations are observed. The agreement has been made between the coulomb oscillation period and physical dimension in the short island devices. However, the long island device shows unusual oscillation period. At room temperature the surface potential is scanned under different biasing conditions to reveal the gate electrode modulation inside the SiNW SET channel.

6.2 Experiment methods

6.2.1 Devices design

For the purpose of characterisation of SET by using potential information, the advanced side gate SiNW single electron transistors in Figure 6.1 are designed for KPFM scan. In the design, the SET devices are based on the 400 nm wide and 2 μ m long doping modulated SiNW channel (Figure 6.1(b), Figure 6.1(d)). There are two intrinsic sections in the SiNW channel. They are used to create energy barriers to confine electrons in the a SET island. The width of the island and barriers are different in each device design. In the mask design the length of island is either 200 or 400 nm long. Meanwhile, the barriers have the length of either 250 or 400 nm long. The SET channel is connected by the wider leads to the contact pads for electrical measurement. In addition the side gate is designed close to the SET island for the energy modulation. The width of the gate is the same as the length of the island. The side gate is separated by air with the fixed distance of 200 nm. In double side gate devices (DSG) two gate are symmetrically located next to the island.

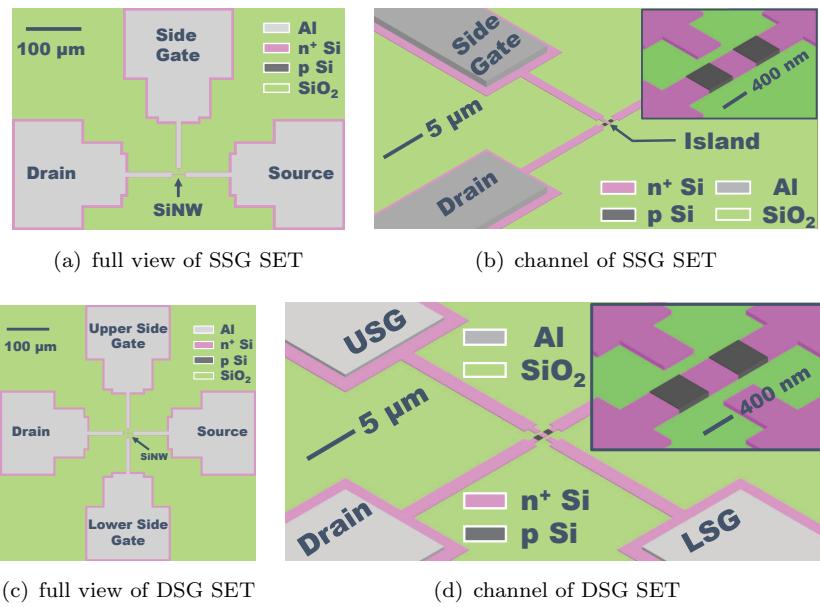


Figure 6.1: Design of single and double side gate single electron transistors.

6.2.2 Fabrication

The simplified fabrication processes used for fabricating doping modulated SET devices is shown in Figure 6.2. The sample was started from a 3 cm \times 4 cm SOI substrate which is shown in Figure 6.2(a). After surface cleaning the fist layer E-beam lithography was taken to pattern the doping mask for two tunnelling barrier to define the island of SET

(Figure 6.2(b)). With protection by the resist for the doping mask area the unwanted SiO_2 was then etched by combination of dry and wet etching in Figure 6.2(d). After etching the remained resist was removed by plasma ashing in Figure 6.2(e) for next fabrication step. The spin-on-dopants (SOD, Filmtronics P507) was then spun on the sample and the wafer was put in a furnace for diffusion at $850\text{ }^\circ\text{C}$ for 5 min (Figure 6.2(f)). The doping modulated SOI surface is formed after removing the residue of SOD and doping mask by HF solution (Figure 6.2). The second layer E-beam lithography was applied to pattern the devices structure (Figure 6.2(g)). Then the unwanted SOI was removed by dry RIE etching (Figure 6.2(h)). After etching and resist removal, the contact pads and SiNW channel are remained on top of the BOX layer (Figure 6.2(i)). Once the devices pattern is defined the last layer E-beam lithography was applied for the metal contact (Figure 6.2). 200-nm-thick Al film was deposited on the top of the resist by E-beam evaporator (Figure 6.2(k)). After the deposition, the chip was put in solvent to remove the resist and also the Al on top of the resist (Figure 6.2(l)). After the lift-off process the Al film only adhere on the patterned area. In the end the wafer is annealed at $450\text{ }^\circ\text{C}$ for 45 s in RTA with the N_2 gas to improve the quality of the Si-Al contact.

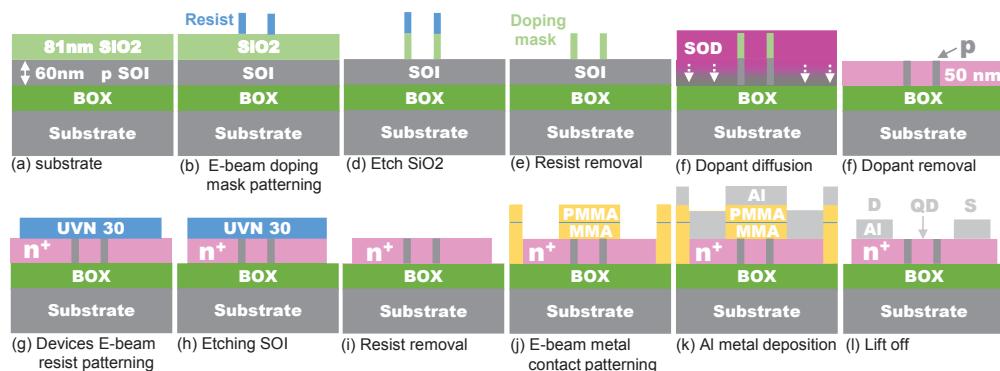


Figure 6.2: Fabrication process of multi-junction SET devices.

The optical images of fabricated single and double side gated SET are shown in Figure 6.3. In the full device image, the Al metal contact which is indicated in white colour covers well the most of contact area and leads. The out skirt pattern in light blue around the metal contact is exposed SOI. The width of the skirt is $10\text{ }\mu\text{m}$ which is designed to avoid accidental short circuit. The skirt is symmetric around the contact pad. It indicates that the alignment between each layer is well defined. Furthermore, the 400 nm wide SiNW SET channel can be clearly observed in the magnified channel image. The structure of tunnelling barrier and island in the $2\text{-}\mu\text{m}$ -long SiNW channel is able to be observed. The intrinsic SOI shows slightly darker colour and the doped n-type Si is brighter.

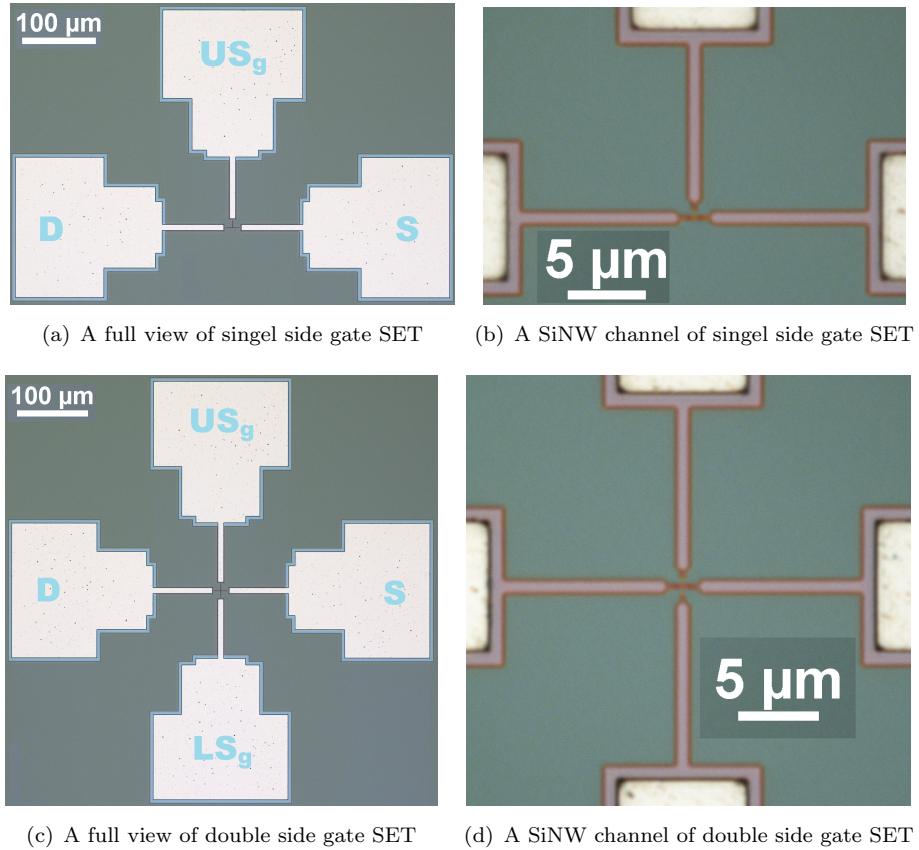


Figure 6.3: Optical image of fabricated single and double side gate single electron transistor.

6.2.3 Method of electrical and surface potential characterisation

The sample was put in the chamber of Cryogenic measurement system for low temperature $I - V$ measurement. The measured samples was wired bonded on a chip carrier which is electrically connected to the $I - V$ measurement system, Agilent B1500, and put in the Cryogenic chamber which offers vacuum and low temperature environment. The surface potential of the SET was also characterised by KPFM under different biasing conditions at room temperature. Similar to the samples which were discussed in the previous chapter, the SET sample was bonded on PCB board which is connected to Keithley 2401 and put in the KPFM measurement system for surface potential scanning.

6.3 Result

6.3.1 Room temperature electrical characteristics

Before low temperature and KPFM measurements $I_d - V_g$ characteristics (in Figure 6.4) of single side gate SET devices were firstly measured at room temperature by Agilent

B1500 with a Cascade probe station. The curves were taken from three devices with different dimensions of the island and barriers. The $I - V$ curve of the sample with the largest island size of $L_{qd} = 400$ nm and the p-type barrier $L_p = 400$ nm is shown in Figure 6.4(a). The $I - V$ curve suggests that the side gate which is coupled with the island is still able to modulate the current of the SET devices. At room temperature, the SET behaves as a normal FET device. The threshold voltage of measured devices is around 5 V. In addition, change of $I - V$ characteristics is observed in Figure 6.4(b) when the size of island is reduced to $L_{qd} = 200$ nm. When the size of island is reduced, the threshold voltage is slightly shifted to lower value of 4 V and the maximum current is increased to around 100 nA. The maximum current the sample within the 400-nm-long island SET is around 50 nA and the saturation of I_d is not shown in the scanned V_g range. On the other hand, the current saturation appears at $V_g \approx 7$ V in the sample with the 200-nm-long island SET. Furthermore, $I - V$ characteristics changes again when the size of the island kept at $L_{qd} = 200$ nm but the length of the p-type barrier is reduced to $L_p = 250$ nm. After the reduction of barrier size, the sub-threshold current is significantly increased in Figure 6.4(c). The short p-channel is no longer able to cut off the sub-threshold leakage current whereas the maximum current level is slightly reduced to 75 nA. The increase in leakage current can be related to the reduction of the effective length of the p-channel due to the lateral dopant diffusion.

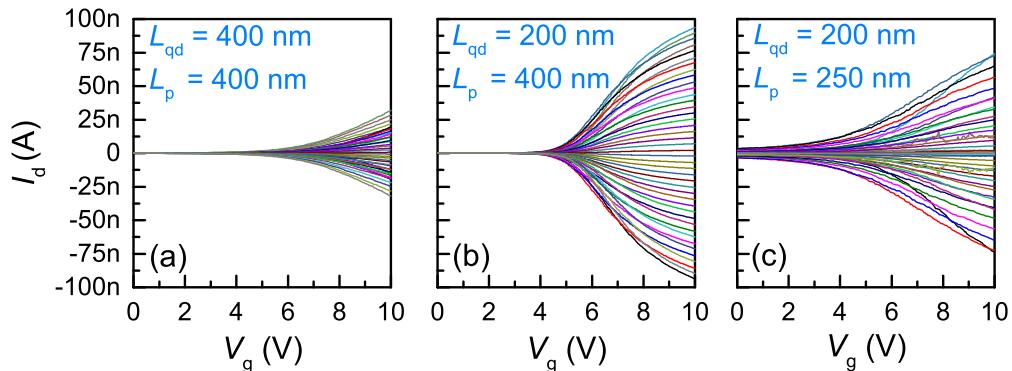


Figure 6.4: Room temperature $I - V$ characteristics of single side gate (SSG) SET devices. The curves were taken under different V_d which changed from -10 to 10 mV with step of 1 mV.

6.3.2 Low temperature coulomb diamond

The coulomb oscillation of side gate SET devices were observed at 5 K in Figure 6.5. At low temperature, the clear coulomb oscillation is shown for the two devices with the barrier length of $L_p = 400$ nm and the island lengths of $L_{qd} = 200$ and 400 nm in Figure 6.5(a) and Figure 6.5(b), respectively. In the figures, the low current level is indicated in dark region in the centre of figure and high current level is presented in bright region on the top and bottom of figure. In Figure 6.5(a) and Figure 6.5(b), we are able to observe the current is oscillating during V_g sweeping when $|V_d| < 7.5$ mV.

On the other hand the oscillation is hard to see in Figure 6.5(c) for the device with the barrier length of barrier 250 nm. There are two clear step structure in Figure 6.5(c) suggesting the threshold voltage becomes larger and doubled during the measurement of the devices with $L_p = 250$ nm, and $L_{qd} = 200$ nm devices. This suggests the short 250-nm-long p-type barrier is not able to confine electrons in the SET island properly. This result is also consistent with the large sub-threshold leakage current observed in the measurement at room temperature. In addition, the different oscillation period is shown in Figure 6.5(a) and Figure 6.5(b) for the SSG long island SET and DSG short island SET, respectively. The change in oscillation period suggests the oscillation period is related to the size of island and also width of the side gate. Here the oscillation period ΔV for the $L_{qd} = 400$ nm is 1 V and for the one with $L_{qd} = 200$ nm is 0.2 V. The change in oscillation is related to the total capacitance of the island. The details of the change in the oscillation period will be discussed in the following discussion section.

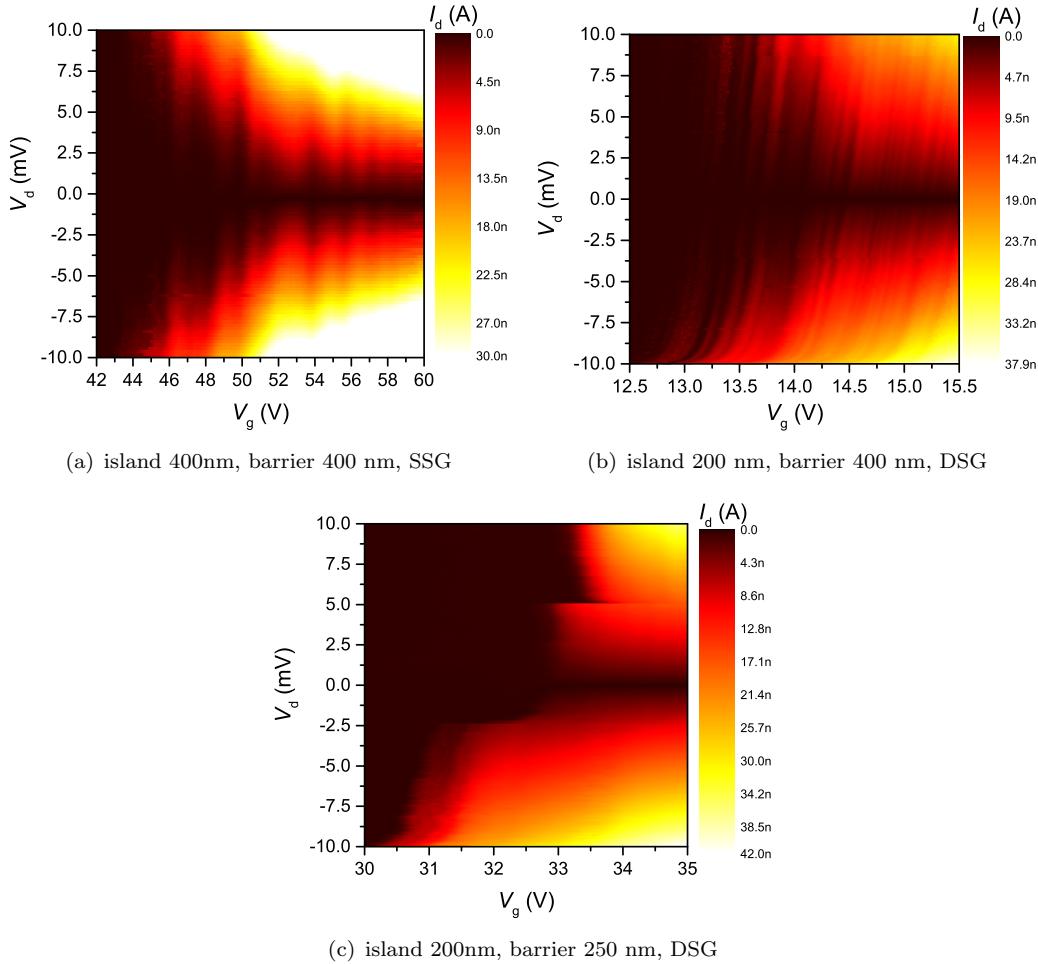


Figure 6.5: Column diamond diagram of side gate single electron transistors at 5 K.

6.3.3 Surface potential observation

6.3.3.1 Static single side gate modulation

Deep understanding of the operation of fabricated SET devices can be achieved by KPFM in-situ potential mapping. The surface potential in Figure 6.6 is for the devices with $L_p = 400$ nm, and $L_{qd} = 400$ nm under changing V_g and V_d . The surface potential map of the 2 μ m long SiNW SET devices at $V_d = V_g = 0$ is shown in Figure 6.6(a). The n-Si channel region is marked by using two parallel dotted lines. The doping profile change along the 300-nm-wide channel is clearly indicated by the change in surface potential level. Here, the n-Si shows potential level around -250 mV and the p-Si shows potential level near -110 mV. The area of 400-nm-wide doping mask is indicated by the vertical dotted line in the arrow-pointed p-region. The width reduction for actual p-Si is clearly shown in the right-hand-side p-region. Total 150 nm reduction can be related to the lateral dopant diffusion from both the n-channel side. A large number of the red dots on the surface of the left-hand-side SiNW channel suggest large amount of charge is adhered on the channel surface. Particularly the top edge of the SiNW shows uniform high potential (-110 mV). That suggest more negative charge is accumulated/trapped on the top edge of the SiNW even all electrode of the devices are grounded.

After the single side gate (bottom side in the image) voltage of $V_{usg} = -6$ V the surface potential on the SiNW channel was scanned by KPFM again. The channel potential modulation is clearly presented in Figure 6.6(b) for the top-bottom direction. In the figure the top part of the SiNW channel with the width of about 100 nm shows uniform high potential distribution (-100 mV) whereas the bottom part with the width of 200 nm shows green colour in the n-area and yellow in the p-area. This suggests that the potential energy for electrons on top of SiNW is higher than that on the bottom under the influence of negative gate voltage. In addition the SET barrier is more clearly observed , suggesting the tunnelling barrier is enhanced by negative gate bias. The surface potential change is related to the charge redistribution in the SET channel under the influence of gate voltage.

The static positive gate voltage $V_g = 8$ V is then applied to observe the formation of conductive channel in the SiNW. In Figure 6.6(c) the potential for electrons in the top part of the SiNW is lower than that on the bottom part. Different from the case with negative V_{usg} is gradually increased in the centre of the SiNW from the top to bottom direction. The observation of the barrier region tells us the potential energy barrier in the bottom of the SiNW is weaken. This suggests the electrons transfer channel under $V_g > V_{th}$. It is worth to noting that the potential map suggests the SET channel is not fully modulated by V_g .

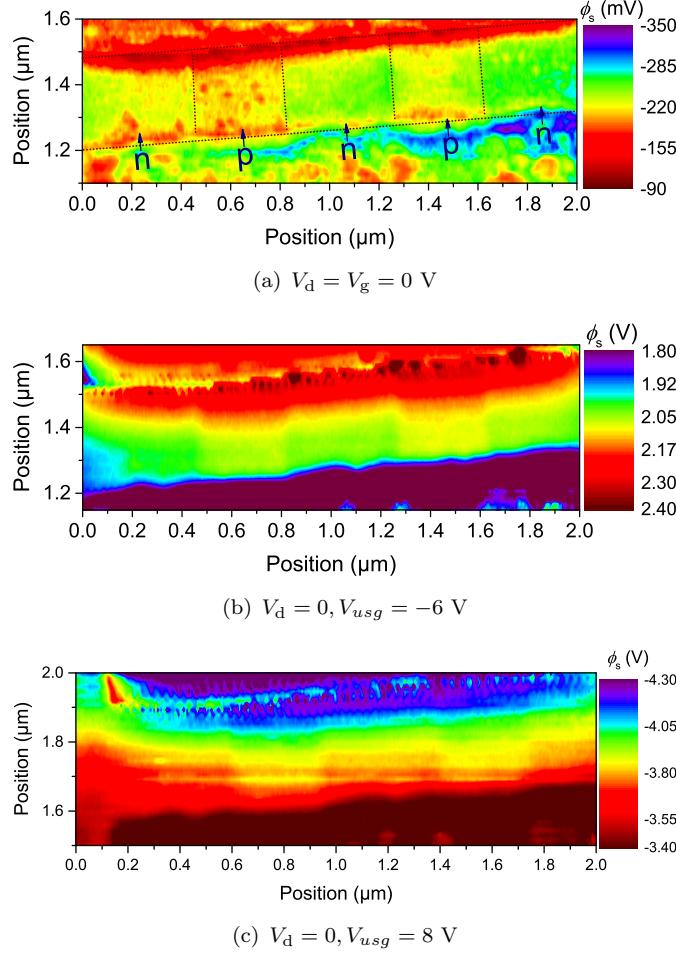


Figure 6.6: Surface potential map of SiNW SET channel under different V_g . Here, the V_{usg} is the side gate voltage. (a) $V_d = V_g = 0$ V. The boundary of p-n region shown in potential map is marked by dot line. (b) $V_d = 0, V_{usg} = -6$ V, the potential change indicated the enhancement of potential barrier in p-Si in the gate near side. (c) $V_d = 0, V_{usg} = 8$ V, the potential image shows the creation of conductive channel in the channel of gate near side.

6.3.3.2 Observation of carrier transport

The surface potential of the current running channel was measured at $V_d = 0.5$ V and with three different V_g at room temperature as shown in Figure 6.7. Under all the electrodes grounded condition (Figure 6.7(a)), the potential at the drain side is almost levelled with the source side and the potential of the two p-type barrier region is about 50 mV higher than that in n-Si region. Without side gate voltage the SiNW surface potential along the channel width is almost uniform. The potential map in Figure 6.7(b) shows that at $V_d = 0.5$, and $V_{usg} = -8$ V the potential profile in the bottom of the SiNW is abrupt but the top of the SiNW is more gradual. There are two energy peaks (~ 30 mV) in the p-type barrier close to the gate side. The abrupt and rapid potential change under V_d suggest charge carrier depletion in the n-p-n structure as we studied in the previous chapter. On the other hand the more gradual potential change suggest the

current path. In this figure, the sub-threshold current of 0.24 nA is flows through the top half of the SiNW.

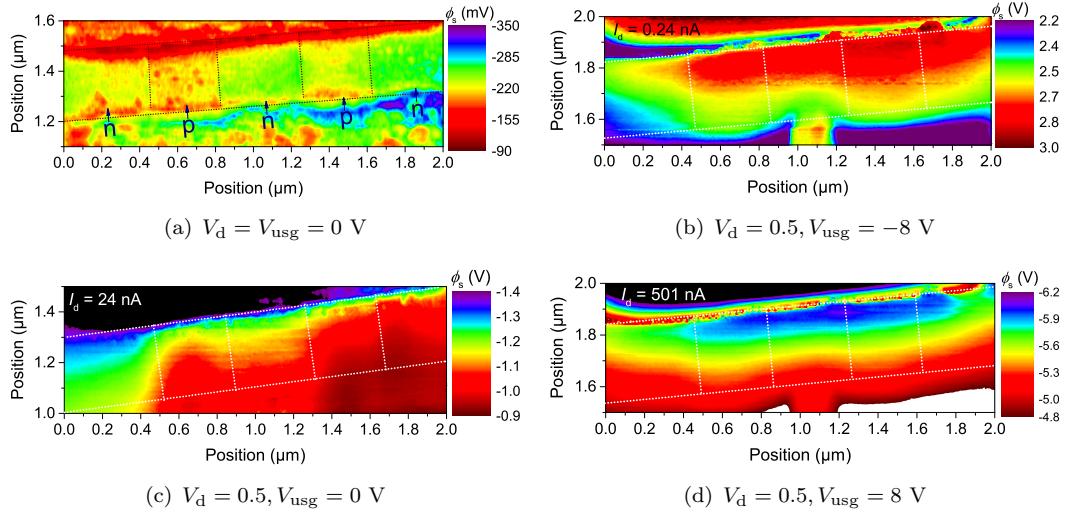


Figure 6.7: Surface potential map of SiNW SET channel under different biasing

The current in SiNW channel is increased to 24 nA when V_{usg} is increased to 0 V. Whereas, the surface potential is scanned and plotted in Figure 6.7(c). Without the influence of V_{usg} , the potential drop (~ 0.4 V in total) from the drain to the source is clearly observed in this figure. The potential drop in the channel is clearly separated into three steps which are indicated by the green (left end, -1.25 V), red (centre, -1.15 V), and dark red (right end, -0.9 V) regions, respectively. The potential step is formed at the left-hand-side of p-Si barrier. This suggests the designed p-Si barrier works to prevent the current transfer through the channel but still allow a small amount of the electron current transfer through (~ 24 nA) the channel. It is worth noting that in the island area the yellow colour tend to spread from the top island edge to the bottom edge. This change suggests more electron possibly congested in the island and change the surface potential distribution. The potential at the top edge of SiNW is higher than in the SiNW channel when the side gate is grounded. The trapped charges at the top edge of the SiNW channel could change the charge distribution and transport properties of the top SiNW region.

Once the large positive gate voltage is applied (8 V) to the side gate, the current is significantly increased to 501 nA. Meanwhile, the current conduction channel is clearly observed in the potential map in Figure 6.7(d). The surface potential of the SiNW in the top-to-bottom direction is significantly changed after $V_{\text{usg}} = 8$ V is coupled to the SiNW channel. Here the measured potential in the SiNW channel close to the gate electrode is about 1.2 V higher than the area far from the gate side. A red ribbon-like potential distribution (~ -3.55 V) is formed at the bottom edge of entire SiNW channel. Under this situation, not only the bottom side of the n-channel was turned into the red colour (~ -5.2 V) but also a narrow (~ 35 nm at -5.2 V) red ribbon is formed in the

two p-type barriers. The formation of the red ribbon suggests that the possible electron accumulation in the n-region and inversion in the p-barrier region to form a large current (501 nA) conduction path in the SiNW channel.

6.4 Discussion

The $I - V$ characteristics of single-side-gate SET devices were firstly studied at room temperature and then at low temperature (5 K). The room temperature $I - V$ study suggests that the **T** shape side gate is able to tune the energy potential formed by two tunnelling barriers. The SET channel works as a normal FET devices at room temperature. The threshold voltage of the device with the barrier size of 400 nm is around 5 V which is consistent with theoretical calculation of $V_{th} = 5.18$ V by using Equation 3.23 for FET devices. In the design, the p-type barrier is coupled with the shoulder of the **T** structure. The distance between the **T** shoulder and the p-barrier is 600 nm in design however the it is increased to 700 nm after 50 nm over etching. The consistency of threshold voltage between measurement and theoretical calculation suggests that the barrier is modulated by the side gate shoulder structure rather than the bulge which have shorter distance 300 nm to the island. In addition, the large sub-threshold leakage current for the device with the narrower p-barrier ($L_p = 250$ nm) indicates that the narrow barrier is not sufficient to build up the charge transfer barrier at room temperature. The lateral dopant diffusion measurements discussed in the previous chapter suggests that the length of lateral dopant diffusion is 107 nm. Therefore, the designed 250 nm p-barrier is reduced to only 36 nm in the real fabrication resulting in the large sub-threshold leakage current. Furthermore, in the room temperature $I - V$ characterisation, the island-size-dependent maximum current level is observed. It can be contributed to the length related channel resistance change. The maximum current of the device with the in longer island ($L_{qd} = 400$ nm) is 50 nA, while the one with the shorter island ($L_{qd} = 200$ nm) is 95 nA. The maximum current is about 2 times larger for the device with the shorter island. This result suggests the resistance of SET devices at room temperature is mainly contributed by the SET island and two barriers.

The Coulomb oscillation characteristics at 5 K suggest that the intrinsic Si is able to construct tunnelling barriers for SET devices. The change in the oscillation period suggests that the SET devices are also sensitive to the change in gate capacitance. Here, the oscillation period for the SET with $L_{qd} = 400$ nm is 1 V and 0.2 V for the one with $L_{qd} = 400$ nm. The gate-island coupling capacitance C_g is estimated as 0.16 aF and 0.8 aF for the long and the short island devices, respectively, by using Equation 3.29. The physical gate-island capacitance based on device design are 0.89 aF for both the long island (400 nm) SSG-SETs and short island (200 nm) DSG-SETs. Here, the physical gate capacitance estimation for the short island DSG-SET is consistent with the capacitance value estimated from Coulomb oscillations. However the physical gate capacitance for

the long-island SSG-SET is overestimated comparing to the capacitance estimation from the Coulomb oscillations. The physical structure of side gate for measured long-island SSG-SET could be different from the design and a larger air gap is expected by looking at the oscillation period and also a significant increase of threshold voltage.

The tunnelling capacitance in two tunnelling barrier can be estimated by depletion capacitance at 5 K. The depletion width of p-region is estimated as 794 nm at 5 K by using Equation 3.14 and Equation 3.17. The total length of barrier is 400 nm therefore the entire p-junction is fully depleted and the depletion capacitance is estimated as 4.3 aF by $C = \epsilon_{si}A/d$. Here, the area A is calculated by 335 nm in SiNW width and 50 nm in SiNW thickness. Due to the the SOI substrate is floated during the measurement the substrate capacitance is not considered. As a result the total capacitance for short island devices is $C_{\Sigma} = C_g + 2C_d = 8.9$ aF. Then Coulomb oscillation window which is the low current level (dark region) in Figure 6.5 is estimated as 18 mV by using $V_d = q/C_{\Sigma}$ which is agrees with the measurement value. In the diagram, the oscillation amplitude is large and not fully measured when V_g close to V_{th} . With increasing in V_g , the oscillation amplitude is reduced to around 5 mV , suggesting that the tunnelling capacitance is increased due to the reduction of the depletion width. This phenomenon is consistent with the depletion width study in the previous chapter. More details will be also possible to extract by KPFM measurement, however, this has not been done due to a time limitation.

The surface potential map of the single side gate long island device reveals the formation of tunnelling junction and potential change in the SiNW channel under different biasing conditions. The change in potential suggests the change in charge carrier distribution in the island and tunnelling barriers. The observation in the potential map by changing the side gate voltage suggests that the SiNW channel is partially modulated by the side gate electrode, *i.e.* only 200 nm out of 330 nm wide barrier shows charge accumulation under the negative gate voltage and 30 nm of 330 nm wide barrier is inverted under the positive gate bias. The detailed analysis of actual change in SET is useful information for the deep understanding of the electrical characteristics of SET devices, *e.g.* junction size, tunnelling resistance and capacitance, dimension of effective island, *etc*. However due to a time limitation, quality surface potential scan has not been done. As the Nanonics CV2000 measurement system is capable to change the measurement environment, to the vacuum and low temperature scan is suggested in future work.

6.5 Conclusion

To sum up, the electrical characteristics and surface potential of doping modulated single side gate single electron transistor are discussed in this chapter. The room temperature $I - V$ characteristics indicates that the SET channel is able to be modulated efficiently

by the **T** shape side gate. Coulomb oscillation behaviour suggests two low doped p-ribbons are sufficient to confine electrons in the SET island at low temperature. The agreement between oscillation period and the calculation result suggests the oscillation in the short island SET is consist with the designed structure. On the other hand, the long island shows inconsistent oscillation period. The KPFM is suggested to be able to reveal the formation of SET structure and the change inside the devices under operation. In the end, the attempt has been made to characterise the SET devices by using surface potential information. Due to a time limitation, the details of change in island and junction are not analysed. In addition, the temperature dependent measurements are preferred in the future work.

Chapter 7

Conclusions

This thesis has evaluated and demonstrated a novel way of SiNW FET and SET characterization by measuring local surface potential distribution using the KPFM technology. As the FET devices are further shrunk into nano scale, the local parameter variation tends to dominate the characteristics of nano devices. The variation of nondestructive local surface doping profile change is detectable. With improved resolution, the KPFM is expected to be able to detect fixed surface charge and individual dopant atoms near surface. On the other hand, the charge distribution in the SiNW channel is confirmed to be measurable during device operation. This thesis has evaluated and demonstrated a novel way of SiNW FET and SET characterization by measuring local surface potential distribution using the KPFM technology. As the FET devices are further shrunk into nano scale, the local parameter variation tends to dominate the characteristics of nano devices. Thanks to the KPFM technology, the variation of nondestructive local surface doping profile change is detectable. With improved resolution the KPFM is expected to be able to detect fixed surface charge and individual dopant atoms near surface. On the other hand, the charge distribution in the SiNW channel is confirmed to be measurable during device operation.

Extraction of a local potential information at nano scale is a challenging work. In the initial stage of this project, I have focused on understanding of KPFM equipment and optimization of the measurement set-up. Good agreement between the theoretical prediction and the measurement result of CPD on Au and Al film was confirmed. Then the doping profile change has been successfully measured for a 50-nm-thick SOI. The later local resistivity characterisation work in Chapter 4 shows good agreement with other characterisation method, *i.e.* four probe, hall effect, and resistivity estimation from the dopant diffusion simulation. The successful measurement of local resistivity suggests the KPFM measurement shows good response to the change of externally applied bias. The CPD calibration works give us better understanding of CPD measurement and confident for device measurements. The CPD calibration in vacuum has been also performed. The

vacuum test shows large impact of moisture molecules on CPD measurements. This result suggests that in characterising nano FET devices, it should be very careful as the results would be different between in ambient and vacuum.

Several types of SiNW devices (uniformly and heavily doped SiNW, multiple n-p-n structure FET, and single-side-gate doping-modulated n-p-n-p-n SET) have been tested for the study of KPFM's ability for SiNW measurements. In the measurements of uniformly heavily-doped silicon nanowire devices, the trapped surface charge and local resistivity of each individual SiNWs were estimated in the range of $5.32\text{-}7.27 \times 10^{-4} \Omega\text{-cm}$ by using surface potential information from KPFM and it is close to the range of resistivity value which is $2.54\text{-}6.91 \times 10^{-4} \Omega\text{-cm}$ by the other measurement methods (Hall effect measurement, Four probe, and $I - V$). After the characterisation of local potential drop in uniformly doped SiNW channel, the KPFM was then used to characterise the doping modulated n-p-n FET transistor to study the doping profile and the behaviour of p-n junction under operations. The KPFM measurement results have been used to estimate the position of metallurgical p-n junction and the result indicates the length of lateral dopants diffusion is 107 nm in furnace diffusion process. Then, the charge redistribution in a p-n-n structure was studied under the influence of gate and drain bias and the transition of capacitance behaviour to resistive behaviour of n-p-n structure has been revealed by the surface potential curve to explain the charge transport property through the n-p-n structure. In the end, the novel doping modulated single side gate SET devices were designed based on the study of metallurgical p-n junction and the p area which is various from 250-400 nm is used to build the tunnelling junction of SET. The formation and the operation of tunnelling junction in a fabricated SET was confirmed by room temperature KPFM scan and the charge carriers manipulation in island and tunnelling barrier is clearly shown in surface potential map. Coulomb oscillation diamond shown in I-V image suggests that the SET is able to be constructed by doping modulated n-p-n-p-n SiNW and the operation of n-p-n-p-n SiNW SET can be further studied by KPFM scan.

7.1 Future Work

This work has demonstrated an ability of the KPFM measurement. The KPFM is able to measure surface potential variations which are influenced by doping, surface contamination or bias application with the high lateral resolution. Assisted with the information of surface potential map, the doping profile change and a charge carriers in devices is able to be estimated so that electrical characteristics can be deeply understood.

The in-situ local resistivity characterisation experiments suggest that the KPFM is sensitive to the externally applied V_d and surface trapped charge. However, during the

characterisation of doping modulated FET devices, it is found that the measured built-in potential in p-n junction is significantly smaller than the theoretical exception. This phenomenon limits the precise estimation of local charge carrier density inside of SiNW devices. The reduction of V_{bi} in the p-n junctions is caused by a poor KPFM feed back loop which the p-channel is connected to KPFM through p-n junction. The AC signal which applied for DC detection smears the build-in potential in a p-n junction. To improve the quality of p-n junction characterisation, the direct connection to the p-channel is necessary since the AC signal tends to coupled directed through electrode. In addition, the vacuum measurement could improve the surface state of SiNW channel since the moistures molecule can be removed by vacuum.

In addition, more future work can be suggested for the SET devices characterisation. Again, the surface potential is preferred to be taken in the vacuum environment. Secondary, the potential scan can be focused to the tunnelling barrier p-type ribbon to observe the actuate size of barrier and electric field change in the barrier. For the advanced characterisation, the temperature dependent measurement is preferred. Due to the change in temperature the formation of barrier is also changed. The successful observation of temperature dependent change could facilitate a deep understanding of SET devices.

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