Metal Oxide-enabled Reconfigurable Memristive Threshold Logic Gates

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***Abstract*—With the recent advances of the emerging memories technologies, research are able to implement novel circuits, systems and computer architectures towards the design of high-performance and low-power electronic systems able to accelerate and/or optimize the functionality of many computer workflows. One emerging technology, the ReRAM/memristor is gathering attention due to its inherent advantages for logic and memory computing systems. At the same time, CMOS circuit design seems to have reached a limit, where easily optimized circuit solutions cannot be found. Thus, further research towards novel logic gate families, such as Threshold Logic Gates (TLGs), a logic family known for its high-speed and low power consumption, is needed. Although many implementation concepts of TLG circuit are using memristors, few of these implementations are based on physical ReRAM devices. In this work we are proposing a memristor-based threshold logic gate design towards the optimization of computer workflows. The presented results include a physical implementation of the proposed circuits which supports the concept of memory-based reconfigurable computing circuits and systems.**

Keywords—memristor, ReRAM, reconfigurable, Threshold Logic Gates, Current-Mode, synaptic weight, memristive neural networks, artificial neural networks

I. INTRODUCTION

Nowadays, conventional computers are based on MOSFET devices and CMOS technology, which became the catalyst for the acceleration of digital electronics the last decades. Although there is still optimism for future improvement of CMOS, the accumulating of scientific evidence indicates the need for advances in new emerging technologies to replace MOSFETs, due to the physical limitations their miniaturization is imposing, as well as new computer technologies and architectures that will enable novel high-performance and low-power computing systems [1], [2].

Recently, many researchers have been focusing on emerging memory technologies such as Phase Change Memory (PCM), Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM), Resistive Random Access Memory (ReRAM) etc. One of the most promising of these technologies is ReRAM, also known as the memristor devices [3]. Some of the most important ReRAM advantages consist of non-volatility, non-linearity, scalability and compatibility with conventional electronics, making them ideal for a wide range of computing applications [4]–[6]. Additionally, the capability of the memristor device to assume multiple states, thus acting as tuneable resistive elements, makes it a promising candidate for many computing applications, including efficient synaptic weights circuit designs.

One of the technologies that benefit from the emergence of memristor devices is the threshold logic (TL) circuits and systems. Some research teams have already seen the effectiveness of the memristive circuits and systems and moved towards applications of memristor-based threshold logic gates (TLG) that could potentially enable novel high-performance memory-centric computer architectures [7]–[9]. Novel methods of implementing TL with emerging technologies have been showcased in some important research findings. Still there are no physical implementations of these proposed circuits that would enable a better understanding of the possible capabilities that could be exploited.

In this work we present a technology for implementing reconfigurable logic gates based on metal oxide-based memory cells, towards building the hardware framework of VLSI-compatible artificial neural networks (ANNs). Specifically, in section II we present the theory of the proposed logic methodology and provide details about current-mode (CM) TLG design as well as the circuit's operation cycle. In section III we present some details of the memristor device technology being used in the experiments. In section IV, we showcase the performance of the proposed Memristive Current Mode Threshold Logic Gate (MCMTLG) through results of our physical implementation regarding fundamental 2-input Boolean functions. Finally, in section V, we present our conclusions regarding the proposed TLG circuit implementation.

II. THEORY

A. Circuit Design

With research in ANNs the first simplified model of all-or-none neuron functionality was introduced. The so-called TLG was a model for performing the comparison of a threshold value to the weighted sum of an input vector. Each weight is assigned to each input and defines the impact of that input to the logic operation of the weighted comparison. TLGs are meant to be used as basic VLSI synaptic and neuron circuits, thus forming fundamental building blocks of unconventional neuromorphic circuits and systems. Naturally, neurons are complicated systems and the simplification to threshold logic elements is questionable. However, the TLG provided a powerful tool in the hands of electrical engineers, enabling a range of efficient logic gate families used in the

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implementation of high performance and power efficient computer architectures [10].

Many different implementations of TLGs have been proposed with different trade-offs regarding their power-noise ratio performance [10]. Recently, the use of CM differential TLGs [11] seems to gaining ground as one of the efficient and fast TL implementation [8]. The basis of our proposed design is the work of Dara et al. in [8] and [9]. The circuit implementation of CM TLGs consists of two parts, the differential and the sensor part. The differential part defines the input and threshold circuits, with their configuration defining the current flowing towards the sensor of the circuit, and the sensor part defines the thresholding element of the circuit, which performs the integrate-and-fire operation.

Fig. 1 shows the design of the Memristive CMTLG (MCMTLG) practically implemented in this work. The differential part consist of two parallel circuits, one defining the threshold vector, the other defining the input vector. Each circuit is connected to one input of the sensor part. The threshold and input vectors parts are defined by two banks, one per vector, of parallel 1 pMOS transistors and 1 memristor (1T1M) composite sub-circuits. The pMOS is enabling or disabling the contribution of each memristor to the current driving operation of the differential part. At the same time, the reconfigurable weight of the memristor devices is itself defining the exact rate of contribution to the final branch current, if enabled by the accompanying pMOS device. The number of the 1T1M circuits in the vector banks and the weights per 1T1M circuit define the current able to be generated through the differential part. Hence the memory-based configurability provided by the 1T1M circuits is defining the functionality of the TLG. In Fig. 1 circuit example the threshold vector is consisting of one 1T1M while the input vector consisting of two 1T1M.

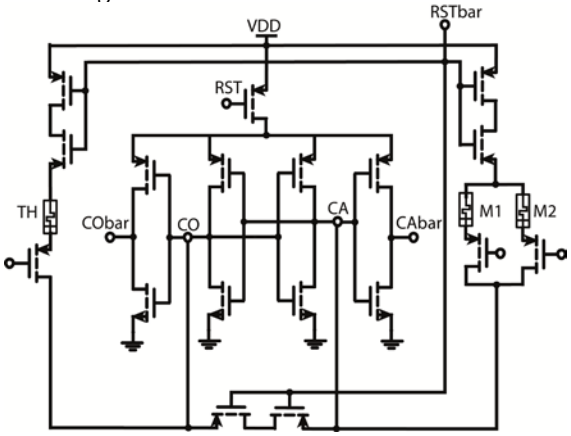

Fig. 1. Memristive Current Mode Threshold Logic Gate (MCMTLG) implementation schematic. Memristors TH, M1 and M2 define the weight per input/threshold of the differential networks. The cross-coupled CMOS inverters (latching element) are the sensor part of the TLG and feed into standard isolation inverters. The outputs of the latching element are defined as CA (canonical) and CO (complementary).

The sensor part circuit is designed as a CMOS-based SRAM memory cell, e.g. a latching element, consisting of two back-to-back (BtB) connected CMOS inverters (Fig.1). The differential part is connected to the drains of the CMOS latch, each branch to a different drain of the BtB inverters. The drains of the sensor are used as inputs for the differential part, during the equalization (reset) phase, while during the evaluation (set) phase are used as outputs of the MCMTLG. The CMOS latching element used for the sensor is operating as a current comparator performing a differential compare function with memory.

Furthermore, two additional CMOS inverters are added at the outputs of the sensor part, one per output, thus avoiding any voltage level degradation and isolating the sensor with the circuitry connected further down the logic cascade.

Due to power-consumption minimization we added a power gate pMOS controlling the power supply of the sensor circuit [11], that turns off the CMOS sensor during equalization phase. Additionally, similar to DCCML TLG design [8] we are using a parallel voltage supply connection for the differential part. The threshold and input networks are consisting of 1T1M circuits, as proposed in related work of memristor-based CM TLG design [9]. For our physical implementation, each parallel circuit uses a two pMOS back-to-back circuits to control the connection of the input and threshold vectors to the reading voltage supply, which is the voltage supply driving the currents of the differential part to the sensor part, thus avoiding logic state degradation of the latching element. Additionally, the BtB pMOS circuits enabling lower power consumption, due to the fact that the differential part does not consume power during the evaluation phase. The voltage supply V_{DD} used in the proposed design is 0.65V, thus ensuring the operational compatibility with the memristive devices being used. Furthermore, BtB pMOS circuit was used also for the equalization circuit that reset the sensor part before the evaluation being performed. The V_{RST}, which control the operation cycle of equalization/evaluation, is 1V.

B. Circuit Operation

The basis of the operation in MCMTLG circuits is the current comparison driven through its differential part from the thresholder circuit, performing current sensing and comparison. The differential part consist of two parallel branches of variable resisistances. Based on the resistance of each path a unique current is feeded to the sensor defining the output of the TLG. The sensor part operation determined by a reset/set cycle, where the part is initialized and then compare the two current generated by the resistive differential paths. The used terminology for the aforementioned operation phases is equalization, regarding the operational preparation of the sensor (reset), and evaluation, regarding the comparison and bi-stable latching (set) [11].

During the equalization phase (EQ) where the reset signal is *HIGH* (1V), the drains of the CMOS latch are short-wired, thus equalizing the voltage level output of the BtB inverters. Simultaneously the voltage supply powering the CMOS inverters is cut-off through a pMOS device power gate. The input cut-off of the differential part connects the reading voltage supply to the memristive parallel paths, thus driving current towards the two inputs/outputs of the sensor part. The differential currents are determined by the total per branch impedance imposed by the memristor devices. As soon as the reset signal goes *LOW* (G_{ND}), thus during the evaluation phase, the sensor power gate connects the voltage supply to the latch

and the isolation inverters while disabling the connection between the complementary outputs of the CA and CO nodes (see Fig.1). The differential part is also cut-off from its power supply through two pMOS-based BtB circuits and no current is flowing from the differential branches to the sensor part. Hence, during the evaluation phase the sensor is enforced to latch into a stable memory state determined by the total differential currents. The evaluation is completed when the sensor performs latching to a bi-stable memory state. Since a stable latching operation is performed, the differential part is being cut-off from the reading voltage supply, thus disabling the current flow towards the sensor part.

III. TECHNOLOGY

All circuits implemented throughout this work rely on the rich dynamics of an in-house metal-oxide ReRAM technology employing metal-insulator-metal devices. Originally, the devices were fabricated on 6-inch SiO_2/Si wafer with bottom and top electrodes patterned using optical lithography, e-beam evaporation and liftoff processes. Similar processes were adopted for the active layer patterning, except that sputtering was used for the deposition with a magnetron-sputtering tool. The active layer is constituted of TiO_2 and Al_2O_3 thin-film metal-oxides. After dicing, 3x3 mm^2 wire-bonded chips containing memristor devices were obtained, with ReRAM constituting of Pt/Al_2O_3/TiO_2/Pt/Ti (10/4/25/10/5) nm. Fig.2.a shows an image of 32 stand-alone 30x30 μm^2 cross-bar devices. Prior any use in TLG circuit the devices were pre-conditioned separately by electroforming and resistance stabilization in the required functional range [12].

One of the most important advantages of the memristive devices is the multi-state programming capabilities. Novel levels of multi-bit performance were introduced recently [12]. The importance of such performance is that it is offering an unprecedented reconfigurability towards implementing hardware synaptic weights circuits and systems. The arbitrary programming of a set of memristive states, enabled by this technology, through the multi-bit memristor technology is shown in Fig. 2(b).

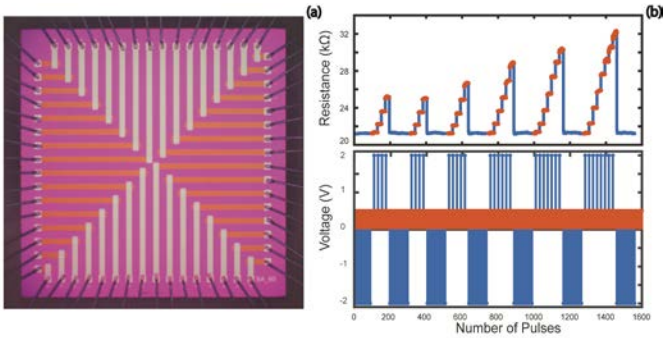

Fig. 2. Characteristic behavior of our memristor devices technology. (a) illustrates a standalone memristive topology. Each crosspoint between top (vertical) and bottom (horizontal) electrodes is a memristive device. (b) arbitrary programming of a test device to selected memristive states [12]. Upper trace: device resisive state evolution. Lower trace: programming (blue) and the read-out (orange) pulses.

Scalability is another advantage of memristors when used in cross-bar array configuration. Pi et al. have demonstrated devices down to 8x8 nm^2 [13] and Khiat et al. have fabricated arrays with 37 pitch, demonstrating a density of 1kbit devices in 1.44 μm^2 surface area [14]. Nonetheless, scalability of resistive switching devices using arrays is reaching the full potential only after resolving sneak-current issue by introducing appropriate selector devices.

IV. IMPLEMENTATION AND RESULTS

The circuit, presented in Fig.1, was implemented on breadboard using discrete components. Discrete pMOS devices of type NDP5020P (1H10AA) and nMOS devices of type SUP85N02-03 (T32BAA) were used. The memristive elements were packaged in a PLCC68 carrier and connected to the MOS-based part of the circuit via a breakout board. Memristive devices details are provided in section III. Power was provided through a benchtop power supply and the control signals (clock and input vector) were generated by a Raspberry Pi. We used this system to demonstrate how changing the threshold and/or input composite memristances we can achieve the operational functionality of multiple Boolean logic gates, through the employment of the same circuit.

A. OR/NOR (MAJ-1) MCMTLG Configuration

We are using the circuit presented in section II, in Fig.1. The physical implementation for the 2-input AND MCMTLG configuration is based on the weight configuration of {*M1, M2; TH*} = {*22k*Ω, *22k*Ω*; 52k*Ω}. Due to the operation of the latching element as a bi-stable memory cell, the CA output is performing an OR function, while the CO output is performing the complementary function, NOR.

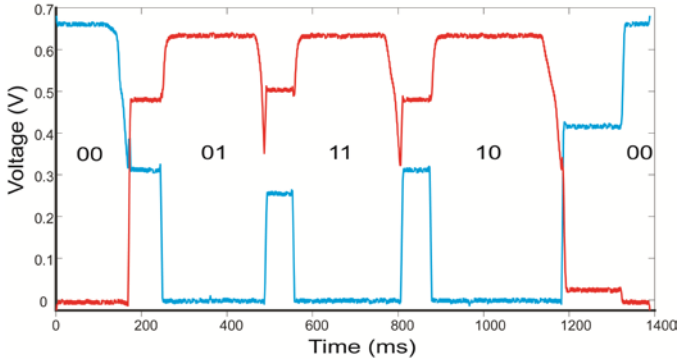

Fig. 3. Measured results of the sensor part outputs regarding the OR/NOR functions configuration. The memristances are programmed to {M1, M2; TH} = {*22k*Ω, *22k*Ω*; 52k*Ω}. The graph showcases four equalization/evaluation operation cycles, where all the cases of the input vector are tested. Red data indicates OR (CA) functionality while blue data indicates NOR (CO) functionality.

The aforementioned differential impedances are enabling a majority functionality in the implemented circuit, where at least one of the input 1T1M sub-circuits (MAJ-1) have to be conductive in order for the input network conductance to enable higher current flow toward the sensor part, thus enforcing a change in the memory state of the CMOS latching element. For an input network of only two inputs (two 1T1M parallel circuits) the MAJ-1 gate is equivalent for a 2-input OR Boolean gate.

TABLE I. MCMTLG OPERATION FOR OR FUNCTION

Input Vector	Composite Memristive Weights of Differential Part		
	Input Network Impedance	*Bias Network Impedance*	*Fn(Comp) dur. EQ*
00	*Inf* kΩ	52kΩ	~ $0A_{(CA)} \leq 7.98uA_{(CO)}$
01	22kΩ	52kΩ	$21.8uA_{(CA)} \geq 6.05uA_{(CO)}$
10	22kΩ	52kΩ	$21.8uA_{(CA)} \geq 6.05uA_{(CO)}$
11	11kΩ	52kΩ	$45.9uA_{(CA)} \geq 4.90uA_{(CO)}$

Fig. 3 presents the circuit response regarding all the cases of the truth table, where both the canonical and complementary outputs of the sensor part are shown. The truth table with the approximate memristive weights, that defines the current comparison performed by the sensor part in the OR configuration, is shown in Table I, where the total composite impedance of each network is shown, with the difference in current flow per network, defining the comparison operation performed during each transition from the equalization phase to the evaluation phase. The current values with CA (CO) sub-note indicate the total current in canonical (complementary) node.

B. AND/NAND (MAJ-2) MCMTLG Configuration

Similarly to the physical implementation of the OR MCMTLG, the AND MCMTLG used the same circuit design presented in Fig.1. Through programming of the threshold memristor we are able to alter the functionality of the MCMTLG. Specifically, by setting the value of the threshold memristor to *11k*Ω, instead of *52k*Ω, we can perform a 2-input AND operation. The differential part configuration is set as {M1, M2; TH} = {*22k*Ω, *22k*Ω*; 11k*Ω}. The change in the functionality was enabled only by altering the memory states of the ReRAM devices, thus altering the current comparison winning condition, generated by the differential part.

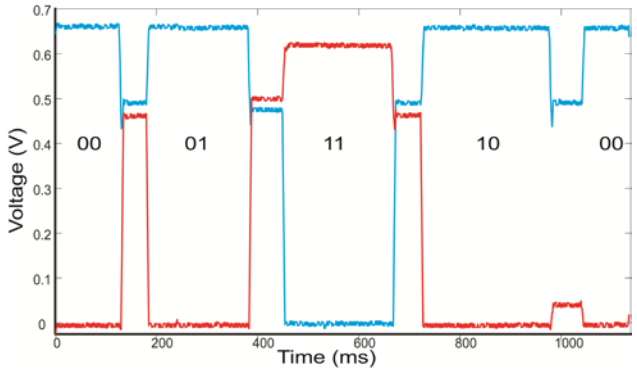

Fig. 4. Measured TLG sensor part outputs in the AND/NAND configuration. Memristances values are: {M1, M2; TH} = {*22k*Ω, *22k*Ω*; 11k*Ω}. Four equalization/evaluation operation cycles are shown, covering all possible input vector cases. Red data indicates AND (CA) functionality while blue data indicates NAND (CO) functionality.

Both AND and NAND functions is performed simultaneously due to the complementary bi-stable operation of the sensor part. The truth table with the composite memristive weights that defines the current comparison for the AND gate configuration as well as the current flow per network that are measured during the comparison operation, are shown in Table II. Similarly to the Table I, the current values with CA (CO) sub-note indicate the total current in canonical (complementary) node.

TABLE II. MCMTLG OPERATION FOR AND FUNCTION

Input Vector	Composite Memristive Weights of Differential Part		
	Input Network Impedance	*Bias Network Impedance*	*Fn(Comp)dur. EQ*
00	*Inf* kΩ	11kΩ	~ $0A_{(CA)} \leq 44.5uA_{(CO)}$
01	22kΩ	11kΩ	$20.9uA_{(CA)} \leq 44.5uA_{(CO)}$
10	22kΩ	11kΩ	$20.9uA_{(CA)} \leq 44.5uA_{(CO)}$
11	11kΩ	11kΩ	$45.4uA_{(CA)} \geq 42.7uA_{(CO)}$

V. CONCLUSIONS

In this work we have presented a physical implementation of a TLG circuit using reconfigurable memristive loads enabling mixed signal TL operation by using analogue weight elements as the binary signal multipliers of the input/bias vector. Through the showcased experiments we can confirm that the comparison operation between the memristance of the threshold device against the composite impedance of the input network is determining the circuit functionality. This enable us to build hybrid memristor-CMOS perceptron circuits, the fundamental building blocks for a wide range of ANN systems. Advances of the technological frontier of novel memristive TLG circuits and systems design could provide benefits to low-optimized digital circuitry such as CMOS implementations of popular operations like convolution, encryption and other massively parallel bitwise-based operations. Thus more effort is needed towards the implementation of new digital and mixed signal logic families approaching hardware realizable ANN-based computing paradigms.

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