Live Demonstration: Benchmarking Analogue Performance of Emerging Random Access Memory Technologies

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***Abstract*—In this demo we present a comprehensive solution for benchmarking the multibit capabilities of resistive memory cells using sequential programming pulses. The algorithm is presented through a rich graphical user interface that allows the user to fully tune the benchmarking parameters**

Keywords—memristors, RRAM, multibit memory, analogue memory, non-volatile, characterization

I. Introduction

Resistive memory cells exhibiting memristive behavior [1], [2] have attracted particular scientific attention due to their increased array of potential applications. Of particular interest is the application in developing non-volatile memories and on-memory computing nodes in the form of neuroinspired circuits. Key parameter for these applications is the ability to maximize the available resistive state of a memristive cell. For this purpose we developed a comprehensive evaluation algorithm [3] to assess the number of available resistive levels in a given cell.

II. Demonstration Setup

The setup consists of a laptop connected to our in-house developed memristor characterization platform [4], ArC ONE™ (fig. 1) running an implementation of the proposed evaluation algorithm. TiO_2-based resistive memory devices packaged in PLCC68 housing will be available for in-situ assessment through the developed graphical user interface (fig. 2).

III. Visitor Experience

The visitor can use the demonstrated software to characterize the packaged devices, manually tune the various parameters and observe their effect in partitioning the operating range of the device into discrete resistive levels. All tunable parameters described in the characterization method are exposed to the user through an easy to use graphical interface while the different phases of the algorithm can be run independently. The results are presented either in a tabular or graphical format and can be extracted for further analysis.

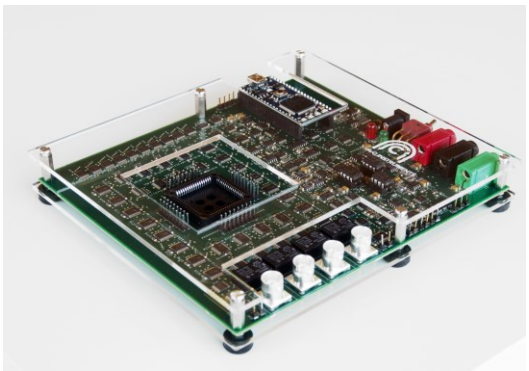

Fig 1: ArC ONE™ parallel memristor characterization platform

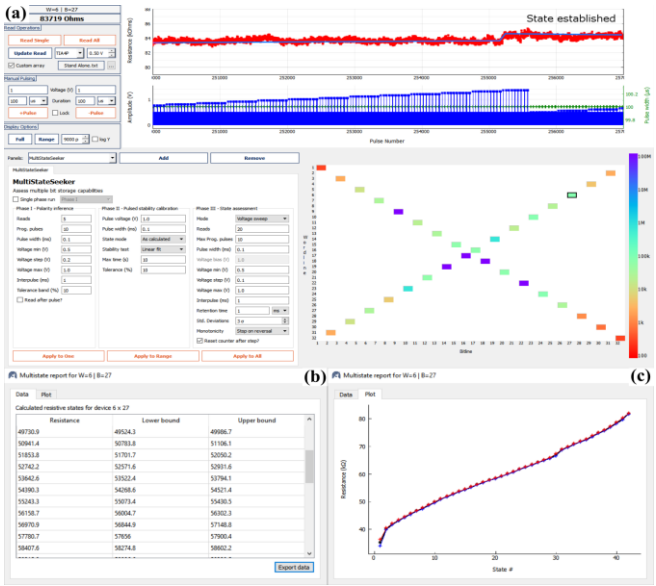

Fig 2: Graphical interface of the implemented algorithm: (a) Device map and current state; list (b) and plot (c) of the extracted resistive states

References

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