Benchmarking Analogue Performance of Emerging Random Access Memory Technologies

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***Abstract*—In this work we present an evaluation routine aimed towards assessing the multibit capability of Resistive Random Access Memory (RRAM) technologies. We illustrate a characterization methodology for the maximum possible exploitation of the resistive states of a RRAM cell. Our characterization routine consists of a three phase algorithm: during the first it infers the polarity needed to induce a change in the device's conductance; the second stabilizes the resistive states of the device into a baseline resistance and during the third a sequence of pulses of increasing amplitude is used to determine the actual resistive states. This technology-agnostic methodology allows for efficient and high resolution partitioning of the cell's resistive operating range allowing them to operate in a truly analogue fashion. Demonstrating the maximum potential of RRAM cells in terms of closely packed resistive states can open new avenues for research in non-volatile memories, reconfigurable electronics and neuromorphic applications.**

Keywords—memristors, RRAM, multibit memory, analogue memory, non-volatile, characterization

I. INTRODUCTION

Since the connection of solid-state resistive memory technology with the theorized fourth passive component, the memristor [1], [2], considerable scientific effort has been put into exploring its applications. Of particular interest is the potential use of such elements either as non-volatile memory cells or as memory-and-computation nodes in the form of neuromorphic circuits and on-node processors [3], [4]. Both of these use cases demonstrate significant performance benefits when realized with multi-bit resistive memory cells. Although there are reports of operating multibit-capable RRAM cells most works are limited to a maximum of 3 bits [5]–[7]. This is partly due to the fact that even though switching and characterizing a RRAM device between two extreme conductance states (1-bit) is straightforward [8], while the realization and assessment of multi-bit RRAM cells poses significant challenges both from a material science as well as a characterization point of view. Towards the latter end, we present in this paper a comprehensive characterization routine capable of determining the maximum number of resistive states available on a given RRAM cell. This allows the optimal use of the operating range of the device and enables the access of individual states in a refined and controllable manner. Section II of this paper introduces the developed characterization methodology. Section III presents distinct measured results that demonstrate the application of our characterization routine with prototype TiO_2-based RRAM cells. The final section provides concluding remarks.

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II. CHARACTERIZATION ROUTINE

Our proposed characterization algorithm consists of three distinct phases. During the first phase (*polarity inference*) the bias polarity required to switch the device is determined; during the second (*baseline calibration*) the device is driven to a stable resistive state and finally, during the third phase (*state assessment*) the resistive states of the device are determined.

A. Phase I: Polarity inference

The first phase of the algorithm is used to determine the sensitivity of the device to the polarity of the applied bias as well as determine the kind of change said polarity induces, ie. if it increases or decreases the device's conductance, similar to what has been described in a previous publication [9]. The resistance of the device is initially recorded and forms the baseline status (R_i). Afterwards a series of N programming pulses of amplitude V_b and user defined pulse width (t_P) is applied to the DUT. This is followed by a further readout of the resistance. If the resistance of the device has changed outside of a predefined tolerance band then the resistive state of the device is deemed as changed. Specifically, if said resistance is higher (or lower) than the initial state then the polarity of the programming pulses causes an *overshoot* (or *undershoot*, respectively) in the resistive state of the device.

On the other case, if the resistive state of the device has remained within the tolerance band then the programming pulses are applied again with inverse polarity. In the case where this biasing scheme also fails to elicit a non-volatile response from the device (resistance still within tolerance) the polarity of the programming pulses is switched again with the amplitude increased by V_{step}. The algorithm terminates if no inference can be made regarding the switching polarity after a maximum biasing amplitude (V_{max}) has been reached and tested with both polarities. Otherwise the assessment continues to phase II. An outline of phase I can be observed in fig. 1a. At the end of the test we can quantify the amplitude

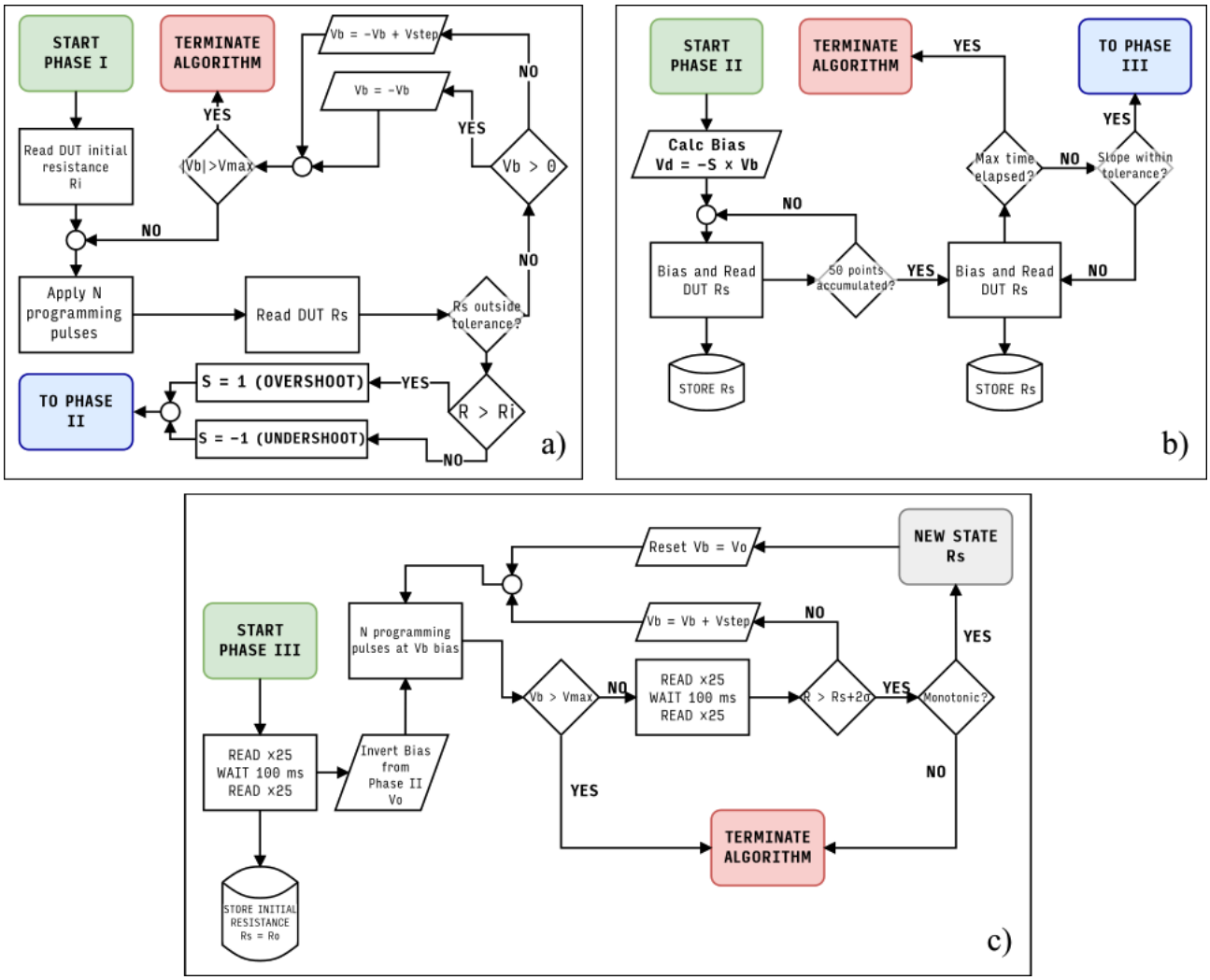

Fig. 1: Block diagram of the characterization algorithm outlined in this paper. The algorithm is composed of three distinct steps: *polarity inference* (a); *baseline calibration* (b) and *state assessment* (c). Explanations of the symbols involved can be found in table I.

and polarity parameter of a pulse signal capable of causing a significant change in resistive state in a known direction (ie. towards *higher* or *lower* resistance).

B. Phase II: Baseline calibration

The second phase of the characterization routine aims to establish the base resistance of the device under test (DUT). Using the inverse polarity from that determined at the end of phase I and a user specified amplitude (the maximum allowed driving voltage for reaching the operational edge of the resistive state range – V_d) the device is subjected to alternating programming and read pulses until at least 50 measurements have been accumulated. Then after each subsequent measurement a linear fit is applied to determine the slope of the gathered data. If the absolute slope of the fit drops within a user-defined threshold (β) the baseline is considered stable. At the end of this phase the *operating minimum* (or *maximum*) resistance has been reached and the device can start being driven towards to its other operating range extremum (phase III). If a maximal time has been exceeded and no compliant fit has been found the algorithm terminates. A block diagram summarizing the testing methodology of phase II is depicted in fig. 1b.

C. Phase III: State Assessment

Phase III comprises the main phase of our protocol. Initially this stage reassesses the base resistive state by determining its average measured value and corresponding standard deviation. This is calculated by two sets of 25 read pulses separated by a user specified retention interval (t_{ret}), nominally at 100 ms. Then using the polarity information extracted from phase I and a user specified amplitude a programming pulse is applied followed by two sets of read pulses separated by t_{ret} to again determine the value and standard deviation (σ) of the current, potentially new, state. If this new resistance is at least 2σ higher (or lower) than the previous state then a new state, R_s, is considered as registered. Otherwise the process repeats, but this time sending a train of two programming pulses. If this also fails to reach a new state, 3, 4, and up to a maximum of N programming pulses are sent. At this point if no resistive state has been established the programming amplitude is increased by a user specified voltage step (V_{step}) and the number of pulses/train is reset to 1. The process then repeats until a maximum programming voltage has been reached. This is a more refined version of the characterization routine described in [10], which itself follows from standard practice in commercially available flash

TABLE I. ALGORITHM PARAMETERS

Param.	Description	Unit	Value
Calculated parameters			
V_R	Read voltage (fixed at 0.5 V)	V	N/A
R_i	Initial resistance	Ω	
R_s	Current resistive state	Ω	
V_b	Programming voltage	V	
S	Switching polarity sign, -1: under- or +1: overshoot	—	
User controllable parameters			
N	Maximum programming pulses	—	10
V_d	Baseline driving voltage	V	–3.0
V_o	Initial programming voltage	V	1.0
V_{step}	Programming voltage step	V	0.05
V_{max}	Maximum programming voltage	V	2.0
t_{ret}	Retention time for state assessment	s	0.1
t_P	Programming pulse width	s	1×10^{7}
β	Stabilization threshold	%	

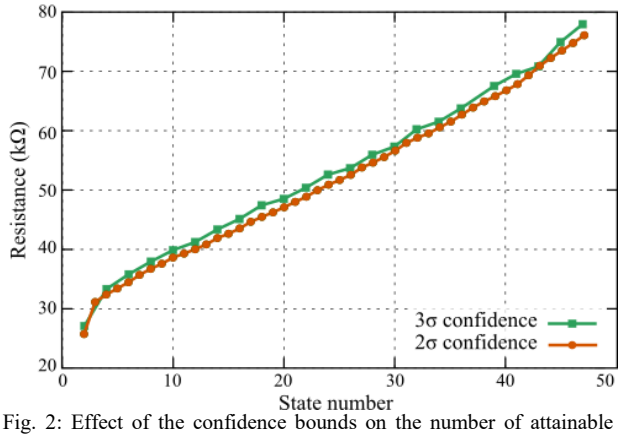

Fig. 2: Effect of the confidence bounds on the number of attainable states. Using 3σ (99.7%) as the confidence interval results to larger interval between usable resistive states but effectively the overall number of available states is halved. In contrast 2σ confidence trades-off a denser distribution of states against the discernibility between the assessed resistive steps.

memory [11]. Confidence intervals can be tuned from 1σ to 6σ to accommodate for either an increased number of states or greater resistance steps. An optional integrity test after each state assessment is also supported by the algorithm in order to determine that the extracted states are always monotonic. If the resistance trend is not monotonic the algorithm terminates. An outline of the last phase can be seen in fig. 1c. At the end of this algorithm outputs a set of distinct resistive states and their corresponding confidence bounds.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The algorithm we propose has been implemented in our in-house developed characterization platform as described in [12]. Both the derived and user controllable parameters are summarized in Table I. We have applied our characterization algorithm to assess the multibit capability on $Pt/Al_xO_y/TiO_2/Pt$ devices. The thicknesses of the device layers are Pt: 10 nm; Al_xO_y: 4 nm and TiO_2: 40 nm. Both of the metal-oxides are amorphous, fabricated by reactive magnetron sputtering. Pristine devices have been electroformed using 1 μs programming pulses with amplitudes ranging from -8 V

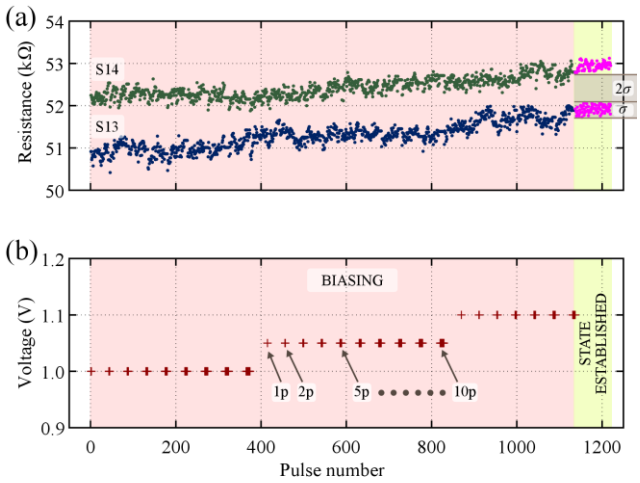

Fig. 3: Phase III snapshot of the discussed assessment algorithm during state evaluation on a $Pt/Al_xO_y/TiO_2/Pt$ RRAM cell. Resistance of the DUT is presented on the top and the corresponding biasing scheme on the bottom. An increasing number of programming (in this case up to N=10) is being applied. Between each train of applied programming pulses two sets of 25 READ pulses at V_R=0.5 V separated by 100 ms of retention time (t_{ret}) are applied. The state is established once the new resistive state is *at least* 2σ higher than the previous. The procedure repeats from the initial voltage until a maximum voltage is reached.

to -12 V to a usable resistive range of 10^4–10^5 Ω and more specifically to ~28 kΩ. Afterwards the assessment algorithm is applied. The initialization of the user controllable parameters can also be found in table I.

Using the above set of parameters a summary of the calculated resistive states for $Pt/Al_xO_y/TiO_2/Pt$ DUT can be seen in fig. 2. Selection of the states has been made with positive polarity pulses as determined from the first phase of the algorithm. For the 3σ confidence interval 24 states can be observed (~4.5 bits per cell). Decreasing the confidence interval to 2σ leads to an increased number of states up to a maximum of 47 (~5.5 bits per cell). In each case the characterization routine allows to partition the operating range of the device with even and uniform resistive steps. The absolute number of states depends on the target application and can be tuned by tightening or relaxing the confidence bounds.

In fig. 3 a snapshot of phase III for the DUT during the transition from a lower to a higher resistive state can be seen. The device is incrementally biased with up to 10 programming pulses initially with 1 V (V_o) and then increasingly by 50 mV (V_{step}). At 1.1 V stimulus the accumulated change in the resistance of the device has already surpassed the 2σ mark above the upper bound of the previous state. As such a new state is established at 52.8±0.18 kΩ. The gradual resistance change observed during the biasing process as shown in fig. 3 results from the continuous, but gentle, voltage stress the device is subjected to during programming. The continuity of the resistance trend depends on the biasing steps as larger voltage steps will eventually result to higher resistance increments [10]. Our algorithm exploits this behavior to gradually and controllably push the resistance of the device towards a region that can be regarded as a new state.

We should stress that the long retention times used by our proposed algorithm are necessary to identify the potential resistive states of the devices but not to actually program the devices themselves. Once the states have been identified and

depending on the device under test a much faster programming scheme can be used as it is evident by [13].

Although it is obvious that the discernibility of usable states heavily depends on the imposed confidence bounds it is important to mention that usable level discernibility is different from the overall resolution that can be achieved with a given technology. As can be seen in fig. 3, while the device traverses from a lower to a higher state it passes through a series of equally valid but indistinguishable resistive levels that are gradually increasing under continuous biasing. The introduction of confidence bounds helps to establish a resistive level band that can be considered a single state.

Finally, the controllable nature of the characterization routine has the added benefit of not requiring a current compliance mechanism for state selection. Current compliance (CC) is a common method used to control the resistance of the device, however, at the cost of increased energy usage [14], [15]. Instead, in our case, by sequentially and gradually pulsing the device at a controllable manner we ensure that only the minimum required amount of programming energy is used to switch the device to a higher (or lower) level.

IV. Conclusion

In this paper we presented a novel characterization routine for benchmarking the analogue non-volatile performance of emerging RRAM technologies. Fully exploiting the potential of a memristive device in regards to the number of states is of paramount important for non-volatile memory and neuromorphic applications. Towards that end, our algorithm, comprising of three distinct phases, assesses the switching behavior of the device, and after establishing a baseline resistance sequentially pulses the device until a new distinct state has been established given a predefined confidence band. This process allows for optimally partitioning the operating range of the device as it was evident from the application of the algorithm on $Pt/Al_xO_y/TiO_2/Pt$ RRAM device. Depending on the application at hand, confidence bands can be tuned to allow for denser states with smaller resistance increments or sparser state distribution with greater steps.

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