UNIVERSITY OF SOUTHAMPTON

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SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

FABRICATION AND CHARACTERISATION OF CVD-GRAPHENE NANORIBBON SINGLE ELECTRON TRANSISTORS

by

Jamie Dean Reynolds

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Supervisors: Professor Hiroshi Mizuta

Dr Yoshishige Tsuchiya

Professor Shinichi Saito

Reviewers: Dr Stuart Boden

Dr Zahid Durrani

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ABSTRACT

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Graphene was the first 2 dimensional material discovered and rapidly received a lot of attention because of its astounding properties. It is still the highest conductivity material recorded and very robust despite its single atomic layer thickness. However a key issue with graphene has been that it is a semimetal and not a semiconductor, so it lacks a band gap. Originally a large amount of focus was on researching methods to overcome this issue for logic devices. At first the patterning into nanoribbons was seen as a method to achieve this, but the fabrication of a nanoribbon came at a cost of graphene's high mobility electrons. From conducting this research an interesting property of graphene emerged. It was capable of acting intrinsically as a single electron transistor, enabling a different type of more than Moore device to be fabricated that can be used in future nanoelectronic applications

The aim of this project has been to investigate the transport properties of polycrystalline graphene grown using chemical vapour deposition. The use of polycrystalline graphene enables the fabrication of wafer scale devices that can be stacked on a large variety of surfaces. So far though there has been a lack of investigation into the scaling effects of polycrystalline graphene nanoribbons and the single electron tunnelling properties associated with them. This work presents the first detailed investigation into their properties and shows that polycrystalline graphene can be used for producing high quality single electron transistors. Nanoribbons are fabricated down to sub 20 nm widths with high aspect ratio transitions from wide to narrow segments. The single electron transistor has demonstrated a single quantum dot impacted by the effect of energy level spacing.

Acknowledgement

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I dedicate this work to my late grandfather Bert Reynolds. I wish you could have seen how far the passion for engineering you helped inspire has taken me.

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Declaration of Authorship

I, Jamie Dean Reynolds, declare that the thesis entitled 'Fabrication and Characterisation of CVD Graphene Nanoribbon Single Electron Transistors', and the work presented in the thesis are both my own, and have been generated by me as a result of my own original research.

I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work or others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
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List of Publications

Conferences

J. Reynolds, L. Boodhoo, C.-C. Huang, D. W. Hewak, S. Saito, Y. Tsuchiya and H. Mizuta; **Transfer-last Suspended Graphene Fabrication on Gold, Graphite and Silicon Nanostructures,** *Graphene Week 2015, Manchester, UK, 22 - 26 June 2015*

Y Nagahisa, T. Zelai, J. Reynolds, L. Boodhoo, C. -C. Huang, D. Hewak, E. Tokumitsu, H. Mizuta and Y. Tsuchiya; **Tip-enhanced Raman Spectroscopy for Suspended Graphene Integrated with Silicon Nanowire Array**, *Microscopy Microscience Congress 2015, Manchester, UK, 29 June - 2 July 2015*

H.Mizuta, Z.Moktadir, S.Hang, N.Kalhor, J.Reynolds, T.Iwasaki, M.Schmidt, Manoharan M.; **Helium ion beam based novel fabrication of downscaled graphene nanodevices**, *The 15th Takayanagi Kenjiro Memorial Symposium (Invited Talk) Shizuoka University, 12 November 2013*

Z.Moktadir, S.Hang, J.Reynolds, K.Higashimine, Manoharan M. and H.Mizuta; **Metal-Insulating transition in disordered graphene nanoribbons controlled by helium ion irradiation**, *2013 International Conference on Solid State Devices and Materials (SSDM2013) Fukuoka Hilton Fukuoka Sea Hawk, 24-27 September 2013*

H.Mizuta, Z.Moktadir, S.Hang, N.Kalhor, J.Reynolds, K.Higashimine, Manoharan M.; **Study of carrier transport for graphene nanoribbons with He+ ion induced point defects and edge irregularities**, *15th International Symposium on "Ultrafast Phenomena in Semiconductors"(15-UFPS) (Invited Talk) Vilnius, Lithuania, 25-28 August 2013*

Chapter 1

Introduction

1.1 The first 2-dimensional material

Over a decade ago in 2004, a remarkable discovery was made, whereby a sheet of semiconductor material only a single atomic layer thick could be isolated and remain stable indefinitely [1]. This began as a simple experiment where graphite was repeatedly peeled with scotch tape. The transfer of the peeled graphite onto a silicon wafer yielded a distribution of various number of layers onto the surface. The subsequent experiments on a single layer of graphene revealed its incredible intrinsic properties, in doing so awarded the discoverers, Andre Geim and Konstantin Novoselov, a Noble prize. Since then there has been a rapid increase in the number of 2-dimensional materials (2DM) being discovered, with the cumulative total of publications on graphene reaching over 60,000 since 2004 [28], creating entire fields of research on utilising these materials.

There are justifiable reasons for such an interest in graphene. It behaves in a manner, unlike any other semiconductor before it. The electrons are considered ballistic due to a small electron mass compared to silicon (~16 times smaller) and measured mobilities of 200,000 $\mathrm{V^2cm^{-1}s^{-1}}$ in a graphene sheet. This far exceeds materials such as germanium or gallium arsenide, which have the next highest mobility for a semiconductor. It has a remarkable mechanical robustness demonstrating an in-plane strength that allows for it to be suspended on a large scale, yet remaining very flexible. A property that had been exploited to create a working speaker [29], showing the capabilities to survive intense fabrication aspects usually associated with silicon. Unlike bulk silicon, graphene can be doped by surface interactions from charge transfer doping and by electrostatic gating. With symmetric ambipolar conduction of electrons and holes, meaning graphene transports both charge carriers at the same velocity and can demonstrate both types of conduction intrinsically. Where graphene falls short is that it is not a true semiconductor and is instead a semimetal with a zero band gap energy.

Understandably this created a lot of embellishment about its impact on the electronics industry. Especially as the concerns for future of electronics beyond silicon move ever closer to the start of the more than Moore era [30]. Since then the expectations of

graphene's use as a direct replacement material for FETs have reached the conclusion that it will never be used for logic devices in such a way. Leading research to explore other aspects of graphene's properties for analogue devices, sensors and optical devices. Along with finding alternative 2DMs that could be used instead of graphene that does not suffer its pitfalls. Although many have been discovered, there has yet to be a material that could be considered superior to graphene. This is why an intense field of research still exists to explore graphene's potential in alternative logic devices.

A lot can still be said about the potential impact of graphene, it particularly poses the question of whether a 2DM is necessary. The answer, however, is not so straight forward. The reasoning always come back to the fact it is an exceptional material by all standards. Yet it has been the pitfalls that occur experimentally when studying this material. The main consideration must always be that graphene as a physical research material has only existed for 10 years. Compared to silicon which has existed as a transistor for close to 70 years now. Despite the fact a great deal has been discovered about the semiconductor physics there is still more to discover. Especially since quantum effects play an ever increasing importance in the role of device behaviour.

1.2 Integration of graphene into nanoelectronics

The key to graphene's success in future nanoelectronic devices relies upon the need to create more than Moore devices. Where the era of Moore has seen scaling of transistor densities double every two years to improve transistor performance. MOSFET scaling has continued for the last 50 years, but the shrinking transistor size is beginning to reach its limit.

The continuous development of silicon transistors has caused their size to decrease close to a 14 nm half-pitch. With expectations to go beyond into a sub 5nm limit. At this scale, the number atoms that actively contribute to the channel region number is less than a hundred atoms. With various problems arising for silicon transistors at this scale as outlined by Bohr in 2007 [5]. The voltage scaling is limited due to an increase in the level of subthreshold leakage current contributing to a device. Meaning the threshold voltage can not decrease further without making operation unstable. The scaling of the gate oxide thickness further will cause direct tunneling through the gate to the channel occur more often. This was solved by using high-k dielectrics to give a thicker oxide to reduce tunneling probability, but this may soon reach a limit as well. Last is the effect of increasing doping concentrations. When increased too high a degradation in the mobility of the charge carriers will limit the switching speed. Additionally leakage from source and drain electrodes will occur due to band to band tunneling.

This allows the nanoelectronics field the chance to overcome the shortfalls sub-5nm MOSFETs present. However to improve the overall chip performance will not require reducing the device size. Instead, mass manufacturing will need to move towards increasing performance through other means. Such as density and switching speed, while

reducing power consumption. With added emphasis on power consumption from a shift to mobile System on Chips [SoCs] compared to traditional processors. The shift from traditional PC architectures where CPU, GPU and other ICs are collected on a motherboard, to a SoC design poses new challenges in which graphene and by extension 2DMs can exploit.

Although there is a desire to move away from MOSFETs, this is unlikely to happen in mainstream computing. Leaving the next immediate stage the 3D integration of transistors, which is already being seen in DRAM. Currently the most desirable method is to stack 2D planar transistors on silicon wafers in succession. Using via interconnects between wafers to connect between each wafer. This creates new problems in heat dissipation and the interconnect densities needed to achieve high performance. It is here that graphene has the right properties to offset wafer stacking. It can be transferred and fabricated in a compatible Back End Of Line [BEOL] process. Producing transistors and interconnects together with comparative ease. Although in terms of performance it won't beat silicon. It could be used in aspects of a systems architecture where the highest performance is not needed. Crucial silicon transistors can be dedicated to heavier processing elements without changing the transistor density.

2DMS enable multiple device layers can stack on top of each other with ease. Using different types of graphene transistors that can conduct in the horizontal or vertical plane. 2D dielectrics in the form of hexagonal-Boron Nitride [h-BN] [31] can insulation device channels. Though there has been limited attempts to create inter-graphene-connections or direct integration with silicon. The best attempt so far was by researchers at IBM [32], where graphene was used in a BEOL to compliment a silicon IC in an analogue device. Using micrometre sized graphene transistors superior cut off frequency to improve the ICs operation. Yet, it will take a lot more effort to have logic devices that can be used in a BEOL process.

This creates two sets of developments that need to be undertaken. First is a suitable process for creating graphene nanoelectronics in a BEOL. Second is to increase the capabilities or performance of graphene logic devices. The third is to prove that the two can be combined in a single device compatible with silicon fabrication techniques.

The potential of graphene to fundamentally change the semiconductor industry has a greater impact than improving the simple MOSFET. The significance graphene has over other potential materials can be seen by the sheer progress of graphene in the last decade. It is for these reasons graphene was heavily considered in the most recent ITRS report [#ITRS1]. Since then graphene has demonstrated wafer scale single crystalline growth on 8" Germanium wafers, polycrystalline for 100m rolls and 78% yield of 6" wafers with mobilities reported to be similar to silicon [33].

1.3 Applications in logic devices

Graphene is favoured more than other high electron mobility materials like InGaAs 2D electron gases. Since it is naturally a intrinsically undoped material in its pure state. Despite graphene's potential as a direct replacement there are several factors impeding the adoption into mainstream electronics. The foremost of these issues where a large focus of research has taken place is the lack of a band gap in graphene. Additionally, detrimental fabrication factors limit the ultimate performance of graphene MOSFETs. Interactions with the substrate, metal and environmental effects degrade graphene's quality by unintentional doping. Where the doping in graphene is caused by charge transfer effects from impurities. The control of graphene doping is achieved via electric field control of the dopant concentration [1]. Combined with the effects from fabrication processes limit the scope of graphene logic devices for traditional applications. In this regard, the differences between graphene and silicon seem stark at first. Where the exploration of silicon devices is attempting to go beyond the default properties of silicon. In graphene research is focused on trying to utilise as much of its potential as possible, and yet when attempting to create new types of logic the two often meet. Although graphene will not reach the ease of fabrication associated with silicon for MOSFETs in the short term. The exploration of future logic devices is still expected to diverge from classical electronics. Increasing the potential impact of graphene.

The lack of a band gap and fabrication effects degrading or creating unintentional modifications of its properties are the significant pitfall to graphene's success so far. For instance, the nanopatterning of graphene into nanoribbons to open a band gap had at first been seen as a method to accomplish this. Using lithography and plasma etching to cut the graphene into nanosized features is a well-established technology. What was not foreseen is opening a band gap in graphene demonstrated the material's weakness to defects. Creating larger than expected energy gaps while severely decreasing the conductivity of graphene. This was the leading factor in preventing graphene's use a replacement for conventional MOSFETs. As Schwierz [34]discusses graphene needs to fulfill certain criteria to be of use in complementing silicon MOSFETs, which are:

- Wide band-gap, excellent carrier transport and high thermal conductivity
- Producible on a large diameter for a high throughput
- Process friendly with standard Si CMOS fabrication techniques
- Long term stability with dielectrics (low atom drift)
- Low defect density that doesn't affect carrier transport
- Low contact resistance

So far graphene is capable of a high-throughput with standard CMOS fabrication, a high thermal conductivity, and low contact resistance thanks to its semimetallic nature.

To improve on these points advances in the state of the art for graphene nanoribbons is needed for a material in a stacked architecture. The true potential of graphene as a logic device does not exist in using as a direct replacement material for MOSFETs. Instead, a More than Moore device has the most potential for graphene. Where graphene's novel properties can be utilised to their fullest. Recent publications prove there has been an undercurrent of late in focusing towards unique devices. The current crop of devices show Tunnel FET behaviour in vertical & lateral dimensions, negative differential resistance and electro-optical properties for electron guiding.

The most interesting of these is the Single Electron Transistor (SET). Where the transport mechanism is driven by discrete units of charge carriers tunneling across the device. Unlike a MOSFET which relies upon a continuous flow of charge carriers to function. Applications of SETs range from low power logic, sensors, spintronics to quantum information technology[35].Of these graphene has the most potential in quantum information technology. Thanks to the long decoherence times of carbon. Providing an advantage over the current state of the art [36]. The SET represents a fundamental component in the present quantum computing architectures [37].

Graphene is uniquely situated for use as a SET due to the duality that exists in the charge carriers, unlike normal semiconductors. A graphene transistor can then act as both a single electron transistor and a single hole transistor in one device with the conduction for holes and electrons being equal. Especially since SETs require a variable gate voltage to tune its properties. This means the ambipolar conduction can be utilised to its fullest. Another advantage for graphene SETs is a high on/off ratio is not a key property for a high-performance device. Circumventing a graphene transistors biggest pitfall. Further to this graphene nanoribbons have been shown to act intrinsically as SETs when measured at low temperatures. Recent techniques have demonstrated a working SET at room temperature [38]. The focus of research in graphene SETs now is to improve the performance to match silicon and 2DEG devices, so graphene's superior properties can be demonstrated.

1.4 Outline of Thesis

An ideal graphene logic device that could be created would be a highly repeatable SET. Targeted for low power logic operations that would be compatible with a silicon fabrication method for use in a BOEL process. Enabling graphene to be used in tandem with silicon devices to create 3D stacked devices. This thesis follows the development of progressing towards this goal. Initial progress is made in fabricating wafer-scale graphene devices by developing the quality of the CVD-graphene. CVD-graphene is used to demonstrate a novel process of transferring graphene as the last fabrication step.

The wafer-scale transfer process is used to produce a large array of nanodevices to measure the various divergent behaviour that emerges from the same fabrication process.

The use of an advanced E-beam system is used to carefully control the design parameters that is not as easily achieved by other means. Controlling the dimensions with a higher accuracy than has been seen before for graphene devices.

The thesis follows the format of detailing the current state of the art in literature for the different aspects of graphene in Chapter 2. First by describing the basic properties of graphene. Then the methods of synthesising the graphene sheet and the unique properties of graphene nanodevices. The theory used to analyse the properties of the graphene nanoribbons to extract the energy gaps. Then the theory of SETs is discussed that relates to the observation of Coulomb oscillations in graphene. Lastly the various aspects of fabricating graphene that need to be considered in particular are discussed. Chapter 3 discusses the methodology used to fabricate and characterise the graphene devices. Chapters 4 and 5 detail the experimental results achieved. Chapter 4 covers the development of a transfer-last process for use in integrating graphene with silicon and covers the development of the CVD process needed to produce high-quality devices. Chapter 5 focuses on the electrical characterisation of graphene nanoribbons produced using CVD-graphene on a 90 nm silicon Dioxide, investigating the scaling effects of CVD-graphene. Lastly, the single electron tunneling effects observed in the graphene nanoribbons are discussed to analyse their properties and determine the unique aspects of these SETs. The thesis is finally concluded and future investigations that can take place from the work of this thesis are discussed.

Chapter 2

Literature Review

2.1 Graphene

A 2DM is a one molecular or atomic layer thick; capable of being successful synthesised in the macro or micro scale. Graphene's outstanding electronic properties were first measured in 2004 [1]. At first by isolating from highly ordered pyrolitic graphite. Using Scotch tape to repeatedly peel graphite and then transfer onto a silicon dioxide substrate . This was a groundbreaking discovery at the time due to the misconception that 2DMs were unstable when isolated[39]. This commonly held belief was built upon the basis that once isolated a 2DM would react immediately with its surrounding atmosphere. Due to the large surface area and increasing melting point when approaching a single layer causing it to thermally or chemically decompose or by some other reaction [40]. Although previous observations of graphene have been predicted as far back as 1962 [41] it was not confirmed with experimental evidence fully until 2004.

2.1.1 Structure

Graphene is a 2DM only one atomic layer thick of hexagonal crystalline carbon. This material comes from Graphite, the many-layered "bulk form" commonly found in pencils. Or it can also be considered a macro-scale molecule of fused Benzene rings, further justified by the sp^2 bonds of graphene (the same as benzene). An sp^2 bond is a unique hybridisation of the 2s, $2p_x$ and $2p_y$ electron orbitals to form the bonding between atoms, otherwise know as a Sigma [σ] bond. The bond length of carbons atoms in graphene is 0.142 nm compared to diamond which is 0.154nm and silicon 0.186 nm. The width of the hexagons in graphene is the lattice constant which equals 2.45 Angstroms or 0.246 nm. A single layer of graphene is called a monolayer, two a bilayer, three a trilayer, anything larger than a trilayer is usually called few layer graphene since its properties are the same for increasing layers.

Like silicon there are two main orientations of graphene that exist, referred to as Arm-chair and Zigzag (see figure 2.1). Chirality is the physical phenomena which underpins

the angle of orientation. Zigzag is a θ of 0 degrees and Armchair is 90 degrees and are considered to have a high symmetry. There can exist other orientations that can have some effect on the electronics properties. The main interest is Armchair and zigzag where the role of the edges is important for the spin orbit polarisation such as zigzag edges are expected to have some magnetisation [42].

Figure 2.1: Graphene crystalline structure

2.1.2 Electrical properties

The chemical bonding of carbon atoms in graphene owes to its excellent electron transport properties. The hybrid sp^2bonds allow the $2p_z$ orbital electrons to move freely across the lattice (or pi [π] bonds) to be shared among the atoms. Conduction in this manner means the electrons are ballistic [19]. Ballistic conduction is where electrons can travel large inter-atomic distances without scattering. This is the where the mean free path is greater than length of the material. Ballistic should not be confused with superconduction since the electrons still require a force to drive their movement. The reason for the ballistic electron behaviour is the electrons are mass-less Dirac Fermions (In a typical material the electrons would be described under Schrodinger's equations). Interestingly the electrons can also have wavelike or photon properties due to this property.

In the first paper by K. S. Novoselov and A. K. Geim in "Electric field effect in atomically thin carbon films"[1]. Several electronic properties of graphene are experimentally demonstrated for the first time. The ambipolar behaviour was demonstrated over a large (1 μm) wide ribbon (see figure 2.2). This is shown by the rapid change in resistance under a varying gate voltage with the minimum point often referred to as the Dirac point. At first the Dirac point is quite offset from 0V but this is assumed to be due to water adsorption on the surface affecting its doping. Later verified when the point shifts after annealing.

When investigating the carrier mobility it is found to be 10,000 $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ at room temperature, roughly 7 times greater than silicon. Later work has shown graphene mobility to be capable of approaching 200,000 $cm^2V^{-1}s^{-1}$ in suspended devices [43], with

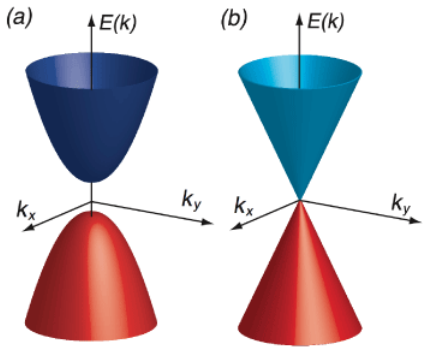

Figure 2.3: Graphene band structure showing the conduction and valance band meeting at the Dirac point in a conical shape (right) Typical semiconductor with parabolic shape and gap (left)

a theoretical limit of $10^6 \mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ [44]. The mean free path is discovered to be ~0.4 μm which is consistent with ballistic conduction. The Shubnikov-de Haas oscillations indicated evidence for quantum hall effect in graphene.

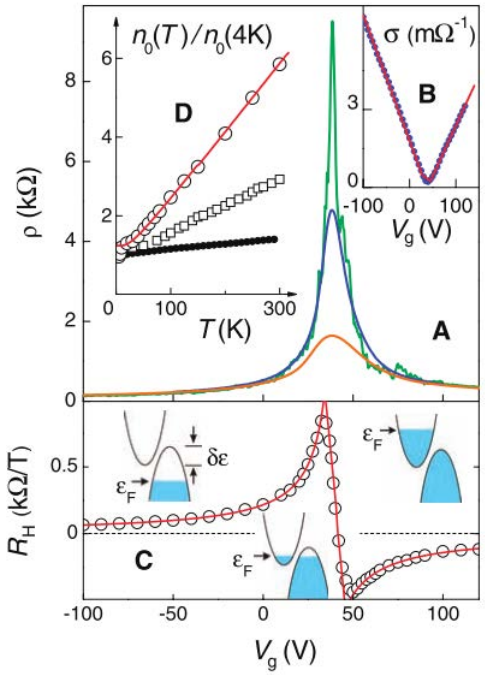

Figure 2.2: Field effect in graphene showing chances in resistance and conductance with changing gate voltage [1]

Despite first characterising graphene as a semimetal with a small band-gap overlap it is later stated to be a zero band-gap material, where the band structure of graphene can be seen in figure 2.3. A transistor is then tested using the silicon substrate as a back-gate to determine a small on/off current ratio of ~30. Although this states it is sufficient for logic devices, it would be more accurate for a bulk graphene device to be suitable for analogue applications. Since an on/off ratio of at least 10^5 is often stated as the most desirable for MOSFETs.

An interesting property of graphene is that the difference in mobility between holes and

electrons is non-existent as discussed theoretically in Wang et al in 2013 [45] and proven in [46] . In fact Lemme et al in 2007 [46] shows that it is possible for the conduction of holes to be greater than electrons, where a lack of high hole mobility semiconductors a problem facing the industry. Another property that has been modeled is the effect of strain, Wang et al [45] shows that the dominant charge carrier can be varied depending on the amount of strain across graphene. Electrons have also been able to maintain a high mobility while under a high electric field, such as a typical field of 70 kVcm^{-1}, which is important for MOSFET applications of graphene [34].

2.1.3 Synthesis

The first point to consider when fabricating graphene devices is the source of the graphene. There 5 popular synthesis methods, each have their own benefits and downsides. This section discusses the merits of each method and which one has been chosen for the majority of the graphene devices fabricated.

2.1.3.1 Mechanical Exfoliation

The first method discovered involved the successive splitting of highly oriented pyrolytic graphite into thinner sheets using sticky tape. After a certain number of times a number of different layers of graphene and some graphite will end up on the substrate. When transferred onto a silicon substrate with a 295nm thick silicon dioxide graphene is visible under an optical microscope. The quality of the graphene is pristine, since it does not have defects leading to the high electron mobilities found in graphene. The issue is that this is not suitable for wafer-scale electronics, the size of individual crystals is rarely larger than $10\mu\mathrm{m}^2$. Another issue is that each chip graphene is deposited onto must be tailored for its specific location, lengthening the design process, or adding difficulty by extending the processing required to place individual graphene flakes to targeted locations.

2.1.3.2 Carbon Nanotube Unzipping

A method for creating nanoribbons with perfectly terminated edges is to unzip or unroll carbon nanotubes [CNTs]. Using Potassium permanganate and sulphuric acid to do this [47]. The main problem with using nanotubes is the same as exfoliated graphene, at first it was not possible to achieve a wafer-scale integration of nanotubes, but IBM research has recently perfectly aligned wafer scale nanotubes [48]. Except in the case of unzipping nanotubes the quality of a nanoribbon does not supersede CNTs in the case of a pure logic device.

2.1.3.3 Silicon Carbide

Silicon carbide [SiC] is a silicon wafer doped with carbon, with a high band-gap. To create graphene on the surface, the carbon is decoupled from the wafer by annealing [21]. The epitaxial growth is achieved by utilising the higher sublimation rate of silicon than carbon. The silicon will leave the sample at sufficiently high temperatures to leave behind excess carbon on the surface which reforms into graphene. The SiC is heated to $1400^{\circ}\mathrm{C}$ in a vacuum in a sublimation chamber.

To create nanoribbons the wafer can be pre-etched and then decoupled leaving graphene along the edge facet. This method can be used for wafer scale growth of transistors, so far demonstrated densities to be 40,000 per cm^2 of 40 nm wide nanoribbons [49]. More recently the highest possible mobilities recorded for graphene have been achieved with silicon carbide of 7,000,000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ [50], this is better than theoretical limits for graphene showing a complete ballistic conduction of a 40nm wide nanoribbon. But, it is an expensive option to produce high quality devices for a scalable method of bottom up graphene synthesis.

2.1.3.4 Reduced Graphene Oxide

A unique and largely scalable process for producing graphene is the reduction of graphene oxide [rGO]. As with silicon, graphene can be readily oxidised in air at high temperature or by oxidising agents . The most popular method of producing graphene oxide [GO] is manufactured by a modified Hummers method [51] using Potassium permanganate, sulphuric and phosphoric acid to obtain GO from graphite. To turn it back into graphene vacuum annealing at $1000^{\circ}\mathrm{C}$ can be done. graphene oxide itself could also be used as a dielectric layer for electronic devices. The reduction process is exploited in all-graphene devices by using a laser reduction method to create isolated graphene circuits, due to isolated heating from the laser and direct writable methods.

The benefit of GO is it can be produced more reliably and much cheaper than any CVD methods. With solution processing using oxidising agents it is a very quick process and thanks to its hydrophillic nature meaning it can be reliably dispersed in water and dispensed easily like ink. The downside to rGO is the electronic quality is quite poor, only 365 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ because of the oxygen vacancies left behind creating vast amounts of defects ,although 5000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ has been claimed to be possible with ionic screening [51]. This low conductivity makes it unsuitable for high quality electronic grade graphene transistors. But it may have its use in depositing interconnects for VLSI ICs, all-graphene contacts, flexible/printed electronics and thin-film transistors.

2.1.3.5 CVD-graphene

The most popular large-area graphene synthesis method is currently chemical vapour deposition [CVD]. It is a tool routinely used in semiconductor fabrication for dielectrics

and amorphous or polysilicon semiconductors. To create graphene, methane is heated up over a copper substrate to grow graphene and then transfer to a target substrate by etching the copper away [52]. This is fast and cheap with a scalable process that can create graphene over 100m rolls on a plastic substrate [53]. The most common method to create graphene devices is from CVD-graphene grown on copper foil. Unfortunately the copper foil is not formed of a single grain so the graphene formed is polycrystalline. Usually graphene is formed in a Low Pressure CVD [LPCVD] system but Plasma Enhanced CVD [PECVD] has been used to grown graphene directly on a silicon wafer to form nanocrystalline graphite or by using copper deposited onto the wafer.

The substrate is coated with a resist to protect the graphene layer, copper substrate is etched in acid and transferred onto a silicon wafer with an oxide (same as exfoliated graphene method). By lifting the silicon underneath the graphene/resist stack that is floating on top of the solution and leaving to dry produces a large wafer scale area of graphene on silicon dioxide. The mobilities reported so far have shown CVD-graphene to be the same quality as exfoliated graphene, with the highest reported mobility above 10000 $\mathrm{cm^2V^{-1}s^{-1}}$so far for 5% of devices fabricated out of 26000 devices, a overall yield of 74% and an average mobility of 2113 $\mathrm{cm^2V^{-1}s^{-1}}$, proving the versatility of CVD-graphene [54].

The CVD-graphene is like polycrystalline silicon, where a number of different grains (or orientations) of graphene join together in a homogenous layer, it forms a grain boundary. The boundaries where the grains meet are defects in their own right but do also have some unique properties. In “An extended defect in graphene as a metallic wire” [55], the grain boundaries are first investigated on graphene grown on nickel. Two different lattice orientations can be formed with both being stable due to a matching binding energy. When the two meet the grain boundary causes an one dimensional defect to occur. This meeting of different adsorption geometries caused by delamination of the graphene on nickel leaves a line defect of 5&8 rings which creates a distinct density of states that exhibits metallic properties.

Later work by Tsen et al. in 2012 [56] shows the effect of grain boundaries on the charge transport properties of graphene ribbons. If there is a grain boundary bisecting the ribbon its minimum resistance does not vary too much but the maximum at the Dirac point greatly increases. It also demonstrates that the typical grain boundary structure of CVD-graphene does not decrease the performance provided the grain boundaries are well stitched together. Giving electron mobilities of 25,000 $\mathrm{cm^2V^{-1}s^{-1}}$with a sheet resistance of 1 k$\Omega/\square$. If the grains are larger the mobility and performance of the graphene is much more affected.

There are many problems with traditional CVD grown graphene on copper, beyond the polycrystallinity. The process of transferring across causes wrinkles and bumps in the sheet and the graphene is usually contaminated with organics from the support polymer, considerable effort has been to remove these problems from graphene.

The limitations of CVD-graphene are slowly beginning to disappear, with a recent reported single crystalline graphene grown on a hydrogen-terminated germanium wafer.

The germanium wafer overcomes the issues related to growing graphene on silicon as it has a much lower carbon solubility. When trying to producing graphene on silicon it is more likely to form a silicon carbide wafer. This means the graphene does not bond with the germanium and is disassociated from the wafer and can be transferred by depositing gold onto the graphene with thermal release tape providing the needed support for the transfer. The uniqueness of this method is graphene can be patterned in two steps by first etching the gold into device structure and in the second etch step removing the gold from the graphene channel using a standard gold etchant. This produced graphene devices of a reported average 7250 +/- $\mathrm{cm^2V^{-1}s^{-1}}$ and a maximum of 10,620 $\mathrm{cm^2V^{-1}s^{-1}}$ [33]. Similar to the best devices on silicon but with a much better average mobility. The prospects of CVD-graphene for future electronic devices is looking very favourable.

2.2 Graphene nanoribbon devices

When considering the use of graphene in electronic devices the limitation of a band gap prevents its use as a direct replacement material for silicon in MOSFETs. Although, it is the zero band gap in graphene that causes most of its unique electrical properties. By only considering graphene's use as a bulk material, most of the potential uses as a transistor is limited to radio frequency or other analogue applications. However, the advent of nanofabrication techniques and exploitation of graphene's unique properties enables alternative methods for creating a suitable more than Moore logic device.

2.2.1 Nanoribbons

To overcome the deficit of a band gap graphene can be patterned into nanometre sized feature called a nanoribbon, where a gap in the Fermi energy is created by the quantum confinement of electrons in the nanoribbon. In principle this gap is dependent on the number of atoms in the nanoribbon and whether it is zigzag or armchair orientated according to theory. Contrary to the predicted behaviour of graphene nanoribbons though, the experimental results produced remarkably different properties. In actuality the edge roughness of the ribbons causes an increase in the Fermi energy gap due to an increase in disorder. The influence of the disorder in the edges is an important characteristic of graphene nanoribbons and is considered later in 2.5.1.

2.2.2 First experimental results

The first observation of a graphene nanoribbon was by Han et. al in 2007 [57], where nanoribbons were created from exfoliated graphene and a HSQ e-beam resist left on for encapsulation. The devices demonstrated a suppressed region of conduction around the Dirac point, see figure 2.4. At first this was attributed to be due to a band gap but was corrected in later works to be a Fermi energy gap [2, 58, 3]. These nanoribbon devices

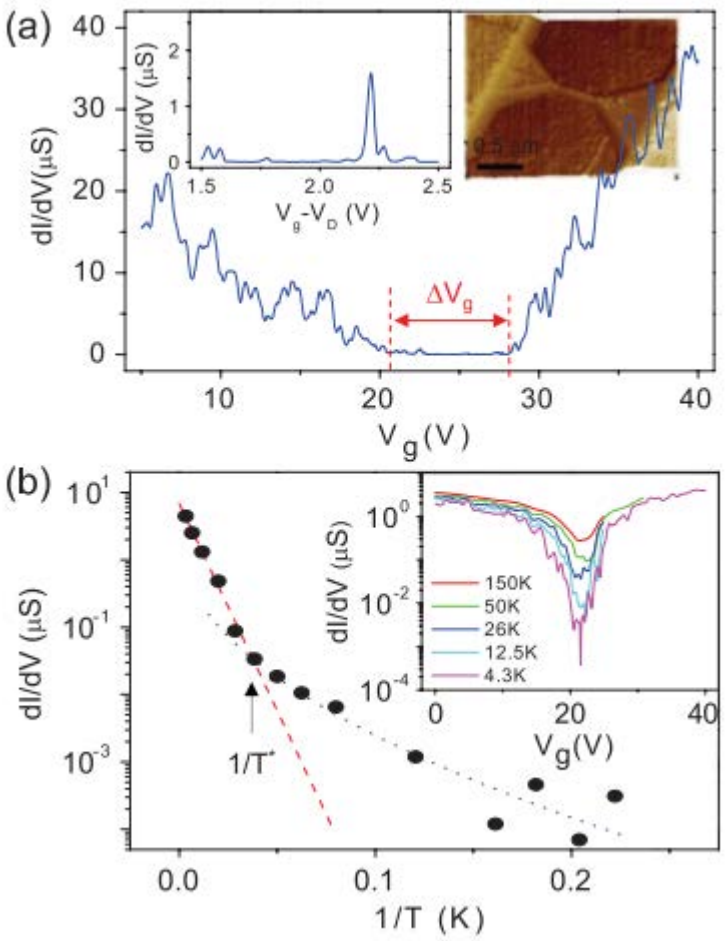

Figure 2.4: Typical characteristics of a graphene nanoribbon. In a) the ambipolar conduction is now suppressed to yield a region called the transport gap. While b) shows the change in the minimum conductance versus temperature. Taken from reference[2]

showed no dependency on the nanoribbon orientation and a larger than expected band gap.

At first the results were only attributed to the influence of the roughness in the edges. However, as was discussed earlier, graphene's intrinsic doping can be modified due to various surface interactions. But this does not create a uniform distribution of doping across the graphene sheet and instead creates electron-hole puddles or localised charges across the sheet.

When patterned into nanoribbons the effect of the localised charges becomes more pronounced when combined with the edge defects, leading to the main transport mechanism of electrons through the nanoribbon to be dominated by electrons hopping between localized states in the channel. This means an intrinsic property of nanoribbon transistors is the tunneling through the localised states act as individual quantum dots, leading to nanoribbons acting as single electron transistors at low temperatures and Coulomb blockade being a significant property of the nanoribbons transport.

So far the best devices have been produced by creating nanoribbons on silicon carbide [49]. These have created nanoribbons with ballistic conduction and smooth edges, demon-

strated by the lack of a transport gap dominated property at low temperature. Other methods of producing high quality nanoribbons is from unzipping carbon nanotubes [59]. Beyond this more recent methods for producing nanoribbons have been from anisotropic etching of the zigzag edge in graphene using hydrogen plasma, though so far these have been used to create graphene nanomesh devices [60, 61].

Currently the investigations into CVD-graphene nanoribbons has been limited with a single key paper that follows the same methodology as Han et al. using HSQ to pattern a 12 nm wide by 1 um long nanoribbon [62]. Their investigation did not show nanoribbon properties much different to the previously obtained results for a graphene nanoribbon.

2.2.3 Predicting nanoribbon properties

The properties of graphene nanoribbons are defined by the generation of a suppressed current region below the value of the quantum conductance, $\mathrm{G_q} = \frac{4\mathrm{e}^2}{\mathrm{h}}$. The size of this flat region of current called the transport gap is determined by the gap in the Fermi energy. At first this was thought to be a direct results of a pure energy gap in the nanoribbon but was later confirmed to be a contribution of the confinement energy and a disorder potential [3, 58].

In "Electron transport in disordered graphene nanoribbons" nanoribbons are fabricated from exfoliated graphene and a HSQ resist to show the width dependent properties of graphene nanoribbons in relation to the size of the transport gap [2]. The size of this transport gap is then extracted to find the size of the Fermi energy gap (equation 2.1) and figure 2.5, for a plot of the different energy gaps for a nanoribbon of increasing width. The Fermi energy gap is also determined by the thickness of the gate capacitance, which is calculated as the capacitance per unit area of the oxide thickness, using the parallel plate capacitance method. The added difference to this is an additional factor to account for the fringe fields from the gate, which increase the total gate capacitance. This factor was verified in “Characterizing wave functions in graphene nanodevices” [63], where the magnetic field measurements of the graphene devices confirmed the factor to be 1.5. So this fringe field factor is used in the calculation of gate capacitance for the graphene nanoribbons.

$$\Delta \mathrm{E_F} = \hbar \upsilon_\mathrm{F} \sqrt{\frac{2\pi \mathrm{C_g} \Delta \mathrm{V_{tg}}}{|\mathrm{e}|}} \tag{2.1}$$

Here $\Delta \mathrm{E_F}$ is the Fermi energy gap, $\hbar$ is the reduced Plank's constant, υ_F is the Fermi velocity of graphene,$\mathrm{C_g}$ is the capacitance per unit area (equation 2.2), e is the charge of an electron and $\Delta \mathrm{V_t g}$ is the size of the transport gap.

$$\mathrm{C_g}(\mathrm{F}/\mu\mathrm{m}^2) = 1.5(\frac{\epsilon_0 \epsilon_\mathrm{ox}}{\mathrm{t_{ox}}}) \tag{2.2}$$

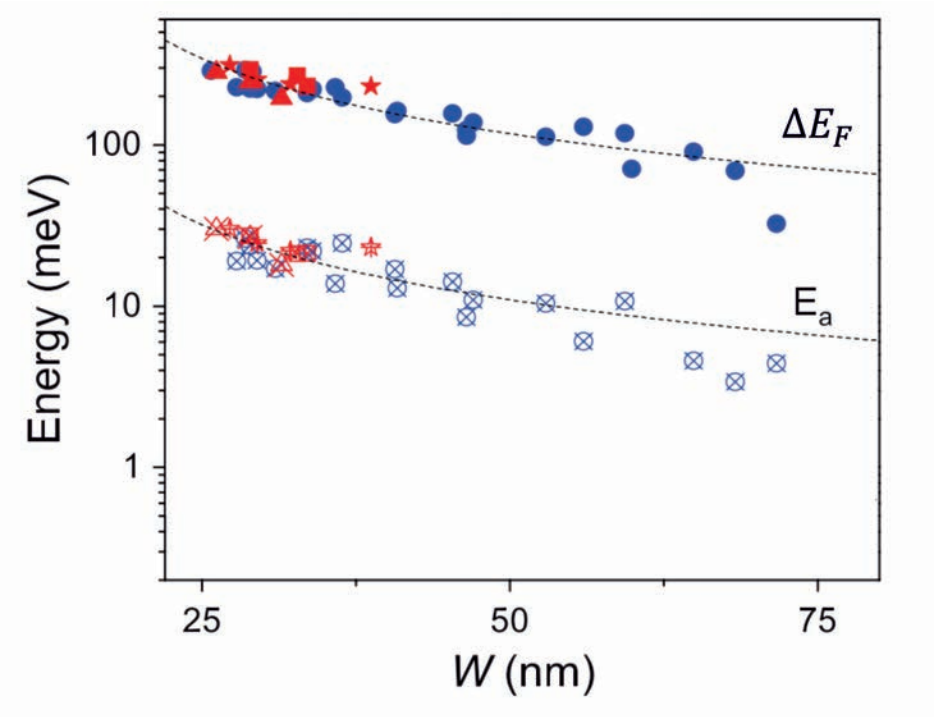

Figure 2.5: Plot of nanoribbon width versus the change in energy for the Fermi energy gap and activation energy of graphene nanoribbons. Taken from [2]

When combined with Ensslin's groups work on the determining the Fermi energy gap from the nanoribbon width allows the energy gap to be determined from the electrical properties, or the transport gap can be predicted from the designed ribbon width. The gap in the Fermi energy of a graphene nanoribbon was determined to be caused by confinement energy and a disorder potential, where the disorder potential is calculated from the charge carrier density fluctuation in an exfoliated graphene nanoribbon, equation 2.4 [64]. The combination of these two energies causes the measured transport gap. The possible effect of the disordered potential fluctuations and how it causes quantum dots to form in the nanoribbon due to localized states is show in figure 2.6. This theory has been verified in the "Transport through graphene quantum dots" review article [11], where the Fermi energy gaps of nanoribbons of different widths were plotted to prove the relation between the confinement energy and a disorder potential causing an increase in the measured Fermi energy of the graphene nanoribbons.

$$\Delta \mathrm{E_F} = \Delta \mathrm{E_{con}} + \Delta_{\mathrm{dis}} \tag{2.3}$$

Where $\Delta \mathrm{E_F}$ is the Fermi energy gap again, $\Delta \mathrm{E_{con}}$ is the confinement energy, Δ_{dis} is the disorder potential and in the equation below $\Delta_{\mathrm{n}}$is the carrier density fluctuation. For an exfoliated graphene nanoribbon the $\Delta_{\mathrm{n}} = 2\,x\,10^{-15}\ \mathrm{m}^{-2}$. Then $\Delta_{\mathrm{dis}} = 0.1043$ eV.

$$\Delta_{\mathrm{dis}} = \hbar v_{\mathrm{F}} \sqrt{4\pi \Delta_{\mathrm{n}}} \tag{2.4}$$

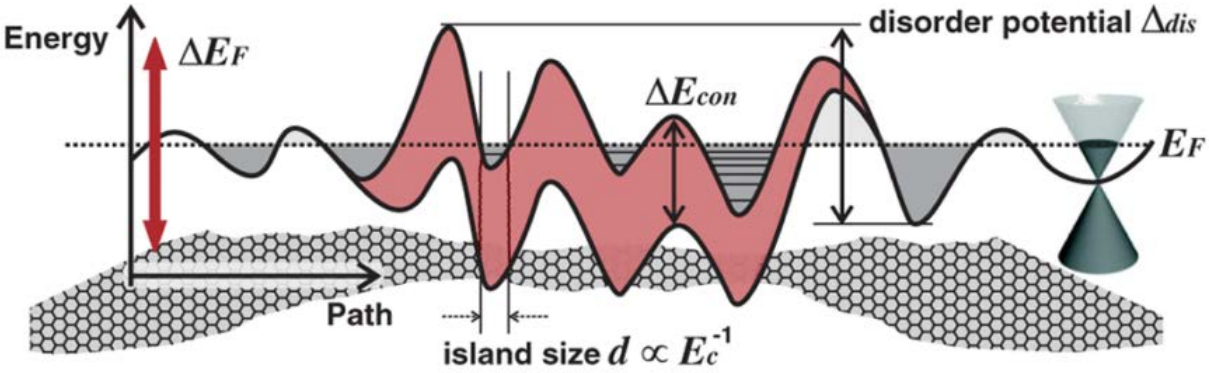

Figure 2.6: Example diagram of how the disorder potential and confinement energy affect the overall energy across a nanoribbon [3]

The calculation of graphene's confinement energy is dependent on the number of atoms and orientation of the ribbon. The first theoretical results determined with tight-binding calculations that all zigzag nanoribbons are metallic and armchair ribbons vary depending on the number of atoms[65]. In later calculations using the spin-moment of the edges this was disproven and shown that all nanoribbons are semiconducting with armchair edges showing the smallest confinement energy. Colloquially the relation between the width and confinement energy can be described as a α/W relation with $\alpha = 2\hbar v_\mathrm{F}$ or $2\hbar v_\mathrm{F}/3$ if it is either armchair or any other relation. This summation of the confinement energy is a simplification of the tight binding calculation, but does generally hold true for the current nanoribbon experiments, where typically the values expected for the nanoribbons are found using the minimum possible confinement energy. The confinement energies for nanoribbons of widths from 100 nm down to 5 nm are plotted in figure 2.7 for the different values of α. α_1 gives the maximum possible confinement energy and α_2 the minimum energy possible.

$$E_{con} = \frac{\alpha}{W} \tag{2.5}$$

$$\alpha_1 = 2\pi\hbar v_\mathrm{F} \text{ or } \alpha_2 = \tfrac{2\pi\hbar v_\mathrm{F}}{3}$$

When determining the transport gap it is typically based on intuition rather than an extraction by calculating the gap. This means the results can be rather subjective based on the interpretation. Especially when the electron transport is complicated the inclusion of Coulomb oscillations in the $\mathrm{I_d}/\mathrm{V_g}$ curves.

The single electron tunneling through nanoribbons can also be used to determine the nanoribbon's width depending on the size of the Coulomb blockade or energy gap in the drain voltage when the data is plotted as a stability diagram. In some circumstances the size of the $\mathrm{V_d}$ gap is not the result of the single electron tunneling as the tunneling

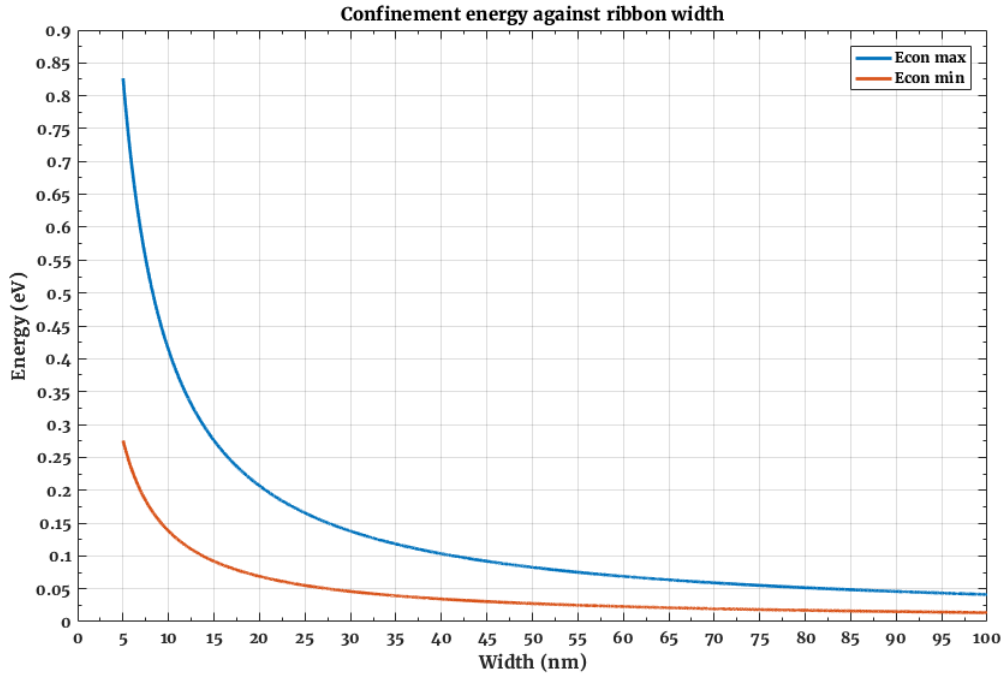

Figure 2.7: Confinement energy for increasing nanoribbon width with different factors of α

is observed within the transport gap due to the difference in energy scales. The cumulative effect of Coulomb blockade through multiple quantum dots had been theoretically investigated by Castro Neto's group and determined the relation between the width of the nanoribbon and the energy gap in the drain voltage sweep. This has been simplified into equation 2.6 using two fitting factors of $\beta = 0.001$ meV $\mathrm{nm}^{-}1$ and $\mathrm{C} = 0.023\mathrm{nm}^{-1}$ and has been shown in their work to fit accurately to the experimental results so far [66].

$$\mathrm{E_g(W)}^{-1} = \beta \mathrm{We}^{\mathrm{CW}} \tag{2.6}$$

2.2.4 Nanoribbon device structures

The semimetal properties of graphene can be utilized for fabricating nanoribbons with integrated wires, such as source, drain and gate electrodes from graphene. These create all-graphene devices where a transistor can be fabricated solely with graphene. From a manufacturing perspective this reduces cost of materials with some routing being achievable on the same plane.

There is less of an effect from Schottky barriers since there is no metal-semiconductor interface on the nanoscale. Conventional silicon devices are impacted by this phenomena in a detrimental way as it affects source and drain contacts of a transistor, with a greater effect at smaller scales. Graphene will not suffer from this effect as there is no lattice or material mismatch between the source and drain contacts, so there is nothing to obstruct the flow of electrons in turn providing a faster device.

2.2.4.1 Wide-narrow-Wide Structure

The first building block to an all-graphene device is to use the wire interconnects for the source and drain in figure (2.8a), with the semiconducting channel isolated to the nanoribbon structure, creating a Wide-narrow-Wide [WnW] device. This provides advantages over silicon which requires metal connections in a 3-dimensional manner (2.8b).

WnW have been used since the first GNR transistor [57] to reduce the effect of Schottky Barriers and is fairly standard practice in fabricating monolithic graphene devices. In Unluer et al in 2011 [4] WnW are modeled with tight binding methods. A 0.74 nm channel with a E_g of 1 eV and a wide source and drain of only 4.18 nm with a E_g of 13.47 meV. Extended Huckel Theory [EHT] is used to find the band-gap as tight binding states it is metallic. This is true in a sense, since at room temperature the energy of k_BT= 25 meV so the wide structure would be conducting regardless. To get a better gate control the top gate should be larger than the channel material because it provides a much better gate modulation. The extracted parameters from the WnW device compared to a dual gated MOSFET shows a higher on current and smaller SS.

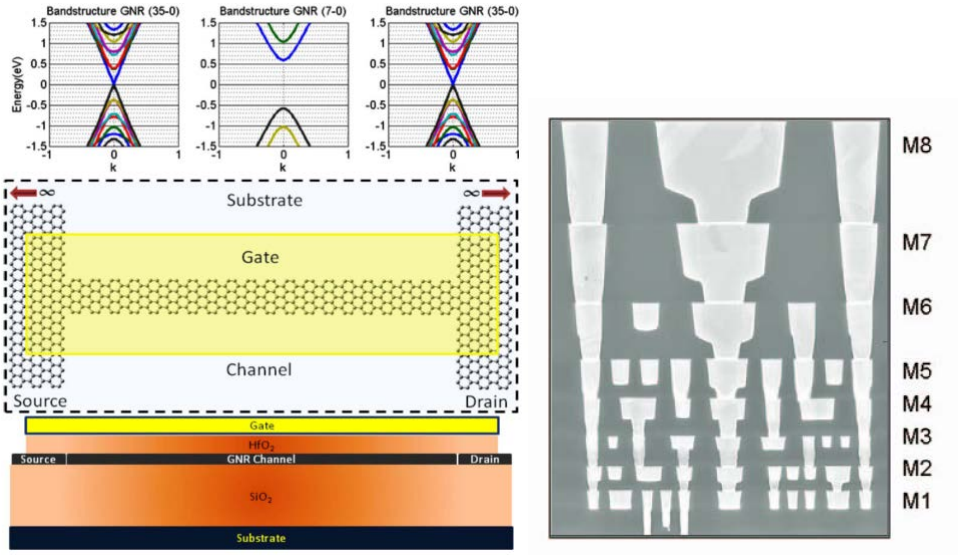

Figure 2.8: a) WnW graphene transistor [4] b) Typical silicon CMOS. [5] Demonstrating the differences in how interconnects can be used as an integral part of the graphene structure without the need to use smaller M1 or M2 layers. Which should provide a lower contact resistance as the area will be greater the higher the metal layer in b is used to contact the graphene layer.

2.2.4.2 Side Gating

When fabricating graphene transistors it is necessary to isolate the transport channel from the rest of the material. The material leftover can be used as a gate without needing a dielectric to insulate the device or depositing metal on top. Side gates have been routinely used in single electron devices so it stands to reason that could be used in standard FETs.

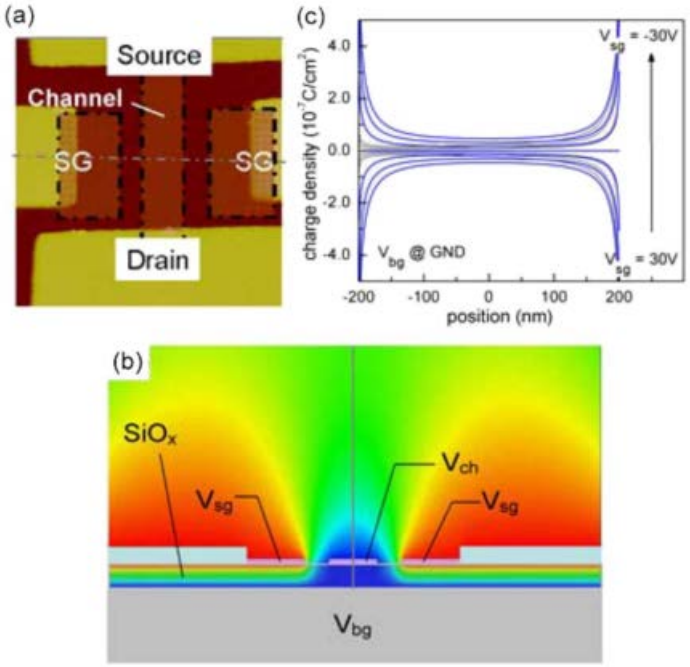

Figure 2.9: a) Side gating device b) Simulated electrostatic potentials at 30V c) Charge density profile of symmetric gating scheme [6]

In Chen et al in 2012 [6] a side gate is first modeled for the electrostatic potentials that affect a 400 nm wide channel and 200 nm gap between channel and side gates. As seen in figure 2.9 this is sufficient for channel modulation when both side gates are used to modulate the channel. The efficiency of the side gate is determined to be the same for both mono and bilayer graphene. If the side gate is used with only one gate on, it is less efficient by ~40% due to the induction of charge carriers being much less. Next the efficiency of side gating is compared to top gating for a bilayer and is found to be equally as effective. From this the simulation are extrapolated for thinner channels and smaller gap distances, it shows the efficiency increases as the device size decreases.

The issue with this is the experiments were conducted at 5K so a room temperature experiment needs to be conducted to determine the extent of electron tunneling that might occur, especially since there is no dielectric barrier to overcome. The ambipolar behaviour has also been demonstrated for side gates made from graphene [67]. The side gated devices fabricated on SiC were 60-125nm wide Hall bars and found that the centre of the nanoribbons were n-doped from scanning tunneling microscopy, while the edges were p-doped and could be actively tuned by the side gates. More work will need to be done for the side gates to be a more desirable method for tuning the switching and carrier concentration in graphene nanoribbons.

2.2.4.3 Suspended graphene nanoribbon

Some of the most exceptional graphene devices have been fabricated by the suspension of graphene. This is thanks to the reducing scattering points and other fabrication

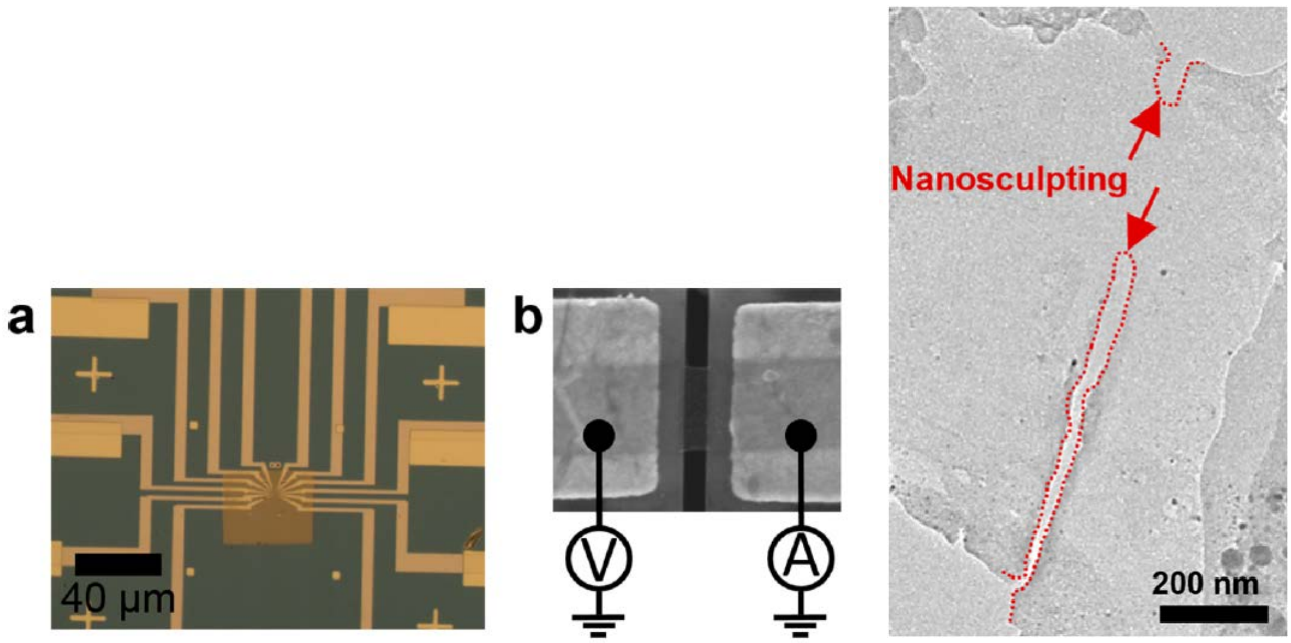

Figure 2.10: Image from visualization of edge defects in graphene. Left: A) Device structure on nitride membrane, B) graphene suspended on metal contacts over a slit in the membrane. Right: Image of STEM while sculpting nanoribbon. Taken from reference [7]

issues that arise from suspending graphene. Some of the best transport mobilities were first demonstrated with suspended graphene (200,000 $\mathrm{cm^2V^{-1}s^{-1}}$). The two interesting types of devices have been for the Scanning Transmission Electron Microscopy analysis of graphene's structure [7] and graphene suspended over metal gates to show ballistic interference patterns [68]. The STEM devices have shown graphene suspended over a 150 nm wide slit in a silicon nitride membrane, with CVD-graphene transferred onto the Cr/Au contacts. After patterning down to a 500 nm wide nanoribbon, graphene is carved using the STEM beam to produce 0.7 nm wide GNRs and measured the resistance with 2 probes showing a value approaching $300\mathrm{k}\Omega$ for a 1.3 nm wide nanoribbon. The physical sculpting of the device is shown in figure 2.10. This work showed a scaled decrease in conductance proportional to the decreasing width.

2.3 Graphene Single Electron Devices

2.3.1 Single electron transistors

If there is a device that best demonstrates the fundamental impact and exploitation of quantum mechanics, it would be the single electron transistor [SET]. It was first conceived by Averin and Likharev in 1985 [69] when considering electron tunneling effects of miniaturizing Josephson junctions (two metals separated by a dielectric barrier). The tunnel barrier forces the electrons into tunneling discretely when a voltage is applied and the temperature is sufficiently low enough the thermal energy is not violated. This creates the equivalent of a resistor and capacitor in parallel. By creating an isolated

island between two barriers so electrons must tunnel in and out of the charging island. Combining with a gate electrode and dielectric as a FET typically would creates a single electron transistor.

2.3.2 Theory of SETs

The first SETs were fabricated from Metal/Oxide stacks, which is the best way to begin in describing the transport mechanism of SETs. In a metal/oxide SET the only electron transport possible is caused by tunneling through the dielectric barrier. If a simple Metal/Oxide/Metal device with only 1 tunneling barrier is considered, at high temperature the electrons have enough energy to tunnel through the barriers unimpeded, meaning the device acts no different to a resistor, with a linear increase in current with increasing applied voltage. However, when the temperature is reduced enough that the thermal energy is no longer strong enough to enable electrons to tunnel through the barriers immediately, an electron must then obtain the energy needed to tunnel across the junction by a change in the electrostatic potential .

$$\mathrm{E_c} \gg \mathrm{k_B T} \tag{2.7}$$

$$\mathrm{k_B T} = 26\mathrm{meV} \text{ at } 300\mathrm{K} \text{ and } \mathrm{k_B T} = 0.086\mathrm{meV} \text{ at } 1\mathrm{K}$$

At this stage the I/V characteristics manifest as a non-linear behaviour, where at low applied voltages the device does not have enough electrostatic potential to overcome the barriers. Creating a central region in the I/V diagram where there is no current flow, see figure 2.11. This region of no current is called the Coulomb gap and is due to phenomena described as Coulomb blockade, because the Coulomb charges are blocked from being transported. The characteristic of blocked conduction is due to the discrete conduction of electrons through the barriers. In the single tunnel junction device, the critical value required for electrons is related to the charge of the electron divided by the capacitance of the junction. This creates the criteria that the current is suppressed when the voltage is $-\frac{\mathrm{e}}{2\mathrm{C}} < \mathrm{V} < \frac{\mathrm{e}}{2\mathrm{C}}$.

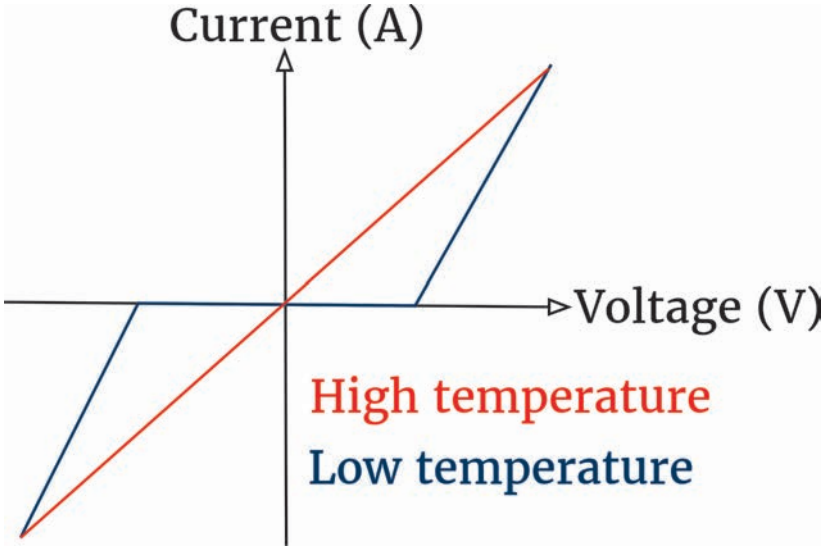

Figure 2.11: Coulomb blockade of single tunnel junction device at low and high temperature

Currently the description of single tunnel barrier is sufficient for understanding the energy requirements for successful electron tunneling. But in actuality the observation of a working device requires the resistance of the metal contacts to be greater than the quantum resistance ($R_Q = \frac{\hbar}{e^2} = 26k\Omega$). As seen in Chapter 2 an SET has two tunnel barriers with an island in between that has a discrete number of electrons occupying the permitted states. This means the charging energy of the island is determined by the electron charge and capacitance of the island or the sum of the barrier capacitances.

The charging energy can be obtained using self-consistent calculations to find the total capacitance of the charging island, but this is computationally extensive. Instead an upper limit of the charging energy is found by calculating the self-capacitance of the island dimensions, where in reality this value would be much lower due to the contributions from the material it and the islands interactions with that material [70].

$$C_{island} = 8\epsilon_0\epsilon_{ox}R \tag{2.8}$$

Where R is the radius of the island.

$$E_c = \frac{e^2}{2C_{island}} \tag{2.9}$$

Since electrons are acting as discrete units they also carry a discrete amount of charge. As an electron tunnels into the island the charge increases. So the energy required for additional electrons to tunnel increases due to the Pauli exclusion principle. An additional electron cannot tunnel into the island until either the first electron tunnels off the island, or the electrostatic potential increases enough for another electron to occupy an additional energy level in the island.

The change in voltage with respect to the charge is equivalent to the formation of a capacitor, meaning the capacitance of the island can be calculated from these properties. This leads to an equivalent circuit (see figure 2.12) for single electron tunneling to be made from an associated resistor and capacitor in parallel for the electrons to tunnel into the island, plus another to tunnel out of the island. If the capacitances of the barrier in and the barrier out are added this gives the total capacitance of the island.

Since electrons are moving into and out of the island and it is related to the charging of the island, colloquially this is called the charging island. The calculations of the change in electrostatic potential show that the charge and capacitance leads to a calculation of the charging energy of the island, whereby the charging must be greater than the thermal energy for single electron tunneling to be possible.

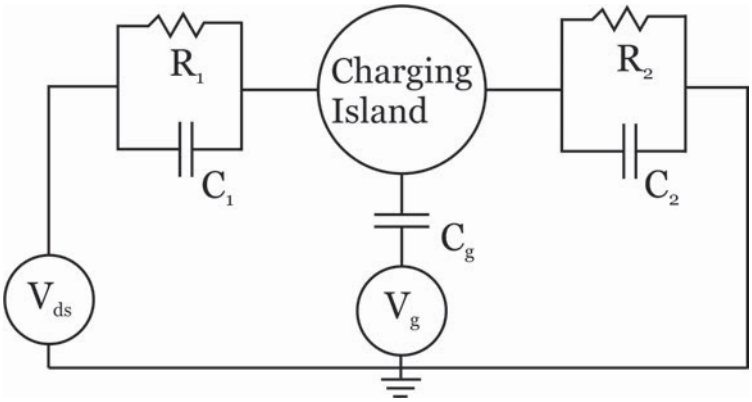

Figure 2.12: Equivalent circuit for an SET, where the tunnel barriers are a resistance and capacitance in parallel with a separate gate capacitance formed by a larger dielectric connected to the charging island.

So far only a device with two terminals has been considered. This does not provide much use beyond acting as a non-linear resistor at low temperature. The introduction of a gate electrode, which, has a much thicker dielectric than the tunnel barrier, so the dominant transport is through the double barriers and not into or out of the gate electrode. Now the device is a single electron transistor and so additional behaviour distinctly different to a normal transistor can be observed. When a gate voltage is applied to the SET the barrier energy is reduced removing the Coulomb blockade. If the gate voltage lines up with an energy level within the charging island an electron is permitted to travel through. This is demonstrated as a sharp peak at regular intervals in the Id/Vg graph. The regular peak shape for this type of electron transport is called the Coulomb oscillation and is plotted in figure 2.13 using a Matlab implementation of the CAMSET (or Master equation) simulation method to produce the Coulomb oscillations from the ideal transport properties of an SET [26].

The charging energy can be determined using the island capacitance or from the sum of the SET capacitances. It is not usually possible to predict the charging energy using C_Σ since the tunnel barrier capacitances can be difficult to estimate, which is why in graphene devices the estimation using the island capacitance is often used.

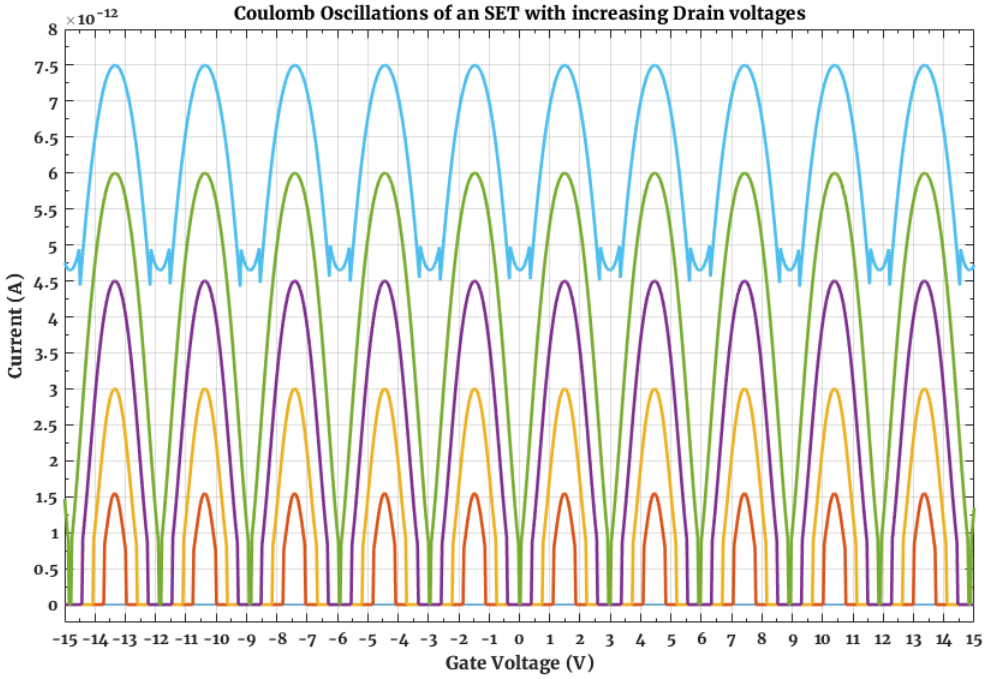

Figure 2.13: Id/Vg graph for a typical SET with increasing Vd, created using a Matlab implementation of a CAMSET simulation. Drain voltage varies from 5 to 25mV in 5mV steps.

$$C_{\Sigma} = C_1 + C_2 + C_g \tag{2.10}$$

$$E_c = \frac{e^2}{2C_{\Sigma}} \tag{2.11}$$

Additionally, the gate capacitance can be used to estimate the peak to peak distance (ΔV_g) in the Coulomb oscillation graphs or extracted from the graph. This is due to the permitted energy levels having an equal spacing. So the peak to peak distance can be calculated from,

$$\Delta V_g \approx \frac{e}{C_g} \tag{2.12}$$

In the energy diagram there is a gap caused by the charging energy and the energy levels of the quantum dot. As shown by Kouwenhoven [70] the spacing between energy levels can be calculated from the electron wave function, where depending on the dimensionality of the quantum dot, the relation between the spacing and the number of charge carriers varies. For a 1D dot the spacing between levels increases with N, while for a 2D it remains constant and for a 3D the spacing decreases with increasing N.

$$E_{n_x,n_y,n_z} = \frac{h^2\pi^2}{2m^*}\left(\frac{{n_x}^2}{{L_x}^2} + \frac{{n_y}^2}{{L_y}^2} + \frac{{n_z}^2}{{L_z}^2}\right) \tag{2.13}$$

$$\Delta E_s = (\frac{n}{4})\frac{h^2\pi^2}{2m^*L^2} \tag{2.14}$$

By introducing the consideration of the energy level spacing the addition energy of the quantum dot SET is now a combination of the charging energy and the energy level spacing, whereas the peak to peak distance in the Coulomb oscillation is now related to the gate capacitance, total capacitance and energy level spacing.

$$E_a(n) = \Delta E_S + \frac{e^2}{C_\Sigma} \tag{2.15}$$

$$\Delta V_g = \frac{C_\Sigma}{eC_g}(\Delta E_S + \frac{e^2}{C_\Sigma}) \tag{2.16}$$

Typically, the effect energy level spacing has on a SET is for there to be a measured aperiodicity in the Coulomb oscillations peak to peak distance. For there to be a direct observation the quantum dot has to be small enough that only a few electrons are active, although the effect of energy level spacing manifests as the broadening of a single peak into multiple peaks as the V_{sd} increases. The distance between the sub peaks relates to the energy level spacing. Additionally, the measurement of an SET under a magnetic field can reveal more information about the electronic states [70].

2.3.3 Graphene single electron transistors

Graphene SETs are fabricated in two methods by patterning into a quantum dot with a quantum point contact either side acting as tunnel barriers. A graphene device can also act as a SET intrinsically due to electron-hole puddles in the graphene sheet. When patterned into a nanoribbon the electron-hole puddles become localised states acting as a series of quantum dots, with the width of ribbon affecting the size of the localised states [71]. Once below 100 nm it can be considered a nanoribbon and the single electron tunneling properties can be observed at low temperatures. The properties of a typical nanoribbon SET are shown in figure 2.14.

Even without exploiting the intrinsic localised states in a nanoribbon SET properties can be seen by unzipping carbon nanotubes, showing possible spin states from the zigzag edge shown by alternate splits in the Coulomb oscillations [9], which is shown in figure 2.15. The stability diagram shows a more regular distribution of Coulomb diamonds across the V_g sweep, while the diamonds widths and height vary outside the central diamond with Kondo effects visible in this device. The height of diamonds varies in an odd-even characteristic, slowly decreasing with increasing number of tunneling events.

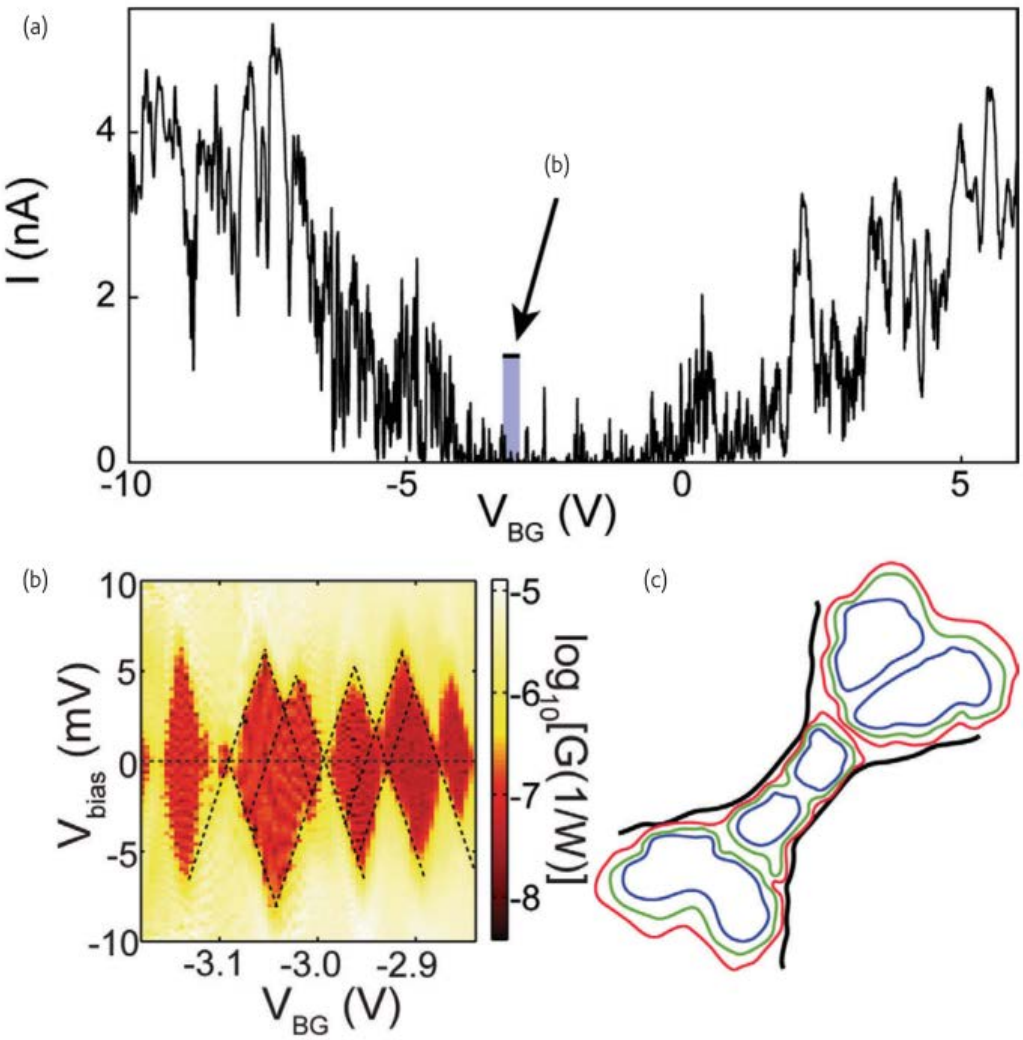

Figure 2.14: Typical characteristics of a nanoribbon SET. a) The Id/Vg curve of the device showing the Coulomb oscillations on top of the ambipolar conduction curve, where the peaks are visible inside and outside the transport gap. b) Stability diagram of the Coulomb diamonds from the zoom in section of the few peaks in a. c) Schematic diagram of the configuration of localised states causing multiple dots to form within the nanoribbon. [8]

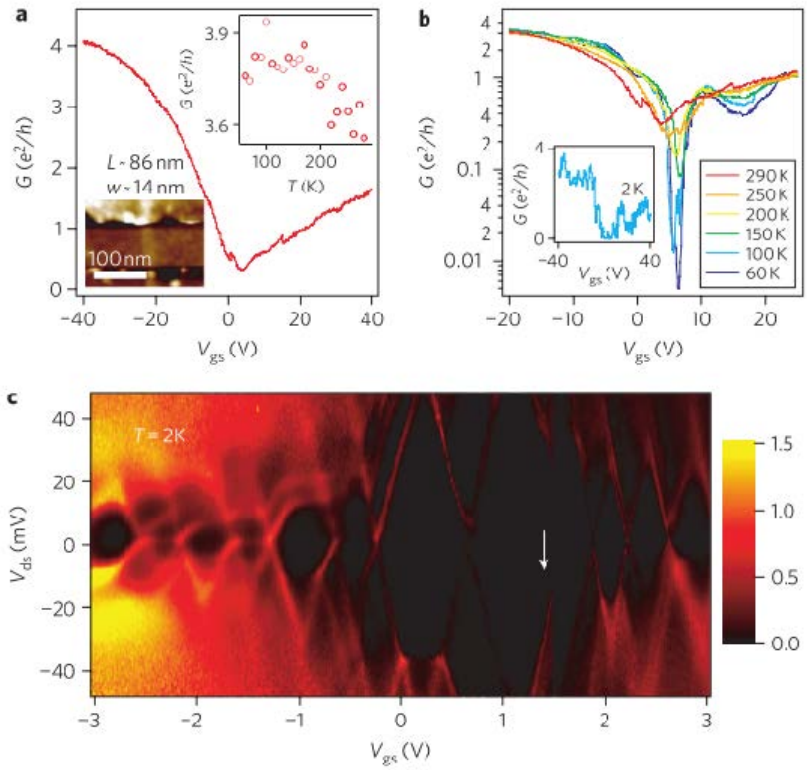

Figure 2.15: Electron transport measurements of an unzipped carbon nanotube[9]

The single electron tunneling is an intrinsic property of graphene nanoribbons that can be exploited to create tuneable SETs [72]. So far graphene devices have demonstrated a mix of SET characteristics depending on the device architecture. With many characteristics emerging from the same device architecture with little difference between their design to account for the different characteristics observed. Currently the most robust method for fabricating graphene SET is from forming tunnel barriers by two quantum point contacts (QPC) and a quantum dot island [10]. The graphene SET behaves as a single quantum dot device but with varying peak to peak distance for the Coulomb blockade observation. This behaviour does not appear to be gate voltage dependence. The Coulomb diamonds also vary in height across the gate voltage sweep in the stability diagram, again with no gate voltage dependence, as seen in figure 2.16.

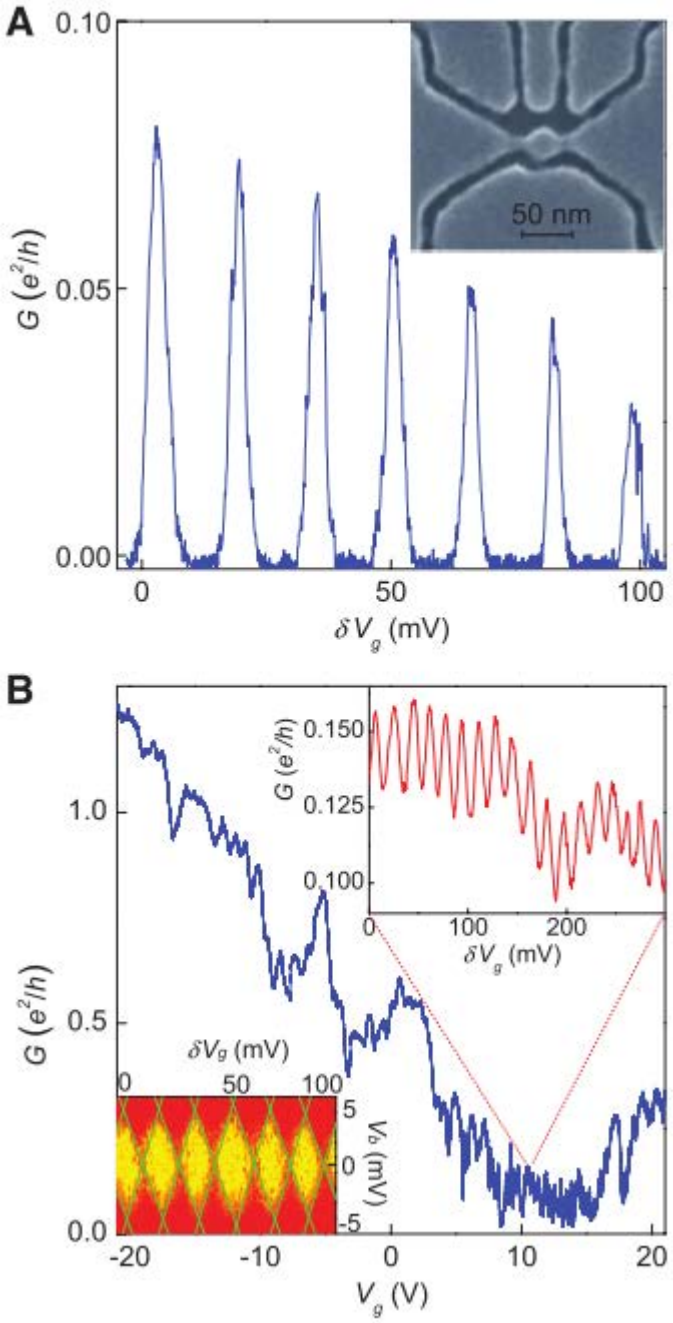

Figure 2.16: Coulomb oscillations and stability diagram of a graphene device patterned into a quantum dot with quantum point contacts. A) The plot of the Coulomb oscillations corrected to level the base conduction blockade region and SEM of the device in the inset. B) The G/Vg showing the suppressed conduction region and the Coulomb oscillations superimposed on the overall conduction plot seen in the inset in the top right. While the bottom left inset shows the stability diagram for the small Coulomb diamonds with a few mV height and width. [10]

The other method for studying graphene SETs is to fabricate the graphene into a segmented nanoribbon, where the nanoribbon is patterned into a wide-narrow-wide pattern. The segmentation refers to how the the wide sections are the leads and the narrow is the confined region. This method has shown the largest variability in Coulomb blockade behaviour. Multiple dot, Kondo effect, interference patterns and NDR have

frequently been demonstrated. The key issue with this method has been the inconsistency between devices of similar design, where localised charges form multiple dots due to charge transfer doping and rough edges, creating devices where electrons tunnel across these localised regions within the channel. More recently K. Ensslin's group has demonstrated how the combination of the leads and channel contribute to the measured behaviour [63]. All these different factors impact the graphene SET leading to the unpredictable nature of this type of device.

Further to this, graphene SETs have been observed with patterned gates for electrostatic control in the same method as other 2DEG devices. This was best demonstrated with bilayer graphene, where the bandgap and doping can be controlled by the multiple gates instead of with RIE etching of the material [73]. The multiple gate structures have been used to tune the coupling between the localised states in a nanoribbon to create multi-dot SETs.

Lastly the use of electro-burning thins the nanoribbon into a point contact which acts as an SET. This method has shown the electro-burning of a suspended nanoribbon creates an SET with an addition energy of 300meV [74]. An energy of this size can be observed at room temperature, unfortunately this method is limited to a small gate voltage range [38]. The suspended nature of these devices causes the device to break if the gate voltage increases beyond the threshold for mechanical pull in of the ribbon.

In a graphene SET the energy level spacing has been predicted from the DOS [11]. To show that the spacing has an inverse relation to the square root of N, which, had be presumed correct due to the fitting with the measurement of excited states in a device under a magnetic field. If the value of N is small though (<5) the theory is predicted to not match as easily. The addition energy has also been proven to be much larger in a graphene Nanoribbon, where the self-capacitance is shown to be ~2.4 times greater than the typical estimation for a disc. This was demonstrated by fitting the extracted addition energy of the graphene SETs against the effective dot diameter, seen in figure 2.17.

$$\Delta \mathrm{E_S} = \frac{\hbar v_\mathrm{F}}{\mathrm{d}\sqrt{\mathrm{N}}} \tag{2.17}$$

2.4 Alternative graphene logic devices

2.4.1 Introduction

If graphene is going to be a useful material for more than Moore devices the unique properties of graphene that can achieve this need to be explored. The fabrication of nanoribbons represent the need to downscale graphene and produce dense arrays of logic devices. But alternative methods to using graphene beyond SETs have to be considered.

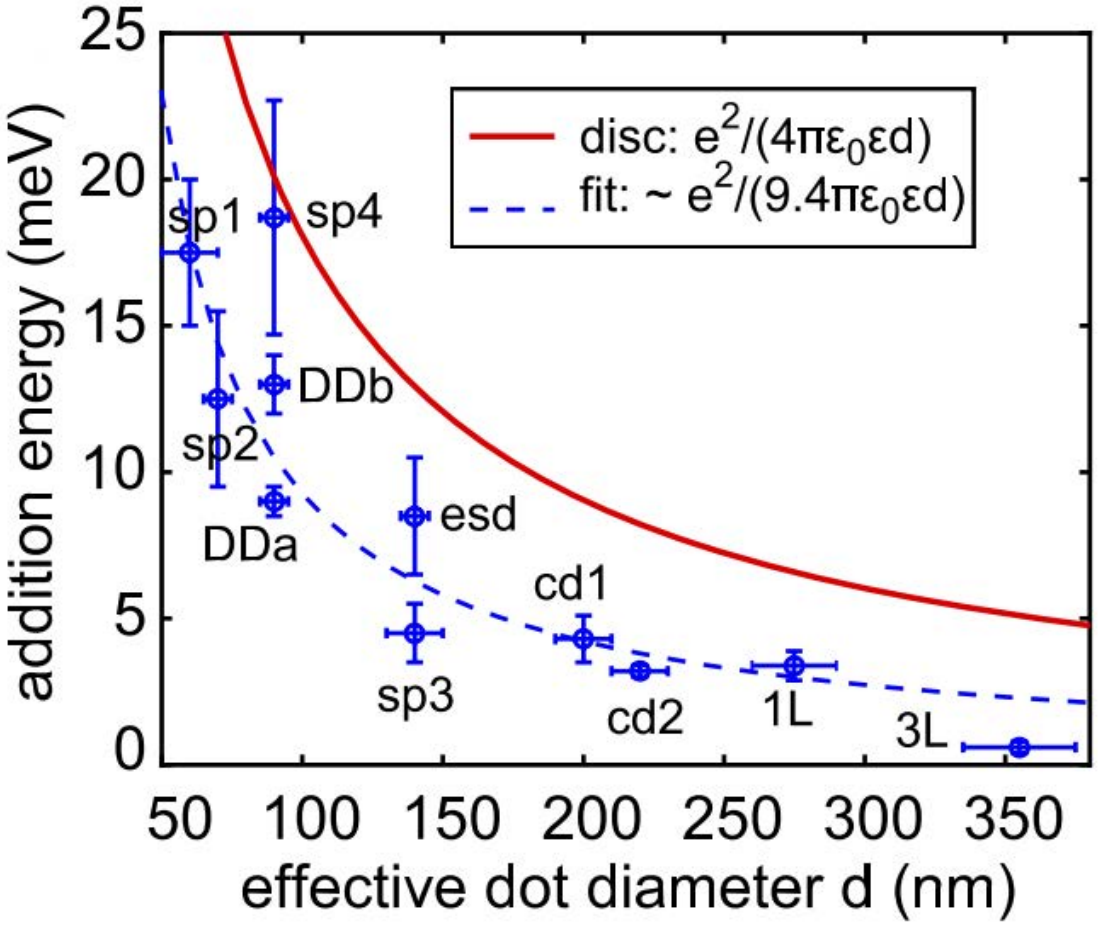

Figure 2.17: Figure of effective dot diameter against extracted addition energy with the two models of self-capacitance. Demonstrates the classical method for calculated the addition energy needs to be adjusted for a graphene device by modifying the calculation by 0.42. [11]

2.4.2 Ambipolar logic

Conventional transistors use a unipolar semiconductor, by doping the semiconductor with with donor or acceptor atoms (Boron or Nitride) which creates a semiconductor that is either N or P type. However the "doping" characteristic of graphene can be manipulated by varying the electrostatic potential applied to the transistor, as discussed earlier in 2.1.2.

For graphene logic devices it would be a requirement for future development to create combinational logic by wiring up these transistors. It is predicted that using ambipolar logic could reduce the number of required transistors down by as much as 38%, delay by 26% and power consumption by 32% [75, 76] .

In Traversi et al (2009) [12] two transistors are fabricated with exfoliated graphene and 3 terminal metal contacts deposited on top using a common drain electrode. This shows the first CMOS inverter with graphene. Initially the two transistors are p-type but by Joule heating one of them at low temperature it shifts to be more negative. A logic signal is input through the device see Figure 2.18. It demonstrates a capable CMOS inverter, albeit with a poor gain, maximum frequency and always-on state. The poor gain is the main difficulty in CMOS logic with graphene since it limits the ability to cascade the transistors together.

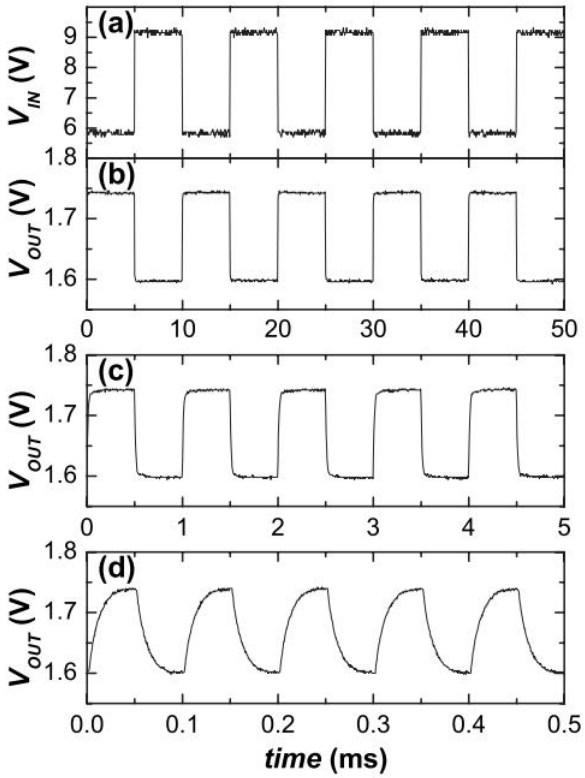

Figure 2.18: Inversion of input logic signal by two graphene transistors [12]

2.4.3 Graphene single transistor CMOS

It has been demonstrated by Sordan .et al in 2009 [77] that a single graphene transistor can exhibit all the different logic gates behaviour by exploitation of the ambipolar behaviour with no band-gap engineering. The transistor is fabricated on exfoliated graphene by depositing two metal contacts and silicon back-gate. By using an arithmetic mean of the two inputs (Figure 2.19a), Boolean logic can be achieved to give the digital waveforms seen in Figure 2.19b. The same problem with low gain occurs but gives a predicted clock frequency of 6.6 GHz when using a typical gate capacitance. The demonstration of logic gates by varying levels of the gate voltage is achieved. This shows the potential graphene has for CMOS logic circuits using a unique architecture.

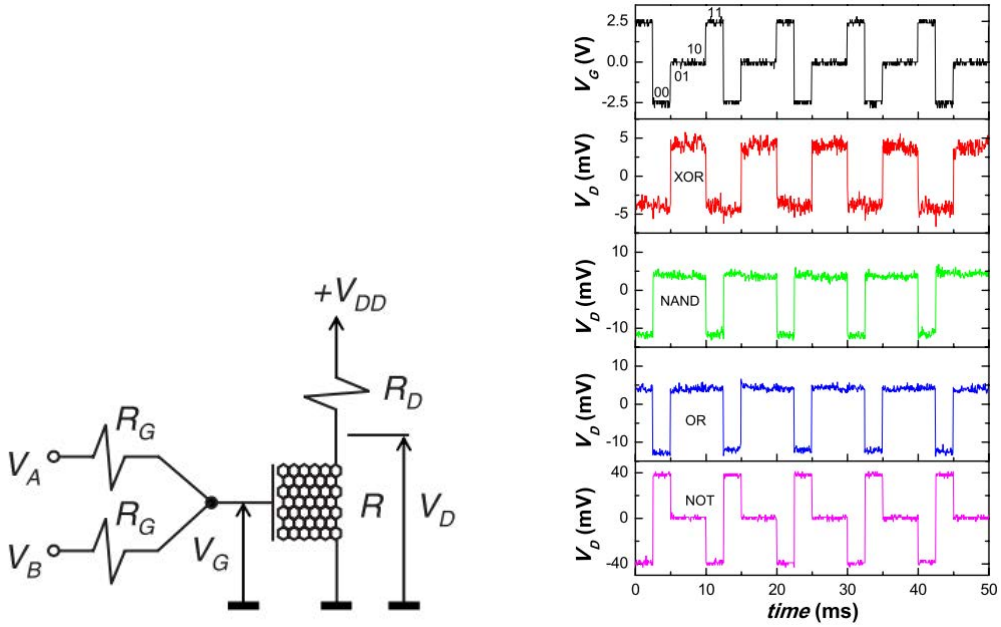

Figure 2.19: a) Circuit diagram of single transistor logic gate with two inputs b) Output logic of gate depending on gate voltage

2.4.4 GNR PN Junctions

A vertical PN junction is made by doping graphene with AuCl_3 and benzyl viologen for p and n type respectively [13]. PN junction diodes are fabricated with ~10^3 on/off ratio which demonstrates vertical electron transport with a two terminal device, see figure 2.20 for the PN junction characteristics.

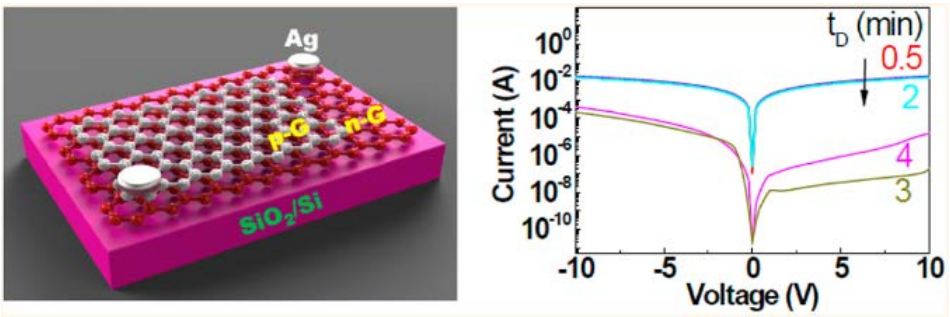

Figure 2.20: PN junction diode schematic and I-V curve [13]

2.4.5 Tunnel FET

Another type of transistor structure that has been developed to overcome the sub-threshold swing limitations of MOSFETs is a tunneling transistors that relies upon band to band tunneling between P-i-N junctions and quantum tunneling of electrons through a dielectric. These have already been demonstrated in silicon [78].

2.4.5.1 Band to band tunneling

In the same way graphene can be used a channel replacement for standard MOSFETs it can also be used as a channel replacement in silicon TFETs. Much like a common transistor is the exploitation of a back to back PN junction with a MOS capacitor to control the inversion layer, the TFET exploits the nature of a tunneling diode. The operation of a tunneling diode is where the conduction band of one side of the junction matches the energy level of the valance band allowing electrons to tunnel through the band. This is called band to band tunneling (BTBT) mechanism which compared to a MOSFET, relies upon thermionic injection of electrons instead. The structure of a typical TFET is a p-i-n junction where the p and n are the source and drain, the device is switched on and off by controlling the band in a reverse-biased mode [79]. To create a CMOS device, the junction is doped either n or p to favour the conduction of electrons or holes.

Of course another way is to create P-i-N junction TFETs with graphene alone. The proposed structure in Zhang et al (2008) [80] is given using graphene as a channel material. This theoretical paper shows a graphene TFET can have a 5 times greater intrinsic switching speed compared to a 2009 MOSFET, due to the subthreshold swing is 0.19 meV/decade while under a 0.1 V gate voltage. This is of course under ideal performance as gate oxide leakage, interface charge and parasitic resistances do not act to degrade the performance. Table 2.1 highlights a transistor can operate with a much smaller supply voltage. The on current is predicted to be much smaller but the leakage current is significantly smaller as well to give a very high on/off ratio. The intrinsic switching speed of the individual transistor is 6 times faster (not to be confused with operation frequencies of processors).

	2009 nMOSFET	GNR TFET	unit
Equivalent oxide thickness	0.75	1	nm
Supply Voltage V_DD	1	0.1	V
Drive Current I_D	1639	800	$\mu A/\mu m$
Off state leakage current I_{off}	070	0.000025	$\mu A/\mu m$
Intrinsic speed ~$I_D/C_{Ox}V_{DD}$	1961	11000	GHz
Off leakage power	0.70	0.0000025	$\mu W/\mu m$
Dynamic Power	820	40	$\mu W/\mu m$

Table 2.1: Comparisons between proposed TFET and a 2009 nMOSFET [80]

Simulations in Kang et al. in 2013 [81] have devised a structure for a monolithic all graphene TFET, where all source, drain and channel regions are graphene. This uses N and P doping on either side of the channel and creates 6 transistors capable of two inverter stages. This paper also highlights the better switching ratio of graphene compared to a 22nm MOSFET. It also has a faster SS and a smaller power consumption especially with a 0.1V supply. But since this is a proposal a number of issues in fabrication will cause detrimental effects to the drive current and SS to occur.

One of the first experimental results using a buried triple gate structure demonstrated the principle tunneling behaviour of a GFET, using the electrostatic doping control to tune the majority carrier in the graphene sheet. Although there has yet to be any significant analysis of the performance of such a device, it provides the desired evidence of the potential of lateral tunneling behaviour in graphene FETs [82].

The use of BTBT tunneling is an important method for obtaining graphene devices using all its potential without as many of the downsides in aggressive patterning down to 2nm dimensions.

2.4.5.2 Vertical tunneling

Quantum tunneling FETs rely upon electrons tunneling directly through a dielectric barrier between a sandwich of two graphene sheets. These types of transistors are usually referred to as vertical tunnel FETs [VFETs]. The first demonstration of this is using h-BN another 2DM to act as the tunneling barrier [83].The discovery of several other 2DMs makes it possible to create heterostructures or Van-der-Waals structures [39] by using a combination of these. This allows the properties of a material to be fine-tuned for its purpose.

Improvements were made on the stacked VFET by using a semiconducting 2DM with for a smaller band-gap such as molybdenum disulphide [MoS_2] or tungsten disulphide [WS_2] [14]. This massively increases the on/off ratio of the VFET to 10^6 due to the WS_2 band-gap being much smaller than h-BN so the electrostatic control of graphene's Fermi level is much closer to the barrier height of WS_2, see figure 2.21.

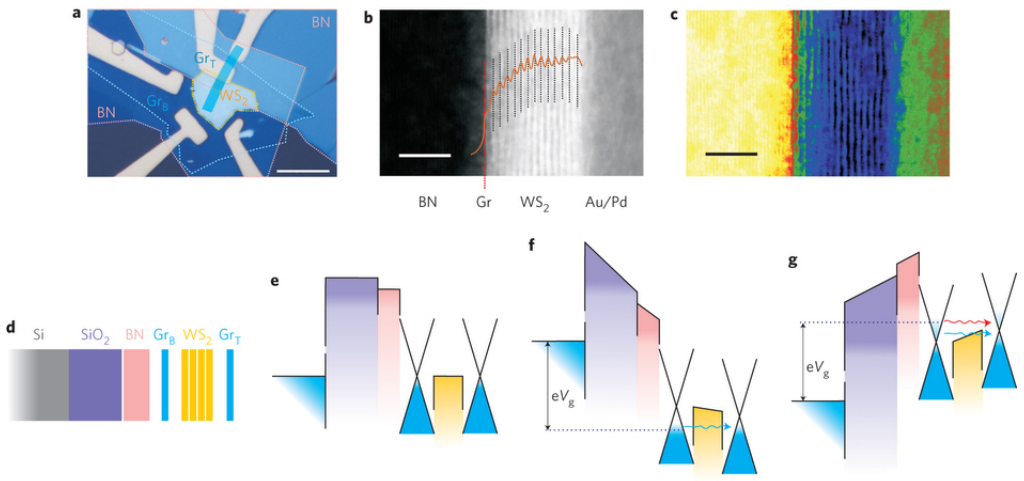

Figure 2.21: a) Image of device b) Observation of WS_2 layers c) Bright-field STEM d) Schematic e) 0Vg Band diagram f) <0Vg g) >0Vg [14]

This gives a better on/off ratio with a high on current of $10^{-6}\mathrm{A}\mu\mathrm{m}^{-2}$, see figure 2.22. This high electron conduction is facilitated by the device using mainly thermionic current instead of mainly tunneling current as it did previously. The subthreshold swing is determined to be less than <60m/decade and limited by the capacitance of the thick gate dielectric, leading to a predicted 20 mV/decade subthreshold swing with a 5 nm HfO_2 dielectric. This type of transistors helps prove graphene versatility for producing devices capable of electron transport in 3 dimensions.

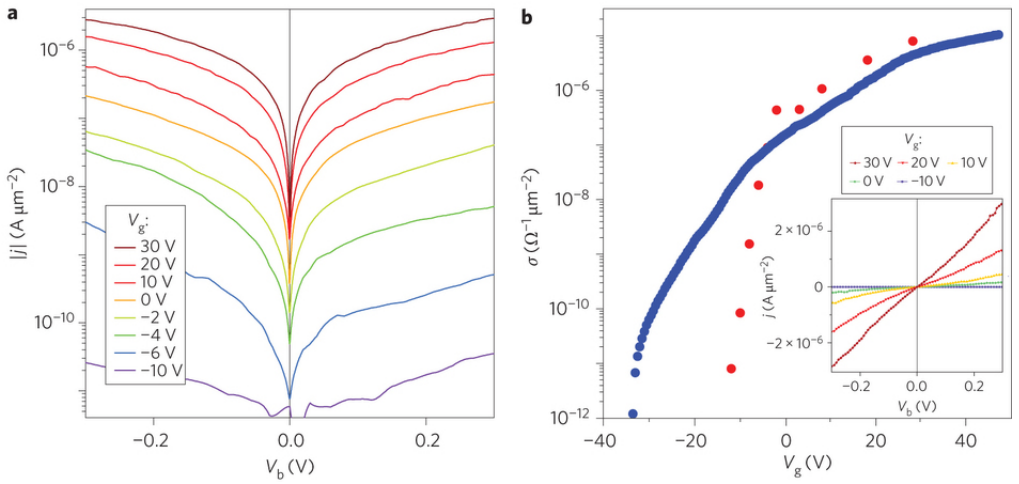

Figure 2.22: Transfer Characteristics [14]

2.4.6 Electro-optical suspended graphene

The ballistic interference patterns are measured using exfoliated graphene that is transferred onto the target substrate using a PVA/PMMA mediated transfer. The target substrate has been fabricated by depositing the gate electrodes first and spin coating a very sensitive e-beam resist on top. Once graphene has been transferred the resist is patterned so the graphene is suspended across the target area. Lastly metal contacts are

deposited onto the graphene for source and drain contacts. The device fabricated this way investigated the conductance mapping by changing gate voltage to vary the carrier concentration. The second devices are used to investigate the interference pattern of electrons by Fabry-Perot [68]. This demonstrate gate bending of the electron paths in suspended graphene to produce optical devices using electrons. Most recently this was taken a step further by the same group to control the electron path using a magnetic field in conjunction [84].

2.4.7 Graphene-silicon integration

The key work that demonstrates graphene's use in a BEOL process was completed by IBM [32]. Here the graphene was transferred onto a silicon chip designed to amplify analogue signals, to act in a complementary nature to the silicon devices. Graphene's superior performance is used as an analogue amplifier due to its higher cut off frequency, to demonstrate the benefit graphene can have when used in combination with a traditional silicon processing method to improve the analogue devices performance in general. Although there has yet to be a logic device that has taken advantage of this method

Another option for graphene-silicon integration is to use graphene as an interconnect material. When the silicon technology reaches the point where decreasing the transistor size is no longer feasible it will be important to look at other avenues for improving the overall performance of the chip. One issue that is often overlooked is the shrinking transistor size introduces further issues with the interconnect material, as the interconnect size decreases the resistance increases [85]. Graphene also makes it feasible to create an interconnect material for flexible devices when integrated with silicon [86].

2.5 Fabrication considerations

2.5.1 Defects

2.5.1.1 Edge Defects

The defects that occur at the edges are largely dependent on the method used to fabricate the nanoribbon. If the edges are terminated perfectly such as in a unzipping CNTs the properties will closely match ideal electronic devices. But if typical mass manufacturing methods are used the edge will be much rougher and disordered, where atoms are use to sputter and bombard the graphene to remove carbon atoms.

Some of the best operating GNRs have been fabricated from unzipping carbon nanotubes Wang et al [87] [9]. This is due to the much smoother edge profile and termination of dangling bonds. By using Palladium as the metal contacts the Schottky barrier effect

is reduced compared to traditional Ti/Au contacts. The 2 nm wide unzipped CNTs are compared to wide (40 nm) nanoribbons. The performance of the nanotube is summarised in the table below. At 40 nm the nanoribbons were found to be metallic, this is due to the band-gap being too small for it to be observable at room temperature.

In Ritter at el (2009) [15] graphene is transferred to a silicon substrate and using a scanning tunneling microscope [STM] to observe the structure of the GNRs. In combination with scanning tunneling spectroscopy [STS] the band-gap called be identified by probing the local density of states [LDOS].Figure 2.23 shows the amorphous edge structure of the GNRs, depending on the percentage of the type of edge, determines if the GNR is armchair or zigzag. A predominantly armchair nanoribbon with a width of 2.9 nm had a $\mathrm{E_g}$ of 0.38 eV, roughly close to theoretical predictions (0.5 eV for 2 nm [42]). The zigzag nanoribbons had a much smaller band-gap of 0.14 eV for 2.3 nm and 0.12 eV for 3.3 nm, significant enough for the zigzag nanoribbons to be semiconducting, clearly not coherent with the tight-binding calculations but if using DFT it can predict a small band-gap due to ”staggered sub-lattice potentials”.

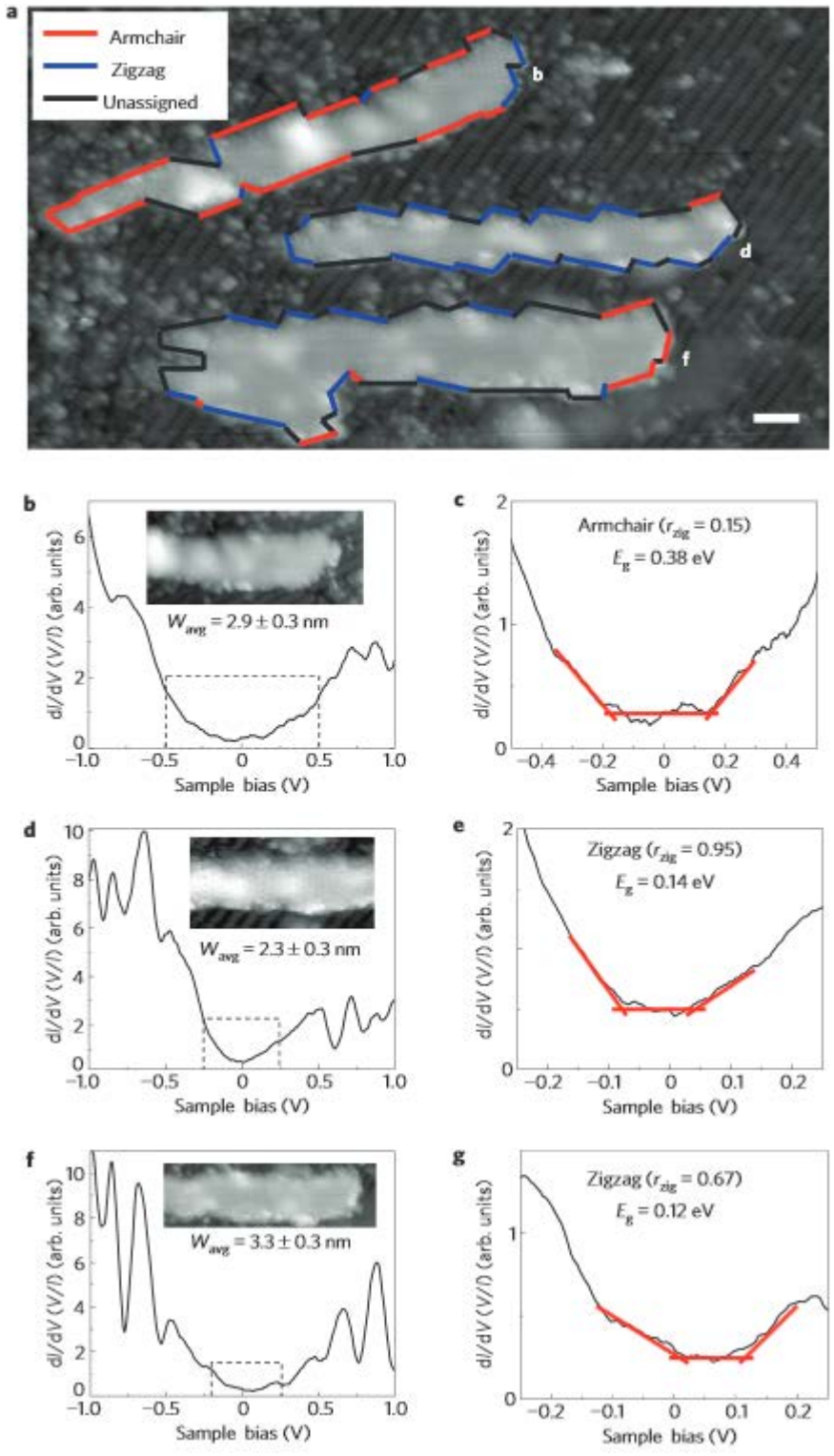

Figure 2.23: Orientation of edges in GNRs and corresponding band gaps [15]

The peculiar nature of the semiconducting zigzag nanoribbons is also described in Li & Lu in 2008 [88]. It states that defects strongly affect the conductance in nanoribbons and gives a reason for zigzag nanoribbons being semiconducting due to Anderson localisation. The situation with zigzag nanoribbons is much more complex when considering the stability of freestanding zigzag edges.

In the work “Low-energy termination of graphene edges via the formation of narrow

CNTs" the stability of edges is considered with the possibility of edges folding back on themselves to form CNTs. The most stable edges are armchair and a reconstructed zigzag into a 5-7 sequence. Klein edges (dangling bonds) is the least stable and determined to reconstruct by pairing the dangling bonds. The formation of nanotubes is more stable and wider nanoribbons and simulated to form an armchair nanotube (rolled zigzag graphene) at (8,8) of the Hamada index. However work by Girit et al [89], shows a zigzag edge is stable under electron microscopy and even demonstrates a reconstruction of graphene atoms shifting to reform the edge structure. An interesting behaviour of edges is the nature of holes on the edges even if the nanoribbon is n-type [90].

The nature of graphene's edges present some unusual results with some contradicting evidence depending on environmental circumstances, leaving some investigations to be discovered on the true behaviour of graphene at the edge.

2.5.1.2 Point Defects

Other defects are caused by carbon atom vacancies or lattice dislocations within the nanoribbon channel. Not much is experimentally verified for the effect single point defects have on the charge transport properties so most focus has been on observing them. Usually the level of defects is analysed by Raman spectroscopy to determine the level of defects without much need to understand the atomic level behaviour of them. Limiting defect analysis down to electrical characterisation.

Robertson et al in 2013 [16] two different types of single point defects are observed in graphene. The first is a symmetric monovacancy [sMV] where the lattice remains unchanged and a reconstructed monovacancy [rMV] where the lattice reforms into a 5&9 rings. This observation is confirmed by the analysis of the geometric phase and bond length, see figure 2.24. It indicates a sMV can exist for short periods of type, although it is possible it could be an oscillating rMV but the evidence mostly suggest otherwise. Other observations are the lattice translations of the 5 ring in the rMV to switch from one side to the other with the intermediate stage observed. Though it is assumed to be an approximation of before and after the translation. The other type of defect is a Stone-wall defect, rather than a missing atom, two atoms and its bond are rotated. The carbon lattice reconstructs into two 7 ring and two 5 ring groups.

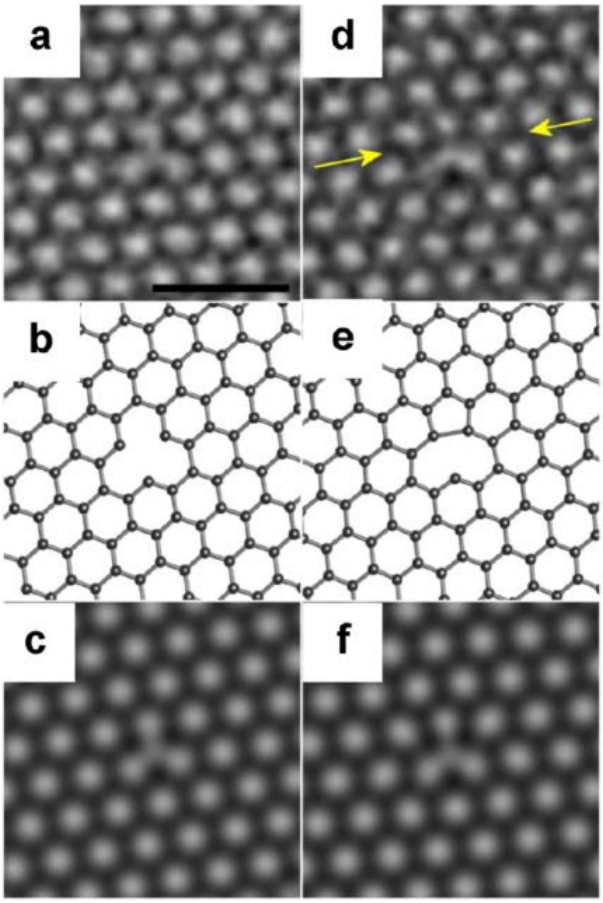

Figure 2.24: Observations of defects in (a & d), Simulations in (b,c,e & f) [16]

The exploitation of defects in a graphene nanoribbon has been done by Nakaharai et al in 2012 [91] using helium ion damage. A dual top gated P-i-N transistor is fabricated with the two gates acting as the electrostatic doping control. The intrinsic graphene channel is 30 nm wide nanoribbon that is heavily irradiated with helium ions to induce a transport gap of 380 meV by defects, with the level of defects apparent from the Raman spectra.

The transistor is switched between nFET & pFET using one of the gates and the transfer characteristic is measured see figure 2.25. It gives a small on current of ~0.08nA for electrons and ~0.025 nA for holes, contrary to evidence of hole mobility being as high. But there is an on/off ratio10^3at 200K and ~10 at room temperature. Demonstrating the potential of graphene devices that combines point defect band gap control, ambipolar gating and a pseudo tunnel FET structure.

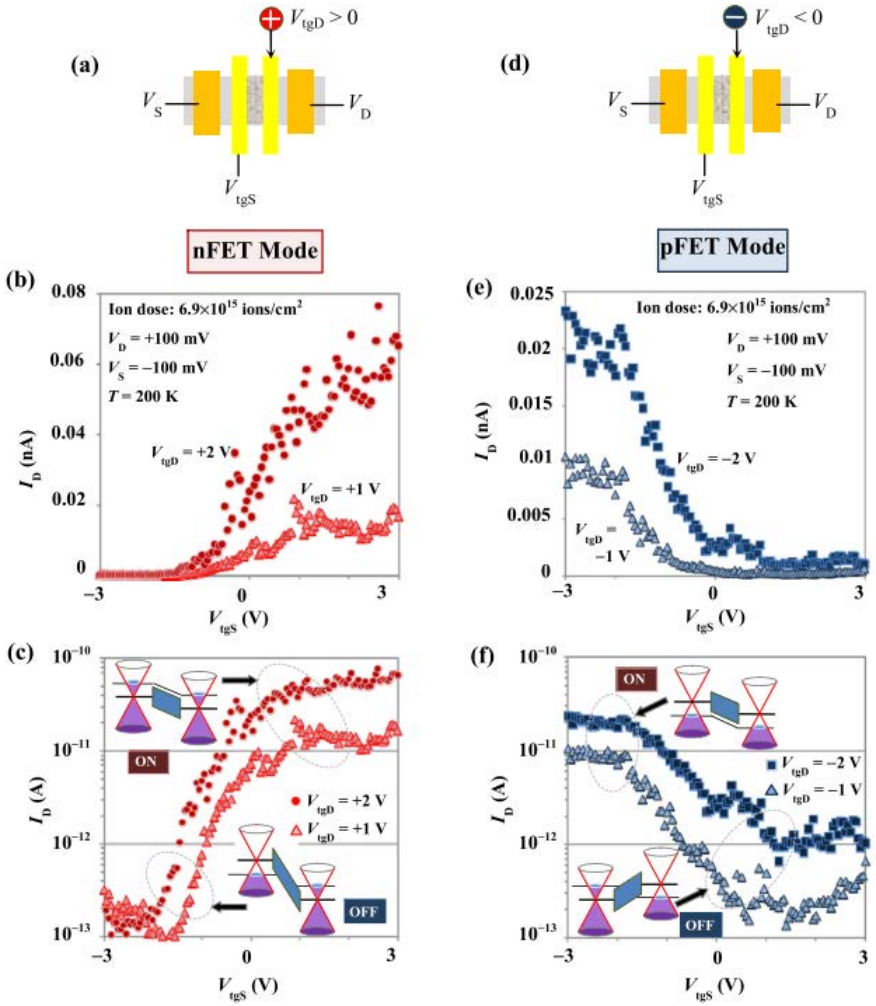

Figure 2.25: Schematic and Transfer characteristics for nFET and pFET modes of operation

2.5.2 Doping

In conventional methods doping is a achieved by ion implantation of donor and acceptor dopants such as boron or nitride. The situation is much more complex with graphene since it is possible to dope purely by physio-adsorption of molecules onto the surface without replacing any atoms in the lattice [13]. It is for this reason most intrinsic materials have been naturally p or n doped due to substrates and water molecules etc [44]. A band-gap can even be induced by bromine absorbed onto the surface [44].

Chang et al in 2013[17] show it to be possible to induce a band-gap in graphene by boron nitride doping. With a 6% level of doping a band-gap of 600 meV can be achieved, higher than the required band-gap for logic transistors. Although it is done with a sacrifice in the mobility, indicated by a 10kΩ difference between doped and undoped graphene, see figure 2.26. The method used though is simple by growing the dopants in-situ with the CVD of graphene. By introducing ammonia borane vapour into the chamber and controlling the concentrations by the heat applied to the molecule.

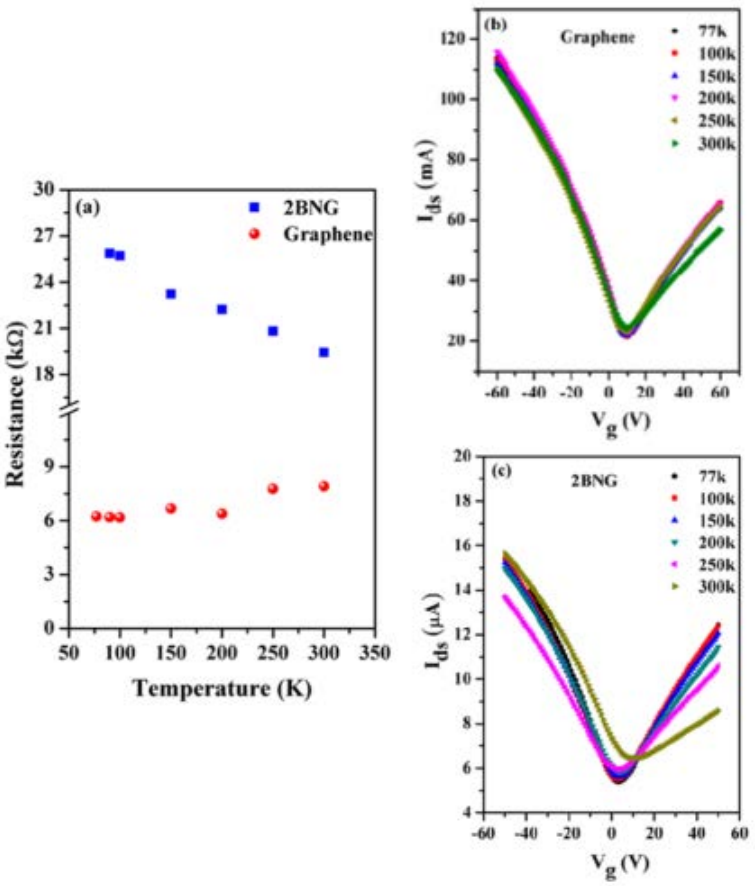

Figure 2.26: Left: Difference in resistance between 2% doped and undoped Right: Transfer characteristic [17]

2.5.3 Surface Interactions

The 2 dimensional nature of graphene means that it is even more importance the effect substrates can have on graphene, from surface roughness to interface interactions with dielectrics and metals. Various substrates have been used for graphene, most notable is silicon dioxide. It has been known for a while that silicon dioxide has a detrimental effect on the mobility in graphene sheets. The continued use of silicon dioxide has mainly been due to ease of use as a substrate and optical interaction with graphene to make it visible to the naked eye. With the increased popularity of CVD grown graphene, it has expanded across to a notable 2DM hexagonal boron nitride. Providing a much better alternative substrate for graphene transistors to achieve a much higher on current.

2.5.3.1 Metals

In the paper "Contact and edge effects in graphene devices" in 2008 [90]. Scanning photocurrent microscopy is used to demonstrate the effect of metal gates on the charge distribution of a GNR when backgated. The metal used is shown to have an effect on the doping. Ti causing an n-type doping and Au to cause a p-type doping. This is

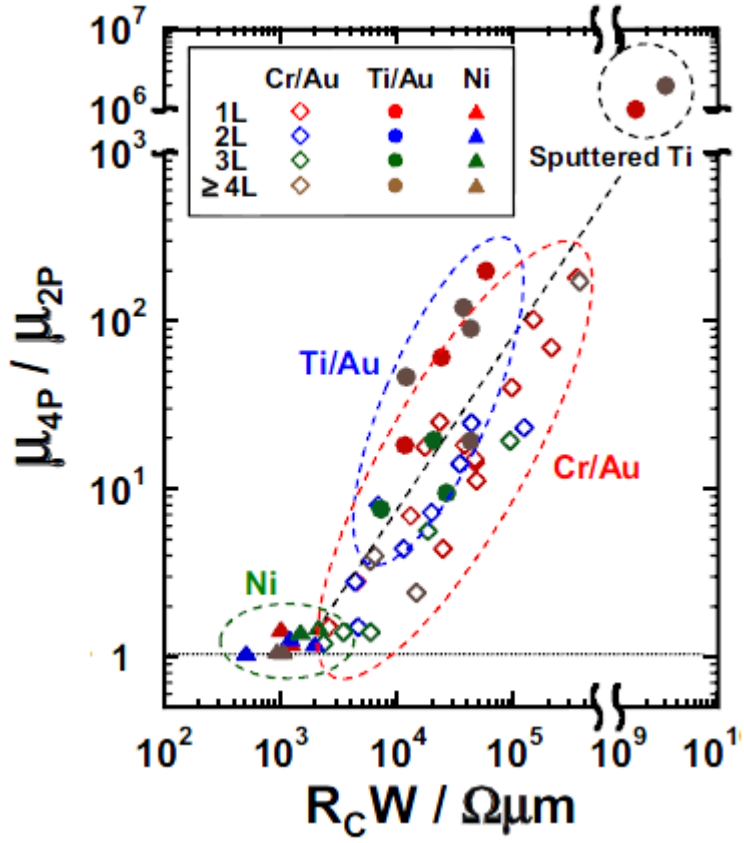

Figure 2.27: Plot of graphene contact resistance measurement for different metals against the mobility. Shows that titanium and cr produced large variations in contact resistance. While nickel shows the best performance. [18]

importance since Ti is often used as a surface contact on graphene, due to the better bonding to graphene. Other metal effects such as alkali and alkaline earth metals can cause electron doping with calcium and potassium. It has even been predicted that superconducting state could exist at 10K [44].

Beyond doping effects from metals due to a mismatch in work functions limiting the graphene devices there is more significant issue in the limitations caused by contact resistance. As investigated in "Metal/graphene Contact as a Performance killer of Ultra high mobility graphene" [18], the lowest contact resistance is $500\Omega.\mu\mathrm{m}$ with Nickel and is $185\Omega.\mu\mathrm{m}$ with the more exotic metal Palladium [92], see figure 2.27. Although these resistances are not unreasonable for GNR-FETs where the resistance greatly increase into the $\mathrm{k}\Omega$ range, for future devices that plan to exploit the ballistic conduction of graphene with a $1\Omega/\mathrm{sq}$ [50] it is of a considerable concern that needs to be further addressed. Another problem is these devices are fabricated on top of graphene and does not consider the issues relating to the graphene trapped between metal and oxide, which can cause further issues, but there has not been any information regarding the contact of graphene by metal.

2.5.3.2 Dielectrics

Konar, Fang & Jena (2010) [93] has conducted theoretical investigations into the affects of high-k dielectrics on graphene's performance due to phonons, it has led to the conclusion that with conventional dielectrics the mobility at room temperature will be limited to $10^4 \mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$. The best dielectric is predicted to be AlN and SiC over SiO_2as a better substrate. The work also reports on recent experimental evidence using HfO_2 as a top gate dielectric. It was found to have a mobility of 10,000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, although the surface optical phonons limited mobility of the material was experimentally found to be 20,000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, which is 5,000 higher than the predicted mobility. The higher value is because of a calculations for a thick crystalline dielectric rather than a 10nm amorphous dielectric used in the experiment.

Another dielectric of interest is hexagonal boron nitride [h-BN] with reported mobilities ranging from 3,400 up to 10,000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ [94],[19].

2.5.3.3 Air Most graphene devices fabricated with exposure to air have had some p doping naturally, this is caused by the air. In particular it is the moisture that is absorbed onto the surface [77]. To achieve a higher quality graphene Mayorov et al (2011) [19] has patterned hall bars with graphene and encapsulated the exfoliated graphene between two ~10nm layers of boron nitride, see figure 2.28. The resulting sandwich gives graphene an extremely high mobility of 100,000 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ at 300K and a near zero Dirac point of 0.1V. Demonstrating a desirable method of achieving high quality graphene devices by encapsulation. In general for experimentation, graphene devices are measured in vacuum or pure nitrogen environments to remove the water, showing a shift back to 0V Dirac point.

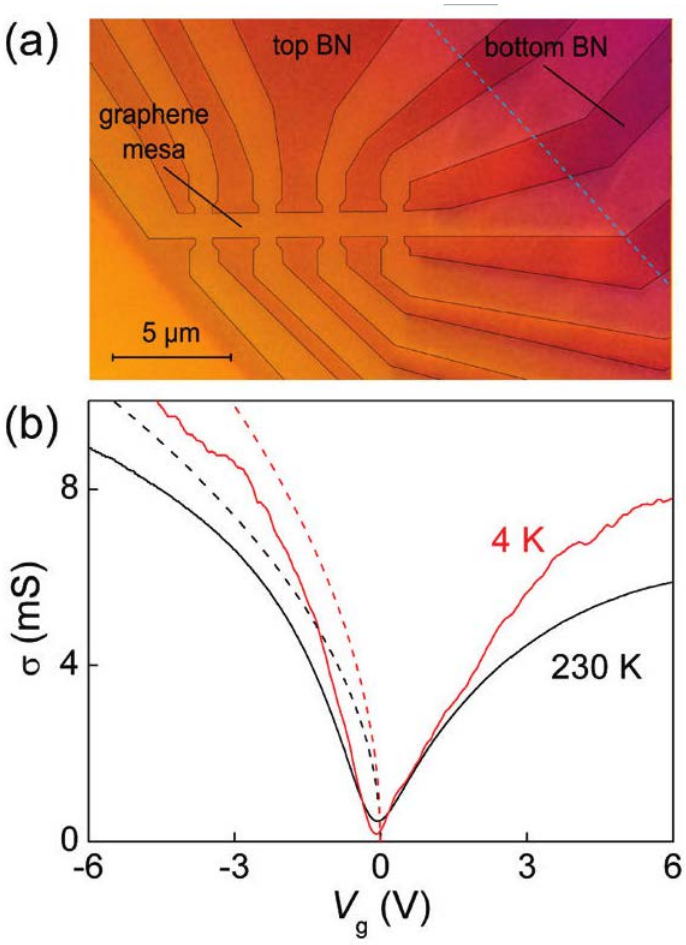

Figure 2.28: Optical image of graphene hall bar device and electrical properties of graphene encapsulated in hexagonal boron nitride. [19]

2.5.4 Etching

2.5.4.1 Dry

A routine method for etching graphene is to use a plasma (dry) process. To etch the graphene a plasma of O_2/Ar at a rate of 10 sccm, 26.5 Pa, 30 W and ~50 V DC bias is used. In Prado et al (2013) [20] the etching quality of this plasma for removing graphene is investigated. The levels of etching are analysed by AFM, optical microscopy and Raman. It is found that the later two methods can give misleading information indicating etching has finished when there is still material on the surface according to the AFM. The reasons for this is because the sp^2 bonds are delocalised or broken so there is no interactive with light or the laser used in the Raman.

The RIE etching is compared between O_2 and Ar separately to find that the quality of etch rate is indifferent to the plasma used. RIE is determined to be mainly a sputtering process, with O_2 acting to terminate the ejected carbon atoms into CO_2. This gives a required etching of 15s to fully remove monolayer graphene and a time of at least 3 minutes in a plasma cleaner, see figure 2.29 for the effect of increasing etching time on a monolayer of graphene.

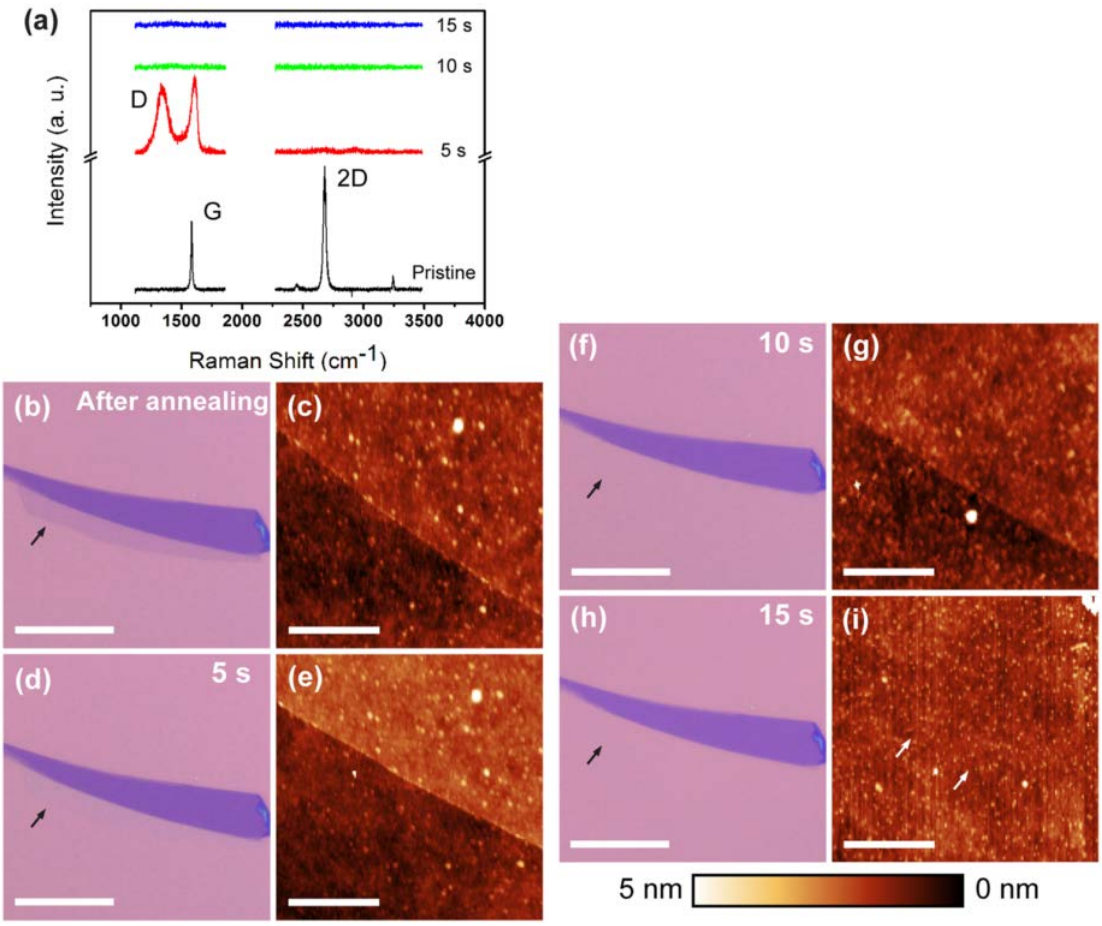

Figure 2.29: Raman spectra, optical images and AFM from increasing etching times of the graphene monolayer with RIE. [20]

2.5.4.2 Wet

To demonstrate graphene's chemical inertness, work by Shivaraman et al (2009) [21] has fabricated nanoelectromechanical [NEM] beams from epitaxial growth on SiC and subsequent under etch of the ribbons to release the structure. Once graphene has been grown on the surface, the gold clamps are deposited and graphene is then etched into ribbons with oxygen plasma. The structures are released by etching with Potassium Hydroxide [KOH] (1%) under a 100W UV light and a current of ~1.2mA.cm^2 for an etch rate of $1\mu m^2/h$ for 4 hours. The etched area is determined by the spot size, where the etching is directed. The samples are then dried using a critical point dryer.

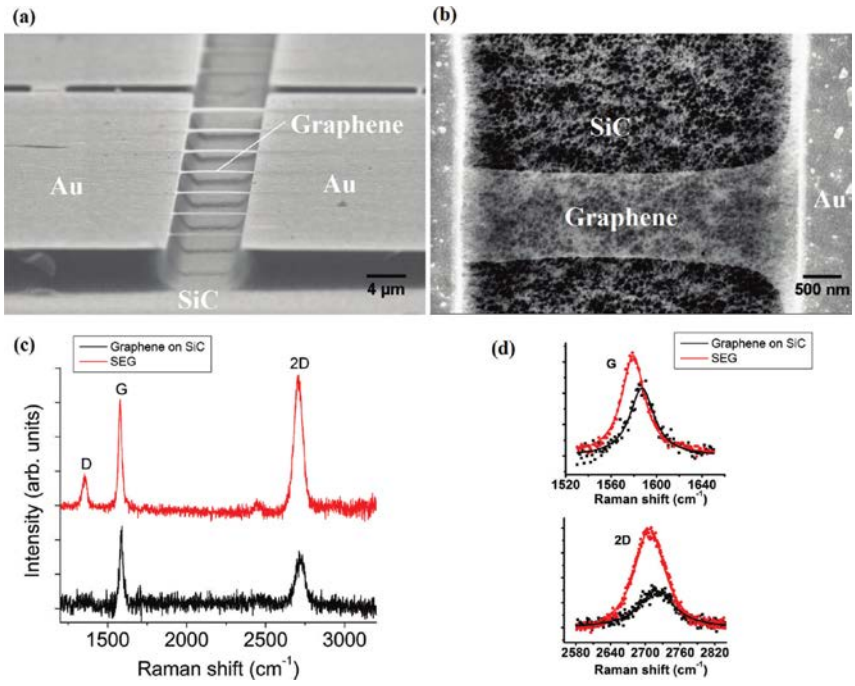

Figure 2.30: Raman Spectra and SEM images of the NEMs beams [21]

The Raman spectra shows a D peak indicating induced defects but no G peak broadening to suggest the defects to be due to chemical reaction. As can be seen in figure 2.30 the graphene can be safely etched quite aggressively and still maintains its structure.

Despite the chemical inertness against most chemicals, graphene is not as strong against strong oxidizing agents. Using Nitric acid it is possible to strip graphene from the oxide surface, the same way other organics are removed.

2.5.5 Suspending graphene

A key point to the development is the method of suspension used. Several methods exist to create suspended graphene, some are unique to graphene and others are based on work done with NEMS devices.

2.5.5.1 Wet transfer manipulation of capillary force

The majority of transfers onto flat substrates use a water-mediated transfer, where the pull in of the graphene sheet by capillary force from the water drying is a benefit to help the graphene adhere to the substrate. As seen in the previous subsection, when transferring onto micrometre sized contacts the graphene will wrap around the structures rather than be suspended. If this method is to be successful in suspending graphene it needs to overcome the capillary force by either using a critical point dryer or by patterning the features down to nanoscale so that the graphene is not pulled to the surface [95], although there has been a lack of evidence for the point at which suspension occurs with a much finer control of the underlying mechanisms.

2.5.5.2 Wet transfer onto polymer with dry release by solvent

As stated previously this method has produced some of the highest performing graphene devices [96]. This is achieved by transferring graphene onto a electron beam resist (LOR-A –Microhem) that is chemically resistant to Xylene, so that the PMMA can be stripped from the graphene without removing the underlying support material. The underlying support is patterned and a solvent is used to remove the exposed LOR-A. This method could produce micrometer sized supension. Some of the issues with this method is the extra handling of graphene and that the support material is still an organic. For this to be suitable to produce suspended devices a material that will not breakdown is necessary.

2.5.5.3 Hydrofluoric acid chemical release

This method is used to suspended graphene using HF vapour to etch the underlying silicon dioxide rather than by liquid so the graphene is suspended in a slow release which lessens the attractive Van der Waals force [97]. HF vapour etching works by cycling a HF vapour. This is a dry process because no water is used in etching or cleaning step. The problem is that not all the substrate is removed other than the channel material and the graphene is still sandwiched between oxide and metal.

2.5.5.4 Dry transfer method

A dry transfer is the transfer of a graphene/polymer stack after it has dried onto a substrate. This has the benefits of transferring graphene onto much larger features possible than by manipulating the capillary force. Since the graphene is transferred onto target substrate without water as the interfacial layer and air is instead, it means there is less complexity in process. Although this method still requires a polymer support material the graphene still suffers from contamination. The most successful of this method so far has been the use of a PDMS mold on top of the graphene/PMMA while it is etched in the ammonium persulphate [95]. After the graphene is removed and left to dry before placing onto the target substrate and heated to improve the adhesion to the substrate. This heating also allows for the PDMS to be removed with delamination of the graphene/PMMA stack.

2.6 Motivation

The properties of graphene have the potential to produce a high quality logic device if the criteria of wafer-scale production, CMOS compatibility and single electron tunneling can be achieved in a device. The single electron tunneling is the most advanced for the current state of the art logic device using graphene. This is due to the intrinsic

properties of graphene that produce SETs that can operate at room temperature and so enable graphene to be used for low power or quantum technologies. So the downscaling of graphene into nanoribbon for SETs has been mostly limited to investigations with exfoliated graphene. If the other criteria are to be met the most cost effective method for achieving a logic device is with CVD-graphene. But so far the investigations into downscaled nanoribbons has been completed by a single device. The lack of research into the effect of using CVD-graphene highlights the need for this to be investigated further. However, the understanding of the impact graphene's crystallographic structure has on the properties of the SET is also limited. By using CVD-graphene a single step suspension process can be developed to enable the study of the graphene nanoribbons structure and understand the impact defects have on the single electron tunneling properties.

The first step would be develop the transfer process for producing CVD-graphene in an electronic grade quality and then using the process to develop a method for suspending graphene. While simultaneously probing the properties of downscaling CVD-graphene nanoribbons and using this information to then produce a suspended CVD-graphene nanoribbon that can be studied to understand the fundamental properties of a graphene SET. The fabrication of the very narrow ribbons can be achieved thanks to the facilities in the Southampton Nanofabrication Centre. The demonstration of the impact a high aspect ratio between graphene leads and ribbon has means a high quality graphene devices can be produced that are difficult to fabricate elsewhere. Thanks to the collaboration with colleagues in the Optoelectronics Research Centre, high quality CVD-graphene process can be developed, where this would otherwise be difficult to achieve due to the high cost of purchasing CVD-graphene commercially. The work presented in this thesis demonstrates the first two aspects of this research and sets up the framework to produce a suspended CVD-graphene nanoribbon SET.

Chapter 3

Methodology

3.1 Production method of wafer scale graphene on silicon

3.1.1 CVD-graphene production on copper foil

The in-house CVD-graphene is grown in a custom low pressure chemical vapour deposition [LPCVD] system. The copper foil used in a 99.8% purity from Alfa Aesar, that is 25 μm thick. It is prepared by cleaning in acetone, isopropanol and acetic acid to remove all organics and surface oxide from the foil. The foil is then loaded into the quartz tube and evacuated to 2 mbar, before being filled with 6% H_2/Ar gas mixture, see figure 3.1 for the schematic diagram of the process. The temperature is then raised to $1000°\mathrm{C}$ under a gas flow of 100 sccm while the pressure is maintained at 20 mbar, once it reaches temperature the foil is annealed before deposition for 30 minutes. To grow the graphene a mixture of 5% $\mathrm{CH_4/Ar}$ with 6% $\mathrm{H_2/Ar}$ under a gas flow of 100 sccm and 210 sccm respectively. The deposition takes 20 minutes to achieve a monolayer growth. The methane gas mixture is then switched and the foil is allowed to cool down to room temperature. This information was obtained from Kevin Huang, a colleague in the Optoelectronics Research Centre.

3.1.2 Transfer process onto a substrate

This subsection describes the transfer process used after the graphene has been grown on the copper foil. This process can be adapted for any sample size, but is assumed here to be for a transfer onto a 6" silicon wafer. This process is used in the results of chapter 5 and production of the wafer scale CVD-graphene sample used in chapter 6. It is detailed here for clarity to not confuse the discussion in chapter 5. The development of this process from the original process template in literature is discussed in detail to demonstrate the improvements of this final process. The reasoning for certain steps is clarified later in chapter 5.

Step:

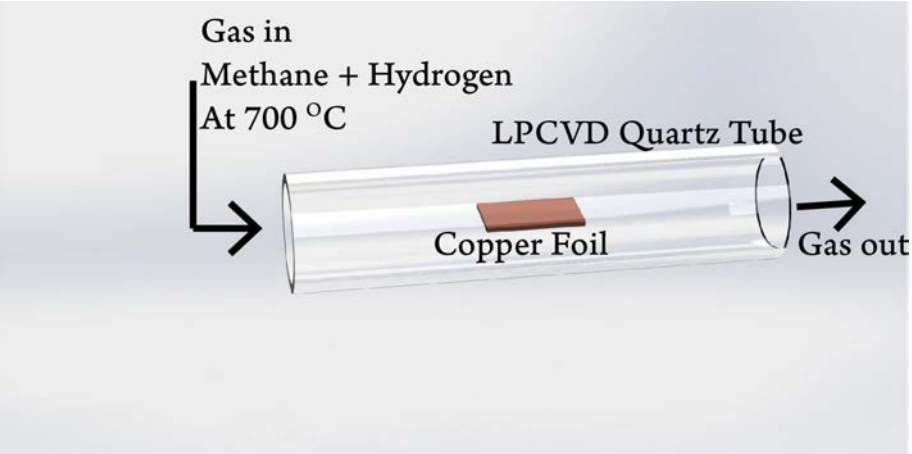

Figure 3.1: Schematic diagram to show the growth of graphene in a LPCVD quartz tube

1. Place the copper foil onto a 6" silicon or glass wafer. With care place another wafer on top and press down to smooth out any wrinkles. Avoid any excess pressure to prevent damage. Tape the corners down while ensuring the foil remains taut.

2. Transfer the wafer/foil stack to a spin coater. Pour the supporting liquid polymer over the foil so it is completely covered. For the final process a poly-vinyl butyral [PVB] powder mixed with ethanol for a 5% concentration is used [98]. Previous methods would have used PMMA as the support layer.

3. Spin the wafer/foil stack at 500 rpm to spread the polymer out for 15 s. Increase to 2000 rpm for 30 s to thin the polymer down to ~500 nm. Finish by curing the polymer at 75C on a hot plate for 2 minutes. See figure 3.2 for the copper foil on a glass wafer curing on a hot plate.

4.

5. Once cool flip the foil over and tape down the corners on the wafer again. Transfer to an Oxford Instruments RIE80 and etch the graphene on the backside of the foil. The recipe for the etch is 20 s at 20 W in a 100 mTorr pressure with a Ar/O2 mix of 80/20 sccm.

6. Fill a tank with a 0.5 M ammonium persulphate solution. Remove the tape from the corners of the foil except one. The last piece of tape is folded over to act as a handle. Gently support the foil with the wafer while holding the tape handle with tweezers and lower into the etchant. The surface tension of the liquid should allow foil to rest on the surface. If this does not happen it may be necessary to remove and dry the foil before attempting again. In figure 3.3 the foil can be seen floating on the surface of the faintly blue liquid in the plastic tray.

7.

8. After 4 hours the foil should of etched and the polymer should be faintly visible on the surface.

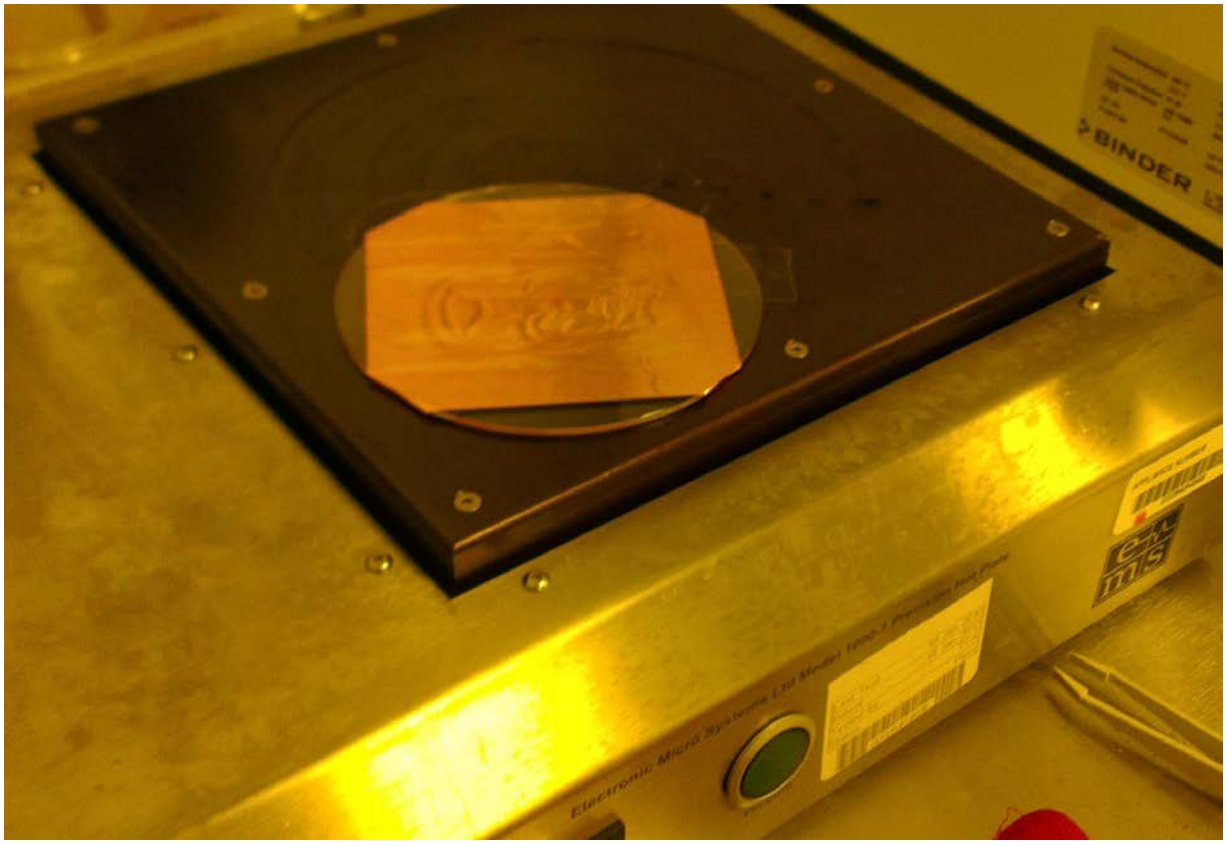

Figure 3.2: Photograph image of graphene and copper foil with PVB curing on hot plate

Figure 3.3: Photograph image of graphene/copper stack floating on the ammonium persulphate etchant solution

9. Use an aspirator to remove as much etchant solution as possible, but leaving enough so the foil is still floating on the surface. Fill with DI water and repeat 2 more times. Leave in the DI water for 5 minutes.

10. Replace with hydrochloric acid (30% concentration) for 2 minutes. Repeat the same procedure as step 7.

11. First clean target substrate in acetone and IPA. Constantly hold the substrate with tweezers and insert underneath the foil. Lift substrate up underneath at an angle in a smooth steady motion. Lift completely out of the water with graphene/polymer stack now on top of the substrate. Use the kapton tap handle to manipulate the graphene onto the desired area. Stick the tape down on the surface to stop the graphene moving about too much.

12. Transfer the wafer onto a cleanroom wipe. Keep horizontal while moving to prevent any water trapped from causing wrinkles. Leave the wafer to dry for 30 minutes in air while in the fume cabinet.

13. Heat at 65°C on hotplate for 3-5 Minutes to remove water and reflow PVB to reduce cracks and wrinkles

14. Allow time to cool. 5 minutes is typically enough time.

15. Soak for at least an hour in Ethanol to remove the PVB.

16. Store in sample box until ready to process.

Using this process is capable of producing a wafer scale transfer of graphene with minimal cracks and wrinkles. The finished graphene on a wafer is shown in figure ##.

3.2 Technologies for graphene device fabrication

3.2.1 Electron-beam lithography

Electron-beam (e-beam) follows the same procedure as photolithography with the exception of using electrons to expose the resist. Electrons allow for a much higher resolution to be achieved by directing a beam of electrons in a pattern across the resist. This is called a direct write method and makes the throughput much lower, the time taken to expose a wafer is not instantaneous and is dependent on the beam conditions to scan across your desired pattern. The Electron beam lithography tool used is a JOEL JBX 9300FS that can pattern with a beam spot size of 4 nm.

E-beam is still a desired method for increasing resolution of IC fabrication if photolithography fails to continue producing greater resolution by increasing the number of beams. Currently though e-beam remains in the use of academia and research for

Figure 3.4: Image of large scale transfer of graphene with minimal cracks, wrinkles and residue on the surface

investigating nanometre sized devices. Although the throughput is lower, the cost of producing a photomask capable of 10 nm features would not be possible.

It is known that electron beams can damage graphene so care has to be taken when using e-beam to pattern on top of graphene [99]. This is done by reducing current of the beam down to 100pa with a small 60um aperture so there is a low dose that exposes the sample, using the resist that is being exposed as a protective layer of graphene as well.

Generating an Electron-beam dose test file

The most widespread method for patterning nanosized features on graphene is to use electron beam lithography, for this there needs to be a library of design geometries for graphene nanoribbon circuits. This is not as straightforward as indicated as the lithography must be matched to the particular machine used to write the E-beam patterns first. Due to the difficulty in controlling the spot size of the electrons and the effects of secondary electrons, the spot size and minimum feature size is much larger than the actual size of an electron. With the JOEL E-beam system, a spot size of 4nm can be reliably reached.

Although, this is only a part of the restrictions that determine feature size. It could be possible for a 4 nm dot could be patterned into the resist, this would be a very isolated feature. If the pitch between separate dots was decreased the dimension would end up being much larger. This is due to proximity effect, when the electrons hit the resist they

do not stop but instead continue being propelled into the substrate. However, they do not follow a straight line into the resist and arch out from deflection by the electrons surrounding the atoms. This accounts for the initial spot size; where this is limited by the beam conditions and the thickness of the resist being used. The other effect that comes into play is secondary electrons. The first electrons have enough energy to energise the substrate and emit more electrons. Unfortunately some of these can exit the substrate and modify the resist, this is called a proximity effect. It is for these reasons that the more dense and closely packed in your designs are the more difficult it is to produce a 4 nm feature separated by a 4 nm gap (which is impossible for this tool). The limit is usually a 10 nm feature size and gap. Even this has quite a bit of difficulty though, so is not a trivial matter to reliably reproduce.

Fortunately many parameters can be adjusted to give the best result, such as the resist (material, thickness, density etc), the beam condition used and the software used to generate the electron beam lithography files. The software's tools allow the compensation of the proximity effect by a proximity error correction (PEC). This analyses the design file (GDSii) and modify it depending on the input parameters given for the Electron beam tool. This adjusts the base dose by decreasing it by as much as 30-40% to achieve the desired pattern. So quite dense features would not need the maximum dose as the proximity lowers the overall needed dose for that area. To accurately do this a Monte-Carlo simulation is used to predict the electrons density's radius, using information regarding the substrate to be patterned on etc. The software has other options to target where features are patterned so they are only in the centre of the patterning field. This is crucial for the highest resolution features of the design as the centre of the 1 mm field gives the best resolution patterning. Although the software can help to prevent any stiction issues where two different 1mm fields overlap to prevent any areas not being exposed properly. It also allows for options to heal the design to prevent any designs that have overlapping patterns so they do not receive double the dose.

Once an output file from the design has been generated, two separate files are produced that describe; (i) the beam condition for the tool (ii) placement of the design files on the chip (iii) the base dose to be applied (iv) the variations in the dose for each design. This allows for a dose test to be created by writing the design into an array and varying the dose for each step of the array. For example an RIE etch of a graphene nanoribbon can be done by making the design repeat in a row and with each step the dose varies by 50 uC/cm2 from 50 to 300. After the resist is developed, the resist or the etched graphene can be imaged to analyse which dose gives the closest to the desired design.

Resists that have been tested:

1. PMMA 495 and 950- The most common resist used for e-beam. It is a positive resist with a very fine control of the thickness, with a high resolution of 10nm that can be achieved with fine tuning. PMMA is used for both graphene patterning and metal lift off. Although PMMA is most convenient to use it is not very selective against dry etching. Except in the case of graphene.

2. MMA - A positive resist typically used in a bilayer with PMMA for lift-off patterning. Since it requires a significantly lower dose than PMMA to expose an undercut is created. This makes the lift off process easier.

3. ZEP 520A- A high resolution positive resist, that is used when a high etch selectively is needed.

4. HSQ 2% and 6%- A negative resist which is referred to as spin on glass. Its structure more closely resembles silicon dioxide than a polymer. For graphene it can additionally be used as a spin on dielectric. The resist is very sensitive and is capable of producing 10 nm features. The best dose needs to be tested for each new bottle of HSQ.

3.2.2 Reactive Ion Etching

RIE is used in the semiconductor industry to etch vertical sidewall patterns into materials, with advantages over wet etching for its isotropic rather than anisotropic (crystal orientation dependent etch). RIE is less dependent on the chemical used to etch, which can be both an advantage and disadvantage of the system. RIE works by generating a plasma in a vacuum chamber using a strong RF field between two parallel plates that ionizes the gas in the chamber. On one of the plates rests the substrate which is charged negative so that once a plasma has been generated with positive ions they are directed towards the substrate. The kinetic energy of this collision is enough to physically remove material by a process called sputtering. If a chemically reactive gas is used in the chamber it will also react with the material to give a chemical etch as well. A combination of these two etches in the RIE is used to etch silicon and oxides. For graphene a very weak plasma is used to remove the graphene by sputter etching rather than chemically. In this work a Oxford Instruments RIE80 is used to etch graphene. Only a 30 second etch at 30 W with 25 sccm Ar and 5 sccm O2 is needed to remove a monolayer of graphene when using exfoliated graphene.

3.3 Characterisation of graphene

3.3.1 Helium Ion Microscopy

Helium Ion is a powerful tool for both observation and fabrication. It works by passing Helium gas in a low pressure and temperature chamber, over a metallic tip that ionizes the Helium by an electric field [100]. The tip is formed into a pyramid and the end goes down to 3 atoms (a trimer) where the electric field is strong enough to ionize. The ions then swept up by focusing fields and beam limiting apertures to impact with the sample. The impact generates secondary electrons and scattered helium ions, which are then detected. The obtained images using secondary electrons are much more detailed that what is capable with scanning electron microscopy. Due to a probe size of 0.25

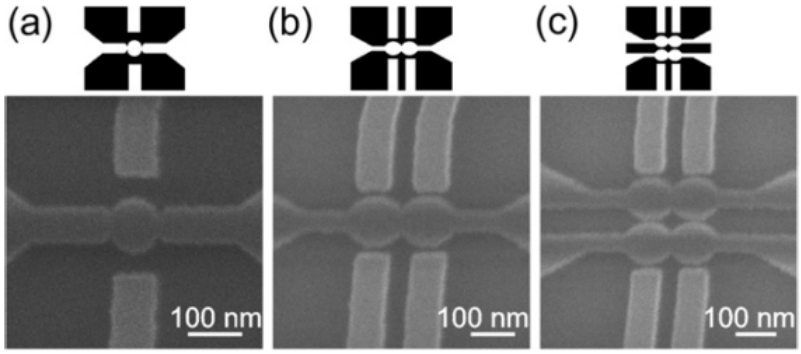

Figure 3.5: Quantum Dot structures made from graphene and milled by Helium ions [22]

nm, as the ions have a much greater momentum than electrons [22], making a <1 nm edge resolution possible. Another option is detect the scattered ions, which is useful for detecting material information where the ions level of scattering is related to the atomic number of the material that is being scanned. The power of Helium ion for imaging is further increased when the material undergoes charging, such as dielectrics or organic materials. It is possible to image the surface by flooding the positively charged material with electrons, making the material visible.

The high resolution of HIM provides a route for milling with accuracy down to sub 10nm [101]. In particular for graphene nanoribbons have been routinely fabricated down to 5nm widths when suspended. Single electron transistors and quantum dots have been fabricated with sub 10nm separation distances on silicon dioxide [22], which can be seen in figure 3.5.

Ion bombardment of the sample, however, causes damage to the sample easily inducing defects in graphene [102]. This creates difficulties in creating pristine GNRs, along with the fact that edges are terminated in a rough manner. Another issue in fabrication is the cleanliness of samples, is if there are hydrocarbons on the sample and in the chamber the focused ions could cause deposition to occur [22]. Care has to be taken when milling graphene on silicon to prevent blistering. This is where Helium ions are deposited onto the surface, obviously ruining any milling being attempted.

HIM remains a powerful tool for fabrication, not just for milling. It is, even possible to deposit and etch metals and use typical plasma etchants to target the location [101]. Plus lithography of e-beam resists such as HSQ or PMMA have been demonstrated with resolutions similar to e-beam without the need for proximity error correction. In this work a Zeiss Orion HIM is used mainly for imaging graphene due to the higher contrast and edge resolution provided over standard SEM. While some preliminary investigations into the exposure of graphene with HIM is investigated in Chapter 5 to determine the feasibility of milling suspended graphene devices.

3.3.2 Electrical Characterisation

Initial testing was done at room temperature to determine the best chip for determining the CVD-graphene nanoribbon characteristics was conducted using the MEMS prober system at the University of Southampton. When using a probe station to measure the devices the pad contacts did not adhere strongly to the graphene. Causing the contacts to scratch away with repeated measurements of a device, this would limit the lifetime for the number of possible repeated tests that can be achieve with these devices.

The rest of the electrical characterisation was conducted at the Japan Advanced Institute of Science and Technology (JAIST). This meant there was a limited period of time to test the devices at low temperature. To ensure the testing time of the devices was maximised, an initial test was carried out at 110K with the vacuum probe station. The minimum temperature it could achieve was 110K, because this system used liquid nitrogen to cool the system. This first test was used to find the best working devices, as the yield was quite low. The 110K was necessary to ensure optimal performance of the graphene devices was achieved to highlight the desired devices for testing. For most devices only quick Id/Vd and Id/Vg were used to find working devices. The sheer amount of devices that needed to be tested created a limitation in the amount of time to test.

Once the yield and best working devices had been done the chip was loaded into the cryo-probe station down to 5/10K. The probe station used was a "Grail 10-308-X-4K-LV" system from Nagase Techno-Engineering Co Ltd. An Agilent B1500A was used for the electrical measurements of the devices, in particular any stability diagram measurements, because the Agilent was found measure with the most data points. When loading into the cryoprobe station the devices were quickly retested to find if any devices had been broken in the cool down. Fortunately, the switch between the two tools did not create any significant issues in breaking many devices. It was decided that although the devices were found to be working. The issues in loading between two tools, meant any future testing for devices should be done immediately in the cryo-probe station.

3.3.3 Raman Spectroscopy

One of the most widely used and important methods for characterising graphene is Raman spectroscopy as pioneered by Andrea Ferrari [24]. It is one of the most capable tools for determining both the structural and electronic quality of the graphene sheet, while also being a fast and non-destructive method. Raman spectroscopy works by exploiting the inelastic scattering of a photon (Raman scattering). Typically when a photon encounters an atom or molecule it is elastically scattered and has the same energy and wavelength as the incident photon. There is a small percentage of photons that when scattered produce a frequency shift due to the interaction with the particular phonon energy of the associated atom or molecule. By measuring the decrease in the frequency compared to the incident photon (Stokes shift), information about the material can be

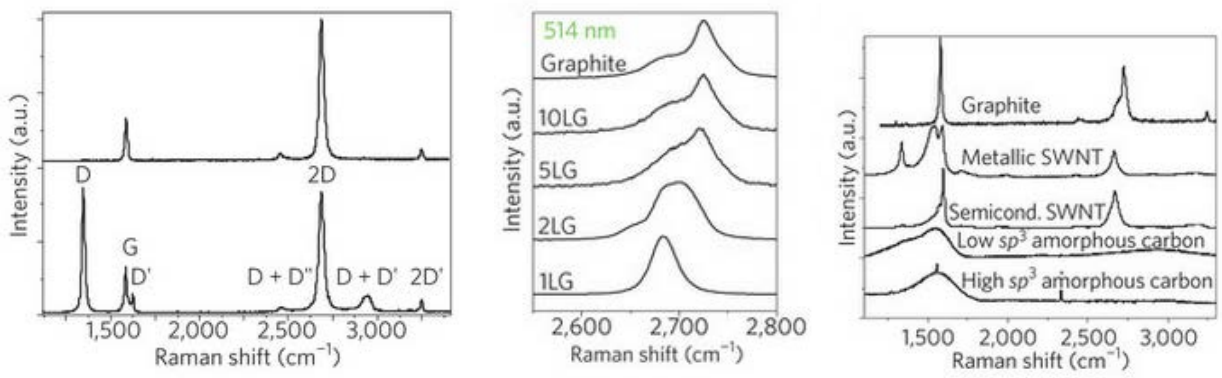

Figure 3.6: Typical Raman Spectra of graphene measuring the shift from 3500 $cm^{-1}$to 500 $cm^{-1}$and the labeled points of a defective graphene sample (below). Raman spectra of graphene with increasing number of layers (left) and different materials (right) [23, 24]

found because of the unique signal that is related to a very particular type of atom and its bonds [23].

One of the only downsides is the small amount of significant data points given by the resulting spectra. For graphene it typically has only 3 major points and sometimes up to 6, whereas Diamond only has 1. With these points though a large amount of information can be determined, such as defects, doping level, edge type, strain/stress or oxidation. For example the D peak only appears when there is defects in the graphene sheet, increasing in intensity the more defects there are. The ratio between this peak and the G peak is used to qualitatively find the quality of the graphene sheet. Even the number of layers of graphene can be found by a broadening of the 2D peak due to an increase in the peak width and shift of the multiple peaks that occur at the 2D peak. Another is that the high doping of graphene can be seen by a increase in the intensity of the G peak due to the suppression of any destructive interference occurs in pristine graphene. See figure 3.6 for the typical Raman measurements made for a pristine and defective graphene layer and the differences between different carbon materials.

Raman spectroscopy is a rather complex phenomena to understand in detail when trying to determine from the resonant phonon states and electron wave vectors the relevant cause of the particular spectra peaks. Fortunately it can be quite simple to understand when considering the cause and effect of the shift and intensity change of the peaks in relation to each other. This is why for most analysis of graphene the change in the D peak intensity and if there is multiple layers is usually the only concern to determine the quality of the graphene. Especially with Tip-Enhanced Raman gaining more interest in the semiconductor industry to analyse the quality and dopants approaching a single atomic level makes it one of the most important tools used.

In this work a InVia Raman spectroscopy tool is used to investigate the quality of the graphene sheet using a 532 nm laser, with cosmic ray removable and 3 accumulations of 10 s each to obtain accurate data on the quality of the graphene.

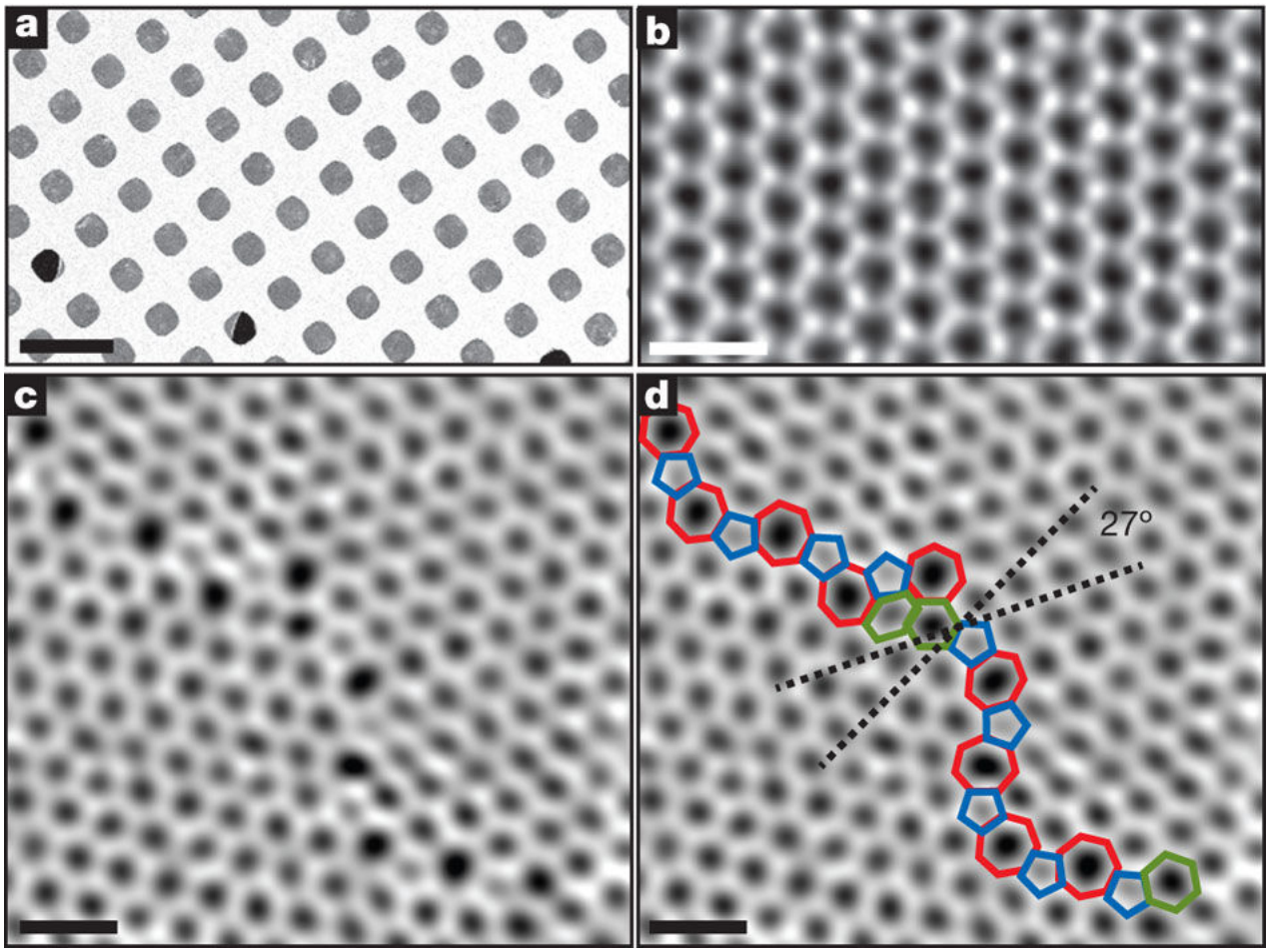

Figure 3.7: STEM image of the structure of a monolayer CVD-graphene sheet with defects across the sheet. [25]

3.3.4 Scanning Transmission Electron Microscopy

Scanning transmission electron microscopy (STEM) with aberration correction provides a method to image the crystallographic structure of graphene, so that the location of individual atoms in the graphene sheet can be identified. STEM works by detecting the diffraction of electrons when it passes through a thin layer of material. As the electron beam is scanned across the sample the interaction with the atoms electron shell enables detection of the crystal structure of materials. An example of the high quality crystal sheet obtained using STEM for graphene is shown in figure 3.7. In this work a JEM-ARM200F at JAIST university is used to collect the information on the crystallographic structure of graphene with increasing exposure to helium ions in Chapter 5.

3.3.5 AFM

AFM is a technique used widely to obtain surface profiles of materials in nanometre resolutions. By passing a very fine nanometre sized tip (~10nm) across the surface of a material it is attracted at first by the Van der Waals force and when the distance it close enough the electron clouds in both the tip and material repel each other causing an up

& down displacement of the tip. This displacement can then be accurately measured using a laser reflecting off the beam of the AFM tip, by measuring this reflection with a detector the information can be fed back into the system for finer control. This high nanometre resolution of measuring the displacement is accurate enough to detect the step change between individual layers of graphene.

In this work a Veeco Multimode V AFM is used to investigate the surface roughness from graphene transfers using the tool in a tapping AFM mode. This gives accurate surface information and post processing using Gwyddion provides the analysis of the roughness and 3D diagrams produced in this work.

Chapter 4

Development of process for integrated suspended graphene devices

4.1 Introduction

While most graphene devices produced so far involve transferring graphene onto flat substrates [1]. The process for producing such a device requires several fabrication steps. First the transfer of graphene onto a substrate then device etching followed by contact deposition. Each fabrication step introduces defects into the graphene sheet and degrades the electrical performance, as established in chapter 2.

A novel approach for fabricating devices would be to swap the typical process order. This can be achieved by transferring graphene onto substrates with patterned electrodes. This skips the final step by producing the contacts first. Reducing the number of processing steps on the graphene sheet. This technique has been coined as a “transfer-last” method. It is transfer-last because the crucial aspect of transferring graphene has been left to the last feasible step. Although the process could also be called a "contacts-last" process.

The transfer of graphene onto a patterned substrate enables unique contact materials to be explored. Materials such as silicon or carbon composites that are impossible to deposit onto a graphene sheet. Additionally, the transfer onto patterned electrodes would enable the suspension of graphene automatically. This can be achieved by patterning the electrodes below the critical dimension for the capillary force to pull the sheet to the surface. The transfer-last method creates opportunities for integration with silicon technology to be explored. Enabling graphene and silicon hybrid devices that are CMOS compatibility.

The current state of the art for graphene devices using the transfer-last method has been achieved by 3 distinct works. The first is the suspension of graphene over metal gate

electrodes. By using the exposure of a resist beneath the graphene and a dry solvent release to suspend the graphene [68]. This demonstrated the ballistic interference patterns in graphene. Proving the high quality of devices made by suspending graphene and the impressive electro-optical properties of graphene. The second is the first tunnel FET made using graphene, where a triple buried gate structure is used [82]. This is a significant first step in producing an alternative logic device with graphene creating a lateral tunnel FET by exploiting the electrostatic doping control of the sheet. The transfer-last in this process is achieved by using chemical mechanical polishing to smooth the buried gates, rather than fabricating multiple gates on the graphene surface. Lastly, is the demonstration of the potential behind the transfer-last method by IBM [32]. The overall performance of a graphene analogue circuit was increased using this method, which created the highest performing analogue device so far.

The work in this chapter focuses on the development of the transfer process to fabricate graphene devices on patterned nanostructures. First, the improvements made to the original transfer process used in literature is presented, where the key aspect of this development is the focus on achieving a wafer scale transfer of graphene that is considered electronic grade. Once a sufficient transfer process has been achieved the process is used to create suspended graphene with the transfer-last method on patterned electrodes. Patterned structures made of gold, nanocrystalline graphite (NCG) and silicon are explored. Gold electrodes are investigated due to the high conductivity and use in Back-end-of-line fabrication. This enables a method of directly contacting graphene without a buffer layer metal (such as titanium). Silicon is investigated for the use in Front-end-of-line fabrication for integrating graphene in future hybrid devices. Also desirable for the ease in manufacturing dense nano-structures. While NCG is of most interest for the direct carbon-carbon interactions of the same sp2 bonded carbon structures. This opens up possibilities for creating electrode contacts without any detrimental doping of the graphene. The exploration of these three materials will enable the future investigation of graphene suspended devices with minimal fabrication induced defects.

4.2 Improvement of the transfer process

4.2.1 Initial transfer method

CVD-graphene provides the best method of producing wafer scale graphene that can approach the quality of exfoliated graphene without the high costs of using SiC. The graphene has to achieve a transfer onto a target substrate with a large continuous sheet, this is referred to as achieving a large area transfer. The key properties of a large area transfer should have minimal cracks and wrinkles in the sheet (folded graphene from the transfer). For the CVD-graphene to be considered electronic grade is should have minimal residue and defects in the sheet. This is evaluated by observing the samples under optical microscope, AFM, and Raman spectroscopy. The optical images are used

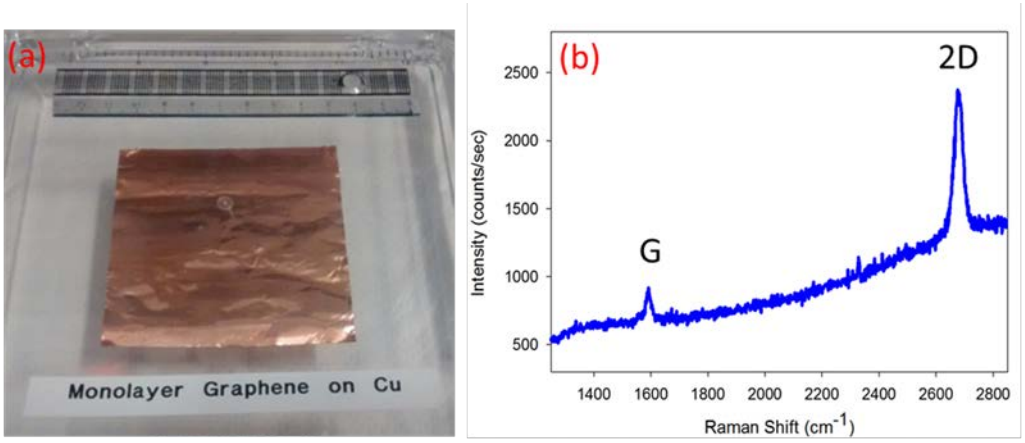

Figure 4.1: (a) Graphene on a copper foil with a 80mm x 90mm size. The wrinkles and creases on the copper (red arrow) will affect the graphene transfer (b) Raman spectroscopy results of the graphene on the foil. The curve in the graph is caused by the copper foil. Significantly though the quality of the graphene is pristine on the foil. This is indicated by the lack of a D peak at the 1350 cm^{-1} mark.

colloquially to evaluate the graphene. AFM is evaluated using average roughness and average mean thickness of each sample and Raman is evaluated using the peak widths and the ratio between the D/G peaks and G/2D peaks. The reason for evaluating using these factors has been described in chapter 3.

CVD-graphene is produced in a collaboration with the Novel glass group in the Optoelectronic Research Centre [ORC]. A CVD chamber (built in-house) is used to grow various 2DMs. The quality of the graphene can been see in figure 4.1, demonstrating the high quality of the graphene before the transfer has taken place due to the lack of a D peak at the 1350 cm^{-1} mark. A PMMA supported transfer method was initially used for the transfer process. Historically the PMMA mediated transfer method was considered the standard method for transferring CVD-graphene.

For an initial evaluation of the in-house CVD-graphene it is compared to graphene produced commercially by iTRIX (now Graphene platform corporation). The Raman spectra indicates a much higher quality graphene, seen by the smaller D peak in figure 4.2. The graphene completely covers the full 1 cm^2 chip sent by iTRIX. Although there is still tears and cracks in some areas across the chip, indicating the transfer process is not sufficient commercially yet either. The AFM images show wrinkles on the 2D plot and the 3D plot highlights the large particles on the surface (figure 4.3). This indicates of quality graphene after the transfer process that needs to be achieved before device fabrication can be started.

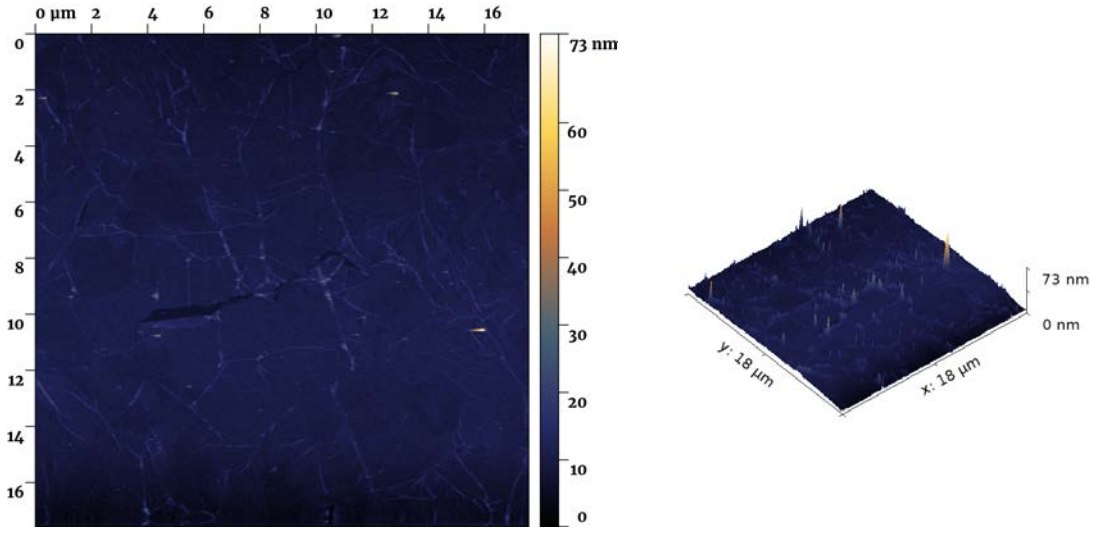

Figure 4.3: AFM images from the commercial iTRIX samples across a 17 x 17 μm area. Left is the 2D image which shows the wrinkling of the graphene sheet that occurs from the transfer of the graphene and cracks that form resulting in folded areas of the sheet. Right shows 3D image to illustrate the height of the residue and smoothness of the sample. The average roughness measured across a 15 x 15 μm area to give an average roughness of 1.378 nm and average mean thickness of 9.634 nm.

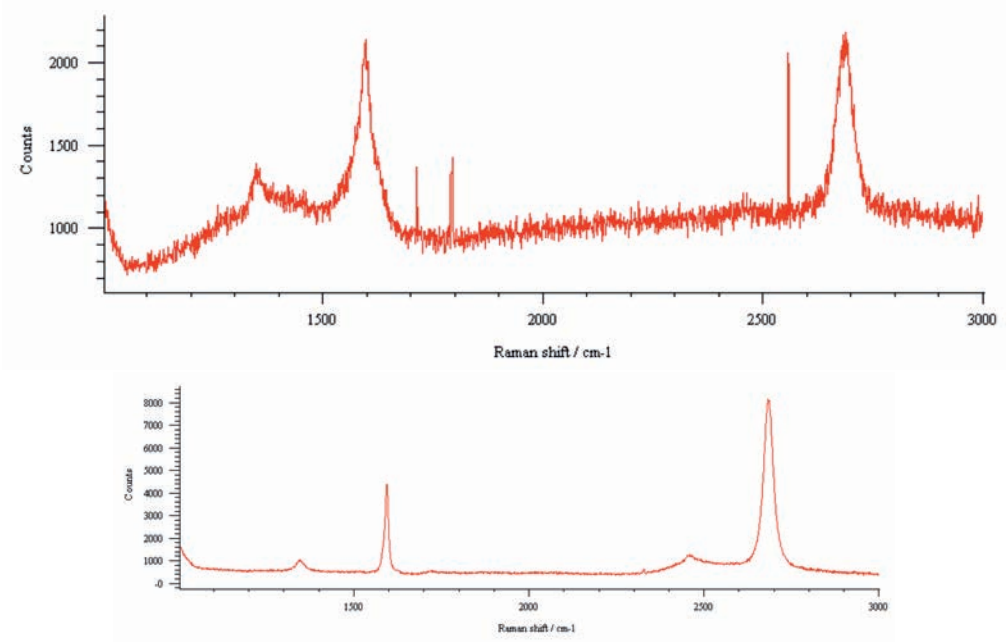

Figure 4.2: Raman spectroscopy results after a graphene transfer. Top represents the results from a transfer using the in-house CVD graphene. Bottom is the results from a CVD graphene sample produced by the commercial company iTRIX. The difference in counts is due to a difference in method used with the Renishaw inVia tool. The crucial points are the difference in the D peak (1350 cm^{-1}) and the G peak (1600 cm^{-1}). The in house graphene has a G/D ratio of 1.69 while iTRIX has a ratio of 4.09. The 2D/G ratio is 1 for the in-house and iTRIX is 1.93.

The basic process for a graphene transfer is described below. This follows the method described in [103] to use a PMMA mediated transfer method, where the PMMA is used as the adhesion layer to give support to the graphene (and visibility) when the copper is

etched away using a liquid etchant.

1. Carefully cut 50 x 50 foil into desired sample size. Tape down the edges on a 4" glass wafer.
2. Spin coat PMMA 495 at 2000 rpm for 60 seconds.
3. Leave to dry overnight.
4. Peel off tape, flip graphene over with PMMA side facing down and tape edges again.
5. Etch in RIE80 for 30 seconds at 50 W in 100 mTorr pressure. A gas mix of Argon and Oxygen flowing at 80 sccm and 20 sccm respectively.
6. Create a mix of 20g/100ml of Ferric Chloride and pour into an etchant tank.
7. Place etched foil side down on top of etchant solution, ensuring the foil floats on the surface.
8. After 6 hours the copper should have etched away, leaving a graphene/PMMA film on the surface.
9. Prepare a Petri dish with deionized water.
10. Using a watch glass, gentle scoop the graphene with some etchant so that it still floats on some solution. Do not let the graphene stick to the watch glass it might break apart or damage the sheet.
11. Transfer to a tank with DI water and repeat this process 2 more times.
12. Lift the target substrate using tweezers at an angle underneath the graphene.
13. Leave sample to dry overnight.
14. Strip the PMMA in acetone overnight.

Despite claims, this method produces a large area transfer of graphene it was rarely possible to achieve this. Figure 4.4 shows the best of the first batch of transfers, where the graphene produced shows the different detrimental defects that occur. Even in the area in the top left that appears to be a large clean area the quality from the Raman was still insufficient. This is seen by the Raman spectroscopy above used to compare to the commercial sample. To improve the reliability of the transfer process several changes are made to the original process; so a large area transfer can be consistently achieved.

Improvements to step 1:

The first change that improved the reliability was to alter the cutting and taping down of the foil before spin coating. The current first step in the process created lots of wrinkles

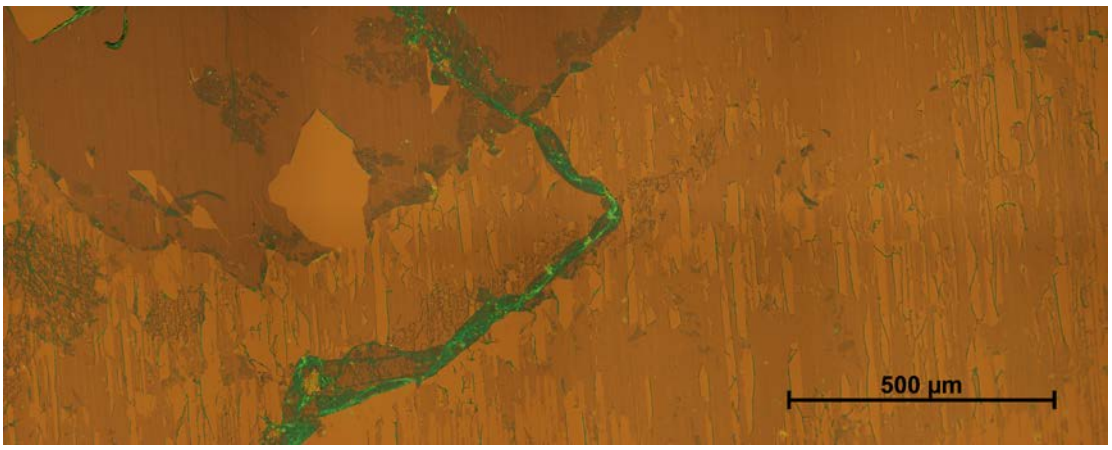

Figure 4.4: Graphene transfer onto a large area with significant cracks and wrinkles formed on the sheet. Although the area in the top left shows a clean uniform area of graphene the Raman spectroscopy revealed the graphene was highly defective and not considering good enough for electronic grade devices.

that would form on the foil, so when spin coating the wrinkles prevented a uniform layer of PMMA coating the graphene. This decreased the mechanical support of the graphene during the copper etch. This was caused by the handling of the foil when both cutting and taping down onto the glass wafer.

To overcome this a minimal approach in handling the graphene until it is protected by a PMMA layer is used. This was made possible by an improvement in the growth process in the LPCVD tube. A larger diameter tube was used that means a larger sized Copper foil can be used to grow graphene. The new size of the sheet is roughly 100 x 100 mm which fits perfectly across a circular 4" glass substrate or across a 6" silicon wafer. While the foil is now rested on the wafer another glass plate is then used to press down on the foil to flatten the foil down. The corners are then folded down around the glass wafer before taping the corners down. This solved the first issue of a non-uniform PMMA layer being spin coated onto the wafer. The image of the copper foil after spin coating can be seen in figure 4.5.

Improvements to step 2:

The PMMA 495 that is used to coat the foil was still mechanically unstable. During some etches the polymer layer would disintegrate ruining a transfer. It was found that PMMA 950 (a more dense version) gives much more support than PMMA 495. This requires a much higher spin coat rotation speed at 4000 rpm to get a similar thickness of 200 nm. Previously the graphene was left to dry overnight but to improve the efficiency of the process the PMMA is cured at 60 C for 10 minutes. Initially, this wasn't done out of concern the graphene would bond too strongly to the PMMA. So when stripping in acetone the graphene would be removed as well because it was not bonded to the silicon dioxide as effectively. By reducing the temperature down to 60 C (a third of the recommended baking temperature) this problem can be circumvented.

Improvements to step 5:

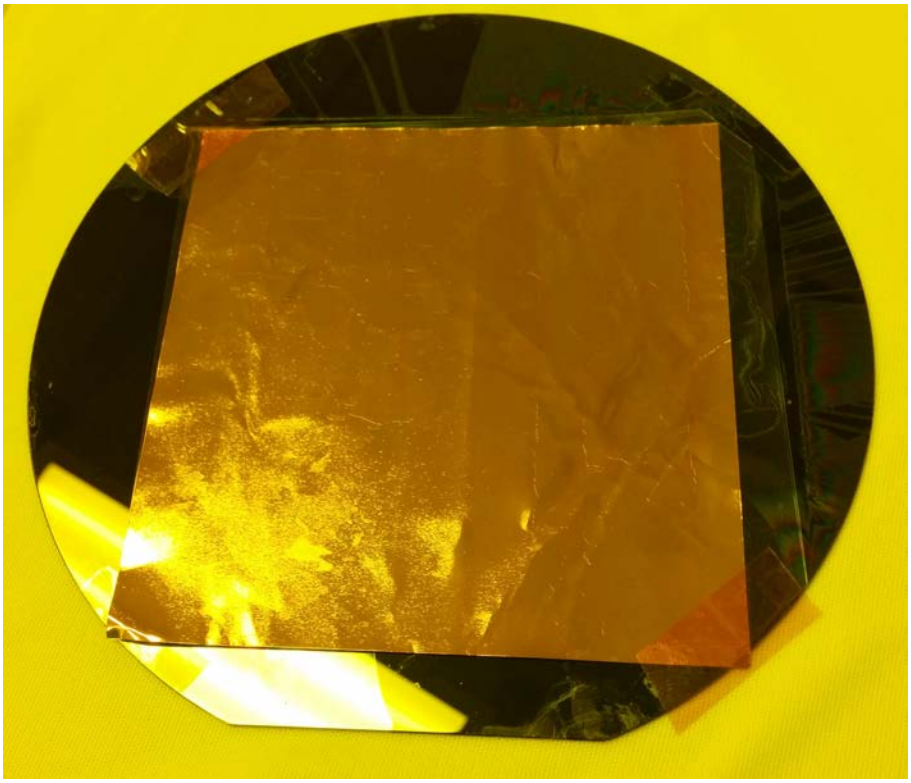

Figure 4.5: Photograph image of the 4 x 4 inch copper sheet taped down onto a silicon wafer after spin coating. The Kapton tape can be visibly seen on the corners or the copper foil in the centre. The foil itself is still smooth although some uneven areas can be observed in the bottom right corner of the foil.

It was found that etching the backside of the copper at 50 W had a damaging effect on the polymer and graphene. Despite only the backside of the copper exposed to the plasma the samples at this power did not yield large area transfers consistently. At first, this step was skipped from the process and had the positive effect of improving the transfer as seen in Figure [figure:RIE of backside Cu], where a large area transfer with no cracks and wrinkles can be observed across a 100 x 100 um area. However, it is important to do the RIE step. Otherwise, the uncoated graphene on the underside breaks apart from the etchant solution and redeposited onto the coated graphene. This leaves tendril-like structures on the graphene sheet. Another factor when RIE is the power of the plasma. This meant the RIE step had to be reintroduced but with a lower power of 20 W., this was sufficient to etch the graphene without causing damage to the resist.

Improvements to steps 6 to 8:

At first ferric chloride was used for most of the etches since it is regularly used in literature for the transfer process. Unfortunately, the ferric chloride used etches the copper too quickly and can degrade the quality of the transfer if left in contact with the graphene too long. This was first confirmed by using iron nitrate to etch the copper instead and reduced the number of cracks and wrinkles observed. This is the etchant that was used to obtain figure 4.6 when no RIE was used. Eventually, the iron nitrate was exchanged for ammonium persulphate solution. This etchant was selected at first because it is com-

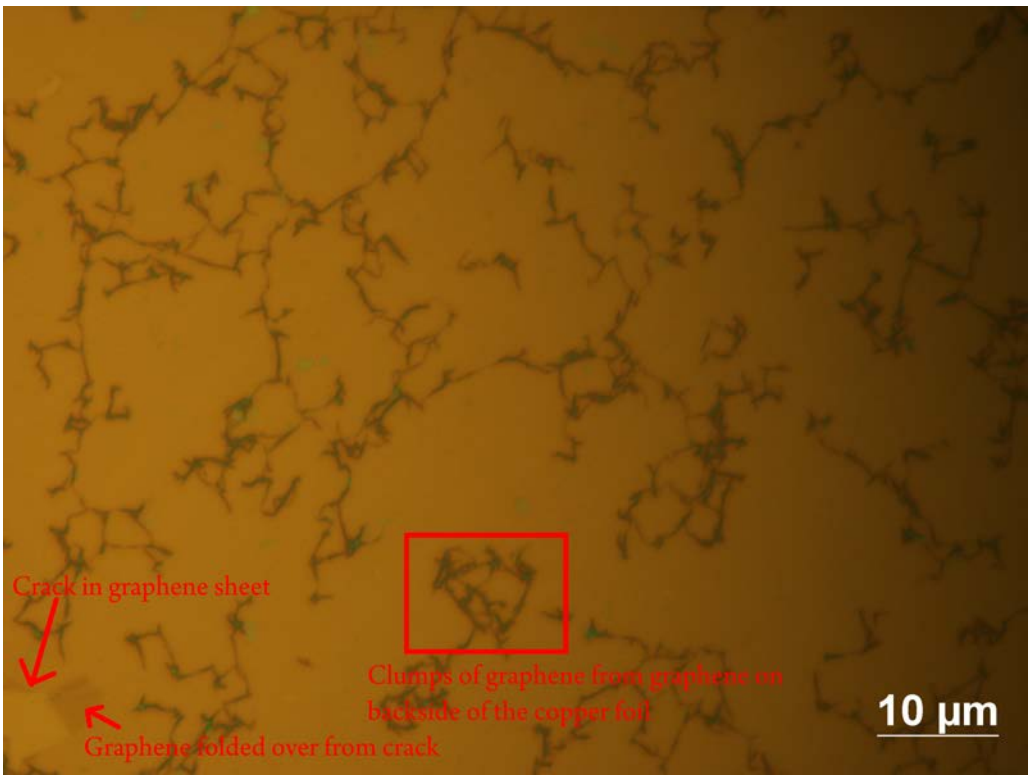

Figure 4.6: Effect of not etching the backside of the copper foil in RIE. The contrast between the graphene sheet and the substrate can be seen from the crack in the corner. The graphene is uniform across the 100 μm area of the image . The graphene that is redeposited during the copper etch is highlighted in the red box. The tendril like formation is spread across the entire sample.

monly used in the production of printed circuits boards after the industry swapped from ferric chloride. This chemical was found to etch the copper in under 2 hours without affecting the graphene sheet and subsequent transfer.

Additional cleaning step:

The paper "modified RCA cleaning of graphene" showed a complicated procedure to clean and transfer graphene. This required a few more steps to produce a clean graphene transfer with minimised cracks and wrinkles. This would have involved a complicated set up for the post copper etch clean and meant handling the delicate graphene/polymer stack more. However, it was discovered the process can be simplified by including a Hydrochloric Acid cleaning step, where a 30% concentrated HCl is used to clean the graphene for 2 minutes. This was beneficial in removing any particulates that could have been leftover from the copper etch.

Final word:

By improving these steps for the transfer, the process has created a more reliable method for achieving large area graphene. With additional improvements in drying the sample on a hot plate at 50 C for 5 mins and stripping the resist in acetone for 1 hour meant the transfer time is reduced. Originally a full transfer process would take 2 days to achieve but can now be done in half a day.

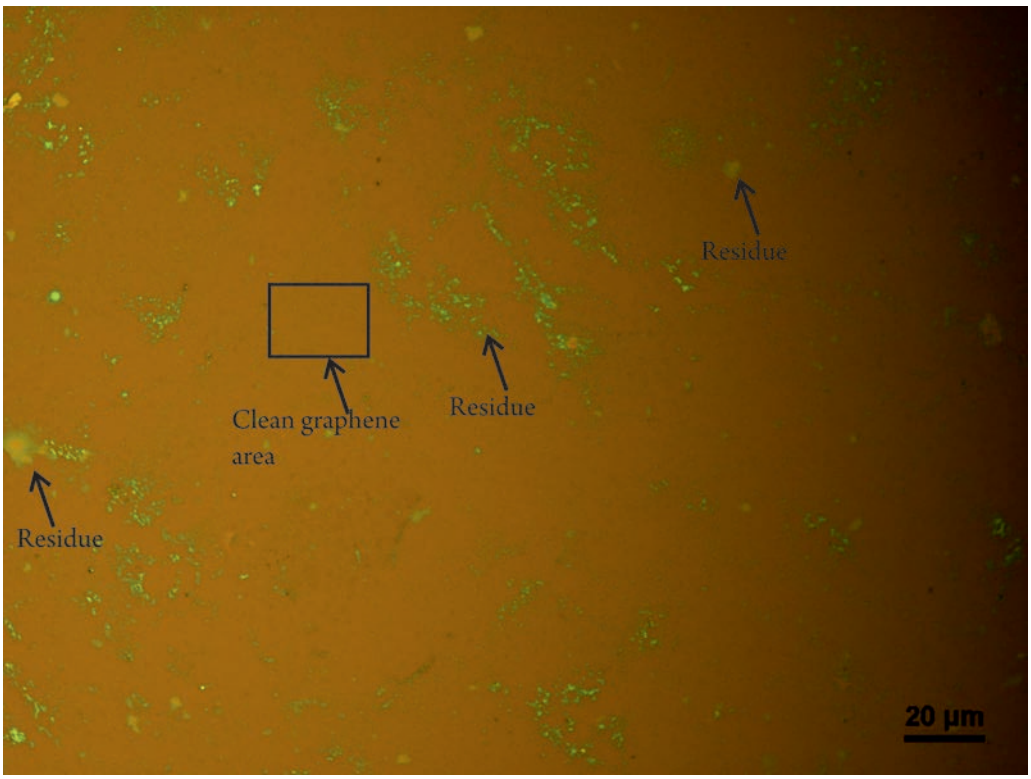

Figure 4.7: Optical microscope image of a graphene transfer achieving a large area transfer with no distinctly visible cracks or wrinkles across the 250 um area. Although the process is robust enough to produce large areas there is significant residue observed on the surface, as highlighted in the image.

4.2.2 Reducing the Surface Residue

The majority of these initial improvements focused on the reliability of transferring graphene onto a substrate to achieve a large area transfer. What these improvements do not improve upon is the contamination from residue left on the graphene sheet as seen in figure 4.7. As has been established in the Chapter 2 the polymer residue acts as scattering points and causes unintentional charge transfer doping on the graphene surface. To have an electronic grade CVD-graphene the residue must be reduced further.

4.2.2.1 Post transfer cleaning of graphene with acetic acid

The first method investigated to remove PMMA residue was to add an extra step into the process after the transfer. By using acetic acid the residue is attacked and the graphene quality is improved [104]. AFM and Raman data confirms this in figure 4.8. Acetic acid is a organic acid more commonly known as pure or undiluted vinegar. The best method found though has been to use the glacial acetic acid for 1 hour, any longer and the graphene becomes damaged or oxidised. The AFM data taken from this method shown in figure 4.9 give a average roughness of 24 nm and average mean thickness of 92.78 nm after acetic acid clean.

Unfortunately, there has not been many other chemical solutions that can remove the PMMA residue on graphene without any damage or modification to the graphene. An

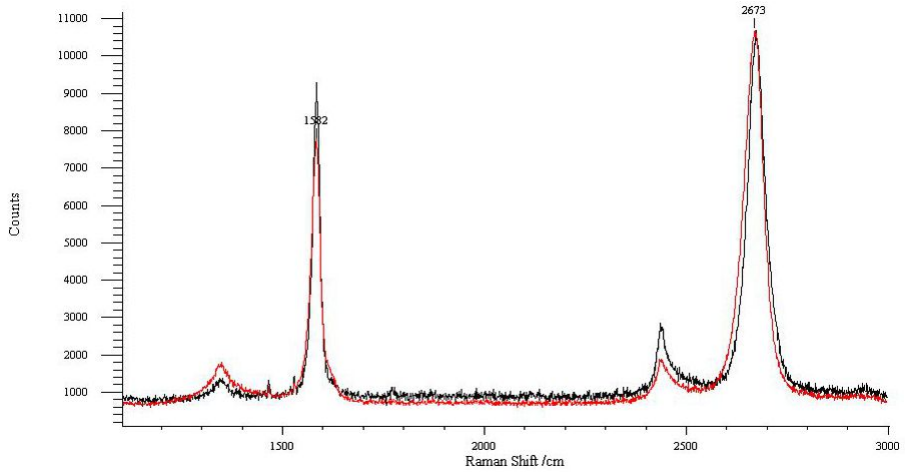

Figure 4.8: Raman spectroscopy of the graphene before (red) and after 1 hour of acetic acid (black). The acetic acid caused the peak to narrow for the 2D peak and the ratio between the G & D peaks shows a decrease from 4.2 to 6.7. Both are already higher than the commercial sample ratio of 4.09. The 2D/G ratio is 1.12 before clean and 1.37 after the clean.

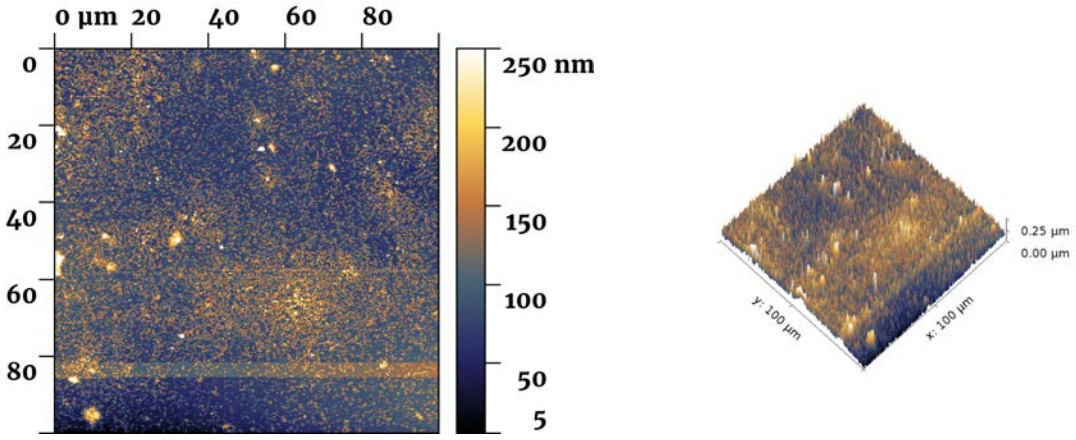

Figure 4.9: AFM image after acetic acid clean from a 100 x 100 μm area. Left shows the 2D image and right shows the 3D image. The sample can be seen to be very rough compared to the iTRIX sample with an average roughness of 24 nm and average mean thickness of 92.78 nm.

alternative would be to use the modified RCA1 to remove organics, but this has not been tested due to facility restrictions. Further restrictions apply to the annealing graphene in a furnace, where this is commonly used for exfoliated graphene. However due to the possibility of copper contamination with the CVD-graphene this was not possible to attempt. So far this limits the cleaning of graphene after transfer with acetic acid, which has had a minimal improvement on the graphene properties.

4.2.2.2 Thin PMMA exposed by UV

Rather than use a post transfer clean which removes the residue after the transfer an alternative is to modify the PMMA after spin coating on the graphene. Since PMMA is sensitive to Deep UV (DUV) wavelengths of 248nm, the PMMA can be weakened by exposing to UV. PMMA 495 is spun on to be 50nm thick, exposed to UV, and a thicker 400 nm PMMA 950 layer is spun after. A simple UV cabinet box with a lamp that covers the DUV spectrum is used to expose the PMMA for 2 minutes. After transfer the chain scission caused by the DUV allows the weakened PMMA to be removed with MIBK in the same manner it is used with e-beam development.

Although the PMMA was sufficiently exposed, the PMMA it is also heated up in the cabinet. This can unfortunately hardbake some of the PMMA onto the surface making it impossible to remove by currently established methods, leaving behind some microsized residue. Fortunately though, the nanosized residue that affects the graphene quality can be mostly removed or reduced in size. Overall the amount of contamination and size of the residue is significantly better than graphene without UV-exposed PMMA. Since the distance between the larger residue locations is quite larger it should not interfere with the fabrication of smaller scale structures where there is no residue. A UV-exposed PMMA can be used in the transfer process to produce a CVD-graphene sheet suitable for electronic applications. The results of the AFM investigation into the transfer method can be seen in figure 4.10, where an average roughness of 15.41 nm and average thickness of 95.29 nm is found.

4.2.2.3 Alternative polymer layer

Although UV-exposed PMMA can be used to produce a high quality graphene layer there is still a key issue with PMMA. Unfortunately the mechanical stability/robustness of PMMA meant a majority of the failed transfers could be attributed to this material. The delicacy required in handling graphene during a transfer could be attributed to this material, where many times attempts to transfer the PMMA/graphene failed due to the sheet breaking apart. It is for these reasons a material capable of spin coating on graphene with less residue on the surface and higher mechanical strength is required to progress graphene transfers further.

The reasons PMMA was used as the default material for graphene transfer was due to the chemical inertness, suitable bonding to a graphene sheet and widespread use

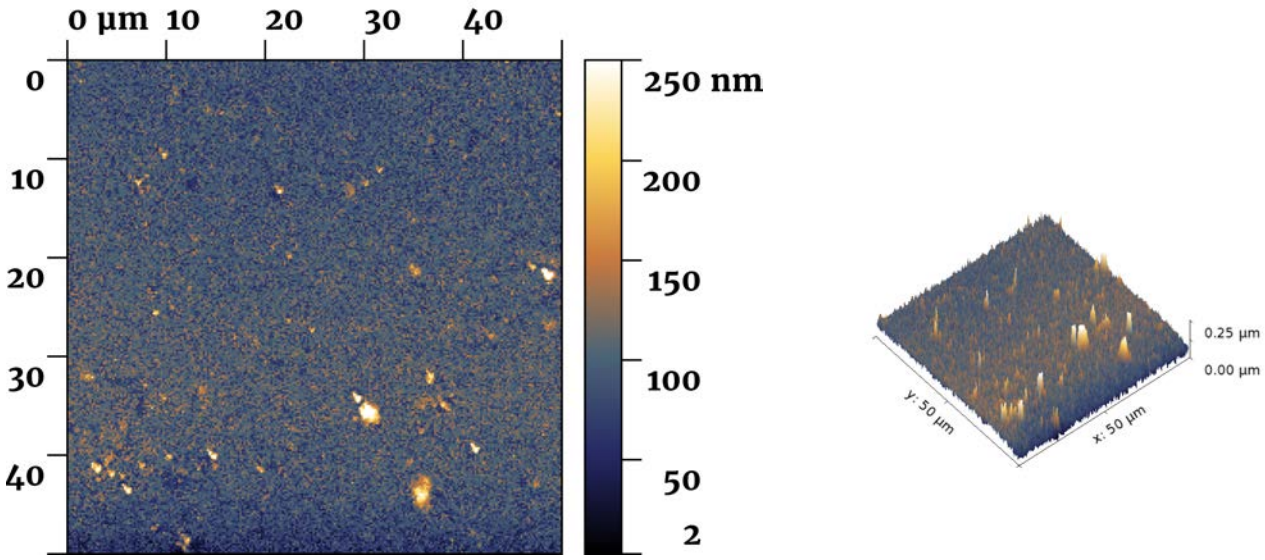

Figure 4.10: AFM images of the CVD-graphene using the UV expose PMMA method. The AFM analysis gives an average roughness across a 15 x 15 μm area of 15.41 nm and an average thickness of 95.29 nm

as a polymer. A replacement polymer must fulfil these requirements to be of use in the transfer process. Some alternative methods for transferring graphene have used Thermal Release tape, but is not as suitable due to the significantly higher residue than PMMA and higher complexities in handling over a standard spin coating & strip methods.

One alternative material that had been proposed in [98] was Poly Vinyl Butyral (PVB). The material was shown to have a higher mechanical stability than PMMA, while maintaining the other useful properties of PMMA. PVB is commonly used in shatter-resist glass as a safety measure for cars. The material is spincoatable produces less residue than PMMA overall and is removed by further diluting with its composite liquid such as ethanol. A benefit of the PVB over PMMA is it can be reflowed at temperatures below the glass transition point at ~60C meaning the PVB does not need to be cured to get the best performance. This can be attributed to the improved quality of the transfer; by a lack of residue due to the weaker bonding and less cracks and wrinkles.

The downsides to this material can be that the PVB is not always fully removed on some transfers. Leaving behind a 50nm thick residue that can only be removed by annealing of the PVB. This can be done at around 400C in N2, which is the point at which the thermal decomposition of the PVB reaches around 90 %. N2 has only be tested so far but it should be possible in forming gas too.

The quality of the PVB can be seen by a direct comparisons of its transfers onto silicon dioxide and when attempted to be suspended. The AFM (see figure 4.11) shows less roughness than the thin UV exposed PMMA layer method, with an average roughness of 11.7 nm compared to 7.7 nm for PVB method. Measured by taking a line roughness from one corner to the other on the AFM data. The average max heigh of the roughness is much lower for PVB by 20 nm. The AFM of the PVB compared to the thin UV exposed

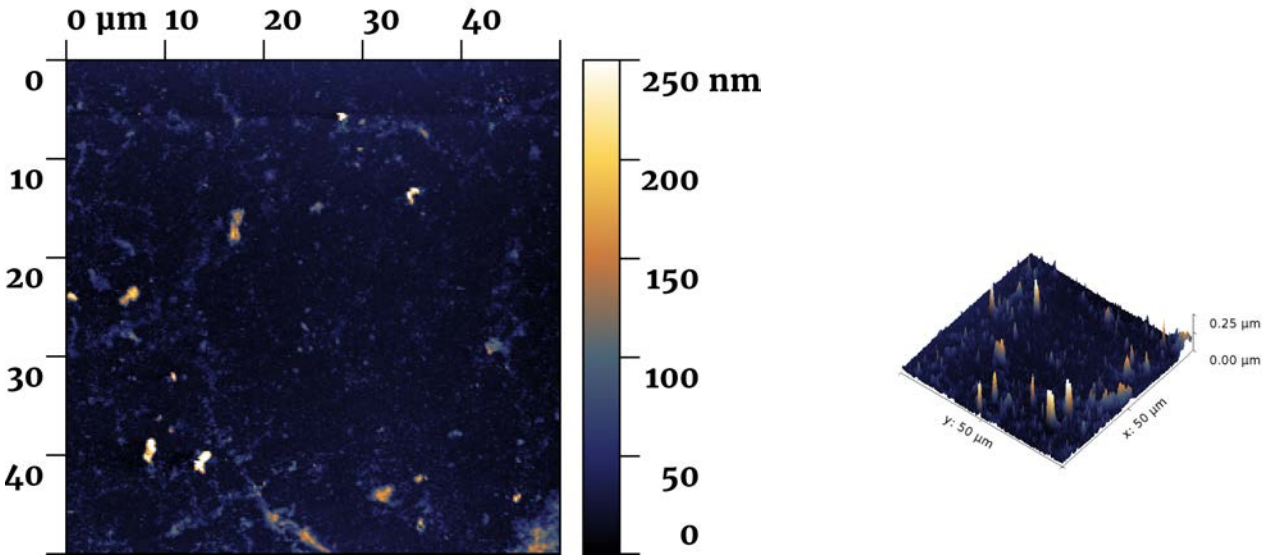

Figure 4.11: AFM images of the CVD-graphene transferred using the PVB method. The average roughness across a 15 x 15 μm area is now 6.643 nm and the average mean thickness is 21.04 nm.

PMMA does look much cleaner. Acetic acid cleaning was tried for the PVB too, however the AFM shows it increases the roughness making the transferred graphene worse. The Raman data in figure 4.12 shows an improvement of the G/D and 2D/G ratio of 5.7 and 2.51 respectively. Compared to the initial values of 1.69 and 1 for the G/D and 2D/G for the first transfers using the in-house graphene. While the commercial iTRIX sample had values of 4.09 and 1.93 for the G/D and 2D/G. This highlights the improvements that have been made in the transfer of graphene, with the ratio figures now higher than those previously obtained from industry.

PVB is not likely to be the best material that can be used for graphene transfer but it is so far the best thanks to its higher mechanical robustness, reduced amount of residue and improved graphene quality.

An ideal support material needs to -

- Have strong support but be flexible
- Be removed without any residue left on surface
- No cracks or wrinkles in the sheet

4.2.3 Summary

Initially the quality of in-house CVD-graphene was poor compared to commercial samples but has progressed to offering a quality greater than most commercial products; as indicated by the Raman spectra with a better 2D/G and D/G ratio. The key developments focused on improving the steps required for the transfer such an experimenting with different etchant compounds and the supporting polymer used. While other steps were improved by optimization through trial and error. One aspect that could not be quantified

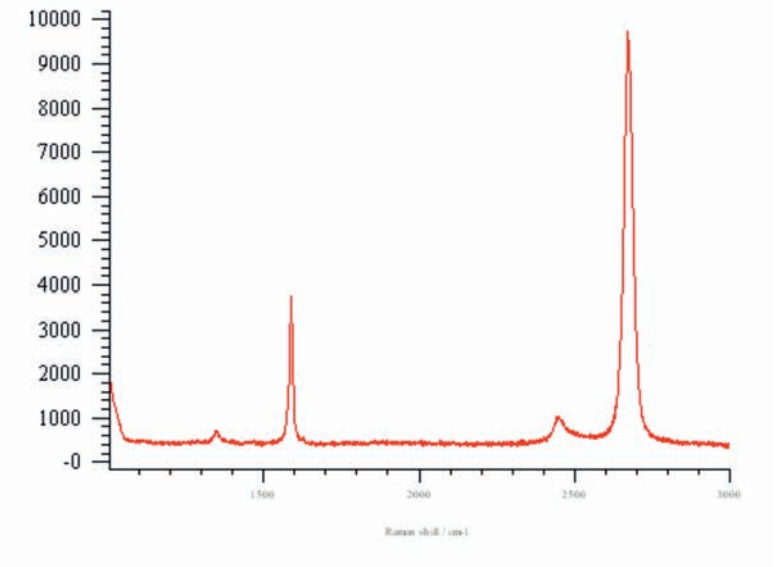

Figure 4.12: Raman spectroscopy of graphene using PVB transfer method. G/D ratio is 5.7 for this method. This is lower than the acetic acid clean but higher than the PMMA transfer method. The 2D/G ratio is now 2.51. This is the highest ratio achieved using any transfer method and shows a vast improvement over the commercial CVD-graphene. This is the same graphene that is used in the results of the downscaled CVD-nanoribbons.

during the development is the increase in skill the user had on handling CVD-graphene, where the end results of the improvement in the development can be attributed to better manual practices.

This leads to one aspect that further work needs to address to improve the process for transferring wafer scale CVD-graphene. For example automation of the transfer process will enable an increase in the quality of the graphene achieved with the transfer process. At the current stage this is not enough and creates an undesirable barrier to producing high-quality graphene sheets. Further minimization of the human interaction with the handling could be achieved by using a mechanical frame for clamping the graphene sheet during the etching procedure.

The development of the improved transfer process has enabled the production of electronic grade CVD-graphene, so the unique properties of CVD-graphene can now be explored, where the downscaling of CVD-graphene nanoribbons is investigated in chapter 5. The rest of this chapter focuses on the exploration of the CVD-graphene transfer process to produce suspended graphene with a transfer-last process.

4.3 Direct transfer on patterned electrodes

Contacting graphene at the nanoscale is still a major factor limiting the performance of electronic devices, where the same problem currently exists with silicon devices when using silicides and copper at decreasing dimensions it creates one of the major roadblocks facing silicon CMOS in the future, as highlighted in the ITRS report [30]. Arguably

the contacting of graphene for integrated devices at the nanoscale is a even greater issue due to the higher mobility than silicon. As seen in literature the metal/graphene junctions have been shown to be one of the major performance limiting factors for graphene devices, where the limitation occurs for graphene devices when contacted by conventional means so that graphene is trapped between two opposing materials. It is trapped between the silicon dioxide substrate and contact metal of titanium, chrome or palladium create additional effects such as charge transfer doping doping to limit the performance of a graphene device compared to a pure contact resistance issue.

The key to creating a high performance CVD-graphene device is to minimise the processing done on the graphene sheet, limit effects of charge transfer doping and extract the optimum properties from graphene. The usual methods to create a graphene device involve transferring graphene onto a silicon wafer with a 295 nm oxide before device patterning and metal deposition. The best way to achieve this would be to fabricate a suspended graphene device. This would remove the problems associated with substrate interaction and increase the achievable mobility for the device. As discussed in the introduction to this chapter the method to produce a suspended device does not need to follow the typical process. A transfer-last process can theoretically achieve a suspended device and be compatible with a CMOS process for BEOL integration. Figure 4.13 shows a simple process flow for producing a transfer-last CVD-graphene device.

The rest of this chapter focuses on the fabrication of CVD-graphene using the development of a wet transfer-last process, where the CVD-graphene is transferred onto a patterned substrate immediately after etching the copper foil, where the aim is to investigate the methodology of this process, at first when producing graphene using photolithography and then when transferring graphene onto different contact materials with decreasing gaps between contacts. Only by using CVD-graphene can this process be achieved with a modest simplicity, although exfoliated graphene can now be transferred onto target substrates the complexity involved makes this too difficult to be reasonably achieved. This enables the wet transfer of graphene for suspended devices without critical point drying or solvent release to be evaluated.

4.3.1 Transfer onto metal contacts using photolithography

The first evaluation of the transfer-last process to determine the viability of the process uses photolithography to pattern micron sized metal contacts and transfer graphene onto the contacts. The contacts are 10 um in width, 220 nm thick and separated by a 20 um gap using a lift-off process. The metal used the AJA Orion sputter system to deposit 20 nm of titanium and 300 nm of gold contacts. The most desirable metal graphene could contact using the transfer-last process would be gold. In the transfer-first process a contacting material such a titanium or chrome is deposited first as an adhesive layer for the gold to deposit onto. If the the titanium or chrome was not used the gold would not adhere to the surface of the material. This is necessary for even silicon devices and is the reason titanium is used as the first metal layer onto the silicon

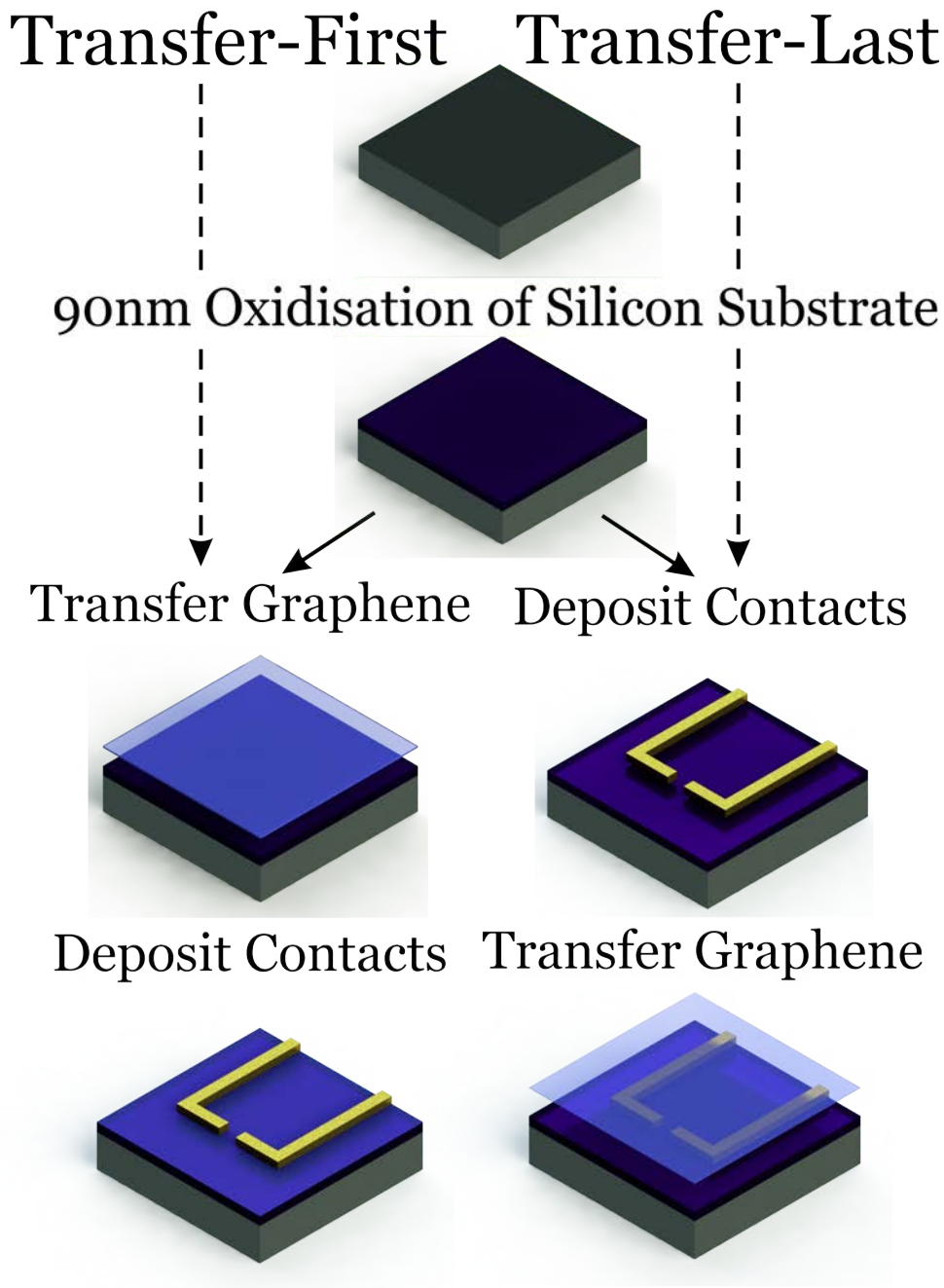

Figure 4.13: Schematic diagram demonstrating the differences between a transfer-first and transfer-last process. The methodology using the transfer onto 2 probes is explored in section 4.2

dioxide substrate. Here the graphene is tested to determine if it will remain in contact with the gold after the transfer, which will allow for a higher conductive metal layer to be used with graphene.

The graphene has then been transferred onto contacts using the improved transfer process. Figure 4.14 shows the AFM data after the graphene transfer, where the graphene has wrapped around the metal contacts with no strain or damage. It is unclear whether the transition angle from the top of the contact to the substrate is caused by the graphene. The 107 degree angle could be caused by the use of a negative photoresist (AZ2070) to pattern the contacts. Since the profile of the resist is known to taper inwards and the sputter deposition has a higher conformality for the coating compared to e-beam evaporation. What can be concluded is the transfer of graphene onto a patterned substrate does not adversely affect the quality of the graphene sheet and still produces a uniform sheet of graphene in direct contact with gold.

4.3.2 Transfer onto 2 wires using E-beam lithography

The design of the e-beam test is to control the contact area and gaps between 2 wires made from gold and nanocrystalline graphite. The high accuracy of the e-beam allows for the contact area and gap to be accurately controlled. The width of the contacts vary from 2.5 um down to 0.2 um and the gap between contacts varies from 8 um down to 1 um. The tests are split into two variations microscale and nanoscale contact dimensions. The parameters are annotated in the figure 4.15 and show the hooked design for the wires with the graphene in blue covering the contacts after the graphene has been etched to cover only a small contact area on the wires. The first stage is to investigate the effect of transferring graphene onto two different materials changes depending on the dimensions of the contacts and gap. Second the critical dimension at which graphene is suspended is found.

4.3.2.1 Metal contacts

The metal used here is repeated from the photolithography test except a thinner layer of gold is used due to the limitation in resist thickness. The AJA Orion sputter tool is used again to deposit a 10nm titanium layer followed by a 90 nm gold layer. The resist for lift-off is a MMA/PMMA bilayer 450 & 150 nm thick. With a dose varying from 250$\mu\mathrm{C/cm}^2$ to 400$\mu\mathrm{C/cm}^2$ in 50 μC/cm^2 steps. This resulted in dose being too low for 200 μC/cm^2 to be fully exposed. The most accurate dose is determined to be for Dose 300$\mu\mathrm{C/cm}^2$. To work this out the difference between the achieved feature size and the targeted size are converted into a percentage and then averaged to find which dose was closest to 100 percent. Dose 300 was the best as its width was 33% bigger than the target and the Gap was 10% smaller than the target. Although Dose 250 was closer to the desired width and Dose 350 was closer to the desired gap, overall Dose 300 was better. After

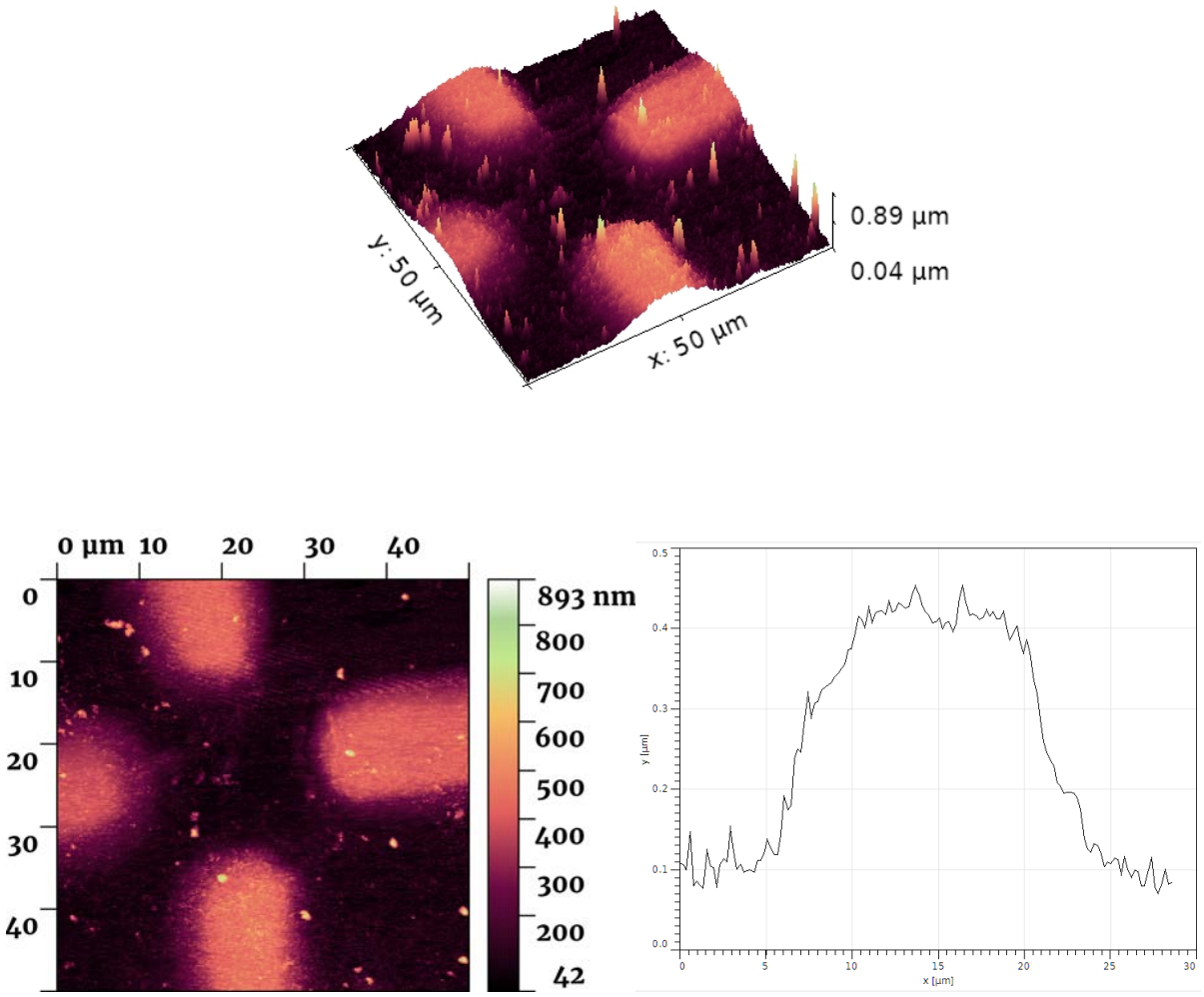

Figure 4.14: AFM data after transfer of graphene onto metal contacts using photolithography. Left: 3D image to show the continuous sheet of graphene wrapped around the contacts without breakage in the graphene sheet. As seen in transfers of graphene onto SiO2 the cracks would be easily visible. Middle: 2D image of the transfer to show the cross section taken for the profile measurement. Right: Profile measurement to show the shape of the graphene on the contact. It is unclear whether the shape is caused by the graphene sheet or tip convolution from the metal deposition.

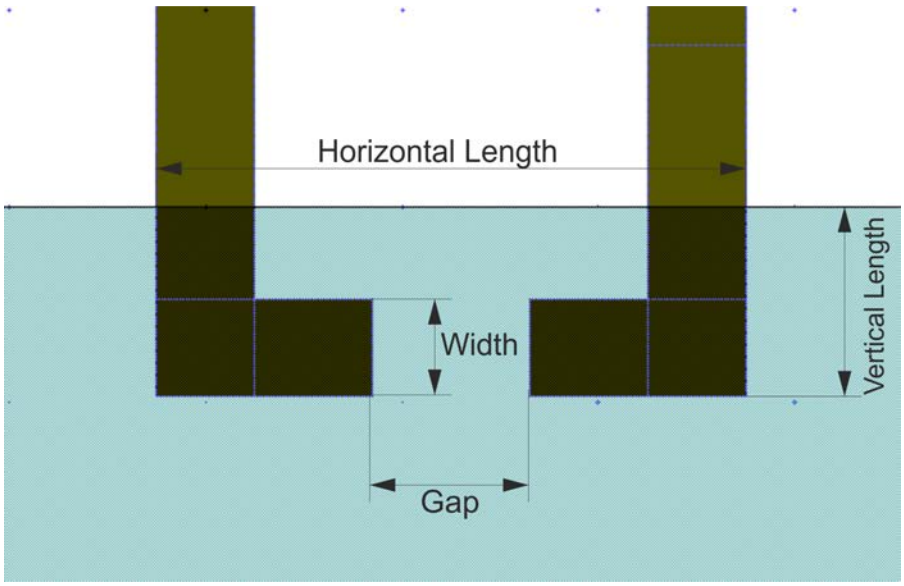

Figure 4.15: 2 wire contact design with graphene layer in blue and contacts in gold. The graphene is designed to be etched after the transfer if it's successful

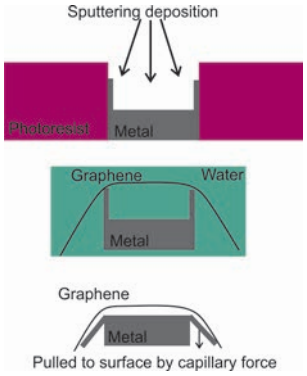

Figure 4.16: Schematic diagram of metal contact sputtering cross section. As the graphene is then transferred while immersed in liquid it rests on top of the two metal fins formed by the sputtering. When the sample dries the large surface area of the graphene sheet is then pulled to the surface by capillary force and causes the fins to collapse.

the contact deposition CVD-graphene is then transferred using the method described in Chapter 3.

Unfortunately using a sputter deposition method to deposit the metal was the incorrect choice for a lift-off process. The sputter deposition is highly conformal and coats the inside of the wall of the resist. This creates metal contacts with a fin surrounding the edge metal layer as illustrated in figure 4.16 and can be seen in the high contrast of the contacts edge in figure 4.17.

In most devices this would not be too much of an issue; but the force at which graphene is pulled to the surface resulted in the side wall edges being knocked over in the angle at which the sample was left to dry. This did produce some rather interesting structures where only a nanoribbon of graphene was left standing and the rest of the graphene had broken apart. Others produced a folded structure so a bilayer fin is left standing and a single fin structure that contacts across the edge of the metal. These types of structures

had repeated several times across two samples showing minor differences where the sample had a 200nm thick layer instead.

Due to the metal folding there was a massively decreased yield in the number of testable devices, where the gold had folded to create short circuit connections. In future devices e-beam evaporation to deposit the contact materials will be used to prevent the side wall issues. This unfortunately meant the critical dimension for suspension could not be accurately extracted. As seen in the figure 4.17 the graphene can be seen to be spread across the wider contact gap and form a 200 nm long nanoribbon across the gap due to the sheet partially breaking across the contacts. The wrinkles in the sheet highlight in figure 4.17 show the strain caused in the graphene as it pulls down across the contacts. This indicates the graphene does suffer mechanical damage from the transfer onto contacts in the nanoscale regime to cause a breakage and extra wrinkles across the device area.

4.3.2.2 Transfer onto Nanocrystalline Graphite

As stated previously one of the significant sources of doping in graphene is the metal contacts. It stands to reason that by changing the material to graphite there would be no doping of graphene. To produce a device with CMOS compatible methods a novel method of fabricating graphite developed at the University of Southampton by Marek Schmidt [105]. This graphite is produced by exploiting the effect of catalyst free growth of graphene on SiO2 using PECVD. As previously described in [106] the catalyst free growth of graphene does not have any thickness limitations compared to copper catalysts. This is exploited to create films of nanocrystalline graphite (graphite due to thickness greater than 2 nm) that show an acceptable conductivity of $1.003\text{x}10^{-4}\Omega\text{m}$ for films 50 nm thick.

The main difference in working with NCG compared to the metal devices is the processing steps are more similar to creating silicon devices. A NCG layer is deposited by by PECVD in the Nanofab (Oxford instruments tool) by passing a methane gas and forming gas mix over a silicon wafer with 295nm oxide at 750°C to create a 360nm thick layer. This thickness was chosen to create as high a gap as possible to increase the chance of suspending graphene. A 30nm silicon oxide layer was deposited to act as a hard mask to protect the NCG from being etched, since the NCG etching recipe is the same used to strip resist. Although the resist needed for the e-beam exposure was 100nm thick HSQ in the end instead of PMMA as intended, the 100nm thick layer was chosen so that the resist selectivity could be tested to determine if the 30nm thick method could be used instead. The same designs as the metal contacts were used the only difference is the dose is varied from 1400 to 1800 in 100 steps. After exposure the HSQ is developed and etched using the standard oxide etching recipe in the RIE for 1 minute 20 seconds to remove the hard mask, followed by a 15 minute O2 etch recipe for 15 minutes. Ellipsometry is used to confirm the thickness of the oxide and NCG at each stage, the profiler is then used to check the thickness of the oxide left. To finish the

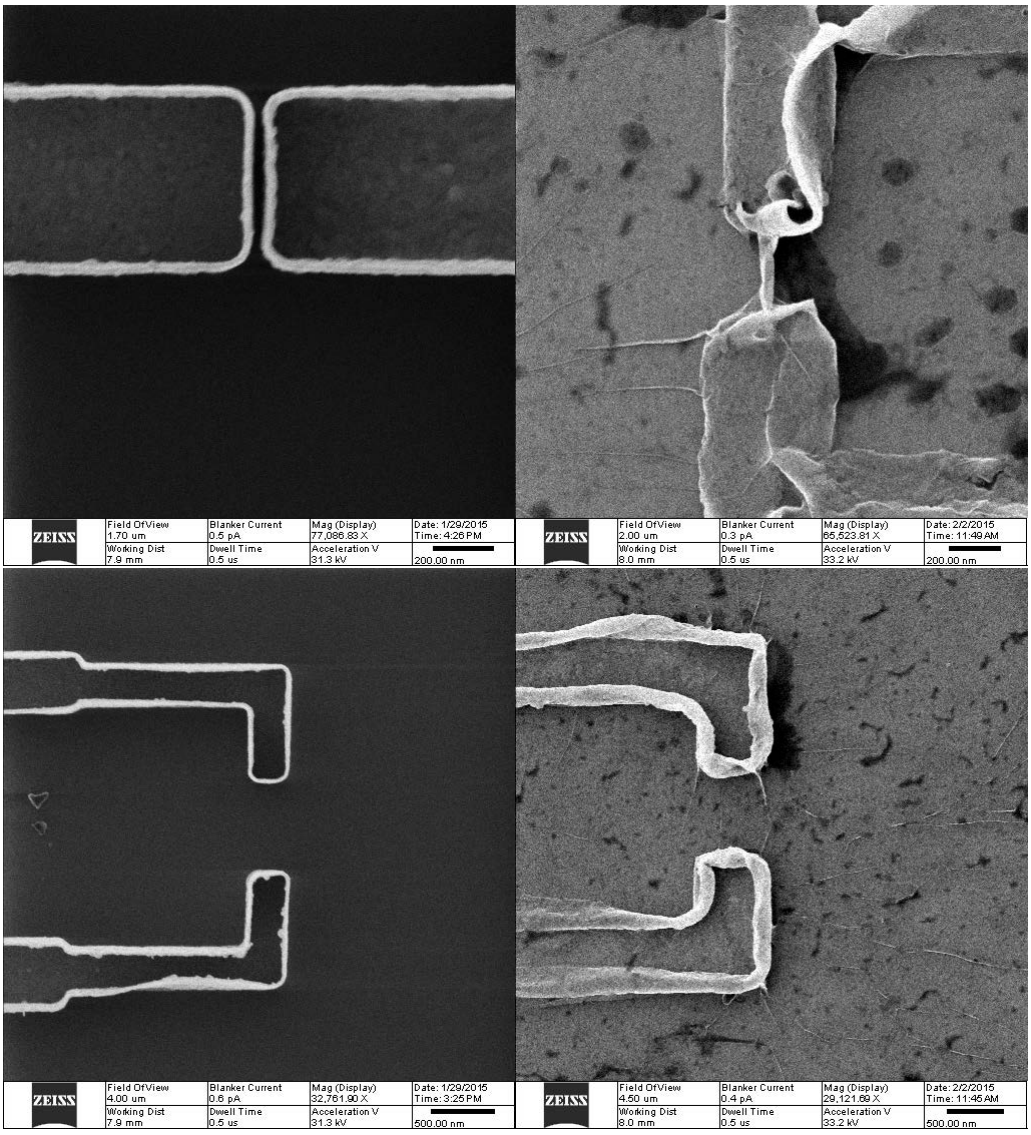

Figure 4.17: HIM images of metal lift off patterns before and after transfer of graphene sheet. Top left: 621nm wide & 40nm gap is the smallest gap achieved between two contacts after transfer. Top right: Graphene nanoribbon suspended between two contacts after transfer. Bottom left: 419nm wide & 668nm gap. Bottom right: Image of device in bottom left after transfer of graphene.The high contrast of the edge of the wire is due to the fin formed from the sputter deposition, where the fin is ~40 nm. After the transfer the collapse of the metal fin can be seen by the increase in the width of the high contrast edge. The graphene can been seen to wrap around the metal in the bottom left despite the fin collapse. The wrap around can be seen by the wrinkles in the graphene sheet on the substrate spreading out from the bottom contact.

remaining oxide is etched in the RIE rather than HF leaving a 400nm step height due to an over etch of the oxide substrate. Lastly optical lithography is used to expose the metal contact & alignment mark patterns, unfortunately the alignment marks made on the NCG and the pad contacts were too overexposed with the HSQ despite PEC to correct any dosage issues, causing a misalignment of 2um for the graphene isolation etching.

The before and after images of the graphene transferring onto the NCG are shown in figure 4.18.The significance of the graphene transfers shows a severe breaking in the graphene sheet from the capillary force pulling the graphene to the surface. As indicated by some of the images, the nanopores caused a considerable weakening of the structural integrity of the CVD sheet, causing the sheet to break apart along the nanopores like a nanoscale game of connecting the dots. This is then further impacted by the grain boundary defects from CVD-graphene's polycrystalline nature, allowing it to tear along the defects where the sheet is weakened. Although there has been strong evidence to suggest that the grain boundaries do not impact the electrical performance as previously predicted [54], it does still show a significant mechanical instability that even the capillary force can break its structure.

Despite these hindrances, the similar effects seen in the graphene on metal contacts has repeated to create suspended nanoribbons across the nano-gaps. With some even 250nm long and 100nm wide seen in figure 4.18. For the next devices to be fabricated using NCG, a much thinner NCG should be used to reduce the force of the pull down to the surface. The metal contacts and alignment marks should be fabricated in the first step, acting as a hard mask prevent any issues of overexposure with the HSQ. To improving the contacting from issues with the lift-off Nickel will need to be deposited first, as Titanium does not provide a sufficient bond. Since the NCG will be thinner and HSQ will be used again for the devices, a thinner HSQ layer can be used without any oxide hard mask needing to be deposited first.

4.3.3 Summary

The main difference between this work and the work by IBM is the use of transfer-last to wrap the graphene around the metal contacts without breaking the sheet. In the IBM work the graphene is transferred onto metal and oxide made the same thickness by CMP. This robustness of graphene to pull to the surface could be exploited for creating interconnects in ICs by simply transferring graphene onto the area of the via rather than by filling the via with metal. The greater contacting of graphene onto gold has been discussed over its improvements compared to traditional methods of using a titanium, chrome or palladium buffer metal for contacting graphene has been discussed. Although as Chapter 5 discusses there is significant difficulty in reliably depositing gold onto graphene, however, this method shows the initial feasibility of contacting graphene directly by gold. Even though the electrical measurements of these devices is poor, it shows great promise for future applications.

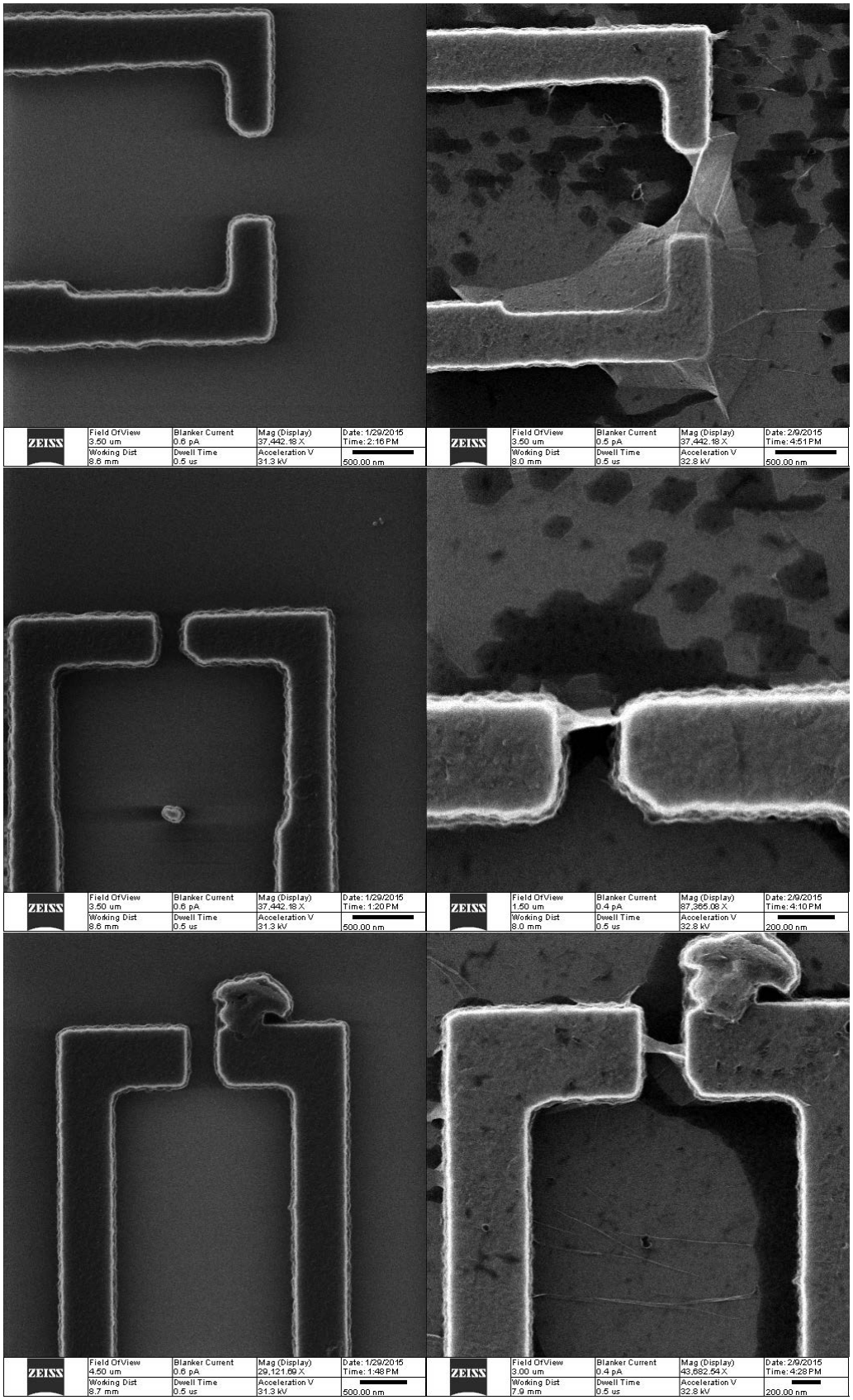

Figure 4.18: HIM images of the NCG 2 wire contacts. Images on the left hand side show the NCG before the transfer of the graphene. The NCG is the darker contrast on top of the silicon dioxide. The right hand side shows the graphene after the transfer. The graphene can be seen on top of the NCG and the substrate due to the lighter contrast of the graphene. Three different transfer results can be seen in the three images. The hexagonal shapes in the graphene sheet are from nanopores formed during a defective CVD-graphene growth. Top right shows the graphene stretched across the bottom con-tact. Middle right shows the graphene forming a fin between the corners of the NCG contacts. The bottom right shows a suspended nanoribbon 40 nm wide and 200 nm long caused by the graphene sheet breaking from the transfer and forming a nanoribbon.

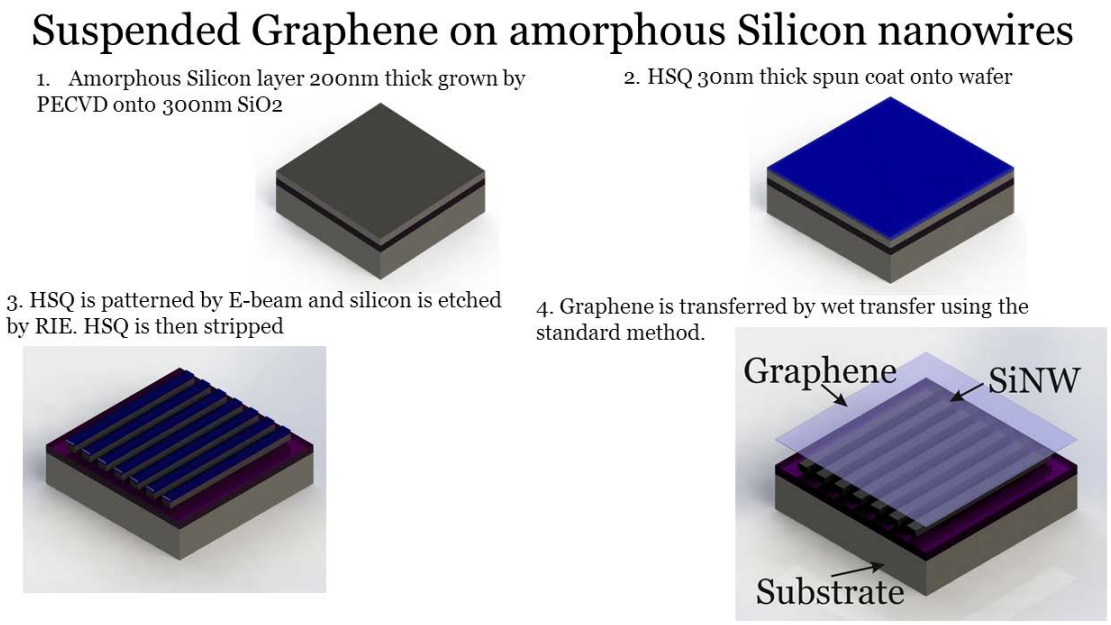

Figure 4.19: Process flow using schematic diagrams for suspension of CVD-graphene on amorphous silicon nanowires

4.4 Direct transfer on patterned silicon nanowire array

Using the data obtained from the previous graphene devices the transfer-last process is tested for the suspension of CVD-graphene onto a large array of amorphous silicon nanowires. See figure 4.19 for the process to create the devices. An array is used to determine the impact of increasing the surface area on the suspension of graphene. Silicon is used to test the compatibility of fabricating a graphene device with a CMOS compatible BEOL process. Additionally, the processing of a silicon based material is a more stable process than NCG to create a dense nanowire array.

Based on the previous results to suspend the devices the gap was determined to be 200 nm between each nanowire. The width of the nanowire is exactly the same to maximise the density of the array. The nanowires are fabricated by depositing 60 nm of amorphous silicon using PECVD at a deposition rate of 0.26 nm/sec using 50 sccm or silane (SiH4) and hydrogen gas at the chamber pressure of 350 mTorr and a temperature of 250 C. The wafer is diced into the 30 x 40 mm sample size then patterning with AZ2960 and etching by RIE 1 um into the substrate for the alignment marks. The sample is quickly cleaned, using a standard RCA1 & RCA2 for 10 minutes followed by 2 minutes in Buffered HF. The sample is then coated with HSQ and patterned with e-beam lithography for the nanowires, followed by a hard bake of the HSQ. To finish the sample is etched by RIE to form the nanowires and the HSQ is stripped with BOE. The graphene is then transferred onto the substrate.

The partial suspension of graphene onto nanowires made from amorphous silicon has been achieved over an area of up to 500 um. In figure 4.20 the difference between the graphene and the nanowires can be seen from the lighter contrast in the HIM for

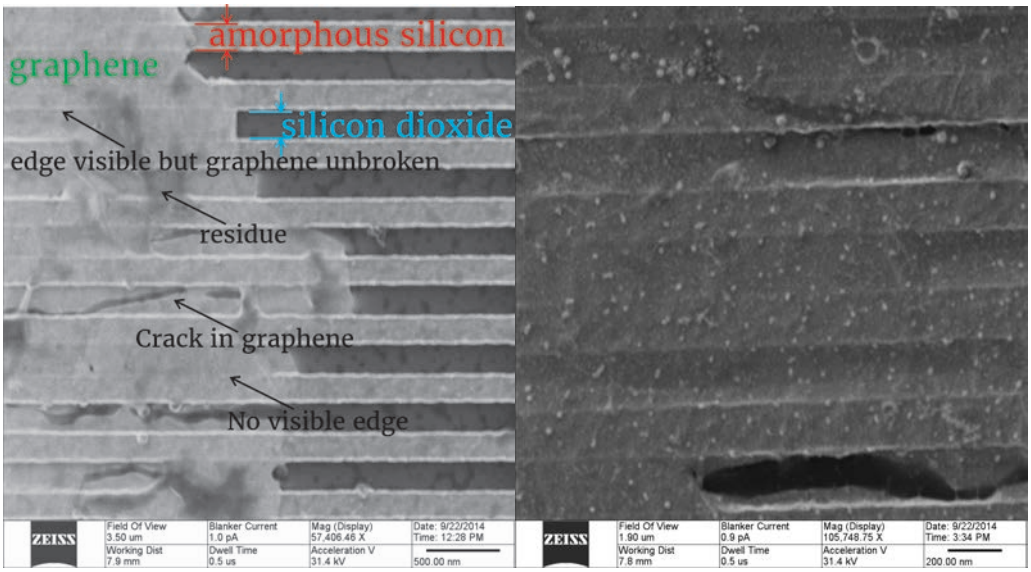

Figure 4.20: HIM images of graphene partially suspended on silicon nanowires. Left: shows distinct difference between nanowires covered with graphene and bare nanowires. Right: shows the partial suspension of graphene with varying height levels of the graphene sheet spread across the nanowires.

graphene. Of note is the higher contrast for the edge of the nanowires. When the graphene is spread across the nanowires the contrast for the edge becomes less clear indicating the graphene layer is perfectly suspended across the nanowires. This is then verified with AFM to show when there is no graphene a gap height of 50 nm and wire width of 200 nm is measured, as seen in figure 4.21. When the graphene is transferred onto the wires the change in height is now between 20 and 25 um across the graphene for the partially suspended graphene. When fully suspended the AFM in figure 4.21 does not show any significant dip in the measured height across multiple nanowires. The AFM data confirms the partial suspension of graphene across a 5 um distance.

This shows a significant technological breakthrough in the suspension of graphene over large areas using the wet-transfer method. This improves upon previous works detailed at the start of this chapter and enables a simple one step process to suspend graphene across a large area. Although the suspension is only partial across the nanowires the key concept has been proven. Future work will address the issues in the transfer that causes the graphene sheet to still break from the capillary force. This could be achieved by modifying the nanowire structure or using a dry transfer of the graphene sheet. Future devices can then use the large-area transfer process to test more contact materials and create suspended TLM devices.

4.5 Summary

The transfer-last method has been established for its use in fabricating wrap-around & suspended devices. The two extremes of device dimensions have been evaluated showing a control from wrapping around structures to suspension on large arrays of supported

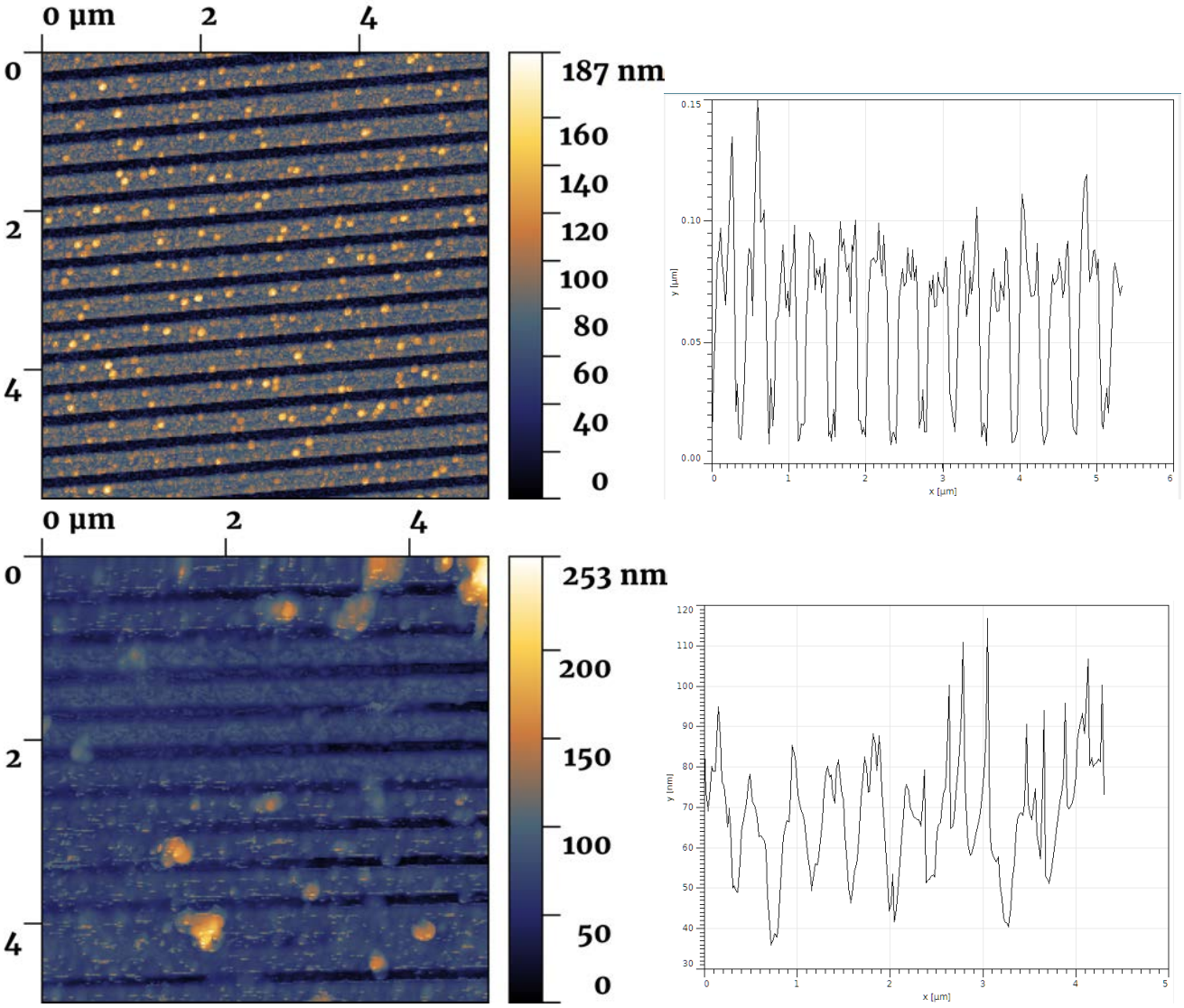

Figure 4.21: AFM data from the transfer of graphene onto silicon nanowires. Top image is the silicon nanowires before the transfer, the height shows the correct distance of 50 nm for the nanowires. The AFM tip was unable to correctly image the gap between the nanowires. The measured nanowire and gap is different than the measurement in the HIM images. Bottom shows the graphene partially suspended on the nanowires after the transfer, the periodic structure seen in the top image is altered by the graphene. The height now shows a difference between 15 and 20 nm for the partially suspended graphene. When the graphene is fully suspended there is no periodic dip across the nanowires and shows a distance of 900 nm rather than the measured 600 nm from the blank nanowires.

nanowire structures and targeted suspension on a small defined area. The potential for graphene devices supported by controlled nanoscale structures using NCG has a wide ranging impact in NEMS, biosensor, ballistic devices and superior FETs , where future work will focus on this aspect of the fabrication methodology. The methods of creating graphene with a CVD process means it can used in transfer-last process methodology. Using the natural nanowire dimensions of first layer interconnects to automatically suspend graphene. Since the critical dimensions are below the threshold needed to suspended graphene. The transfer-last process has been demonstrated as a important technique for future devices fabricated using CVD-graphene.

Chapter 5

Single electron transistors on CVD-graphene platform

5.1 Introduction

The use of CVD-graphene has so far had limited investigations into the impact of down-scaling on CVD-graphene compared to exfoliated graphene. So far no work has investigated the width dependence of graphene nanoribbons using CVD-graphene. The only evidence of patterning CVD-graphene into a nanoribbon was done by [62], where a 12nm by 1um ribbon was patterned on a 90nm silicon dioxide. This single device did not show any distinct differences to the properties of those undertaken with exfoliated graphene nanoribbons. Demonstrating the long nanoribbon fitted with the theory of a transport gap dominant behaviour [62]. Although this device was measured at low temperature the single electron tunneling properties were not investigated. Currently the only investigations into single electron transistors using graphene nanoribbons have involved fabricating from exfoliated graphene. At first this could of been done out of the principle that reducing the number of defects sheet improves the SET. But as has been seen in Chapter 2 the patterning and etching of graphene already introduces defects and a significant change in the properties of graphene. For this reason the study of CVD-graphene , which, have an increase in lattice defects and grain boundaries still merits investigation. The divergent properties of the scaling effects in CVD-graphene nanoribbon devices can still provide interesting insight into the properties of graphene.

In this chapter the focus is on producing a simple 3 terminal device using a silicon back gate to highlight the unique aspects of the CVD-graphene nanoribbons. This is done after the methods in using HIM milling to fabricate devices was shown to increase the overall defects in the nanoribbons and would further complicate the analysis of the devices.

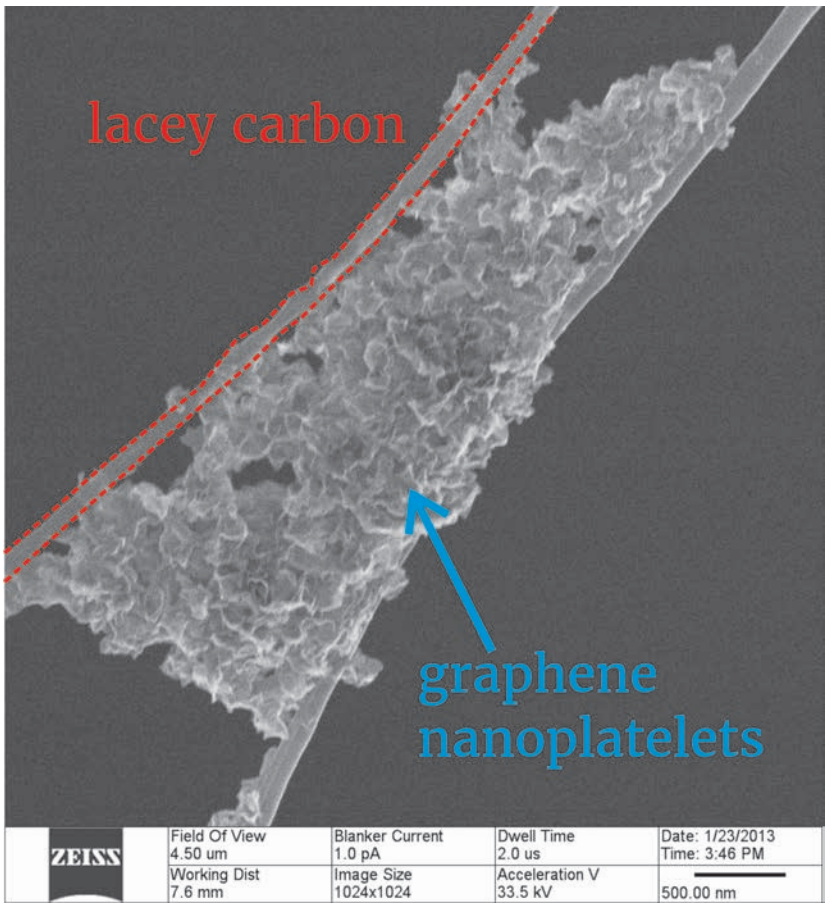

Figure 5.1: Graphene nanoplatelets suspended between thin support beams made from lacey carbon in a TEM grid section.

5.2 Fabrication of devices

5.2.1 Helium Ion milling of suspended graphene quantum dot

The use of a helium ion microscope to fabricate graphene devices has been well documented to produce downscaled nanoribbon transistors, SETS and suspended devices . If the production of a suspended nanoribbon device is to be achieved, the simplest method to achieve this would be the imaging and milling of graphene with HIM. The use of HIM allows the fabrication of suspended graphene nanoribbons without relying upon the difficult exposure of suspended graphene using an e-beam resist. This project focused on the impact on the atomistic structure of graphene, while a colleague (Shuojin Hang) investigated the impact of helium ions with Raman spectroscopy on a flat substrate, where the desire was to produce a suspended nanoribbon device that can be imaged using STEM to correlate the atomistic structure with the electronic properties. However the impact of HIM on the quality of graphene sheet had not been attempted before. To do this the first stage of the research was to investigate the change in atomistic structure of graphene with an increasing dose of helium ions.

The simplest way to achieve the initial assessment was to use commercially available graphene that already exists on a TEM grid, rather than fabricating a TEM from

scratch. The TEM grid was manufactured by Electron Microscopy Sciences and was the one supplier found to produce a graphene sample capable of producing graphene clean enough for STEM imaging [108]. The graphene was deposited using a gas phase growth method where the graphene forms nanoplatelets on a support structure made of lacey carbon spread across the 3 mm copper grid frame. As seen in 5.1 the graphene looks like crumpled graphene but in reality is a stack of nanoplatelet sized graphene in a random arrangement.

The first investigation with the HIM was to test the impact milling a gap into the graphene surface had on the crystallographic structure. Since HIM gives surface information it made it difficult to discern where monolayer graphene might be from the clumps of nanoplatelets. By assumption from the TEM images of the unexposed graphene the most likely location of monolayers was reasoned to be at the edges, where the contrast from the secondary electrons is faintest. Crude attempts at milling were made by overexposing the graphene sheets by leaving the HIM to continuously scan across the sample until it had eroded away. Several regions of graphene was milled with different sizes, with the smallest a 10nm gap in the graphene layer of figure 5.2. However when analyzing the milled graphene using STEM it revealed it was not possible to observe a graphene structure on any of the nanoplatelets exposed to the helium ions. The helium ion bombardment on the nanoplatelets had turned the surrounding region on the graphene sheet amorphous. It is was expected the ion bombardment would caused beam induced point defects in graphene. What was not expected is the low imaging doses used would affect the graphene to such an extent.

This led to an investigation into the effect of varying dose on the levels of deformation of the graphene lattice. The dose was varied from 10^3 to $10^5 ions/cm^2$, while the accelerator voltage was set to 10kV. The does was exposed across the 5 x 5 um grid of the TEM. The results in figure 5.3 show how the increasing helium ion dose caused extensive damage to the graphene crystalline structure. The unexposed graphene in 5.3a shows the typical result for a graphene layer when imaged with STEM. As the dose increases the ordered structure in the graphene is disrupted until the $10^5 ions/cm^2$ dose has damaged the graphene sheet to the extent the structure is no longer recognizable, where the structure more closely resembles the results obtained from amorphous carbon [109]. These results were later confirmed by a colleague conducting extensive Raman spectroscopy analysis of the damage cause by Helium ions [110], where the back scattering of helium ions was shown to affect the graphene structure in an area much larger than the milled region.

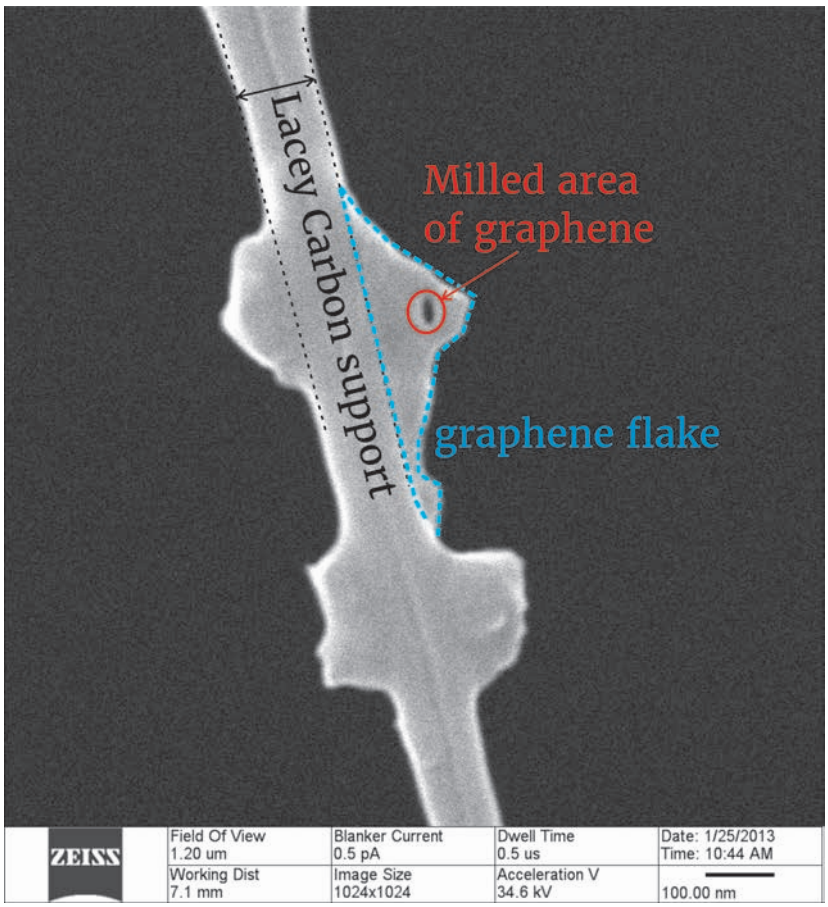

Figure 5.2: Graphene on the edge of a lacey carbon beam. The red arrow points to the 10 nm hole milled in the sheet to investigate the helium ion damage to the surrounding graphene.

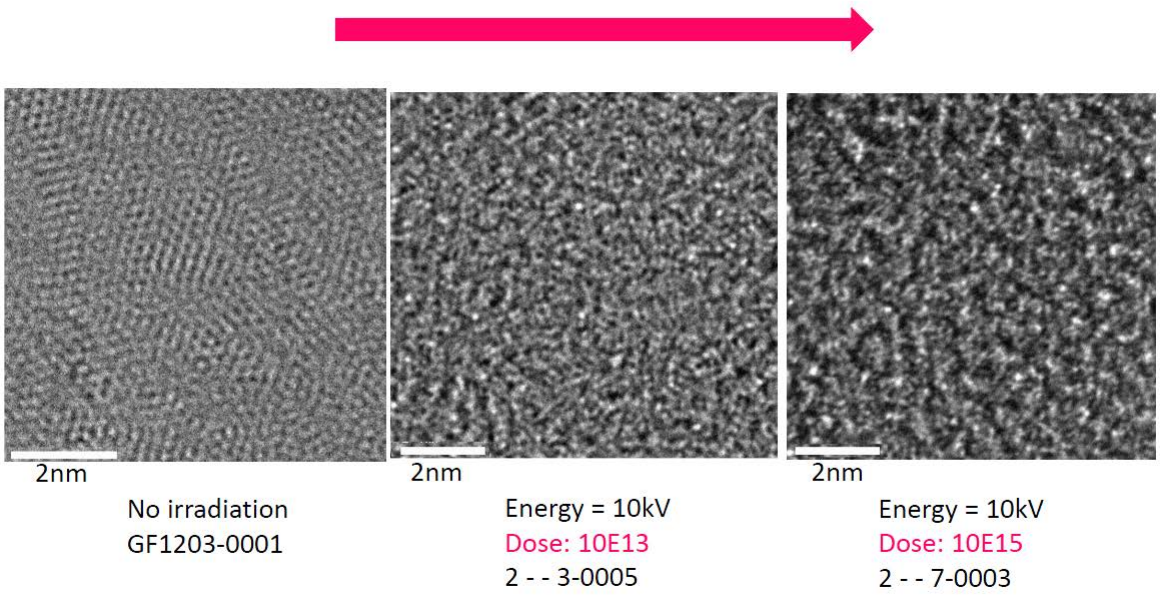

Figure 5.3: STEM images from the exposure of graphene with increasing doses of helium ions. Left shows the effect of no irradiation on the graphene sheet with the dose increasing as the images go right. The dose is not enough to mill the graphene but shows the breakage of the ordered graphitic structure seen on the left images. As the dose increases the disorder can be seen to increase further. There is no distinctive graphitic structure observable in the image on the right.

Although the use of HIM had been seen as unique method to obtain extremely downscaled nanoribbon devices it has been decided HIM milling should not be used anymore. The degrading impact of the helium ions on the structure of the graphene means the device region will be physically altered to the extent it no longer correlates with a graphitic structure. If the investigation into the CVD-graphene scaling is to be achieved the properties of the final devices must closely resemble the expected structure at the end of the fabrication. HIM milling will prevent any conclusions into the results of the CVD-graphene devices to be attributed solely to the CVD-graphene.

5.2.2 Nanoribbons fabricated using electron-beam lithography and PMMA

If HIM is unsuitable for producing the extreme downscaling of graphene nanoribbons then the limit for fabricating nanoribbons using electron-beam lithography need to be explored. Although e-beam would of been necessary to pattern the larger feature sizes before a helium ion milling step, the maximum possible tool resolution for e-beam only devices now needs to be investigated. The first e-beam resist to be tested is PMMA, this is due to historical reasons from fabrication with exfoliated graphene, so less optimisation is needed. Additionally, the PMMA is a positive resist which means when the resist is removed the underlying CVD-graphene layer can be viewed after the exposure and testing.

Initial efforts in using PMMA to fabricate CVD-graphene focus on patterning all-graphene devices, where graphene is patterned into a wide-narrow-wide nanoribbon with graphene side gates as seen in Chapter 2. The purpose was to determine the optimum feature size achievable for graphene transistors using PMMA as the e-beam resist. To optimize the design of the graphene device an array of nanoribbons are patterned with varying width, length, square or angled tapering, source and drain thickness and gate width. This was done to approximate the density of transistors possible for wafer-scale all-graphene transistors.

The first design was made using L-edit and is shown in figure 5.4. This shows the 3 x 3 array of 9 different test patterns, which is then in turn repeated again 9 times across the 1 cm^2 sample in a 3 x 3 array again. The total area of this one test pattern is 200um by 200um. The shown is the pattern for the graphene after etching. To expose this design the pattern has to first be inverted for the e-beam. This is done by drawing a box around each design and using a Boolean subtraction of the test pattern. The box is limited around each test pattern to minimize the exposure time.

The parameters that are adjusted for each test design are:

1. Varying nanoribbon width from 10 nm, 20 nm, 50 nm, 75 nm & 100 nm for each column
2. Varying the gap between the gate and nanoribbon from 20nm, 40nm, 80nm & 160nm for each row.

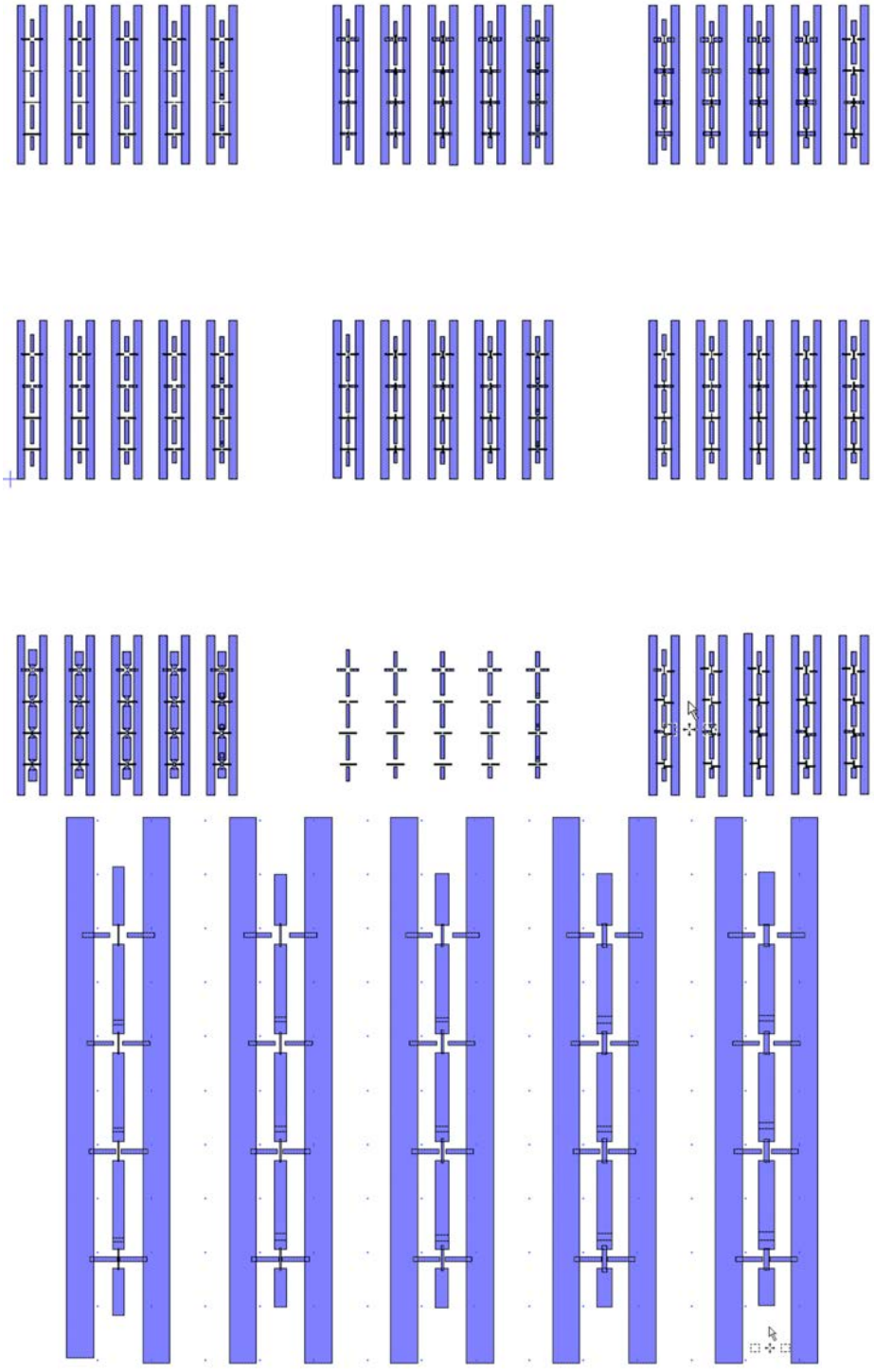

Figure 5.4: Images of the various pattern designs used to test the PMMA exposure. Top shows the 9 different designs in the 3 x 3 grid. Bottom shows the design of the nanoribbons with the different nanoribbon widths for each column and the gate to nanoribbon gaps increasing with the rows.

3. Nanoribbon length vary from 150 nm, 300 nm or 500 nm
4. A squared edged nanoribbon seen in figure 5.4 or a 45 degree tapered edge
5. Gate widths from 40 nm, 80 nm, 150 nm & 250 nm
6. Source and drain widths of either 300 nm or 500 nm

The parameters 1 & 2 are repeated for each design and when not being changed the Nanoribbon length is 150nm, gate width is 80nm and Source & Drain are 300nm wide with the gates all joined together. The PMMA used was the 495 variant and was 150nm thick. The variation for each dose goes from from 100 to 400 uC/cm2 in increasing doses of 50uC/cm2.

The results of this test exposed several issues in the large area patterning of CVD-graphene. The yield became quite low. Out of 9 different doses, only 2 were still fully intact. Although the individual cells of the particular dose was heavily damaged, with large areas of graphene removed or individual graphene columns removed. It is difficult to determine what possible mechanisms could of caused this. The most feasible reasons are (i) the ones that survived had received too large a dose for the smallest features to be patterned so were etched away, (ii) the stripping of the resist also removed the graphene as the graphene bonded better to the PMMA than the silicon dioxide (iii) damaged caused by plasma penetrating the thin PMMA during etching. The large area damage to the graphene sheet can be seen in the helium image of figure 5.5, where on a good area where some of the nanoribbons had survived the crack in the top left was much more common across the rest of the sample. Even when the bulk of the graphene surrounding the patterns survived the nanoribbons had been lifted off, as seen in the blank squares with some shadowing left over from the RIE step. The process was repeated a second time and found that the results for using a CVD-graphene layer with PMMA was insufficient to produce a high yield of devices. A HIM image (figure 5.6 was also taken from one of the surviving nanoribbons to show the high quality of edge shape achieved from the pattern and etching of the graphene layer.

Due to these results the use of PMMA was decided to be unsatisfactory for creating high quality CVD-graphene devices, since they would reduce the yield of the devices too much. The next best available e-beam resist to be HSQ, which was used in early works by Philip Kim's group [57] [2]. This has the advantage of encapsulating the graphene devices when they are transported to JAIST for testing, but does mean that the exact width of the nanoribbon underneath the HSQ is not known due to the undercut that occurs when etching.

5.2.3 Fabrication of CVD nanoribbons with HSQ

Design of CVD nanoribbons

To investigate both the scaling effects on the properties of CVD-graphene nanoribbons and SETs a simple 3 terminal device is used. On the CVD-graphene surface only 2

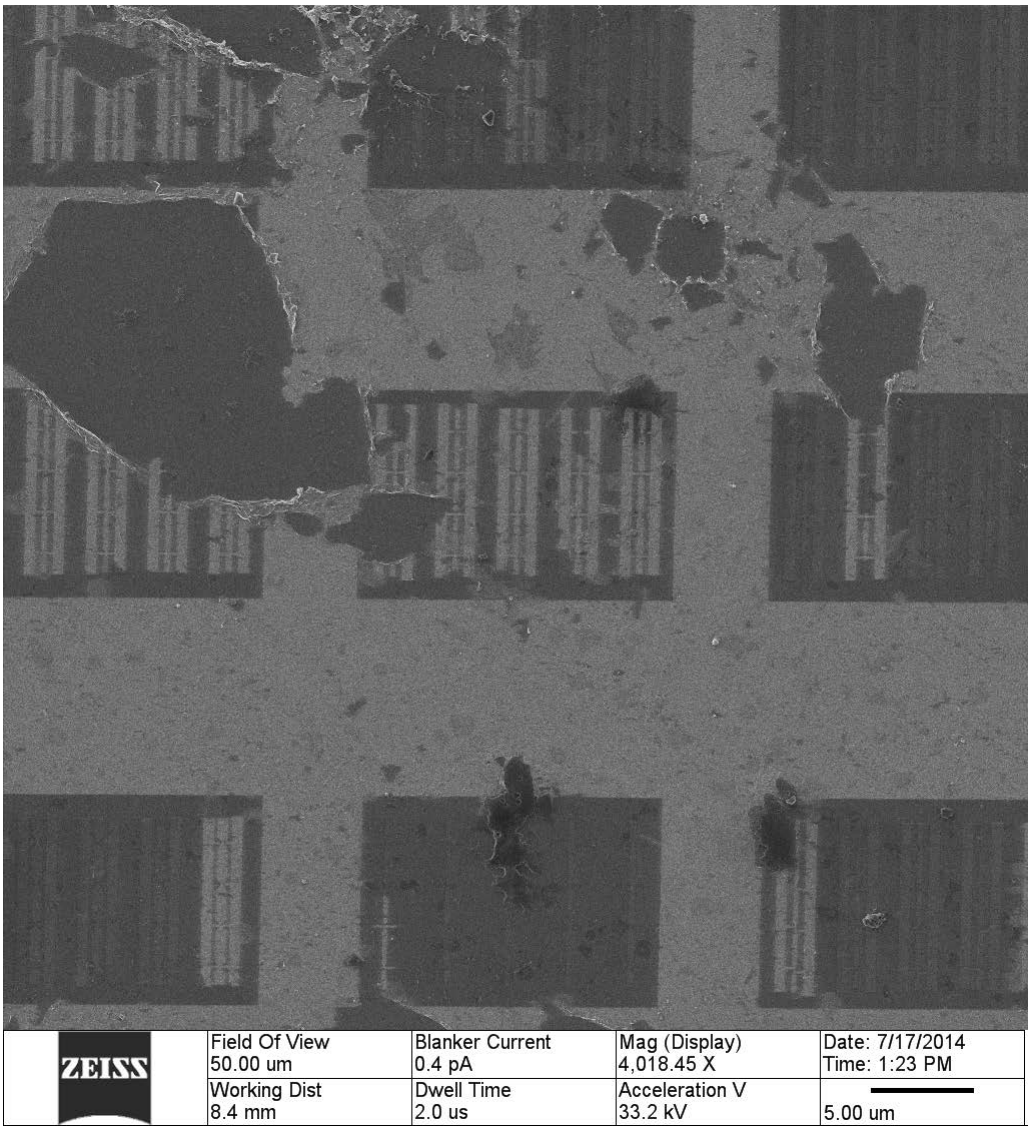

Figure 5.5: HIM image of the CVD-graphene after the RIE and PMMA strip. Image shows a single array of graphene where the sheet has been peeled away on an area and the dose test devices have completely lifted away from the sample leaving a shadow behind from the etch. The edges of the graphene show it has peeled and folded in on itself indicating it was after the PMMA strip that the issues had occurred.

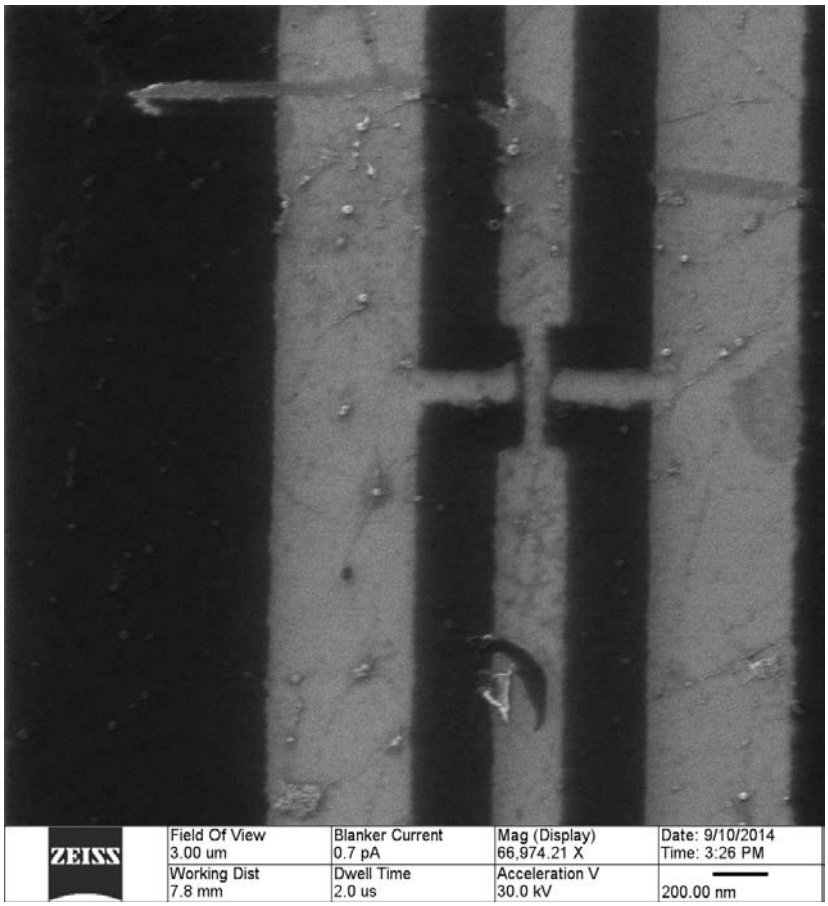

Figure 5.6: Image of etched nanoribbon using HIM, taken at low dose to avoid damage to the nanoribbon from one of the areas that had survived the PMMA stripping. Shows a small 100 nm long and 50 nm wide nanoribbon with 10 to 20 nm gap between the ribbon and the side gates.

metal contacts and deposited for the source and drain while the silicon carrier is used as the backgate. This design is chosen to reduce the complexity in the measurements after the difficulties previously encountered when trying to obtain measurable devices. To ensure the devices have a sufficient yield the more robust resist of HSQ is used to pattern the devices. This method of fabrication follows the same methods used by Han et al. in the seminal work on nanoribbon scaling [57] and the only other significant work on CVD-graphene nanoribbons [62].

The designs of the nanoribbons are made in L-edit using 3 masks for the devices, see figure 5.7 for the diagram of the design. First for alignment, second for the contacts, and the last is the nanoribbon pattern. The devices are to be fabricated onto a 27 x 32 mm sample sizes. With the alignment marks patterned first in a regular array on a blank silicon wafer before the graphene transfer. This allows for as many samples as possible to be fabricated provided the graphene is covered that sample area.

The design for each sample produces 100 rows of nanoribbon devices with increasing width for each row in a wide-narrow-wide pattern. While the ascending columns increase in nanoribbon length, although with lengths repeating in size to maximise yield. The first row designed to be 1 nm is width and step in 1 nm widths until 100 nm for the final row. While the smallest length is 100 nm increasing to 200 nm and 500 nm and is repeated 4 times for each length. The wide graphene regions are 100 nm in width and between 500 nm (for 100 and 200 nm ribbons) and 1 um (for 500nm ribbon) in length. The designed nanoribbons are fit into 1 mm cells each to be suitable for use in a cryostat after wire bonding. Each cell can accommodate 10 devices in a 5 x 2 arrangement. The naming convention for the devices uses the annotation AA-BB, where AA = Designed Width and BB = Designed Length is used.

Although the nanoribbons have been designed to be 1 nm in width for the smallest size, the physical minimum will be determined by the e-beam lithography. Because the minimum dose of the resist when using e-beam lithography will mean they are much wider in reality. In part due to the minimum beam size of the e-beam is a 4 nm spot and additional effects from proximity error. However, the minimum possible width of the nanoribbons is not known, so it is necessary to design the patterns to achieve the smallest nanoribbons for this process.

Another crucial factor in the design is these nanoribbons have a sharp transition from the wide to narrow segment transition, where the ideal result would be to achieve a transition angle as close to $90^{\circ}\mathrm{C}$ as possible. Based on evidence shown in “Characterizing wave functions in graphene nanoribbons, 2014” [63] the sharper the transition angle the better control of the electron wavefunction wide nanoribbon sections is possible. Although the aspect of a sharp transition angle has not been fully explored on the impact of device properties but from the search in literature this produces a superior SET devices. In an ideal case the effect of transition angle would be explored but the focus of this experiment in the scaling effects of CVD nanoribbons and the SET properties of the smallest nanoribbons. For that to be possible the yield of the devices has to be maximized.

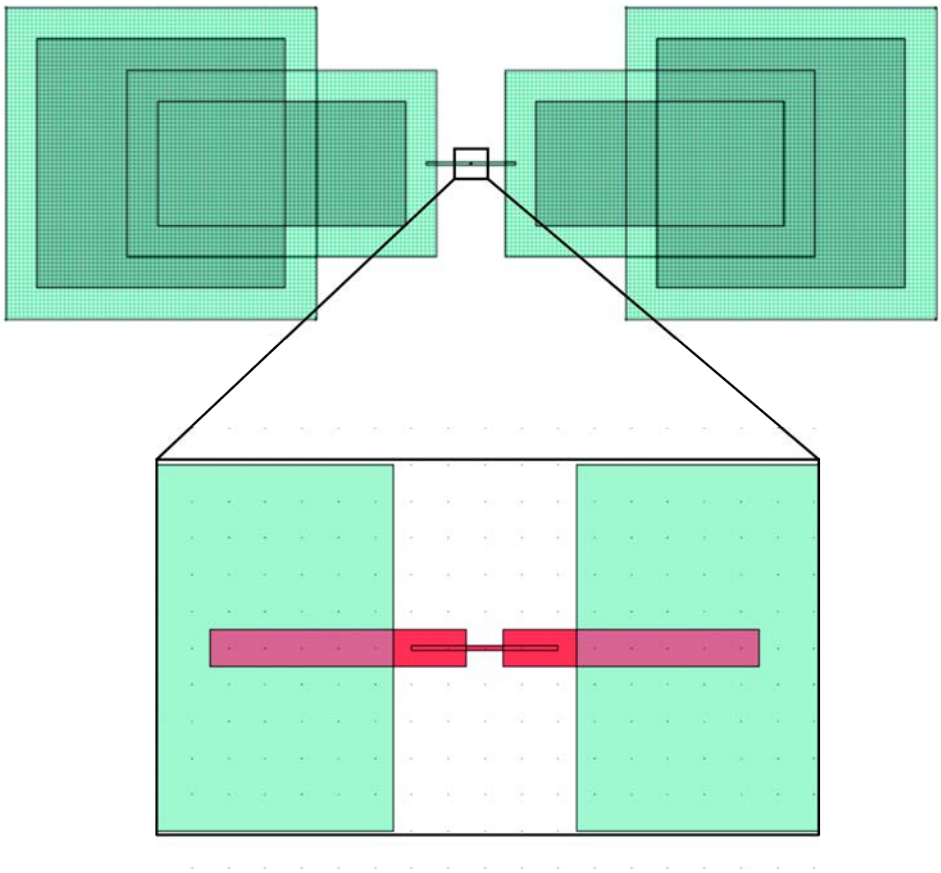

Figure 5.7: Design of nanoribbon from L-Edit. The top image shows the metal contact pads in green with the small black dot in the centre the 1 um long nanoribbon design. This is zoomed in on the bottom image to show the HSQ and graphene layer in red with the 100 nm wide graphene leads overlapping the green metal contacts and the sharp transition to the narrow 100 nm long and 10 nm wide nanoribbon in the centre.

Fabrication process to produce nanoribbons

Step 1 - Wafer preparation:

The wafer that is chosen for the base of the samples is a high conductivity 6" silicon wafer. The high conductivity is needed for finer control of the gate modulation of the devices. In particular the wafer is p-doped to a resistivity of 0.001Ohm.cm. As always the first step in preparing the wafer is to thoroughly clean it using the RCA clean method. This uses the standard clean 1 & 2 solutions and a hydrogen fluoride (20:1 concentration) dip. Standard clean 1 is a mixture of water, ammonium hydroxide and hydrogen peroxide to remove organics and particles. This step has the effect of oxidising the wafer. Standard clean 2 is a mix of water, hydrogen chloride and hydrogen peroxide. This step is to remove any metal contamination. Both Standard clean 1 & 2 are heated to ~75°C and left for 10 minutes. The Hydrogen Fluoride is the final step and is used to remove any oxide built up on the wafer from the previous cleaning step. In between each step the wafers are rinsed in a quick dump release tank for about 10 minutes [111].

After this the wafers are oxidised in a dry oxidation furnace tube for 131 minutes at 1000°C to achieve a thickness of 90 nm. 90 nm is chosen so that the graphene is visible after the transfer, since the quality of the graphene transfer is easier to interpret visually. The dielectric breakdown can be calculated as 0.5 V/nm, so the highest gate voltage range for measurement is +/- 45 V before the dielectric fails. The reason for using 90 nm instead of the standard of 300 nm used for graphene devices is the greater gate modulation of the graphene devices.

Next the oxide is removed from the backside of the silicon wafer. This is done by coating the front side with S1813 resist, the resist chosen for the minimal residue and ease of removal compared to other resists. The wafer is then left in the 20:1 ratio HF tank for 5 minutes, based on an etch rate of 0.5 nm/s. Once the oxide has been removed there are two options to strip the oxide from the front side of the wafer; fuming nitric acid or oxygen plasma ashing. The latter is chosen for these wafers since it provides the benefit of negatively shifting the Dirac point of the devices. This is especially important when coating with HSQ, where the Dirac point could be shifted to around 20V or more if it is not compensated for.

Alignment marks are made using e-beam with ZEP 520A for a 1 μm etch into the wafer using the RIE80. If the marks are etched any less than 1 um the e-beam system will have trouble scanning across the alignment marks. The process is show in the schematic diagram of figure 5.8.

Step 2 - Graphene transfer:

The graphene used is from BGT-Materials and comes in a size of 4 x 4 inch and comes on a copper foil stuck to a piece of PET plastic sheet. The commercial graphene has an advantage over the in-house graphene since it is electrostatically stuck down to a piece of PET for transport. This ensures the copper foil remains smooth and reduce the

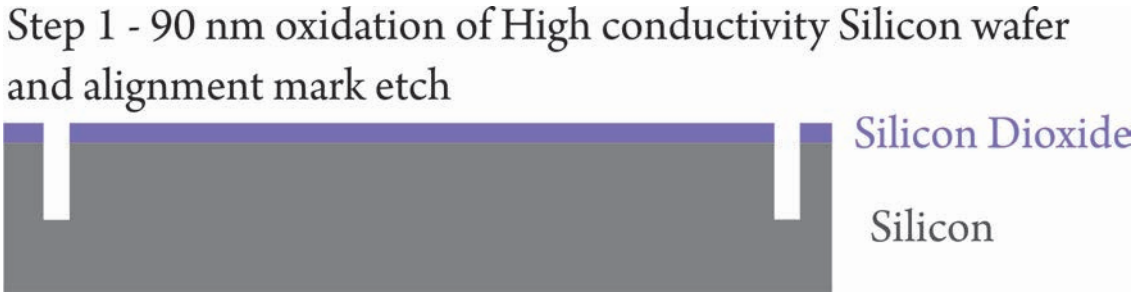

Figure 5.8: Schematic diagram of step 1 showing the oxidation of the wafer and etch of the alignment marks into the wafer

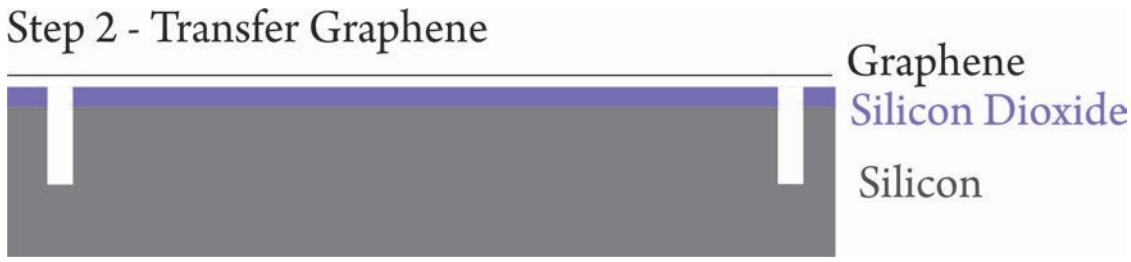

Figure 5.9: Schematic diagram to show the graphene after the transfer on the target substrate. The graphene is shown to suspend across the alignment marks in the diagram but will be broken and pull to the inside of the alignment marks for the actual transfer. If the graphene was suspended across the alignment it would cause issues with the e-beam system since a SEM is used to detect the height change in a sample from the contrast of the edges. A suspended graphene layer would prevent this.

number of wrinkles when spinning on the supporting resist. The reason a commercial supplier is used for these devices is due to the in-house CVD-graphene LPCVD tube had broken and was unable to be fixed in time. The graphene is then transferred using the process detailed in section 3 and shown in figure 5.9 for the schematic diagram.

Step 3 - Contact deposition:

The best method for depositing metal contacts using e-beam lithography lift-off process using a resist bilayer composed of MMA and PMMA. The MMA is in contact with the graphene layer so the previous issues using PMMA did not occur again. The decision was made to pattern with metal contacts first, since the HSQ is left soft with no post bake annealing to prevent any issues with $210°C$ heat causing bonding with the graphene. Due to the HSQ remaining soft, it was a concern that a second spin coat and bake with MMA/PMMA would ruin the first HSQ layer. This should also have the added benefit of improving the contact resistance as the only residue will be from the PVB layer after the graphene transfer. The metal is then deposited using a Leybold LAB700 e-beam evaporation system to deposit a 10 nm layer of titanium and a 70 nm layer of aluminium. The MMA/PMMA is then stripped using NMP overnight to lift off the unwanted metal. Figure 5.10 shows the graphene layer underneath the MMA/PMMA after the e-beam exposure. While figure 5.11 shows the devices after the metal lift-off but before the device patterning.

Step 4 - Graphene nanoribbon fabrication:

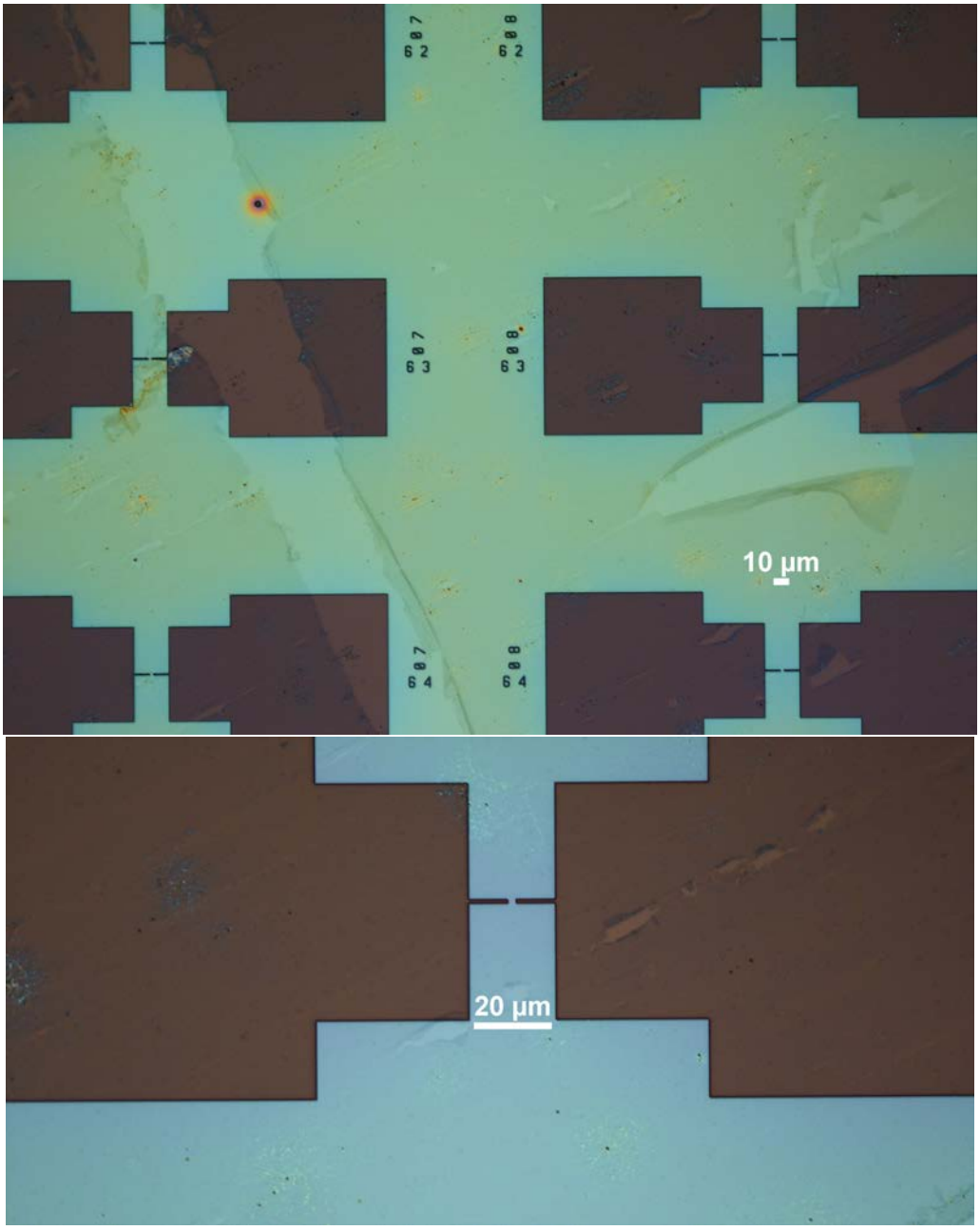

Figure 5.10: Optical images of devices after E-beam exposure of the first metal layer. As highlighted the MMA/PMMA is the faint green and blue layer in the top and bottom images respectively. The graphene layer can be seen through the MMA/PMMA layer. The top image shows the large area of graphene produced with some wide cracks visible on the sheet. The bottom image shows the graphene that is not broken when zoomed in is still of a good quality with minimal residue on the exposed area.

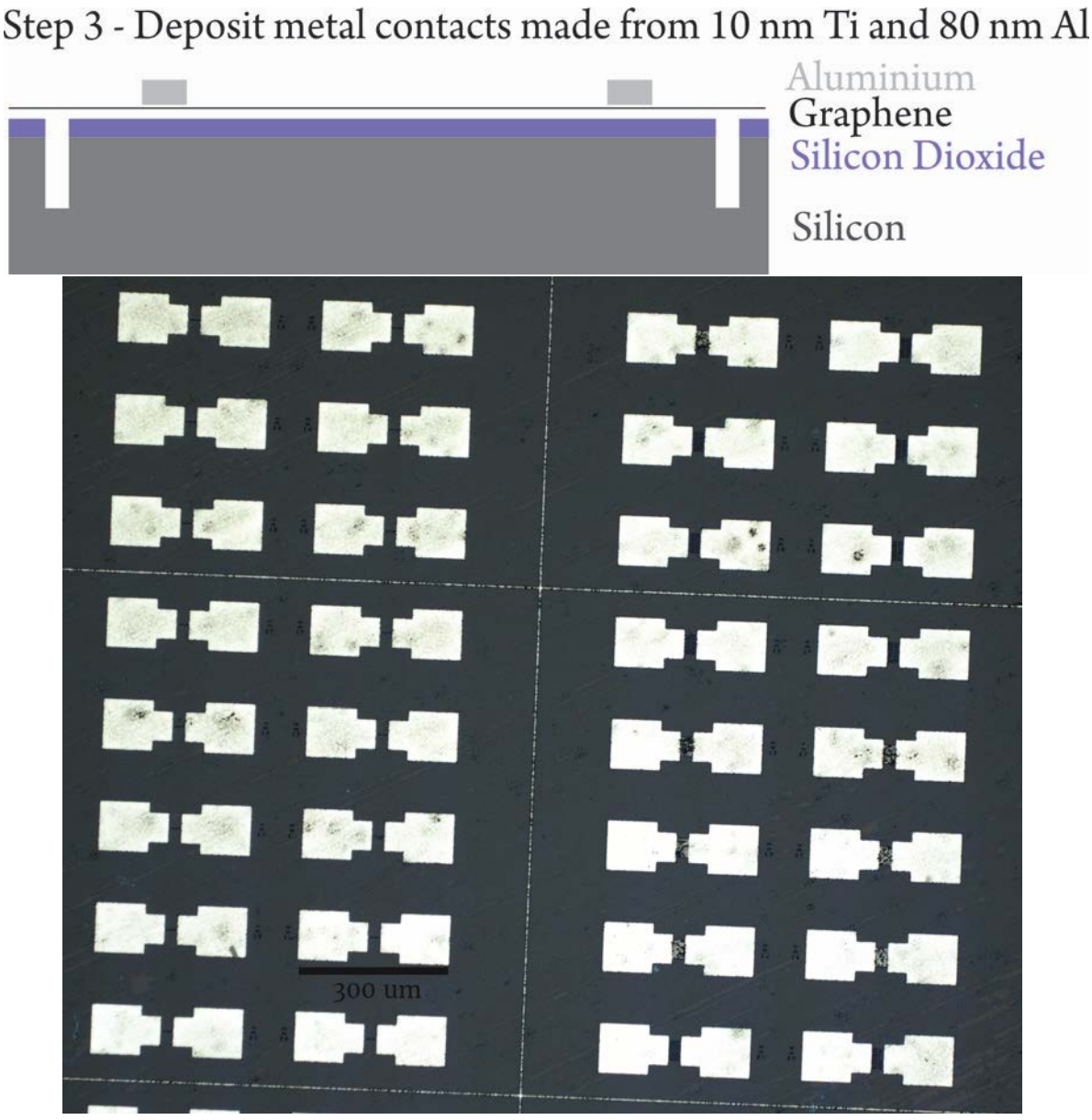

Figure 5.11: Top: Schematic diagram of the metal lift-off on graphene. Bottom: Optical image (5x zoom) of the metal transferred onto the graphene after lift off .

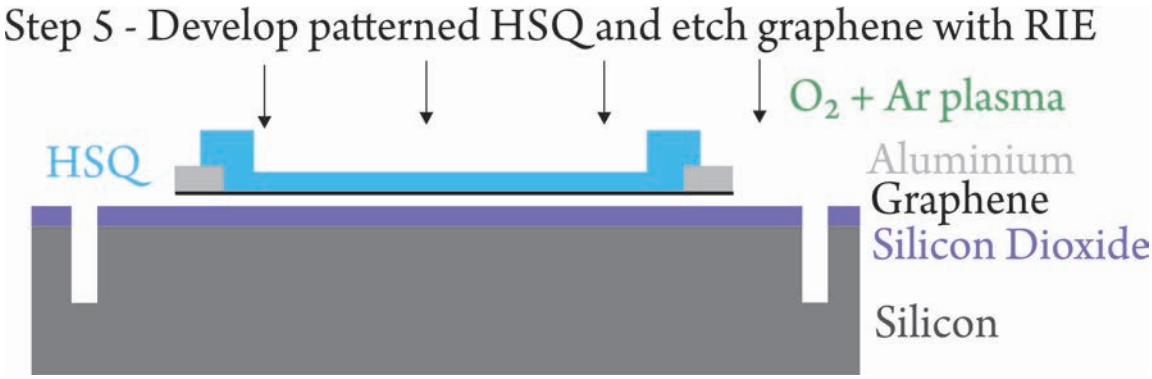

Figure 5.12: Schematic diagram showing the final device after HSQ development and RIE etch of the graphene layer

Finally, a 30 nm thick 2% HSQ (produced by Dow corning) is spun onto the graphene. The resist is developed using MF319 for 3 minutes and left to dry in a vacuum oven at 40 C. The graphene is etched for 30 seconds using a 15 W plasma at 30 mTorr pressure and a gas flow of 20 sccm argon and 5 sccm oxygen, this is shown schematically in figure 5.12. The etching is confirmed by SEM can be seen by the distinct difference in contrast between before and after the etch.

As expected the HSQ layer did not produce a 1 nm wide mask layer on top of the graphene. From the SEM images the minimum width that was achieved for the 100 nm long nanoribbons was ~20 nm. A selection of these devices were imaged after the HSQ development. As can be seen in figure 5.13 of the smallest designed width of 1 nm the small width achieved was 19 nm but could be up to 27 nm for the same device, while figure 5.14 shows the result from a much wider designed nanoribbon of 41 nm. In figure 5.15 the device is compared after etching to determine the transition angle that was achieved with the lithography process. On the right hand side is an image of the device at a $50°$tilt to show the success of the HSQ spun coat after the metal contact deposition. While in figure 5.16 the AFM after the graphene etching shows the metal contacts and HSQ layer without any visible graphene surrounding the device.

Finally, an issue that was not expected when fabricating these devices is that the use of a E-beam evaporator to deposit the metal did not adhere strongly to the graphene. Although all the devices lifted off successfully, the contact pads themselves did not withstand repeated scratching with the probe needles for measurement. It was later discovered by colleagues at JAIST that it was not possible in their lab to deposit metal directly onto the CVD-graphene, with most of their devices lifting on. The reason this fabrication process has assumed to have yielded devices is due to the higher impact velocity of the metal in the evaporator used in the Southampton Nanofabrication Centre. Future devices will use an extra fabrication step to pattern the contacts in two stages. First the contacts pads for the devices is patterned on the sheet, the graphene will be etched first before the metal deposition to improve the adhesion of the metal. Second the wires bridging between the contact pads and graphene device, this allows for a thicker pad contact to allow the devices to be wire bonded.

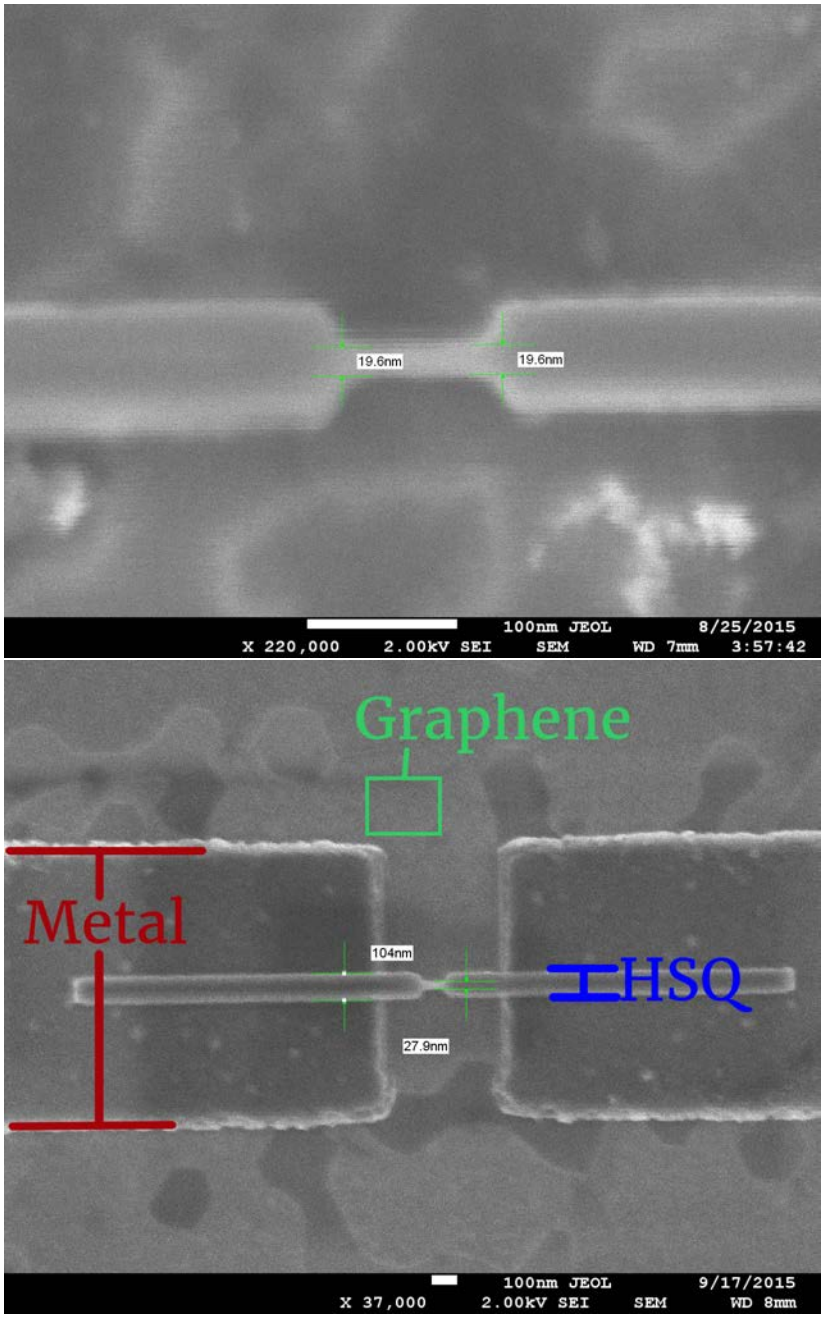

Figure 5.13: SEM images after HSQ layer development but before etching for devices on 1st row of exposures, where a single beam line was drawn with e-beam system. The minimum width achievable is between 19 and 27 nm for a single spot size. The lighter contrast of the graphene can be seen surrounding the HSQ and metal contacts with some defective nanopores in the graphene sheet.

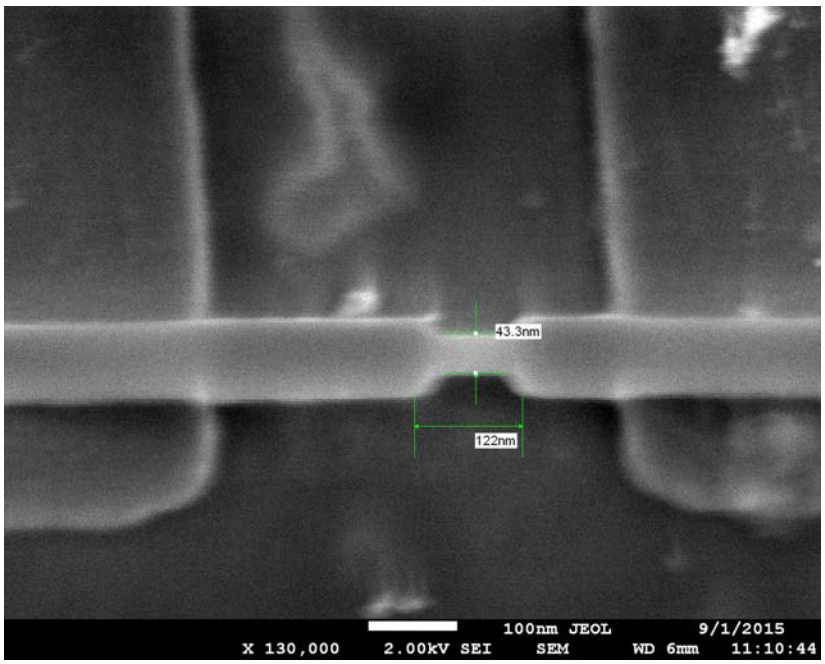

Figure 5.14: SEM image of device at row 41 (41 nm designed width) which gives a HSQ width of 43 nm. The dose for the HSQ is more accurate at wider patterning widths. Although not shown was accurate from row 20 (20 nm) and upwards. This means any rows smaller than row 20 can all be assumed to be 20 nm and the increase rows can be assumed to be within a 5% tolerance for the dimension achieved.

5.3 Simulation Results

Using the theory established in Chapter 3, the properties of the designed devices can be predicted. Since the devices use CVD-graphene and a 90 nm oxide, the expected change in device characteristics from the standard equations in Chapter 3 can be calculated. Both methods for extracting the nanoribbon widths of the devices using the transport gap and bias energy gap method are found, where in the ideal case both of these methods would show similar results.

The first calculation is the expected magnitude of the Fermi energy gap that can be found based from the maximum transport gap that could be measured. The maximum transport gap that can be measured for the devices is determined from the maximum possible gate voltage sweep achievable for a 90 nm oxide, which is 80 V. The other change to the equation is the gate oxide capacitance per unit area used. Here the standard parallel plate capacitance with the additional fringe field capacitance from Guttinger (2012) is used [11]. For the devices the gate oxide capacitance is determined to be $5.75\text{x}10^{-4}\text{F/m}^2$, compared to the 300 nm oxide which has a value of $1.5\text{x}10^{-4}\text{F/m}^2$. The difference between the maximum Fermi energy gap that can found is shown in figure 5.17. For instance a 0.45 eV Fermi energy gap can be found with a 25 V transport gap for a 90 nm oxide whereas a 300 nm oxide needs to measure an 80 V transport gap. This show the greater gate modulation of the graphene devices that can be achieved with a 90 nm oxide. Although a 300 nm oxide would still be able to find the same Fermi energy gaps as a 90 nm, there is usually a limitation for measuring devices with a higher gate

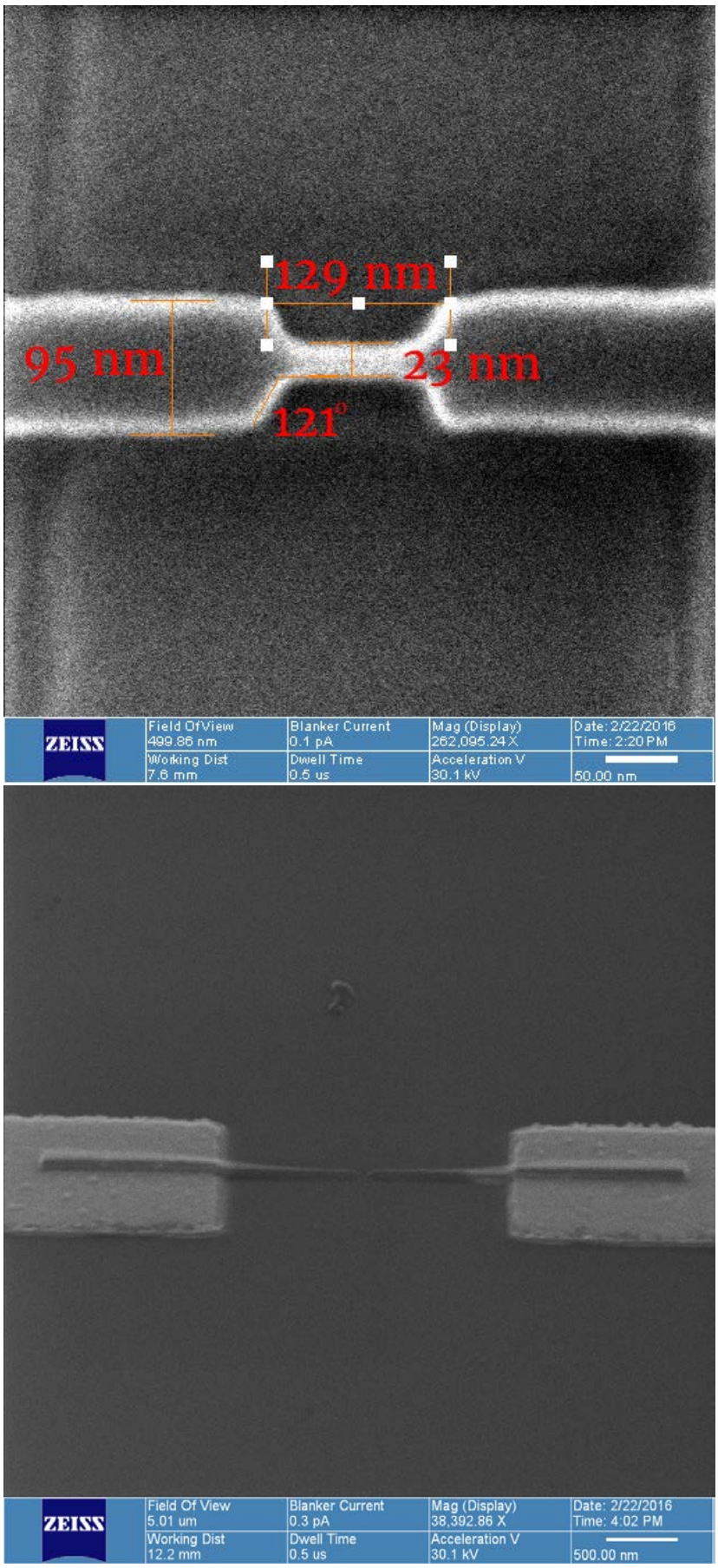

Figure 5.15: Top: Helium Ion Microscopy image of the measured transition angle and different widths of the HSQ pattern. Bottom: HIM image of the device at a $50°$tilt after the graphene etch, the HSQ can be easily visible surface of the substrate and the metal contacts. Compared to the previous figure the high contrast of the graphene is no longer visible showing a successful etch of the graphene layer with RIE.

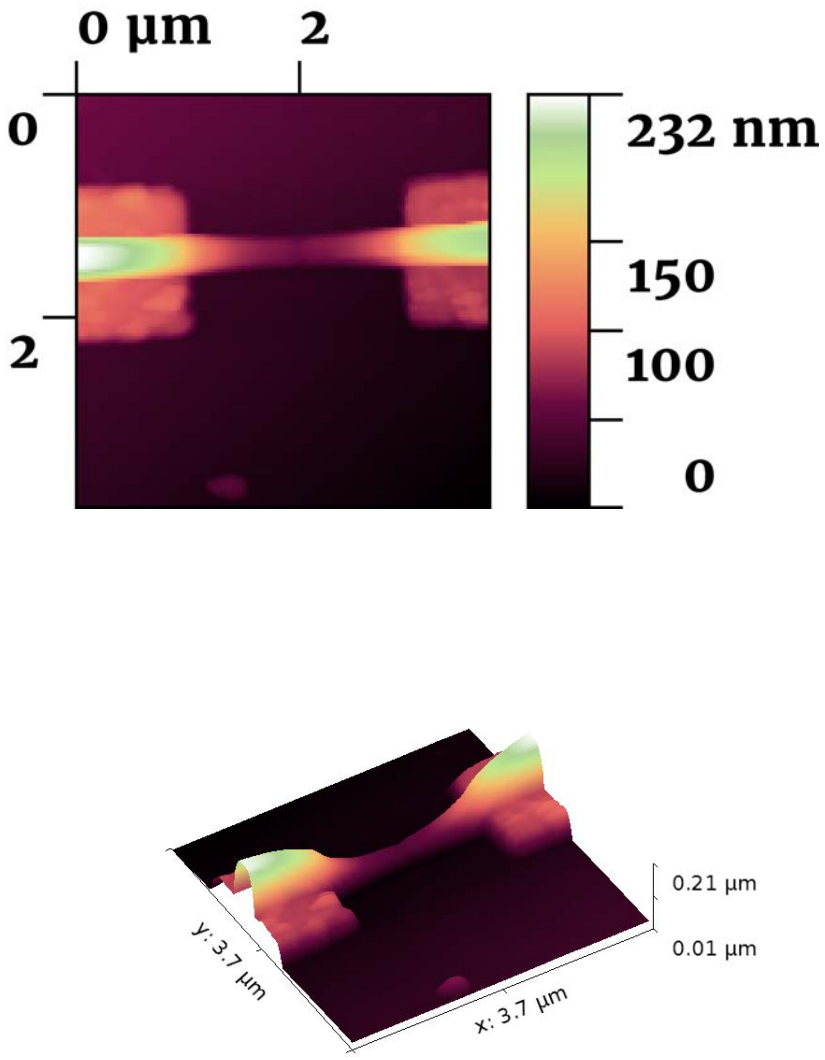

Figure 5.16: AFM image of a device after the etch has finished. The HSQ profile shows an encapsulation across the contacts and the clean surface surrounding the device further demonstrates the etching removed the graphene. The AFM was unable to image constriction in the HSQ but it can be seen clearly in the HIM images.

voltage swing of +/- 40 V. For this reason the 90 nm is shown to be a more viable oxide thickness for measuring graphene devices.

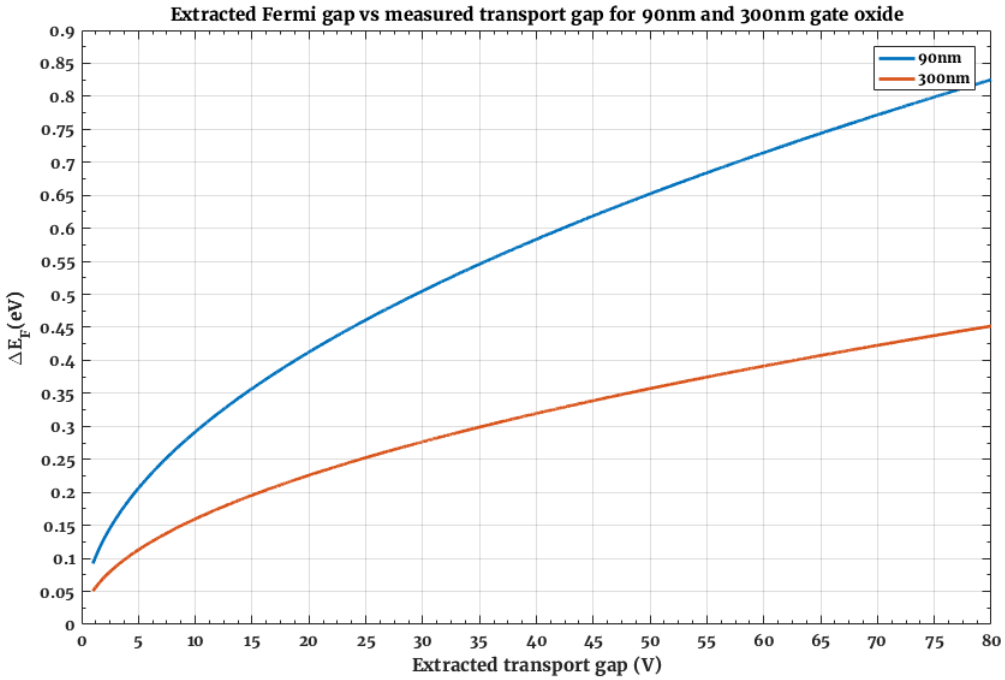

Figure 5.17: Theoretically possible extracted Fermi energy gaps against increasing measured transport gap. The difference between measured Fermi energy gaps for different oxide thicknesses is shown.

Secondly, the different nanoribbon widths from 100 nm to 5 nm is calculated to show the Fermi energy gap that can be expected from the different confinement energies of bulk (exfoliated) and CVD-graphene, where the carrier density fluctuations in CVD-graphene has a disorder potential and so a higher confinement energy. So the disorder potential now has a value of Δ_{dis}= 0.5759 eV compared to 0.1043 eV for bulk (or exfoliated) graphene. The CVD-graphene disorder potential is calculated from the carrier density fluctuation given in "Scaling properties of charge transport in polycrystalline graphene" [112] to give a carrier density fluctuation of $\Delta \mathrm{n} = 6.1\mathrm{x}10^{-16}\mathrm{m}^{-2}$. This gives a better approximation of the maximum Fermi energy gaps that can be expected from CVD-graphene nanoribbons. In particular the smallest nanoribbon measured of 20 nm would give a maximum Fermi energy of ~ 0.8 eV, this means the devices could show a transport gap of up to 75 V. With a maximum voltage swing of 80 V means it may be difficult for the most disordered nanoribbons to be measured.

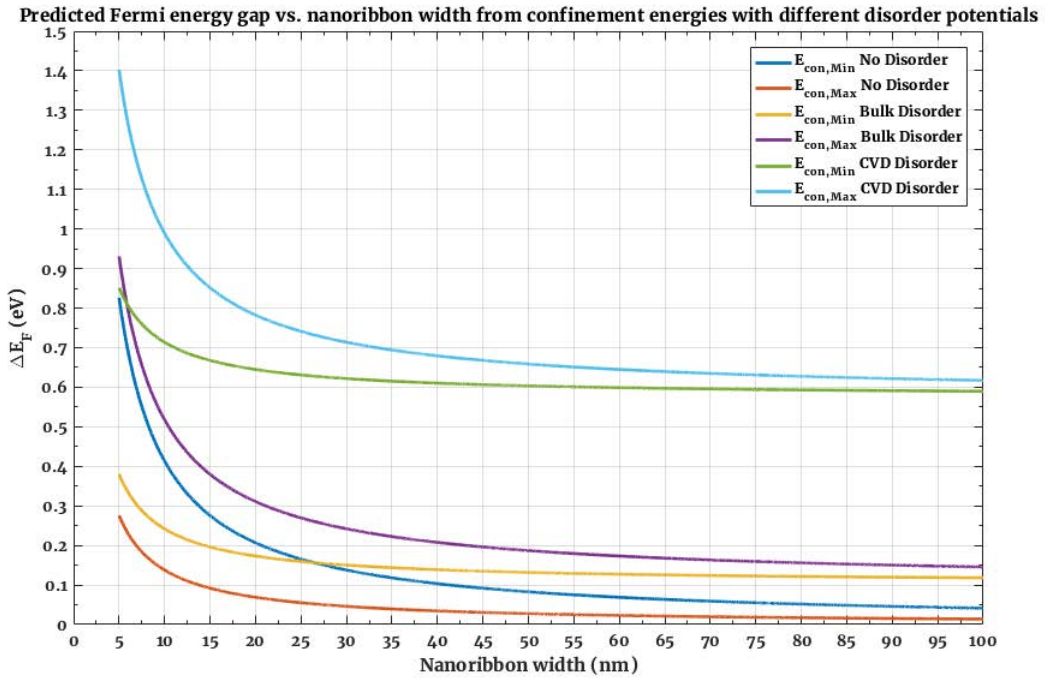

Figure 5.18: Predicted Fermi energy gap for different disorder potentials

Further to this if the assumption of a constant CVD disorder potential is true then it will not be possible to observe a transport gap below 40 V for the designed devices if the largest nanoribbon width of 100nm is achieved. Taking this further figure 5.18 shows a small variance in magnitude of the predicted Fermi energy gap for nanoribbons of 40 to 100 nm in width. A maximum possible variation in transport gap will be between ~41V and ~43.8V. Meaning only a 3V difference will be observed. Which, considering the subjective nature of how to extract the transport gap from the Id/Vg graphs could mean it will be difficult to distinguish between a 40 nm and 100 nm device experimentally.

Lastly the SET electrical characteristics for different dot diameters is calculated to determine the estimated back-gate capacitance that can be extracted from the devices electrical properties, as shown in figure 5.19. This is again estimated using a 90nm oxide with an increase in capacitance from fringe fields. For the smallest achieved device an expected a back gate capacitance of around 0.18 aF can be predicted. But could be as low as 0.045 aF if a 10nm over-etch of the graphene is achieved. It is possible for the RIE to cause a 10nm undercut from the designed HSQ width based on previous results in literature [2].

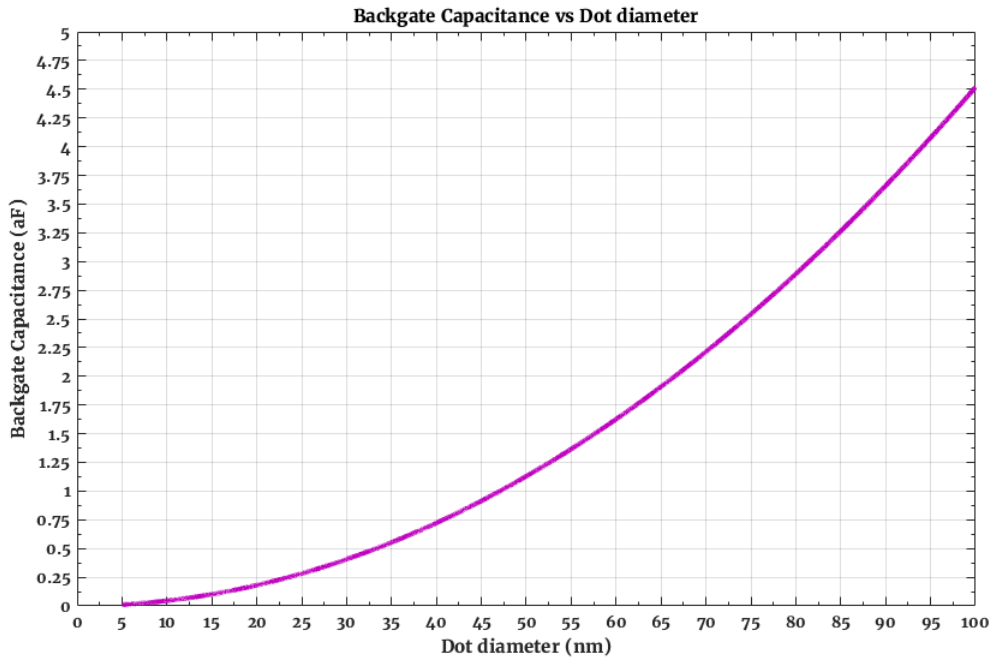

Figure 5.19: Quantum dot diameter against the possible backgate capacitance that can be extracted for a device with a 90nm oxide

Using these results the single electron tunneling characteristics are predicted to give the expected Coulomb oscillations observed within the transport gap and the associated stability diagram for the smallest device that has been achieved from the fabrication is shown in figure 5.20. The diagram shows the calculation for a 20 nm HSQ nanoribbon on a 90 nm oxide. The ΔV_g is determined to be 920 mV and ΔV_d to be 25 mV. Although a ΔV_d of this size would suggest the device can be measured at room temperature ($k_b T$ = 25.6 meV at 300 K), the temperature needs to typically be at least a tenth of the thermal energy. So for a 20 nm nanoribbon the maximum measuring temperature should be around 29 K.

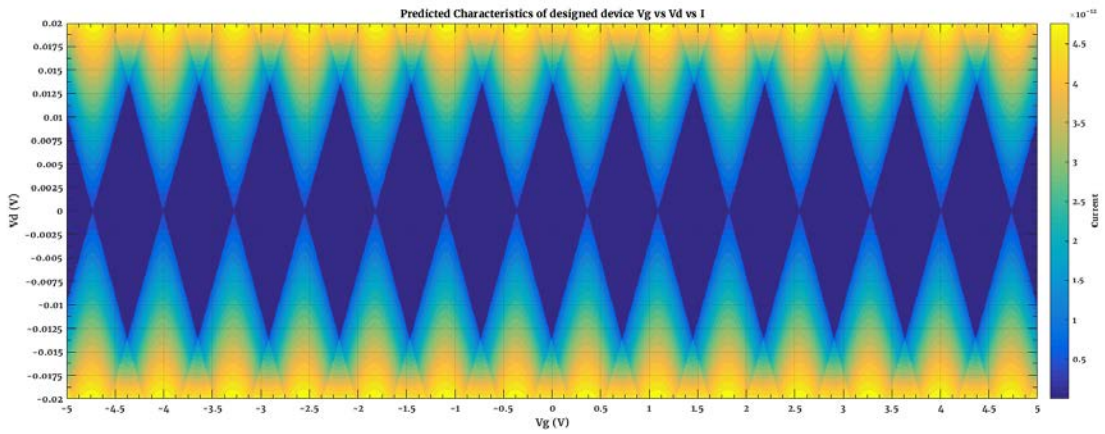

Figure 5.20: Stability diagram of expected graphene Nanoribbon SET if it is 20 nm in width. Calculated using the MATLAB implementation of a CAMSET simulation [26].

5.4 Electrical Characterisation

The capabilities of the measurement system allow for a maximum 2 cm^2 sample size, which means multiple devices can be measured at once. Since the aims are to measure both the scaling properties of the nanoribbons and the SET properties the devices will be cooled down to the minimum possible temperature for the system of 4.2 K. This is to compensate for the largest devices, which will need below 10 K to be able to accurately determine their SET properties. This also has the added benefit of reducing the thermal noise from the samples as much as possible and provide clear transport characteristics for the smallest devices. The key properties for both the effect of scaling on the transport gap and the SET properties can be determined using the same electrical measurement. By measuring the devices with a gate voltage sweep at different drain voltages will provide the optimal amount of information on the devices that will be measured. This allows the time spent measuring the devices at low temperature to be spent more efficiently. The measurements focus on finding the transport gap and SET properties simultaneously by measuring the Id/Vg at different Vd voltages. Typically SET devices measure the Coulomb blockade using Id/Vd at increasing Vg to obtain the stability diagram. For graphene the Id/Vg sweeps give more information on the relation between the transport gap and Coulomb oscillations that occur in the devices, which is why the focus of the measurements is on the Id/Vg sweeps.

The results of the measurements follow the format of first demonstrating the individual devices to highlight the unique characteristics of the devices. The divergent behaviour from exfoliated graphene is discussed and the transport gap and Fermi energy gap properties are discussed for devices of increasing width and length. Lastly the single electron transistor properties of the CVD-graphene nanoribbons are analysed and discussed.

5.4.1 Narrow CVD-graphene nanoribbon

Device 17-100 demonstrates the closest transport properties to the typical result expected for a graphene nanoribbon. This device is designed to be 17 nm wide and 100nm. The device is measured at 4 K in the Nagase probe station at different drain voltages from 4 mVd to 200 mVd in 4 mVd steps at both positive and negative drain voltages. The gate voltage is swept from - 40 to 40 V in 0.1 V steps. Figure 5.21 is a plot of the device at 4 mVd. Coulomb oscillations of varying peak heights and differing number of peaks for each tunneling event is seen across the gate voltage sweep.

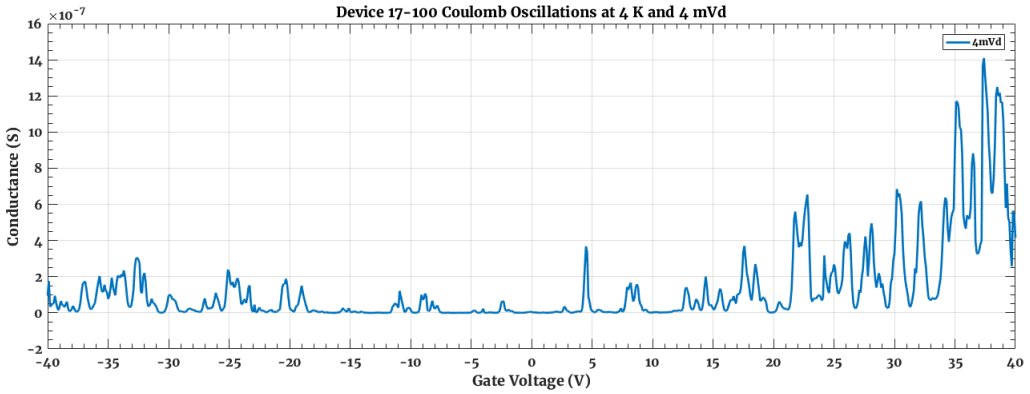

Figure 5.21: 17 nm wide and 100nm long device at 4 mVd. The characteristics at 4 mVd show the expected supression of current in the centre of the device around the -5 V dirac point. Of note is the increased height of the peaks from the Coulomb oscillations for successive tunneling events in the device both inside and outside the suppressed current region of the transport gap.

As can be seen in the figure there is a central region where the current is mostly suppressed from the Fermi energy gap resulting in a transport gap in the Vg sweep. Inside the transport gap there are regions of fully suppressed current interspersed with sharp multiple peaks. Unlike devices reported in literature the conductance peaks within the transport are large and compare in height to outside the transport gap. This indicates the device acts better as an SET than as a nanoribbon FET due to the dominant behaviour of the Coulomb oscillations creating an imbalance between the quantum regime, where electrons are transported by hopping through different quantum states compared to the Fermi energy gap dominant behaviour, where the tunneling of electrons is strongly suppressed resulting in very small conductance peaks.

An additional property of this device is the large fluctuation in conductance from the Coulomb oscillations that are still visible outside of the transport gap. Which, even for SETs fabricated using the double quantum point contact constriction method do not demonstrate such clear oscillations [10]. Indicating the coupling between the quantum dots formed by the charge localisation of electrons and holes within the nanoribbon is coupled differently to those found in literature. Although the typical graphene nanoribbon or quantum dot will show some oscillation outside the transport gap [72] the extent of the peaks and troughs produced with this device is further exaggerated. Further to this point the conductance measurement is significant, with the largest peak in the transport gap measured at 0.4 uS. A conductance peak height of 0.4 uS is below the quantum conductance limit of 154 uS to indicate the devices at 4 mVd are operating within the regime for a quantum dot rather than a classical SET. This is an important difference to devices in literature. In literature the peak height of the resonances in the transport is very small compared to the increase in conduction outside the transport gap. Here peak heights are comparable to the increase in conduction outside of the transport gap are observed.

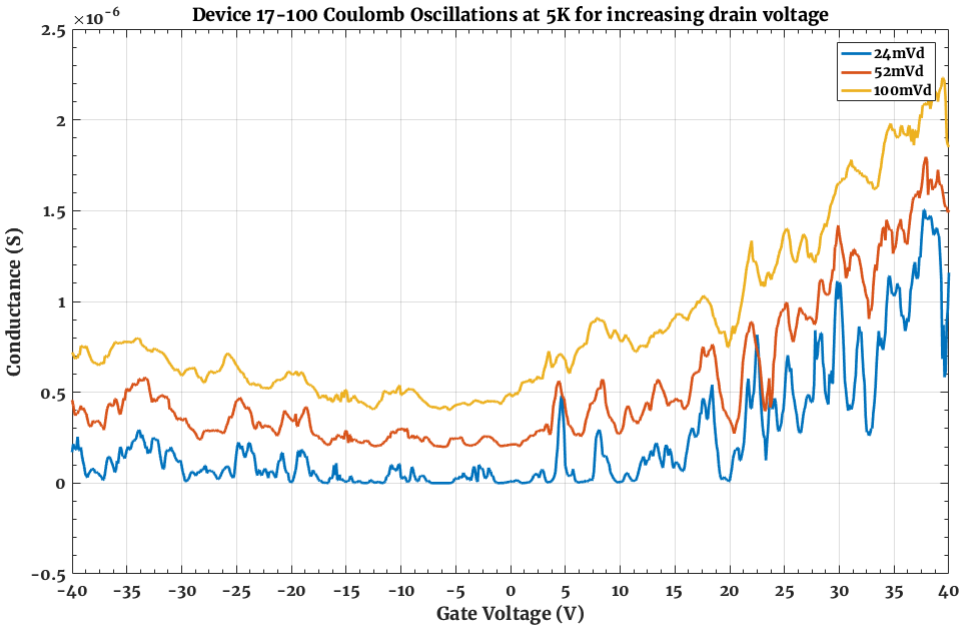

Figure 5.22: Electrical measurement of device 17-100 at mid-low to high drain voltages and offset by 0.25 uS for clarity. The transport is still visible for the device at 24 mVd but is suppressed as the drain voltage decreases along with the clear Coulomb oscillations.

As the drain voltage increases in figure 5.22 the transport of electrons through the quantum dots is slowly suppressed as seen in the measurement at 100 mVd, where the Coulomb oscillations are suppressed resulting in a device where the conduction continues to increases in a steadier pattern. Although some of the key peaks in the Coulomb oscillation can be observed still as the voltage increases. The variation in peak shape and height of the conductance fluctuations is a signature of the quantum states within the nanoribbon as the electron is permitted through multiple conductance paths across h the device at different gate and drain voltages. Although the exact state and type of hopping that occurs within the quantum dot is undefined. It can be predicted that the transport occurs through multiple dots across the nanoribbon and up and down through different energy levels. If the nanoribbon device fits the current model to create multiple dots of varying dimensions within the nanoribbon leading to multitude of possible transport mechanisms across the device.

The off and on ratio of the device is extracted at 24 mV drain voltage to give an on/off ratio of 1500, where the off conductance is 1 nS and on conductance is 1.5 uS. This is a reasonable value for a nanoribbon and is comparable to other efforts with CVD-graphene, which extracted a value of 10^3 [113]. This shows that CVD-graphene nanoribbon is capable of acting as a nanowire FET at 4 K with intrinsic SET properties without the need to design the device into a quantum dot.

5.4.2 Increasing device width

Increasing the device width yields the expected result of decreasing transport gap size with increasing device width. The change in width is observed across 4 different device widths from 17, 31, 51 to 81 nm. The data in figure 5.23 has been offset to show different size in transport gap clearer.

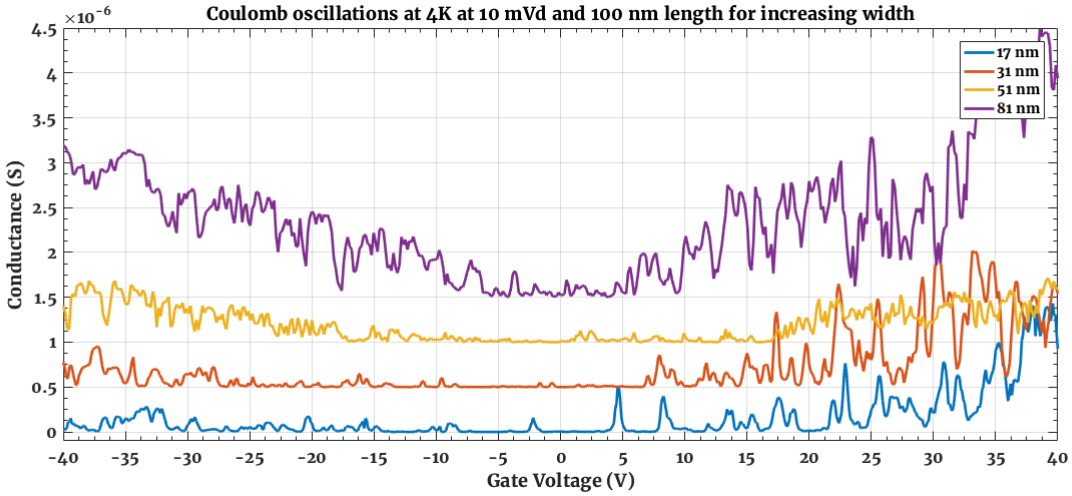

Figure 5.23: Comparison of devices at 10 mVd for increasing nanoribbon width. The devices all show a decreasing transport gap with width and strong fluctuations in conductance due to the dominant transport of electrons and holes through the quantum dots.

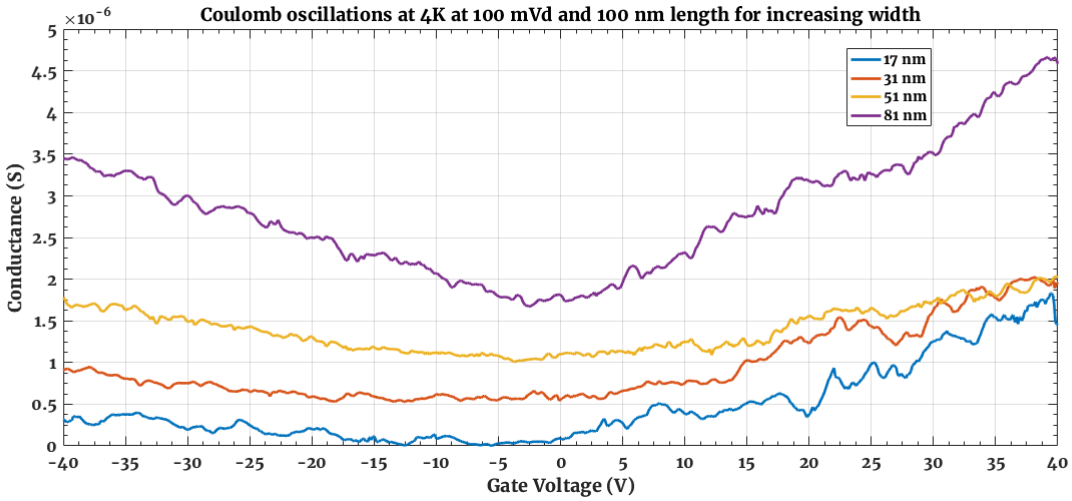

Figure 5.24: Comparison of devices at 100 mVd for increasing device width shows the strong suppression of the Coulomb oscillations when the devices are no longer dominated by the transport through a quantum dot. The devices now operate with the expected ambipolar conduction expected for a graphene transistor.

As the device width increases the decrease in transport gap causes a slight change in the transport characteristics. At low drain voltages the Coulomb oscillations are still visible outside the transport gap for all devices but the increase in conductance outside

transport gap is less suppressed as the width of the nanoribbon increases. The difference between figure 5.23 and figure 5.24 between low and high drain voltages shows the impact a quantum dot mediated transport has on the properties of the devices even at a width of 81 nm. At low drain voltages the multiple peaks and troughs from the Coulomb oscillations is visible for all the devices except as the gate voltage increases away from the dirac point (~ -5 V) the rate the conductance increases for the wider devices is much greater. The signatures and shapes of the peaks varies from the smallest to the widest device, where the 17 nm wide device shows some distinct single peaks, but as the width increases more energy levels are available for the electrons to transport across the nanoribbon resulting in the continuous multi-peak shape observed in the 51 and 81 nm wide devices. However, once the drain voltages has increased to beyond the regime of quantum dot mediated transport the electrical spectra of the devices is similar, where the consistent parabolic curve associated with graphene devices can be observed.

5.4.3 Increasing device length

The increase of the device length yields a divergent behaviour than expected from the literature. Devices 17-200 (200nm long) and 17-500 (500nm long) demonstrate a change in the transport gap.Where device 17-500 shows a smaller transport gap than those measured for 17-100 and 17-200 discussed in section 4.5. Which shows an unexpected change since the gap is supposed to be a property independent of changes in length [2]. With the devices showing the increase in device length alters the electron transport properties through an increase in the number quantum dots available due to the increasing length. Although the devices do show a consistency with the literature for devices where an increase in the bias voltage gap for devices of increasing length is observed. This means the change in properties can be associated with the effect from using CVD-graphene to produce the nanoribbons.

As can be observed for the two devices individual characteristics in figures 5.25 and 5.26 the Coulomb oscillations are much clearer outside the suppressed current region. With almost no peaks observable for device 17-500 inside the gap unlike 17-100, while 17-200 shows a decrease in the number of observed tunneling events within the transport gap as well. The devices of increasing length show that the SET properties and Fermi energy gap are not directly related. When the device length increases the energy required for an electron to tunnel through the is increased. Resulting in a stronger suppression of the Coulomb oscillations within the transport gap and a decrease in the conductance outside as seen in the comparison between the different lengths in figure 5.27.

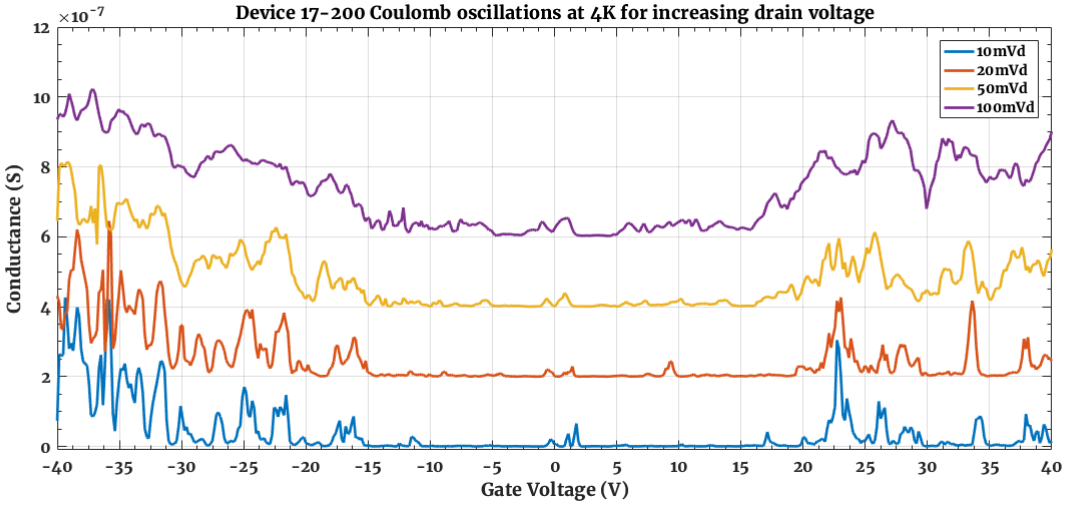

Figure 5.25: 17 nm wide and 200 nm long device for increasing drain voltages and offset by 0.2 μS. The device shows a stronger suppression of the Coulomb peaks within the transport gap around the Dirac point of -5 V. Of interest is the change in peak shape as the drain voltage increases. Single peaks can be observed splitting from the increase in the number of energy levels available for transport. Although the Coulomb oscillations are mostly suppressed at 100 mVd the transport gap is still visible correlating with the theory for a device of increase length causing an increase in the observed source-drain gap for the Fermi energy gap.

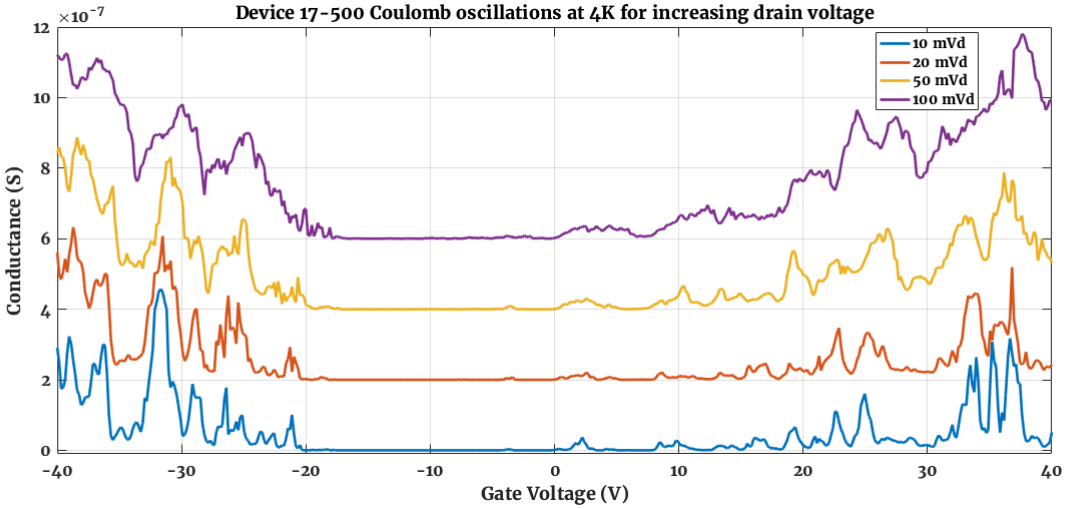

Figure 5.26: 17 nm wide and 500 nm long device for increasing drain voltages and offset by 0.2 μS. Outside the strongly suppressed conductance around the Dirac point the device still exhibits clear Coulomb oscillations. But observed peak shape devolves much quicker for increasing drain voltage than those observed for smaller lengths. The same increase in source-drain gap can be seen by the increase in width of the transport gap at 100 mVd compared to 17-100 and 17-200.

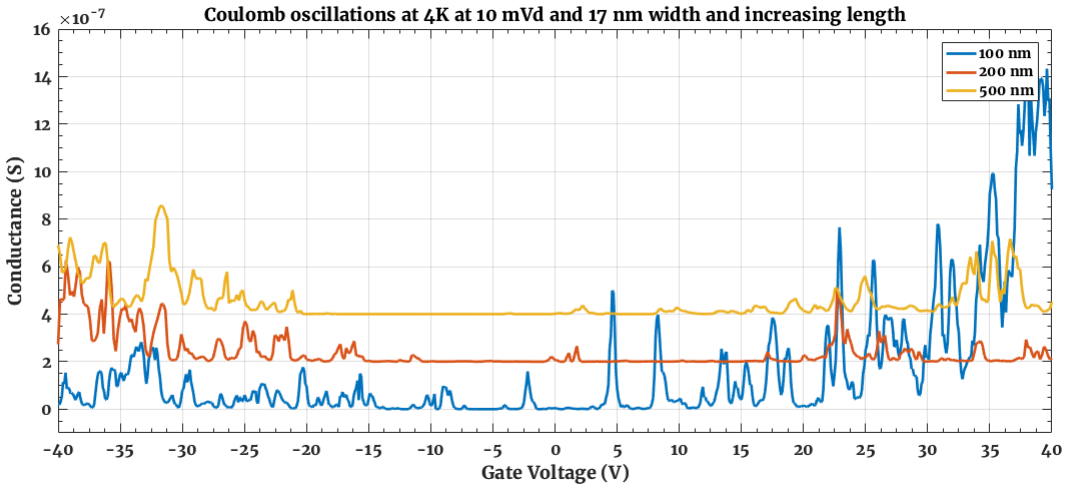

Figure 5.27: Comparisons of the Coulomb oscillations at 10 mVd for devices of increasing length with a 0.2 μS offset. The devices show that as the length increases the maximum conductance observed in the peaks decreases. This shows that as the length increase the defects in the CVD-graphene cause more scattering events and blockade from the increased number of barriers between dots to tunnel through, so the electrons are unable to pass through the device with as much energy as the shorter 100 nm device.

Where the significant difference between the devices results in the Coulomb oscillation peak magnitude within the transport gap. 17-100 demonstrates a very strong conduction for the peaks, but as the length increases the peak height decreases. With the longest device, 17-500 (500 nm) not presenting strong Coulomb oscillation peaks inside the transport gap, whereas, 17-200 (200 nm) does show a mix between the two. However, outside the transport gap the shape of the Coulomb oscillations peaks are still relatively sharp unlike the devices 51-100 and 81-100. This indicates the transport through the nanoribbon is dominated by only a few energy levels due to the much smaller size of the quantum dots. However due to the increasing number of tunneling events required for conductance the peak shape for a single tunneling event is caused by the non-linear transport regime for quantum dots [70]. Resulting in more peaks with multiple dips in a single peak rather than a single sharp peak seen in 17-100.

In the case of 17-500 the Coulomb oscillations are barely observable within the transport gap where the current is suppressed. In fact the peak heights are less than 1 nS. Which is 100 orders of magnitude less than the peaks seen in 17-100. What is interesting is when the 100 nm and 500 nm devices characteristics at 100mVd are compared in figure 5.28. Even at 100mVd the transport gap is visible for the 500nm long device, while the 100nm shows no evidence of a transport gap. This characteristic of an increasing source-drain gap with increasing length fits the literature [58]. Except the source-drain gaps observed here are much larger than the results for exfoliated graphene.

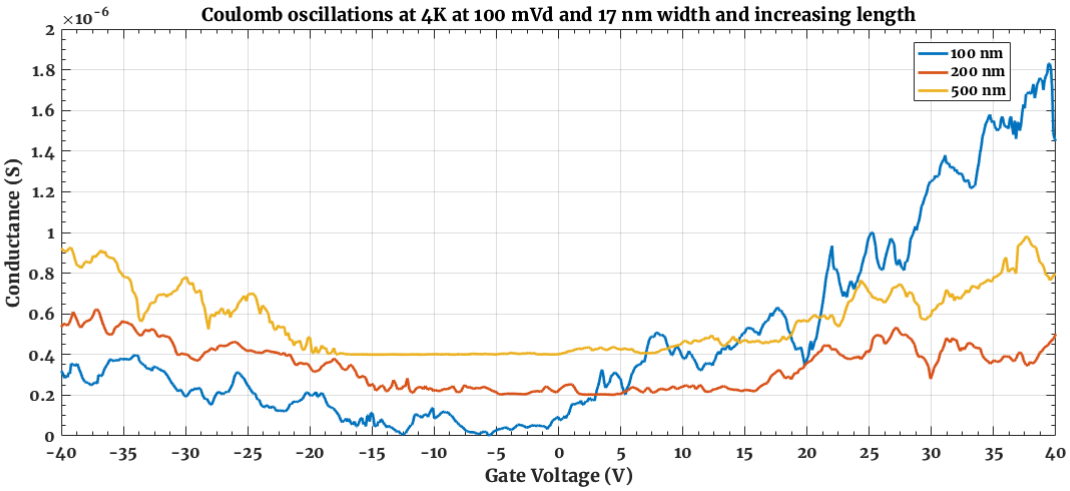

Figure 5.28: Comparisons of the Coulomb oscillations at 100 mVd for devices of increasing length and offset by 0.2 μS . The devices show that around the Dirac point the transport gap is still visible at higher drain voltages which correlates with the theory for nanoribbons of increasing length.

In 17-100 clear peaks and gaps between them are observed, but 17-500 device acts as expected for the current state of the art for a graphene SET, where the source-drain energy gap from the Fermi energy gap of a nanoribbon constriction in graphene is not related to the individual addition energies of the quantum dots formed inside the nanoribbon. Causing the single electron tunneling behaviour to exist solely within the transport gap, as outside the gap there is no fully suppressed conductance with the same minimum conductance as inside. Despite the peaks and troughs from the Coulomb oscillations visible outside. This shows an interesting transition between the number of localised states that can exist within the nanoribbon and how the interaction between them changes the device properties as the length increases.

The divergent transport properties seen as the length increases could be caused by a change in the coupling strength between successive quantum dots in the nanoribbons, where in short 100nm ribbons it is dominated by the coupling between the dots and leads, rather than the coupling between the tunneling through each dot. Hence why a much stronger Coulomb oscillations and a stronger conduction outside the transport gap is observed. So that the transport is dominated less by quantum dots in the ribbon because the increase in disorder from the CVD-graphene increases the size of the electron-hole puddles. But, as the length increases the transport is dominated by the large number of tunneling events that has to happen for the electron to conduct through the device and the change in energy required for the electron to conduct across the nanoribbon. With only 3 devices measured of a similar width more investigations would need to happen to verify this and account for any anomalous behaviour observed in any of these devices.

5.4.4 Clear Coulomb oscillations

Device 22-100 produced the most remarkable transport properties of all the graphene nanoribbons measured so far. Clear Coulomb oscillations for multiple tunneling events of a single electron through a single quantum dot as would be expected from theory. Except with the distinct quadratic ambipolar conduction trend of graphene superimposed on the conductance peaks with increasing gate voltage. In this regard the graphene device 22-100 is more similar to a silicon SET than the typical graphene nanoribbon results previously observed (including devices fabricated by QPC/QD method). Demonstrating what could be described as a true zero-band gap (or semimetal) SET.

The device was first measured at 110 K at a couple drain voltages when trying to determine which devices survived the fabrication process and showed the clearest electrical characteristics for a graphene device. 22-100 was the first device to be measured at 10 K and then later at 25 K. The devices presented that precede this discussion were measured after.

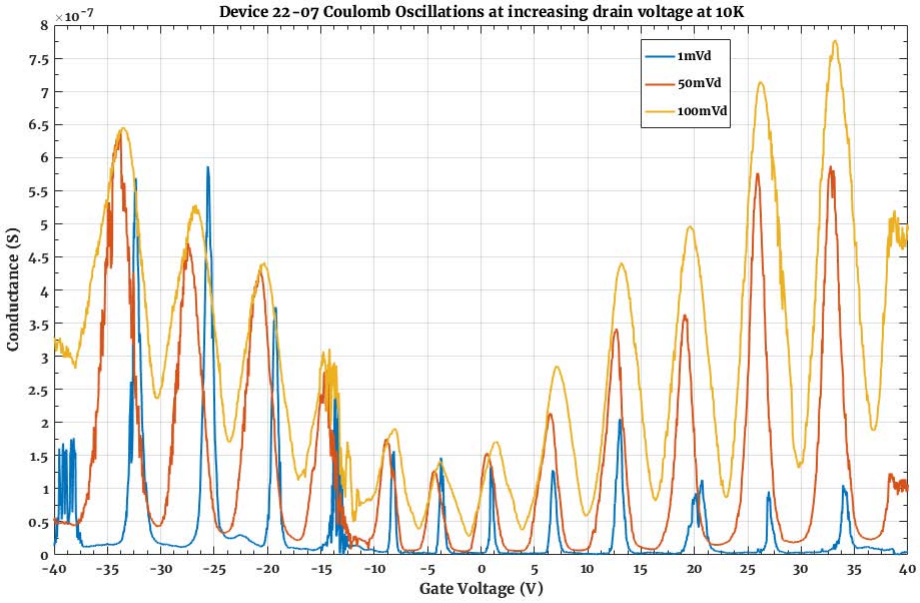

Figure 5.29: 22 nm wide and 100 nm long device for increasing drain voltages. The random variation in peak height at low drain voltages is consistent with a quantum dot rather than classical SET Coulomb oscillations properties. As the drain voltage increases the peaks and troughs show a consistent parabolic trend, where the quadratic ambipolar conduction of a graphene device outside the quantum regime is stronger. Significant charge shifting can be observed for the devices since none of the peaks remain in the same position as the drain voltage increases and is a known issue for SET devices.

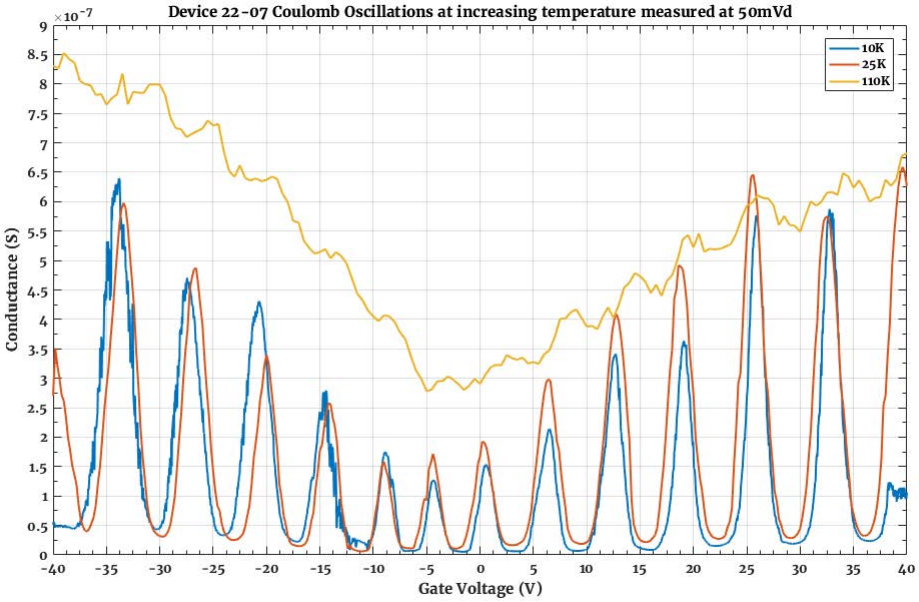

Figure 5.30: 22-100 for increasing temperature measurements at 50 mVd. The device shows consistent Coulomb oscillations at both 10 and 25 K. At 110 K the increase in thermal energy means the device no longer operates within the Fermi energy gap regime, exhibiting the typical parabolic trend for a ambipolar graphene device. The Coulomb oscillations are still visible by comparing to the lower temperature oscillations and some peaks that closely match the frequency at 25 K can be seen.

The increasing temperature plots shows a strong suppression of the Coulomb oscillations within the transport gap at 110K, where the thermal energy now exceeds the Fermi energy gap regime so no suppression of current is possible. The device now yields to the typical characteristics for ambipolar conduction, but by comparing the frequency of peaks at 25 K and the measurement at 110 K the Coulomb oscillations can be verified to still exist at this temperature. It is unfortunate the smallest drain voltage was measured at 50 mVd at 110 K so the energy of the system was too high, since it may have still be possible to observe the transport gap or clearer Coulomb oscillations. This measurement does shows the limit for even a small graphene device and the progress that still needs to be made for a device to function at room temperature.

By comparing the conduction at low drain voltages in figure 5.31 the difference between a single and multi-dot SET can be observed, where 17-100 shows some single peaks, however, mostly double or more sub-band peaks observed within each tunneling event, whereas 22-100 shows only single peaks and no fluctuations in the blockade regime consistent with expected transport properties of a single quantum dot. The difference in conductance between the blockade region and peak height is ~100x difference in conductance values for both 22-100 and 17-100. Demonstrating the strong tunneling properties are related to the short 100 nm length and not the number of quantum dots an electron needs to tunnel through. The observation of the Fermi energy gap from the transport gap in the Id/Vg sweep shows a gap can not be determined for 22-100, where 17-100 shows a sharp increase in the conductance outside its gap, no observable trend can be seen for 22-100. This indicates the device is much smaller than 17-100.

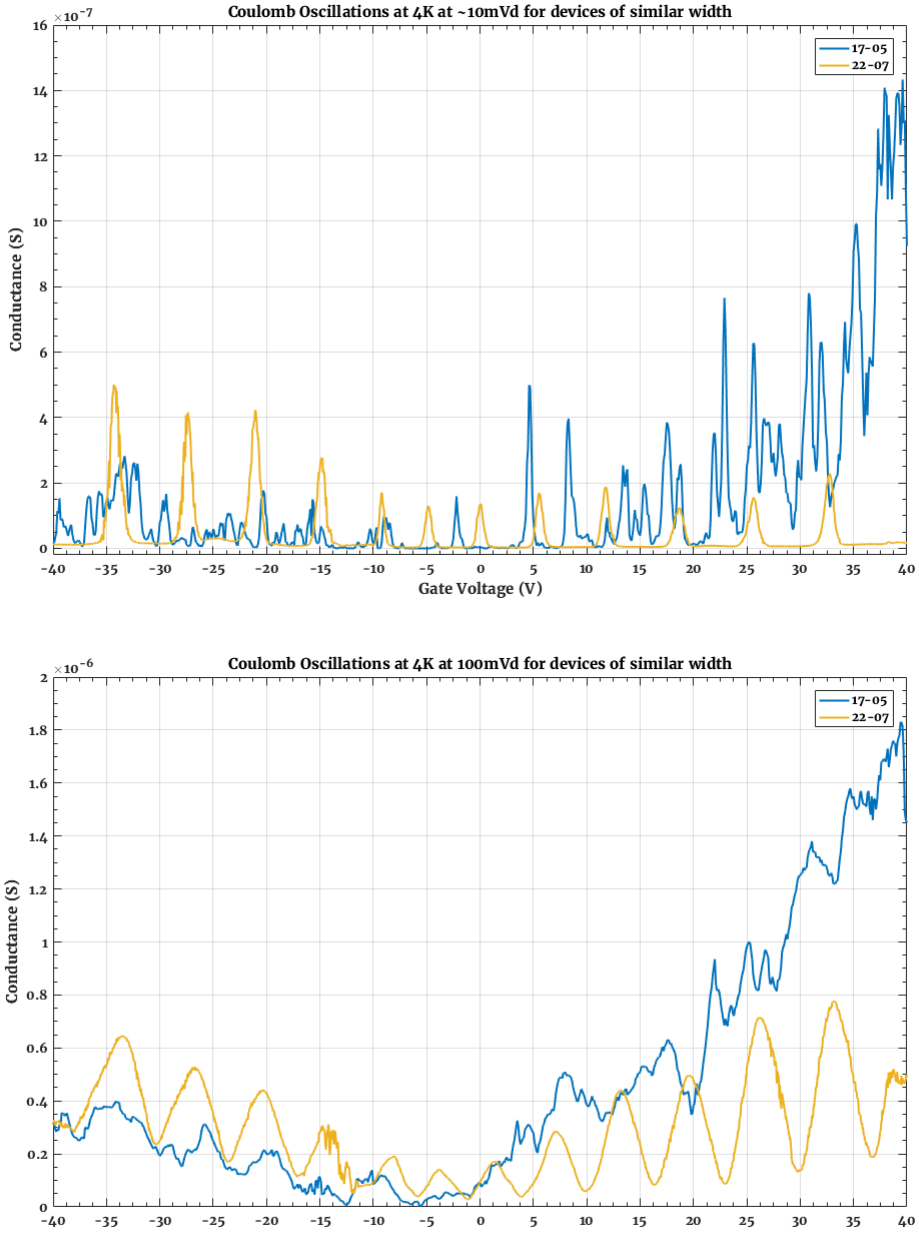

Figure 5.31: Comparison between devices 22-100 and 17-100 at low drain voltage (top) and high drain voltage (bottom). The two devices exhibit strong peak heights in relation to the blockade region of the Coulomb oscillation. With 22-100 showing the characteristics of a single quantum dot compared to the multi-dot characteristics of 17-100. The comparison between the two devices shows the lack of an observed transport gap in 22-100, where 17-100 shows a sharp increase conductance outside its transport gap. 22-100 does not show such a characteristics, indicating 22-100 is much smaller than 17-100 such that the transport gap can not be observed. At high drain voltages the suppression of the Fermi energy gap at 100 mVd proves the device operates in the same manner.

Unfortunately 22-100 did not survive the experimentation after a couple measurements at 25 K were made. Upon investigating the HSQ patterned revealed a catastrophic failure in which not only the graphene layer had broken but the HSQ layer on top was also burned away at the same time. It is therefore only possible to surmise the cause of 22-100's unique device properties from the evidence of its neighbouring nanoribbon

devices.

When comparing the differences between 17-100 and 22-100 it is difficult to determine why the differences have occurred. Both devices were of a similar designed width and the entire fabrication processes was exactly the same for both. This does not leave many options for the cause of its unique properties. There are a number of scenarios possible for the different behaviour of 22-100 to the rest of the devices, that could have influenced the formation of a single quantum dot in the nanoribbon. The scenarios that could lead to the unique properties of the device relate to the CVD-graphene used. The first is the effect of a grain boundary bisecting the device, which there is limited evidence for effect of grain boundaries on the device properties especially on nanoribbons. To quantify the effect a new set of devices would need to be created that can be measured and imaged using scanning transmission electron microscopy. The other scenarios can be caused by the CVD process for growing graphene on the copper foil can produce up to 5% bilayer graphene. Or from a wrinkle/fold in the sheet caused by the transferring of the graphene onto the substrate, where the wrinkle or fold in the sheet would create a bi or trilayer to form that could be twisted so the atomic layers do not match correctly and decouple the layers from each other.

The most probable scenario is due to the chaotic nature of the reactive ion etching process coupled with defects in the HSQ layer. As seen in figure 5.32 a significant point constriction can be observed in the HSQ layer for a different device. Although there is no known selectivity of etch rate depending on the lattice orientation for graphene, the etch process is known to create uneven edges. When this is combined with the fact that not all the HSQ layers on the graphene were perfectly uniform and had subtle edge deformations. This leads to the most probably cause for a single dot formation is due to observable fabrication defects that consistently repeat itself across the devices structures.

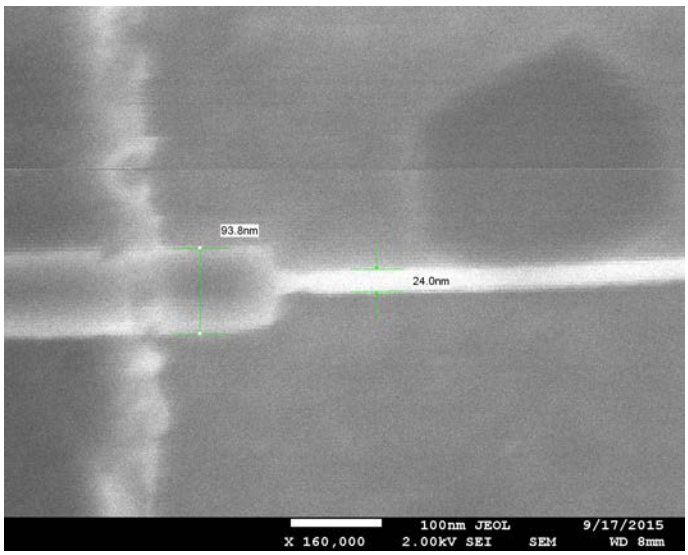

Figure 5.32: HSQ layer for devices with defects in the resist layer. On the left hand side of the HSQ layer where the 24 nm measurement is made, but before the 93.8 nm lead transition a indentation in the HSQ layer can be observed. Resulting in a point constriction in the layer to cause a significantly smaller quantum dot.

5.5 Discussions

5.5.1 Transport gap of CVD nanoribbons

So far the unique transport properties observed in the individual devices have been discussed. But the discussions of the extracted transport gap were purposefully ignored until now to analyse the difference between experimental devices and literature in one section. The first key investigation of the nanoribbon properties is to determine the variation in transport gap with increasing nanoribbon width and length. This characteristic should give insight into the differences between exfoliated graphene and CVD-graphene when considering the impact of the disorder potential fluctuation. Next is the extraction of the mobility and on/off ratio for the devices as a pure nanoribbon FET. So far the devices have shown a greater extent of quantum dot driven transport from electrons hopping between different states across multiple quantum dots for all the devices except 22-100, where this device is omitted from the discussion of transport gap properties due to the lack of an observable gap at any Vd, suggesting the device is much smaller than 17-100.

To make a meaningful extraction of the transport gap the Coulomb oscillations are filtered using a local weighted linear regression in Matlab. In particular a robust loess which uses a quadratic polynomial to fit the data across a span of 0.1 (10% of the data points) and the robust aspect is needed to ignore the extreme changes in data point value. By using a robust loess to filter the data, the random fluctuations in peak height is suppressed to give two linear regions of increasing conduction and a suppressed region of conduction. A higher span can be used or a lowess fit (linear polynomail fit) to create a more linear fit but a robust loess was used out of personal preference for the resulting shape of the filtered data that still retains some of the variation in conduction to enable the observation of when the spectra transitions to a gate voltage outside the transport gap.

The results of the loess filtering is shown in figure 5.33 and 5.34 for the devices of the same designed width (17 nm) and increasing width, respectively. As can be for the 17 nm wide devices the filtering works to show that the extracted transport gap for the 100 nm and 200 nm long devices are very similar, with a sharp increase in conductance on one side of the data outside the transport gap. However for these two devices on the other side the conductance is still strongly suppressed. The extracted transport gap of 55 V is given as a minimum value but could be at least 10 V due to the unfiltered data still showing some minimum data points that meet the purple minimum conductance line.

To extract the mobility and on/off ratios the robust loess is used again for the devices at 100 mVd when the Fermi energy gap is suppressed and the conductance spectra is more linear. Here a 0.6 span is used to yield a linear conduction path, as seen in figure 5.35 where the Coulomb oscillations are completely filtered out to yield a parabolic curve. The mobility is then extracted using the theory in reference [9] to give equation 5.1

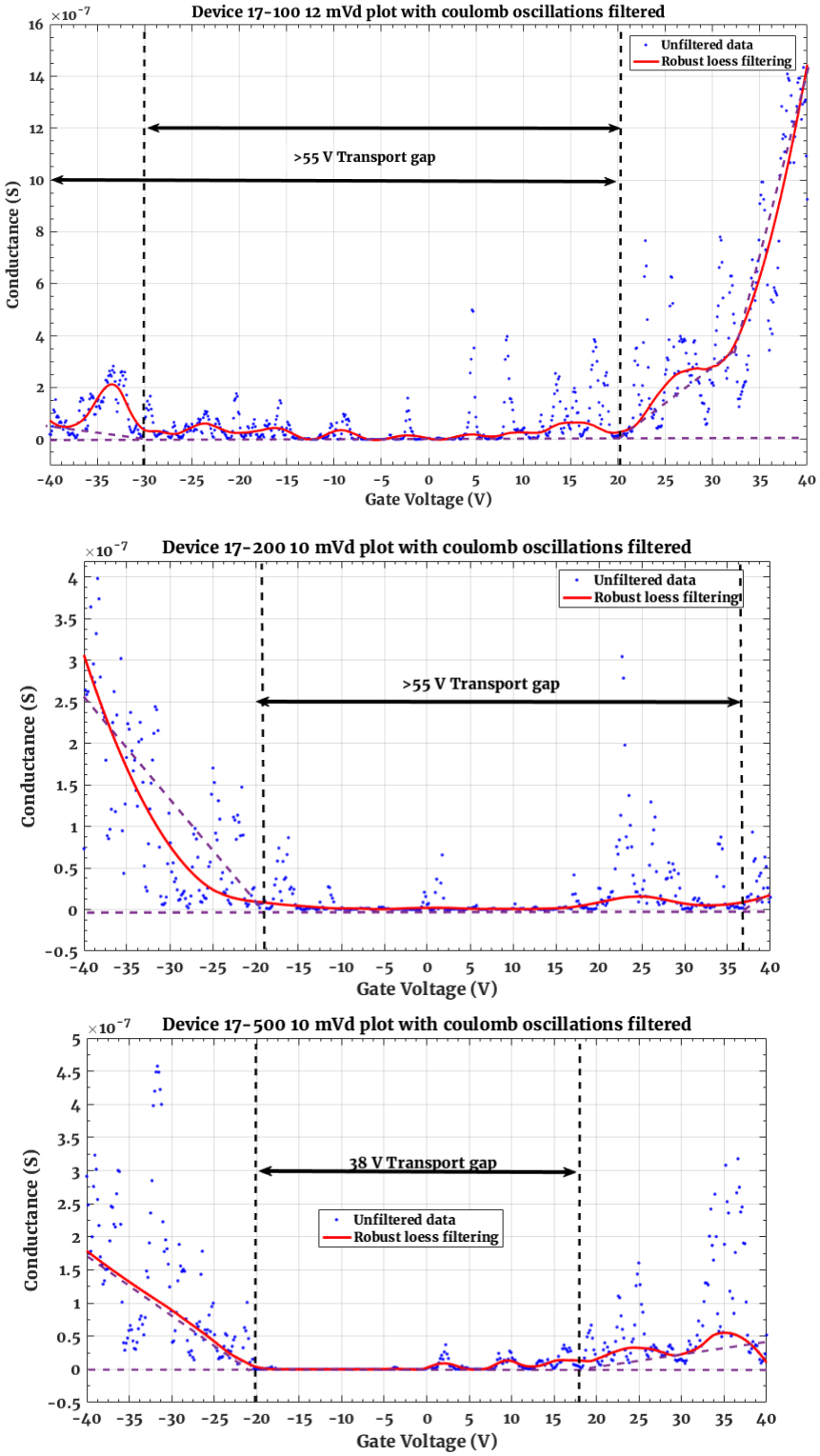

Figure 5.33: Extracted transport gaps from devices of 17 nm width using a robust loess (0.1 span) in Matlab to smooth the data. The red line shows the smooth data and the blue dots is the original data. The graphs are then annotated to show how the transport gap is extracted. For both the 100 and 200 nm length the transport gap is similar as would be expected. However the 500 nm long device shows a 17 V smaller transport gap. In the case of 100 and 200 nm long devices the estimate of a 55 V transport gap is the minimum visible in the extracted data. It is possible the data extends beyond the measured gate voltage sweep and could be more than 65 V for the transport gap. While 17-500 could also show a transport gap closer to 50 V.

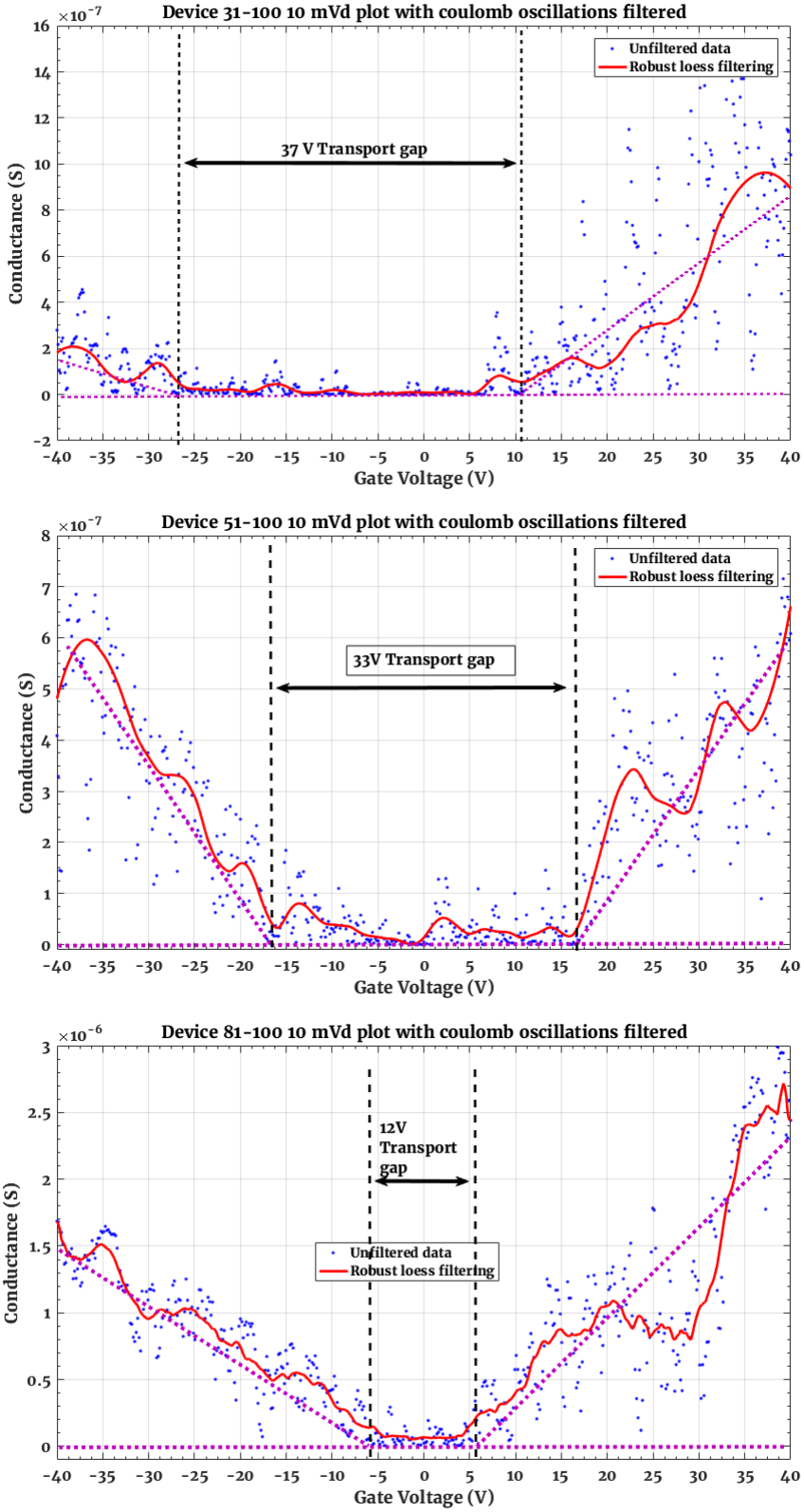

Figure 5.34: Extracted transport gaps from devices of increasing width using a robust loess (0.1 span) in Matlab to smooth the data. The red line shows the smooth data and the blue dots is the original data. The graphs are then annotated to show how the transport gap is extracted. The device of an increasing width show the expected change in transport gap for a graphene nanoribbon.

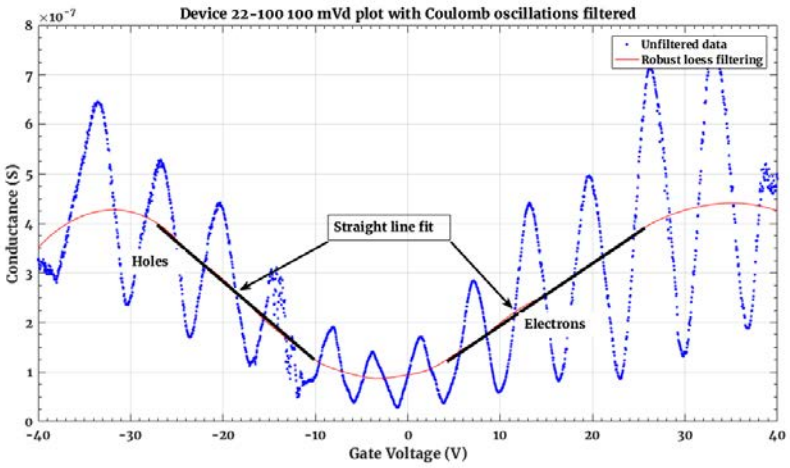

Figure 5.35: Device 22-100 with Coulomb oscillations filtered to yield a parabolic curve, the black lines annotated on the diagram indicate where the gradient is extracted for the mobility.

which calculates the mobilty as the gradient of the conductance vs gate voltage from the linear region of the spectra and is then multiple by the length square divided by the gate capacitance, where the gate capacitance used is the same discussed in the literature review where the stray capacitance is used. The on/off ratio is then taken as the highest conductance value divided by the lowest measured conductance value. The extracted values for all the measured nanoribbons and then put into the table 5.1 for comparison.

$$\mu = \frac{dG}{dV_{gs}} x \frac{L^2}{C_g} \tag{5.1}$$

Table 5.1 reveals the decreasing Fermi energy gaps for these devices as the width decreases. Which is calculated from the theory stated in section 5.3 of this chapter from the extracted transport gap values. The predicted values of the Fermi energy for a CVD-graphene nanoribbon using the confinement energy and disorder potential calculation from the literature review are presented alongside to show the significant difference in magnitude . The data is then plotted in figure 5.36 against the different Fermi energy gaps possible for the minimum confinement energy and different disorder values for increasing nanoribbon width. The experimental values are plotted as the midpoint between the maximum possible nanoribbon width and the minimum from the estimated undercut of 8 nm, where the undercut is determined from the stability diagram of 17-100 in the next section. While the Fermi energy gaps are the minimum energy possible for the devices. The plot reveals that the experimental devices does not match the theory with the Fermi much larger than expected for 17-100 and a lot smaller for device 81-100.

Device	Transport gap (V)	Predicted gap (V)	Extracted ΔE_F(eV)	Predicted $\Delta E_{F,CVD}$ (eV)	Mobility($cm^2V^{-1}s^{-1}$)	On/Off ratio
17-100	55	48	0.7332	0.64	10	1500
31-100	37	45	0.6023	0.62	2.32	2927
51-100	33	42	0.5069	0.6	1.05	1740
81-100	12	41	0.3444	0.59	2.47	717
17-200	55	48	0.7332	0.64	1.22	957
17-500	38	48	0.6096	0.64	0.90	722
22-100	Unknown	48	Unknown	0.64	2.06	27

Table 5.1: Table of extracted properties for the nanoribbons of different widths and lengths. The extracted transport gaps and resulting Fermi gaps and shown against the predicted values for these devices. For the smaller devices the predicted values of the CVD-graphene fits closer to the extracted values proving the CVD-graphene does have an increased disordered potential resulting in a larger Fermi energy gap. As the device width increases the extracted energy drops quicker than expected to suggest the model for disorder potential is more complicated than originally predicted, whereas the increasing length produces the same Fermi energy gap for 100 and 200 nm long devices but at least 0.1 eV less for 500 nm length. The devices show a large variation in mobility with 17-100 the best mobility of all the devices and 31-100 the best on/off ratio at 50 mVd.

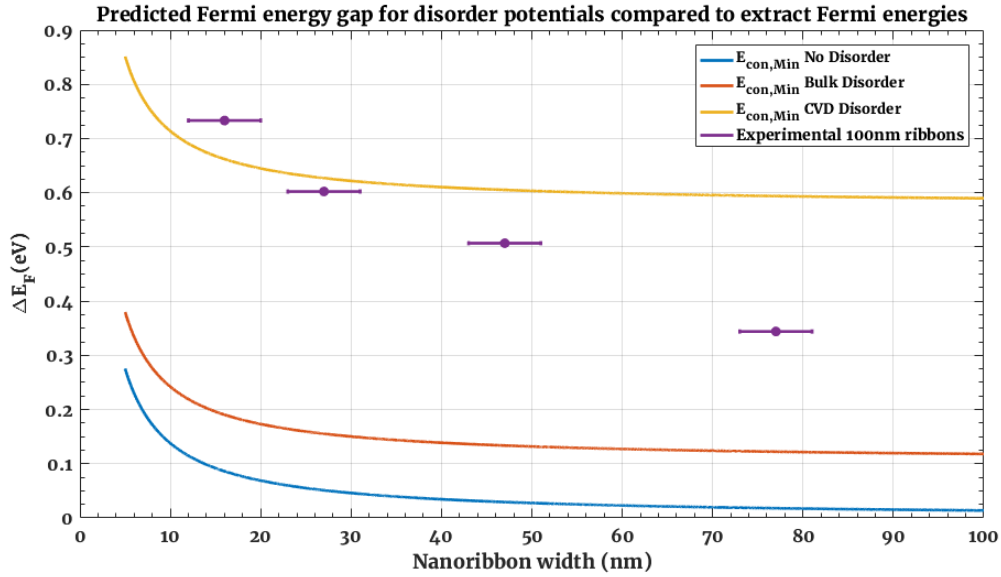

Figure 5.36: Plot of extracted Fermi energy gaps against nanoribbon widths with theoretical prediction of different disorder energies. With a calculated undercut of 8 nm for the devices, the circle is average width between the designed width and estimated width. With the error bar representing the min and max limits of the nanoribbon width for the measured devices.

The plot reveals the current model for extracting the Fermi energy gap from the transport gap and then matching the extracted energy to the calculated Fermi energy gap from the calculation of confinement energy and disorder potential is not sophisticated enough to handle CVD-graphene nanoribbons. The results of these devices would suggest that either the disorder potential is not a constant value for nanoribbons of increasing width. Or the calculation of the confinement energy for CVD-graphene nanoribbons is not a α/W dependence. Although so far the confinement energy has not been violated so it can not be larger than equation 2.5. This would indicate that the simple method of using a single value for the disorder potential is incorrect. Highlighting the need for further pursuit into identifying and quantifying the additional factors that contribute to the disorder potential. Although the devices of 200 nm and 500 nm are not plotted they still indicate a separate trend for the increasing length dependence on the Fermi energy gap, gives further evidence that for CVD-graphene some new physics within the nanoribbon is occurring that can't be determined. Since previous literature results have shown that the Fermi energy gap does not have a length dependence behaviour [2, 58]. Although without further data any further analysis on the increasing device length can not be conclusive.

Lastly the mobility values for the extracted devices show that mobility is lower than those found in nanoribbons made from exfoliated graphene. The data extracted from the nanoribbons is then compared to data from the review in reference [27] which produced the table seen in figure 5.37. Although the mobility values are ~10x lower than those of other devices the "bandgap" (actually the Fermi energy gap) is 4th best device recorded with a value of 730 meV that is closer to fabrications using high quality graphene samples while retaining a higher on/off ratio than those devices. But still lower than the

ratios obtained for exfoliated graphene devices.

This work demonstrates the width dependent behaviour of the CVD-graphene nanoribbons against the Fermi energy gap, where the use of CVD-graphene has increased the disorder potential within the ribbon causing an increase in the measured transport gaps for the devices. High values of 730 meV have been found for smallest devices, mobility of 10 $cm^2V^{-1}s^{-1}$, and on/off ratio of ~3000. Which, compared to devices from literature reveal a nanoribbon FET that has a high Fermi energy gap without sacrificing the mobility and on/off ratio of the device. This work has been revealed the need to further explore the fundamental properties of CVD-graphene nanoribbons in relation to the Fermi energy gap.

5.5.2 SET properties of CVD nanoribbons

The initial focus of the measurements was to investigate the properties of CVD-graphene nanoribbons, but an integral aspect of graphene nanoribbons is the electron transport dominated by single electron tunneling. In this section the specific single electron transistor characteristics are analysed for the two smallest devices. 17-100 which shows transport close to the typical nanoribbons and 22-100 which shows the clearest Coulomb oscillations observed in working SET for a graphene nanoribbon so far.

Typical graphene nanoribbon

In a typical graphene nanoribbon the SET properties demonstrate multiple dot properties, usually indicated by overlapping Coulomb diamonds in the stability diagram or in the case of the Id/Vg graphs the Coulomb oscillations show an inconsistent change in the peak shape for increase drain voltages. Which is associated with the electron tunneling through different energy levels across multiple dots. In figure 5.38 the Id/Vg characteristics of 17-100 at low drain voltages from 4 mVd to 20 mVd are plotted to determine how the peaks from the Coulomb oscillation change. Here the peaks show no consistent change a low drain voltages except around the 5 V region, which is plotted in figure 5.39, where the figure shows the same charge shifting observed in 22-100 around the 4.5 V gate voltage and a double peak at 8.5 V, which the shape changes at each drain voltage measurement. The key aspect of these two tunneling events is indicative of the small number of quantum dots and energy levels available for transport. The peak at 4.5 V shows that the electron only had one energy level available in each dot to transport through the nanoribbon, while at 8.5 V the double peak shape is due to two coherent states available across the dot, where the change in height between each of the sub-peaks is due to the matching between the drain voltage and energy level of the first quantum dot since the electrostatic potential from the gate voltage remains the same. This is discussed in Kouwenhoven's chapter in reference [70] for the non-linear transport in semiconductor quantum dots.

Technique	Advantages	Disadvantages	Min. width (nm)	Carrier mobility ($cm^2 V^{-1} s^{-1}$)	Bandgap (meV)	I_{on}/I_{off}
Mechanical exfoliation and lithography	- Formation of single-layer GNRs	- No precise control of GNR edges - Difficult in large-scale	~15		~200	
Exfoliation and chemical treatment	- Nearly pristine GNRs - Smooth edges	- Non-uniform shapes	<10	~100–200	>300	Up to 10^7
Exfoliation and catalytic etching	- Well-defined edges	- Etching is only possible along crystallographic directions	~15			
Metal-assisted etching	- Aligned GNRs - Large-scale production	- Large and non-uniform width	19		~100	~7–10 up to 5000
CVD and electron beam lithography	- Wafer-scale graphene - Controllable dimensions	- Unavailable information on edge definition	12	~100		~10
CVD, electron beam lithography and neutral beam etching	- Aligned GNRs - Ultra-low defects	- Unavailable results for narrower GNRs	70 (Tested) down to 30	>200		$\sim 10^3$ $\sim 10^4$
CVD and STM nanolithography	- Narrow GNRs with defined crystallographic orientations	- Edge roughness - Difficult in large-scale	3		~300	
Direct growth on silicon dioxide	- No substrate transfer - Large-scale production	- Formation of plateaus - Large and non-uniform width	20	>1000	~50	~2
CVD on germanium	- High aspect ratio - Clean GNR/substrate interface	- Nonuniform edge definition - Low control on GNR placement	8.2			~20
SnO_2 nanoribbon mask and O_2 etching	- Reduces process steps for fabrication of GNRFETs	- Requires selection and transferring of SnO_2 nanoribbons	230		~800	3.7
Cyclodehydrogenation of precursor monomers	- Well-defined edges - Atomically precise width	- Limited to substrates compatible with precursors	0.74		1600	
Polymerization of molecular precursors	- Narrow GNRs with well-defined edges - Bandgap similar to silicon	- Unpredicted length - Width variations	~1		~1300	
Growth on SiC trenches	- Well-defined and precise dimensions - Reproducible features	- Limited to SiC substrate	~1.4		>500	

Figure 5.37: Table of extracted nanoribbon properties taken from reference [27]

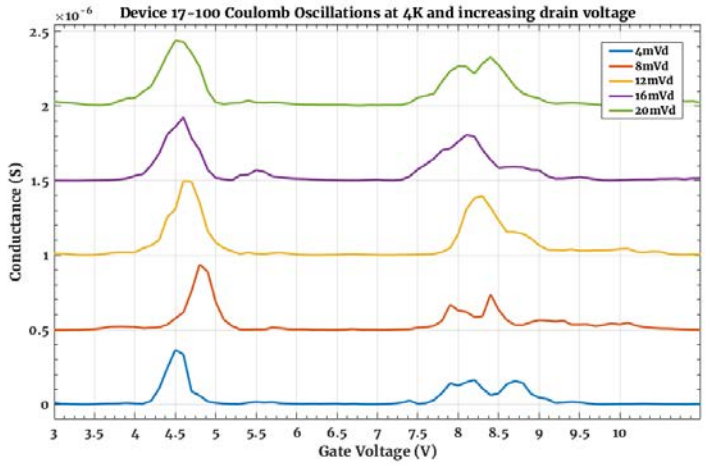

Figure 5.39: Top: Zoomed in shot of data to show the evolution of the peak shape with increasing drain voltage, measured with a 0.1 V Vg sweep resolution. The change in peak shape reveals the multi-state hopping through multiple quantum dots.

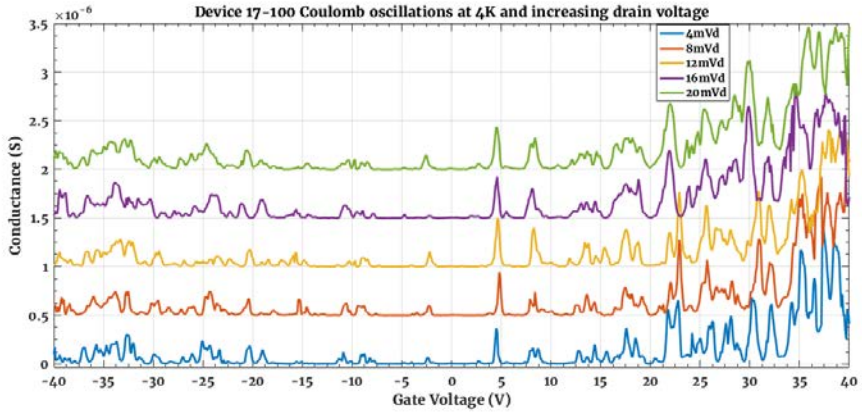

Figure 5.38: Electrical characteristics of 17 nm wide & 100nm long device at low drain voltages from 4 mVd to 20 mVd

The evolution of the peak shape with increasing drain voltage, on the left hand side of the image between 4 and 5 V the peak be seen to both shift and broaden with increasing Vd indicating at this energy the SET barrier has been modulated to permit a single electron, whereas on the right hand side between 7.5 and 9.5 V the double peak shape varies significantly at each increasing drain voltage. Here the exact quantum state to cause this is unknown due to the effects from multiple types of hopping between different energy levels in multiple dots as illustrated in the bottom of the figure.

When the stability diagram is plotted in figure 5.40 for device 17-100 the regions of no conduction can be seen clearly. With the diamonds decreasing in height as the gate voltage increases in either direction from the Dirac point, where the Dirac point for 17-100 is at ~-5 V and is also the highest diamond. From these characteristics it is most likely that 17-100 is an SET with only a couple quantum dots, where the extracted stability diagram shows the properties of the SET are comparable to the behaviour of unzipped carbon nanotube SETs seen in reference [9]. Although no smoothing has been applied to the graph, the diamonds can be observed clearly in the negative drain voltages

and show some merging at positive drain voltages around the central diamond near the Dirac point. The voltage bias gap of the largest diamond indicates the device is likely to be ~12nm wide when using Castro's model (from the literature review) to extract the device width. This gives a value of 8 nm for the undercut based on the measurement of a 20 nm minimum device width seen in fabrication section of this chapter. This value of 8 nm undercut is how the error bars seen in the plotted Fermi energy gap graph seen earlier.

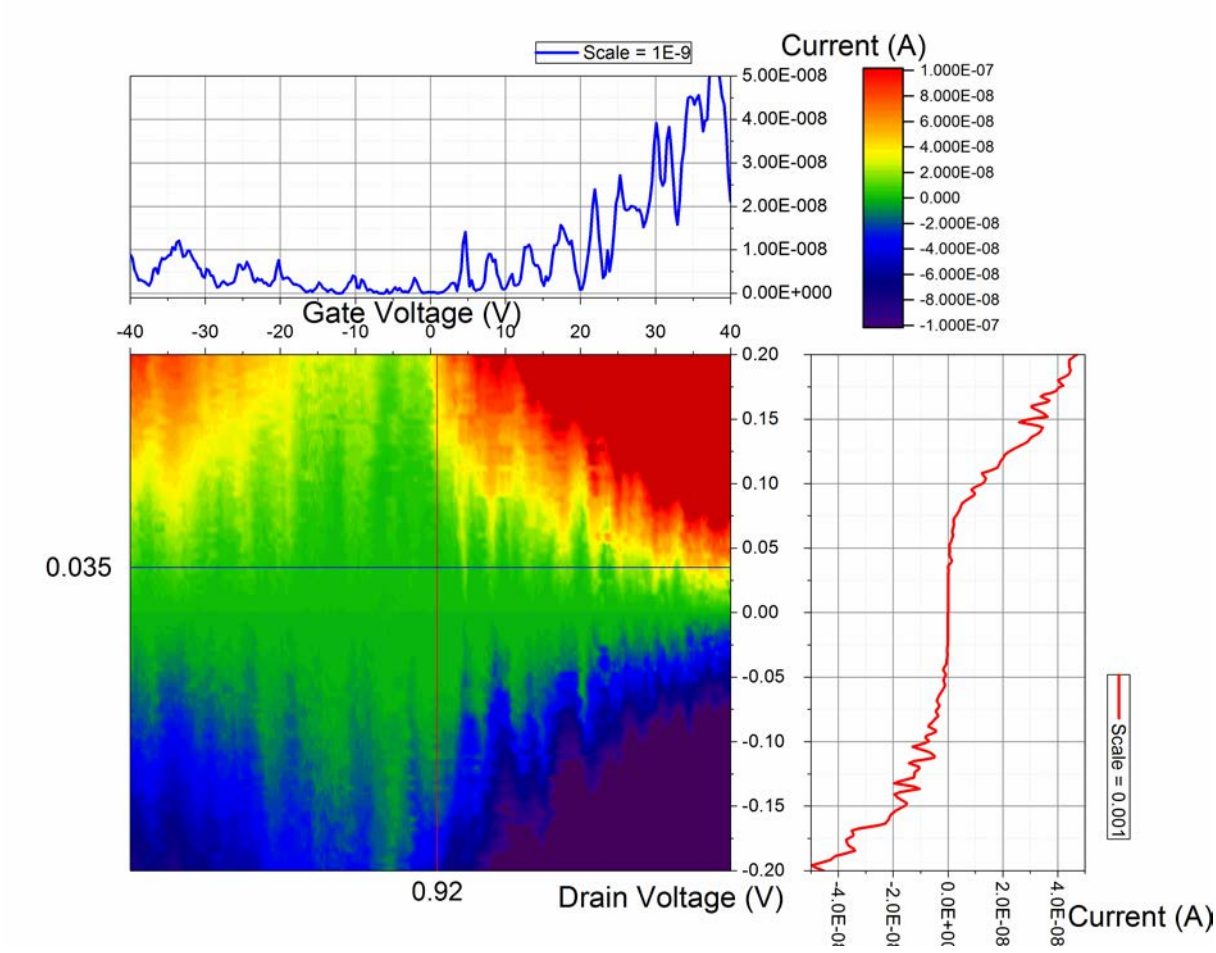

Figure 5.40: Stability diagram of device 17-100 produced using origin, there is 80,000 data points used for the stability diagram with 800 points for each Id/Vg sweep in 0.1V steps and 100 Vd sweeps in 4 mV steps. No smoothing is applied to the image which makes distinguishing some of the diamonds in the diagram unclear, but if the Coulomb diagram shape is analyzed in the negative drain voltage values the typical diamond shape can be observed. The extracted profile of the Vg in the top shows how the different Coulomb oscillations affect the diamond shape for clarity whereas the profile on the right shows the Coulomb blockade across one of the diamonds in the stability diagram.

As seen in the results of the Id/Vg graphs most of the devices show the typical behaviour for a graphene nanoribbon. With the increasing width the distance between the peaks decreases due to the size of the localised states also increasing in size. This in turn increases the capacitance of the states. The width of the devices increases until the Coulomb oscillations are barely visible within the transport gap. Despite the transport gap remaining relatively large. The change in the Id/Vg with increasing width demonstrates the concept of interdot coupling. As the device width increases the peaks become

much harder to be distinguished compared to the individual peaks observed in the 17 nm device.

The increasing device length shows that shorter tunneling lengths are preferable for improving the SET properties. As would be expected since there is less localized states needed to successfully tunnel through the device. This is observed by the much higher peaks for the 100 nm long devices compared to 200 and 500 nm devices, where the peak height decreases to be 10x smaller from 100 to 200 for the largest peaks within the transport gap. This shows an interesting trend between the length of the devices for the SET properties, that merits further exploration in future works.

Single quantum dot device

Unlike typical graphene nanoribbons device 22-100 is a single quantum dot from the clear single peak Coulomb oscillations. The hypothesis from the Id/Vg graphs is the quantum dot was a smaller size than expected compared to 17-100. Caused by a defect in the HSQ layer to create a smaller single constriction in the nanoribbon, so a quantum point contact is created. It's because of this the coupling between the tunnel barriers the Coulomb oscillations become much clearer to observe, since the transport is dominated by the significantly single smaller quantum dot and the larger quantum dots acting to increase the extended wave function with the wide leads to form the barrier. Figure 5.41 shows a possible configuration of the energy bands in the nanoribbon that could cause the single dot characteristics to present itself in a 100 nm nanoribbon.

Additionally, if the characteristics of the single peak measured at 10 K and another at 25 K is focused on a minor oscillation superimposed on the large Coulomb oscillation peak is observed(5.30). This could be an artifact from the lack of resolution of the measurement at 25K. Which is measured with a 0.2 V step compared to 0.03 V step for the measurement at 10K. Alternatively it could be due to a resonance within the tunnel barrier [114], which in the work has a distinct characteristics of increasing the temperature suppresses the resonance for a single dopant SET. If this is also true for these graphene devices it would further emphasize the single dot characteristics are caused by a HSQ defect creating a point contact in the nanoribbon. So the resonances would be caused by the localised states formed within the tunnel barrier, which are then coupled to the barrier. Distinguishing 22-100 further by the use of a 2 stage tunnel barrier, with a wide-narrow-narrower segmentation. Rather than a tunnel barrier caused by the transition from a wide-narrow segmentation and the properties dominated by electron tunneling through multiple quantum dots of a comparable size rather than a single much smaller quantum dot.

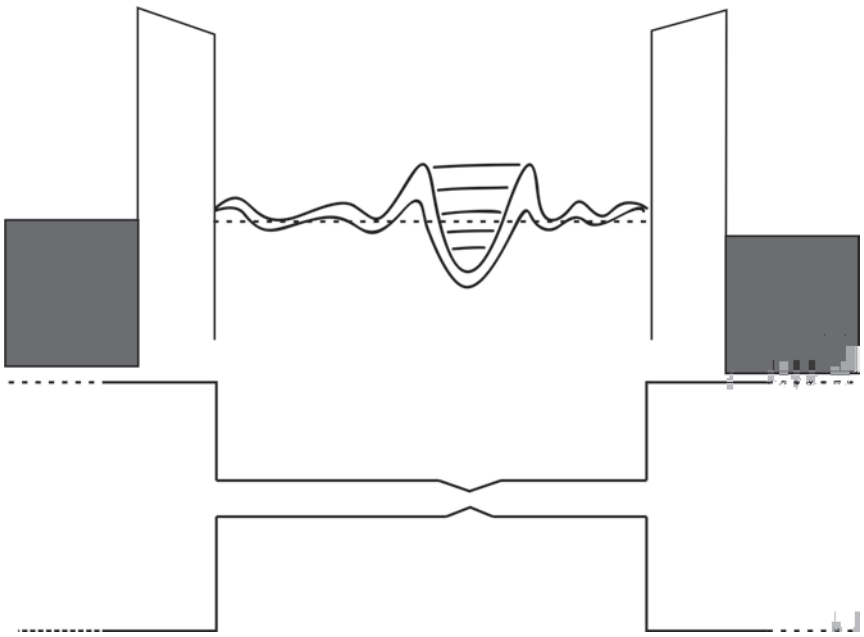

Figure 5.41: Predicted energy band diagram for the configuration that would cause a single quantum dot to form (top) and the associated pattern of the nanoribbon that would cause this pattern (bottom)

In Figure 5.42 the Coulomb oscillations previously plotted in Figure 5.29 have now been normalized around the Dirac point so the centre of the Coulomb oscillation at the Dirac point has been shifted to a value of 0 V. Doing this compensates for the charge shifting caused by the effect of background charging on the device and provides a clearer picture on the effect of the gate voltage on the $\Delta V_g$and means a stability diagram can be plotted from the measured device data as seen in Figure 5.43. The peaks can be seen to correlate with each other around the Dirac point but as the gate voltage increases in either direction the peak position becomes less consistent. This indicates an effect of the gate voltage on the Coulomb oscillations.

On an initial assessment of the clear Coulomb oscillations in the Id/Vg of Figure 5.42 an extraction of the peak to peak distance (ΔV_g) between the peaks is the first obvious step to make to determine the gate capacitance and diameter of the quantum dot, where at the Dirac point of around -7.5 V or when N=0 the ΔV_g is 4.2 V, which gives a C_g of 0.038 aF. Extracting from the Coulomb diamonds in the stability diagram gives a ΔV_d of ~90 mV to give an E_c of 90 meV. Estimating the quantum dot diameter with Castro's model from the charging (or bias) energy gives a predicted diameter of 9 nm. If the quantum dot is then assumed to be a single circular constricted area within the nanoribbon rather than acting across the entire length of the nanoribbon then a 9 nm dot would produce a 4.2 V ΔV_g, which means the device acts as expected for the first tunneling event. This matches the prediction that the 22-100 device contains a single point constriction within the length of the nanoribbon to limit only a single quantum dot to affect the electrical properties of the device. This can be noted from the lack of a visible transport gap in the device and lower extracted mobility compared to 17-100, where the transport gap in 17-100 is only capable of being measured for a device predicted to be ~12 nm wide, so if

22-100 is 3 nm smaller then it is reasonable for the device to have no apparent transport gap.

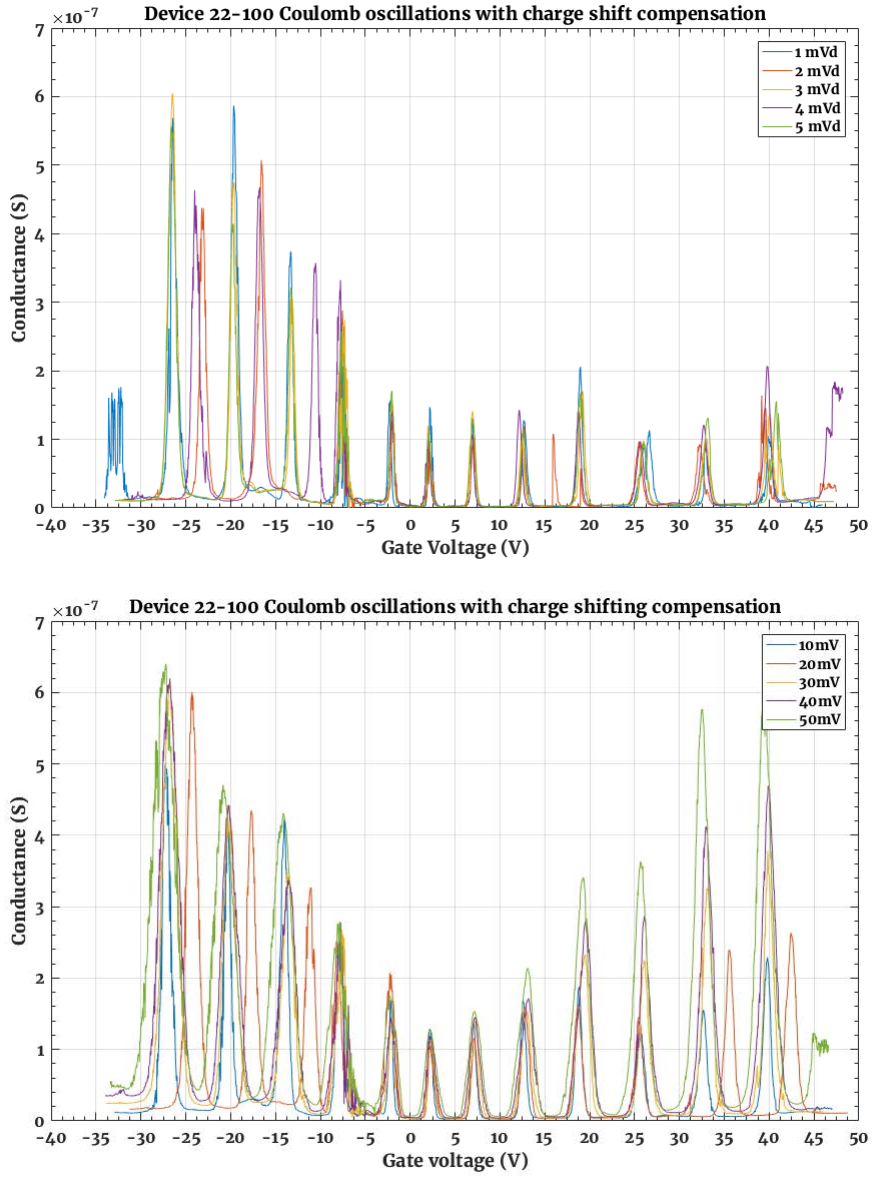

Figure 5.42: Electrical data from device 22-100 at different drain voltages with the charge shifting now compensated for by moving all devices to have the midpoint of the Coulomb oscillation at ~-5 V to be shifted so it is now at 0 V. Because the midpoint between the two peaks is different for each V_da different is used to compensate for this shift. As can been seen at around 0 V now the peaks are aligned, however as the gate voltage increases the position and width of the peaks becomes more erratic indicating an additional gate voltage effect on the Coulomb oscillations.

The Coulomb diamonds visible in the stability diagram and show an interesting relation between both the change in gate and drain voltage, where for an increase in N the diamond shape changes, so as the number of holes of electrons increases both the height and width of the diamonds are altered. If the change in ΔV_g alone is considered against

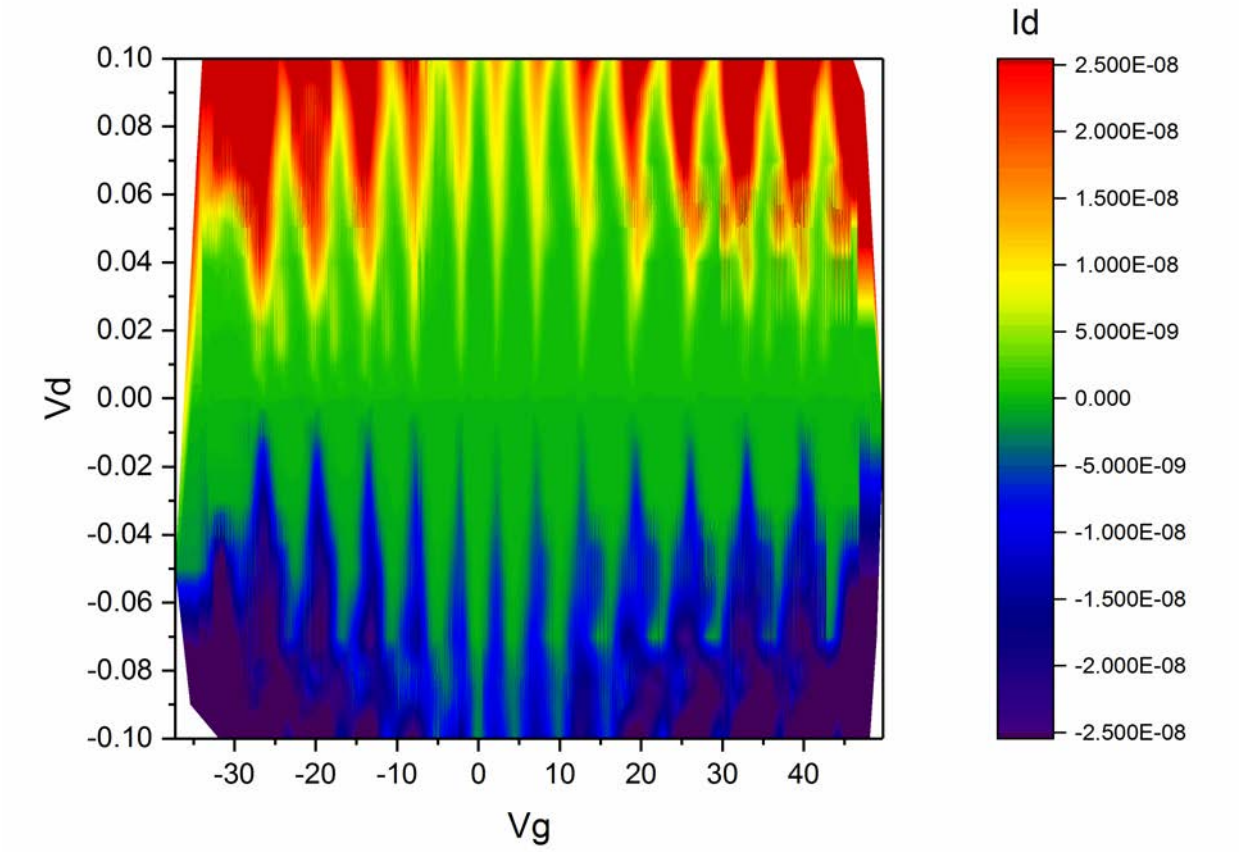

Figure 5.43: Stability diagram of 22-100 with charge shifting compensation

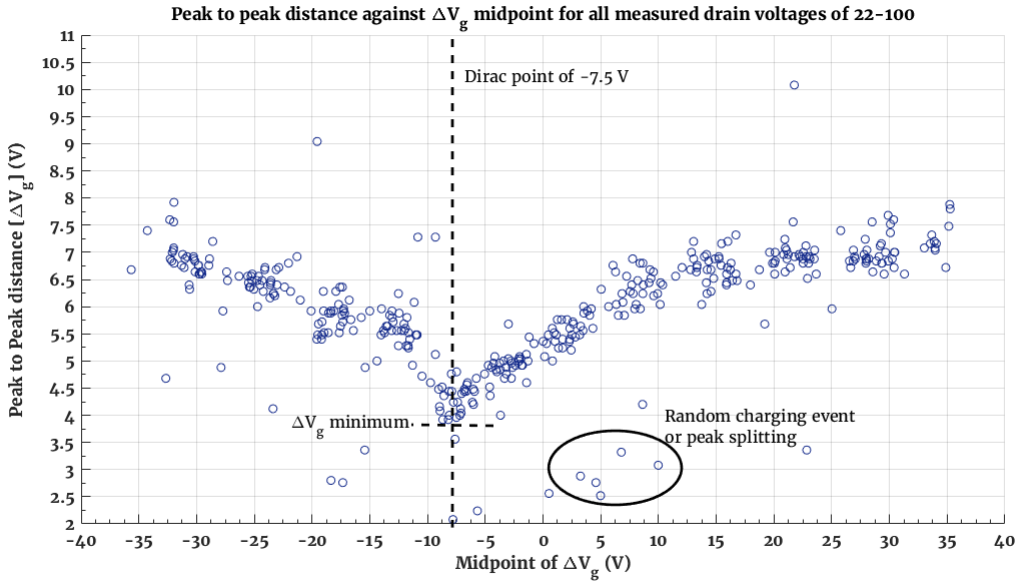

Figure 5.44: Plot of the extracted ΔV_g against its midpoint value to show the relation between gate voltage and successive tunneling events when the data is not shifted to compensate for charge shifting to show how the raw data is distributed. This overall trend shows a clear variation in ΔV_g with increasing gate voltages

the increase in gate voltage (or increasing number of tunneling events) some additional behaviour can be observed unique to this device. The extracted ΔV_g against the midpoint value plotted in figure 5.44 shows the relation between the gate voltage and ΔV_g clearer. This behaviour of a change in the ΔV_g with increasing gate voltage correlates with the observed behaviour in some silicon and 2DEG devices [115] [70], where the change in ΔV_g is due to the energy level spacing in a quantum dot. When the diameter is small enough the difference between energy levels is large enough to be of a significant value that it impacts the devices measured properties. If the average variation in ΔV_g is considered instead against each charge tunneling event to normalize the effect of charge shifting the trend can be seen much clearer in Figure 5.45. This demonstrates the observed of a few electrons in a graphene quantum dot to cause an alteration of the measured ΔV_g in the Coulomb oscillations.

5.5.3 Energy level spacing of a Single quantum dot

So far in literature the energy level spacing of graphene quantum dots has been observed by electrons tunneling through excited states or an aperiodicity in the Coulomb oscillations. This is because most ribbons previously measured have either been multiple dot devices or the quantum dot was too large to measure any significant energy level spacing. Resulting in the typical result of energy level spacing causing aperiodicity in the Coulomb oscillations. As seen in the 22-100 though, this is no longer the case for graphene quantum dots. It is possible for the Coulomb oscillations peak to peak distance to be consistently varied by the gate voltage. Then in turn the number of charge carriers on the charging island.

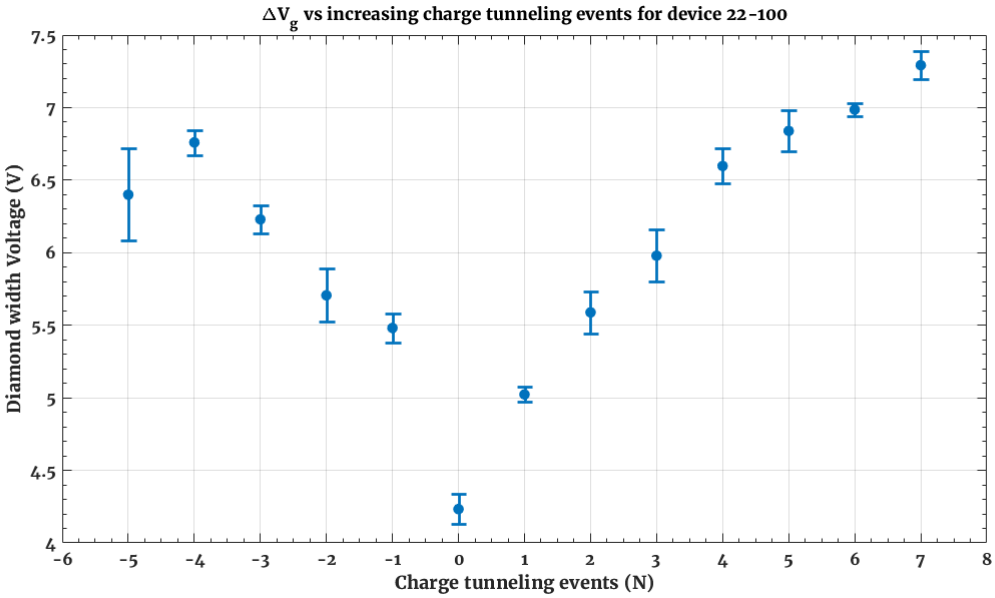

Figure 5.45: Plot of extractedΔV_gat each successive charge tunneling event, where 0 is at the Dirac point and minimum value of ΔV_g. The trend in the right hand side of the image can be seen much clearer, whereas the left hand side for transport of holes is less distinct. This agrees with the previous figures where the charge shifting was compensated for, which showed the negative gate bias caused a more chaotic trend in the positioning of the Coulomb oscillations.

From the theory established by [116] and [70] the full equation (equation 5.41) for determining the peak to peak distance (ΔV_g) in the Id/Vg is a function of gate capacitance, total capacitance, electron charge and energy level spacing. Typically the energy level spacing is too small to cause much variation in the peak to peak distance so on average the measure distance is a function of electron charge and gate capacitance.

In figure 5.46 the extraction of the peak to peak distance for the Coulomb oscillations at increasing drain voltages and plotting against the charge carrier number is shown again , where the 0 is taken from the Dirac point of the devices and assumed to be when 0 electrons or holes have tunneled onto the island. As the number of tunneling events increases the average value of ΔV_g is shown to increase in a consistent manner, where for N=0 ,ΔV_g = 4.2 V and for N=6 & N=-6 ,$\Delta V_g \approx$7 V. With the minus sign for N indicating hole transport. The oscillations are then compared to the theory established by Guttinger [11] for a graphene SET, where the energy spacing is determined by reciprocal of the dot diameter multiplied by the square roof of the number of charge carriers or that $\Delta E_S \approx 1/\sqrt{N}$ (See equation 2.17). As can be seen for low values of N this theory does not correlate with the CVD-graphene device measured.

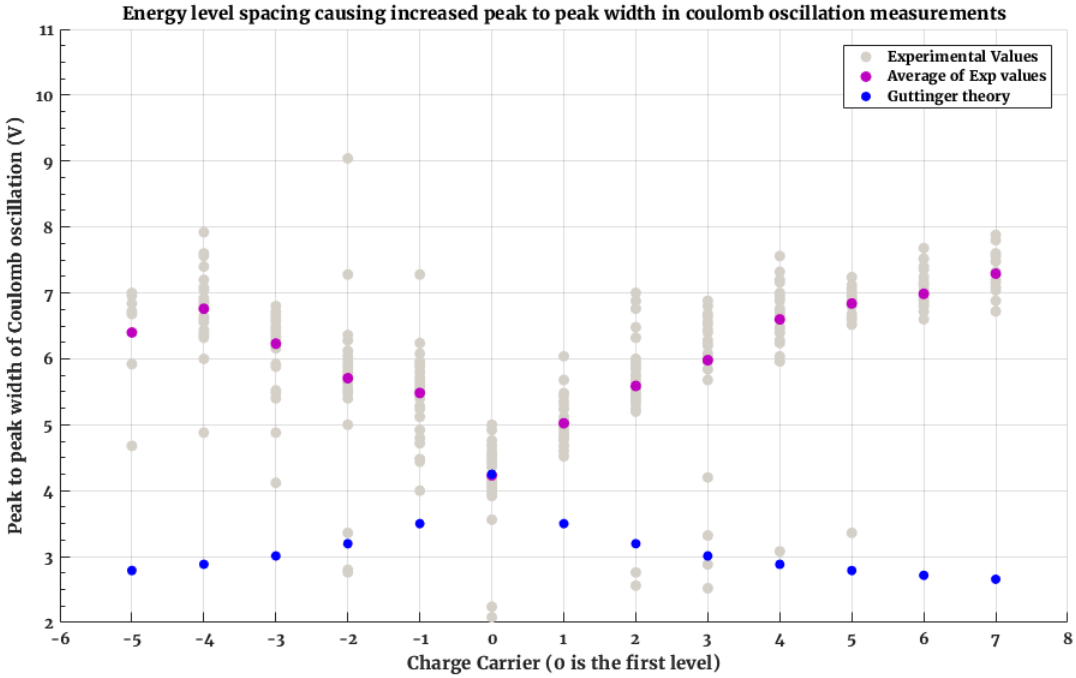

Figure 5.46: Extracted ΔV_g against theoretically predicted values of a 9 nm sized graphene quantum dot using Guttinger's theory in Reference [11].

If this is understood in a different manner to the original theory of a 1D quantum dot a better fit to the extracted $\Delta \mathrm{V_g}$can be found. In Kouwenhoven's work the increase in $\Delta \mathrm{V_g}$ would be expected to increase with N in a linear rate, since the relation for$\Delta E_S \approx N$ (See equation 2.14). If the increase in $\Delta \mathrm{V_g}$ was plotted for a 1D quantum dot of this size it would result in the first diamond as 6 V and the 8th tunneling event as 16 V wide. Which does not correlate with the size of $\Delta \mathrm{V_g}$found in this this device or the non-linear relation between N and $\Delta \mathrm{V_g}$observed. However, this can be further explained by the relation between graphene and the effective electron mass. In graphene the effective electron mass is not a constant value as is assumed for other semiconductors. Instead the effective electron mass is affected by the charge density in equation5.2 [117], where the charge density is also controlled by the gate voltage in equation 5.3[36].

$$\mathrm{m^*} = (\frac{\hbar}{\upsilon_\mathrm{F}})\sqrt{\pi \mathrm{n_{2D}}} \tag{5.2}$$

$$\mathrm{n_{2D}} = (\frac{\epsilon_0 \epsilon_\mathrm{r}}{\mathrm{et_{ox}}})\mathrm{V_{bg}} \tag{5.3}$$

The energy level spacing is known to have an effect in SET devices and has been shown in other semiconductors to have a pronounced effect on the peak to peak distance in the Coulomb oscillations or in the diamond width of the stability diagram, in relation to the number of charge tunneling events at low values of N [70, 115]. In graphene this behaviour has not been seen before. The only glimpses have been seen so far in the excited states in the stability diagrams for much larger nanoribbons or quantum

dots [11], where the limitation for these devices has been the larger size (>50nm) of the devices when this has been observed. However in work by D. Bischoff et al. in 2014, graphene was patterned into 30 by 30 nm point constrictions connected to much wider (500 nm) leads and did not show any clear Coulomb oscillations or diamond width dependent properties [63]. This means there is either something unique in the design of the nanoribbon SET presenting in this work or a unique property of the CVD-graphene that has been exploited to create a single quantum dot.

Since the fitting of the current theory for energy level spacing does not fit the measured change in ΔV_gusing Guttinger's or Kouwenhoven's prediction, an alternative to proving the effect of energy level spacing must be done by analyzing the change in ΔV_g with increasing temperature. This can be done easily for 10 and 25 K for the measurements made at 50 mVd seen in figure 5.30 where the Coulomb oscillation is clearly visible. At 110 K though the Coulomb oscillations are strongly suppressed from the high temperature, however by comparing the oscillating peaks and troughs with the location of those at a lower temperature an estimate for the ΔV_g at 110 K can be made. In figure 5.47 the results of this extraction is shown, the trend at 25 K closely matches the extraction at 10 K indicating the energy levels are quick large. As the temperature increases to 110 K the change in ΔV_g with increasing tunneling events becomes more random in size, but some dependency on increasing tunneling events is still visible.

This can be related to an additional gate voltage effect on the quantum dot in addition to the modification of the effective electron mass with gate voltage. Which is due to an increase in the electric field strength across the entire nanoribbon. By considering how the quantum dot is formed within the nanoribbon this can be further understood, where the quantum dot is formed by a constriction within the nanoribbon and is then isolated with tunnel barriers of a low transparency. However the tunnel barrier is formed by variations in the density of states across the nanoribbon, where the variation in the density of states across the nanoribbon results in extended electron wavefunctions that form the barrier at the transition between the wide leads and the narrow ribbon [63]. Any change in the electric field will then modify the barriers and quantum dot in turn.

Since the increase in disorder from CVD-graphene and the sub 20 nm quantum dot diameter requires a large gate voltage modulation to observe the full extent of the Coulomb oscillations. A much larger electric field now impacts the measured properties of the SET and adds an additional gate modulation effect to the measured ΔV_g. Which means isolating the effect of energy level spacing against a gate voltage modulation of the electron density in the nanoribbon can not be excluded from each other. When considering the additional effect of gate voltage on the effective electron mass on the energy level spacing means the resulting ΔV_gdependence with increasing gate voltage is further complicated when trying to predict the exact shape of the Coulomb oscillations for this device.

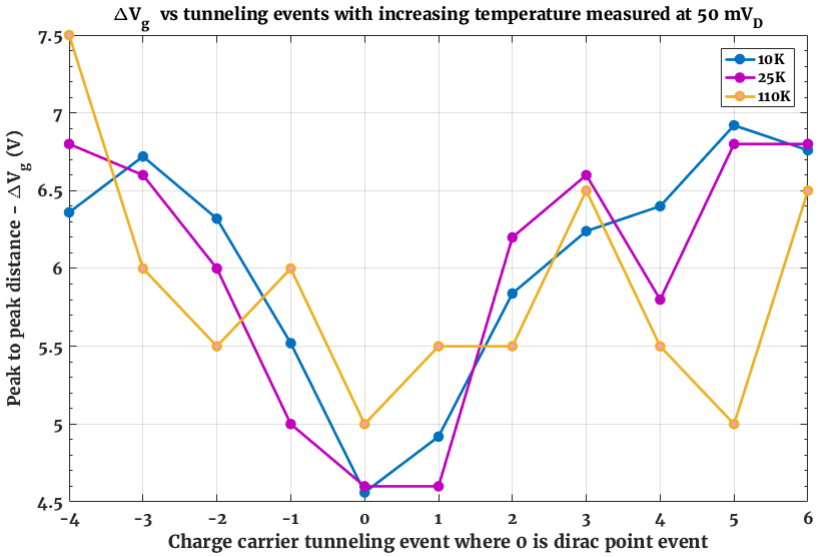

Figure 5.47: Measured ΔV_g with increasing temperature for increasing charge carrier tunneling events. The extracted data shows that for both 10 and 25 K the change in ΔV_g follows the behaviour of a single quantum dot with energy level space. However as the temperature increases the trend in the data is more randomized, but does show a minor relation to the increasing number of tunneling events in the Coulomb oscillation. Indicating an additional gate voltage dependent behaviour that can impact the energy level spacing measurements at 10 K.

5.6 Summary

There are 2 distinct results from this work, the first is the observation of a single quantum dot device with observed energy level spacing and the second is the divergent transport properties of CVD-graphene nanoribbons, where the key points of the divergent properties are the increase in Fermi energy gap due to an increase in the disorder potential of a CVD-graphene nanoribbon. However the data revealed a breakdown of the disorder potential induced increase in Fermi energy gap. Showing that the disorder potential is not a constant value for CVD-graphene and instead varies with increasing nanoribbon width.

Devices that match the current state of the art for graphene nanoribbons are observed, demonstrating devices that yield a large Fermi energy gap without sacrificing the mobility and on/off ratio of the device. This can be attributed to a multitude of factors. The design of the nanoribbons with 100nm wide leads and 100nm long devices improves the coupling of the quantum dots to the tunneling barriers. While the superior fabrication capabilities produce devices with 20 nm features. Lastly the CVD-graphene has shown that the increase in disorder potential can increase the single electron properties without significantly degrading the conduction of the device.

In this work the energy level spacing for a single graphene quantum dot SET has only been measured once, while the rest of the devices showed typical nanoribbon behaviour of multiple dot SETs. Although the effect of energy level spacing can be extracted. Until there is further evidence a calculation of the exact relation between the graphene

SET and number of charge carrier tunneling events will not become clear. However, to fully understand the observed energy level spacing, theoretical approaches need to be developed to explore the unique properties of this device. With a better theoretical model of the graphene device it should be possible to understand the unique spin states and degeneracy factors that contribute to the observed quantum dot properties. Additional experiments need to be conducted to replicate the single quantum dot device in a nanoribbon by altering the nanoribbon shape into a point contact constriction on purpose, introducing more local gates to probe the nanoribbon and remove the wide graphene lead barriers with dielectrics of a known capacitance and resistance.

The base characteristics of the CVD-graphene nanoribbon devices have been established providing insight into the direction future research will need to be taken. A base device of 100 nm long and 2o nm wide with 100nm wide on a 90nm oxide can be used in future studies to probe the fabrication aspects of the CVD nanoribbon transport properties. Any further investigations should include a device of this design as the standard device for a comparison measurement of the change in properties.

Chapter 6

Conclusions

6.1 Conclusion

When graphene's physical properties are considered, both benefits & downsides, it is still only a 2 dimensional material. Which presents itself as the ultimate limit in scaling in the vertical direction. Its prospects further broaden when considering the patterning down for SETs & Nanoribbon FETs. Yet a key element has not seen the progress it needs, is there is little point in fabricating a 2DM laterally when compared to a 3D crystal. Since they still yield the same density in a 2D plane. It has been a detriment to graphene that it is transferred onto silicon dioxide for devices to test the nanopatterning. The effects of the substrate and other materials degrade its properties. It is this very method of transferring graphene a single atomic layer material that most of its potential lies. If a single layer can be transferred with a high quality then even more can be stacked, but so far this had not been explored.

Rather than using multiple layers of 2DMs, the use of existing materials in nanofabrication is employed to stack graphene on nanowires as a proof of concept for the transfer-last process when fabricating graphene devices. It was unfortunate that there was not enough time to extensively characterise these devices electrically. Nonetheless the transfer-last process has shown that graphene can be naturally suspended across a sub 400nm gap or across a large area onto patterned electrodes without needed to do any post-processing to release the graphene layer for suspension.

Graphene's full potential has yet to be decided as a material for nanoelectronics. Most other materials have been put to the wayside, or lack the potential to create an entire new growth for the semiconductor industry. My work provides the framework to incorporate graphene devices at all points of an integrated circuitry. This has been by considering the nanopatterning of graphene into nanoribbons to investigate the scaling effects of a wafer scale process using CVD-graphene, where the first detailed investigations into the divergent behaviour of graphene that is produced using CVD is demonstrated. The inherent carrier density fluctuations that exist in graphene that contribute to the Fermi energy gap are increased due to the polycrystalline nature of the material. This

has the effect of increasing the Fermi energy gap up to 0.6 eV, at the cost of the on current. This work also shows that the disorder potential is not constant factor dependent on the carrier density fluctuation and is also influenced by the length of the graphene nanoribbons. So far though this has only be shown in devices that have a sub 20 nm width and requires more evidence for this to be a confirmed property of the disorder potential.

The investigations into the scaling of CVD-graphene has resulted in an advancement of the state of the art for graphene single electron transistors. Due to the naturally existing single electron tunneling properties within graphene nanoribbons rather than by design. Despite the tunneling properties being a intrinsic property clear Coulomb oscillations have been observed, demonstrating a single quantum dot with energy level spacing. Revealing new properties that can exist for a graphene SET, although only for 1 of the graphene nanoribbons that had been tested. The most significant issue this device presents is the exact origin of the observed SET properties. The current prediction is that a second constriction exists in the nanoribbon due to a defect in the HSQ when considering the possible differences that can exist between a device of similar dimensions. This creates a new significant undertaking of research into engineering a device that will recreate the same SET properties.

Although a suspended graphene nanoribbon using the transfer-last process to investigate the SET properties was unable to be produced. Some exciting properties of the devices that merit further investigation have been demonstrated. Future research is needed to broaden the understanding of nanoribbon properties since it is not as simple as previously observed and predicted. Even the single electron tunneling in a graphene nanoribbon holds a lot more potential and merits investigation into understanding the origin of its properties. Since the current properties of the best SET prove that graphene can approach the quality of silicon SETs and provides exciting potential for graphene to exceed the state of the art for SETs.

6.2 Future Work

This work has created a number of opportunities for future investigations into graphene nanoribbon devices and fabrication technologies. Using the base characteristics of the CVD nanoribbons studied in this work, it provides the framework to begin studying the process parameters and investigating new fabrication methods. Our wafer scale process provides the means to investigate the subtle variations in design parameters with a greater ease than exfoliated graphene due to sheer throughput possible that can be achieved with CVD-graphene. Combined with the developed transfer process it becomes possible to engineer a vast amount of different nanoelectronic devices for a variety of purposes. This presents a lot of opportunities in the future to explore these possibilities and new interesting device behaviour that occurs when using CVD-graphene.

6.2.1 Lithographic Control of HSQ pattern

The first step to advancing graphene nanoelectronics is to pin point the exact mechanism causing the single quantum dot with energy level spacing properties. From the results of 22-100 the expected cause of the clear Coulomb oscillations is point constriction within the nanoribbon region. This will require the fabrication of devices with a HSQ patterned that intentionally creates a 3 stage restriction in the nanoribbon, to recreate the unintentional single quantum dot properties, seen in figure 5.8.

This provides the opportunity to fabricate devices that can be wire bonded. To prevent the most significant issue when testing the devices when probing onto the contacts. Which ensures a stronger adhesion of the contact pad to the substrate and prevent the metal from being scratched away easily. This also provides the capabilities of testing the devices under a magnetic field. Since the cryoprobe station did not have this capability it meant the true properties of the SET could not be extracted to determine the spin states, mobilities and electron mass. If the devices can be wire bonded then the properties of these devices can be investigated in the same manner as has been done for previous 2DEG materials when investigating the energy level spacing properties.

Further to this the new devices can be fabricated to include local gates either as side gates or deposited across the device using the HSQ layer as a dielectric. Ideally the side gates would use metal rather than graphene to improve the yield and electric field control of the device. The use of graphene with rough edges could have an underlying effect on the side gating of the nanoribbon. By using the local gates the conduction across the wide-narrow-wide segmentation design can be analyzed to determine if the control of the tunnel barriers potential and coupling improves the SET.

Currently the best known description of the tunnel barriers is caused by extended wavefunctions from the nanoribbon and wide segments. These prevent electrons from tunneling to an accumulation of charge carriers that screens further charges from transporting across the narrow nanoribbon segment. Analyzing the tunnel barriers under a changing electric field can provide further information on the impact the transition from a wide to narrow segment. In addition designing the devices with different transition angles and widths of the wide segments can provide information about the transport mechanism that causes the SET properties of this type of device.

6.2.2 New fabrication processes

One of the possible reasons for the clear Coulomb oscillations could be caused by a grain boundary bisecting the nanoribbon and causing an effect on the SET properties. The difficulty with determining if this was the cause is the physics of a grain boundary bisecting a nanoribbon SET are unknown. Also imaging the graphene structure to find a grain boundary requires a suspended sample for STEM imaging. This can be done by using the same method by Tsen et al. [56]to deposit CVD-graphene on a silicon nitride membrane or by creating a fully suspended graphene device.

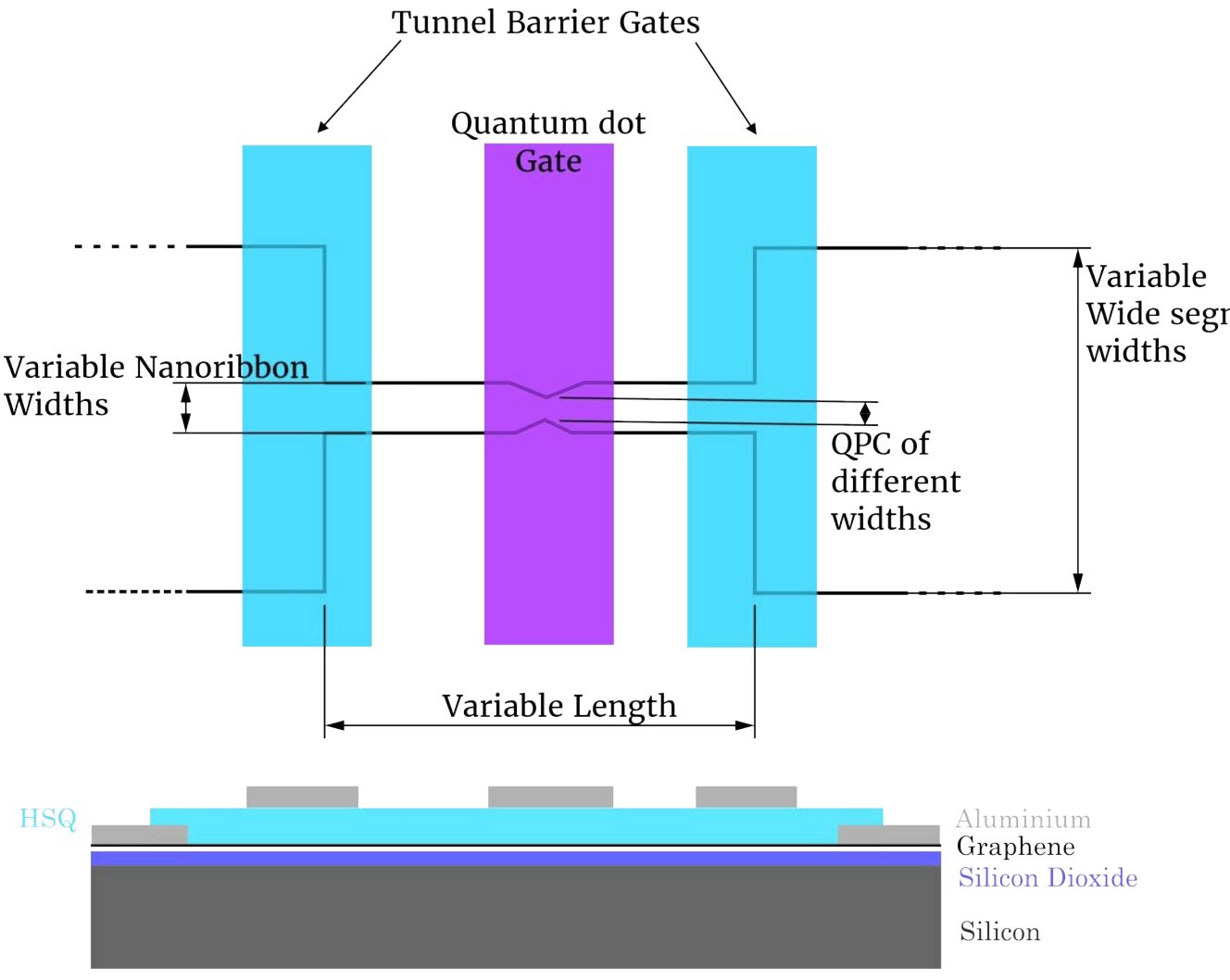

Figure 6.1: Schematic design of graphene nanoribbon with point contact constriction in the middle with local gates on top of nanoribbon to probe the control of the barriers connected to the quantum dot.

The other scenarios that could of lead to the unique characteristics is the formation of a bilayer or wrinkle in the CVD sheet that created new properties. These can be checked using a combination of Raman spectroscopy and HIM imaging of each device before etching to know if a device has this type of fabrication defect. Another interesting method that could be investigated is fabricating the devices by transferring two layers of CVD-graphene on top of each other to intentionally create twisted bilayer graphene across a wafer. Rather than hoping for an accidental defect to occur again.

Beyond attempting to discover the cause of the single quantum dot behaviour in the nanoribbon further investigations into using new etching methods and substrate support should be pursued. The first would be to develop the fabrication of devices with zigzag edge termination. This can be done using a hot hydrogen plasma to anisotropically etch the graphene in the zigzag edge direction to have a greater control over the nanoribbon pattern [118, 60, 119, 120]. The next process to develop would be the use of a material like hexagonal boron nitride [h-BN] that does not cause any doping and increases the device mobility [19] . With h-BN now available on a wafer-scale by growth on copper foil [121]. It should be possible to develop a wafer-scale process to encapsulate the graphene nanoribbons on either side with h-BN before fabrication as has been done with exfoliated flakes [122]. Using the anisotropic etch, improved substrate interaction and optimized device design a CVD-graphene nanoribbon superior to this work should be achievable.

6.2.3 Fermi energy gap relation

The issues regarding the disorder potential still need to researched to determine the cause of the length dependent behaviour observed in the CVD nanoribbons. This can be done at the same time as the new devices, but it would be best to focus on less fabrication parameters at a time. Firstly more devices need to be measured at wider widths and more length variations. But the devices should be designed to have repeated widths of the same size to compensate for the low device yield. Rather than the 1 nm step variations in the design before, the device lengths should scale from 25 nm (if possible) and increase in 25 nm steps up to a 250 nm length to provide a greater quantitative analysis of the Fermi energy gap results.

The next step would be to try and fabricate devices with a much smaller width than before without relying upon the undercut etch. With the established base parameters though the etch rate of the undercut should be something that should be carefully investigated as well. Combining with the anisotropic etch of the graphene nanoribbon will provide direct comparisons between the effect of the edge states on the Fermi energy gap and disorder potential.

6.2.4 Transfer-last suspended devices

Finally the use of the transfer-last process developed can be used to obtain the contact resistance of the different materials once it has been optimized further to prevent the large variance in measurements that was found earlier. Rather than attempt to create 2-probe contact devices again, the optimal method would be to suspend graphene across the nanowires. Using the large area transfer method to fabricated suspended TLM or 4 point probe structures. Additionally the transfer last process provides a method of contacting the graphene sheet from both sides if an extra material is deposited on the other side for a metal-graphene-metal stack. This would reduce the contact resistance even further than a oxide-graphene-metal stack.

The large area transfer process on amorphous silicon can now be used to fabricate using silicon or silicon on insulator to develop devices using crystalline silicon. To begin with the same investigations into the contact resistance should be achieved before attempting to fabricate suspended devices using the silicon as a gate and electrode material. An interesting prospect would be to use the charge transfer doping of graphene with doped silicon to create PN junctions of graphene without using the ambipolar doping.

Lastly the transfer-last process can be used to fabricate suspended graphene nanoribbon devices as the figure 6.2 shows. This would combine the optimized nanoribbon fabrication with the suspension of the devices with the transfer-last process to create suspended devices. These could be used for fabricating a new type of Nanoelectromechanical switch or an SET/nanoribbon that can be used with the STEM to investigate the crystallographic structure and electrical properties simultaneously.

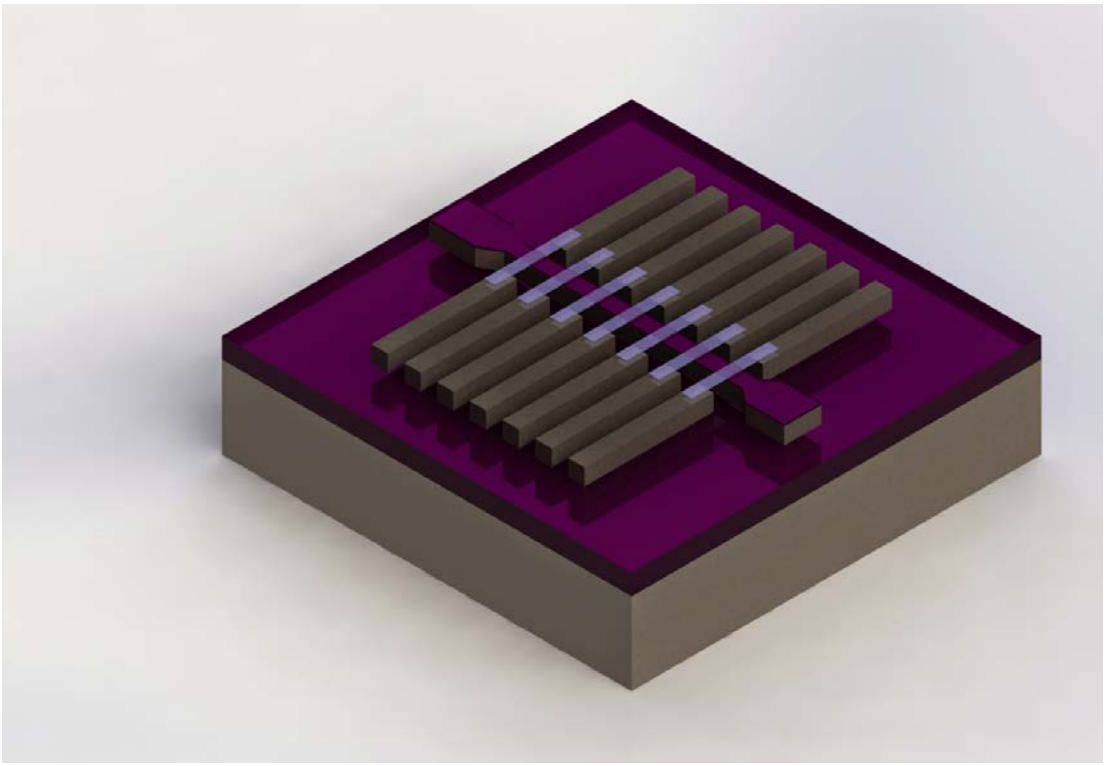

Figure 6.2: Diagram of an example use for the graphene suspended across a gate using the transfer last process

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