UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Optoelectronics Research Centre

PASSIVELY ALIGNED PACKAGING SOLUTIONS FOR SILICON PHOTONICS

by

Scott Reynolds

Thesis for the degree of Doctor of Philosophy

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UNIVERISITY OF SOUTHAMPTON

ABSTRACT

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Packaging is a critical component in bringing silicon photonics to application. Without low cost, high throughput packaging, the per-unit cost of silicon photonic integrated circuits will be too high for mass markets.

Passive alignment of optical fibres to silicon photonic waveguides would significantly reduce the assembly time currently required where active alignment is labour intensive and time consuming.

In this work a design is presented that has the potential for high volume cost effective packaging. The design accomplishes this by supporting and positioning multiple fibres relative to a silicon photonic integrated circuit. The capping chip passively aligns the fibres to silicon nanowires via a grating couplers. V-groove structures in the capping chip are used to support and position the fibres and the end facet of the v-groove reflects the light down on to the grating coupler. Plugs on the capping chip align with holes on the photonic chip assuring accurate positioning and optimal coupling.

The processing required has been detailed and demonstrated, including a hybrid lithography process, crystallographically aligned v-grooves and highly accurate alignment structures. Once combined these processes will passively align fibre optic cables with silicon photonic waveguide gratings with a misalignment less than 2um which in theory will produce an added loss less than 1dB, grating couplers have been produced based on a bespoke design fitting the demands of the packaging solution and show a loss of 2.7dB with room for improvement compared to a simulated result of 1.67dB.

Academic Thesis: Declaration of Authorship

I, SCOTT REYNOLDS,

declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

PASSIVELY ALLIGNED PACKAGING SOLUTIONS FOR SILICON PHOTONICS

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Journal papers

[1] C. G. Littlejohns, A. Z. Khokhar, D. J. Thomson, Y. Hu, L. Basset, S. A. Reynolds, G. Z. Mashanovich, G. T. Reed, and F. Y. Gardes, "Ge-on-Si Plasma-Enhanced Chemical Vapor Deposition for Low-Cost Photodetectors," Photonics Journal, IEEE, vol. 7, pp. 1-8, 2015.

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[3] D. J. Thomson, K. Li, F. Y. Gardes, Y. Hu, M. Nedeljkovic, C. Littlejohns, R. Topley, A. Z. Khokhar, S. Stanković, J. S. Penades, C. J. Mitchell, S. A. Reynolds, G. Z. Mashanovich, P. R. Wilson, and G. T. Reed, "Silicon photonics at the University of Southampton," presented at the PIERS 2015, Prague, Czech Republic, 2015.

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Patents

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Book Sections

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Chapter 1: Introduction

1.1: Silicon Photonics

Photonics itself is a huge industry that encompasses a wide variety of fields from high power industrial lasers through to medicine. Traditionally these industries tend toward using exotic compounds produced from group III elements such as Gallium and group V elements such Arsenic. These are combined to produce III-V compounds for example, Gallium Arsenide or Indium Phosphide. These compounds are used in order to exploit their direct bandgap which makes lasing possible. Silicon has been successful within the electronics industry mostly due its low cost, ease of processing, excellent native oxide and abundance. Although not direct bandgap, it has many promising attributes that gives it great potential within photonics. What is seen as its greatest advantage is its compatibility with the very large scale integration (VLSI) involved in electronics manufacture; III-V materials are inherently incompatible due to them being contaminants within a CMOS (Complementary Metal Oxide Semiconductor) fabrication facility. Furthermore, photonic concepts using silicon can benefit from the many years of development of silicon electronics processing techniques. Silicon has the potential for truly monolithic integration allowing for low cost optical communications in many areas such as: fibre optic communications to the home, short reach optical interconnects or even intra-chip optical communications.

1.2: Motivation

In the context of photonics and electronics, packaging is the process of taking a fabricated device and its relevant I/O peripherals and wrapping it all up in to a marketable product that is reliable, robust, and easy to use. Common integrated circuits (ICs) are a good example of this, where a silicon chip's input and output lines are attached to easy to use pins or pads and the whole device is encapsulated in plastic or ceramic for protection and usability. This is a small sample of many electronic packaging methods that have a wide variation depending on the application. When considering photonic circuits, the goals are the same e.g. convenience

and protection; however, the approaches are significantly different. Unlike electronics, light must be accurately directed, or coupled, into an on-chip waveguide which is no easy task. In fact, this is the primary issue in packaging photonic circuits where often fibre to coupler alignment accuracies are less than one micrometre compared to the sub ten micrometre requirements for electronics.

Previously, production of optical devices has not been on a mass scale and so ultra-low cost packaging has not been required. Therefore, current solutions are usually labour intensive, costly, and slow due to the requirement of active alignment techniques. Active alignment is a process whereby light is launched into a device and monitored at the output, the input and output fibres are then adjusted to maximise the transmitted power. Although this is the best way to ensure maximum transmitted efficiency, the process is not cost effective for mass market devices. In fact, this process can amount to a third of the cost of developing a photonic integrated circuit (PIC)[1]. The preferred method of alignment uses passive techniques where structures produced through manufacture align the fibre automatically, vastly improving development time and cost.

1.3: Techniques

In this work, in order to produce a reliable, passive packaging solution, two separate chips will be used; a device chip complete with waveguides, devices and grating couplers combined with a capping chip utilising alignment V-grooves. These two chips will sandwich optical fibres, securing them and allowing precise alignment. The V-grooves will also provide a reflecting surface allowing in plane coupling from fibre to device and vice versa.

The device chip for testing purposes will have waveguides and bespoke grating couplers, produced on an SOI (Silicon on Insulator) platform. They will be produced using e-beam lithography and dry plasma etching. The capping chip will utilise a thick silicon nitride (Si_3N_4) layer on silicon wafer where the Si_3N_4 will be formed in to alignment plugs, also using dry plasma etching, and the V-grooves will be formed using wet KOH (potassium hydroxide) etching. Whilst e-beam lithography is not a production tool, the tolerance analysis implemented in this work has assumed the tolerances associated with high quality commercial lithography systems, thereby making the work compatible and transferable to real applications.

Full assembly and testing is beyond the scope of this project but will be considered and discussed in future work.

1.4: Thesis Layout

Chapter 2 of this thesis begins by introducing the fundamentals regarding coupling and describes fundamental packaging concepts and methods. It then goes on to describe how these are implemented in the state of the art, at the time of writing. This is followed by a description of designs which are considered to improve on the current state of the art. Chapter 3 describes the tools, equipment and how they are set up to familiarise the reader with their basic function before describing the recipes and processes used in chapter 4. Chapter 4 discusses the development of the processes required for producing the solutions laid out at the end of chapter 2, including the final process flows for producing samples ready for assembly. Finally, chapter 5 summarises and concludes the thesis and goes on to outline further work that can be completed to improve the concept further.

Chapter 2: Background

The background chapter will start by broadly discussing the fundamentals required to undertake the project; explaining coupling and packaging, and why it is necessary. This leads on to a discussion of what has been accomplished in the state of the art, identifying the limits in current research that will be tackled in this project, thereby setting this work into context.

2.1: Fundamentals

2.1.1: Fibres

Optical fibres are made of strands of glass of the order of 125µm in diameter, approximately the thickness of a human hair. They transmit data in the form of light which is confined within the fibre by multiple layers of glass with different optical qualities [2](Figure 2.1). Fibres hold significant value in the sphere of communications as they can transmit large amounts of data quickly, over long distances compared to its predecessor, copper.

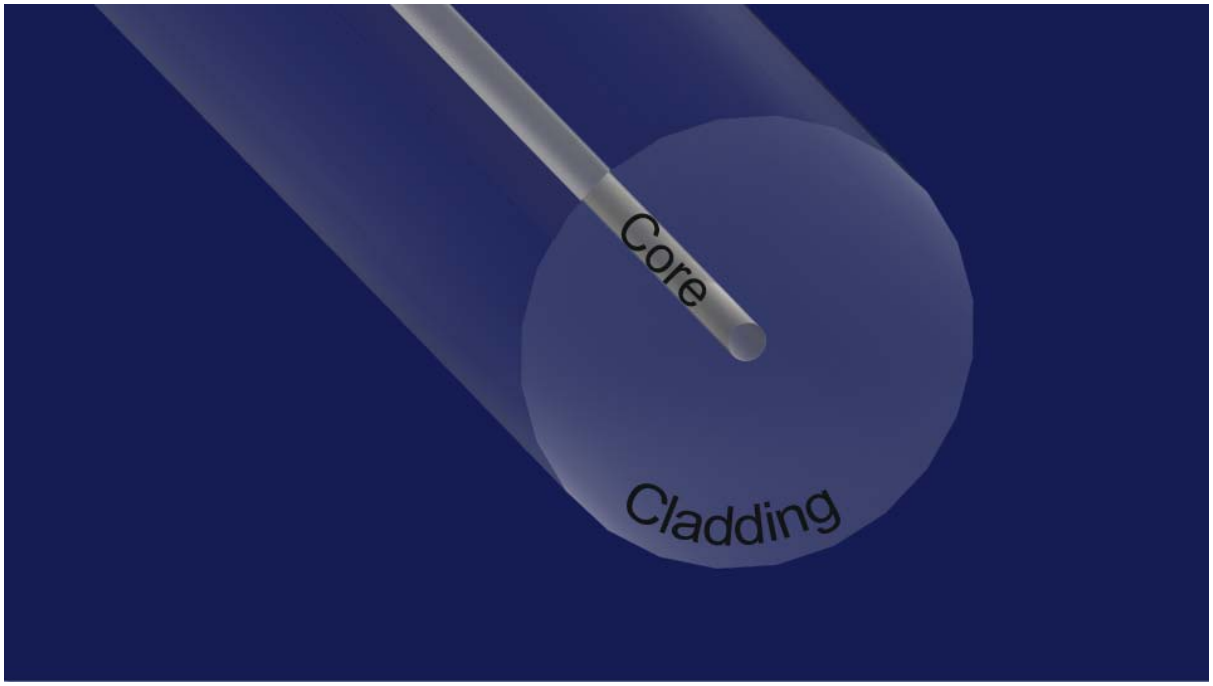

Figure 2.1 An optical fibre showing the core and cladding which confines transmitted light.

Fibres mainly come in two forms, multimode and single mode, the main difference between them is the size of the core which affects the constraints for propagation. Multimode fibres allow multiple modes of light to propagate due to a larger core size compared to that of a single mode fibre, which as the name suggests only allows propagation of a single mode. Multimode fibres are finding application in next generations of communications systems as they can allow higher data rates. They are, however, susceptible to modal dispersion which is attributed to the individual modes propagating at different effective velocities along a given length of fibre thus resulting in the spreading a pulse or bit of data in the time domain. Dispersion limits the speed of transmission or length of the cable as eventually the pulses overlap rendering the data undecipherable. This means that multimode systems are used for

short range interconnects. Figure 2.2 shows the ranges and speeds that single mode and multimode fibre technologies operate over[3].

The larger core size of a multimode fibres also complicates the coupling of light between the fibre and the small waveguides used in silicon photonics, which will be discussed later in this chapter.

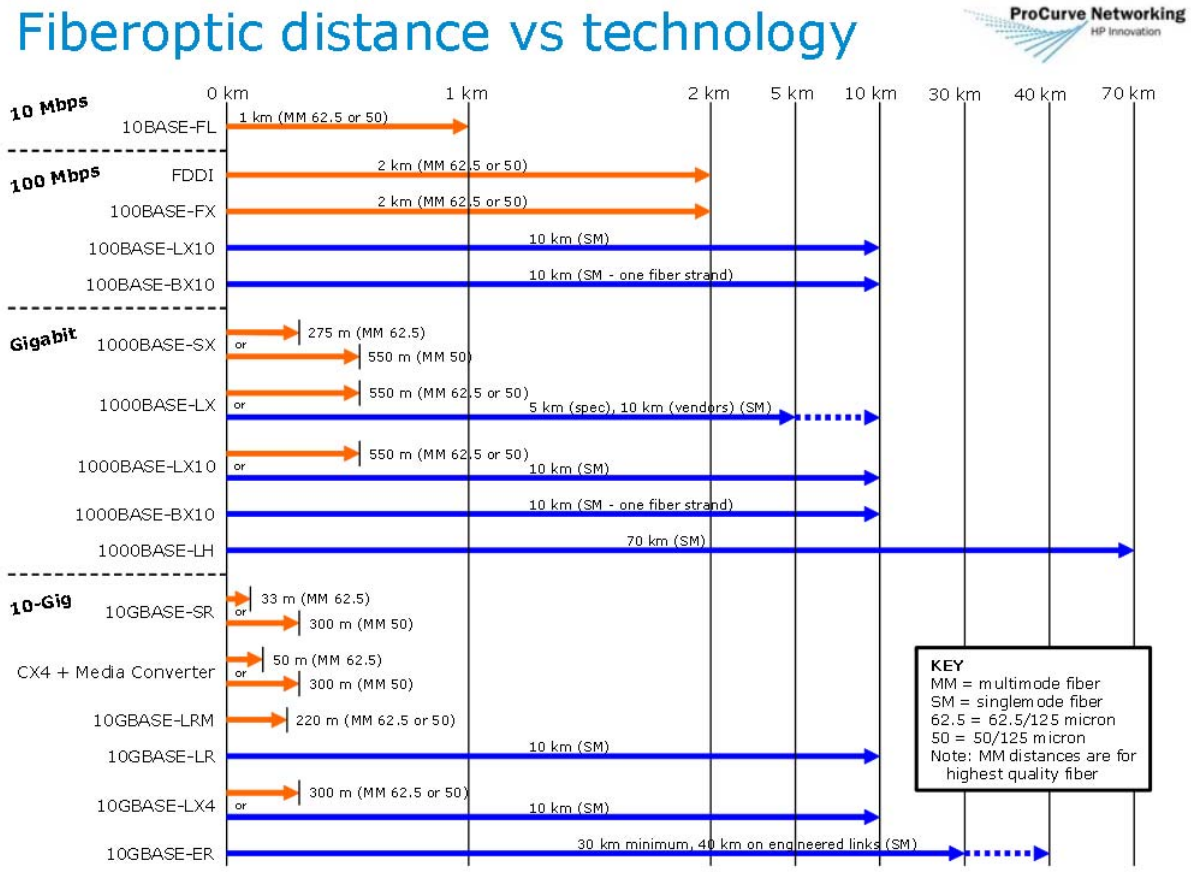

Figure 2.2 A chart displaying different fibre technologies, their speeds and distances[3].

Single mode fibres are used for long distance communications and are more common than multimode fibres. They are also more common within silicon photonics, even though silicon photonics is focused towards short range interconnects this is somewhat a misnomer, the networks that silicon photonics needs to penetrate are those that are too short for long haul communications to address due to their current high cost. This boundary lies around 10km and the distances between racks within a data centre can be as far as this, which prevents multimode from being desirable because of its limited range of 2km (Figure 2.2). Single mode methodologies allow easier coupling to silicon photonic circuits with sub micrometre

waveguides and also allow higher aggregate transmission rates per fibre via wavelength division multiplexing (WDM) which is also possible in multimode fibre, but is limited by its high modal dispersion[4]. Due to these advantages and the broad use of single mode fibres, this project will only use single mode fibres, specifically SMF28 fibres made by Corning. This is a commonly used optical fibre, and therefore has widespread application.

2.1.2: Waveguides

Waveguides perform the same routing function as an optical fibre, except they route light on a photonic circuit rather than along a cable. There are many different waveguide structures both in single mode and multimode configurations. However, due to the constraints mentioned previously and the fact that many optical devices used in silicon photonics are not compatible with multimode operation, only single mode waveguide structures will be considered here. Even with this restriction, there are still many structures to consider. Photonic crystal, suspended, strip, and slot waveguides have all been demonstrated in the photonics community [5-8](Figure 2.3). However, frequently when designing near infrared devices, rib waveguides are used, due to their lower loss[2], and potential advantages when creating active devices[9]. Rib waveguides can also be defined and etched in the same process step as grating couplers which have been shown to work well, further details of this are reported in section 4.3: Grating Couplers. Therefore, in order to conform to common processes, rib waveguides will be used for this project. It is important to note that this decision does not rule out other methods and minor modifications are required to scale the project design to operate with a range of waveguide types.

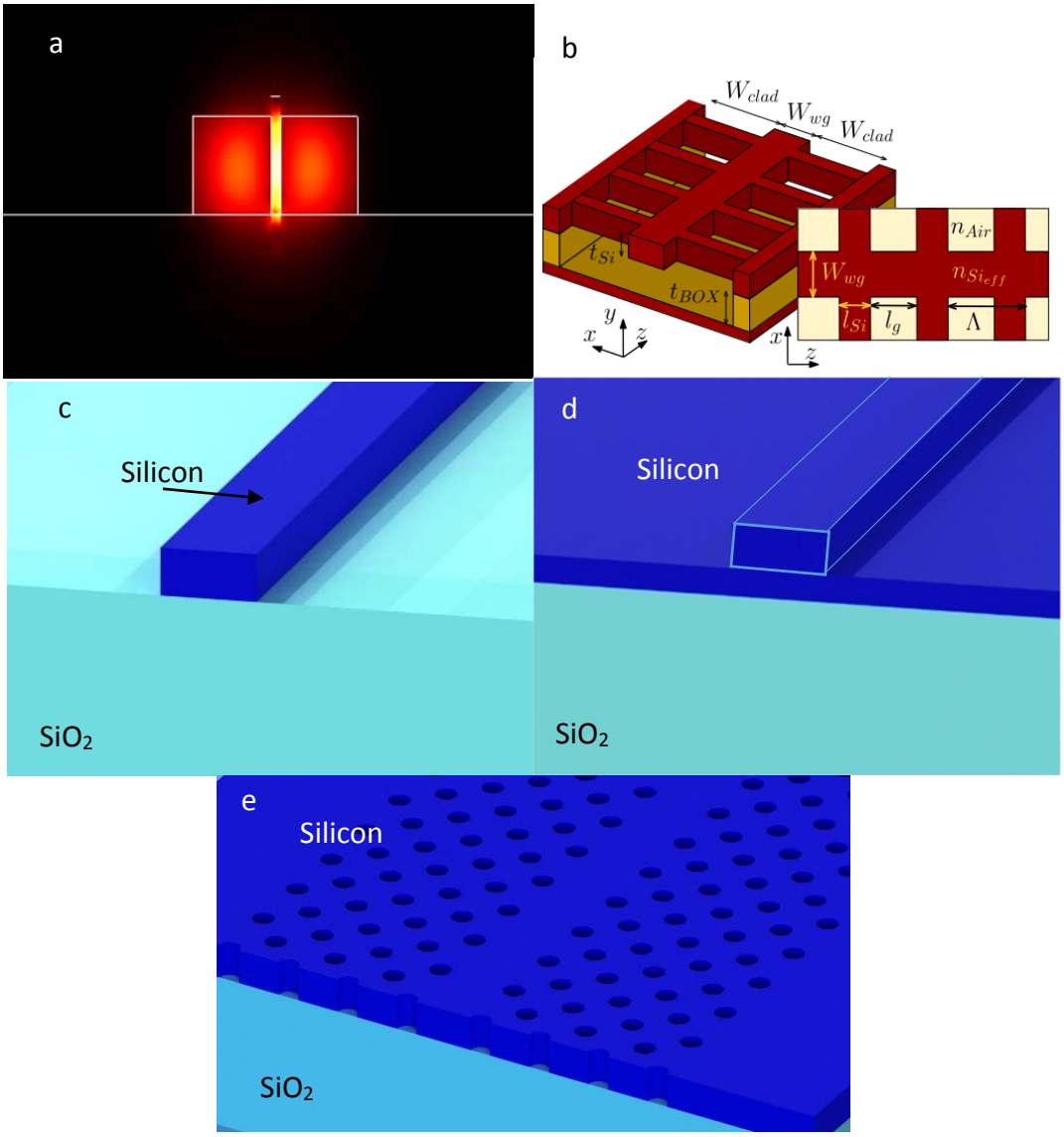

Figure 2.3 (a) a representation of a slot waveguide with a simulated guided mode[5]. (b) A schematic drawing of a suspended waveguide[6]. (c) A schematic drawing of a strip waveguide[10]. (d) A schematic drawingof a rib waveguide[10]. (e) A schematic drawing of a photonic crystal waveguide.

2.1.3: Coupling

Coupling from an optical fibre to a silicon nanowire is difficult for a number of reasons, predominantly due to the dimensions of the fibre core being much larger than the dimensions of a silicon waveguide, producing significant differences in mode field profile as shown in Figure 2.4[11]. This figure shows the single mode fibre to have a core diameter of 8m and the waveguide to have dimensions of around 400 x 200nm. Without manipulation of this field profile, severe coupling losses can be expected, up to -16dB [11]. Light transmission is also sensitive to refractive index differences between waveguides making coupling from one medium to another a challenge.

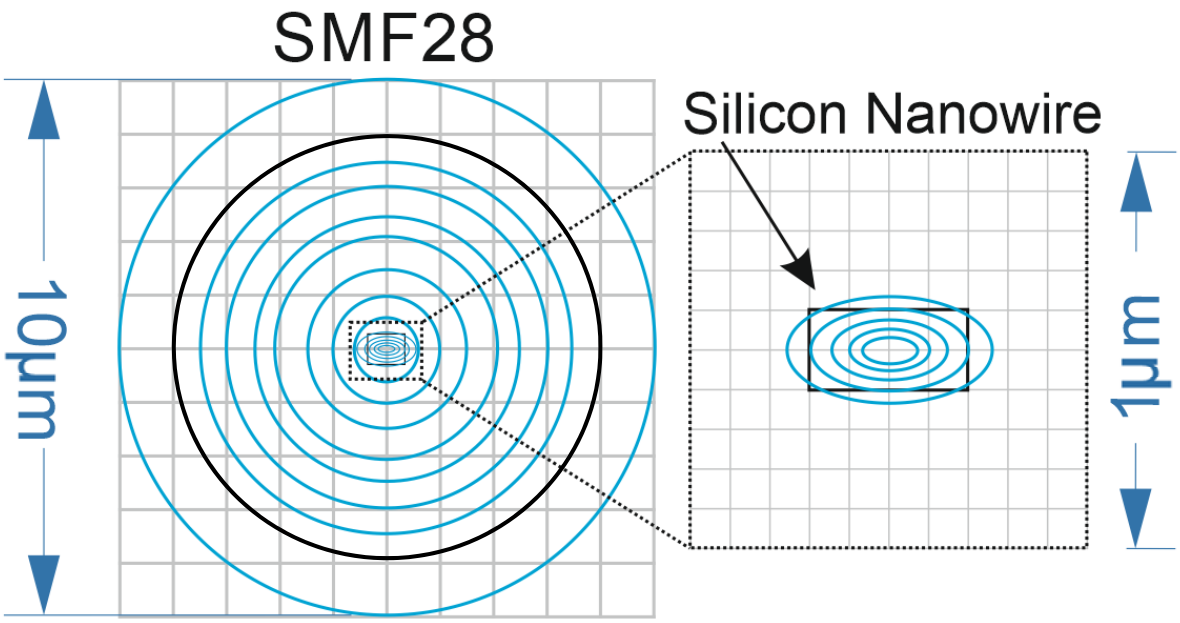

Figure 2.4 Displaying the large field profile mismatch between an SMF-28 optical fibre and a photonic nanowire. Figure reproduced from[11]

2.1.4: Tapering

Waveguide tapering is the method wherein the field profile is manipulated allowing for easier transmission from one medium to another. This improves coupling efficiencies as the field profile is usually manipulated with the receiving medium in mind typically a fibre. There are a number of methods of tapering and the primary ones are discussed in this section.

One Dimensional Tapers

In One Dimensional (1D) tapering the waveguide is extended in one direction in order to expand the mode field profile laterally (Figure 2.5). This is a reciprocal process, so propagation in the opposite direction would reduce the mode field profile. These tapers are very simple to manufacture if the taper is only varied in a horizontal plane, as this is merely a function of the photolithography mask used for the device, and 1D tapers therefore allow rudimentary field profile manipulation. Although the resulting profile can be as wide as desired it is still restricted in the vertical direction. Whilst this can improve the coupling efficiency, it results in a method that is still very inefficient, and is inadequate for commercial applications.

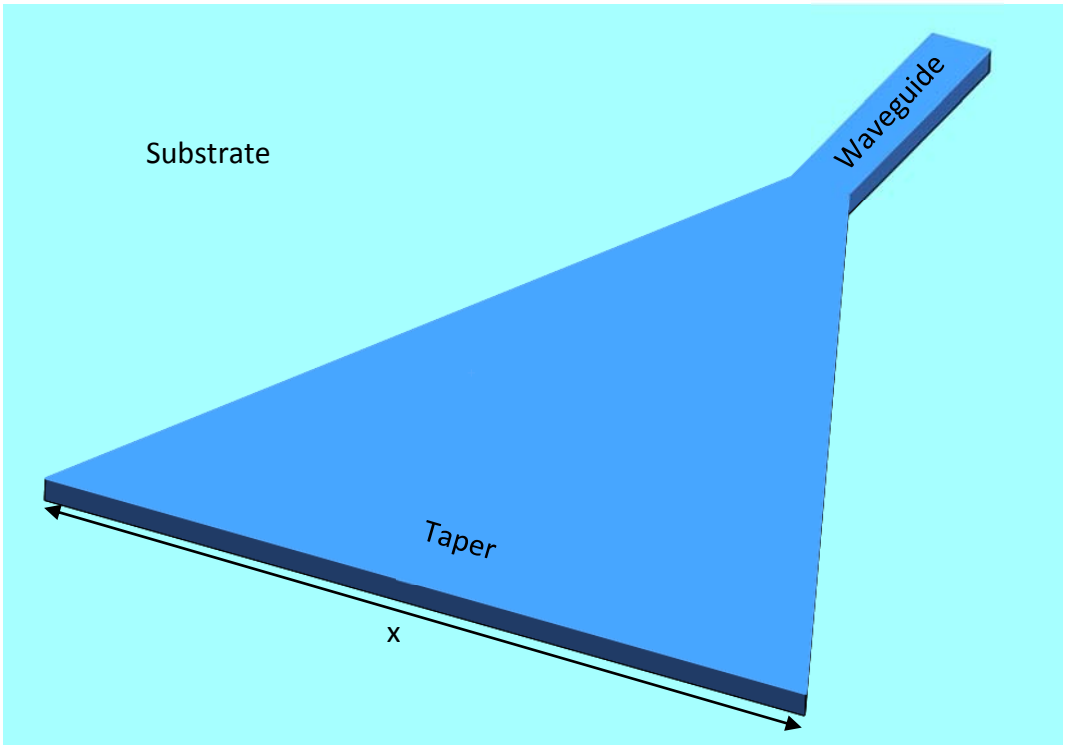

Figure 2.5 A one dimensional taper

Two Dimensional Tapers

Similar to single dimension tapers, the waveguide is expanded to increase the field profile to better match that of an optical fibre. In this case the waveguide is also increased in size both horizontally and vertically allowing the field profile to expand (Figure 2.6). Two dimensional tapers (2D) are very advantageous as the resulting spot size can easily be made to match that of a fibre. However, 2D tapers are generally difficult to produce as the vertical dimension of the waveguide needs to be in the order of 10 microns. From a manufacturing point of view this is a challenge as it requires a thick layer in the locality of the taper, which in turn requires either specialist wafers or deposited materials which both require specialised manufacturing techniques that can limit subsequent development.[12][13]. Furthermore, it is extremely difficult to produce smooth vertical waveguide sidewalls as the taper dimensions reach a few hundred nanometres, resulting in high scattering loss. In addition, 1D and 2D taper require antireflection coatings (ARC) to be applied to reduce Fresnel reflection at the silicon-air interface.

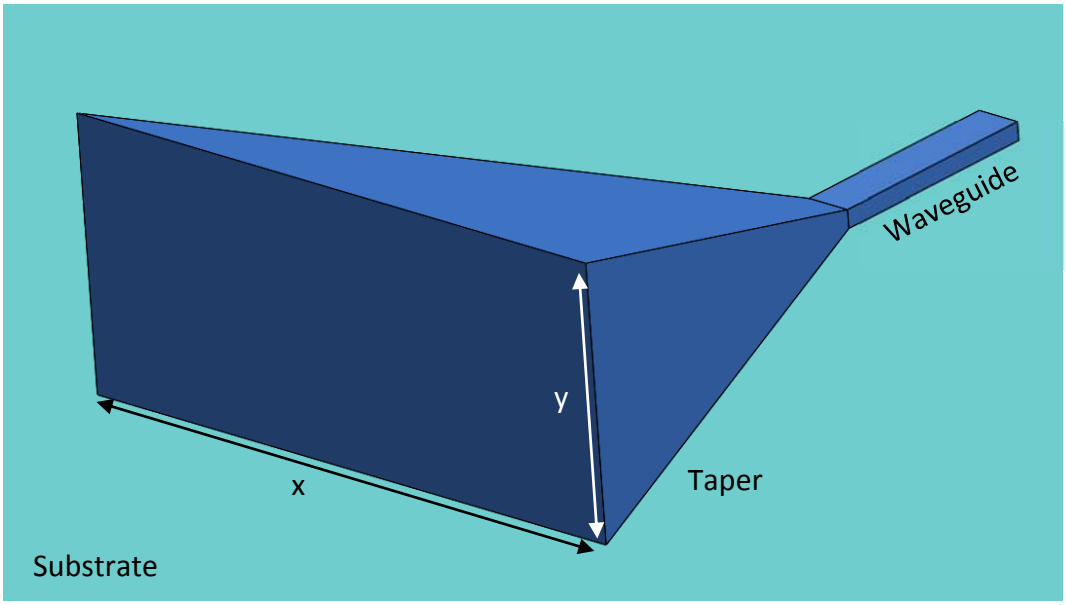

Figure 2.6 A two dimensional taper

Inverted Taper

Inverted tapers, in contrast to the multi-dimensional tapers discussed previously, narrow the waveguide to a point which squeezes the mode out of the waveguide. This allows the field profile to spread out into a surrounding medium that forms a cladding waveguide. In a typical example Pu et al. [14] have shown that if the taper is created inside a polymer block that is 3x3µm in dimension, then the field profile expands to this size and allows low loss coupling of 0.36dB to a lensed fibre (Figure 2.7).

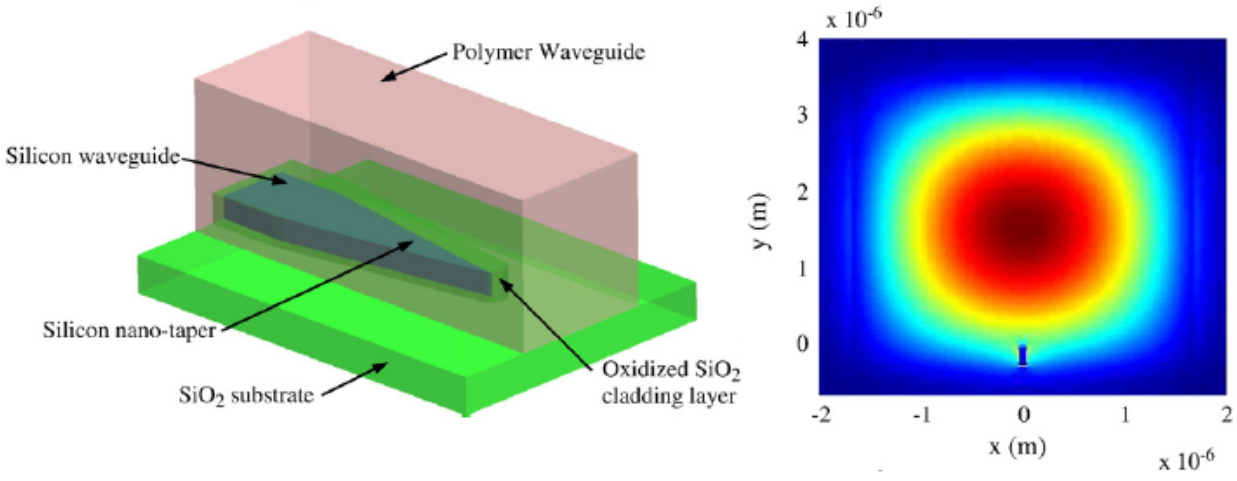

Figure 2.7 Inverted taper structure (left) and field intensity image of the mode inside the polymer waveguide (right)[12].

B. Ben Bakir et al[15] produced a similar structure using silicon dioxide as a cladding waveguide coupled to a lensed fibre with losses of 0.25dB and a 3dB spectral range of more than 300nm. Due to the restrictions in deposition of cladding waveguide materials, the spot size conversion is limited, these examples along with most other inverted tapers rely on lensed fibres to reduce the spot size which increases misalignment penalties and reduces their desirability as a packaging component. Further to this, fabrication is complicated by the need for a very small tip at the end of the waveguide taper, typically less than 100nm (Figure 2.8), with fabrication tolerances that are difficult to meet. This is observed by T. Barwicz et al who avoid using a tip in their inverted taper packaging solution by using metamaterials, which will be discussed further in section 2.3.2.

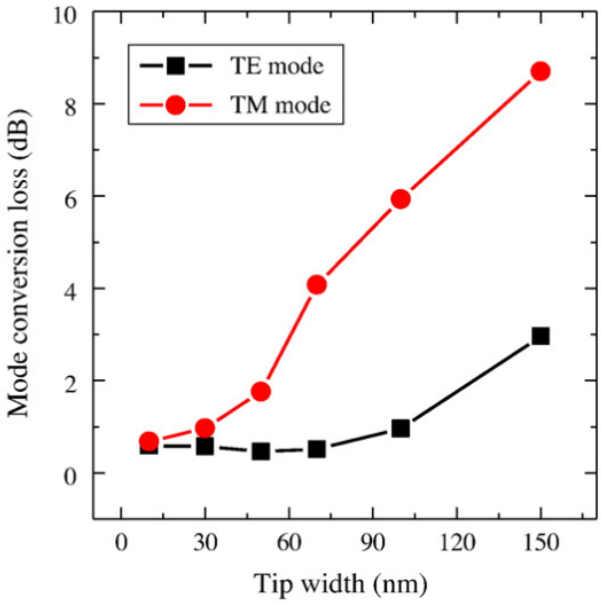

Figure 2.8 A graph showing the mode conversion loss with respect to tip width, showing the need for a small tip[14].

Taper Transition and Footprint

Regardless of the tapering method the footprint and transition are both an important consideration. The length of the taper is associated with its efficiency, where a shorter taper will exhibit more loss than a longer one and so a compromise must be made between having a larger footprint and a low loss taper. Linear tapers are easy to produce but need to be very long to achieve an adiabatic transition in which case propagation loss can become a factor. Non-linear tapers smooth the taper transition, reducing loss and has been shown to reduce taper length by over 50% while maintaining a consistent loss[16]. A good example of a

nonlinear taper is shown in Figure 2.9 where the paper also compares the transmission loss of linear and different nonlinear tapers.

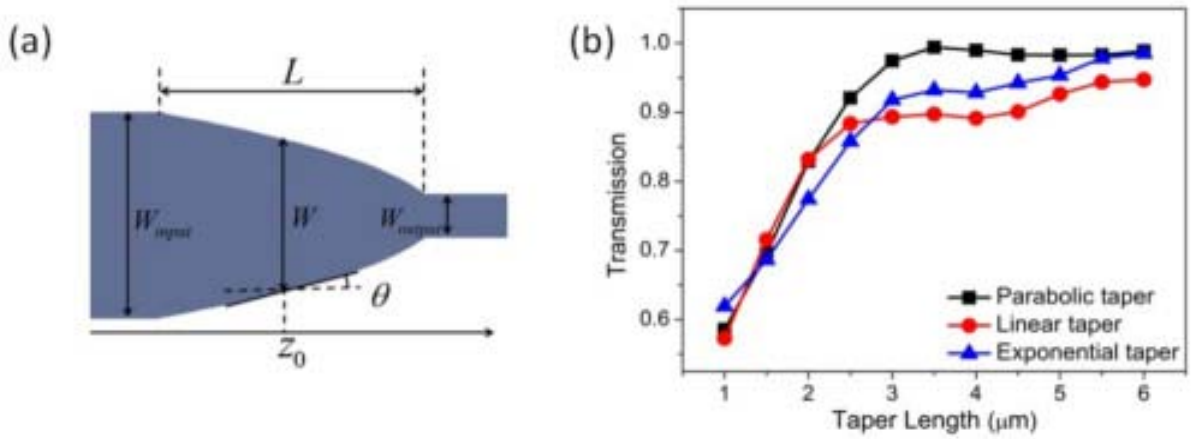

Figure 2.9 An example of a parabolic taper (a) and a transmission comparison with respect to taper length for parabolic, linear and exponential tapers (b) presented by Tong Ye et al [17]

2.2: Coupling Methodologies

Different coupling methodologies require different tapers. Before deciding which taper could be used, the type of coupling must be considered. Within photonics there are two coupling methods that are widely used; in plane coupling and out of plane coupling, both of which will be discussed in the following section.

2.2.1: In plane coupling

In plane, is performed by simply aligning a fibre to the facet of a waveguide (Figure 2.10). The waveguides have usually been subjected to field profile manipulation methods as mentioned previously. The alignment is, in theory a simple concept, however in practice there can be many complications. For example; the facet that will receive or transmit the light must be as smooth and as clean as possible. In order to accomplish this, the device chip must be perfectly cleaved and if that is not possible, typically many hours of polishing are required. In itself polishing is a labour intensive process and can produce problems of its own such as debris damaging the device chip or causing additional scattering. Etched facets are also an option, an example of this is shown later in this chapter in section 2.3.2. Chips can also be cleaved but that results in inconsistent facet quality.

Further disadvantages are apparent with aligning to the edge of a sample as dicing the wafer removes the possibility for wafer scale testing.

In plane coupling can take advantage of all of the field profile manipulation techniques discussed previously and, even though there are still significant field profile mismatches after manipulation, very low coupling losses can be achieved with sub-micron alignment precision.

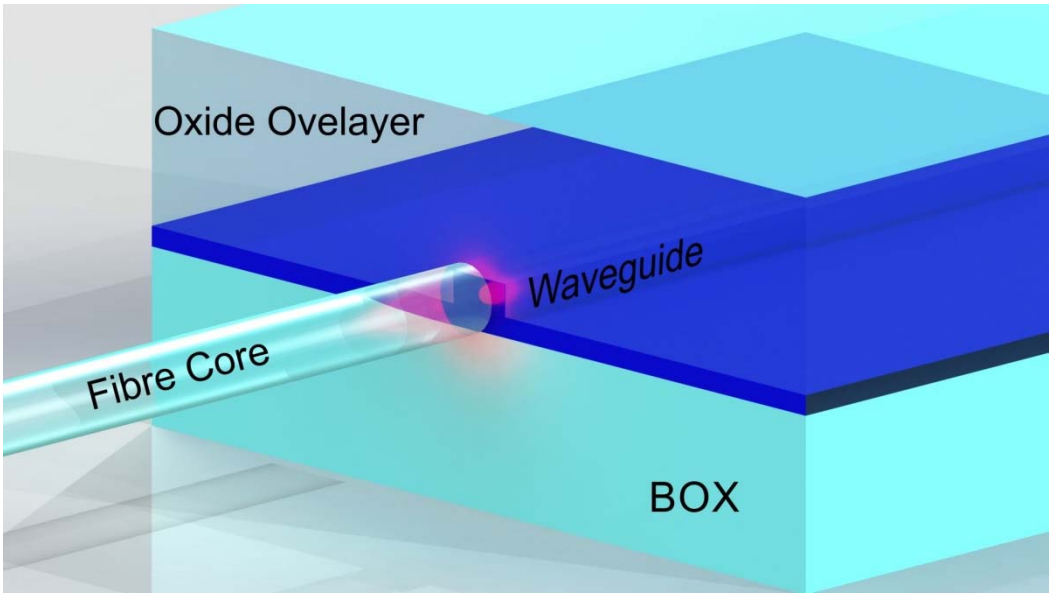

Figure 2.10 An example of Butt Coupling where light from a fibre is being launched into a waveguide. The fibre cladding has been omitted for clarity

Because of the small feature sizes, the misalignment penalties are severe. Typically, different device chips have different structures, depending on size and geometry, so there are no generic loss characteristics to quote. However as an example, Figure 2.11[11] shows the loss as a function of displacement of a lensed fibre to a 3x3µm waveguide which is typically the size of an expanded inverted taper waveguide.

It can be seen that ±0.5µm gives a 1dB loss, which shows how difficult a fibre can be to align even after modal expiation techniques such as inverted tapers.

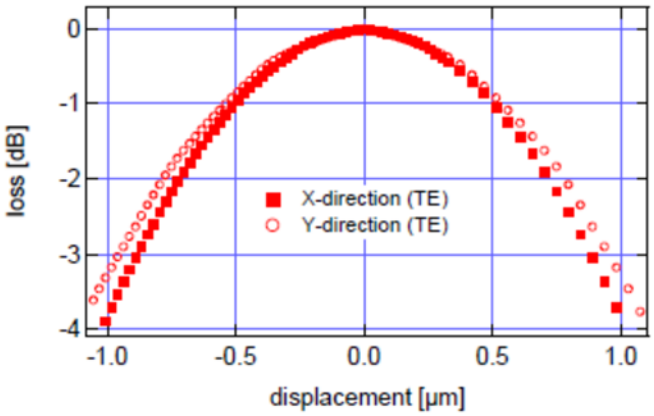

Figure 2.11 Loss verses displacement characteristics of a lensed optical fibre being aligned to a 3x3µm facet [11].

All things considered, butt coupling does have a key advantage as it utilises an in plane approach which allows the fibres to be supported easily. Potentially, passive alignment techniques, with the use of v-grooves, can also be combined with butt coupling. These will be discussed in further detail later. Most significant of all its advantages are polarisation diversity and optical bandwidth which allow very high data rates through wavelength division multiplexing because more wavelengths are available.

2.2.2: Vertical Coupling

In order to avoid the difficulties of butt coupling, light could be introduced from anywhere on the device surface; however, the basic concept is fundamentally flawed.

For example

Figure 2.12[2] shows a waveguide cross section and an incident beam on the surface at an angle of θa. z is the direction of intended propagation, β is the waveguide propagation constant and n_1, n_2 and n_3 are the respective refractive indices of each of the three materials. In order for light to travel in the z direction within the medium n_1, the propagation constants in the z direction must be the same. The beam will propagate in the medium n_3 with a propagation constant of $k_0 n_3$ in the direction of propagation (where the arrow is pointing).

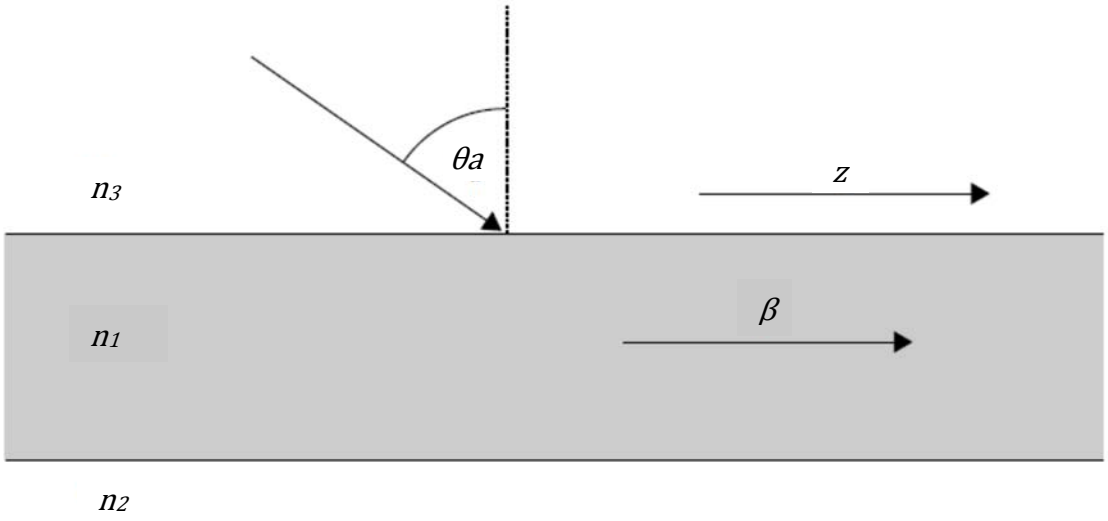

Figure 2.12 A diagram of an incident ray on the surface of a waveguide[2].

In order for the light to propagate in the z direction in this medium the propagation constant k_z must be equal to 2.1:

$$k_z = k_0 n_3 \sin\theta_a \quad 2.1$$

So we now know the propagation constant in z for n_3 and this must match β, the propagation constant in z, within the waveguide:

$$\beta = k_z = k_0 n_3 \sin\theta_a \quad 2.2$$

Now this is where a flaw appears; β is determined by the critical angles of the upper and lower claddings of the waveguide. The critical angles are the angles at which light will be totally internally reflected within the waveguide allowing propagation to occur. The maths of the critical angle will not be discussed here but the critical angle limits β to be:

$$\beta \geq k_0 n_3 \quad 2.3$$

This means that the condition in 2.3 can never be met as $\sin\theta_a$ will never be unity (i.e. θ_a = 90°) and coupling will not occur. Hence something is required in order to make vertical coupling possible. There are two preferred methods for this, one being prism coupling which introduces a prism to the top of the waveguide and reduces the refractive index change between n_3 and n_1 and allows the phase match condition to be true. Prism coupling does show potential, however the development steps are more complex than grating couplers, which also satisfy the phase match condition. The difficulties are due to the requirement of a

thick layer of a high refractive index material in the region of the coupler, similar to the problems seen when trying to create two dimensional tapers[2].

Grating couplers (Figure 2.13) utilise periodic recesses on the top surface of the waveguide. The recesses create a periodic modulation of the effective refractive index of the waveguide with respect to the wavelength of light, satisfying the phase match condition. Careful design of the recess depth, period and mark/space ratio allow precise optimisation for a given fibre approach angle[2, 18].

As mentioned previously the propagation constant of the waveguide is, β, however the periodic nature of the grating now permits a number of added propagation constants, shown as:

$$\beta_p = \beta_w + \frac{2p\pi}{\Lambda} \quad 2.4$$

where Λ is the period of the grating and $p = \pm 1, \pm 2, \pm 3, etc.$ is a series of diffraction orders for the diffraction grating. In order for the phase match condition to be true a number of changes need to be made; firstly, in order for β_p to be higher than $k_0 n_3$, p must be negative. It is also normal to design the gratings such that there is only a single phase match with a waveguide mode, therefore $p = -1$ and the waveguide propagation becomes:

$$\beta_p = \beta_w - \frac{2\pi}{\Lambda} \quad 2.5$$

and the phase match condition becomes:

$$\beta_w - \frac{2\pi}{\Lambda} = k_0 n_3 \sin\theta_a \quad 2.6$$

Writing βw in terms of the effective index N, 2.6 becomes:

$$k_0 N - \frac{2\pi}{\Lambda} = k_0 n_3 \sin\theta_a \quad 2.7$$

and on substituting for k_0 we obtain:

$$\Lambda = \frac{\lambda}{N - n_3 \sin\theta_a} \quad 2.8$$

This allows the design of a grating with a period for a desired coupling angle and wavelength, but this doesn't necessarily provide an efficient grating coupler. Many variables complicate grating design such as the size of the waveguide, the thickness of the buried oxide, the thickness and makeup of a cladding layer, the field profile of the coupled light and the etch depth of the grating coupler. As there are so many variables, a complex study is required to understand if a grating coupler is likely to be efficient and so simulations are regularly carried out to model ideal grating couplers under specific conditions. Often waveguide structures, buried oxide (BOX) and cladding thicknesses etc. are already defined due to their own efficiencies and so these can remain constant to reduce simulation complexity. Tuning the remaining variables e.g. aspect ratio, period and etch depth, is still a laborious task and so simulation tools such as the Lumerical FTDT solutions have convenient built-in features to aid in designing the most efficient grating coupler for a given scenario. For this project, the particle swarm optimisation was particularly useful as it allows the optimisation of multiple variable ranges and the software will complete a large number of simulations converging to the best performance[19]. This will be discussed further in section 4.4: Grating Coupler Design.

Adding complexity to the design of a grating coupler can yield higher efficiency, for example non-uniform gratings can be used to minimise the difference in mode field profile[20], and will be discussed later in this thesis.

When using grating couplers with SOI waveguides, some light is directed downwards and is lost to the substrate, so buried reflectors can be used to reflect the light back up and subsequently improve efficiency. An example of this has been demonstrated by D. Taillaert et al who improved grating efficiency by 31% [21].

A combination of a non-uniform grating with a metal backside mirror was presented by Y. Ding et al[22], boasting a record coupling efficiency of -0.58dB with a 3dB bandwidth of 71nm.

Footprint can be an issue for grating couplers as tapering structures can be very long. Focused gratings can be used to reduce taper lengths and F. van Laere showed an eight fold reduction in taper length with no added loss[23].

In order to address the lack of polarisation diversity in grating couplers two dimensional couplers have been created that split transverse electric (TE) and transverse magnetic (TM)

polarisations at the point of coupling. L. Carroll et al. showed the best example of this in terms of loss with 0.95dB of coupling loss and low polarization dependant losses of 0.3dB[24].

The surface grating approach (Figure 2.13) avoids having to cleave the chip and makes gratings specifically beneficial to wafer scale test procedures. More importantly however, the grating design allows for a much larger acceptance area as the dimensions are not restricted by the thickness of the silicon over layer. This means alignment tolerances are significantly increased as shown in Figure 2.14[11] where this example demonstrates only 1dB of loss for over 2µm of displacement in both the x and the y axis. Although advantageous in many ways, a vertical approach is not ideal for packaging; it makes securing the fibre problematic as it must be adhered and supported robustly enough for commercial applications. It also cannot utilise any well-developed forms of passive alignment. In many cases these gratings can be produced in a single etch step, where waveguides and grating couplers are defined in the same lithography step[21] which streamlines production in comparison to any butt coupling technique or prism coupling.

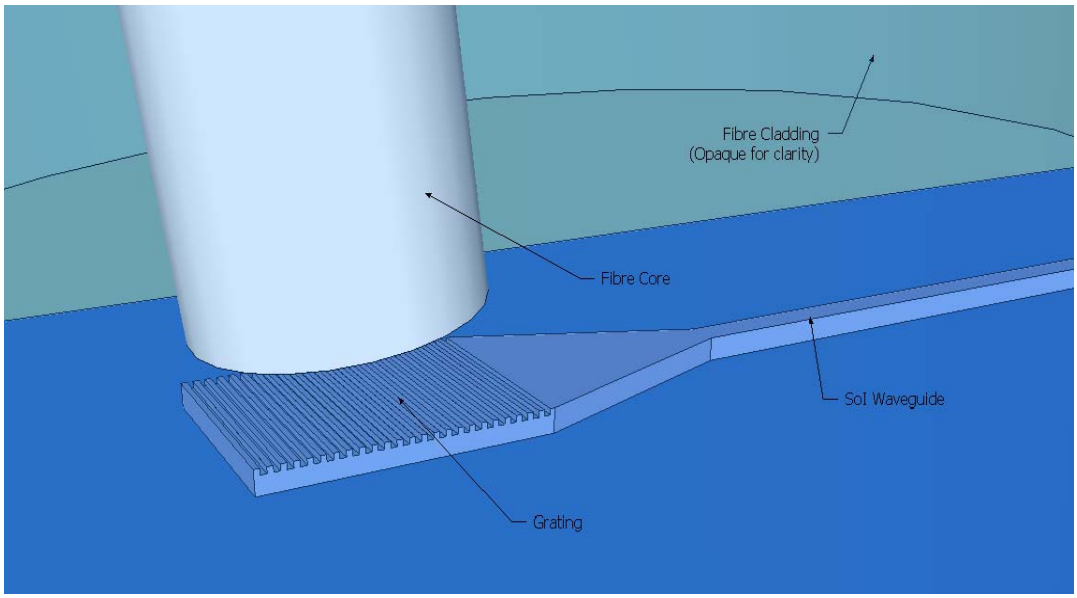

Figure 2.13 A diagram of a fibre being aligned to a grating coupler.

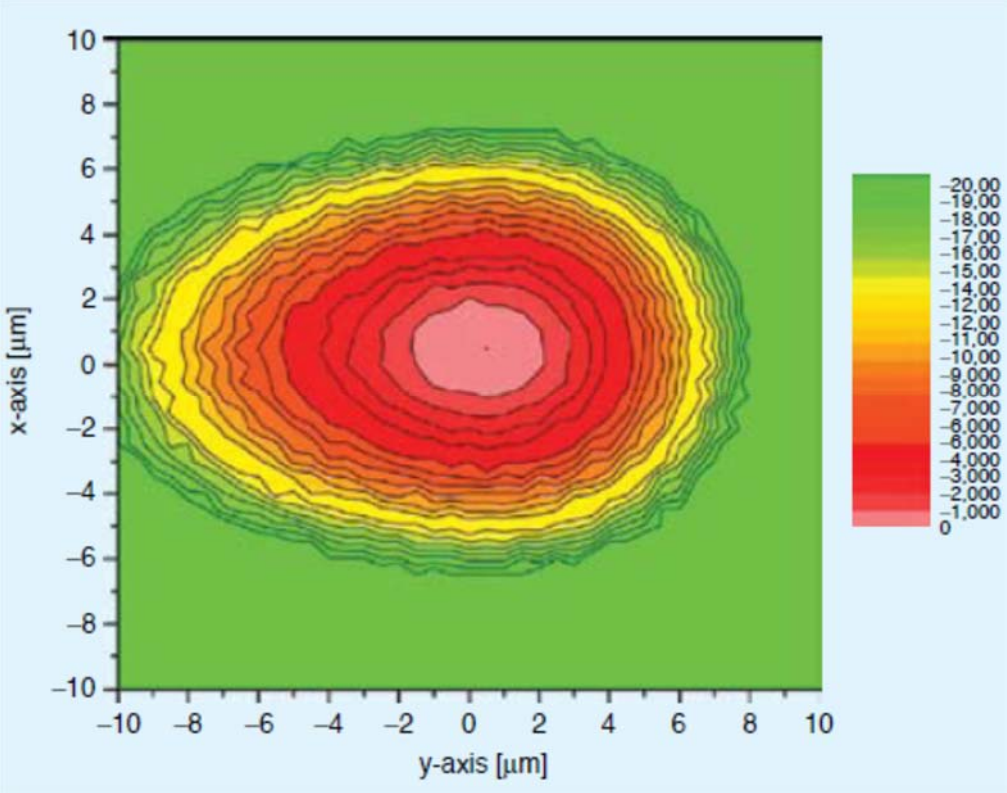

Figure 2.14 Miss-alignment characteristics of a grating coupler, the key on the right shows the loss in dB [11]

2.2.3: Comparison

Different coupling methodologies have their pros and cons, whenever an approach is considered, compromises are necessary (Table 2.1). Grating couplers are limited in their spectral range (70nm -3dB[22]) and polarisation diversity[24] and can be perceived as inefficient with efficiencies ranging from 30-46%[20]. This can be improved significantly up to 88%[22] with the addition of features such as backside mirrors and anodization, however this typically increases fabrication complexity. A vertical approach does not align to traditional packaging methodologies but in their simplest form gratings make PIC development, testing and packaging simpler and cost effective. Their relatively large alignment tolerance[11] and ease of access make them a strong choice from a packaging perspective.

Table 2.1 A Comparison showing the advantages and disadvantages of butt coupling and grating coupling

	Grating Coupling	Butt Coupling
Spectral Range	Low -	High ++
Efficiency	Low -	High ++
Approach	Out Of Plane -	In Plane +
Wafer Scale Testing	Yes +	No -
Sample Prep	Low ++	High ---
Alignment Tolleranc	High +++	Low ---

In plane coupling is reported to accomplish up to 92% efficiency[14], has wide spectral bandwidth (300nm)[15] and are polarisation diverse compared to grating couplers. However, requiring access to the edge of the chip is limiting, chip preparation is time consuming and misalignment tolerances are high. The in plane angle of approach for butt coupling does make it ideal for packaging but misalignment tolerances make passive alignment particularly difficult.

2.2.4: Antireflection

When coupling from one medium to another there is always some undesired reflection due to a change in refractive index. This reflection is approximately 31% for a silicon to air interface at normal incidence and can induce a loss of 1.6dB[2]; to combat this, antireflection coatings can be used. The fundamentals behind antireflective coatings are beyond this text, however they comprise a layer deposited on the facet of a waveguide to reduce reflection. Antireflection coatings are rarely used for silicon photonic packaging because index matching fluids or adhesives are more often used to ease the refractive index change between the fibre and waveguide.

2.3: Literature Review

Although limited, there have been advances in silicon photonics packaging, some of which have been implemented in production. This section will outline some of those demonstrated products. Inspiration can also be obtained from other areas of photonics which use similar techniques and technology to exhibit the same goals. These examples can be split into two different groups and will be described in the following sections. The first of these will be solutions based on an out of plane approach and the second on in-plane couplers.

2.3.1: Out of Plane Solutions

Approach angle is a key component in packaging, and an out of plane approach is not often desirable as it makes securing and supporting the fibres problematic. The following solutions have tackled this problem, creating both commercial and research based applications.

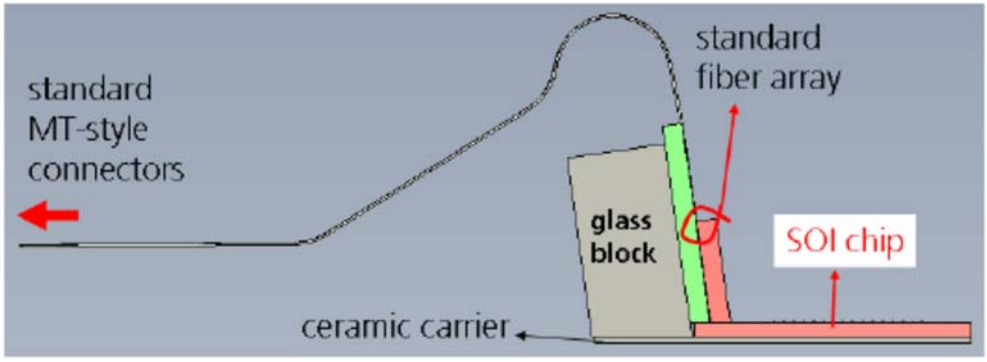

Figure 2.15 Multi-channel fibre array grating coupled to an SOI chip using v-groove etched blocks as support [25].

Zimmermann et al have produced a range of solutions based on waveguide gratings[25], for example, Figure 2.15 shows a solution using fibre arrays vertically aligned to an SOI chip that have been sandwiched between two blocks for support. One of the blocks supports the fibres with v-grooves, positioning them to the correct pitch and alignment with a ±1µm tolerance, whilst the other block holds the fibres in the v-grooves. The assembled block is then polished to an angle reducing back reflections and allowing the fibres to sit directly on the gratings. Once positioned the block is secured using UV epoxy. This method is actively aligned and the additional loss caused by the packaging process is 2dB ±1dB. These losses are high considering that it is actively aligned.

Luxtera have used a similar solution to develop a wavelength division multiplexing (WDM) transceiver [26] which demonstrates 40Gb/s data rate over four channels (Figure 2.16). The packaging process is not described in detail in the article.

These solutions show that with improvement, grating couplers could be used in the process of packing. However, current solutions are still bulky, lossy and actively aligned. They do not fit into traditional packaging schemes, and although they demonstrate the potential for grating couplers within photonic packaging, much improvement is needed before true mass production can be realised.

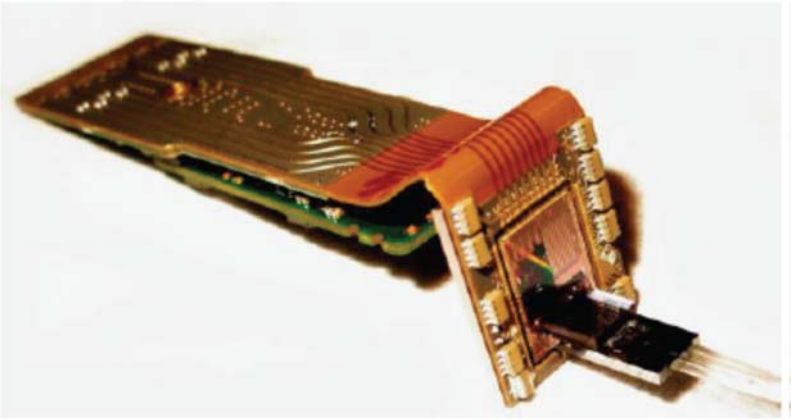

Figure 2.16 Luxtera 40Gb/s transceiver using grating coupled fibre arrays [26].

2.3.2: In Plane Coupling Solutions

Photonic packaging is not limited to silicon. The packaging of lasers has often had to overcome the same difficulties when trying to couple to photonic waveguides, especially when trying to realise passive alignment. M. S. Cohen et al developed the approach shown in Figure 2.17; it shows an in-plane coupling method, utilising v-grooves and a capping chip for passive alignment [27]. The experiment used four separate parts; a v-groove chip for fibre support, a LASER chip, a substrate to hold them together and a glass alignment plate. The fibre and laser chips have alignment marks defined by lithography that match alignment marks on the alignment plate. The v-groove chip and laser chip are moved in to position while being viewed through the alignment plate, once positioned they were held against the alignment plate by a vacuum applied through the alignment plate itself. Solder is applied to metal pads on the substrate, it is heated and raised under the other two chips that have matching metal pads on their underside. When they come in to contact, the solder is cooled and the device is secure.

This is a long, complex process and is technically passive alignment but too lengthy for high throughput production.

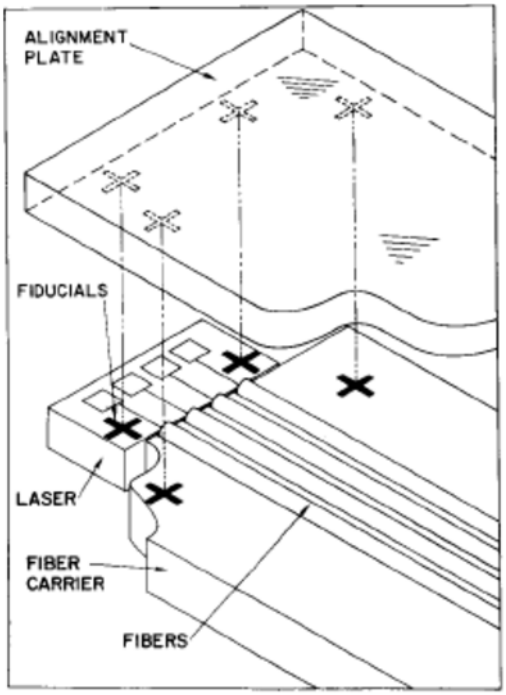

Figure 2.17 Shows a laser chip, fibre carrier and capping chip allowing passive alignment [27]

J.V. Galan et al[28] have attempted to make an in-plane version of the fibre blocks from the previous section. They have mounted electronic and photonic circuits on a sub-mount carrier, and a fibre block is aligned to the photonic chip which is secured by glue (Figure 2.18). Single grating efficiency of 24% is reported but the additional loss of the packaging approach is not specified.

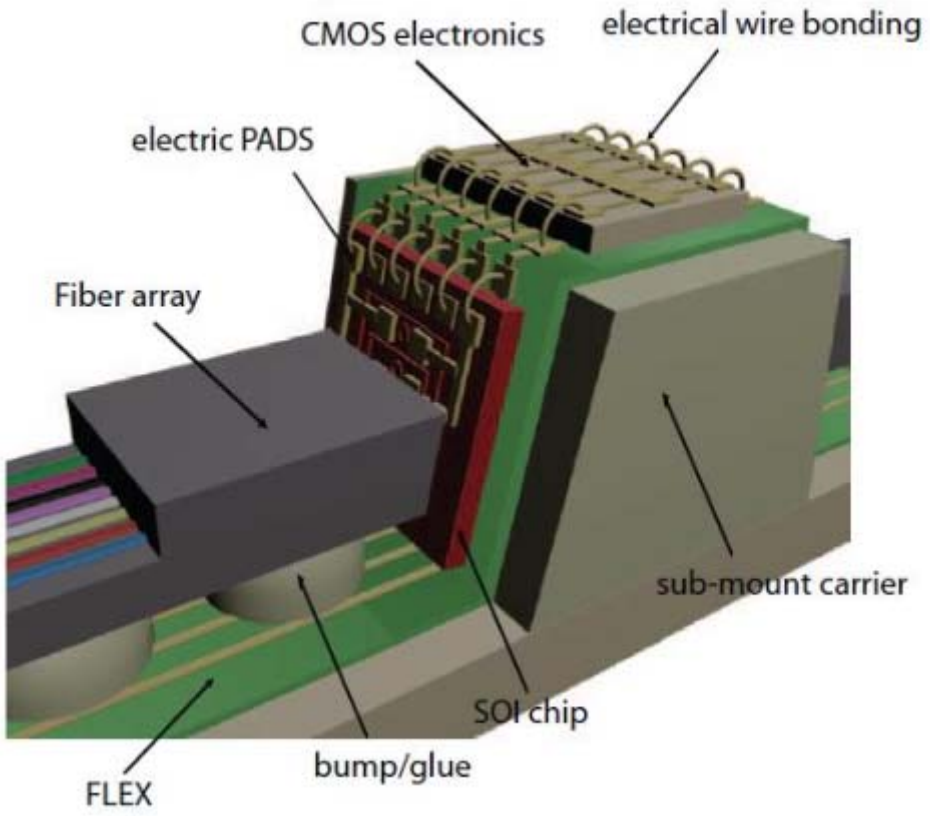

Figure 2.18 Low profile silicon photonic package utilising a sub-mount carried to support ICs and fibres[28].

A solution which utilises V-grooves to allow passive alignment was also produced by J. V. Galan et al[29](Figure 2.19). It boasts ±300nm alignment tolerances which are crucial for this type of packaging. 400nm wide strip waveguides are etched in to a 220nm/2µm silicon (Si)/silicon dioxide (SiO_2) SOI wafer, inverted tapers are used to couple adiabatically in to a SiO_2 waveguide etched in to the BOX. This waveguide is then under etched using potassium hydroxide (KOH) which also creates a v-groove to support a fibre. Losses of 7.5dB are reported partially due to the lack of an upper cladding. Coupling losses of ~1-2dB could be expected here but an upper cladding would make fabrication troublesome.

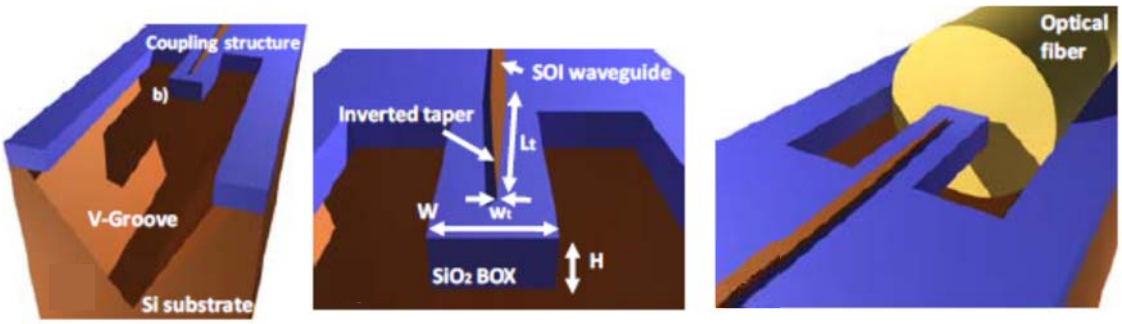

Figure 2.19 Butt coupling using v-grooves and a novel undercut solution to avoid cleaving and polishing [29].

In the past year IBM have shown a lot of interest in packaging and have identified that "novel approaches to photonic packaging are required for silicon photonic technology to reach its full potential"[30]. They have produced a number of packaging approaches and one that is particularly significant is shown in Figure 2.20 which is similar in construction to the concept shown in Figure 2.19. except that instead of a typical inverted taper, they use a metamaterial taper made up of a subwavelength grating which eases the manyfacturing tollerences of a standard inverse taper. They report -1.3dB in peak transmission efficiency at O-band (1260-1360nm) wavelengths with a 0.8dB penalty over a 100nm bandwidth while submerged in index matching fluid.

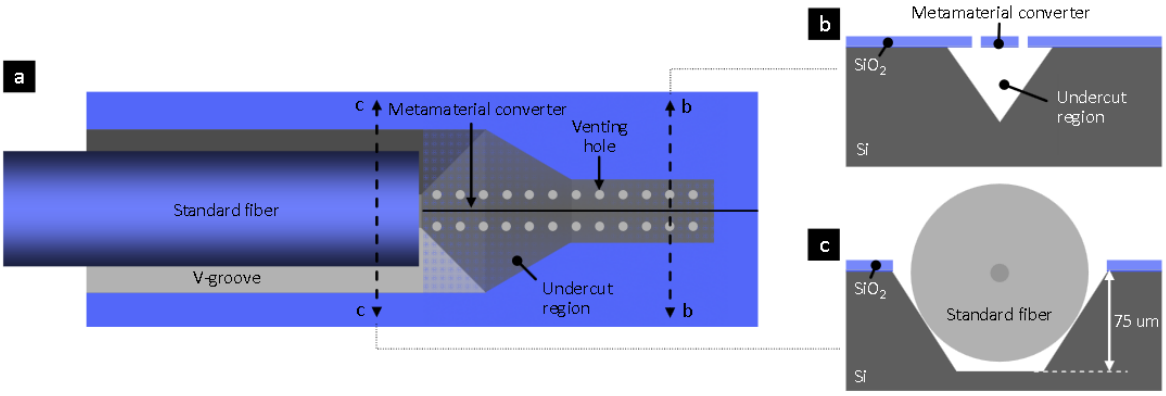

Figure 2.20 "Schematic of metamaterial fiber interface with integrated v-groove fiber self-alignment structure. (a) top-view, (b) cross-section through the suspended metamaterial converter, (c) cross-section through the v-groove and fiber"[31]

They have also demonstrated this technique using multi-fibre arrays [32] as shown in Figure 2.21, boasting a worst case misalignment of 1.3µm without mention of loss. They align 12

fibres using a polymer block to support the fibre but also allows some movement for the fibres to align themselves within the v-grooves.

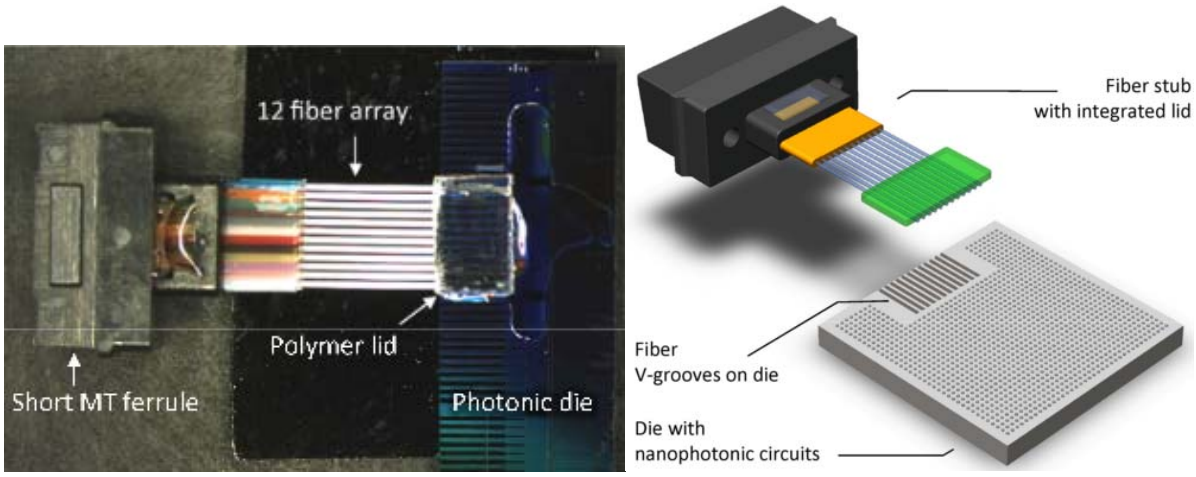

Figure 2.21 (Left)"Top-down optical micrograph of a fiber stub assembled to a photonic die. The length of the fibers can be customized to a given application"(Right) A schematic showing the fibres held by a polymer lid and the optical chip with v-grooves.[32]

Another interesting solution is shown in Figure 2.22 for which Luxtera have filed a patent. This solution utilises the benefits of grating couplers while employing an in-plane approach using an angled fibre tip as a downward reflector[33].

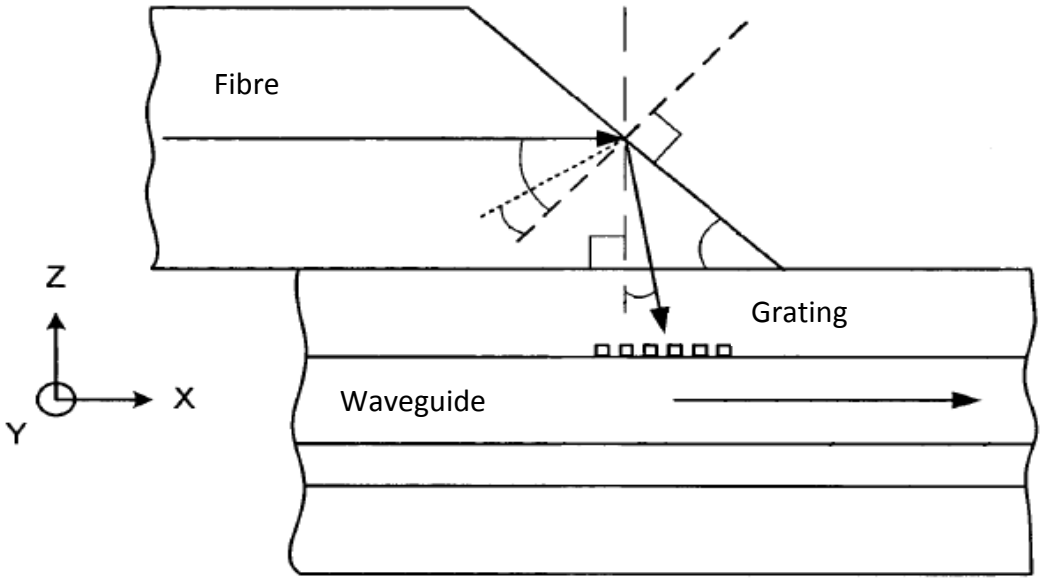

Figure 2.22 Combining the advantages of in plane coupling and grating couplers for a novel packaging solution [33].

ePIXfab have brought this patent in to reality and now offer a modular packaging solution utilising this in plane approach in both single (Figure 2.23 left) and multi-channel (Figure 2.23 right) approaches[34]. They boast a single fibre excess loss of less than 0.2dB with a total loss of 4.5dB. This is an actively aligned solution which in the single fibre regime requires polishing of a fibre and alignment in not just x, y and z, but also in rotation as well.

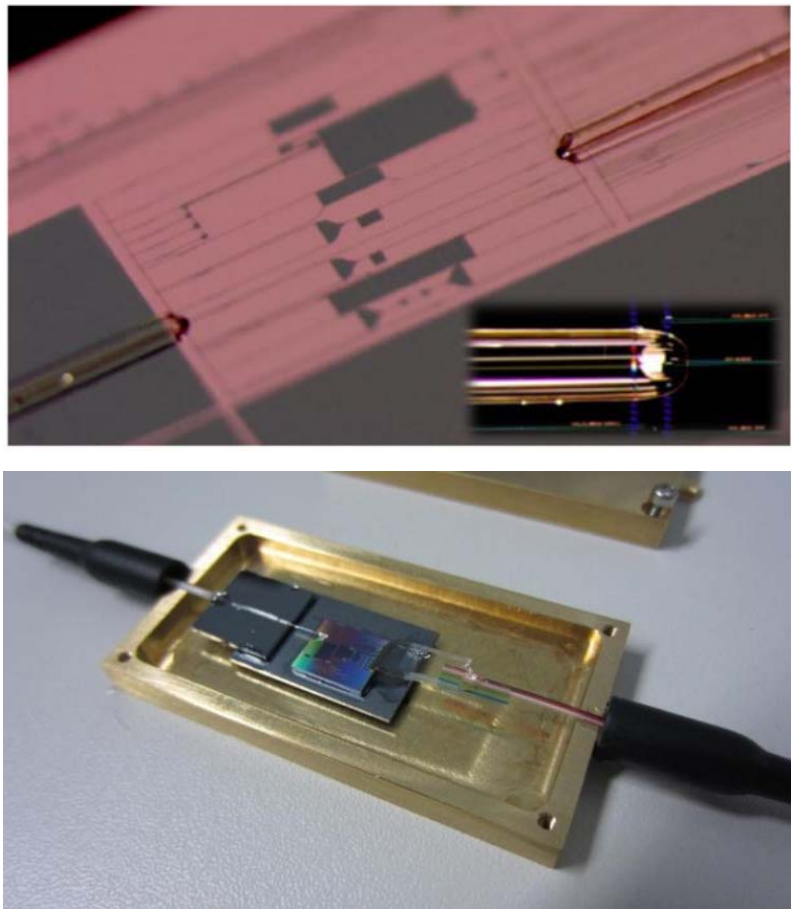

Figure 2.23 ePIXfab's packaging solution utilising angled fibre tips to reflect light down on to a grating coupler single channel (top) and multi-channel (bottom)[34].

Stéphane Bernabé et al published a paper in 2012 [35] showing the possibility of using a capping chip to secure the fibre while reflecting light downwards on to a grating coupler (Figure 2.24). A microferrule is etched in to a silicon capping chip to create a v-groove, the end of this v-groove creates a facet used to reflect light down on to a grating coupler. Using this technique, a penalty of 4dB was measured compared to active vertical alignment without index matching fluid, losses are expected to reduce to 2.4dB with the cavity between fibre and coupler filled with an index matching fluid to reduce divergence and reflection. This

approach uses semi passive alignment where the capping chip is aligned to the optical chip using computer vision.

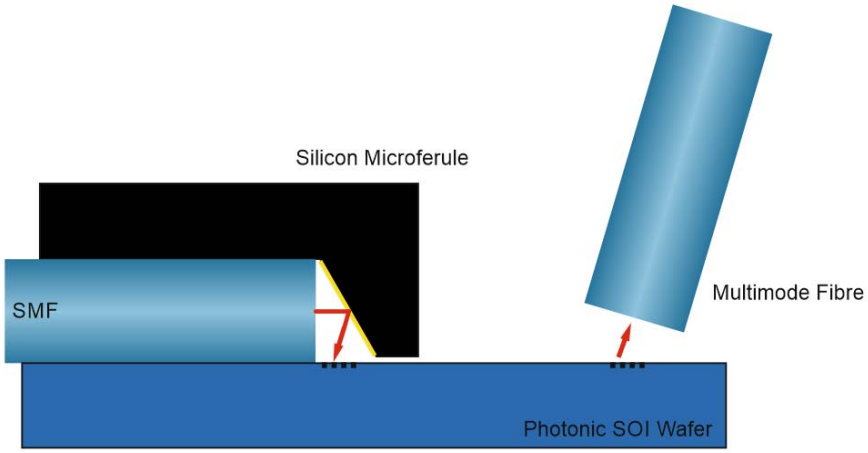

Figure 2.24 The combination of a silicon micro ferule as a mirror to reflect light down on to a PIC. Reproduced from[35].

In the same paper, they also report a semi passive butt coupled method, using lensed fibres and inverted tapers (Figure 2.25), although as the paper states, they require a polished facet and therefore the cost would be too high for large scale production.

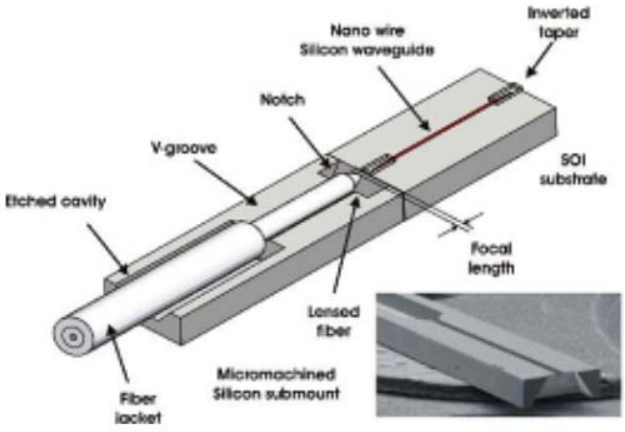

Figure 2.25 A lensed fibre supported by a v-groove semi passively aligned to a PIC using inverted tapers[35].

Another completely different in plane solution is the development of photonic wire bonding. This process uses direct write three dimensional laser lithography based on two-photon polymerisation. They show losses down to 1.7dB per link, however the write time for the wire bonds are around five minutes per bond. If the authors meet their expected target of “a few

seconds per fibre-chip photonic wire bond" and reduce coupling loss, they could have a viable high volume solution [36, 37].

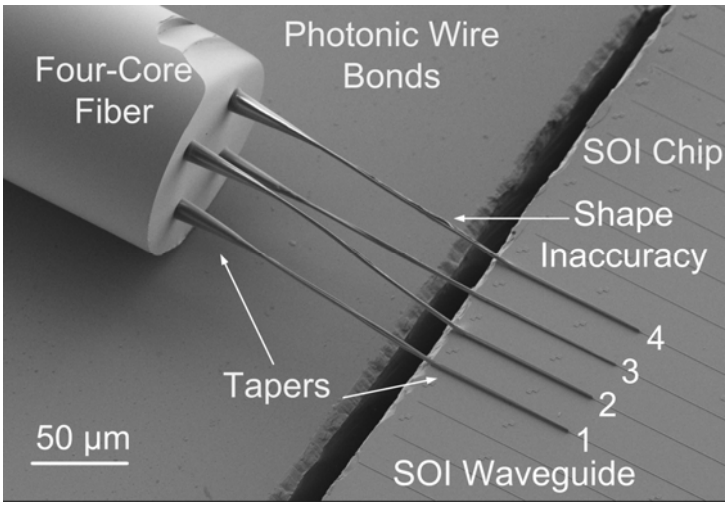

Figure 2.26 photonic wire bonds between a four core fibre and silicon photonic chip[36].

In order to produce a novel packaging concept, a large amount of inspiration has been taken from the literature displayed in this section. The advantages and disadvantages of each concept have been considered and formulated into the solution detailed in the next chapter. This concept design has been patented by the author, along with other members of the Silicon Photonics Group[38].

2.3.3: Literature Review Summary

Current trends in silicon photonic packing are showing an increase in focus on passive aligned solutions while maintaining a trend in reduced loss as shown in table 2.2.

Table 2.2 Summary of the state of the art in silicon photonics

Author	Institution	Year	Method	Added Loss (dB)	Coupling loss (dB)	Coupling Type
L. Zimmerman	ePixPack/Berlin/Fraunhofer	2008	V-groove Block	2		Active
J. Galan	Valencia	2008	V-groove/Inverted Taper	1.5	7.5	Passive
	Luxtera	2008	V-groove Block			Active
J. Galan	Valencia	2011	In Plane Fibre Block	1	7	Active
S. Bernabe	CEA LETI	2012	Capping Chip	4		Semi Passive
P. O'Brien	Tyndall/ePixPack	2013	Angled Fibre	0.2	4.5	Active
N. Lindenmann	KIT	2015	Photonic Wire Bonds		1.7	Passive
T. Barwicz	IBM	2015	V-groove/Inverted Taper		1.3	Passive

2.4: Design Process

The state of the art shows that packaging with passive alignment is a highly sought after to reduce the time take and therefore the cost of packaging silicon photonic devices. Since the start of the project similar designs have been published that show positive results but the designs created in this project will improve on them. By combining grating couplers and v-grooves, the advantages of low grating coupler alignment tolerance and passive alignment features of v-grooves can be incorporated in to a planar packaging solution. By adding self-aligned processing to create alignment plugs and holes, a design can be implemented that will allow low complexity assembly with high accuracy and throughput.

2.4.1: Solution 1

The proposed solution in Figure 2.27 is a combination of a reverse coupled grating design and passive v-groove alignment, all combined by a capping chip with a reflective coating to reflect the light from the optical fibre, into the optical chip.

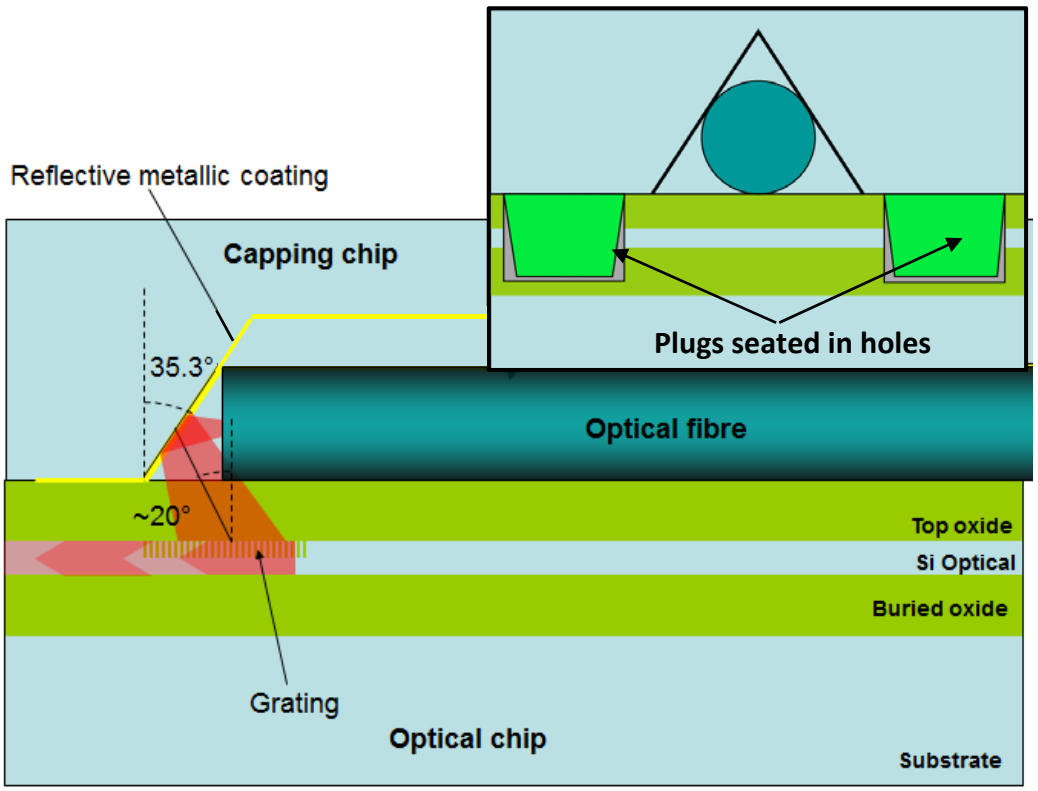

Figure 2.27 Initial design concept showing a fibre being positioned and secured by the v-groove of a capping chip which reflects light down towards the optical chip using a metal coated angled surface as a reflector which can be produced by the v-groove etching profile. (inset) shows the concept of plugs and holes being used to position the capping chip (not to scale).

This technique will allow for an in plane fibre approach which is easy to secure and will benefit from the more robust coupling produced by the grating coupler without its vertical approach. The fibre will be secured and passively aligned using a capping chip that will utilise v-grooves which are widely used for passive fibre alignment [27, 29]. Passive alignment will be accomplished with plugs in the capping chip slotting in to locating holes etched in to the device chip. Having this passive alignment feature holds a significant advantage over other packaging concepts such as the similar approach in [35]. Within this solution the side wall angle at the end of the v-groove produces a convenient mirror allowing for light to be reflected down on to the device chip surface. V-grooves are easy to produce using KOH etch techniques which will be discussed later.

2.4.2: Solution 2: Deep Device Chip Etch

Divergence

While light is propagating through a fibre the refractive index difference between the core and the cladding constrains the light to the fibre's path. Once the light leaves the fibre the beam spreads which is known as divergence [39]. For this proposed solution excessive divergence will reduce coupling efficiency due to the wider beam. With the free space propagation distance that is relatively long, the divergence of the beam may create a spot size too large for the coupler and therefore generate significant coupling loss. The initial design had a free space propagation distance of around 111µm. As can be seen in Figure 2.28, this would generate a spot size of 24µm (beam radius being half the spot diameter). This is not ideal as an optimised grating coupler would be significantly smaller than the spot and a large amount of loss would be realised. To reduce the divergence, special collimating fibres could be used allowing a smaller spot size although this would increase costs [40] and may increase misalignment penalties. A balance needs to be identified between coupler efficiency and misalignment penalty.

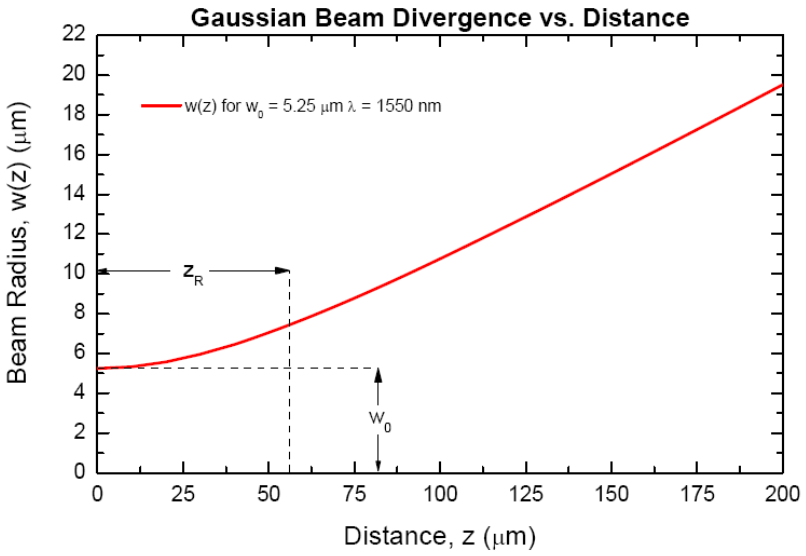

Figure 2.28 The Gaussian beam divergence vs. distance after being launched from an SMF-28 optical fibre [39].

In lieu of this a new design was proposed which involves a deep etch in the optical chip to inset the fibre (Figure 2.29), thus reducing the height and subsequent distance for the light to propagate in free space.

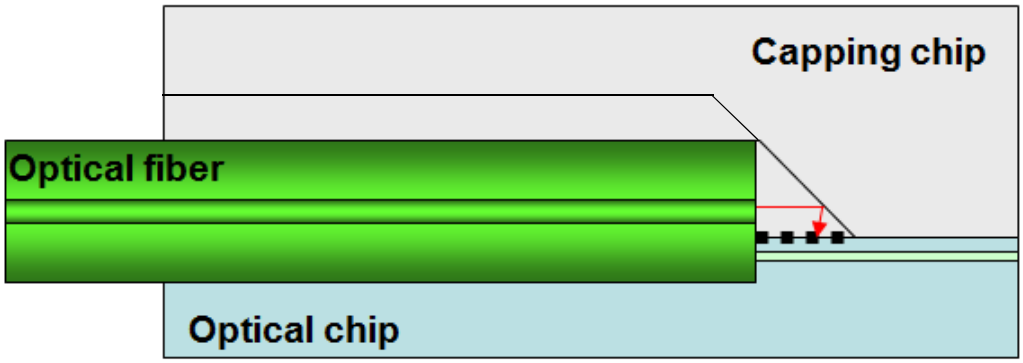

Figure 2.29 A revised concept design with the fibre embedded in the optical chip, reducing the distance from the fibre facet to the grating coupler, in turn reducing divergence.

Recessing the fibre into the optical chip by 55.5µm could reduce the propagation distance to 52µm, decreasing the spot size to 14µm. This suits the grating coupler better and requires less spot size manipulation in order to launch it in to the silicon nanowire. This does add fabrication complexity as 55µm is particularly deep and the accuracy of this etch is critical so some form of etch depth control would be required. The depth control requirement can be mitigated with a through wafer etch as described in the next section.

2.4.3: Solution 3: Through Wafer Optical Chip Etch

This solution is an evolution of the design in section 2.4.2. Etching through the wafer for the fibre cavity and alignment holes (Figure 2.30) creates a number of advantages. The most significant being during assembly of the two parts, the holes will allow vision of the capping chip, this will permit accurate alignment of the plugs to the holes and will reduce the complexity of assembly (Figure 2.31). Having access to the fibre cavity, post assembly also presents the opportunity to insert fibres after bonding of the samples, permitting wafer scale assembly of the devices through either pick-and-place or whole wafer bonding. Besides the added complexity this solution requires the v-groove to control the height of the fibre, this means that the required accuracy of the v-groove is much higher and a greater care in the production of them is necessary.

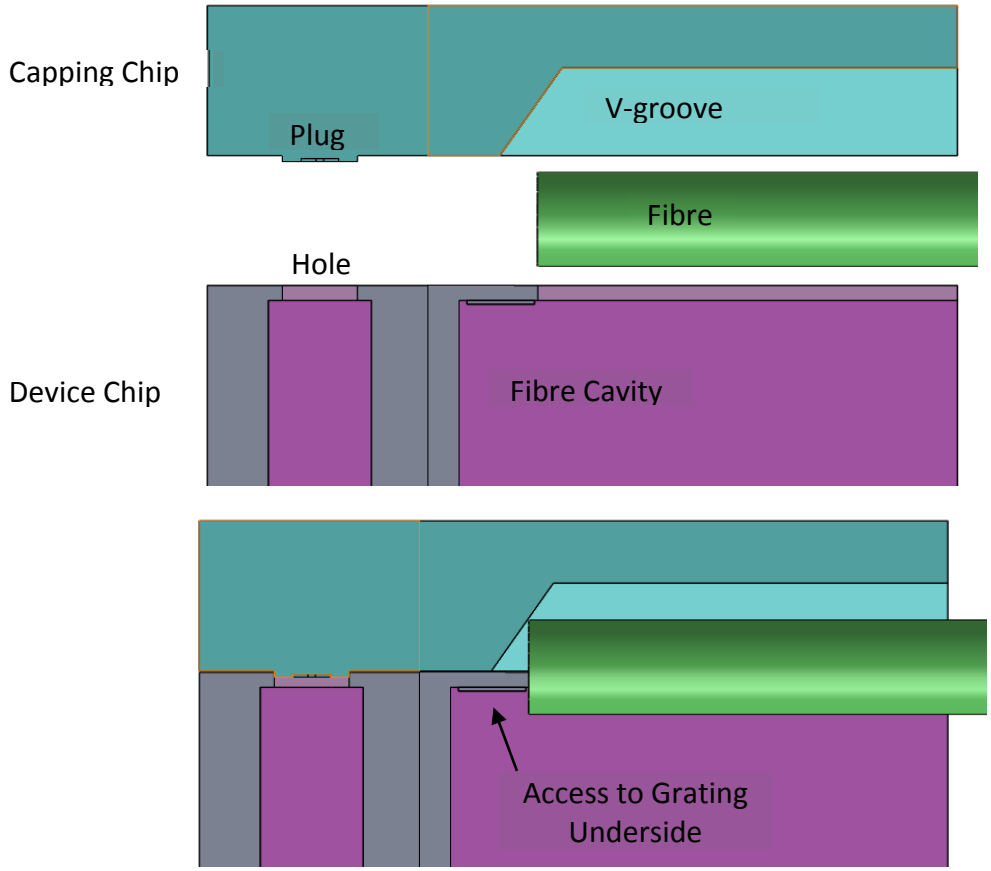

Figure 2.30 A cross section diagram of the packaging design in an exploded view (top) and assembled (bottom)

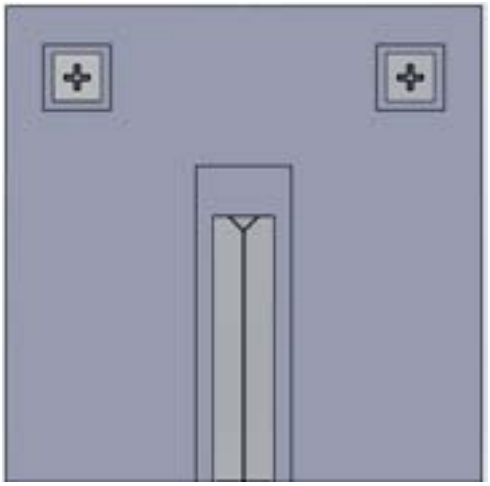

Figure 2.31 Shows the packaging design with a through wafer process allowing vision of the capping chip through the device chip which makes alignment easier during assembly. The fibre can also be inserted after chip assembly.

The initially designed process flow of both parts is shown in appendix 1, it is a flow chart that describes every step required to produce the design. Each of these steps will be discussed further, later in the thesis. In order to complete the design every step must be precisely aligned to minimise displacement losses. Every stage of the process will have tolerances that will all eventually add up and must be minimised where possible. Physical tolerances that will affect this design are detailed in Table 2.3.

Table 2.3 The predicted misalignment causes which could affect coupling accuracy and their potential remedies.

Misalignment Cause	Tolerance	Minimisation Method
Fibre Diameter[41]	±0.7µm	None
Cladding Core Concentricity	±0.5µm	None
Trench Depth	Unknown (Not applicable with through wafer etch)	Accurate etch depth calibration
V-groove Depth	Addressed in this work	Accurate masking
V-groove Lattice orientation	±1° (to wafer flat)	Lattice orientation test

The processes detailed in the next chapter will confront these issues and develop methods of improving these tolerances where possible.

Chapter 3: Tools and Equipment

This chapter will give a general scientific overview of the different tools and equipment used to complete the project. It will not describe the recipes used as specifics will be discussed later. Instead, this chapter will grant a familiarisation of such tools when detailed processes are discussed in later sections.

3.1: Cleanroom Equipment

3.1.1: Mask Design

Before devices can be fabricated mask designs are required. These designs can be created using a two dimensional vector drawing tool called L-Edit. Figure 3.1 shows an example of a cell which encompasses the complete packaging design, each colour corresponds to an individual layer or fabrication step. The files created by L-Edit are either sent to a company who create photolithography masks, or they can be directly written using e-beam. Both of these methods will be discussed further in section 3.1.2: Lithography.

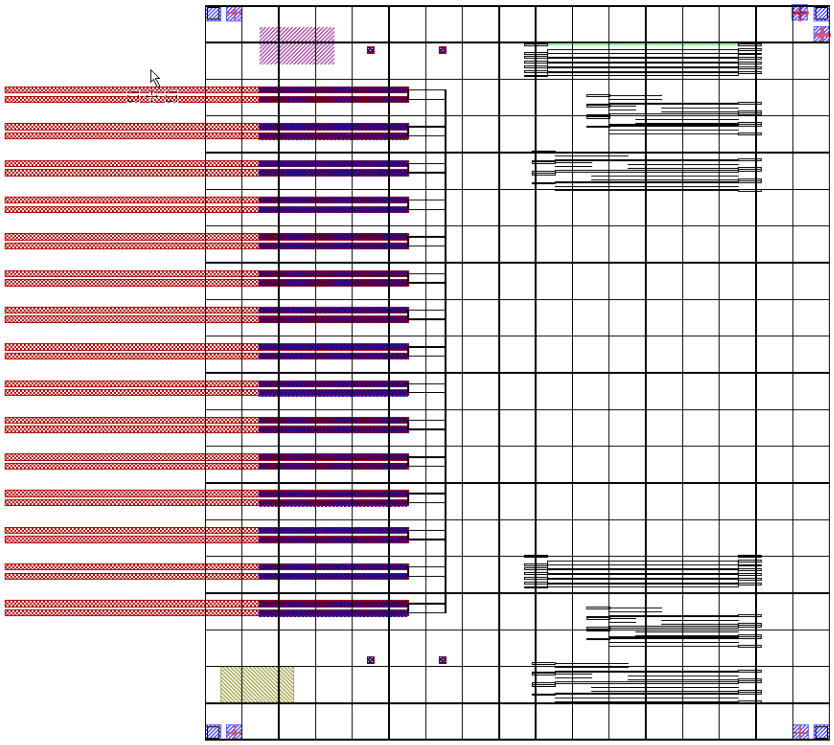

Figure 3.1 The complete mask design used for this project. Each colour corresponds to an individual layer or fabrication step.

3.1.2: Lithography

Lithography is a process wherein a pattern is defined in a soft mask made up of photosensitive or electron beam (e-beam) sensitive material known as photoresist or e-beam resist respectively. There are a number of ways the resist pattern can be defined, but within this project the process was performed by two methods; e-beam lithography and optical photolithography. Both of these processes alter the chemical composition of the resist, either making it more susceptible to development (positive), or less susceptible (negative). To clarify, when using negative resist, the areas that are exposed remain after development,

whereas when using positive resist, the areas that are exposed are etched away during development. Development is the process where the substrate is placed in a chemical solution which etches away the desired areas[43].

Lithography usually takes place in a “yellow room” which is lit with yellow light, void of any UV contamination which would expose resist prematurely.

E-beam Lithography

The E-beam tool is used to define features that can be smaller than 10nm and position them with nanometre accuracy. It uses an electron beam to chemically change a specially formulated resist. Depending on the resist type, this either makes it more resistant or more susceptible to development chemicals. This difference allows for positive or negative definition. As this writing process is performed by an electron beam, the feature sizes are limited to the size of the beam but the smaller the beam, the longer a pattern takes to write. The Jeol JBX9300 in the SNC has course fine and ultrafine beam conditions which are; 100, 20 and 5nm spot sizes respectively. E-beam photoresists are usually optimised for thin layers and for very high resolution structures.[43] However in this project we have also developed the use of a thick resist layer, enabling greater etch depths to be achieved. The most demanding features within this project with respect to feature size are grating couplers, they have critical dimensions less than 100nm and this will require high resolution lithography. The best tool for this within the Southampton clean room is the e-beam. Positional accuracy between lithography steps is also a priority and as the e-beams alignment tolerance is in the order or nanometres it is an ideal tool.

Contact Lithography

Contact lithography uses a flood of ultra-violet light in order to expose the photoresist (Figure 3.2). In order to create the desired pattern, the light is blocked in areas by a mask. The masks used for this project were made from glass (to allow UV transmission) with a pattern of chrome on the surface to prevent exposure of the desired areas. A mask aligner uses a vacuum to hold a mask which substrates can be positioned under. Cameras are present on both the top side and underside of the substrate and are used to align the substrate to the mask if previous alignment marks are present. When the substrate is aligned to the mask, the tool exposes the mask to UV light, chemically changing the resist.

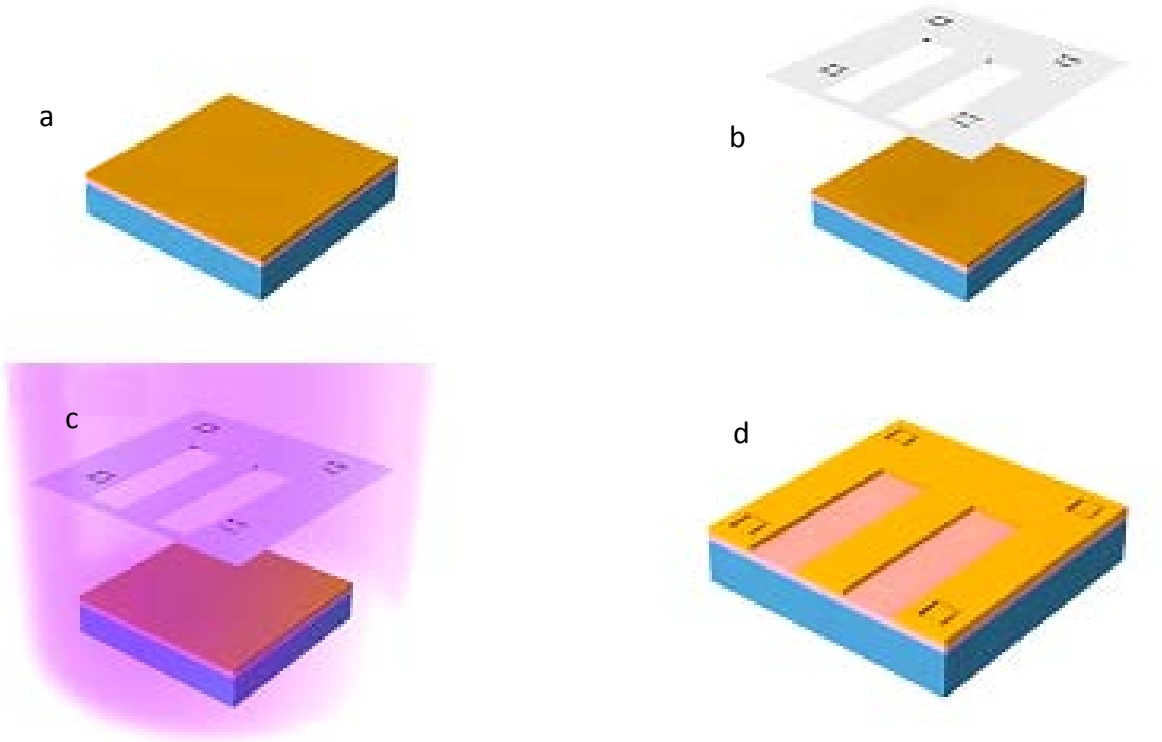

Figure 3.2 A diagram of the photolithography process a) deposition of resist. b) Positioning of chrome mask. c) Exposure of UV light. d) Development to form features.

Spinning, Baking, and development

Each resist has an optimised process to ensure the required resolution, sidewall angle and thickness. The thickness is controlled by the viscosity of the resist combined with the speed at which it is spun. The spinner uses a vacuum plate to secure the wafer and spins at speeds up to 6000 revolutions per minute. Once the resist is coated, the substrate is placed on a hot plate. The high temperature, up to a hundred degrees or more, cures the resist so that it is no longer a sticky liquid. Some resists require a post exposure bake to further chemically activate the material, this can be required for a number of reasons; in chemically amplified resists it is required to complete the photoreaction acquired during exposure. Within this project, post exposure baking was required to crosslink the negative resists used. Basically, this means that the chemical change initiated during exposure is completed when exposed to high temperature.

The development can either be accomplished by submersion in a bath of developing chemical, or on an automated spinner, similar to the resist spinner. This developer removes the resist that has not been cross linked with a very high selectivity to the cross linked material. Once

development is complete, the wafer is rinsed with DI water and dried. Inspection is then required to confirm correct exposure and development.

3.1.3: Etching

Etching is the process wherein material is removed in order to create three dimensional features, or strip away unwanted layers. During the course of this project two main types of etching were used: Wet etching uses acids or alkali in liquid forms to chemically remove material from the surface of a wafer. Dry etching is the term for using plasma tools to both chemically and physically etch material from a substrate. Both of these techniques will be discussed further in this section.

Reactive Ion Etch

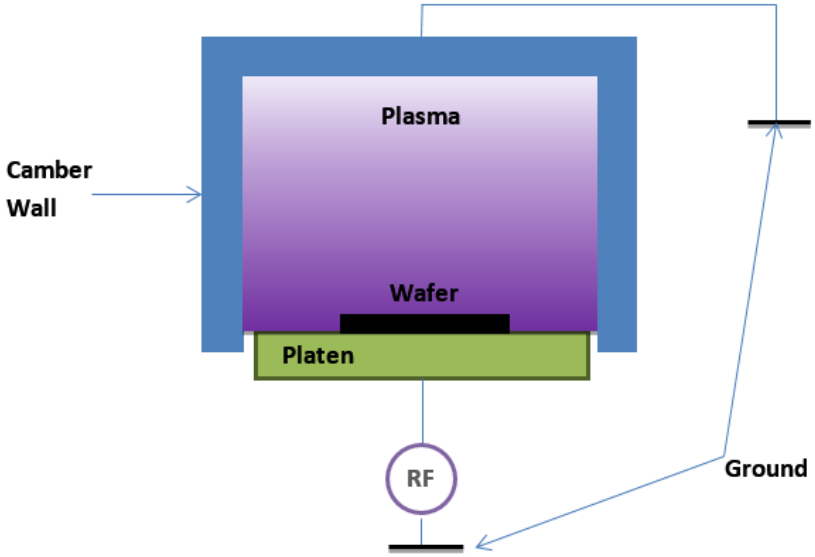

Figure 3.3 A schematic diagram of a reactive ion etcher.

Reactive Ion etching (RIE) is a process where a material is etched by high energy ions within a plasma (Figure 3.3). This plasma is created by subjecting the wafer platen to a large RF electric field. The oscillating field ionises gas molecules within the chamber by stripping them of electrons. Whilst within the RF field these electrons move within the chamber according to their polarity, colliding with the chamber wall and the platen. Those hitting the chamber walls are absorbed as the chamber is grounded, whilst those striking the platen build up a negative charge as the platen is isolated. The relatively large, positively charged ions are not affected significantly by the RF electric field as they are heavy and slow. Once the platen is biased from

the accumulation of electrons, the positively charged ions become attracted to it and start to accelerate towards it[43].

The systems used to perform an etch can be broken down in to two types. There is a highly directional physical etch, known as sputtering and a chemical etch where the ions created from the gasses used, chemically react with the surface to be etched. As well as etching, depending on the conditions created within the chamber, passivation of polymers can be obtained, allowing further control of the etch process[44].

The RF power, vacuum pressure, temperature and gasses within the plasma are carefully controlled in order to create the desired reaction with the target. This recipe is sensitive to many things including; the material to be etched, the mask material, the ratio of exposed area to resist and the total size of the wafer, therefore etch processes must be optimised for these scenarios.

Inductively Coupled Plasma Reactive Ion Etch (ICPRIE/ICP)

The inductively coupled plasma (ICP) etch process is similar to the standard RIE however a large inductor surrounds the chamber (Figure 3.4 left). Subjecting the inductor to a separate RF electric field increases the density of the plasma. This typically increases the etch rate while maintaining resist selectivity by shielding the plasma from the capacitive coupling of the RF source which creates higher energy ions. Without these, ion bombardment is reduced which is usually the main component of resist etch rate[45].

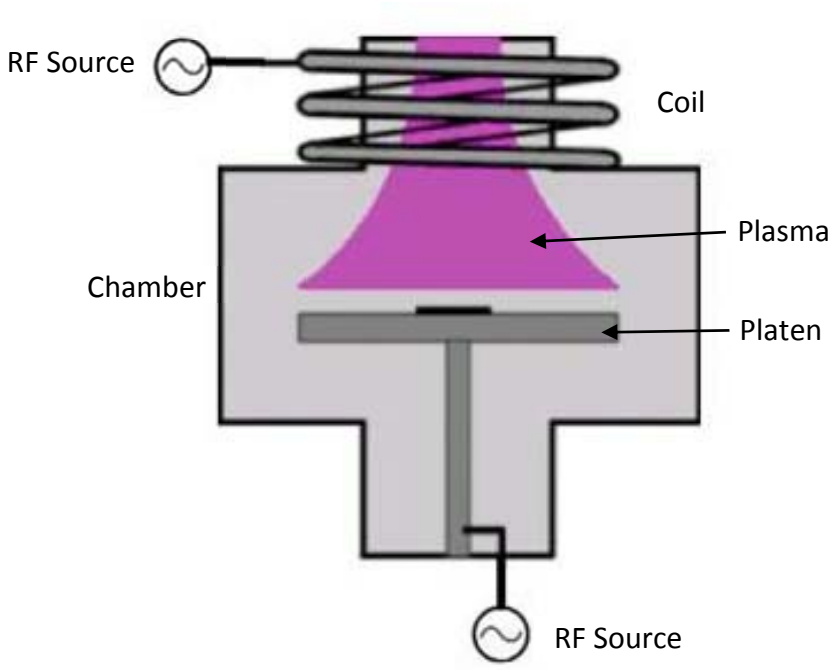

Figure 3.4 A diagram of an ICPRIE (left) showing a similar construction to a standard RIE but with a large inductive coil encapsulating the chamber.

Deep Reactive Ion Etcher (DRIE)

The DRIE is an ICPRIE which is used to dry etch deep features in silicon. It achieves this by utilising a 3 stage etch process, and switching recipes periodically. The first stage of the process is a partially anisotropic etch step, the second is a passivation step, depositing polymer everywhere, finally a highly anisotropic ion bombardment removes the polymer deposited on the horizontal surfaces. The next time the isotropic etch starts, the reactants will only be exposed to the area without polymer. Due to the inherent verticality of RIE etching, the passivation layer is etched less on the side walls allowing for a vertical etch profile, albeit with slight scalloping (Figure 3.5) [44]. This process is patented and called Bosch process but is also known as deep silicon etching (DSE) or DRIE. This is used to produce very deep, vertical etch profiles which can penetrate all the way through a silicon wafer

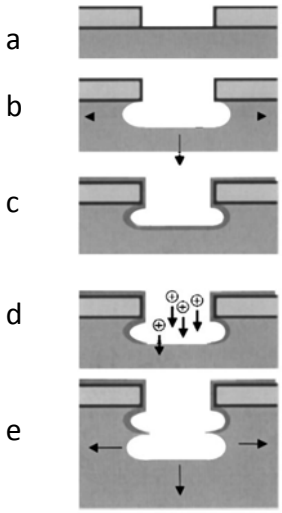

Figure 3.5 A diagram showing each phase of the DRIE etch process starting with a masked substrate (a) then submitted to an isotropic etch(b), followed by polymer passivation (c), anisotropic ion bombardment removes the polymer from the horizontal surfaces (d) which allows access for the isotropic etch to start again(e)[46].

Wet Etch

A number of wet etches are used within this project, mostly for the stripping of masking layers and cleaning, as well as the production of the V-grooves using a KOH etch. The basic principal of wet etching is straightforward: the wafers, having had a mask pattern produced, are then transferred in to a tank of the etchant (Figure 3.6). While submerged, chemical reactions take place at the exposed surface of the layer to be etched. The wafers are then left for the desired time based on the etch rate, and are then removed and rinsed. Some etch tanks have heaters to control etch rate, bubblers for agitation, and drip feeds to control chemical concentration.

Figure 3.6 A typical wet bench with four etch baths containing (from left to right) orthophosphoric (H_3PO_4) acid, RCA tanks one and two, and a KOH tank. There is also a rinse dump tank toward the front.

The etching mechanism is chemical and there are a vast range of chemical reactions for different materials. The reaction is either slow at the surface, which limits the etch rate, or fast at the surface and the etch rate is limited by transportation of etchant to the area and the transport of by-products away from it. Transport

dependant reactions can be boosted by agitation.

Many of the acids or alkalis that are used for wet etching are extremely dangerous and special wet benches and personal protection equipment (PPE) is required to protect users.

POTASSIUM HYDROXIDE (KOH) SILICON ETCH

KOH etching is most commonly used for etching silicon. It is an anisotropic etch that has a very high selectivity to the different crystal planes in silicon due to their different bond energies and more dangling bonds being available on the planes with a higher etch rate[47]. This means that depending on the crystallographic orientation of a silicon wafer, different structures will be created when areas of the surface are masked off[48]. (100) oriented wafers, with rectangular openings in the masking material will create v-groove structures that have 35.3° sidewalls, whereas (110) oriented wafers will produce near vertical sidewalls[48]. These structures are generated due to the diamond crystal structure and have a wide range of uses.

Table 3.1 shows a comparison between etch rates of different materials when etched with KOH. When choosing a masking material, selectivity is important and this table shows that silicon nitride (Si_3N_4) is an ideal masking material as the etch rate is less than an angstrom per minute which is equivalent to a >10000:1 selectivity to (100) silicon. Silicon dioxide (SiO_2) still yields a good selectivity of 1200:1, under some circumstances this may be desirable one of which will be discussed later in the thesis.

Table 3.1 The etch rates and selectivity of silicon crystal planes and common mask layers

Etchant	Etch rate ratio		Etch rate (absolute)			Advantages (+)
	(100)/(111)	(110)/(111)	(100)	Si_3N_4	SiO_2	Disadvantages (-)
KOH	300	600	1.4 um/min	<1 Å/min	12 Å/min	(-) Metal ion containing
(44%, 85°C)						(+) Strongly anisotropic

Although KOH is surface reaction dependant, one of the products of the KOH reaction with silicon is hydrogen. This coalesces into bubbles which block the transportation of chemicals at the surface completely. Agitation in the form of nitrogen bubbles forces the hydrogen bubbles to detach and allows for an evenly etched surface. [44]

HYDROFLUORIC ACID (HF) SIO_2 ETCH

When silicon dioxide is stripped or wet etched HF is used, usually buffered with ammonia fluoride which is added to increase and maintain a constant etch rate, while increasing the pH-value which improves resist stability. A HF concentration of either seven to one or twenty to one ratio (ammonia fluoride to HF) is typical. It has a very high selectivity to silicon, in some cases not etching silicon at all. Some metals can also be etched with HF such as titanium which can etch at over a micron per minute [49].

HOT PHOSPHORIC/ORTHOPHOSPHORIC ACID (H_3PO_4) SI_3N_4 ETCH

Orthophosphoric acid is used to strip silicon nitride as it has a relatively good selectivity to silicon of around 16:1. In order to achieve acceptable etch rates the phosphoric acid must be diluted with water and raised to boiling point which our experiments showed to be around 157°. This is significant because the boiling process expels water, reducing etch rate. Therefore a DI water drip is required to maintain steady etch rates and selectivity [50].

WAFER CLEANING

Between processing steps wafer cleaning is often required which can be completed in the wet room. There are two cleaning processes available within the SNC: Firstly, the RCA clean which is an acronym for the Radio Corporation of America and is named after the place where it was developed. The RCA clean consists of a three stage chemical clean which includes an organic/particle clean using ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) in solution with deionised water, followed by an option HF dip and finished with an ionic clean in a solution of water, hydrochloric acid (HCl) and H_2O_2. The first and last steps typically last around 10 minutes and are heated to a temperature of around 80°C with thorough rinsing between each step[51]. The second process available is FNA or Fuming Nitric Acid (HNO_3) where two tanks contain the same 90% HNO_3 solution; one is used for stripping resist coatings and the second is used as a clean step for removing organics from the surface[52].

3.1.4: Chemical Vapour Deposition

Chemical vapour deposition is a process of depositing layers of material on a wafer surface. These layers can be used as a hard mask, waveguide cladding or for surface protection. The deposition techniques used within this project are discussed in this section. The temperatures allowed for deposition depends on the stage of processing that has been reached. High temperature deposition, greater than 450°C, is undesirable after active devices have been made as aluminium metallisation -which is commonly used for contacts- begins to degrade beyond this point. Beyond 600°C copper will diffuse and effect transistor characteristics if CMOS components are present and as temperatures rise further more metals with critical roles are affected [53] Beyond 800°C dopants within active devices begin to diffuse reducing performance[43].

Low Pressure Chemical Vapour Deposition (LPCVD)

LPCVD uses high temperature furnaces (**Error! Reference source not found.**), typically at temperatures of 700 to 1000°C, to deposit thin films on wafer substrates. Gasses are pumped into the furnaces and the high temperatures causes chemical reactions at the surface of the substrate. These chemical reactions result in the deposition of layers, the composition of which is dictated by the gas recipe, and the temperature and pressure profiles.

The rate of deposition is slow compared to other techniques, although multiple wafers can be processed at once and the quality of the layer produced is usually better than Plasma enhanced chemical vapour deposition which is discussed in the next section.

Plasma Enhanced Chemical Vapour Deposition (PECVD)

PECVD uses a similar process to RIE in order to perform deposition of layers on to a wafer surface. Like the RIE process, a plasma is struck using an RF electrical field, and the plasma is used to cause molecular disassociation of the gasses, thus generating neutral species. These neutral species react with the surface of the wafer which is heated to typically 300°C, aiding the reaction. This plasma process allows much lower temperatures than LPCVD permitting back end processing[44]. **Error! Reference source not found.** shows the Oxford Instruments Plasmalab System 100 available in the SNC.

3.1.5: Plasma Ashing

Somewhat similar to the RIE, a plasm asher uses high energy ions to remove materials from a wafer, the main difference being that there is no directional etch within the chamber. This isotropy is principally due to the chamber being barrel shaped (Figure 3.7.). Ashers use high energy O_2 plasmas to remove remaining photoresist after previous etch processes are completed. [54]

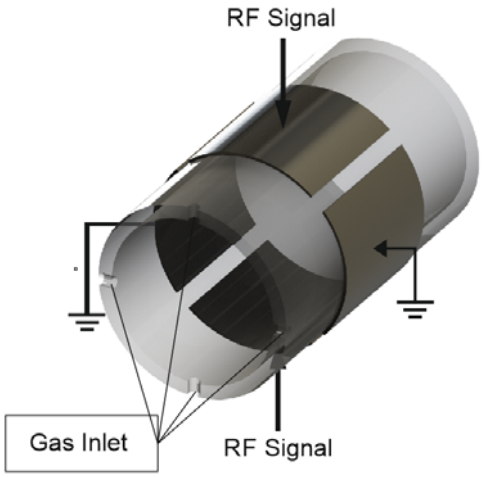

Figure 3.7 A schematic diagram of a plasma asher.

3.1.6: Metrology

Ellipsometer

When etching, determining the etched depth is critical for both creating accurate structures and the control of etch rates when defining processes. An ellipsometer uses a linearly polarised light source reflected from the surface of a sample to measure the thickness, composition, crystallinity, roughness, doping concentration and other optical properties that can be identified through a change in optical response. This response is based on how the reflection affects the polarisation and amplitude of the light (Figure 3.8). A model is defined using known material parameters, and the software package CompleteEASE is used to fit this model to the data collected by the ellipsometer by adjusting the thickness variable in the model. When an accurate fit is acquired, the depth of the material layers within the sample is realised.

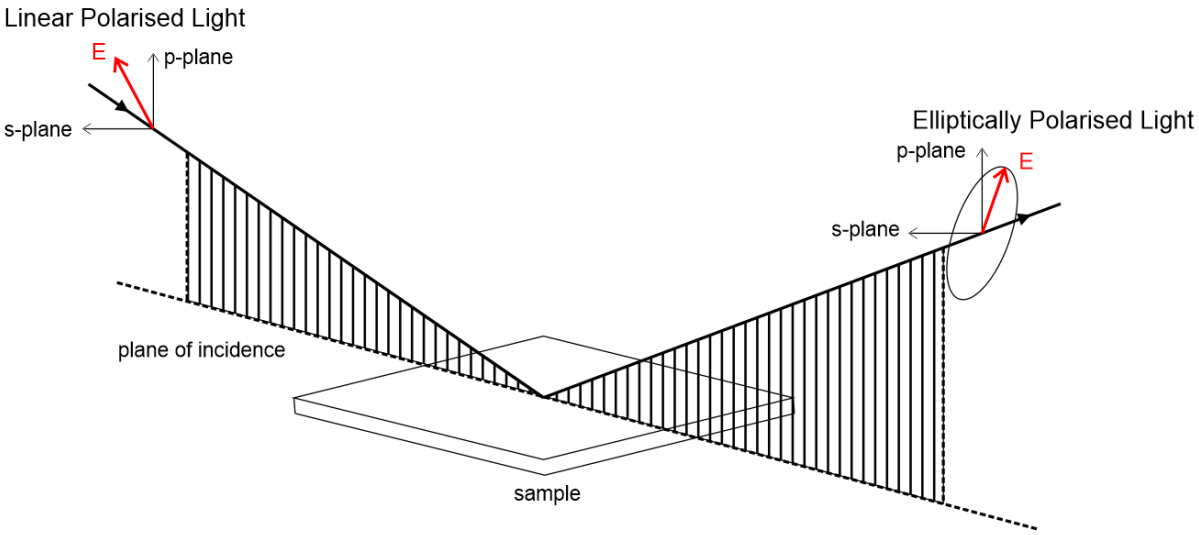

Figure 3.8 A diagram depicting a sample ellipsometry measurement. Reproduced from [55]

Profilometer

A profilometer is a simple yet versatile tool that drags a stylus across the surface of the sample being measured. It can then display accurate information on the surface topology with a maximum resolution of 0.08Å over a step height of 134µm[56] although this accuracy was never required for this project. Once resist is stripped it can describe accurate etch depths, and when used in combination with the ellipsometer it can identify the etch rate of a resist layer as the ellipsometer will allow calculation of the etch depth of the layer being etched, the difference of this compared to the profile will show the thickness of the remaining resist. It can also describe surface roughness where its accuracy increases to 0.004Å when the surface topology is less that ±3.2µm, and sidewall angle although this is limited by the taper angle of the stylus tip, where any side wall angles greater than the stylus taper angle will not be measured. Undercut is also hidden from a profilometer.

Optical Microscope:

Visual inspection is often required during processing, and the quality of each step is often dictated by the preceding step. Maintaining cleanliness and good process quality is paramount. During the development of resist layers, features are often checked under the microscope to assure proper clearing.

Scanning Electron Microscope (SEM)

When features are too small to image with an optical microscope, an SEM can be used. An SEM directs a beam of electrons at a sample and detects the interactions between the

electrons and the specimen. These interactions can then be formed into an image via a computer. Non-conductive surfaces are likely to charge when the electron beam is directed at them, which blurs the imaging process. Coating specimens in a very thin layer of gold (or other conducting material) will prevent charging but in many cases ruins the sample, limiting the scenarios where an SEM can be used[57]. During this project, SEM images are used to characterise etch profiles, cleaving a sample in two and looking at a cross section of an etch is a typical and very useful application for the SEM.

3.2: Laboratory equipment

When aligning to grating couplers, sub-micron accuracy is required in order to determine the maximum efficiency. A precise and controlled laboratory environment is required to remove any environmental vibrations and temperature fluctuations as well as allowing high precision positioning of fibres. This section will discuss the equipment used in the laboratory, focusing on the testing setups built and used.

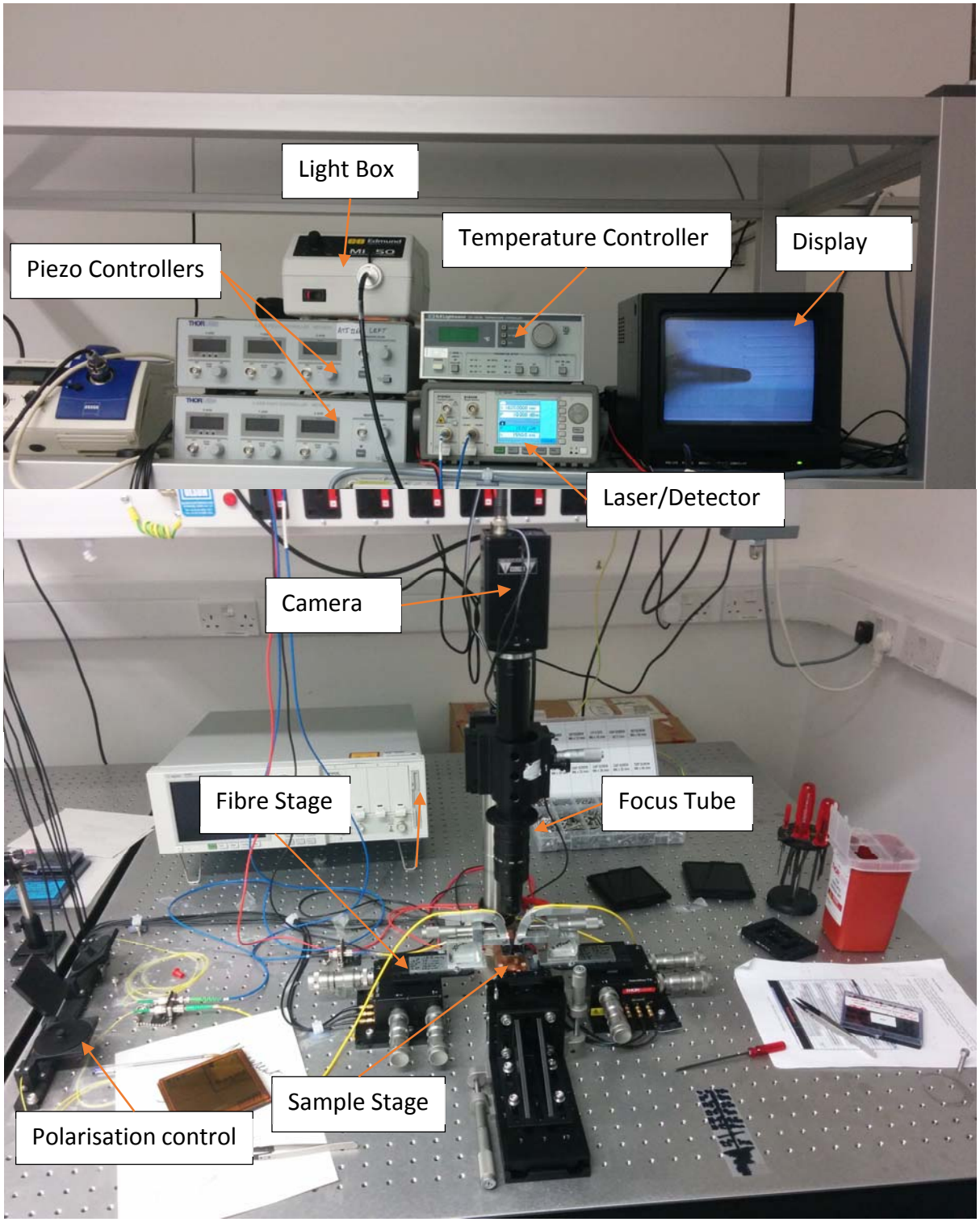

Figure 3.9 The setup for measuring passive grating coupler based devices.

Figure 3.9 shows the grating coupler characterisation bench the function of which will be discussed in this chapter.

3.2.1: Fibre Holders

As grating couplers need a near vertical fibre approach angle, fibre holders are used that support fibres above samples under test. During the project, novel fibre holders were created in order to make the laboratory test setups more flexible. Supporting fibres for vertical coupling can be difficult due to the presence of a camera and general stability issues.

Prior to the author's involvement in the group, rudimentary fibre holders had been used within the labs, ranging from strips of aluminium bent to the desired angle, to more complex angle controlled machined aluminium devices (Figure 3.10). These did not meet the requirements for the project due to limitations in fibre approach angle, and so, work was carried out to improve on the design, not just to make allowances for this project, but to try and make them as useful as possible.

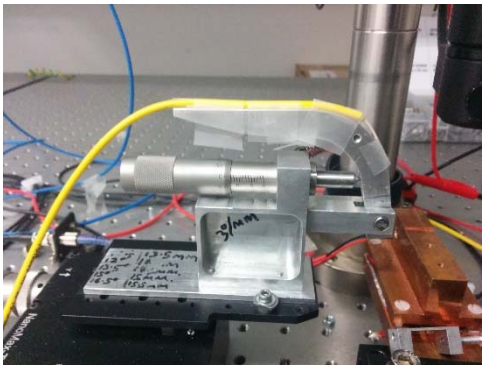

Figure 3.10 An example of the fibre holders used prior to the authors redesign.

Having developed a number of designs that can potentially benefit everyone working with vertical coupling, the author has requested to file for a patent and is investigating the potential for selling the holder as a product.

Basic Fibre Coupler Model

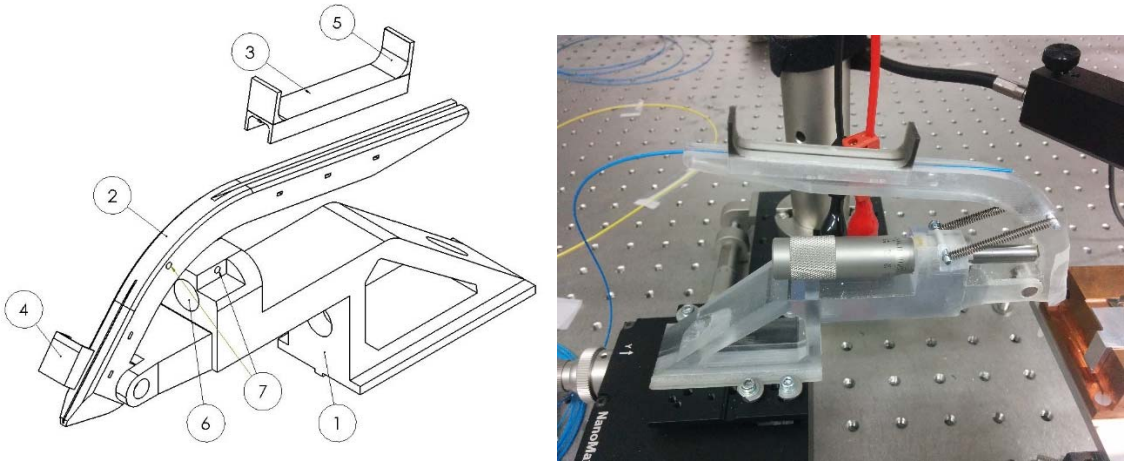

Figure 3.11 (Left) a fibre holder base (1) with a basic fibre arm (2) and two caps, one at the front and one on top (3-4) which clip to the arm, securing the fibre. Supports on the cap (5) are used for holding an inclinometer which is used to measure the angle of the fibre. The angle is controlled by a micrometre inserted in to the hole marked (6). (7) Shows screw holes that secure a spring that stabilises the arm. (Right) is a 3D printed prototype used to trial the design.

Initial designs were made to improve the usability while adding functionality (Figure 3.11).

Tape was being used in previous versions to secure the fibre to the holder. In order to make cleaning or changing the fibre easier, clips were designed to secure the fibre to the arm in this case. The implementation of a stand is demonstrated in Figure 3.12, it allows the arm to stay upright when removed from the stages, thus making it easier to change fibres without risk of the arm falling onto the fibre and damaging it. The bend in the arm was made shallower to allow for a larger range of angles, thus solving the issue for this project.

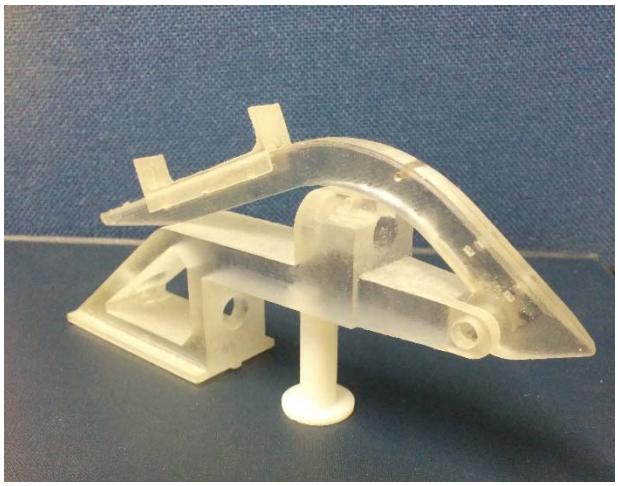

Figure 3.12 A 3D printed fibre arm prototype with a 3D printed stand to keep it level when not secured to a movement stage.

Often when testing active devices, large PCBs are included and the previous fibre holders did not have sufficient reach to access grating couplers. The author has addressed this by extending the length between the fibre tip and the base.

Accurate angle positioning is vital for grating coupler measurement. In order to easily measure the fibre approach angle, the clip used for securing the fibre to the arm has added supports for a digital inclinometer, this can display an accurate angular measurement relative to the sample under test.

Many prototypes have been made out of a transparent resin called VeroClear (Figure 3.12) using an Objet500 3D printer. For the most part this is ideal, however the material itself is quite brittle and the support material is difficult to remove, creating debris which is not ideal for laboratory testing. Upon further use it was discovered that the holders were susceptible to drift. The cause of this is unknown and so milled aluminium versions were commissioned to rule out the possibility that it was a problem with the 3D printed material (Figure 3.13). Tests are ongoing.

Figure 3.13 machined aluminium fibre arms.

Modular Model of the Fibre Coupler

Further designs have been produced for a version which includes polarization control which is facilitated by rotating the fibre, therefore removing the need for extra polarization controllers, provided PM fibres are used. The added complexity of this design is exacerbated by the requirement for it to be compact and easy to use. Figure 3.14 shows one of the many

designs implemented to test the concept. It is still undecided whether it would be better to create a permanent ferule attached to the fibre as securing the fibre can be difficult.

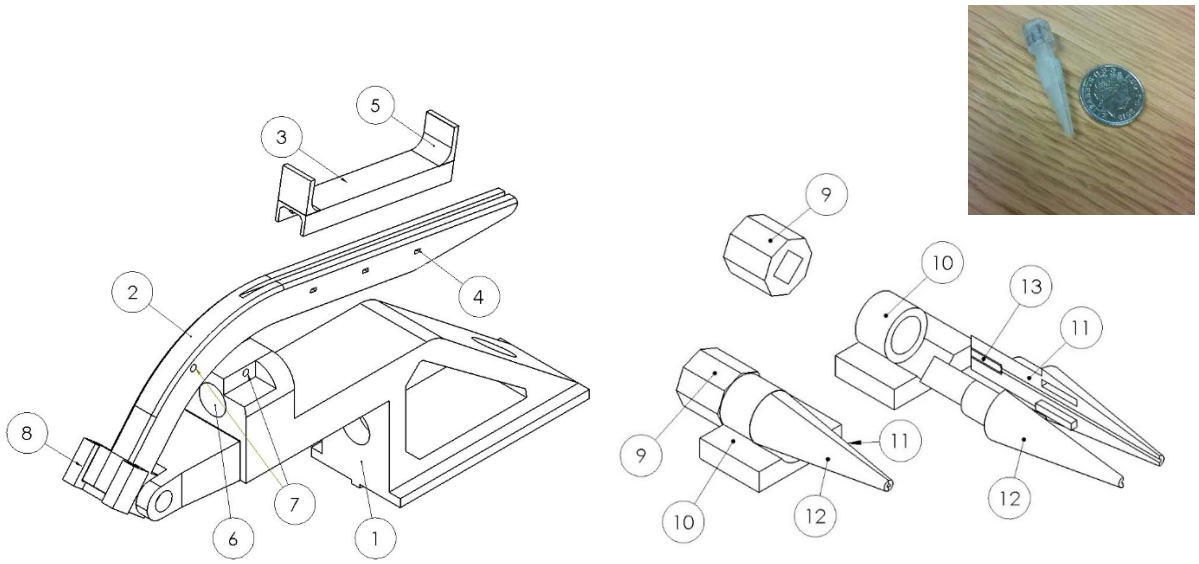

Figure 3.14 (left) a fibre holder base (1) with a modular fibre arm (2) and cap (3) which clips to the arm (4), securing the fibre. Supports on the cap (5) are used for holding an inclinometer which is used to measure the angle of the fibre. The angle is controlled by a micrometre inserted in to the hole marked (6). (7) Shows screw holes that secure a spring that stabilises the arm. (8) is the receptacle that allows different modules to slide in and out when needed. (right) a polarisation rotating fibre holder that is rotated by twisting a handle (9) and is supported by the insert (10) which slots in to (8), (11-12) sandwich the fibre and (13) is a rubber grip to ensure the fibre does not slip on rotation. (inset) a 3D printed prototype of the fibre rotator.

Another consideration is producing a holder for fibre arrays, which may also be required for testing multi fibre experiments.

All of these concepts can be combined in a modular fashion, so if different fibre conditions are required on the same test set up, they can be swapped in and out with ease.

3.2.2: Fibre Stages

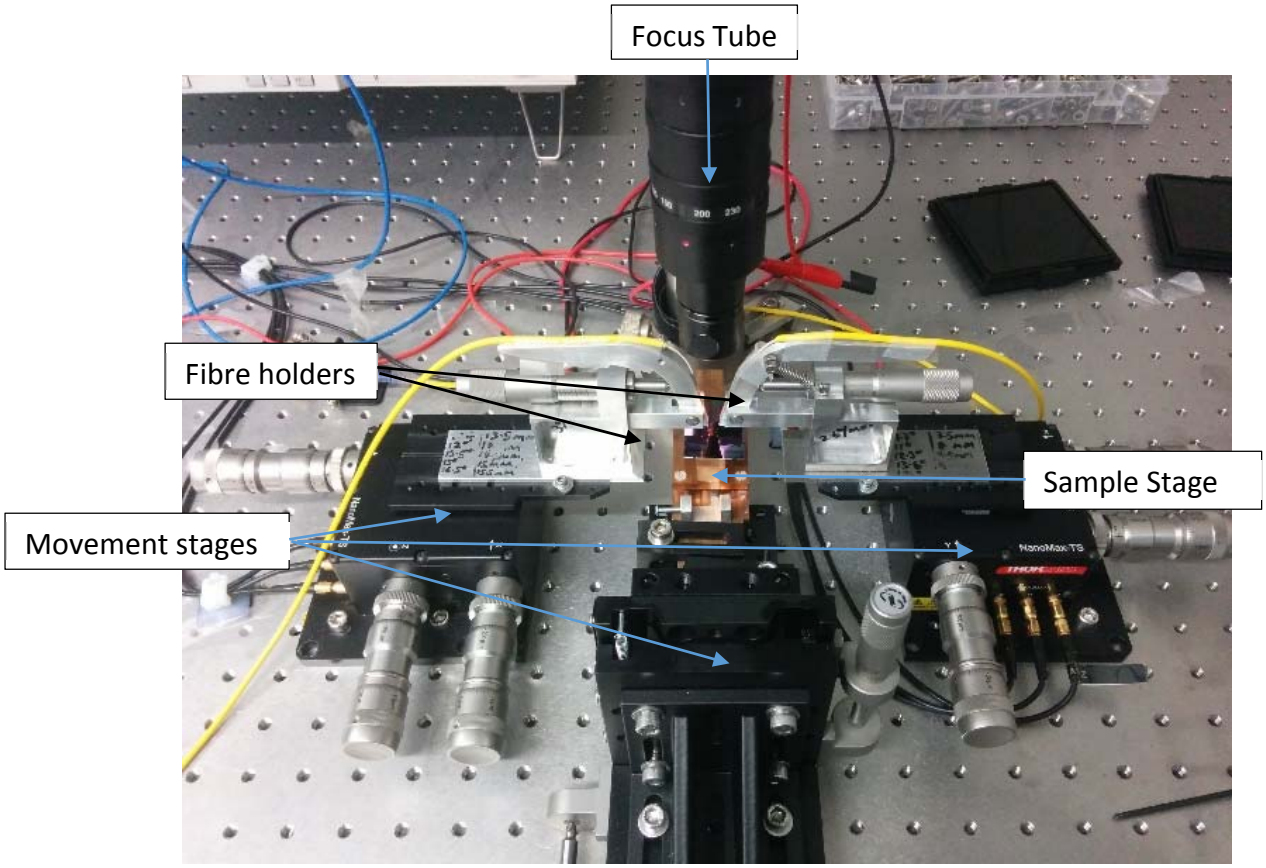

Figure 3.15 Close up of the grating coupler measurement setup showing two movement stages with fibre holders, the sample stage and the end of the focus tube.

Once the fibre is secured, it requires translation in the x, y and z planes in order to be positioned above a grating coupler. Translation stages are used which have highly accurate micrometre controlled movement. These stages also have piezo electric controllers which allow nanometre precision when aligning them. This allows highly precise alignment with a resolution of 20nm to grating couplers, permitting the best coupling efficiency possible.

3.2.3: Sample stage

The sample stage is made up of an aluminium base, a Peltier device for temperature control, a thermocouple and a solid copper sample holder (Figure 3.16). The base and the sample holder sandwich the Peltier between them with thermal paste to assure good thermal transfer. The assembly is held together with plastic bolts to avoid thermal leakage between the two pieces. The copper allows efficient thermal transfer to the sample being tested and the thermocouple is used to feedback temperature readings to a temperature controller

which in turn adjusts the voltage across the Peltier to maintain a steady temperature. This assembly is bolted to a two dimensional stage which is used for moving the sample during testing. Thermal stability during testing is important as many silicon photonic devices are sensitive to temperature change.

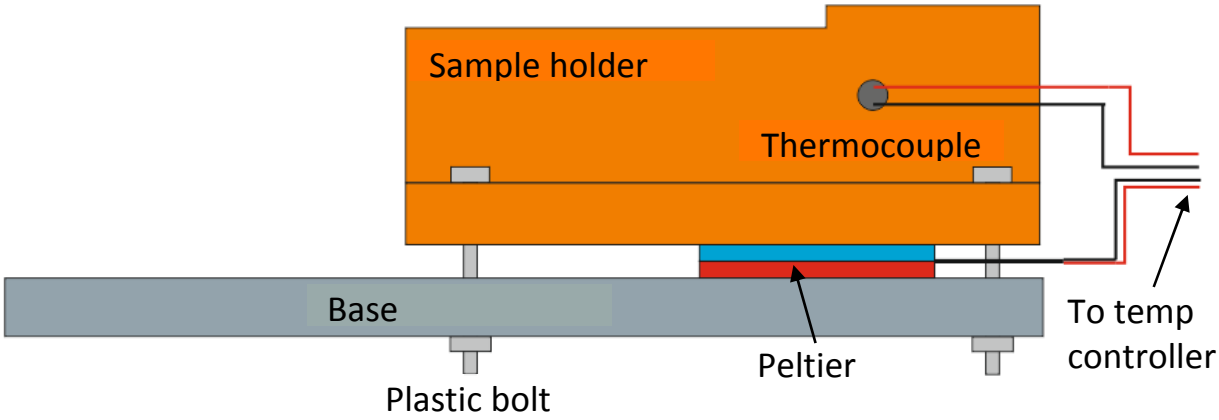

Figure 3.16 A diagram of a sample stage based on the stage used for grating coupler alignment.

3.2.4: Optical bench

Optical benches are used in order to minimise vibration to preserve alignment at the highest precision. They float on compressed air or magnets, removing contact with the ground where most vibrations are transferred.

3.2.5: Imaging

To make fibre to coupler alignment possible, vision of the sample is required. Therefore, a microscope and illumination is needed in order to see the sub millimetre features of the fibre and grating coupler. A simple yet effective set-up utilising a camera, focus tube, mirror and a light box is connected to a standard CCTV display via an analogue signal (Figure 3.9).

The light box shines light on a partial mirror which reflects the light down on to the sample illuminating it. The partial mirror also allows light to pass upwards through it into the focus tube and subsequently the camera (Figure 3.17).

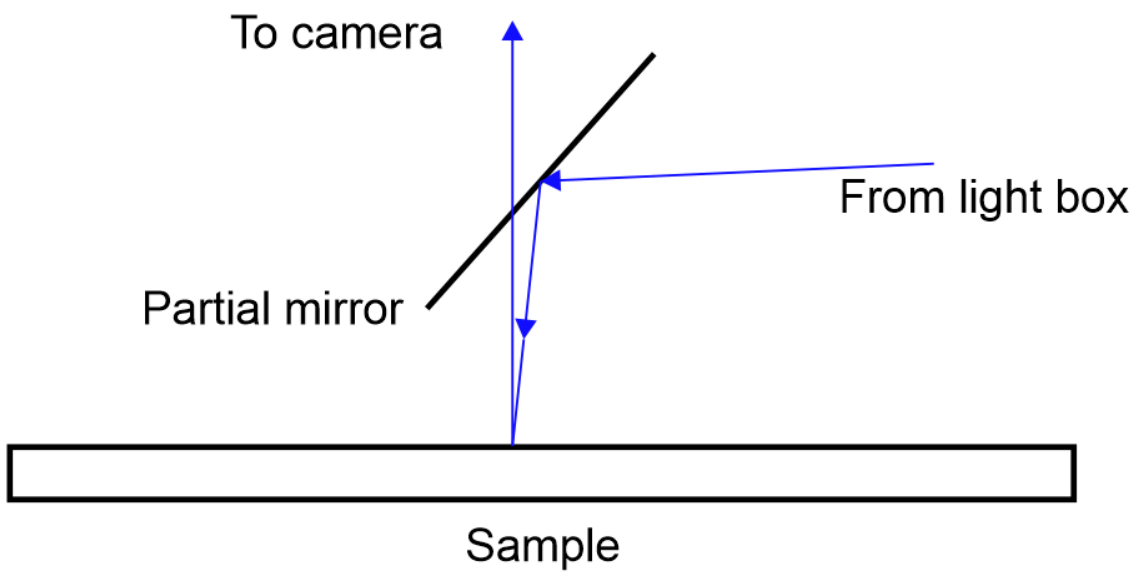

Figure 3.17 A diagram showing how a partial mirror illuminates the sample while also allowing vision of the sample via a camera

3.2.6: LASER and Detector

The laboratory contains an Agilent 81940A tuneable LASER and an 81634B low polarisation dependence optical power sensor (**Error! Reference source not found.**). Polarisation maintaining (PM) PM-S405-XP patch cables run from the source to a three paddle polarisation controller. This is connected via a standard SMF28 patch cable to a flat cleaved fibre secured to the input fibre holder. A flat cleaved fibre is also attached to the output fibre holder which is connected, via another PM patch cord to the sensor.

The LASER and sensor are both contained within an Agilent housing which has a control panel for adjusting power output and wavelength etc. The housing also allows connection to a PC which permits use of software that can control the system while also serving as a convenient data collector.

The screen on the control panel allows monitoring of the detected signal while alignment to the photonic chip is adjusted, when the peak efficiency is found the “Photonic Application Suite” which is software produced by Keysight technologies (formerly Agilent) is used to complete a scan across specified wavelengths. It then compares the output power from the LASER with that received by the detector and shows the loss in decibels across the scanned wavelengths.

The software displays a graph of the loss in decibels and the data can be exported as an Excel file for manipulation and formatting.

3.2.7: Polarization Control

The polarization controller uses three paddles or “fibre retarders” to induce birefringent stress in a fibre, they act as a quarter, half and quarter wave plate allowing the polarisation of the transmitted light to be rotated and transformed between circular, linear and elliptical (Figure 3.18). As grating couplers and waveguides are polarisation dependent carefully manipulation of the polarisation is required to maximise transmitted efficiency. As the polarisation of the light being transmitted from the fibre is difficult to determine, light is transmitted through test structures and the detected power is monitored with respect to wavelength. The polarisation is optimised by maximising transmitted power and reducing ripple observed on the signal, which is assumed to be caused by the wavelength dependence of birefringent polarisation control shifting the polarisation thus moving in and out of alignment with the grating couplers polarisation acceptance.

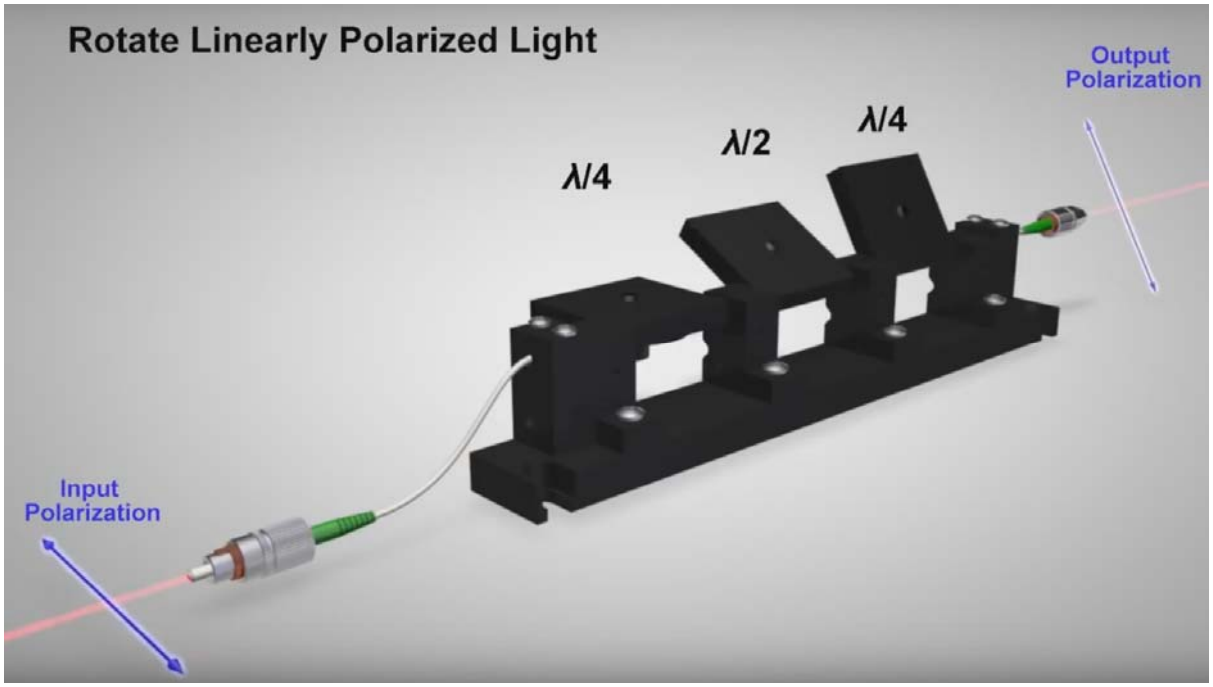

Figure 3.18 A diagram of a three paddle polarization controller showing the quarter half quarter wave plate configuration. taken from a video at thorlabs.de [58]

Chapter 4: Fabrication

Development of cleanroom recipes is a critical component in cleanroom work and is required before any fabrication takes place. The process for designing experiments for recipe development is discussed at the start of this chapter. The packaging concept is created in two parts; a capping chip containing v-grooves and alignment plugs, and a device chip containing photonic devices, holes that marry with the alignment plugs and fibre cavities for improved coupling and convenience of assembly. The wafers used for the capping chip are silicon wafers bought with a 4µm layer of LPCVD silicon nitride which is used as the material for the plug and is also used as masking layer for the v-grooves, both of which are produced in the same photolithographic step. The device wafer is a 400nm silicon on 2µm silicon dioxide SOI wafer and uses e-beam lithography for device production and a combination of photolithography and e-beam lithography for the packaging structures. Separate sections within this chapter specifically describe how the tools and processes defined in the previous chapter were used to create the resulting samples. The grating couplers are a component part of the optical chip and so section 4.3 in this chapter describes their design. Finally, the fabrication development is discussed critically identifying difficulties and summarising the achievements.

4.1: Design of Experiment (DOE)

When developing an experimental recipe that has complex parameters and unpredictable results, design of experiment (DOE) is used. There are many different ways to carry out a DOE, however usually they use a systematic approach to identify a relationship between a changeable variable and the resulting factors. Trends identified by the experiment can either be used to narrow input parameters for greater optimisation with a further DOE or show an ideal recipe.

DOE is typically used when finding an RIE recipe because the etch chemistries are extremely sensitive and there are a large number of variables to consider. When consulting the literature, it is unlikely to find a demonstrated scenario which matches the experiment in question and even when a process is demonstrated on two tools that are nominally the same, small differences apparent due to tolerances during manufacture may still make process development challenging.

At the start of the authors candidature a task was presented that would develop cleanroom familiarization and experimental method. The assignment was to produce a SiO_2 implant mask etch for active devices which had potential to be used within the packaging project. This required and RIE etch with high selectivity and near vertical sidewalls to protect waveguides from implantation as doping of the waveguide will induces loss.

A DOE was designed using the commercial software package, Minitab which is a statistical design and analysis tool[59]. A Box-Behnken DOE was used which is specifically designed to result in surface plots which should identify optimised areas. A three dimensional experimental space is generated by the low and high values of the desired variables (Figure 4.1 and Figure 4.2). which were chosen based on an existing recipe which did not meet the sidewall and selectivity requirements. The software then takes the midpoint of each variable and creates the experiment (Figure 4.3), choosing a random order to avoid bias in the results due to extraneous or uncontrollable conditions while repeating the centre experiment twice as it is likely to be the most desirable solution. If each variable combination in this space was tested the total number of experiments would be 27, however by removing the extreme values a Box-Behnken experiment reduces cost while estimating the missing results.

Factor	Name	Low	High
A	Ar Flow	0	48
B	Power	100	300
C	Pressure	50	100

Figure 4.1 A screenshot of the table to be filled out for a three parameter Box-Behnken DOE within Minitab

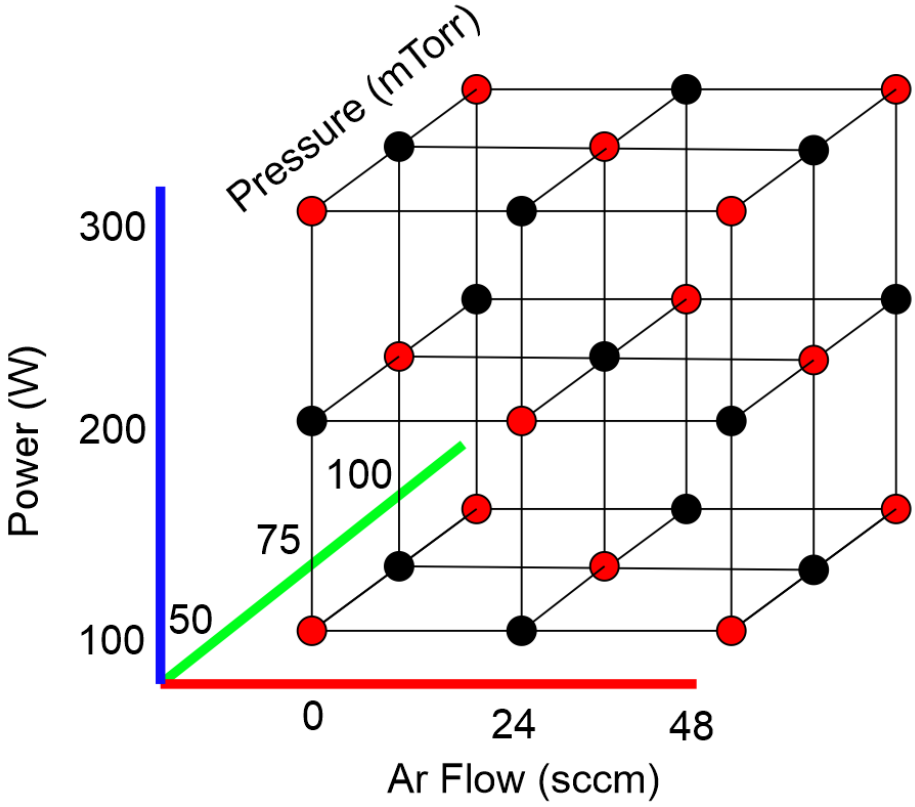

Figure 4.2 The 3D experiment space generated by a box Box-Behnken DoE where the red points are omitted to reduce the number of experiments

	RunOrder	PtType	Blocks	Ar Flow (sccm)	Power (W)	Pressure (mTorr)	Oxide Rate (nm/m)	Si Rate (nm/m)	Selectivity
1	1	2	1	0	300	75	100.4	79.2	1.268
2	2	0	1	24	200	75	100.6	80.0	1.258
3	3	2	1	0	200	50	21.4	1.2	17.833
4	4	2	1	0	200	100	100.4	80.2	1.252
5	5	0	1	24	200	75	0.0	0.4	0.000
6	6	2	1	48	300	75	83.0	14.0	5.929
7	7	2	1	24	100	50	25.2	5.4	4.667
8	8	2	1	24	300	100	76.8	13.2	5.818
9	9	2	1	48	200	100	58.6	0.2	293.000
10	10	2	1	48	100	75	24.2	5.2	4.654
11	11	2	1	0	100	75	-2.6	1.0	-2.600
12	12	2	1	24	100	100	17.0	0.0	*
13	13	0	1	24	200	75	55.4	8.2	6.756
14	14	2	1	48	200	50	51.8	13.0	3.985
15	15	2	1	24	300	50	72.8	13.2	5.515

Figure 4.3 A screenshot of the Box-Behnken experiment in Minitab showing the parameter combinations, the order they should be tested in and the results attributed to them highlighted on the right.

Carrying out the experiment on a wafer scale with e-beam structures, that are required to produce the hard mask, would consume more time and resources than desirable, instead a single Si wafer was prepared by depositing 250nm of SiO_2 via PECVD, spinning a 1µm layer of s1813 photoresist and exposing the resist through a process development mask. Once developed, the wafer was cleaved into 15 samples ready for etching.

Each sample was measured using an ellipsometer and profilometer before being etched under the conditions described in the experiment in addition to a constant CHF_3 flow of 80sccm. The SiO_2 samples were etched alongside SOI samples that would identify Si etch rates. After etching it was apparent that the recipes involving a 300W power had burnt the resist and so the samples were discounted. The rest of the samples were measured again, and the results were loaded in to Minitab (Figure 4.3 *right*) where trends can be identified.

The data showed a peak selectivity of 293:1 in run order 9 (Figure 4.3) so the sample was cleaved and examined with the SEM (Figure 4.4). The side wall was shown to be near vertical which is ideal and the recipe was trialled on full wafers.

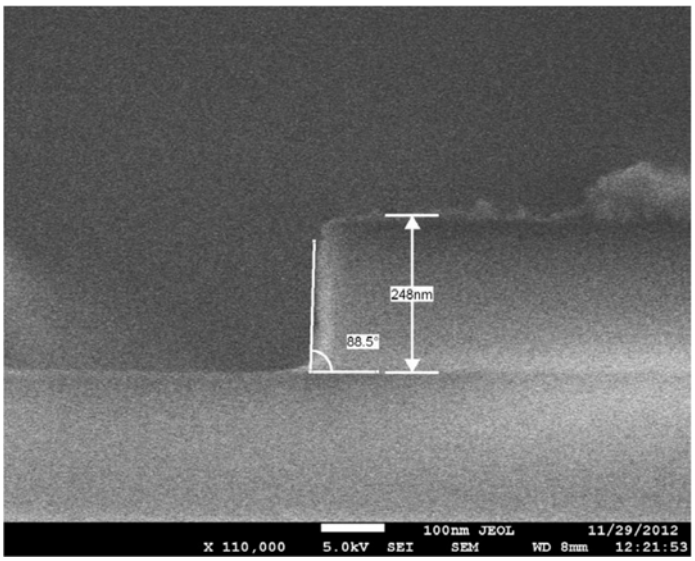

Figure 4.4 A cross section SEM image of the SiO_2 etch sample showing near vertical side walls.

The full wafer etch was carried out much in the same way as the samples. A problem was immediately apparent as the etch uniformity was visibly poor (Figure 4.5). When measured, etch rate was 13% slower at the edge compared to the centre of the wafer.

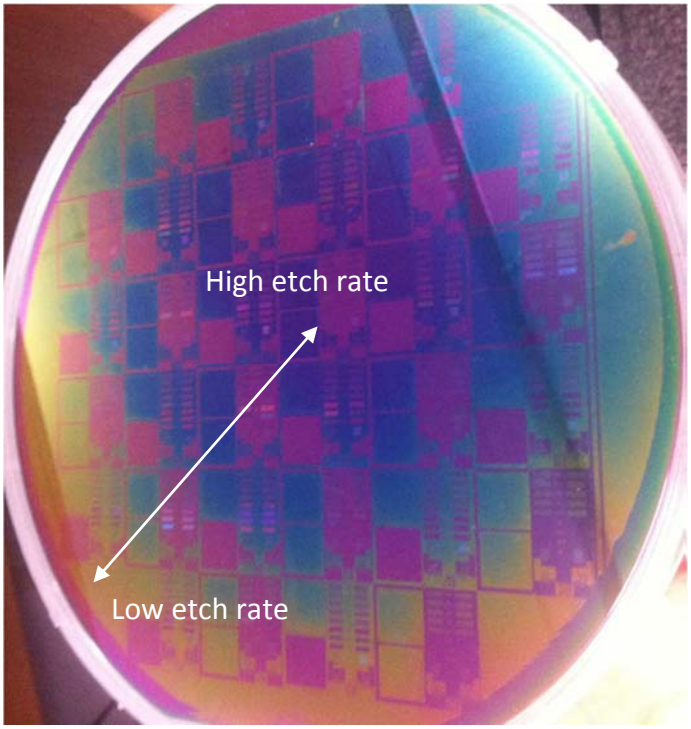

Figure 4.5 The 6 inch SiO_2 etch test wafer showing poor uniformity with a higher etch rate in the centre transitioning to a low etch rate towards the edge.

After consulting Dr Owain Clarke, who was the technical engineer specialising in plasma tools, the cause of the non-uniformity was considered to be higher polymer deposition at the edge of the wafer, reducing etch rate. A solution to this is to reduce the pressure and CHF_3, the lower pressure permitting higher mobility for physical etching and lower CHF_3 to reduce polymer formation. A new trial run was performed with the following parameters:

- CHF_3 – 60sccm
- Pressure – 90mT
- Ar – 48 sccm
- Platen Power – 200 W

This significantly improved the uniformity with a non-uniformity of 2.4% from the centre to the edge. Further investigation in to this recipe were performed by Dr Colin Mitchell however not long after this point the Plasmatherm Versaline tool was installed in the cleanroom which was installed with a SiO_2 etch that outperformed the recipe outlined here with 90° sidewalls which led to a complete switch to this process from that time.

When performing a DOE, the subject under test must be as close to that which will be used during fabrication because factors such as sample size, exposed etch area and resist chemistry

are highly sensitive to change. Beyond the experiments of the author further tests found that the high temperatures that did not affect S1813 photoresist melted e-beam resists which are more susceptible to dry etching, further complicating the process. Fortunately, many of the processes used for this work were adapted from existing recipes, saving time, but in few cases causing complications as discussed later in this chapter.

4.2: Optical Wafer

The optical wafer is made up of the samples to be packaged. For the purposes of the project grating couplers, tapers, waveguides and bends are created as a platform to test the packaging, under commercial circumstances any active or passive structures can be packaged on the samples.

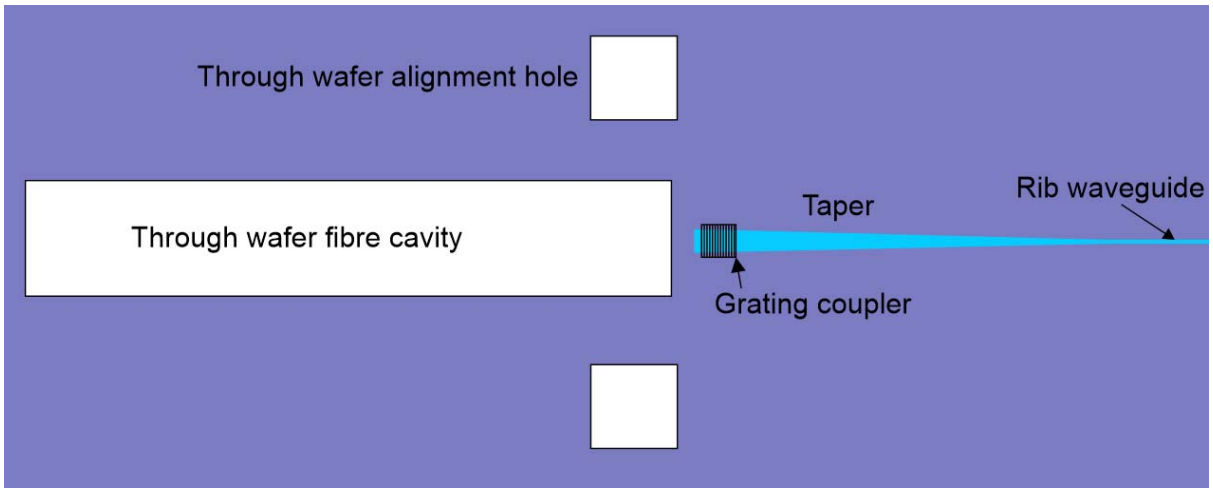

Figure 4.6 Top down diagram showing the main components of the optical wafer

The wafer starts off as an SOI wafer, the dimensions of which are not critical as the processing is flexible to a majority of scenarios. The processing of devices is another non critical process as the packaging process will need to conform to many different device structures across the silicon photonics platform. For the purposes of this project the devices will be created by e-beam. Once the optical devices have been made, the packaging process is in effect. The process flow for which will be explored in more detail in this section.

4.2.1: Process Flow

The optical wafer was designed to be produced in four main steps, shown in Table 4.1. The e-beam alignment marks are made, then devices are created, followed by a relatively deep front-side etch which becomes a through wafer cavity when the remaining substrate is removed from the backside.

Table 4.1 The optical wafer process flow.

Alignemnt Marks							Optical Components							Fibre Cavity Front								
Zep S/B	Espacer	Ebeam	Rinse	Develop	Etch	Ash	Zep S/B	Espacer	Ebeam	Develop	Etch	Ash	SiO_2 Dep	AZ2070 S/B	Espacer	Ebeam	Rinse	UV Flood	Bake	Develop	Etch	Si3n4 Dep

Backside through etch					
AZ9260 s/b	Expose	Develop	Bake	DRIE	Si3N4 Strip

4.2.2: Alignment Marks

When exposing more than one lithography step, alignment marks are required and are usually written at the same time as the first step. It was thought that alignment marks etched during the shallow device etch would not be sufficiently well defined to be detected by e-beam through the thick soft masks required later. Initially the alignment marks were e-beam written in ZEP520A (Table 4.3) and then etched through the Si and as far into the BOX as the resist would allow using the Si etch. It was found that this did not improve the clarity of the alignment marks through the thick resist and so the alignment marks were defined at the same time as the optical devices. E-beam alignment was a continuing problem throughout the project and often alignment marks were not detected preventing some samples from being written by the e-beam. Larger alignment marks are easier to detect but the distortion is still likely to affect alignment although using larger alignment marks did not yield any noticeable misalignment when observed under a microscope. In many cases a clearing etch would be used to remove impeding layers before lithography takes place, however seeing as the resist layer is 7 times thicker than the SiO_2 over layer the effect of clearing is unlikely to have an effect. Using a high resolution scanner/stepper may also mitigate this problem as the method of detecting alignment marks is optical which may not be affected as much as an e-beam albeit with lower accuracy.

Table 4.2 OIPT ICPRIE Si etch recipe used for etching devices and alignment marks.

Material	Tool	Gasses (sccm)	Flow Rate (sccm)	RF Power (W)	ICP Power (W)	Pressure (mT)	Temperature (°C)
Si	OIPT ICP	SF_6/C_4F_8	24/45	50	800	15	15

Table 4.3 Lithography process table

Resist	Spin Speed (1000 rpm)	Spin Time (s)	Thickness (µm)	Soft Bake Temp	Soft Bake Time (s)	Dose (uC/cm^2)	PEB Temp (°C)	PEB Time (s)	Exposure Time (s)	Dose µC/cm²	Developer	Develop Time (m)
S1813	4	60	1.3	115	60	NA	NA	NA	7	NA	MF319	~1:30
AZ2070 Photo	2	100	7	110	420	NA	110	60	11	NA	AZ 400k 4:1	~3
AZ9260	3	60	7	110	120	NA	NA	NA	11	NA	AZ 400k	~3
ZEP520A	6	60	0.45	180	120	190	100	120	NA	190	ZED-	1
AZ2070 E-Beam	2	100	7	110	420	100	110	60	NA	100	AZ 400k 4:1	~3

4.2.3: Optical components

The optical components used for this project are grating couplers, tapers, bends and rib waveguides. They are all defined in a single e-beam step using ZEP520A photoresist (Table 4.3) and a single silicon etch is carried out on the Oxford ICPRIE S380 to transfer the pattern in to the silicon over-layer. The etch depth is 220nm and takes approximately 30s using the recipe shown in Table 4.2, leaving a 180nm slab.

Once the devices have been etched an SiO_2 over-layer is deposited to act as an upper cladding and protect the structures (Table 4.4).

Table 4.4 PECVD process table.

Material	Gasses	Gas Flow (sccm)	Temp(°C)
SiO_2	$SiH_4/N_2/N_2O$	4.2/80/350	350
Si_3N_4	$SiH_4/N_2/NH_3$	12.5/500/20	350

4.2.4: Fibre Cavity and Alignment Holes

Due to the complexity of the layers and the high positional accuracy required, the fibre cavity and alignment holes are produced using a multi etch procedure. Figure 4.7 shows the optical wafer stack looks like after the optical components have been fabricated and is the most commonly used configuration within the silicon photonics group for near infrared designs. All of the process recipes are flexible and have the potential to accommodate thicker layers without added complexity.

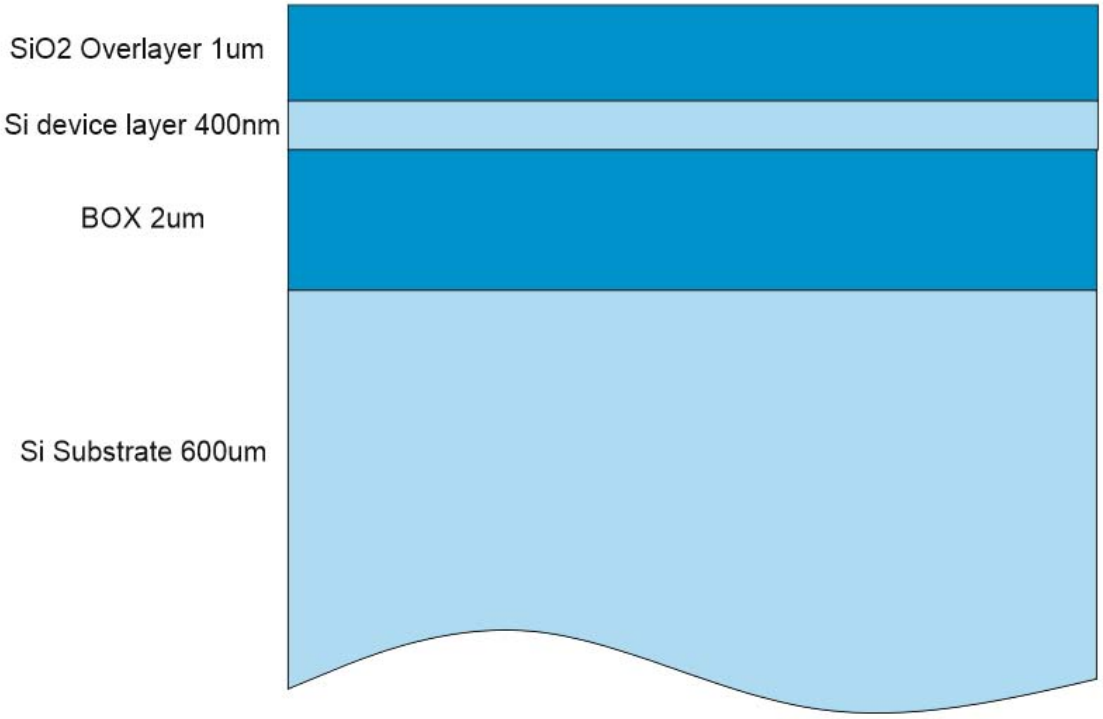

Figure 4.7 The optical wafer stack after production of optical devices and the deposition of a SiO_2 cladding layer.

In order to etch through the entire wafer, a thick soft-mask is required, however, the positional accuracy requires e-beam photolithography, reducing the number of available resists. Generally, e-beam resists are thin in order to allow for smaller critical features and do not usually have high resistance to dry etches compared to other resists.

To resolve a solution Dr Ali Khokhar was consulted for his broad knowledge of e-beam processing. The standard e-beam process used within the silicon photonics group use ZEP resist for small critical features over shallow etches, and PMMA950A11 which allows deeper

etches while maintaining small features. For the process in question, small feature sizes are not critical, but resistance to plasma etching, precise alignment accuracy and thickness are. As PMMA950A11 was the thickest resist used, an etch test was conducted to measure its selectivity to Si and SiO_2 etching.

The etched cavities were designed to penetrate through the wafer, and the DRIE tool was used for its high selectivity while etching Si, in the order of 100:1 Si to typical photoresists. etch tests using PMMA950A11 agreed with this.

The DRIE was also chosen to etch the SiO_2 layers as it has proven to etch SiO_2 with a vertical profile (

Figure 4.8) which is important for fibre positioning. Experiments showed a selectivity of 1:2 SiO_2 to AZ2070. This selectivity dictates a total resist thickness of over 12µm (4.1).

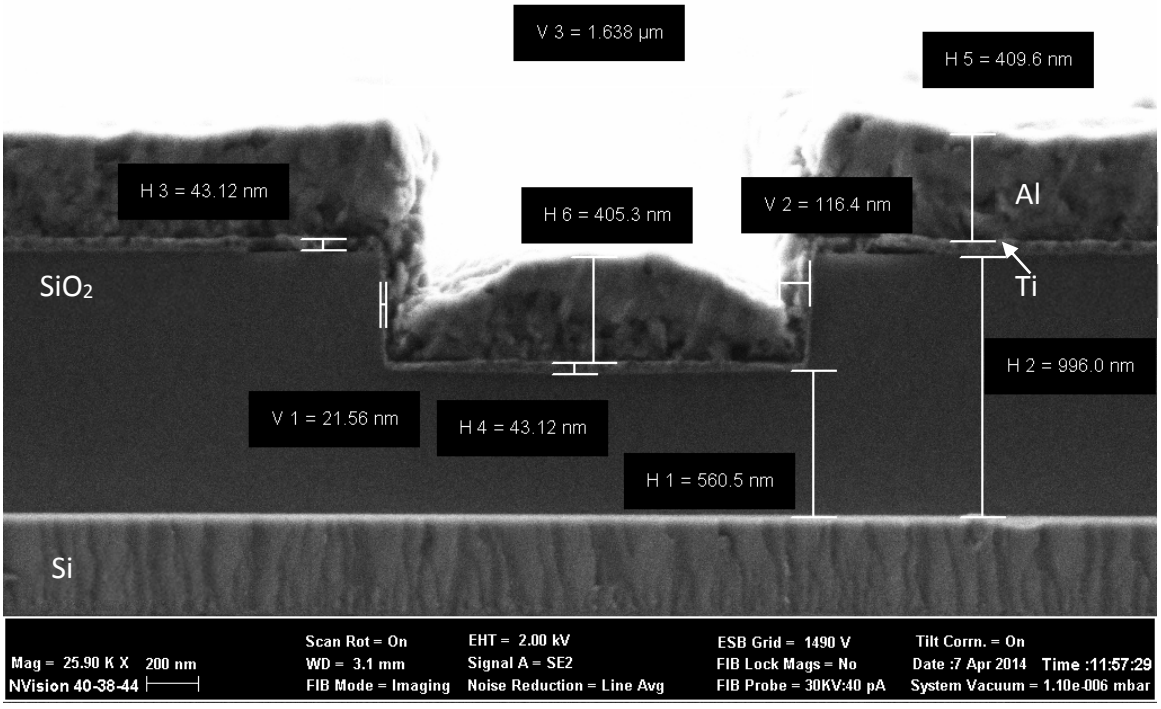

Figure 4.8 An example of the SiO_2 etch in the DRIE showing its ability to produce a vertical sidewall SiO_2 etch. Image credit; Callum Littlejohns.

$$\frac{600\mu m}{100} = 6\mu = Resist\ required\ to\ etch\ Si \quad \textbf{4.1}$$

$$\frac{3\mu m}{0.5} = 6\mu = Resist\ required\ to\ etch\ SiO_2 \quad \textbf{4.2}$$

For e-beam resist this is unlikely especially PMMA950A11 as attempts to deposit layers thicker than 3µm ended in delamination.

In order to reduce the demands on the resist thickness, all of the Si substrate could be etched from the backside of the wafer and would not need the accuracy of the e-beam tool provided the top layers were etched accurately. This halves the required resist layer for the top and bottom and standard photoresists are easily available in thicknesses of over 6µm. AZ9260 was chosen as the processing involved is mature within the cleanroom (see Figure 4.12 (1) on page 75).

A >6µm e-beam resist was still required to etch the front layers of SiO_2 (see Figure 4.12 (4), AZ2070 is a resist that can be used for standard photolithography well over 6µm, and the mechanism used to crosslink the polymer with UV light, where radical species are produced, is similar to when e-beam is used where electron collisions cause the same radical species to occur and thus crosslinking[60]. Therefore, AZ2070 could potentially be used e-beam lithography. Currently, there have been no studies of using it as an e-beam resist for layer thicknesses greater than 1µm thick. Dose test experiments were run to see if it could be exposed and developed well enough for this cause and it was discovered that the process worked, developing completely whilst maintaining feature size.(Figure 4.9).

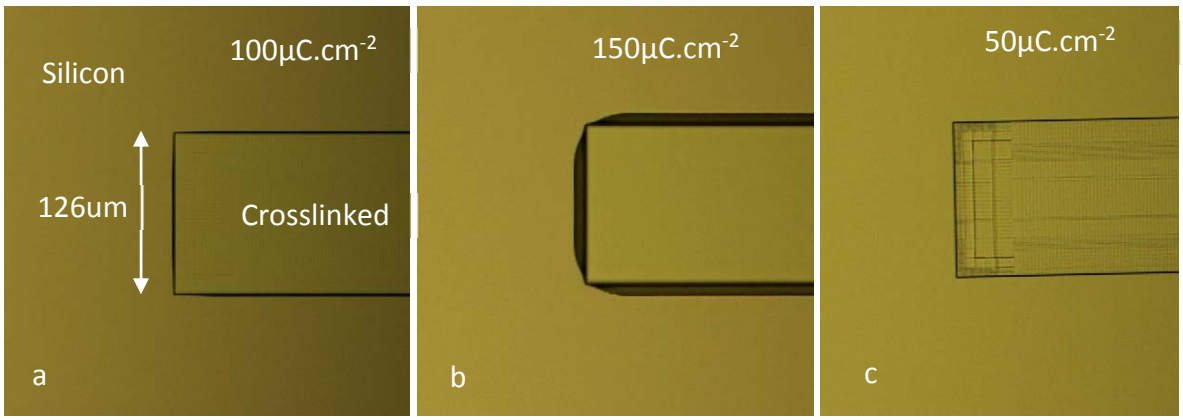

Figure 4.9 A dose test using AZ2070 showing resist layers after 2 minutes and 35 seconds and a dose of 100µC.cm-2 with good development (a), 150µC.cm-2 which shows overexposure (b) and 50µC.cm-2 which shows underexposure(c) .

The only drawback to using AZ2070 is that it is a negative resist, in order to define holes in the resist to etch through, a majority of the wafer would need to be written which would take an unfeasible amount of time. As AZ2070 can be used as a photolithography resist a 2 stage

process can be used to reduce the amount of write time. The first stage would be to outline the structure with e-beam, creating an outline thick enough to allow for the alignment tolerance of the contact aligner which is better than ±2.5µm therefore 5µm boarders were used. Using a photolithography mask aligned to the e-beam mask, the rest of the wafer is then exposed, crosslinking a majority of the resist in a short amount of time. Figure 4.10

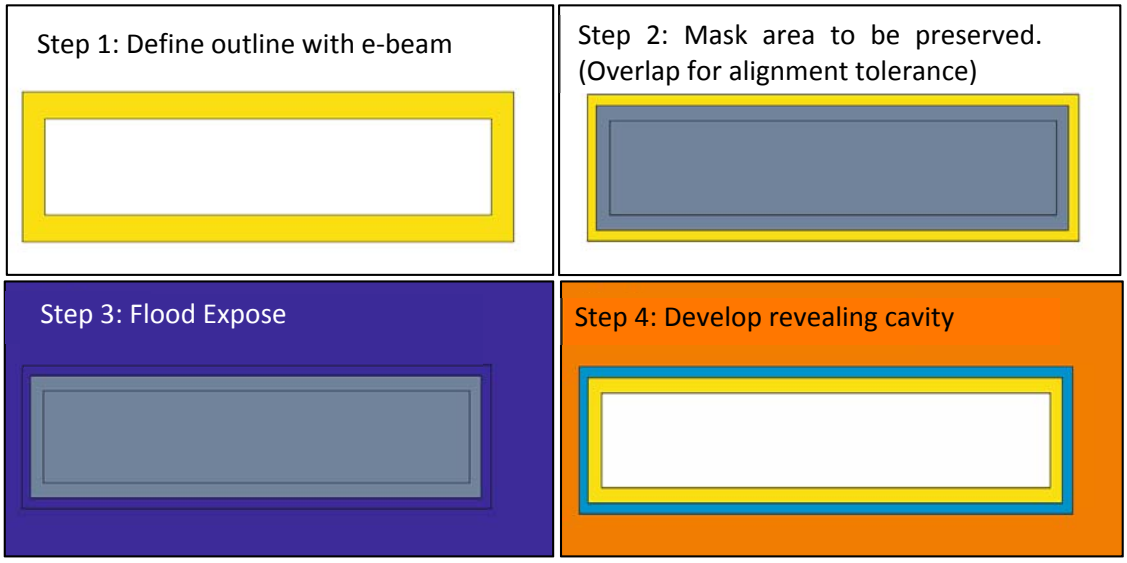

Figure 4.10 A diagram showing the hybrid lithography process using e-beam lithography to define an outline and contact lithography to reduce write time by exposing non critical areas.

Experiments yielded good alignment between the two lithography steps, see Figure 4.11, where alignment within the ±2.5µm can be observed.

It is worth noting that the author was required to use the e-beam for its accuracy. However, this could be achieved by a high throughput stepper for an industrial application, removing this resist complication.

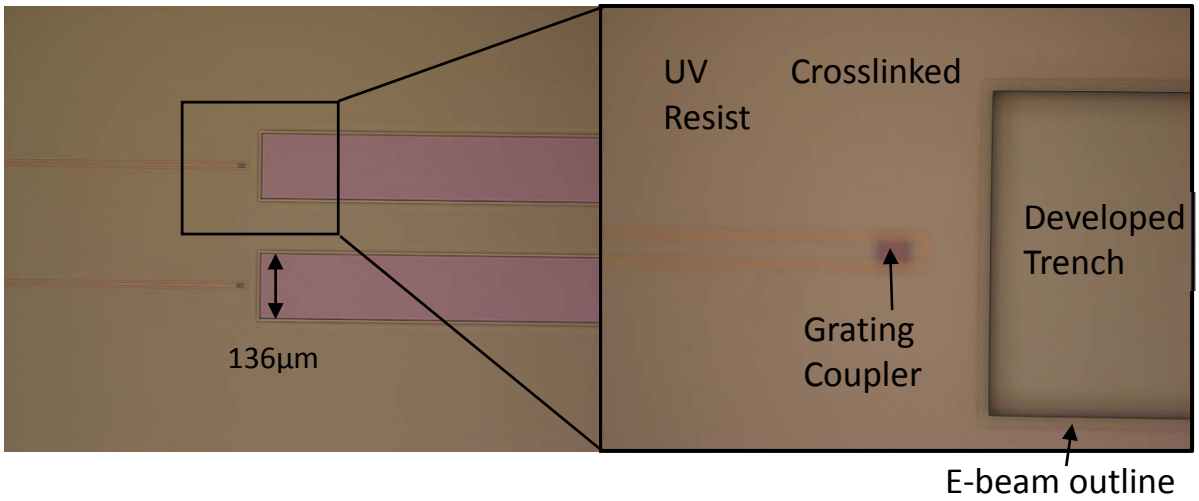

Figure 4.11 The completed hybrid lithography process.

A condensed version of the device wafer, through wafer etch process flow is shown in Figure 4.12 where some of the less critical process steps are omitted. Firstly, the front side hybrid lithography process is used to define a soft mask using AZ2070 (Table 4.1). The DRIE tool is then used to etch through the SiO_2 over-layer, the silicon device layer and then the SiO_2 BOX, all in the same etch step (Table 4.5). Once the front side etch is complete, a 500nm Si_3N_4 layer is deposited on the front side which serves as a protection layer for the rest of the process (Table 4.4). The back side process starts by spinning on 6µm AZ9260 and exposing it using backside photolithography (Table 4.3). With a selectivity of 100:1 this thickness is plenty for the DRIE process which uses the patented Bosch etch (Table 4.5) to remove the silicon, leaving the completed deep etch.

Table 4.5 Plasmatherm Versaline etch process table.

Material	Tool	Gasses (sccm)	Flow Rate (sccm)	RF Power (W)	LF Bias (V)	ICP Power (W)	Pressure (mT)	Temperature (°C)
Si (Device)	OIPT ICPRIE	$SF_6/C4F_8$	25/45	50	NA	800	15	15
SiO_2	Plasmatherm Versaline	CF_4	50	100	0	400	5	15
Si (Bosch)(1)	Plasmatherm Versaline	SF_6/Ar	150/30	0	250	2000	40	15
Si (Bosch)(2)	Plasmatherm Versaline	SF_6/Ar	350/30	0	10	2500	80	15
Si (Bosch)(3)	Plasmatherm Versaline	C_4F_8/Ar	150/30	0	10	2000	25	15

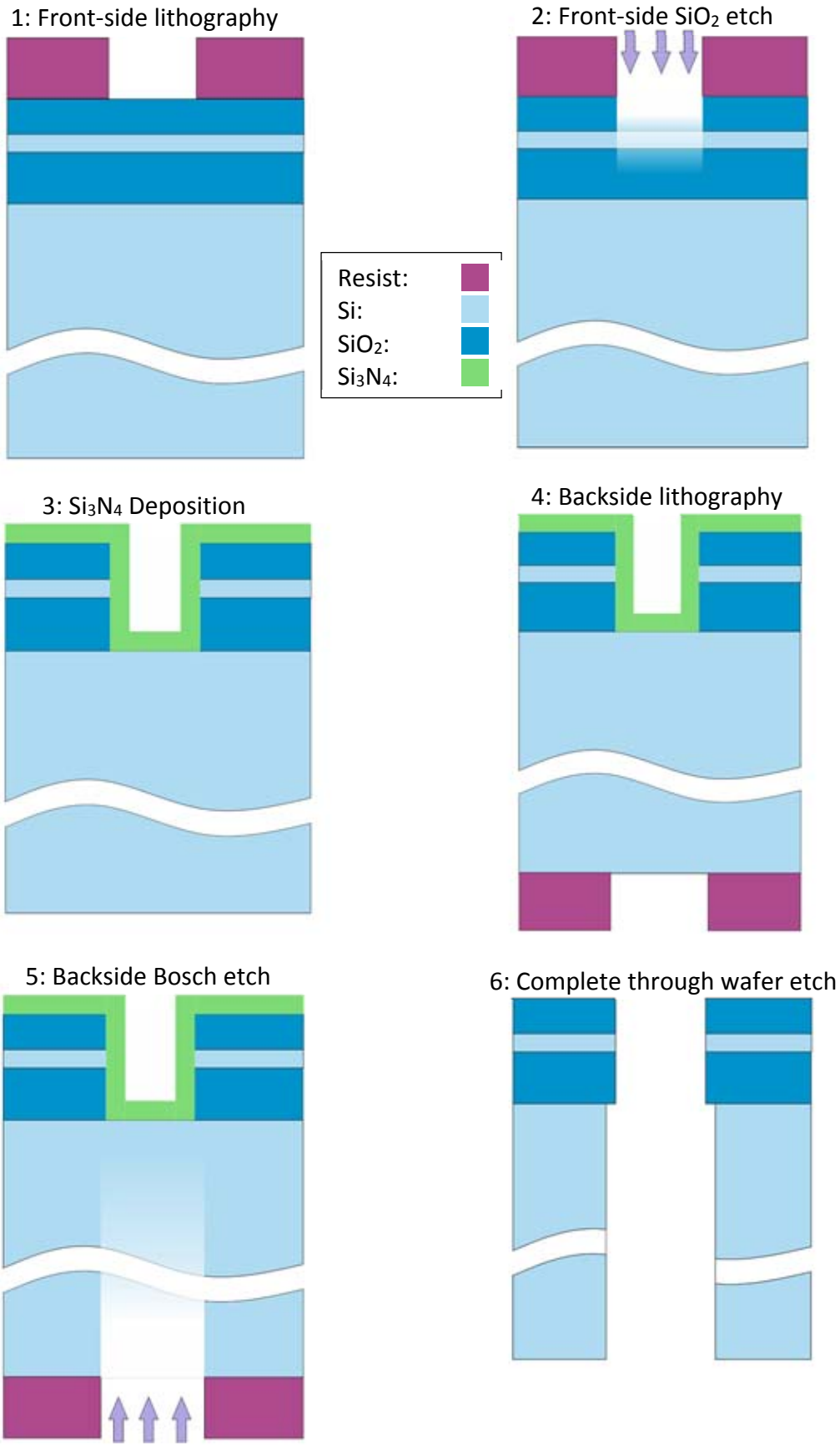

Figure 4.12 Diagrams of the device wafer, through wafer etch process depicting lithography and etching of the front side down to the substrate, depositing nitride to protect the platen and then lithography and etching of the substrate from the back side.

The images in Figure 4.13 and Figure 4.14 show the SEM images recorded during process development. They were used to show sidewall angles and verify resist selectivity and etch rates.

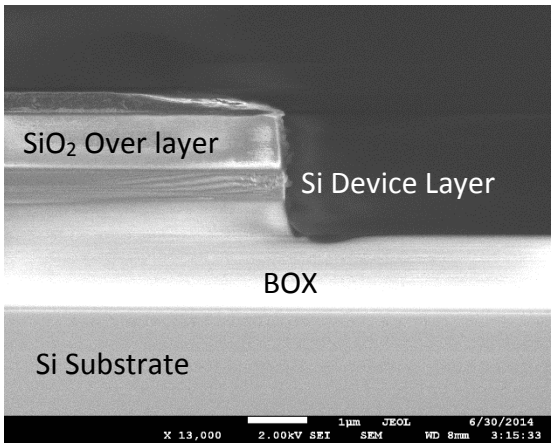

Figure 4.13 An SEM image of a partial front side SiO_2 etch, showing vertical sidewall profile.

Firstly the front side etch was characterised, (see Figure 4.13), and shows around half of the front side etch having been completed with good sidewall verticality and good continuity between Si and SiO_2. It also shows the lack of resist, highlighting the requirement for a thicker AZ2070 layer.

Figure 4.14 shows the initial steps for developing the deep backside etch. It shows grassing or pillars of silicon in the bottom of the trench, this is due to a lack of power in the DRIE preventing effective ion bombardment, resulting in areas of the passivation layer remaining and acting as a mask during the chemical silicon etch. It was found that the low frequency bias voltage needed to be ramped up as the etch continued. Fortunately, the Plasmatherm tool has a function that allows shaping of process parameters during processing. The bias voltage was ramped from 250V to 400V over a 20 minute etch which produced the etch profile shown in Figure 4.15 on page 79.

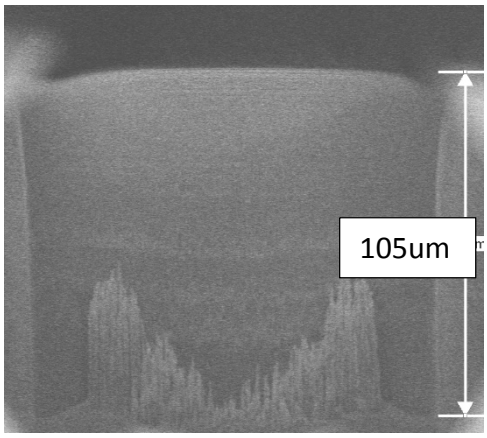

Figure 4.14 An SEM showing a back side deep etch trench with grassing at the bottom caused by a lack of power as the etch gets deeper, preventing the complete removal of the passivation layer deposited previously.

Non-uniformity in the backside etch has been found to cause problems where some of the trenches break through before others, and as Si_3N_4 is not an ideal etch stop as it is also etched. Once the integrity of the wafer has been broken, the helium backside cooling leak rate increases, stopping the process. To combat this, a 2µm layer of SiO_2 was deposited on top of the Si_3N_4 layer, acting as an etch stop. This addition makes the stripping process more complex as the BOX has been revealed by the backside etch, stripping the etch stop will also remove the BOX material which is critical for fibre positioning. To protect the BOX, resist was deposited on the backside, filling the trenches and allowing the use of HF to strip the etch stop. Then, once the resist and nitride are stripped, a through wafer cavity is revealed.

Edge defects due to wafer handling caused holes to be etched round the rim of the wafer, as the backside etch is completed in multiple stages to check etch depth, misalignment of the clamp of the Versaline meant these holes allowed the backside helium cooling leak rate to increase again. Careful handling of the wafers, plus the bead of SiO_2 around the edge of the wafers solved this issue.

Resist sticking in the Versaline was an ongoing issue during the project. The clamp pressure was changed and helium flow rates were adjusted by the technical engineers without positive results. It was found that post development baking of the wafer for 20 minutes in a 120°C oven stopped the sticking. However this is known to reduce feature accuracy due to non-uniform solvent evaporation affecting resist profile [61]. A new clamp design is being considered to try and rectify the problem for which the process is still ongoing.

The backside etch has a secondary advantage where the etch window can be opened out to etch beneath the grating allowing for the deposition of a mirror to improve the efficiency of the coupler[62] this will be proposed as part of future work.

4.2.5: Backside SiO_2 Removal

The discovery of SiO_2 on the backside of the SOI wafer came late in the project, and backside etch studies were carried out on bulk silicon wafers to save the relatively expensive SOI wafers. When the backside of the SOI wafers failed to etch it did not take long to realise that the growth of the BOX during the production of the SOI wafers also deposited SiO_2 on their backside. For reasons explained earlier in this chapter, it was desirable to maintain a bead of SiO_2 on the edge of the backside of the wafer. After spinning on S1813 resist Table 4.3 a rough mask was created using kapton tape to cover the wafer's outer edge, the wafer was then exposed on the EVG620TB mask aligner and developed in MF319 developer. HF was used to strip the unmasked SiO_2 to reveal the backside silicon (Table 4.6) for dry etch.

Table 4.6 Wet etch process table.

Material	Chemical	Temperature(°C)	Concentration
SiO_2	HF	24	40%
Si_3N_4	H_3PO_4	145	~75%

4.2.6: Final Process flow

Having produced an initial process flow, all of the individual steps were characterised and any issues were solved. They were then completed in order, and further problems were solved. This resulted in a number of changes, and the resulting process flow is shown in Table 4.7.

Table 4.7 The final process flow

Backside SiO_2 removal					Devices							Front-side deep etch									
Back S1813	Exopse Edge	Develop	HF	Ash	Zep S/B	Espacer	Ebeam	Develop	Etch	Ash	Sio2 Dep	AZ2070 S/B	Espacer	Ebeam	Rinse	UV Flood	Bake	Develop	Etch	Si3n4 Dep	Ash

Backside through etch					
AZ9260 s/b	Expose	Develop	Bake	DRIE	Si3N4 Strip

The desired results for the optical wafer are almost apparent, Figure 4.15 shows the current progress for which completion is only limited by the backside etch which in itself is still limited by wafer sticking in the Plasmatherm DRIE. Some poor development is observed in the backside trench as it is difficult to observe the development on the backside of an unpolished wafer. A more reliable solution for this development is required, one option is to use back side polished wafers.

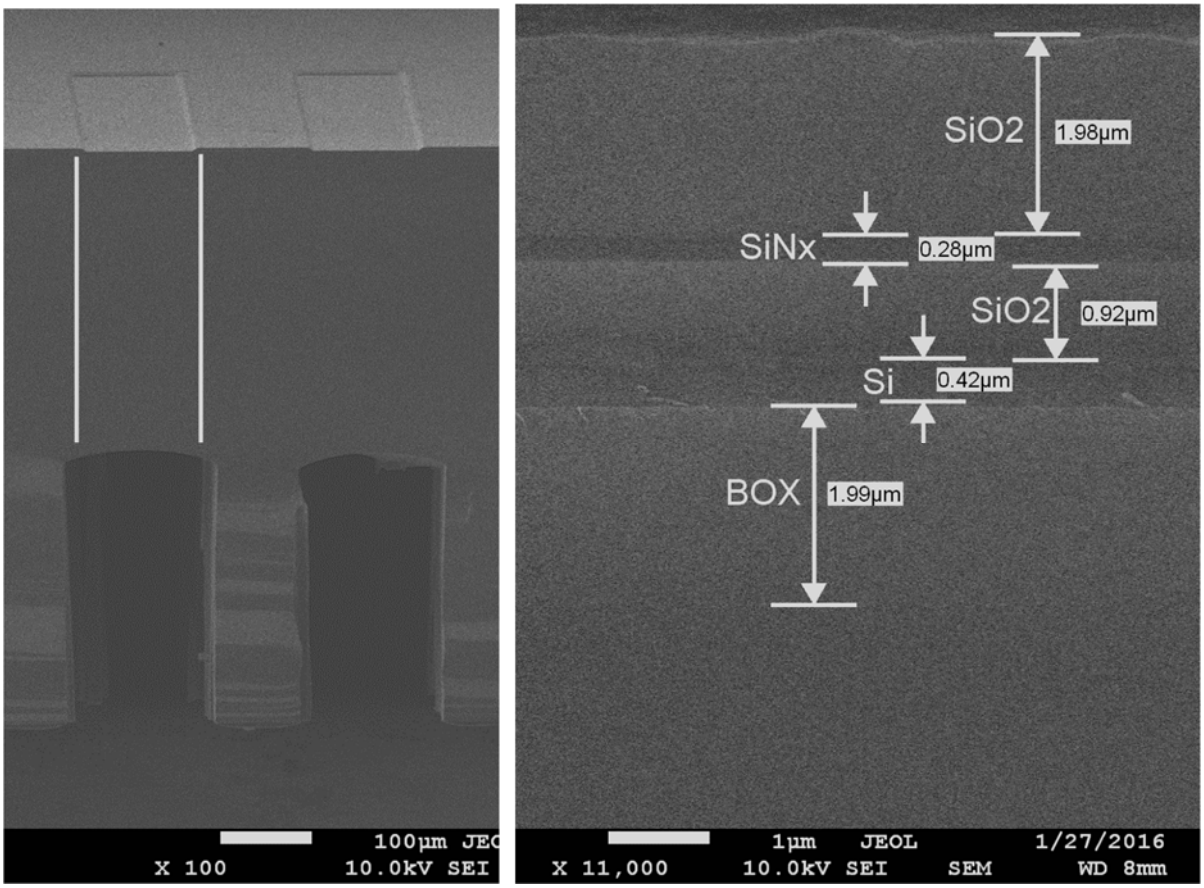

Figure 4.15 SEM cross section images of an optical chip showing (left) the complete front side etch and partial backside etch showing backside alignment within the ±5µm tolerance. Some lateral etching is observed but is not critical and poor development needs addressing. (right) The complete stack before stripping the front protection layers.

4.3: V-Grooves and Alignment Plugs

The v-grooves and plugs are the two components that make up the capping chip (Figure 4.16) the v-grooves support and position the fibre while the plugs locate and secure the fibre and capping chip to the device chip. The two components are defined in the same process step in order to maintain exact positional accuracy. The plugs are made from the silicon nitride (Si_3N_4) material used for the KOH etch hard mask, which allows fewer process steps than depositing separate layers for masking and plugs. Consequently, the nitride mask needs to be as thick as possible to secure the two halves of the device. Deposition of silicon nitride generates stress due to the lattice mismatch between it and Si [63] and therefore it is challenging to reliably deposit thick layers without deformation or damage. The literature and industry shows that thick silicon nitride films are possible [64], however it was decided that initially the Si_3N_4 wafers would be purchased from a third party called SiMat for ease of development. Deposition of thick nitrides can be developed later if necessary.

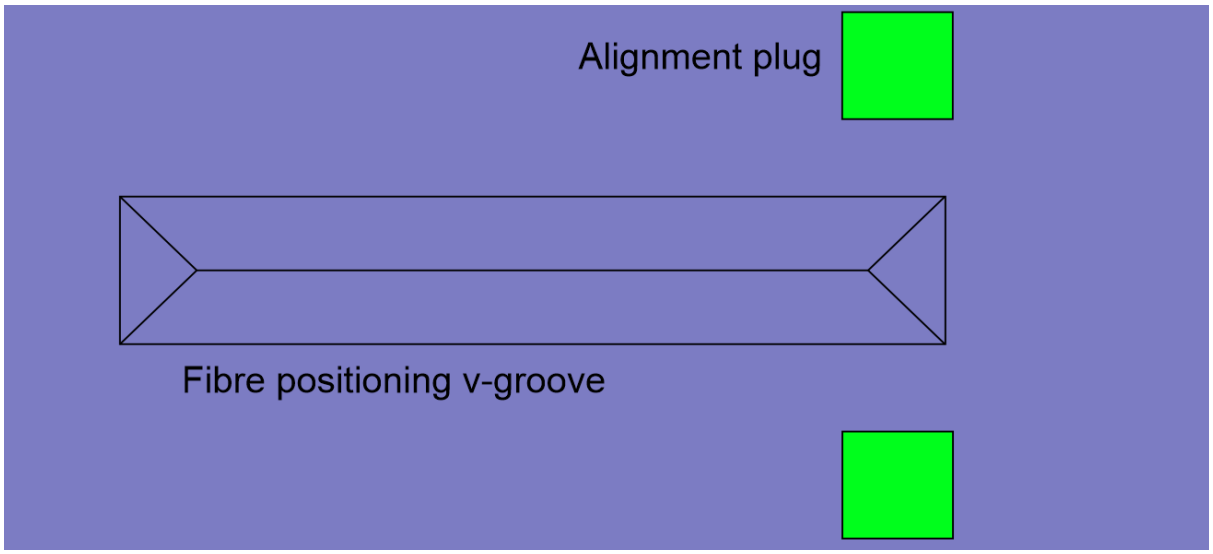

Figure 4.16 A diagram showing the layout of the capping chip with a v-groove to support a fibre and plugs for passive alignment

At the start of the project a process flow was designed for producing the plugs and grooves, this section will initially describe the designed process flow, it will then explain what issues occurred while implementing it and the methods used to overcome them. The resulting process flow will then be shown.

4.3.1: Process Flow

The capping wafer was designed to be completed in three main steps shown in Table 4.8 and illustrated in Figure 4.17. Alignment marks are created to allow accurate crystallographic alignment to an accuracy of ±0.05° [65]. The v-grooves are aligned to this and are defined and etched at the same time as the plugs in the next major process step. Finally, redundant Si_3N_4 needs to be removed while preserving the plugs.

Table 4.8 is an excerpt from the spreadsheet used to track development progress. Every step in the process is represented.

CA Marks								Nitride Trenches an Plugs								Plug Protect and Strip								
AZ9260 Spin	Bake	Rest	Expose	Develop	Nitride Etch	Ash	KOH Etch	AZ9260 Spin	Bake	Rest	Expose	Develop	Nitride Etch	Ash	KOH Etch	SiO2 Dep	S1813 Spin	Bake	Expose	Develop	HF Strip	Ash	Orthophos	HF Strip

4.3.2: Crystallographic Alignment and V-grooves Process

The process starts with the purchased Si_3N_4 wafers which are six-inch silicon substrates that have 4µm of low pressure chemical vapour deposition (LPCVD) silicon nitride on the front surface. AZ9260 photoresist was chosen as a soft mask as it can be deposited in a relatively thick layer (>12µm). With an etch selectivity of 2:1 (Resist to Si_3N_4) less than 3um is required, however 7µm is used as the recipe is mature and allows for much thicker BOX and SiO_2 over layers, improving the flexibility and reliability of the design. The AZ9260 is patterned with crystallographic alignment marks which are aligned to the flat of the wafer (Table 4.9) and the Si_3N_4 is dry etched in the ICPRIE (Table 4.10), then any excess resist is removed in the asher. The alignment marks are etched with KOH (Table 4.11) to reveal crystal plane alignment which is described later in this chapter. The process steps to create the v-grooves are similar, but with the v-groove mask accurately aligned to the crystal plane using the alignment marks produced in the initial step. After the second KOH etch the v-grooves are complete.

Table 4.9 Lithography processes used for the capping wafer.

Resist	Thickness	Soft Bake Temp	Soft Bake Time (s)	Dose (uC/cm^2)	PEB Temp (°C)	PEB Time (s)	Exposure Time (s)	Developer	Develop Time (m)
AZ9260	7um	110	120	NA	NA	NA	11	AZ 400k 4:1	~3
AZ2070 E-Beam	7um	110	420	100	110	60	NA	AZ 400k 4:1	~3
S1813	1.3um	115	60	NA	NA	NA	7	MF319	~1:30

Table 4.10 The Si_3N_4 etch process.

Material	Tool	Gasses	Flow Rate (sccm)	RF Power (W)	ICP Power (W)	Pressure (mT)	Temperature (°C)
Si_3N_4 (landing)	OIPT ICPRIE	CHF_3/O_2	77/4	175	0	22	20

Table 4.11 The wet etch process used for making the capping wafer.

Material	Chemical	Temperature(°C)	Concentration
Si	KOH	80	40%
Si_3N_4	H_3PO_4	145	~75%
SiO_2	HF	24	40%

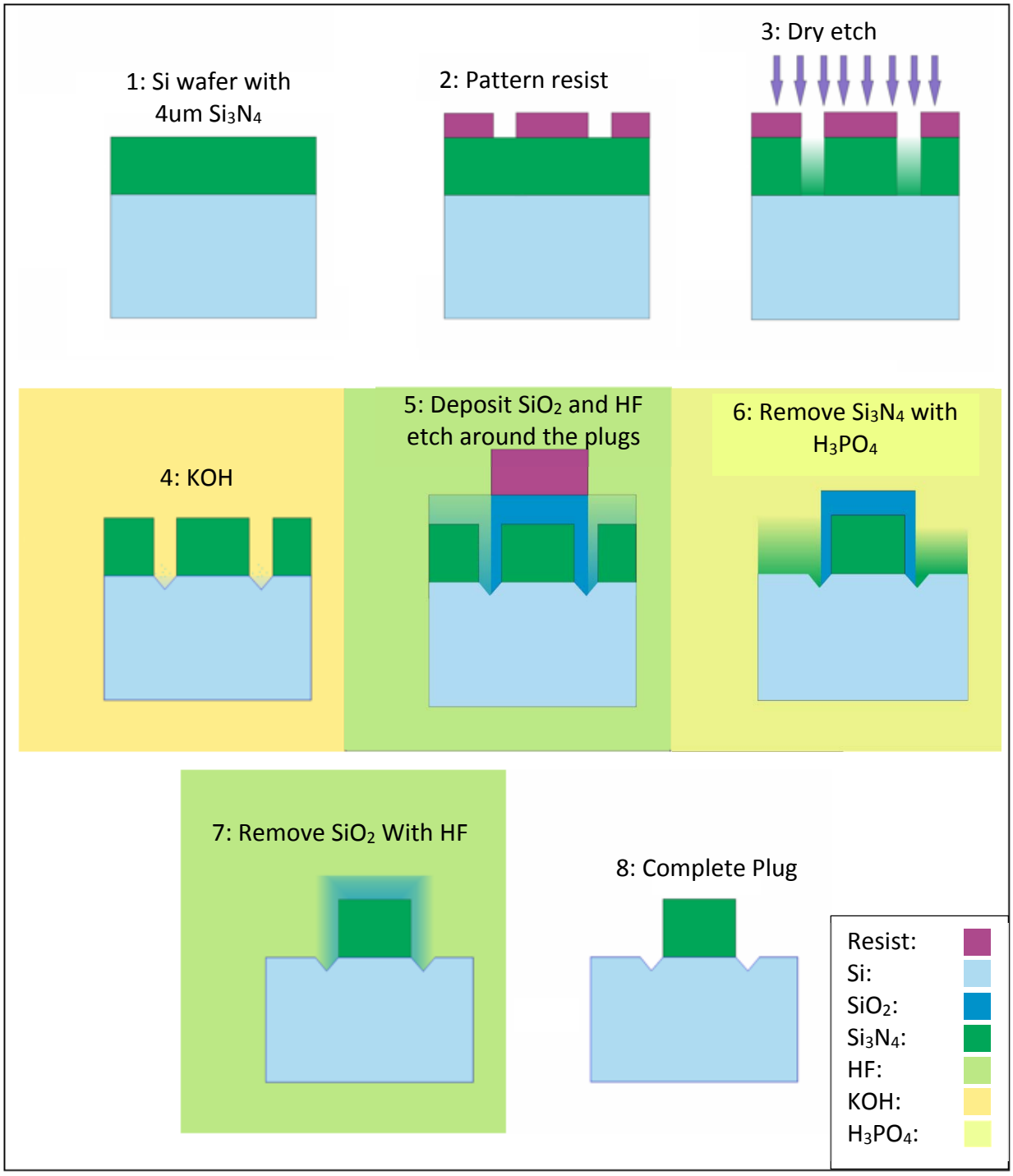

Figure 4.17 An illustration of the initial process flow.

4.3.3: Plug Protect and Strip Process

The next steps are carried out in order to strip the excess Si_3N_4 while preserving the plugs (Figure 4.17). PECVD silicon dioxide is deposited (Table 4.4) as a hard mask for the plugs and then S1813 is spun on and exposed (Table 4.9). The alignment for this exposure is not critical, the width of the trench is 10µm, allowing an alignment tolerance ±5µm.As long as the mask overlaps this trench on all sides, the plugs will be protected. Once developed the silicon dioxide is etched in HF (Table 4.11) and what remains covers the plugs. The excess resist is ashed away and then the exposed Si_3N_4 is etched in hot phosphoric acid (Table 4.11). When the SiO_2 protection layer is removed in HF, all that is left on the wafer is the v-grooves and silicon nitride plugs.

Table 4.12 PECVD process table.

Material	Gasses	Gas Flow (sccm)	Temperature(°C)
SiO_2	$SiH_4/N_2/N_2O$	4.2/80/350	350
Si_3N_4	$SiH_4/N_2/NH_3$	12.5/500/20	350

4.3.4: V-groove Fabrication

Under Cut

KOH is used to create the v-grooves that will support the fibre and create the mirror to reflect light from the fibre to the grating coupler on the optical chip. Considerations when masking the Si must be made that are different to other etching methods. When etching to the (110) plane, it is easy to undercut the mask layer as shown in Figure 4.18, causing the dimensions of the etched cavity to change. There are two main contributors to undercut: over etch of the Si_3N_4 hard mask and crystallographic alignment/misalignment.

Figure 4.18 a SEM image showing significant undercut on one of the first KOH experiments.

CRYSTALLOGRAPHIC ALLIGNMENT

Incorrect mask alignment to the Si crystal plane results in an undercut of the mask. The dimensional change depends on the size of the etch window and the rotation angle away from the crystal plane. The change in width is the critical feature here as a longer length is desired to support the fibre as much as possible, causing the width to expand dramatically if any rotation occurs (

Figure 4.20, Figure 4.19).

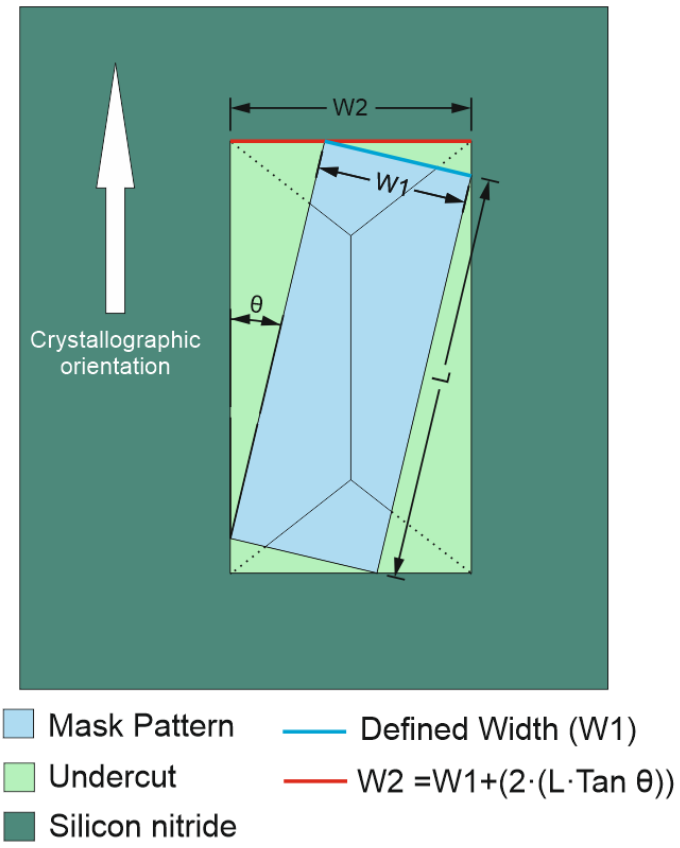

Figure 4.19 If a mask is rotated away from the crystal plane the resulting KOH groove will be larger by a function of the rotation and size.

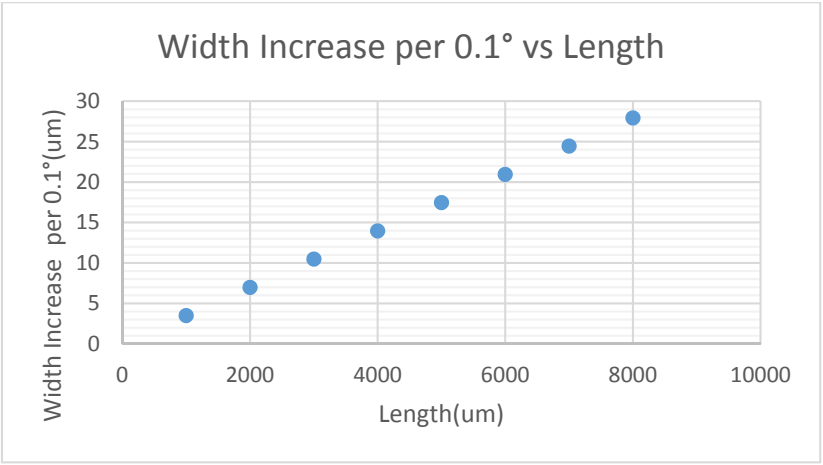

Figure 4.20 Graph showing the calculated increased width per 0.1° of KOH etched v-grooves for various lengths based on equation W2 in Figure 4.19

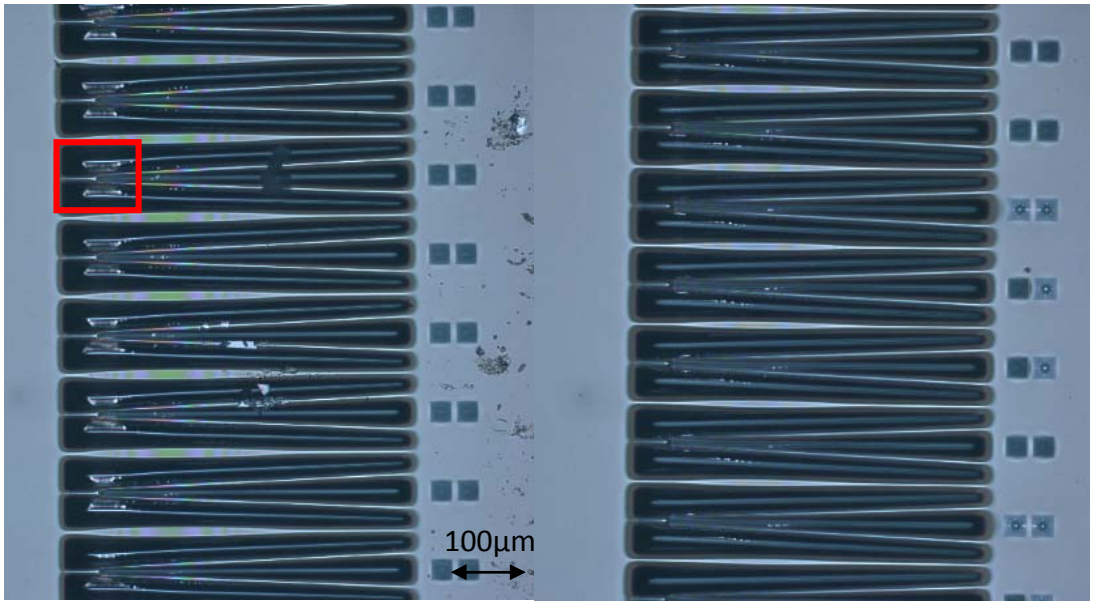

Figure 4.21 Crystallographic alignment forks after KOH etching that show symmetric patterns on the left and asymmetric on the right.

In order to minimise this error, crystallographic alignment marks were implemented using designs demonstrated by Mattias Vangbo and Ylva Backlund[65].

These structures (Figure 4.21) are 535µm long and 100µm wide, they show crystallographic alignment using symmetrical fork structures and are each rotated incrementally away from the crystal plane, in the example shown in Figure 4.23, each structure is rotated by 0.05°. The asymmetry observed is due to the angle of one fork tine being closer to the crystal plane than the other, causing the anisotropic etch to join the 110 planes sooner on the lower fork as seen in Figure 4.22. The mask design is shown in Figure 4.23. The mask is aligned to the flat of the wafer, which is aligned to the crystal plane ±1°, therefore enough forks are required to encompass this misalignment. As the structures used are incrementally rotated by 0.05°, 41 of them are required to cover the flat misalignment range of ±1°. That is 20 rotated positively and 20 rotated negatively with one at 0°. Each one had to be carefully positioned so that the focus point of all the structures is in one place and so they are evenly spaced to better visualise the symmetry of each structure compared to its neighbours.

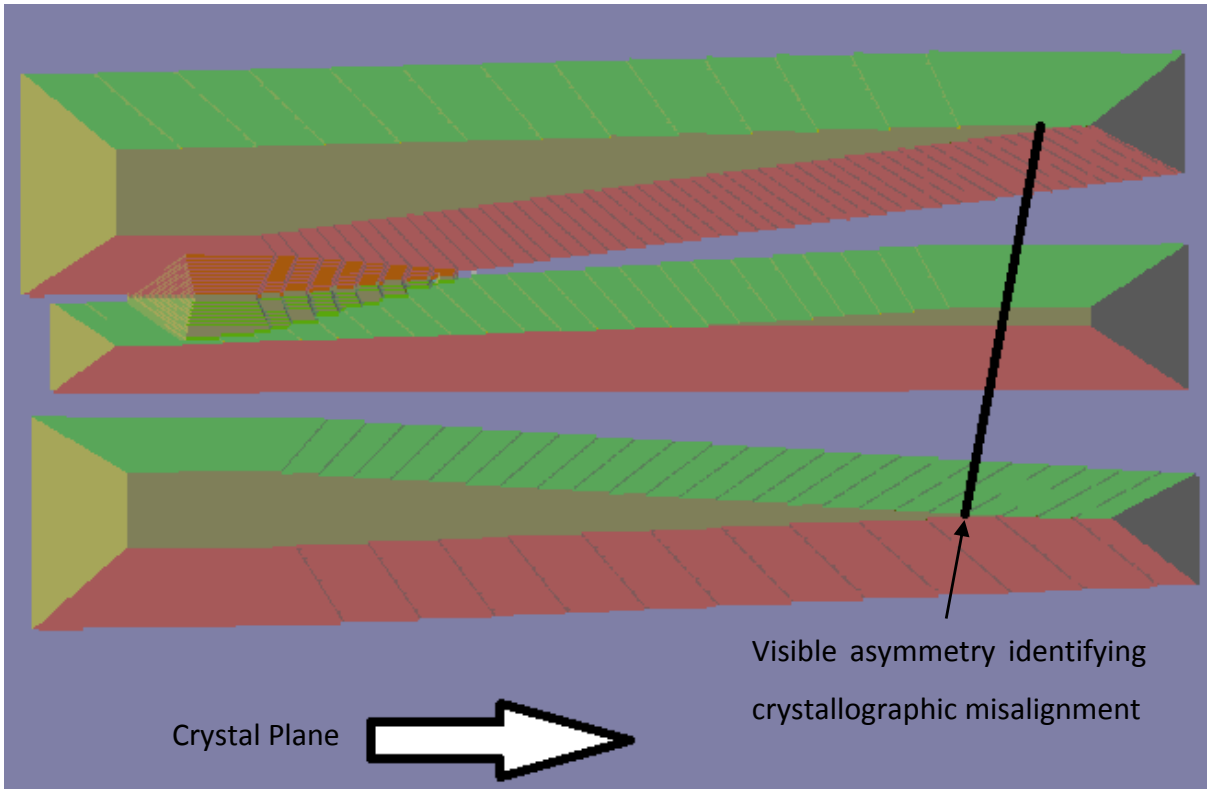

Figure 4.22 Simulated KOH etch of a crystallographic alignment fork rotated 2 degrees away from the crystal plane using ACES simulation tool

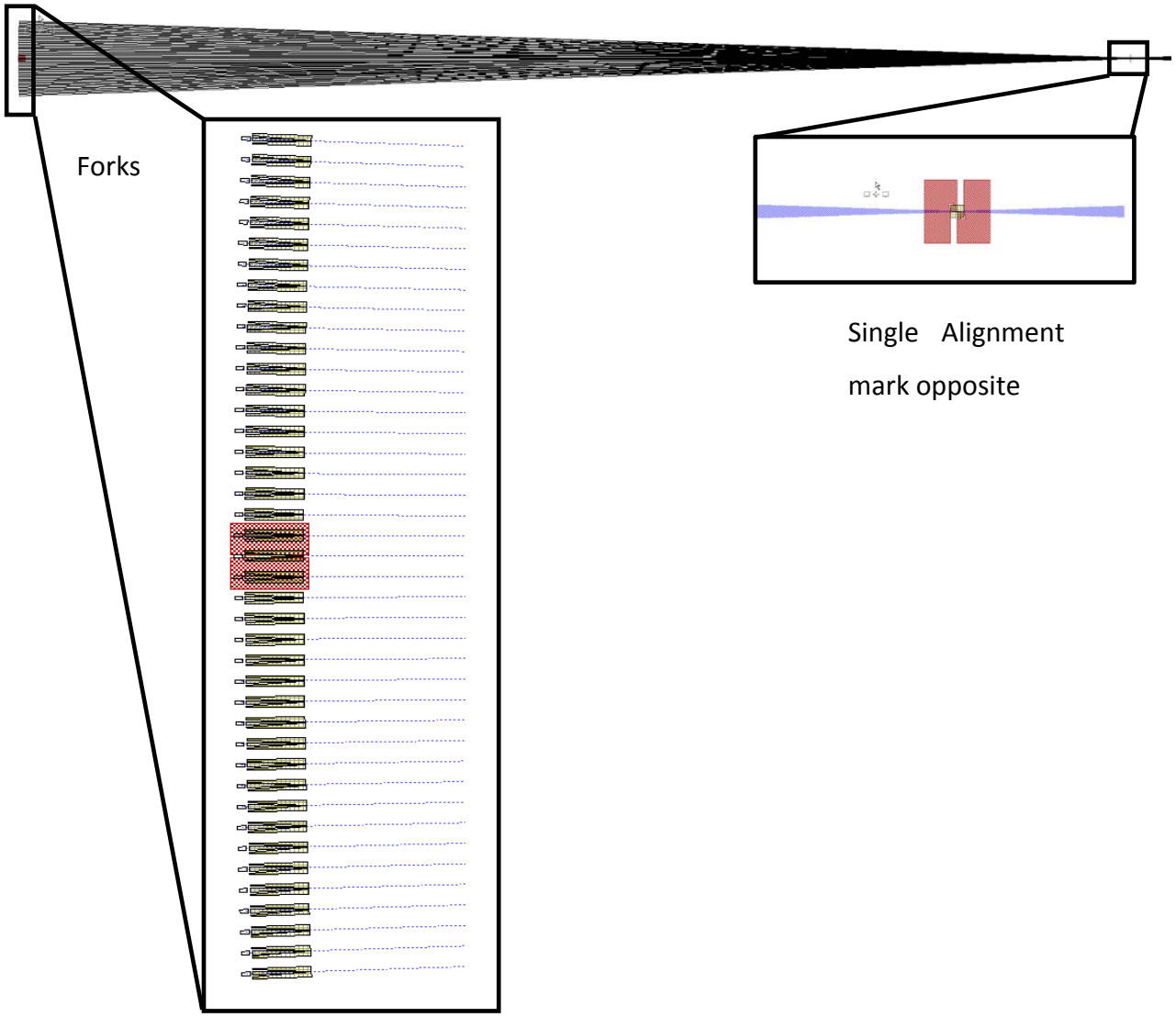

Figure 4.23 The LEdit cell showing the crystallographic alignment marks with lines added to show the focus point on the opposite side of the wafer.

Once these structures are defined in resist, a Si_3N_4 hard mask is dry etched. The wafer is then KOH etched to reveal the symmetry shown in Figure 4.21.

When producing the actual v-groove structures, the mask is aligned to these test alignment marks allowing ±0.05° accuracy.

OVER ETCH

When etching the Si_3N_4 as a mask for a KOH etch, any over etching translates to undercut during the KOH process (Figure 4.24). This changes the dimensions of the defined cavity. The undercut will affect each side of the structure and the change in dimensional size can be calculated using;

$$Dimension\ change = 2Uc = 2(Oe \cdot (\tan\theta)) \quad 4.3$$

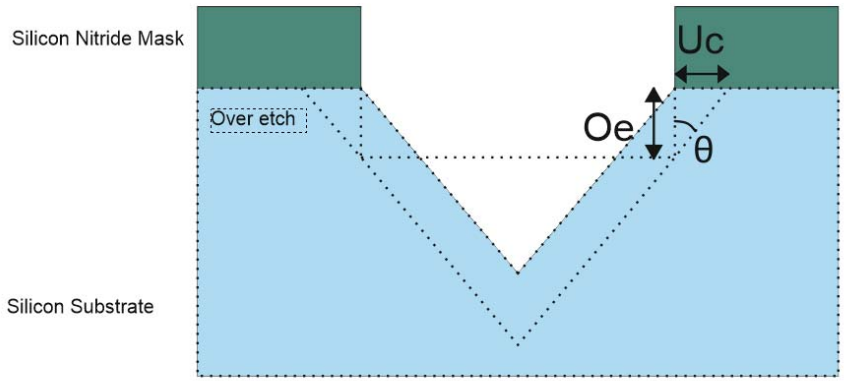

Figure 4.24 How over etching effects the v-groove structure.

Because of the nature of the (110) Si crystal plane, θ is always 35.3°. It can be surmised that, for every nanometre of over etch the v-groove will be 1.8nm wider and 1nm deeper. This makes it important to have a Si_3N_4 etch that accurately stops on the Si layer.

Nitride etch

Table 4.13 Fast Si_3N_4 ICPRIE Recipe.

Material	Tool	Gasses	Flow Rate (sccm)	ICP Power	RF Power (W)	Pressure (mTorr)	Temp (°C)
Si_3N_4 (Fast)	OIPT ICPRIE	SF_6/CHF_3	65/35	2000	80	14	20
Si_3N_4 (landing)	OIPT ICPRIE	CHF_3/O_2	77/4	0	175	22	20

Etching of the 4µm Si_3N_4 to create the KOH hard mask was initially conducted using a two stage process; the majority of the layer was etched using a fast etch (~450nm/m) that has poor selectivity to Si(0.2:1) (Table 4.13) and the remainder was etched using a landing etch, used to etch up to or “land” on the substrate. The landing etch has a relatively low rate (30-

40nm/m) and a selectivity to silicon of 4:1, reducing the potential for over etching. Figure 4.25 (left) shows an initial etch test that shows a higher etch rate in the corners which causes over etching at a rate of 33nm/s when using the fast Si_3N_4 recipe, due to its SF_6 based etch chemistry. As the plasma breaks through the nitride layer early, this high Si etch rate etches large holes. This is preventable by switching to the landing etch earlier, at the point shown in Figure 4.25 (right) before the Si_3N_4 has been compromised.

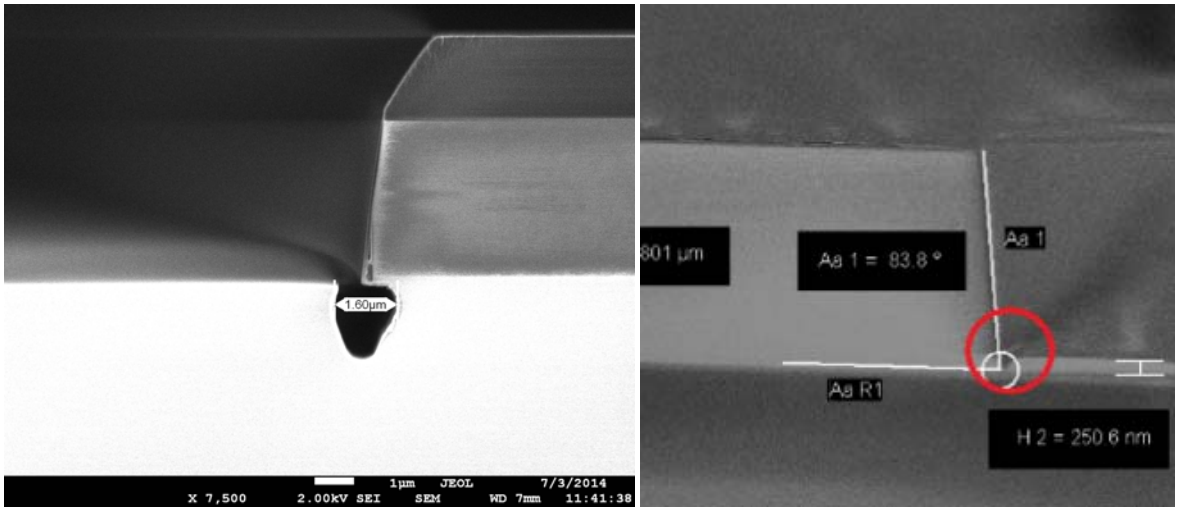

Figure 4.25 (Left) Large channel over etched at the silicon nitride edge. (Right) the point at which the nitride etch broke through at the edge prematurely.

It was found that the point at which the fast etch broke through was not predictable and the relatively selective landing etch was still not selective enough to prevent over etching of up to 500nm. It was therefore decided to use the landing etch process to fully etch the wafer. The disadvantage was that the etch would take around two and a half hours, but the results would be more reliable and accurate. This is not an indictment of the process, as a more appropriate etch could be used in an industrial environment, but reliability is essential for this proof of principle process. Initial tests showed problems with uniformity where the edge etched faster (35nm/m) than the centre (25nm/m) and the channels were not clearing completely. There was a possibility that polymer deposition was hindering the etch rate and so, increasing the O_2 in the chamber was considered as this should increase the polymer etching. Increasing the flow rate from 3sccm to 5sccm showed an inversion in the uniformity, 44nm/m at the edge and 39nm/m at the centre, and fortunately an increase in overall etch rate. By tuning the O_2 flow a uniform etch can be achieved which is defined within Table 4.10.

Further tuning is often required due to two factors; primarily, because the etch rate has been seen to be unstable between etches, the reasons for which are unclear although may be attributed to polymer build-up on the chamber walls, in which case only carefully controlled dedicated manufacturing processes will result in consistent etch rates and uniformities [66, 67]. Secondly, the purchased wafers have an inherent non uniformity in the Si_3N_4 layer of up to 80nm[68] the recipe must be tuned on a wafer by wafer basis to etch through the nitride across the wafer at the same time by periodically measuring the etch rates and adjusting the O_2 flow to maintain uniformity.

KOH Etch

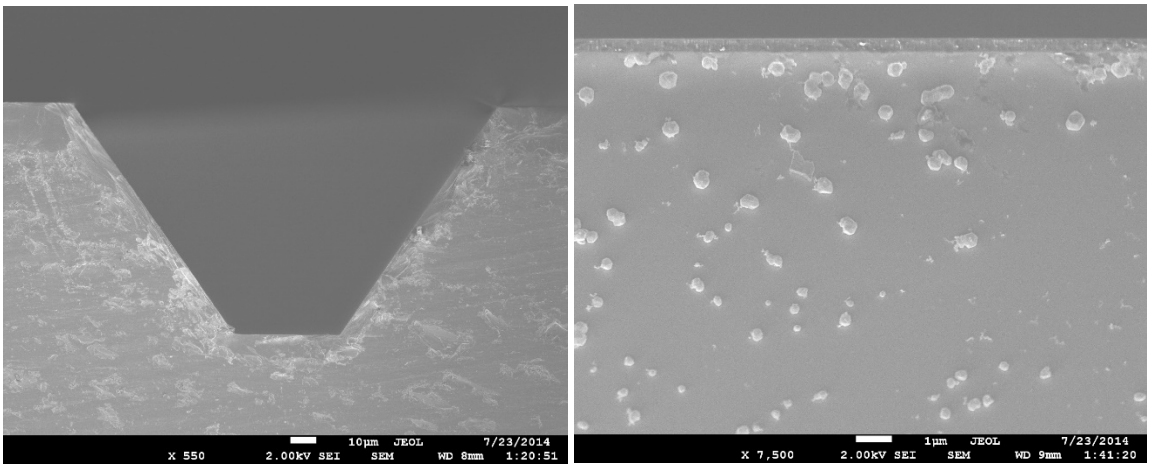

Figure 4.26 SEM images of (left) a cross section of a v-groove etched in KOH and (right) of the sidewall of a KOH etch facet showing ~500nm size particles assumed to be caused during dicing process.

Etching of the v-grooves (Figure 4.26 right) was performed using a 40% KOH solution heated to 80°Cwhile being agitated a bubbler to remove nitrogen bubbles that form on the etched surface (Table 4.11). The KOH etch was a mature process in the Southampton cleanroom and was not problematic, although the roughness and optical characteristics of the sidewall were not investigated as changes to the etch process are not possible due the effect on other cleanroom users and it was believed that other areas of the project were more critical with the time constraints. There are ways to reduce roughness; agitation by ultrasonic means can dislodge the nitrogen bubbles generated on the etched surface[69] however this requires specialised equipment which would be time consuming to acquire and develop the process. Surface roughness may be an issue in the future (Figure 4.26 right). However, metallisation is likely to affect the roughness in some way and will need to be investigated at the same time.

If the KOH etch process cannot be developed to within desirable tolerances, Tetramethylammonium hydroxide (TMAH) can be used to complete a similar process with the added advantage of having no metal ions.

PLUG UNDERCUT

An initial oversight in understanding the KOH etch lead to undercut of the plugs, initially the lack of plugs after KOH etching was put down to poor development of the soft mask as the plugs were not checked after the dry etch stage. Once it was confirmed that the plugs were still present prior to KOH etching, simulations were carried out using Anisotropic Crystalline Etching Simulation (ACES)[70] to confirm that undercut occurred due to the (111) plane being open to the KOH as shown in table 2.7. This prompted a change in process flow as the plug protection process would now have to happen before the KOH process. The fabrication of this will be discussed in section 4.3.5.

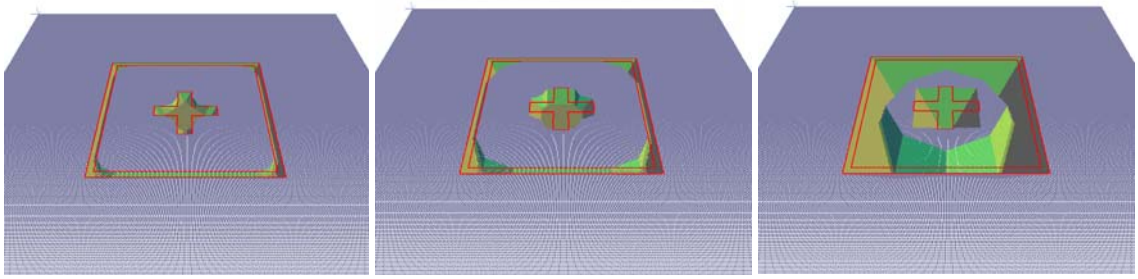

Figure 4.27 KOH etch model showing undercut of the nitride plugs using ACES wet etch modeling software [53]

4.3.5: Plug Protection Fabrication

The discovery of the plug under etch made the plug protect process more complex. The plugs would have to be protected during the KOH etch as well as the nitride strip. SiO_2 can still be used albeit with a faster etch rate in KOH than in H_3PO_4. To try and reduce process complexity a single deposition of SiO_2 is used to protect the plugs from both hot phosphoric and KOH. In order to identify the thickness that the SiO_2 mask layer needs to be, a selectivity test was carried out (Table 4.14). PECVD SiO_2, LPCVD Si_3N_4 and Si were all etched in both orthophosphoric acid and KOH to identify their respective etch rates. This table shows an SiO_2 mask thickness of 1µm will be more than enough to protect the plugs through both KOH and orthophosphoric etching.

Table 4.14 Etch rates of SiO_2 Si_3N_4 and Si in KOH and orthophosphoric acid.

Material	Rate in KOH	Rate in H_3PO_4 (nm/h)
SiO_2	12Å/m	20
Si_3N_4	<1Å/m	100
Si	1.4um/m (100)	2

To reduce time in developing the new process, rather than obtaining a new mask, e-beam was used to write the plug protect pattern. There was only sufficient time to attempt this process once and a mistake was made when aligning the layers and the plug protect pattern was written away from the plugs. Even with this misalignment, the completion of the process shows that without this misalignment, the plugs would be protected.

The etch rate for the Si_3N_4 in orthophosphoric is 100nm/h this means that potentially 40 hours are required to complete the strip. A shorter time would be desirable and this slow rate is possibly due to the lower temperature achieved in the tank compared to examples in literature [49]. According to this the best case would be an etch time of around 24 hours at a temperature of 160°C however further selectivity tests would be required.

Attempts to strip the Si_3N_4 for long periods resulted in failure as the chiller used to condense the evaporated water vapour over heated as it does not meet the specification for the system. The system is currently being upgraded to use the PCW (Process Cooling Water) system which will have a much high thermal capacity and should allow high temperature processing for long periods of time.

4.3.6: Pyramid structures

Pyramid structures were trialled to determine their viability for fibre support as they could have minimal footprint, reducing the rotation undercut effect while also not requiring extra fabrication steps like segmented v-grooves which will be discussed in future work. This was prior to finding out the undercut issue with the plugs and the problem probably should have been identified at this point. The trial was carried out and Figure 4.28 shows how the square

mask is under cut, by the time the etch is deep enough to accommodate a fibre the mask is completely under cut and the support structures are compromised.

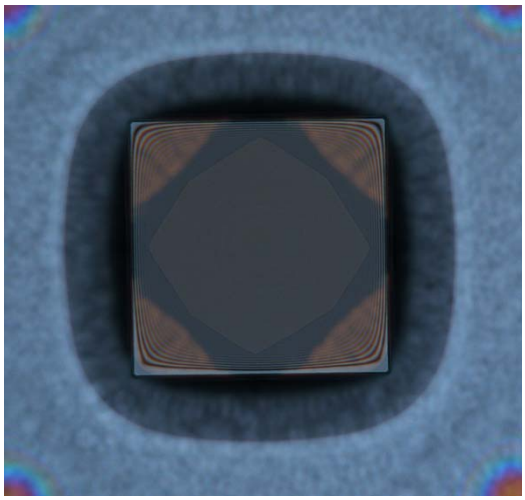

Figure 4.28 Pyramid structures trialled for fibre positioning and support showing under etching of the (111) plane

4.3.7: Final Process Flow

At the conclusion of the project the process flow had evolved to solve development issues during its course. The finalised process flow in Table 4.15 depicts how the v-grooves and plugs are produced.

Table 4.15 The finalised process flow incorporating the changes in process compared to the table produced at the start of the project.

Wafer	Location	Identifier	CA Marks								Nitride Trenches an Plugs							Plug Protect, KOH, Strip									
			AZ9260 Spin	Bake	Rest	Expose	Develop	Nitride Etch	Ash	KOH Etch	AZ9260 Spin	Bake	Rest	Expose	Develop	Nitride Etch	Ash	SiO2 Dep	AZ2070 Spin	Bake	E-spacer	E-beam	Develop	HF etch	Ash	KOH Etch	Orthophos	HF Strip

4.4: Grating Coupler Design

As the coupling conditions for the packaging solution are unique, a grating coupler must be designed to couple light between fibre and waveguide. Due to the angle created by the KOH etch at the end of the v-groove a mirror is where the silicon will reflect planar light back on itself with an angle of 19.5° incident to the sample surface, as shown in Figure 4.29. The mirror can be improved with the deposition of metal on the silicon surface however this will not affect the angle used to design the grating coupler. the grating coupler can either coupled the light back on itself again or be coupled in a forward direction. Using a forward coupler can only be accomplished if the fibre is not recessed into the optical chip, the advantages for which outweigh the potentially non-existent efficiency gains from a forward coupler.

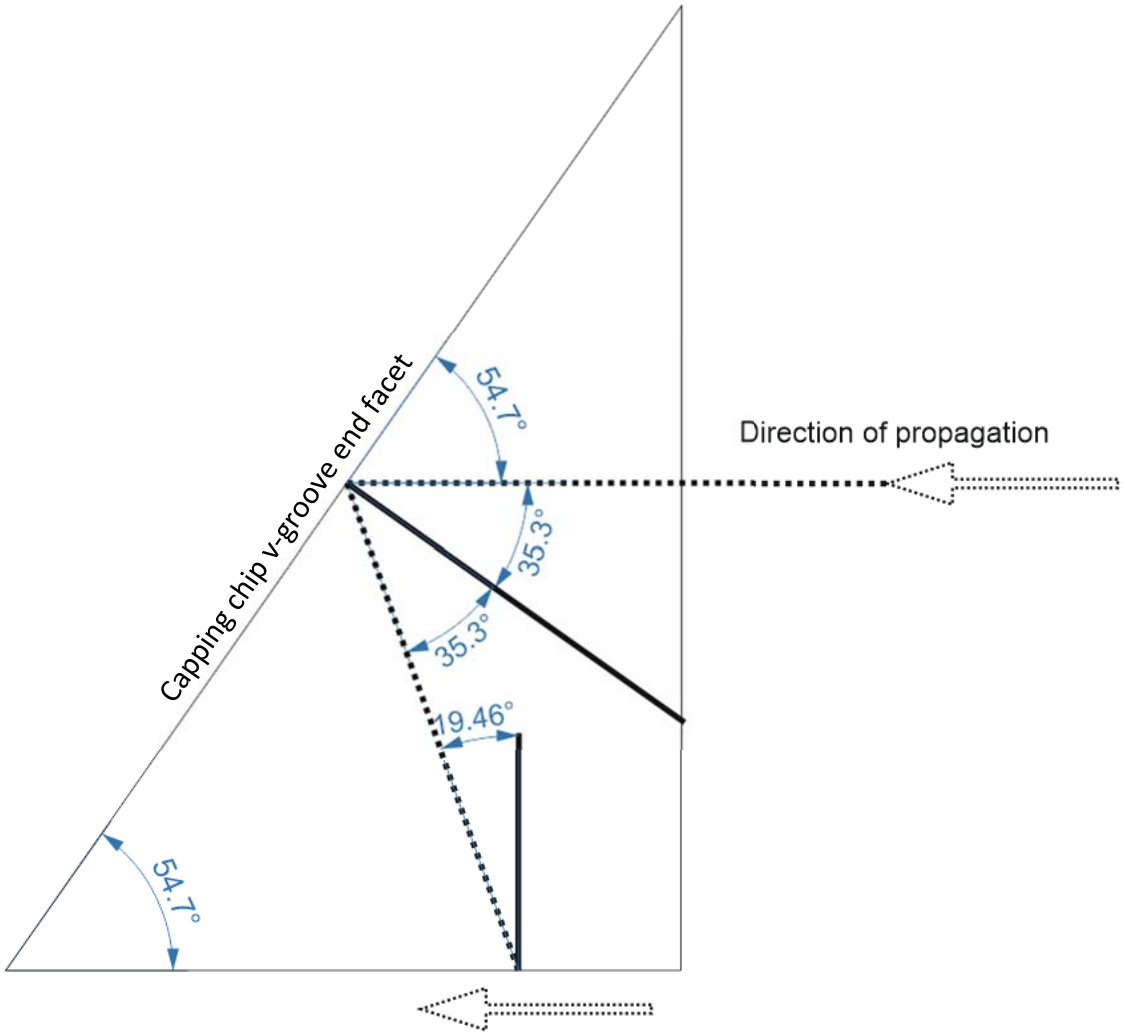

Figure 4.29 A diagram showing how light will be reflected from the capping chip mirror, resulting in a 19.5° coupling angle in the reverse direction.

4.4.1: Uniform Grating Couplers

Uniform gratings are grating couplers that maintain the same period and aspect ratio along their length (Figure 4.30) and are relatively simple to design.

Using the equations outlined in section 2.2.2 an initial period was devised. However, the period equation is a function of aspect ratio which can affect efficiency. In order to define a grating which meets the phase match condition and also has the best efficiency, finite difference time domain (FDTD) simulation software is used. In this case Lumerical FDTD software was used with the help of Dr Robert Topley. Particle swarm optimisation (PSO) was utilised to simulate many different fill factors and periods. PSO is a population based stochastic optimisation technique, in basic terms, the simulation tool randomly generates a set of simulations based on parameters within a set range[71]. This produces a single generation, the results from which are used in following generations to optimise results towards desired criteria.

For the simulation the pitch range was set between 400nm and 700nm, and the fill factor range was between 0.2 and 0.8. the simulation was also based on a fixed etch depth of 220nm dictated by the rib waveguide design, a centre wavelength of 1550nm, a BOX thickness of 2µm and approach angle (θ_a) of -20°. One component which was not optimal was the source condition; bespoke conditions are required as the relatively long propagation between coupler and fibre makes the mode field profile different from a typical scenario where the fibre is directly above the grating coupler. This may have affected the results and was addressed when producing the non-uniform gratings described in the next section.

The figure of merit used to optimise the grating coupler was the average transmission over a range of wavelengths centred around 1550nm. The results gave an optimised grating coupler with a period of 496nm and an aspect ratio of 0.4.

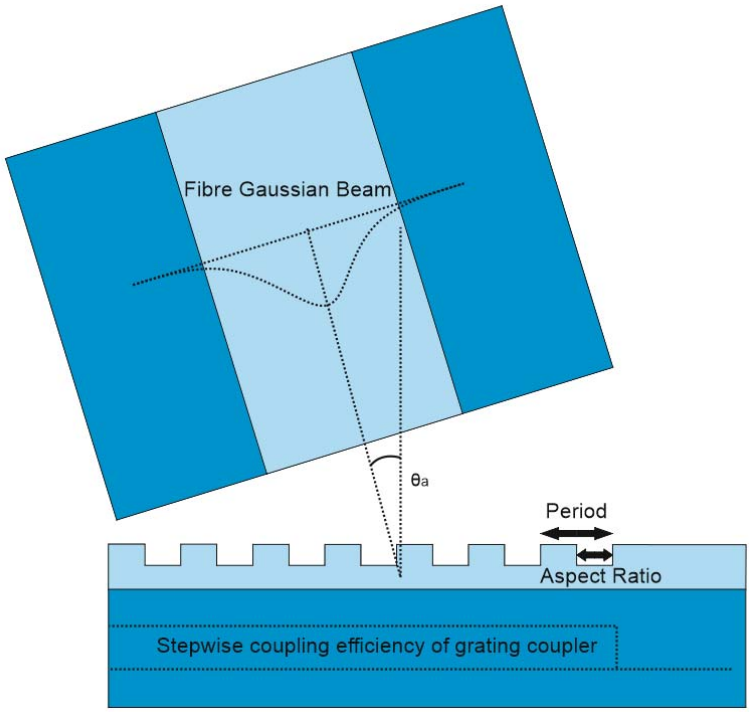

Figure 4.30 A schematic diagram of a uniform grating coupler with a fibre set to an angle to avoid back reflections.

50 different grating couplers were fabricated and capped with a 1µm layer of SiO_2 where the gratings pitch and aspect ratio varied in order to mitigate manufacturing tolerances. Because the grating couplers were being measured from a non-planar fibre and the measurement set up cannot accommodate -20° the coupler had to be rotated by 180° with respect to the direction light is propagating from the fibre, which is due to the couplers reverse coupling characteristics. 180° bends were used to bring the waveguide round to propagate across to the opposite coupler as shown in

Figure 4.31. This configuration allows the fibre angle on the measurement set up to be +20° while maintaining a reverse coupling direction.

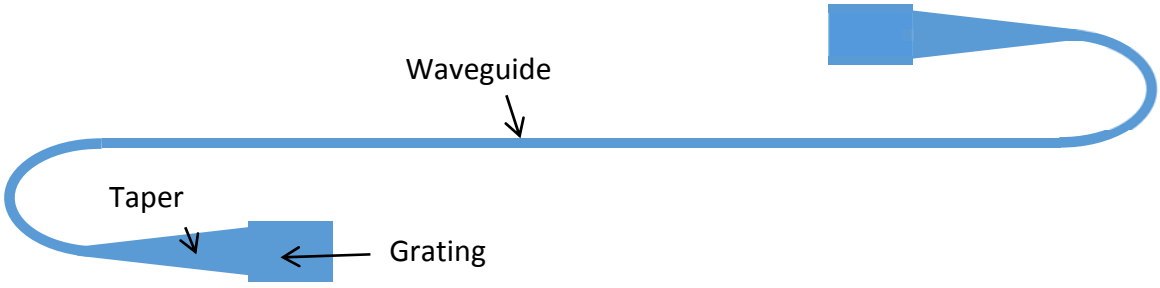

Figure 4.31 The reverse coupled grating couplers configured for coupling with out of plane fibres.

When measured, the grating couplers showed a normalised loss of around 5dB per coupler (Figure 4.30) where L25 is the 25th coupler on the left hand side of the measured sample. In order to normalise the loss to a single grating coupler, loss structures were also produced on the samples to isolate losses from bends, waveguide propagation and tapering. 5dB is higher than expected so they were observed using a scanning electron microscope (SEM) it was discovered that the grating couplers were not what was expected as shown in Figure 4.33. The actual period was 483nm with an aspect ratio of 0.45.

This error can be attributed to poor resist development or other errors in production. It is worth noting that the grating couplers that were designed for a more traditional 10° coupling angle and had proved to have typical losses of 4-5dB, were significantly wavelength shifted and lossy, so problems in fabrication are apparent.

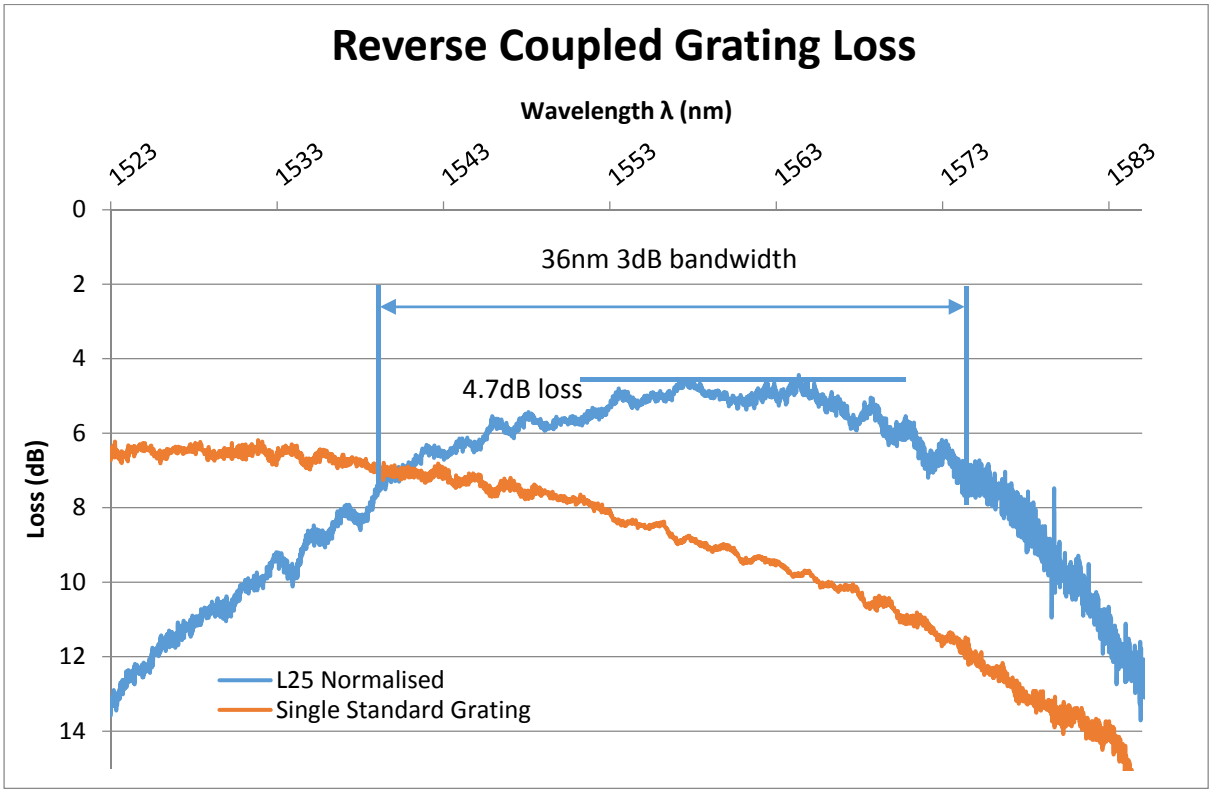

Figure 4.32 A graph showing the normalised grating coupler loss for gratings with a period of 483nm and aspect ratio of 0.45 measured with a fibre angle of -20° (L25) and a standard uniform grating coupler measured at 10°.

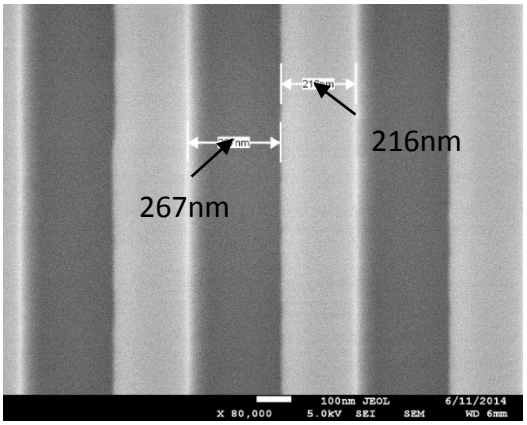

Figure 4.33 An SEM image of a grating coupler showing a period of 483nm and aspect ratio of 0.45.

4.4.2: Apodized Grating Couplers

Improvements in the grating design where completed by Nathan Soper, who developed a one dimensional apodized design based on work by X. Chen et al [20] where the aspect ratio of the first five periods are changed to shape the coupling efficiency along the length of the coupler to better match the (near) Gaussian beam of the fibre Figure 4.34.

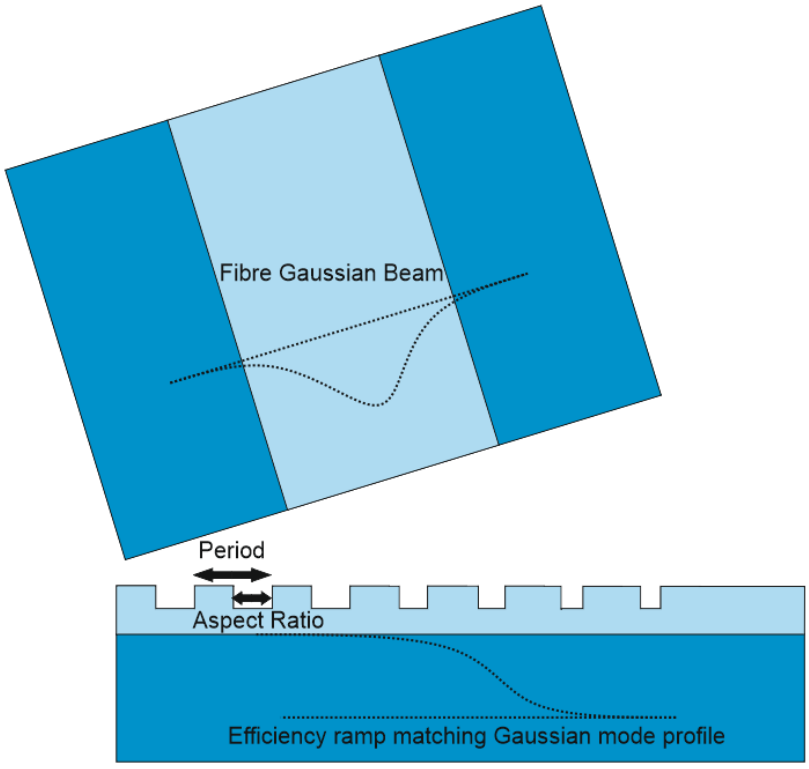

Figure 4.34 a schematic diagram showing the Gaussian mode field profile of the fibre and how an apodized grating coupler tries to match it.

Simulated results shown in Figure 4.35 display a peak efficiency of 68% or a loss of 1.67dB. These gratings have been measured and the results show a loss of 2.69 dB which is a vast

improvement of 37% compared to the uniform couplers measured previously, but still lower than simulations, so improvements are still possible.

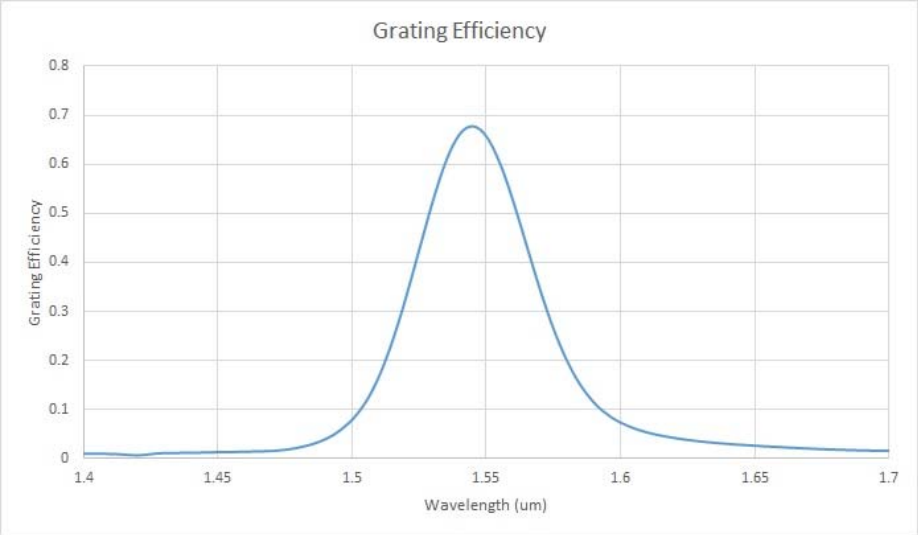

Figure 4.35 A graph showing the simulated grating coupler efficiency of 68%

There is more work to be done to improve the grating couplers, although the couplers produced here are adequate to prove the packaging concept.

4.5: Fabrication Discussion

A complete design and characterised process flow was the main goal for this project, in the pursuit of this there were many trials. A particularly difficult aspect was dry etch characterisation in the reactive ion etch (RIE) tools as discussed previously in section 4.4.

In many cases whilst developing processes, in order to keep to time constraints there was an element of having to utilise processes that weren't fully optimised, or to use processes that were designed for a similar purpose. If time was not a concern, then many of the processes would have been refined to meet their requirements better more exactly. This takes more time than it would appear as, for example in the process of photolithography, if the thickness of resist is changed then the dose, baking and development recipes all need to be tuned accordingly more than likely requiring a DOE.

A large amount of time restriction was due to the lack of reliability in the cleanroom equipment. As the tools are complex, when they break down it can be for a long period of time and causing a significant bottleneck. During the course of this project the inductively

coupled reactive ion etcher (ICPRIE) went offline for several months at a time, seeing as it held an integral part of both process flows it was particularly disruptive. In addition, the wet room was deemed unsafe late on in the project and was completely replaced causing significant delay. The deep silicon etcher (DSE) was also a problematic tool as it was replaced around the project's midpoint and had a number of long inoperable periods as the chiller broke down.

Regardless of delays, once the processes had been developed individually they had to be completed in two parallel process flows, producing two samples ready for assembly. When attempting to complete the process flows in order, a number of unexpected developments required adjustment of the recipes and the order they took place in. The processing involved for each sample had a particular problem that arose very late in the project as they only became apparent in the final stages of wafer production. For the device wafer it was the discovery of a silicon dioxide (SiO_2) layer on the backside of the wafer which had both negative and positive connotations, where it could be used to prevent etching of the edge of the wafer during the through wafer etch, however it was a very late stage to change the order of processing and was therefore, rather rushed. This did not prevent the completion of the wafer and the process flow has been proven to work.

In the case of the capping wafer, an oversight in not determining that the alignment plugs where being under etched during the KOH process caused a significant change in the process order. As the affected processes used photolithographic masks, and there wasn't enough time to order new ones a final attempt was made using e-beam lithography which failed due to an error in the alignment calculations. Carrying out the final process steps with this misalignment does still show that the "plug protect" process works and once the calculations are corrected, and a new fabrication run is attempted the whole process flow should work.

Chapter 5: Summary, Conclusion and Future Work

5.1: Summary and Conclusion

As silicon photonics penetrates into mass market applications, for example, deeper in to the datacentre architecture and/or closer to the home, packaging is going to become a key component in driving down costs and maximising efficiency. The literature is yet to show an efficient packaging solution for the future, however potential has been shown and key ideals have been identified. Passive alignment is a highly desirable concept as it reduces the complexity and time required for assembly, and consequently is the only realistic way in which costs can be sufficiently low for some mass market applications. Also, in plane methodologies allow robust assemblies with a low profile which will save space and increase durability.

This project tackles the key issues for packaging, producing a design that has the potential for passive alignment of multiple fibres in a planar assembly. The design is made up of two silicon chips; the first being a photonic chip that would contain the silicon photonic devices/circuits, and the second which serves as a capping chip securing and positioning input and output fibres.

When brought together the chips self-locate, using self-aligned plugs on the capping chip which marry to through wafer etched holes in the device chip. The capping chip employs silicon v-grooves to hold the fibres in an accurate position while the end of the v-groove works operates as a mirror, reflecting light from fibre to chip and vice versa. The coupling of light from fibre to waveguide is performed by grating couplers for their relatively low alignment tolerance eases the demands on alignment accuracy. The self-aligned structures have been designed to reduce the demands on fabrication tolerance and where this is not possible, high accuracy lithography can be used to maintain precision.

When etching the through wafer alignment holes on the optical chip, a trench is etched where the fibre is held, and the advantages for this are threefold.: Firstly, a portion of the fibre

cladding can be embedded into the silicon, below the surface of the optical chip, reducing the propagation distance to the grating, and therefore the divergence of the propagating mode. Secondly it allows fibre population to take place after the assembly of the samples two chips opening up possibilities for wafer scale assembly through either pick and place of the capping chip, or via wafer to wafer bonding. The final advantage comes in the form of visibility during assembly as the plugs can be viewed and aligned from the back of the device chip. As a majority of the through wafer etch was completed through the backside of the wafer, there is an opportunity to etch underneath the grating coupler and improve its efficiency using a backside reflector.

To quantify what has been developed during the course of this work, the following paragraphs will identify what has been achieved.

While creating the optical wafer, removal of SiO_2 from the backside of the SOI wafer was performed, while preserving a bead of SiO_2 around the edge maintaining the seal between wafer and clamp while being deep etched.

The optical design incorporates bespoke grating couplers that take in to account a mode field with an approach angle of -20° and its divergence due to propagation over 50µm. These grating couplers have been shown to have losses of the order of 2.7dB. There are also loss structures that allow normalisation of the grating couplers and will identify the added penalty of the assembled package.

A hybrid lithography process combines the accuracy of e-beam lithography and the speed of contact lithography to produce an accurate masking layer in thick resist that is used to dry etch through 3µm of oxide and 400nm of silicon which defines the trench that the fibre will sit in.

A contact lithography mask is used to etch through the entirety of the wafer and is defined on the backside, aligned to the previously etched trenches on the front side.

For the capping wafer, crystallographic alignment was achieved by etching symmetrical forks in to the thick nitride mask, these were then KOH etched revealing asymmetric patterns where the forks were not aligned to the crystal plane. These structures allowed precision

alignment to the crystal plane ±0.05°. Once the alignment was found, a v-groove mask was aligned and etched using the same process used to create the alignment marks.

In order to etch the Si_3N_4 mask a new etch needed to be characterised for etching through 4µm of Si_3N_4 while maintaining selectivity to both Si and soft mask resist. Multiple etch processes were attempted using a combination of non-selective etches and a landing etch, however complications prevented this process from working and so a slow, selective etch was used. This etch takes over an hour to complete but the high selectivity to Si makes it worth the time.

The alignment plugs used to mate the capping chip with the optical chip are defined at the same time as the v-grooves, and are formed from the Si_3N_4 hard mask. This allows for highly precise positioning with respect to the fibres that are supported by the v-groove. As the rest of the hard mask needs to be stripped, the plugs must be preserved so they remain after the stripping process. This was the only process that was not completed successfully as explained previously and it is expected to be completed in the short term.

In conclusion, the main challenge of this project was to design and characterise a complete process flow, involving fifty-five process steps, most of which were developed from scratch and some of these steps, to the knowledge of the author, have never been completed before, especially in the Southampton cleanroom. Specifically, a 4µm Si_3N_4 dry etch and the hybrid lithography process, which are explained in detail in Chapter 4. Delays have reduced the rate of progress a little, but the vast majority of the process flow has been demonstrated. and completion of the final steps is imminent. Nevertheless, sufficient progress has been made to determine that the process will be successful and the accumulated errors are small. Consequently, it can be concluded that a viable self-aligned process can be developed from the ideas upon which this project is based. Once complete the processing will open up the possibility for passively aligned packaging with a predicted added loss of less than 2dB where added loss is the loss produced by the packaging process alone (fibre misalignment and mirror reflection). The parts can be assembled with minimal labour requirements and can potentially be assembled at a wafer scale, maximising throughput and reducing costs. In effect, this facilitates packaging for mass markets.

5.2: Future Work

5.2.1: Segmented V Grooves

As mentioned in chapter 4 section 4.2.2, the crystallographic alignment of the v-grooves is critical in maintaining accurate dimensions. The resulting error is a function of the size of the v-groove and so, longer v-grooves will induce a larger error. By segmenting the v grooves the effect of the crystallographic misalignment is drastically reduced because each individual segment is significantly smaller than its whole and the error will be reduced as such. This can be seen in Figure 5.1 where a 9mm long v-groove is rotated by 1°. The figure shows that by dividing the v-groove in to its smallest possible segments a 97% improvement is observed. An additional etch step is required to allow the fibre to sit in the trench, but will require minimal accuracy.

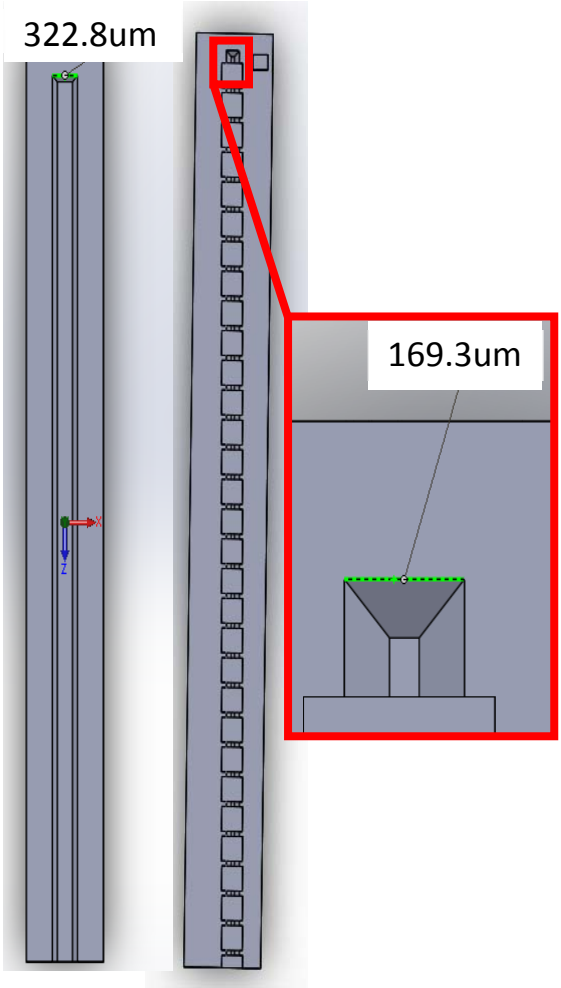

Figure 5.1 A diagram showing how segmented v-grooves can minimise the effect of crystallographic misalignment. Both v-grooves represent a groove defined as 9mm long and 165.8µm wide, rotated 1° away from the crystal plane. This is an exaggeration to display the effect.

5.2.2: Mirror Improvement

The optical characteristics of the mirror were not investigated, and this will be required in future work. The facet quality can only foreseeably be obtained as part of the packaging design as a whole, however once the parts are assembled this can be ascertained and probably improved upon.

As part of the original design, metallisation of the mirror was expected to improve efficiency. Metallisation processes are mature in the Southampton cleanroom and metal deposition and patterning is likely to be a straightforward process.

The roughness of the facet produced by the KOH etch may also be investigated and the literature shows there are methods that can improve the quality of the etch, such as adding isopropanol to reduce surface tension and in turn reducing the formation of nitrogen bubbles [54].

5.2.3: Assembly

The assembly process aligned least to the author's conventional technical expertise of a university group, and consequently it was decided that a collaboration was best in order to complete the assembly process. The packaging company Optocap were approached for their wide knowledge of packaging optical components. Designs for assembly processing have been discussed, however these are company confidential. At the time of writing this thesis, refined process development is underway and assembly of samples is expected to take place within quarter 1 of 2016.

In order to comply with assembly specifications some design changes are required. Most of the mask designs were made from the perspective of process development and not with real world scenarios in mind. This, however, will not affect the processing steps that have been developed during the course of the project.

5.2.4: Wafer Scale Assembly

The addition of through wafer etching made wafer scale assembly an option. A review of wafer scale bonding techniques shows that sub-micron accuracy could be obtained. With some adaptations to make the plugs self-positioning, wafer scale assembly is a foreseeable option [55]. Further to this, discussions with Optocap support the theory as they have contact with a company that have completed similar processes for microfluidic wafer scale structures.

Wafer scale assembly allows for a more efficient assembly process, the time saved can be used to allow higher precision alignment or reduce production time as whole.

5.2.5: Etching of Redundant V Groove Mirror

Only a small portion of the end facet of the v groove is used as a mirror, in fact the rest of the angled facet is a hindrance as it prevents the fibre end facet from being closer to the grating coupler. A portion of the side wall could be etched away, creating a cavity, and allowing for the fibre to move further forward. This reduces the distance that the light needs to travel between the fibre and grating, reducing divergence and improving efficiency even further. This etch process is compatible with the relief etch mentioned previously for segmented v-grooves therefore this work will be completed in parallel.

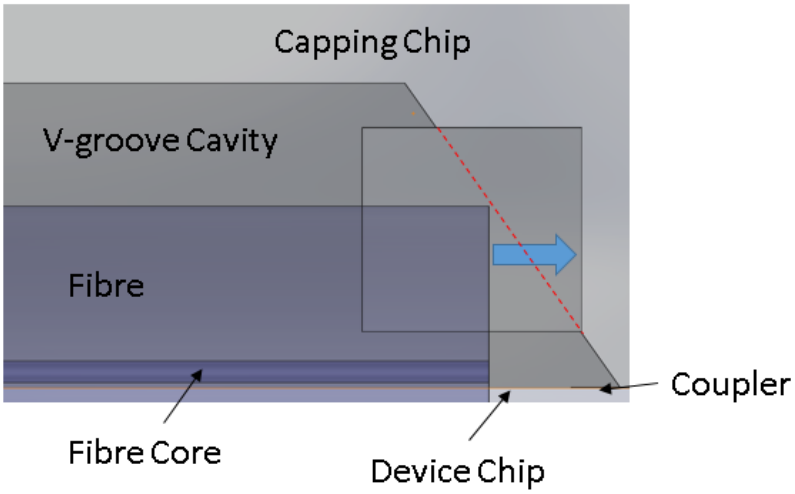

Figure 5.2 A schematic diagram depicting how removal of the redundant mirror could move the fibre closer to the grating coupler, reducing divergence.

5.2.6: Grating Coupler Improvements

The figure of merit for packaging is the additional loss caused by the packaging method, therefore it can be perceived that the coupling method would not be part of that figure as coupling is required either way. That being said, this packaging solution induces unusual grating coupler design rules compared to normal circumstances and to truly design a competitive solution the whole system loss must be reduced to an absolute minimum.

As mentioned in chapter 1, there are a number of ways to improve grating coupler efficiency. As the approach angle is unusual, new designs are necessary to maximise efficiency. Some progress has been made towards this over the course of the work, however the backside etch can be used to create backside mirrors without the extra complex processing that is usually

required where W. S. Zaoui et al have shown that a simple backside metal mirror can improve the efficiency of a uniform grating from 47% to 69%. Polarisation diversity and focused gratings can also be addressed, along with continuing to improve the more simplistic designs completed so far.

5.2.7: Silicon Nitride Deposition

The thick nitride layer is an integral part of this packaging concept, control over its thickness would be desirable when assembling samples or wafers to determine how secure and accurate the alignment can be. As the wafers used were purchased, a Si_3N_4 LPCVD process would be required to run large experiments with different thicknesses, wafers purchased with this level of customisation would be too expensive.

5.2.8: Minor Improvements

Lithography Improvement

Some of the lithographic processes are used for their convenience rather than compatibility with this work e.g. the spun photoresist is often thicker than required or exposure recipes may not be optimised. Further optimisation allows for a greater level of accuracy in the longer term as thinner photoresists generally maintain a better resolution, especially in the e-beam.

Improvement of Both Dry and Wet Silicon Nitride (Si_3N_4) Etches

The Si_3N_4 etches in hot phosphoric acid and the ICPRIE are slower than desired. Work can be carried out to try and increase the etch rates while maintaining selectivity. In the case of the dry etch, the sidewall profile may need to be controllable to allow the plug structures to self-locate when assembly occurs, therefore an etch study to adjust the sidewall angle is desirable.

Larger Plugs

Initial talks with the packaging company, Optocap has identified that the thickness of the plugs may be smaller than ideal. Investigation to either increase the Si_3N_4 thickness or an additive process where thick photoresist is defined on top of the nitride plugs is likely to need investigating.

Further stability

Optocap also suggested adding holes through the entire assembly that can be filled with adhesive, creating a much more stable assembly.

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Appendix 1. Process Flow Diagram