# Conduction mechanisms in Pt/$TiO_2$/Pt memristors

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Resistive random access memories (RRAMs) receive increasing attention as very promising candidates for the next generation of nonvolatile memories[1], as well as for artificial neuronetworks[2] and reconfigurable systems[3] developments. A key feature for the aforementioned applications is their ability to obtain multiple resistive levels by proper tuning of the biasing schemes[4]. Therefore, clarification of the dominant conduction mechanism, which remains to date a topic of debate, is of a paramount importance. This strongly depends on the device characteristics (oxide and electrodes' materials[5]) and the programming bias schemes.

This work aims to identify the conduction mechanism during switching operation of Pt/$TiO_2$/Pt stack. For this, three identical devices were electroformed and programmed to different resistive level (Fig. 1.a), by using a pulsing-based and compliance-free forming protocol. For each attained resistive state, the current voltage characteristics (I-V) were recorded and analyzed at different temperatures (Fig. 1.b). This analysis allowed extraction of the signature plots (Fig. 1.c) revealing the dominating transport mechanism. The results suggest that switching occurs due to gradual modification of the interfacial barriers (Fig. 1.d), during biasing. This study demonstrates the importance of interface engineering in performance optimization of the devices.

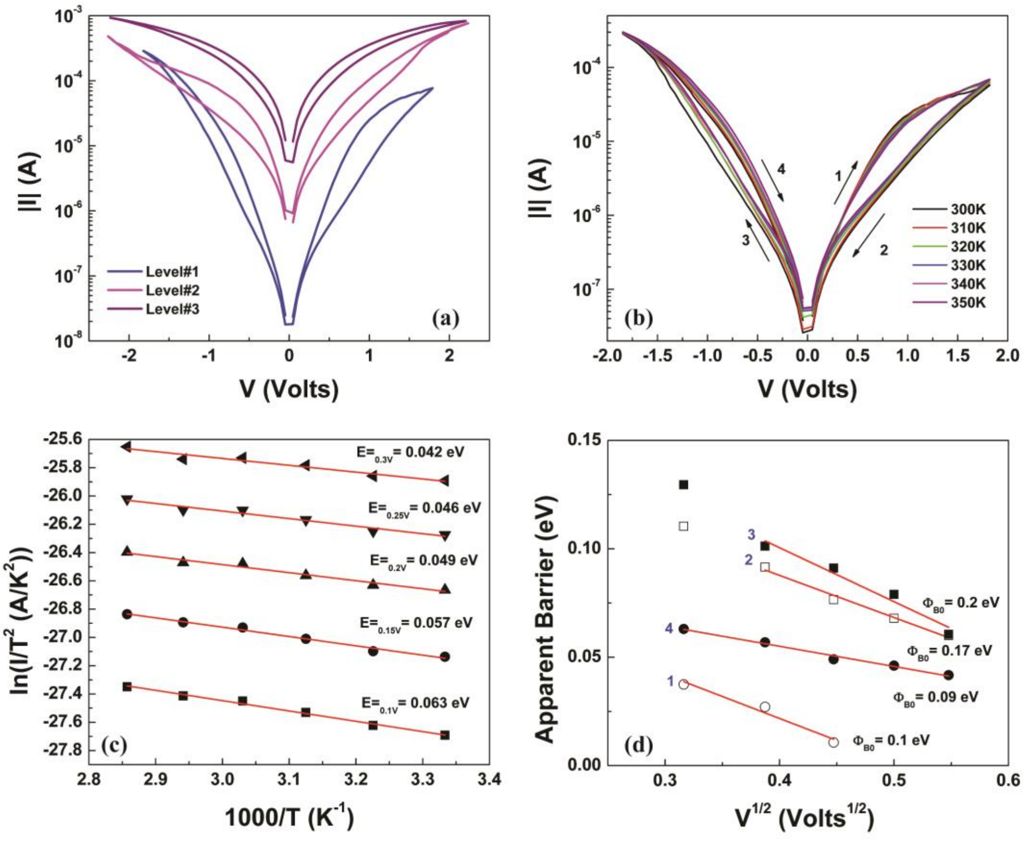


**Figure 1**: Electroforming may bring the device to different resistive states (a). Recording of the I-Vs versus temperature "Level#1 device" (b) allows the extraction of signature plots (c) that lead to identification of the dominant transport mechanism, in this case interface controlled (d).

## References

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