Power-Neutral Performance Scaling for Self-powered Multicore Computing Systems

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Introduction

Due to recent developments in runtime management, **multicore systems** are able to outperform single-core systems in both power consumption and performance.

As such, **heterogeneous multiprocessor system-on-chips (MP-SoCs)** are rapidly becoming the de-facto technology for powering modern, high-performance embedded devices.

Motivated by the limited device lifetimes achievable when using batteries, research has recently looked at replacing batteries and using **energy harvested** from the environment.

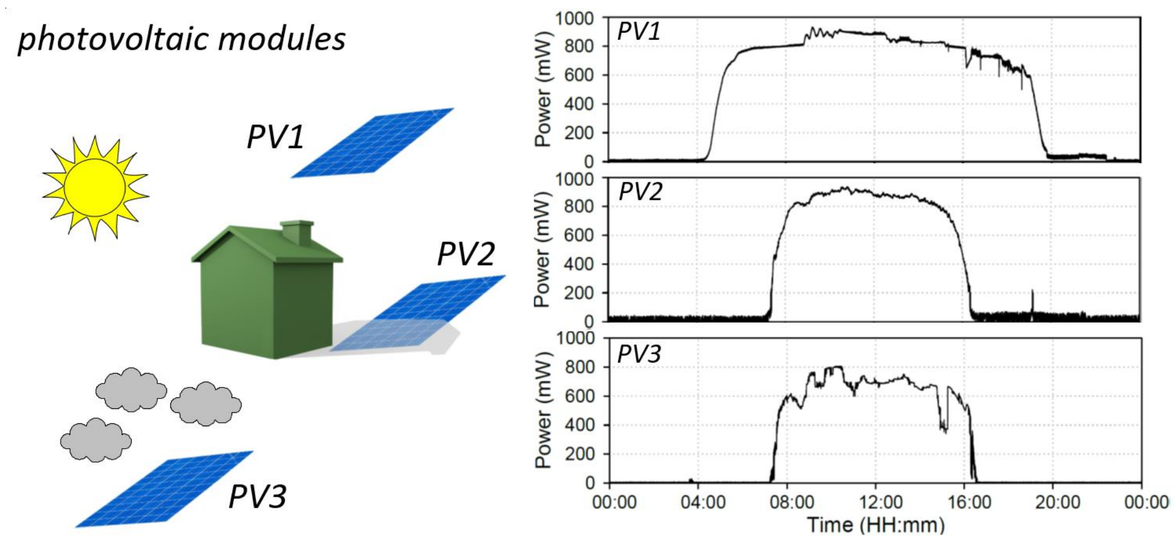
However, such energy sources are typically unpredictable, with high temporal and spatial variability.

To overcome this, large energy buffers are incorporated to achieve **energy neutral (EN) operation**, where the energy consumed over a certain period of time is equal to the energy harvested.

Large energy buffers, however, pose environmental issues in addition to increasing the size and cost of systems.

To address the issues related to high source variability, we proposed an alternative approach whereby systems operate directly from the EH source, minimizing the need for additional energy storage.

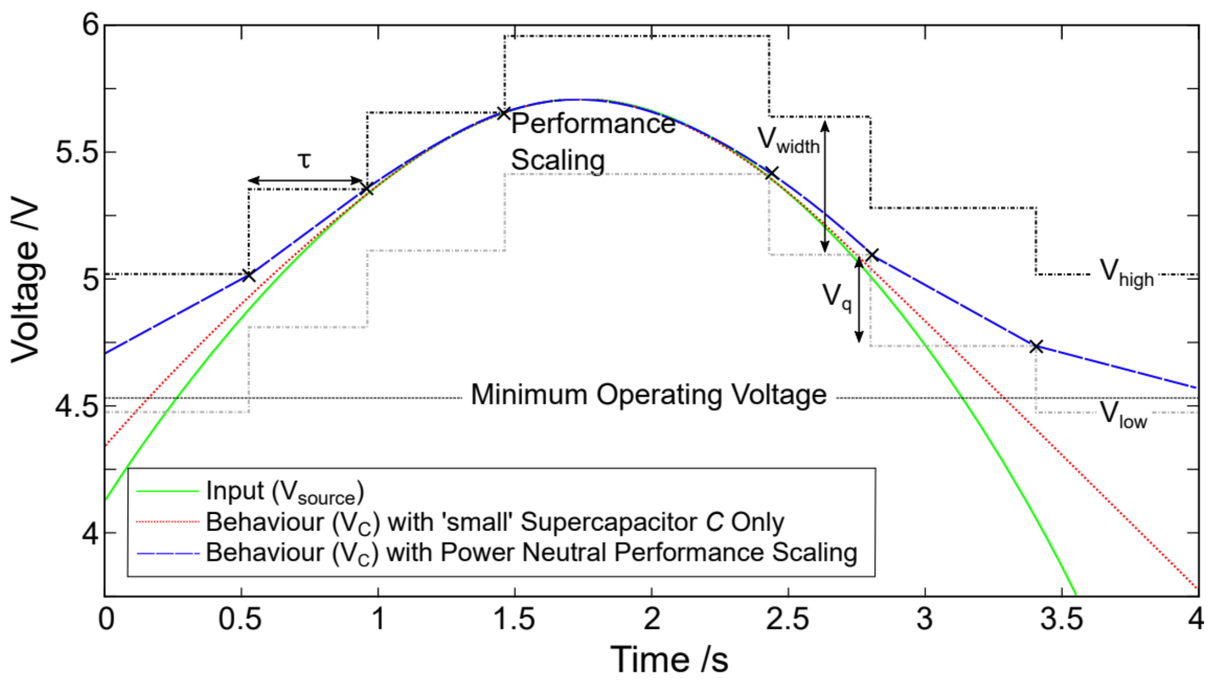
Variable and Unpredictable Source



Power outputs from three PV cells located outdoor

Power Neutral Operation

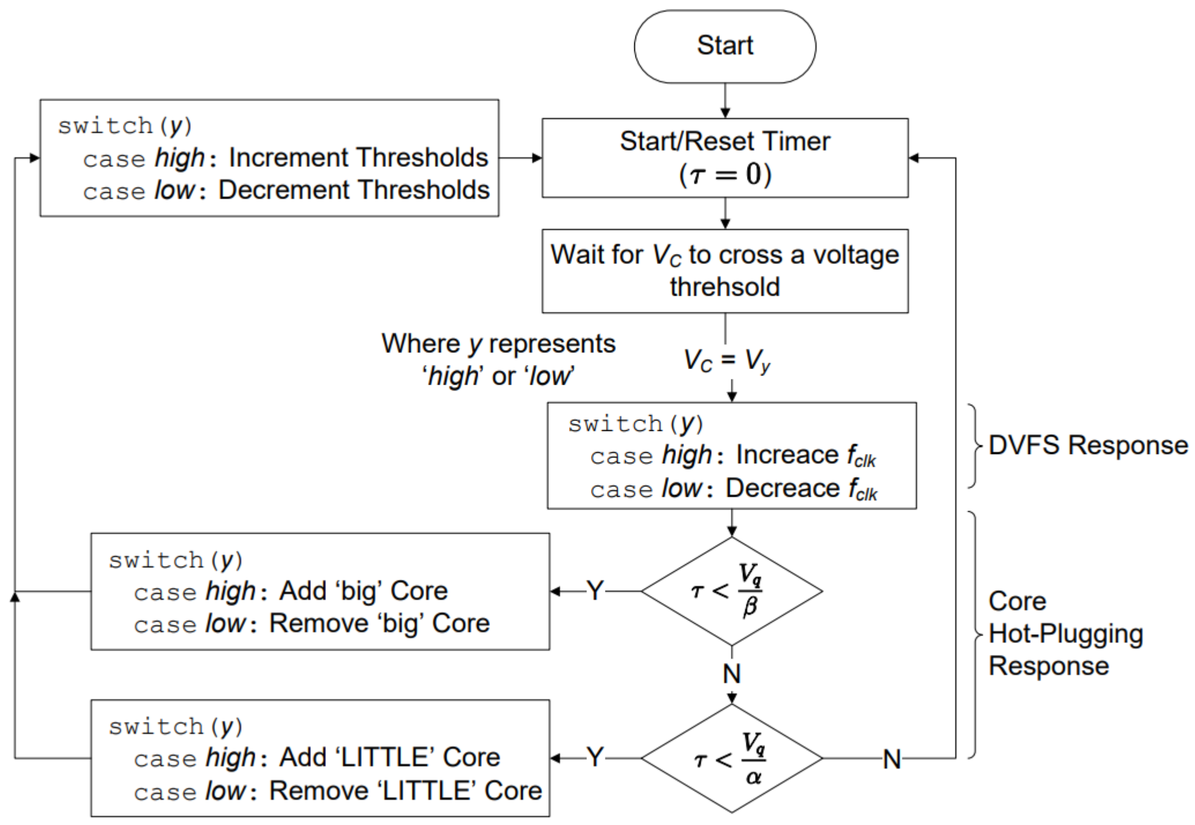
Power-neutral operation, where the instantaneous power consumption of the system is dynamically adjusted such that it matches the instantaneous harvested power. This is achieved by dynamically adjusting the system's performance and hence the consumed power.



Behaviour of an EH system to a transient input (green), with (blue) and without (red) power neutral performance scaling

Power Neutrality with MP-SoCs

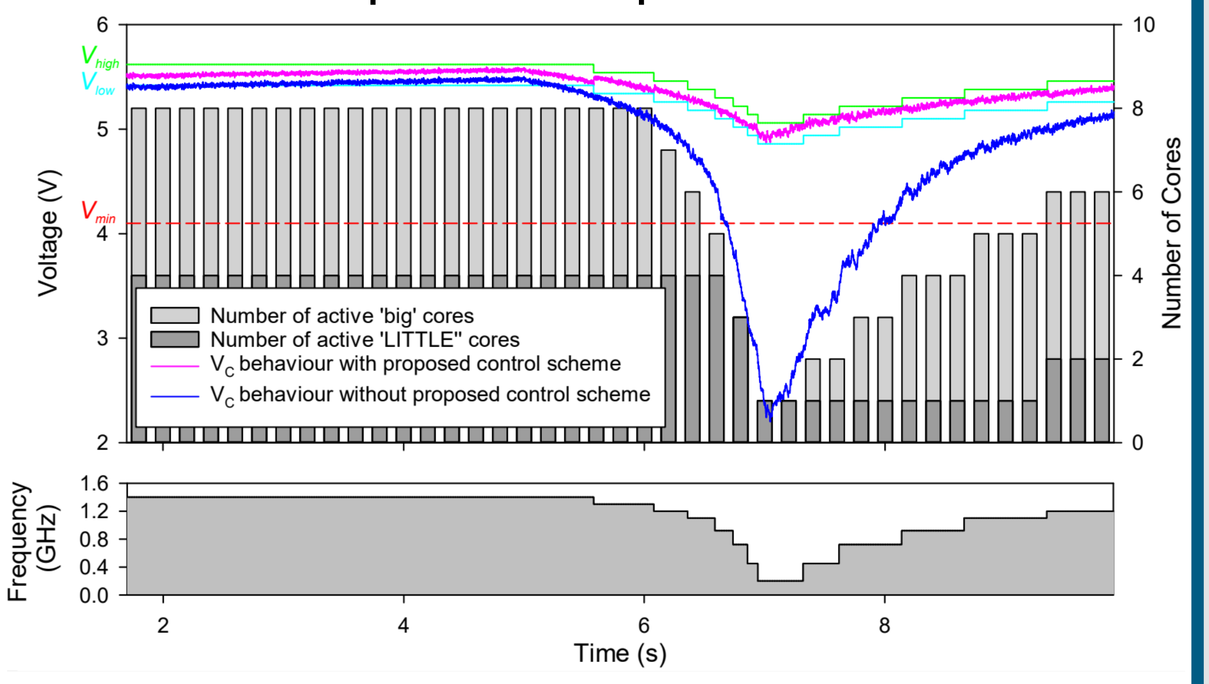
We extend the concept of power neutral operation to a **heterogeneous multi-core processor**, and propose a novel **performance scaling scheme** by controlling both DVFS and DPM. This scheme has been simulated and practically implemented on an typical heterogeneous MP-SoC platform (the Exynos5422 big.LITTLE SoC, with four big ARM A15 cores, and four LITTLE ARM A7 cores), directly coupled to a PV EH.



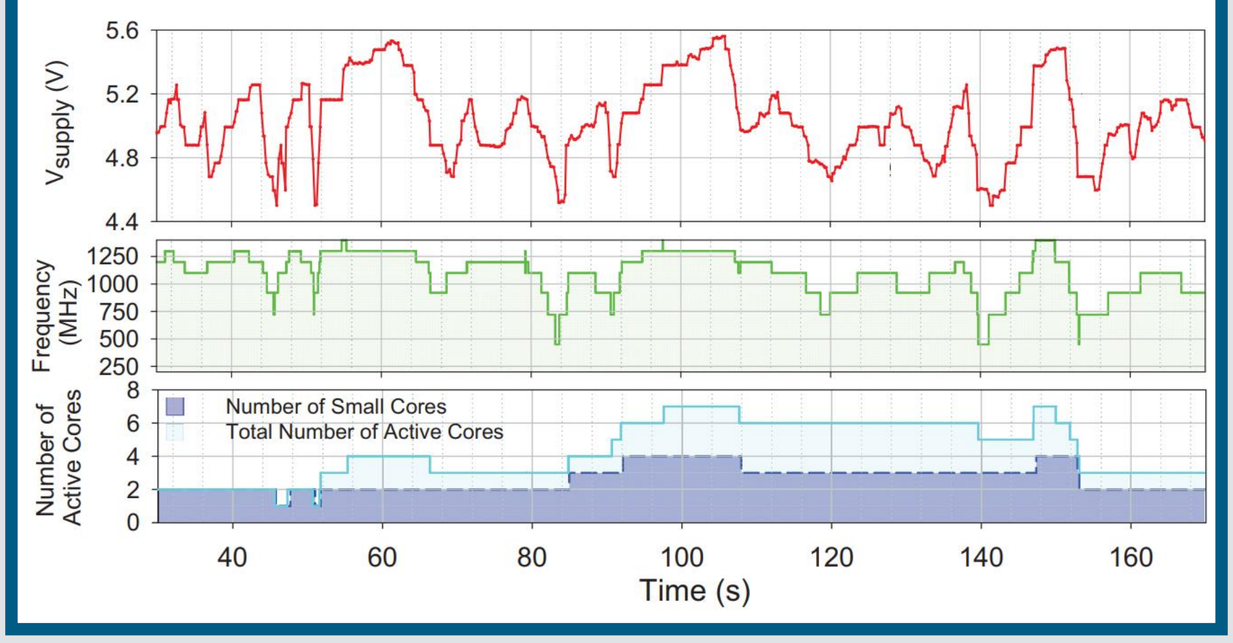
Flowchart depicting the principles of the power neutral performance scaling approach using DVFS and core hot-plugging

Results

Simulation of operation under power neutral control scheme



System performance using a controlled voltage supply



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