Power-Neutral Performance Scaling for Self-powered Multicore Computing Systems

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***Abstract*—In this poster, we present the power neutral paradigm and extend this to heterogeneous multi-core systems. To achieve power neutrality, a novel performance scaling scheme is illustrated, which control both dynamic voltage and frequency scaling (DVFS) and dynamic power management (DPM).**

I. Introduction and Related Work

Due to recent developments in runtime management, multicore systems are able to outperform single-core systems in both power consumption and performance. As such, heterogeneous multiprocessor system-on-chips (MP-SoCs) are rapidly becoming the de-facto technology for powering modern, high-performance embedded devices. Motivated by the limited device lifetimes achievable when powering these systems using batteries, research has recently looked at replacing batteries and using energy harvested from the environment. However, such energy sources are typically transient, with high temporal and spatial variability. To overcome this, large energy buffers are incorporated to achieve energy neutral (EN) operation, where the energy consumed over a certain period of time is equal to the energy harvested. Large energy buffers, however, pose environmental issues in addition to increasing the size and cost of systems.

To address these issues, an alternative approach has been proposed whereby systems operate directly from the EH source, minimizing the need for additional energy storage. This emerging class of systems presents an alternative to the EN paradigm: power-neutral (PN) operation, where the instantaneous power consumption of the system is dynamically adjusted such that it matches the instantaneous harvested power [1]. This is achieved without interruption by dynamically adjusting the system's performance and hence the consumed power. In large MP-SoCs techniques can be used to achieve power neutrality such as DVFS and core hot-plugging.

The power neutral paradigm has been first demonstrated through a practical implementation on an ultra-low power single-core MCU where power consumption was controlled through dynamic frequency scaling (DFS) [1].

II. Power Neutral Performance Scaling

In this poster, we extend the concept of power neutral operation to a heterogeneous multi-core processor, and propose a novel performance scaling scheme by controlling both DVFS and DPM [2]. This scheme has been simulated and practically implemented on an typical heterogeneous MP-SoC platform (the Samsung Exynos5422 big.LITTLE SoC, featuring four big ARM A15 cores, and four LITTLE ARM A7 cores), which is coupled directly to a photovoltaic (PV) EH source. Fig. 1 shows the simulated behavior of this system in a period of sudden shadowing. The blue line shows the behavior of the system with static performance, and the magenta line shows the behavior using a power neutral control scheme, which scales performance such that the supply voltage V_C does not fall below the minimum operating voltage, V_{min}, as would happen without it. Fig. 2 shows the performance of the system under power neutrality using a controlled variable supply.

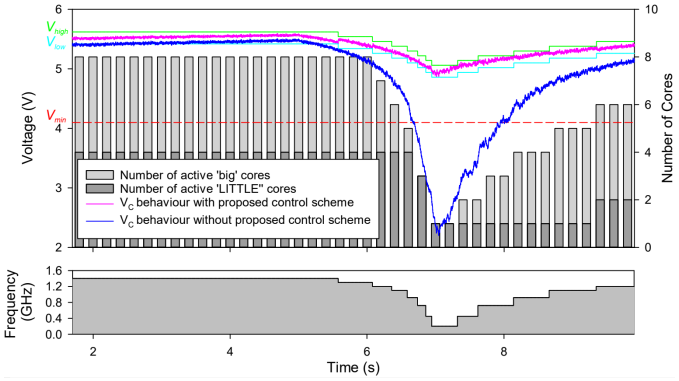

Fig. 1. Simulation of operation under power neutral control scheme [2].

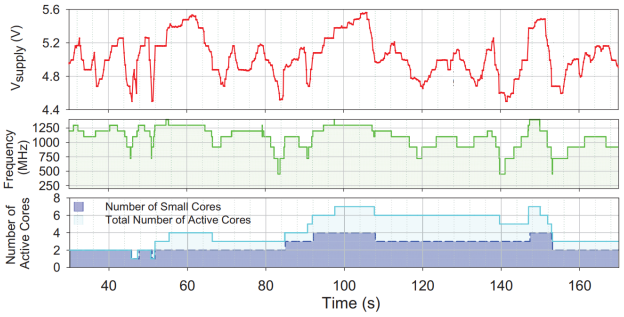

Fig. 2. System performance using a controlled voltage supply [2].

References

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