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Multichannel ZnO Nanowire Field Effect Transistors by Lift-off Process

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Abstract.

This paper describes a new low cost top-down fabrication process, which makes it possible to define nanowire field effect transistor (NWFET) arrays with different numbers of nanowires simultaneously and systematically compare their electrical performance. The main feature of this process is a developed bilayer photoresist pattern with a retrograde profile, which enables the modification of the nanowire in width, length, height and the number of transistor channels. The approach is compatible with low cost manufacture without electron beam lithography and benefits from process temperatures below 190°C. Process reliability has been investigated by SEM, TEM and AFM. Electrical measurements demonstrate enhancement mode transistors, which show a scalable correlation between the number of nanowires and the electrical characteristics. Devices with 100 nanowires exhibit the best performance with a high field effect mobility of 11.0 cm^2/Vs, on/off current ratio of $3.97x10^7$ and subthreshold swing of 0.66 V/dec.

Keywords: zinc oxide (ZnO), field effect transistor (FET), nanowire, top-down fabrication

1. Introduction

One-dimensional (1D) nanostructures such as nanowires, nanotubes, nanorods and nanoribbons have been investigated in numerous studies because of their exceptional electrical and optical properties [1]. Nanowire field effect transistors (FET) are of interest for sensor applications [2], [3], including the detection and quantification of biomolecules such as enzymes or DNA [4], [5], [6]. Compared to silicon, ZnO exhibits a wide direct band gap ($E_g = 3.37$ eV @ 300 K), which allows a high sensitivity [7], [8].

ZnO NWFETs have been fabricated with either bottom-up or top-down techniques [9]. Typical bottom-up approaches involve nanowire synthesis by chemical vapour

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deposition (CVD) or a hydrothermal process, both of which result in high quality nanowires in terms of monocrystallinity, homogeneous morphology and a high aspect ratio, although the nanowire width and length can vary [10], [11]. However, bottom-up fabricated nanowires are difficult to be deposited at well defined positions on device substrates, which reduces the NWFET yield after subsequent top-down process steps that define other elements such as the source and drain electrodes at predetermined positions [12], [13], [14]. Recent investigations on bottom up technqiues show very controllable defenition of the nanowires to the substrate, but are also very cost intensive due to the use of electron beam lithography [15], [16]. To avoid this complex hybrid of bottom-up and top-down fabrication, other groups have explored an exclusively top-down strategy. Hereby, the main idea of the nanowire generation involves the spacer technique, where deposition and etching processes are used to create a non-reversible template [17]. This strategy exploits the lithography-determined position of the spacer, and therefore the nanowire location, on the device substrate. Moreover, the NWFET channel length, width and thickness can be varied to meet a range of performance specifications [18]. Recent studies on this fabrication approach have shown good transistor performance and also demonstrated biosensor functionality [19], [20]. Further improvement on the NWFET characteristics has been achieved by reducing the nanowire surface roughness, which is known to have a significant effect on the electrical properties of nanowires [21], [22]. However, the previously developed spacer technique has several disadvantages. The fabrication process is based on a non-reversible template and is not suitable for low temperature processes and hence precludes the use of polymer substrates. Furthermore, the nanowires are formed by anisotropic dry etching where ions and radicals from the plasma source are implanted into the nanowires and change their top surface chemistry and hence their electrical properties [23]. Another problematic issue is non-uniformity of the back gate layer, associated with a poor control of the transistor channel [19]. Finally, although the spacer technique in principle enables a range of nanowire lengths and nanowire array sizes to be realized simultaneously on the same substrate, this has to date not been demonstrated.

In the present study, a new spacer-based fabrication approach was developed and scaling of the nanowire dimension and array size was demonstrated, enabling an analysis of the electrical characteristics of the various NWFET configurations. This process benefits from low temperatures, below 190 °C. Two process steps, thermal oxidation and inductively coupled plasma etching, were eliminated. To reduce the impact of implanted ions into the ZnO crystal lattice during the anisotropic etch step, a removable bilayer photoresist pattern was developed to protect the ZnO from ion bombardment. Two different photoresist layers were patterned, coated with ZnO by plasma enhanced atomic layer deposition (PEALD) and etched. This lithography technology is well known for metal lift-off as it exhibits excellent undercut profiles [24], [25]. In this investigation two different photoresist layers are patterned and coated with ZnO by plasma enhanced atomic layer deposition (PEALD) and etched. Here we show that it can also improve control over the charge carrier concentration in the nanowire channel.

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Furthermore, the presented fabrication process can be adapted to allow the nanowire to be formed on a planar back gate dielectric thin film, which enables an improved back gate control. ZnO NWFET arrays are used in biosensing applications, but their scaling properties for different nanowire numbers have not been investigated [26], [27]. Therefore, the ZnO NWFETs were manufactured as arrays with different numbers of nanowires (2 to 100) and with different channel lengths (5 μm to 45 μm). The structural and morphological properties of the final device were examined with Sscanning electron microscopy (SEM), transmission electron microscopy (TEM) and atomic force microscopy (AFM). All NWFETs arrays were electrically characterized, demonstrating excellent field effect transistor behavior. I_D / V_{GS}measurements were performed to extract the transconductance, field effect mobility, threshold voltage and subthreshold slope. As a prototype device, the nanowires were fabricated on a silicon wafer, but due to the low temperatures the process is transferrable to low-cost silicate or polymer substrates.

2. Experiment

The developed process enables the fabrication of NWFETs at process temperatures below 190 °C. Thermally oxidized silicon wafers with a silicon dioxide thickness of 100 nm were used as substrate material. The template for creating the nanowire was a two-layer photo resist pattern of lift-off resist (LOR3A, Microchem Corp.) and diluted negative resist (AZ2070 1:1.33 AZ EBR Solvent, Microchemicals GmbH). LOR3A consists of polymethylglutarimide (PMGI), which is not sensitive to UV exposure. This bottom layer acts as a sacrificial thin film, exhibiting excellent adhesion and high temperature stability. It is compatible with g-,h-,i-line photo resists and can be developed with standard TMAH containing developers [28]. AZ2070 was chosen as it provides a very high stability against thermal softening. Due to the small feature target dimensions, a diluted version of the resist was used to achieve a film thickness of 400 nm.

First, the LOR3A was spun at 5000 rpm to a 178 nm thin film and baked 10 minutes on a hotplate at 190 °C to increase the structural stability. The thickness of the LOR3A defines the gap height, where the nanowire is formed. For a 30 nm thick nanowire the gap needs to be at least 100 nm high to ensure an unobstructed deposition of the ZnO. To obtain 100 nm, the LOR3A film was thinned in a 30 s developer bath containing 2.38 % TMAH. After rinsing and drying, diluted AZ2070 was spun at 5000 rpm on top of the LOR3A layer (figure 1a)), then baked at 90 °C for 30 s, exposed to UV (40 mJ/cm^2) and post-baked at 115 °C for 1 min.

The resist development was carried out in two steps. First the wafer was developed for 1 minute in diluted AZ 726 MIF (Merck Performance Materials GmbH) until all unexposed resist was completely removed (figure 1b)). To achieve a gap at the bottom resist layer it was necessary to harden the top layer to reduce its dissolution rate against TMAH. To this end, a flood exposure at 1 J/cm^2 and a 150 °C bake for 1 minute were carried out. The second development step etches the LOR3A to the desired gap width

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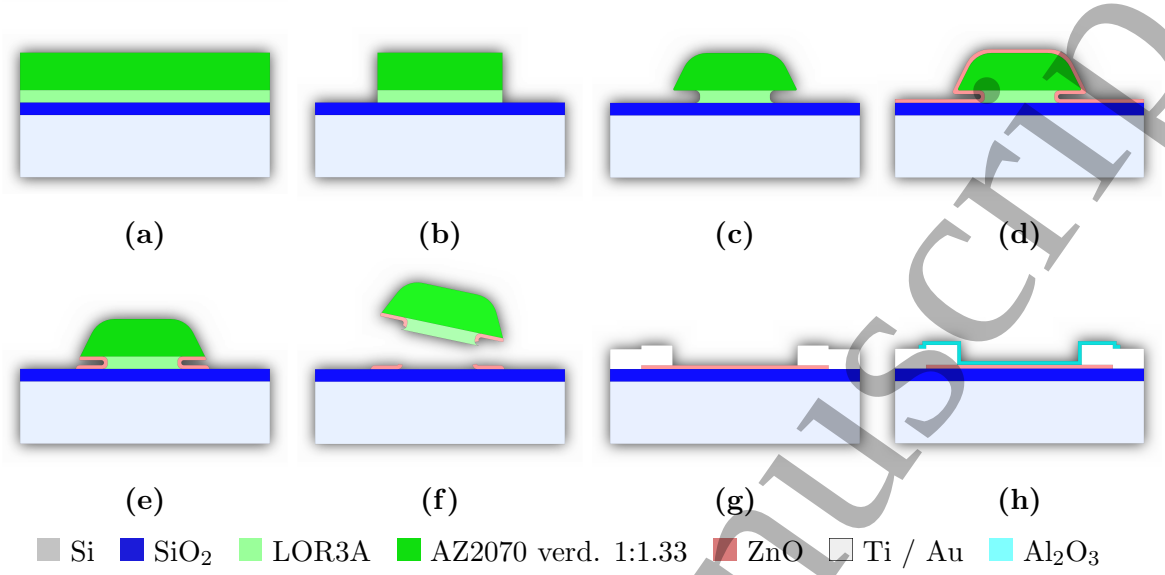

Figure 1. Schematic process flow cross section of (a) spun LOR3A and diluted AZ2070 on oxidised silicon wafer, (b) resist pattern after first development, (c) resist pattern after hardbake and second development, (d) ZnO coated resist pattern by PEALD, (e) anisotropic dry etched pattern, (f) resist lift-off process, (g) metal pad formation along the nanowire, (h) deposited and structured Al_2O_3 layer along the nanowire

of 250 nm (figure 1c)). With this step it is possible to adjust the resulting nanowire width. Figure 2 a) shows a SEM cross section of the patterned resist. The pitch between each pattern is 5 μm long.

Next, ZnO was deposited by PEALD (figure 1d)). PEALD has been used in spacer-defined double patterning and enabled low temperature deposition on photo resists [29]. Compared to thermal ALD processes PEALD uses an inductively coupled plasma (ICP) source to ionize O_2 instead of a water tank for the oxygen supply of the ZnO. This technique improves the range of the ALD process window and enables coating of the thin film at 150 °C without compromising the conformality of the layer. A ZnO thickness of 30.92 nm was achieved using 218 ALD cycles with 100 ms diethylzinc (DEZ, $Zn(C_2H_5)_2$) pulse, 4 s DEZ purge, 2.65 s O_2 plasma step with 100 W RF power and 4 s O_2 purge. A very conformal ZnO deposition was observed using scanning electron microscopy, where ZnO fills the patterned gap of the bilayer photo resist (figure 2 b)).

Subsequently the sample was etched anisotropically in an Argon ion beam etcher (IBE) (figure 1e)). IBE has been used due to several benefits. Compared to plasma etching techniques, where the sample is placed within the plasma, IBE decouples the wafer from the plasma source and prevents unwanted uncontrollable side effects such as charging. Gas chemistries with CHF_3 and Cl_2 promote reactions of the ZnO and the photo resist and leave residues, for example ZnF_2 and $ZnCl_2$, which are hard to dissolve [30]. The etching process is better controlled due to the use of inert Argon gas. With a beam current of 300 mA and beam voltage of 500 V, an etch rate of 17 nm/min was achieved. Figure 2 c) shows the SEM cross section of the etched area, where the ZnO

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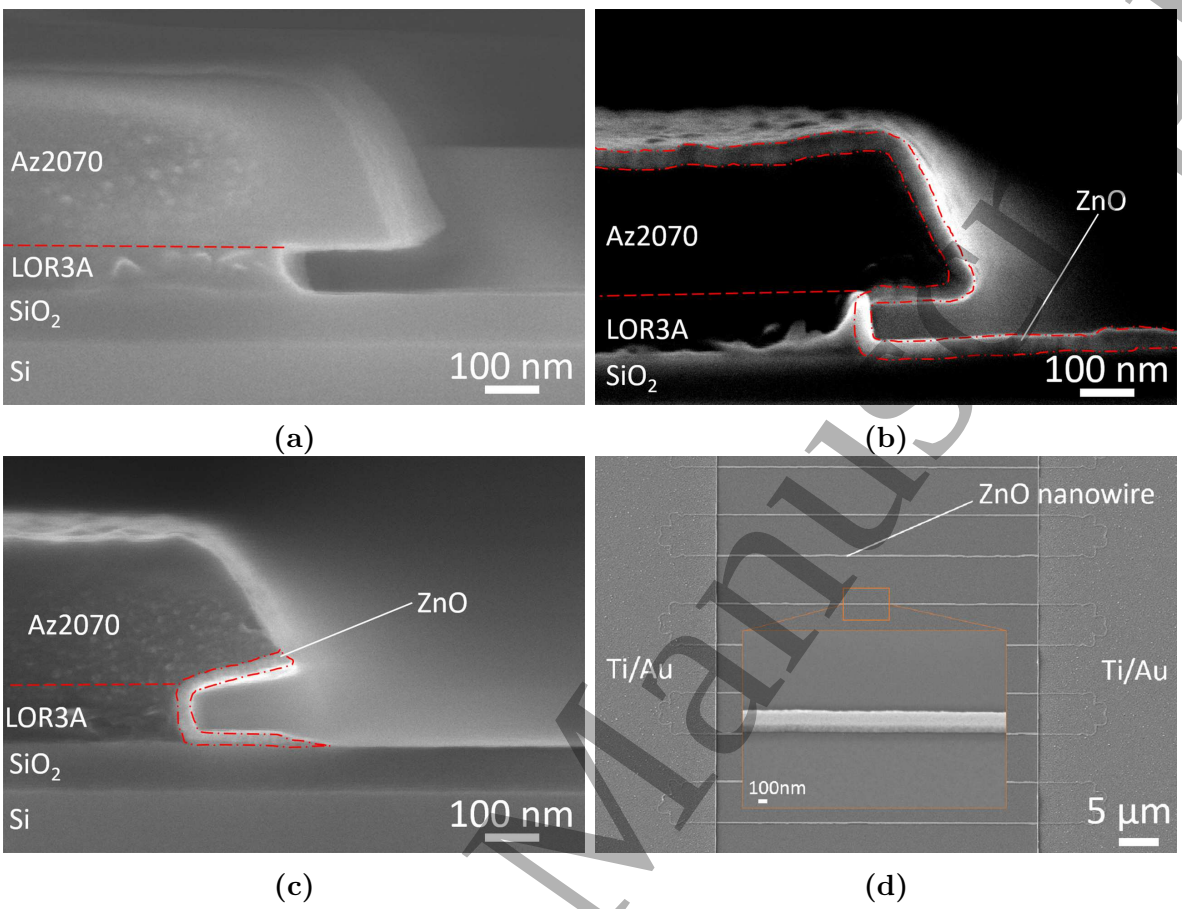

Figure 2. Scanning electron micrograph of (a) a cross section of the developed bilayer photo resist pattern, (b) a cross section of the ZnO coated photo resist pattern using PEALD, (c) a cross section of the ZnO coated resist pattern after IBE dry etch, (d) a top view of nanowire array with patterned Ti/Au metal pads

remains at the gap area in the sidewall of the photo resist pattern.

The resist was then stripped by placing the sample into a N-methyl-2-pyrrolidone (NMP) ultrasonic bath at 80 °C. During the strip, the bilayer resist including the ZnO thin film on it's sidewall was lifted off and only a ZnO nanowire, which adheres on the substrate was left (figure 1f)). Ti/Au (10 nm / 150 nm) was evaporated over a patterned AZ2070 negative resist and the lift-off technique was employed to form metal contacts at the source and drain region of the NWFET (figure 1g)). The top view scanning electron micrograph from figure 2 d) shows a NWFET array with straight and regularly positioned nanowires. For depositing a 30 nm Al_2O_3 passivation layer over the sample, a 300 cycles long PEALD process was used with 20 ms TMA pulse, 3 s TMA purge, 3 s O_2 plasma step with 300 W RF power, 1 s O_2 purge. Metal contact areas were opened by another pattern and IBE etch of the Al_2O_3 with 300 mA beam current, 500 V beam voltage with an etchrate of 4 nm/min (figure 1h)).

For comparing the influences of different gate dielectric layers to the electrical performance of the NWFET another wafer was fabricated using an Al_2O_3 gate dielectric.

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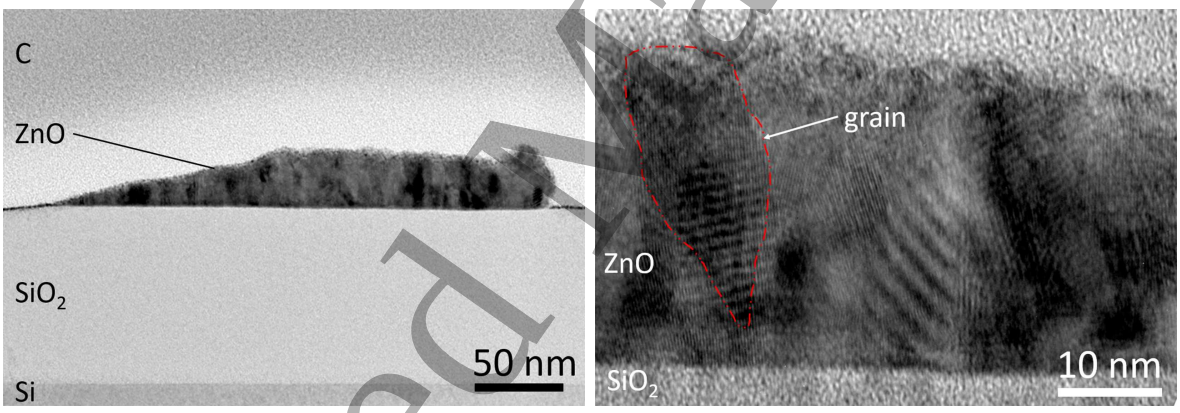
The fabrication follows the same process like the other samples described above exempt the step of growing a thermal dry oxide. Here the sample was coated with a 30 nm thick Al_2O_3 thin film using PEALD with 300 cycles including a 20 ms TMA pulse, 3 s TMA purge, 3 s O_2 plasma step with 300 W RF power and 1 s O_2 purge.

3. Results

3.1. Characterisation of ZnO nanowire morphology

Focused ion beam (FIB) was used for transmission electron microscopy lamella cross-section preparation of a nanowire. TEM was carried out at 200 kV acceleration voltage using a FEI Tecnai F20 with a Gatan Multiscan CCD Camera. Nanowire cross section dimension exhibits 30.9 nm height and 257.4 nm width (figure 3a)). It can be seen that the nanowire consists of a polycrystalline structure with grain sizes up to 9.8 nm x 28.3 nm (figure 3b)), which accommodate with the publications of ZnO ALD processes [31], [32].



(a) **(b)**

Figure 3. Bright field TEM cross section of a single nanowire; (a) overview, (b) detail

X-ray diffraction 2θ - θ scans on a Rigaku Smartlab have been carried out to investigate the ZnO thin film crystal orientation. The grazing incidence 2θ scan, with 0.5 degree, in figure 4 a) shows peak position, which were identified as hexagonal structure ZnO [31]. The 002 diffraction peak is much stronger than theoretically expected, indicating that the ZnO thin film exhibits a strong c-axis orientation. However, as this scan is a grazing incidence 2θ scan, the scattering vector is inclined about 34/2-0.5=16.5 degree from surface normal at 0002 diffraction condition. Therefore, the exact preferred orientation from this scan method can not be determined. Another in-plane diffraction scan with an incident angle of 0.2 degree has been carried out (figure 4 b)). The observed peak positions were identified as hexagonal structure ZnO. The 100 and 110 diffractions were stronger than theoretically expected, supporting the c-axis preferred orientation of the film.

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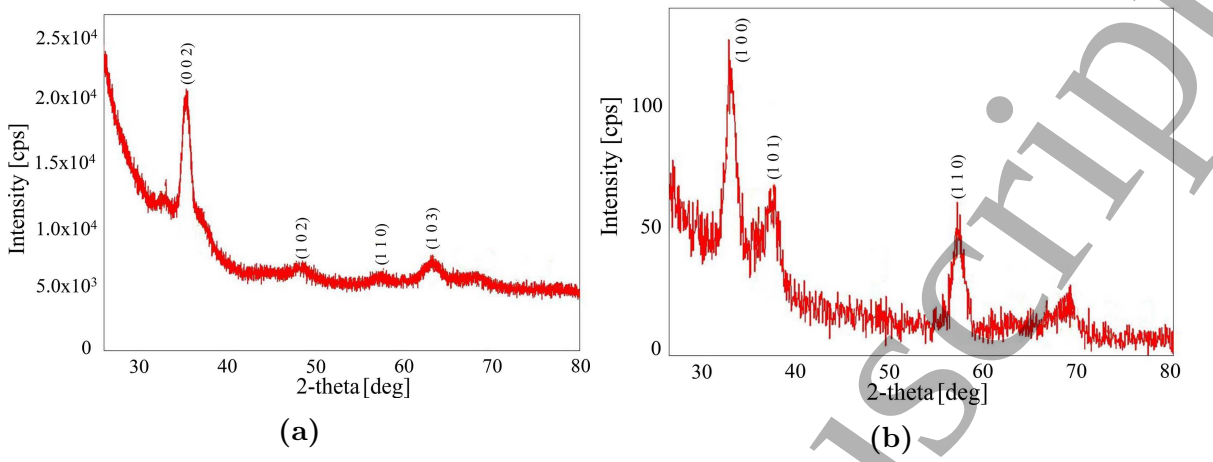

Figure 4. X-Ray diffraction spectra of deposited ZnO thin film: a) Grazing incidence 2θ scan; b) in-plane diffraction scan

3.2. Surface roughness of the ZnO nanowire

To investigate the ZnO surface morphology and roughness atomic force microscopy (AFM) was performed under ambient condition in intermittent non-contact mode with a PPP-NCHR probe from Nanosensors^{TM}. The tip is pyramid shaped and provides a <10 nm tip radius of curvature and a height of 10 μm to 15 μm. Image processing and analyses are performed using Gwydion software. The observed nanowire dimensions correspond to the TEM measurements. Figure 5 a) shows the AFM scan over the nanowire surface area with a length of 500 nm. A surface roughness rms of 1.2 nm was extracted from figure 5 b).

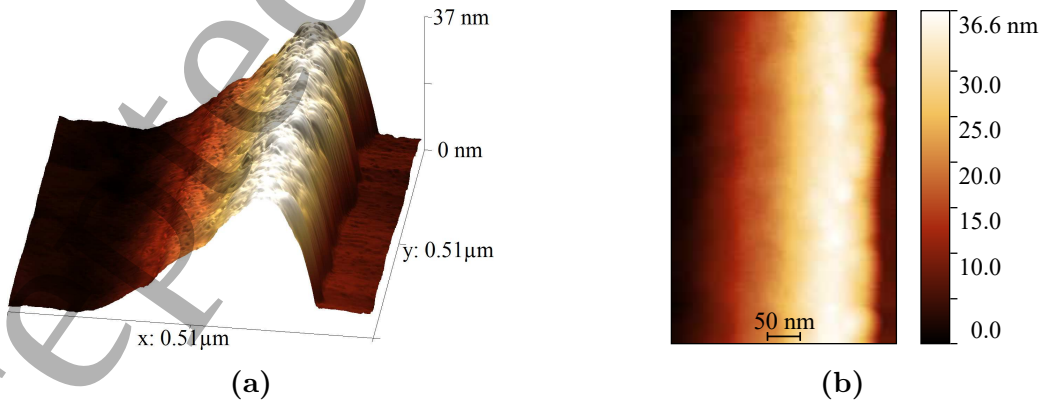

Figure 5. Atomic force microscopy image of a single ZnO nanowire top surface over a length of 500 nm: a) 3D plot of the nanowire shape, b) top surface 2D scan result

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3.3. Transfer characteristic

To investigate the ZnO NWFET operation performance, electrical characterisation was carried out using a semiconductor parameter analyser (Keysight Technologies B1500A) in the dark at room temperature. Drain current vs. gate source voltage (I_D/V_{GS}) measurements were performed for NWFET arrays with 2, 4, 6, 10, 50 and 100 nanowires and varying channel lengths of 5 μm, 15 μm, 25 μm, 35 μm, and 45 μm. As an example figure 6 shows the I_D/V_{GS} characteristic for a NWFET with 2 and 100 nanowires at $V_{DS} = 0.5$ V. While the V_{th} for a two nanowire transistor varies with the channel length, devices with 100 nanowires start to operate at a fixed gate voltage of 9 V. Figure 7 shows the I_D vs. V_D transistor output characteristics with gate sweeps from 5 V to 35 V. Here a maximum output current of 33.4 μA was measured.

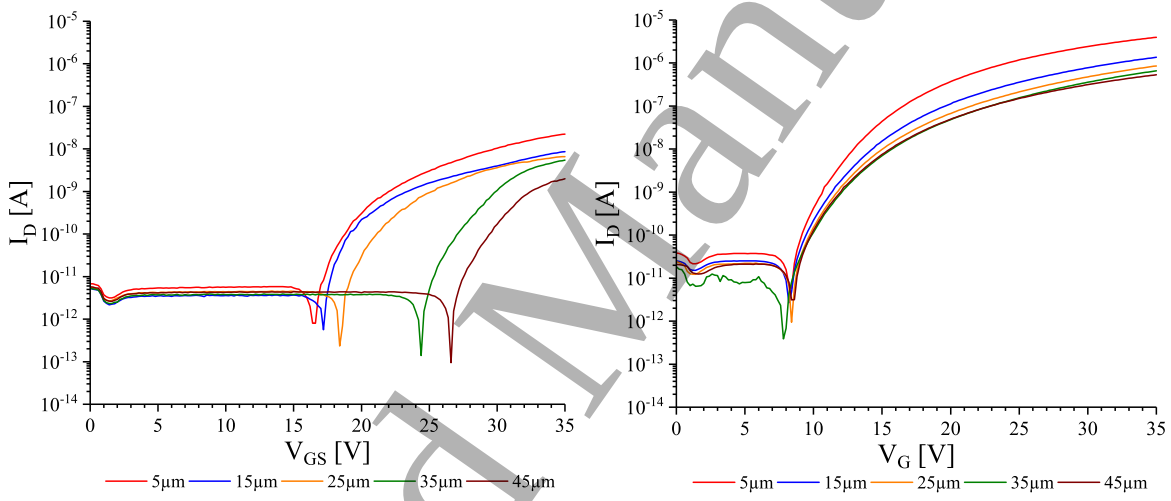

Figure 6. I_D vs. V_{GS} characteristic for passivated NWFETs with 2 (a) and 100 (b) nanowires and channel lengths between 5 μm and 45 μm at $V_{DS} = 0.5$ V

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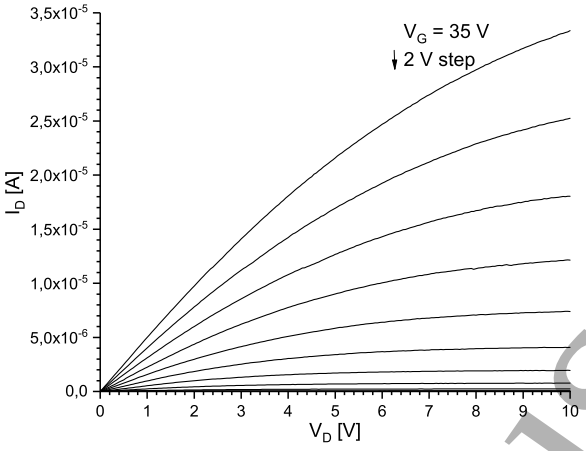

Figure 7. I_D vs. V_D output characteristics for gate sweeps from 5 V to 35 V with 2 V step size

Table 1 summarizes the measured I_D drain current in the transistor saturation regime at a gate voltage of 35 V with applied drain voltage of 0.5 V. It can be observed that the transistor output increases with the number of nanowires and decreases with longer channels. The lowest drain current of $2.0x10^{-9}$ A was detected for a NWFET with two 45 μm long nanowires and the maximum current of $4.0x10^{-6}$ was measured for a 100 nanowire FET with a channel length of 5 μm.

Table 1. drain current I_D at $V_{GS} = 35$ V and $V_{DS} = 0.5$ V for NWFETs with 2 to 100 nanowires and channel lengths from 5 μm to 45 μm

number of nanowires	I_D [A] vs. channel length				
	5 μm	15 μm	25 μm	35 μm	45 μm
2	$2.2x10^{-8}$	$8.6x10^{-9}$	$6.6x10^{-9}$	$5.5x10^{-9}$	$2.0x10^{-9}$
4	$3.2x10^{-8}$	$3.1x10^{-8}$	$9.7x10^{-9}$	$6.6x10^{-9}$	$2.2x10^{-9}$
6	$1.0x10^{-7}$	$4.3x10^{-8}$	$2.6x10^{-8}$	$1.9x10^{-8}$	$1.3x10^{-8}$
10	$2.1x10^{-7}$	$1.2x10^{-7}$	$7.8x10^{-8}$	$5.4x10^{-8}$	$4.0x10^{-8}$
50	$1.6x10^{-6}$	$5.4x10^{-7}$	$3.3x10^{-7}$	$2.9x10^{-7}$	$2.4x10^{-7}$
100	$4.0x10^{-6}$	$1.4x10^{-6}$	$8.5x10^{-7}$	$6.6x10^{-7}$	$5.3x10^{-7}$

Table 2 compares the I_{on} / I_{off} ratio vs. channel length by varying the number of nanowires. The highest value of $3.97x10^7$ was found for a 100 channel 5 μm long device, while the lowest I_{on} / I_{off} was observed for a two channel NWFET with a channel length of 45 μm.

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Table 2. I_{on} / I_{off} ratio for NWFETs with 2 to 100 nanowires and channel lengths from 5 μm to 45 μm at V_{DS} = 0.5 V

number of nanowires	I_{on} / I_{off} vs. channel length				
	5 μm	15 μm	25 μm	35 μm	45 μm
2	$2x10^5$	$9x10^4$	$7x10^4$	$6x10^4$	$2x10^4$
4	$3x10^5$	$3x10^5$	$1x10^5$	$7x10^4$	$2x10^4$
6	$1x10^6$	$4x10^5$	$3x10^5$	$2x10^5$	$1x10^5$
10	$2x10^6$	$1x10^6$	$8x10^5$	$5x10^5$	$4x10^5$
50	$2x10^7$	$5x10^6$	$3x10^6$	$3x10^6$	$2x10^6$
100	$4x10^7$	$1x10^7$	$9x10^6$	$7x10^6$	$5x10^6$

3.4. Transconductance and field effect mobility

Figure 8 a) contrasts the transconductance g_m of each device. The transconductance was extracted from the peak of the first derivative of the I_D/V_{GS} curve at a V_{DS} of 5 mV to appreciate the carrier transport in the channel. Values range between 0.006 nS (45 μm and 2 nanowires) to 3.4 nS (5 μm and 100 nanowires). These values are higher than top down fabricated NWFETs using the spacer technique [19], [21], but are still lower than single crystal ZnO NWFETs [14], [33]. All transistors demonstrate a dependency on

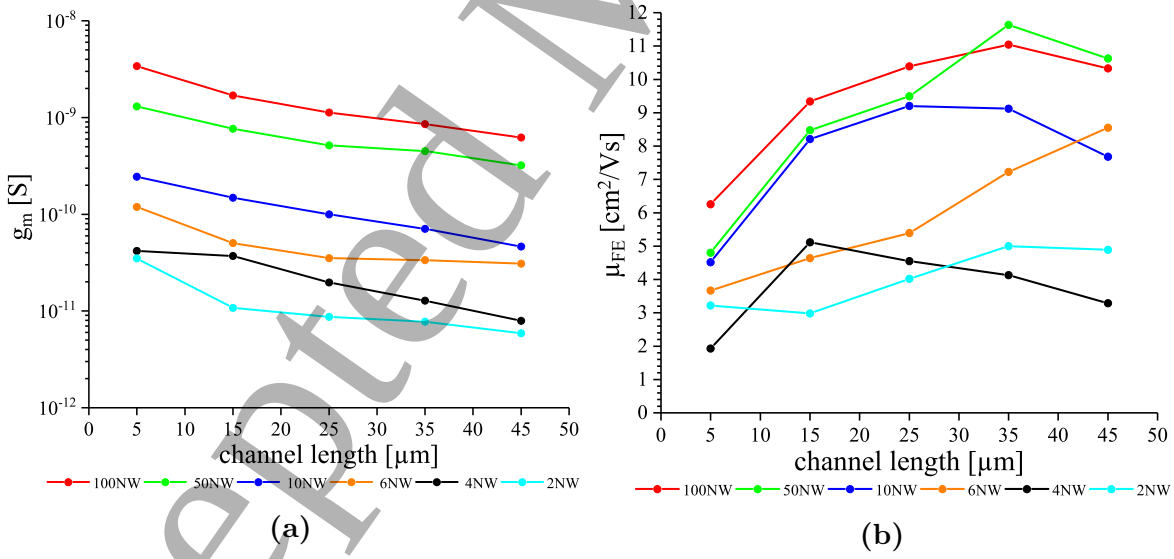

Figure 8. (a) Transconductance peak vs. channel length for NWFETs with 2 to 100 nanowires at V_{DS} = 5 mV; (b) Extracted field effect mobility vs. channel length for NWFETs with 2 to 100 nanowires at V_{DS} = 5 mV (lines between data points are a guide for the eye)

the channel length, where the transconductance decreases with larger channel lengths. As the shape of the nanowires is rectangular and the back gate is planar, the field effect mobility μ_{FE} was extracted from the value of the transconductance peak using

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the standard MOSFET equation

$$\mu_{FE} = \frac{C_{Ox} V_{DS} w}{l g_m n_{NW}} \quad (1)$$

where C_{Ox} refers to the back gate capacitance and was calculated from $C_{Ox} = \varepsilon_0 \varepsilon_{SiO_2}/d$ (with oxide thickness d), w is the nanowire width, l is the channel length and n_{NW} is the number of nanowires [34]. The graph in figure 8 b) shows the correlation between field effect mobility, channel length and number of nanowires. The highest field effect mobility was 11.6 cm^2/Vs for a 35 μm long transistor with 50 nanowires, while the lowest value of 1.9 cm^2/Vs was measured for a 4 nanowire transistor with a 5 μm long channel.

3.5. Threshold voltage and subthreshold slope

The threshold voltage V_{th} of each NWFET was investigated using the SD method, published by Wong et. al. [35]. With this approach the second derivative of the I_D/V_{GS} graph is calculated. The resulting maximum at a designated V_{GS} can be used to estimate the V_{th} for nanowire channels of different length, as shown in figure 9 a). All the transistors show an enhancement mode operation. It can be observed that a

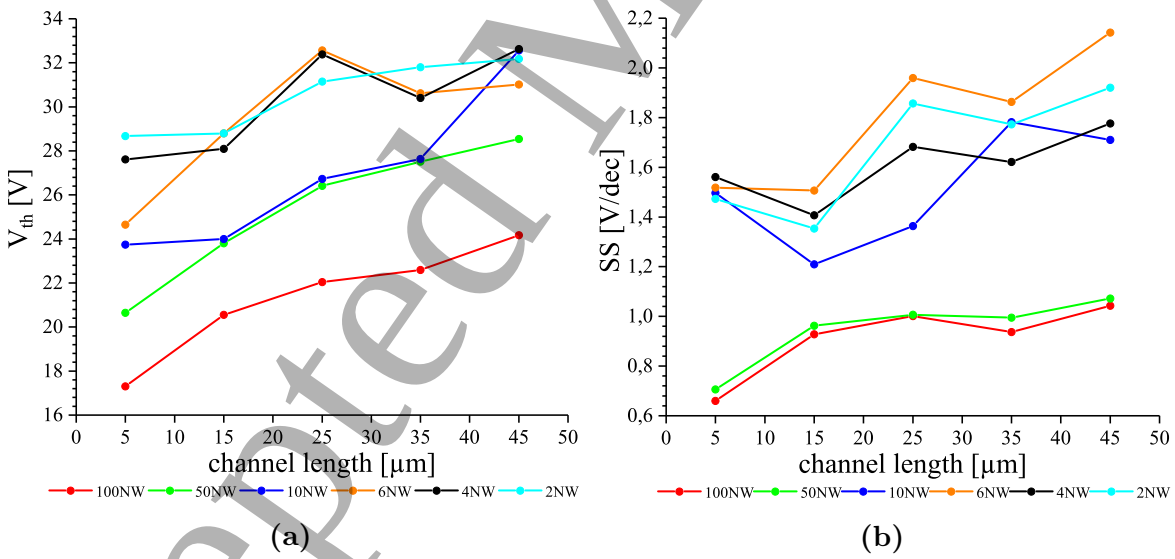

Figure 9. (a) Threshold voltage characteristic vs. channel length for NWFETs with 2 to 100 nanowires at $V_{DS} = 0.5$ V; (b) Subthreshold slope characteristic between $I_D = 10$ pA and $I_D = 100$ pA vs. channel length for NWFETs with 2 to 100 nanowires at $V_{DS} = 0.5$ V (lines between data points are a guide for the eye)

higher number of nanowires in the transistor leads to an average reduction of the V_{th} between 2 and 100 nanowires of 9.2 V. Another impact can be found by varying the channel length. An average V_{th} decrease of 6.4 V for NWFETs with channel lengths between 5 μm and 45 μm was observed. Figure 9 b) summarizes the results of the subthreshold slope measurement between the drain currents of 10 pA and 100 pA at $V_{DS} = 0.5$ V. While transistors with 10 nanowires or less exhibit a subthreshold swing

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SS of 1.2 V/dec to 2.2 V/dec, NWFETs with 50 and 100 nanowires show a significant reduction ranging from 1.07 V/dec to 0.66V/dec (5 μm length and 100 nanowires)

4. Discussion

A new top-down fabrication method for ZnO NWFET devices was developed which eliminates key disadvantages of previous approaches. Compared to bottom-up methods this new technique can be used to fabricate reliable NWFET arrays with reproducible dimensions using standard UV lithography. For top-down processes this approach offers several advantages. With the spacer technique the nanowire size is determined by the trench dimensions. We adjusted the development time of the LOR3A photo resist to achieve a retrograde undercut. This method has been shown successful in t-gate transistor fabrication [36], [37]. The fabrication flow developed in this study offers high reliability and reproducibility, by using only four low thermal budget processing tools (UV pattern tools, PEALD coater, ion beam etcher, metal evaporator). Process temperatures below 190 °C allow device fabrication on polymer substrates. PEALD exhibits excellent control of the deposition rate, which allows to change the nanowire height precisely. However, if the back gate dielectric is not planar, the nanowire channel will still experience a non-uniform field. Our bilayer resist method enables formation of planar nanowires on a dielectric material by removing the reversible photo resist template by lift off. From TEM and AFM inspection it can be seen that the nanowires exhibit a very smooth top surface. Any roughness results only from the ALD process. The retrograde resist profile protects the top surface of the nanowire from Ar ion bombardment during the anisotropic etch.

All measured devices show a clear n-type enhancement transistor behaviour and indicate an improvement of electrical performance with increasing number of nanowires. The devices show clear scaling properties for the drain current in terms of the number of nanowires per device, as also observed by Regonda et al. [38]. NWFET biosensing applications will benefit from a better signal response due to steeper subthreshold slopes, higher mobilities and a better signal to noise ratio because of high drain currents and low off currents [39]. It can be also seen that the drain current follows an approximate scaling trend in terms of longer channel lengths. Here the back gating could change the effective length. The measurements showed NWFETs with small number of nanowires have higher threshold voltage V_{th}, which line edge roughness can be the contributing (LER) effect. As reported by Hong et al. nanowire LER roughness has a significant effect on the electrical characteristics [40] and relies on the quality of the pattern transfer. Particle contamination during lithography can also lead to a significant increase of the LER. The impact of the electrical performance of a single irregularly shaped nanowire on the performance of a two-channel NWFET is much higher than that on a 100-channel transistor. This effect contributes to the increase of the V_{th} with a decreasing number of nanowires. A reduction of V_{th} with decreasing channel length can be attributed to short channel effects. Especially the drain induced barrier lowering was observed during

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I_D/V_{GS} measurements (not shown) of one channel length with varying drain voltage, where the threshold voltage is reduced with higher values of V_D. The results in figure 8 b) show the field effect mobility values saturating as the channel length increases for different number of nanowires. This is also observed by Jo et. al., Luan et. al. and Sultan et. al. [41], [42], [43], where parasitic contact resistance, which we measured at 100 kΩ for the 100 nanowires transistor, at the source and drain region can affect the field effect mobility extraction. In addition, the large voltage drop over the parasitic contact resistance for the shorter channel devices would increase the electric field across the channel and electrons accumulation at the ZnO insulator surface, thus reducing the mobility through scattering effect [44]. The average the field effect mobility varies from 1.9 cm^2/Vs to 11.6 cm^2/Vs, which correlates as well with the LER of nanowires, discussed above. Nanowires with lowest LER, will result in higher field effect mobilities due to less defects at the transistor channel. Therefore, these nanowires will dominate the transistors electrical characteristics. NWFETs with a high number of nanowires possess a high chance of exhibiting a high number well-defined channels.

The enhancement mode operation is assumed to correlate with grain boundary charges and trapped interface charges between the ZnO and the SiO_2. Investigations on ZnO thin film structures have shown that double Schottky barriers form at every grain boundary and that deep acceptor traps affect the static and dynamic properties of the electron transport [45], [46]. Increasing the number of grain boundaries will reduce the field effect mobility of the transistor and influences the resistance within the nanowire channel [47], [48]. As a result the transistors operation regime will shift from a depletion mode to an enhancement mode [49]. A reduction of the grains inside of the ZnO crystal structure can be achieved by tuning the PEALD deposition process to temperatures of 100 °C [50]. To investigate whether the transistor can be shifted to a depletion mode, I_D vs V_{BG} measurements on a top gate biased 10 nanowire FET with a channel length of 15 μm were carried out (figure 10 a). It can be seen that the transistors transfer curve can be shifted towards negative voltages. This is, because deep trap charges are pushed away by applying V_{TG} on the transistor channel. Another source of trapped charges is attributed to deep level interfacial traps in the vicinity of the ZnO / SiO_2 interface [51], [52]. In this respect, Al_2O_3 is a promising alternative to SiO_2, because of reduced dislocation, vacancy and interstitial defects and less deep trapped charge generation [53], [54]. For this reason another NWFET array with 100 nm wide nanowires was fabricated with a 30 nm thin Al_2O_3 back gate oxide layer instead of the 100 nm SiO_2 thin film. This thinner gate insulator also gives a higher dielectric constant. Figure 10 b) shows the I_D vs V_{GS} measurement at a V_{DS} of 50 mV where the Al_2O_3 back gate transistor switches on in the negative mode and operates in depletion mode. This experimental observation is indeed consistent with a reduction of interface charge injection.

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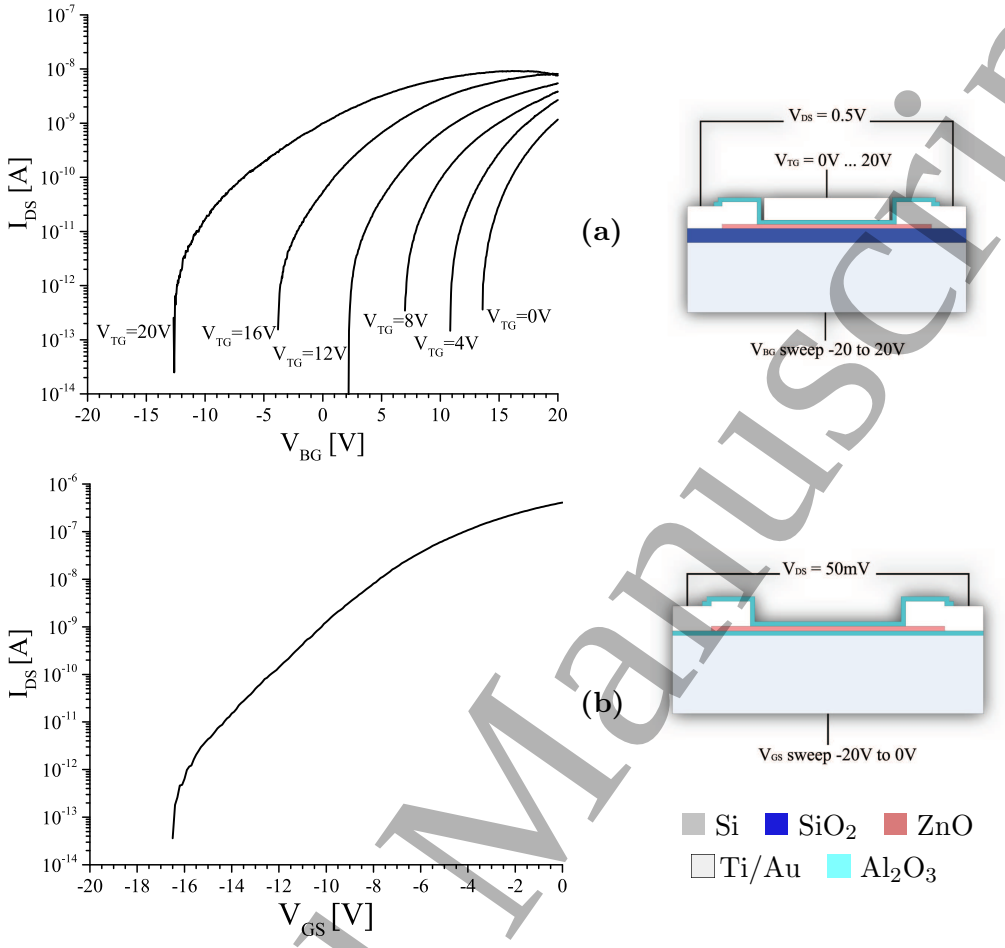

Figure 10. (a) I_D / V_{BG} characteristic and measurement schematic for a 10 nanowire FET with 15 μm channel length with a back gate sweep and static top gate voltages from 0 V to 20 V and a V_{DS} = 0.5 V; (b) I_D / V_{GS} characteristic and measurement schematic for a 100 nanowire FET with 15 μm channel length with a 30 nm thick Al_2O_3 back gate at a V_{DS} = 50 mV

5. Conclusion

A scalable fabrication process for NWFET was developed which allows the formation of planar ZnO nanowire arrays on any type of gate dielectric layer using standard UV light lithography. Defining a wide range of NWFET configurations simultaneously enables rapid exploration of device performance parameters and identification of optimal parameters for specific applications, including biosensing. A retrograde bilayer photo resist pattern was investigated to reliably form nanowires scalable in number, length, width and height. The process benefits from low temperatures up to a maximum of 190 °C, which allows fabrication of NWFET devices on any type of substrate, even polymer samples. SEM, TEM and AFM analysis show the reliable fabrication of the nanowire and a very smooth ZnO surface with a rms roughness of only 1.2 nm, due to a very low impact of ion bombardment during IBE. Electrical measurements of the transistor arrays show a clear scalable regime, where an increase in the number of

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nanowires improves the electrical performance of the NWFET. Devices with the highest number of 100 nanowires per transistor show a field effect mobilities of 11.0 cm^2/Vs, a high I_{on} / I_{off} of $3.97x10^7$ and a minimum subthreshold slopes of 0.66 V/dec. All NWFETs exhibit an enhancement mode behavior, which is assumed to correlate with grain boundary deep level trapped charges and ZnO / SiO_2 interface injection charges. Future work will include NWFET fabrication on polymer samples and investigations on their performance for biosensing applications.

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