A comprehensive technology agnostic RRAM characterisation protocol

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Resistive switching memories, also known as memristors, have exhibited an immense potential for a wide array of applications, ranging from non-volatile memories[1] to neuromorphic computing[2] and reconfigurable circuits[3]. As the scope of these applications expands there is an increasing need for a comprehensive characterisation methodology.

Towards that goal we present a characterisation routine that covers a broad range of device aspects. Our testing routine employs our in-house developed memristor characterisation tool[4]. The proposed workflow starts with a pre-electroforming I–V in order to deduce the dominant transport mechanisms[5]. This is followed by the electroforming process which can be carried out using either current-compliant I–V curves or pulsed voltage ramps for a compliance-free approach. After establishing a base resistance we reevaluate the transport mechanism since both the core material and the interfaces have been altered with respect to their pristine state.

Switching performance of the device is benchmarked with endurance and retention testing either in room or elevated temperatures to extrapolate the lifetime of the memory window. We then proceed to evaluate the switching dynamics of the devices by applying a biasing scheme optimiser[6]. This allows us to determine the switching behaviour under external bias, as well as the switching polarity and operating range of the device (fig. 1). After these parameteres have been established we evaluate the maximum number of operationally relevant states using a bespoke routine[7] (fig. 2). Finally, an analytical model[8] of the response of the device can be readily extracted.

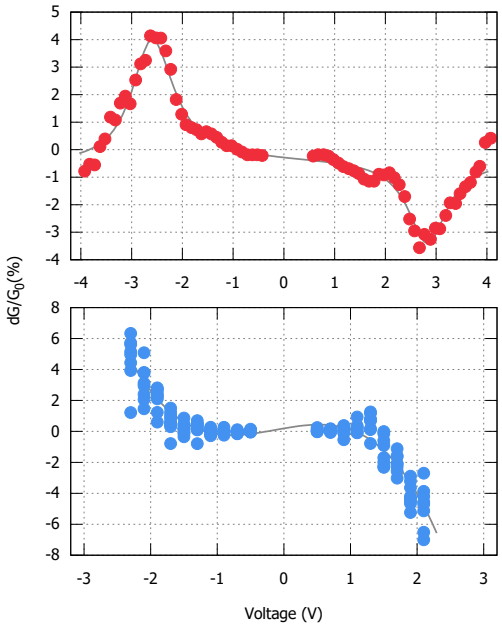

Figure 1 Relative conductance change in relation to applied bias for a Au/TiO_2/Pt device exhibiting mixed unipolar/bipolar behaviour (top) and a Pt/TiO_2/Pt device exhibiting pure bipolar character (bottom).

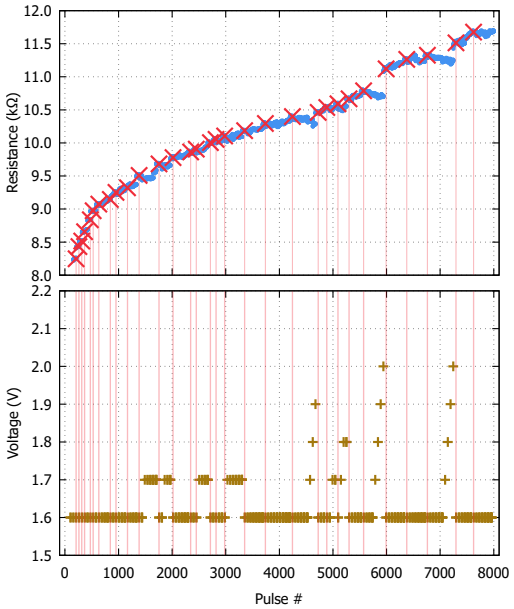

Figure 2 Evaluation of a Pt/TiO_2/Al_xO_y/Pt device in terms of multibit resistive state capacity. Established states are marked with red crosses (top); the programming protocol is evident in the bottom graph.

References

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