Back-end-of-line a-SiO_xC_y:H dielectrics for resistive memory

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Abstract

Resistive switching of W/amorphous (a)-SiO_xC_y:H/Cu resistive memories incorporating solely native back-end-of-line (BEOL) materials were studied. A-$SiC_{1.1}$:H, a-$SiO_{0.9}C_{0.7}$:H, and a-$SiO_{1.5}C_{0.2}$:H were exploited as switching layers for resistive memories which all show resistive-switching characteristics with ultrahigh ON/OFF ratios in the range of 10^6 to 10^{10}. Ohmic conduction in the low resistance state is attributed to the formation of Cu conductive filament inside the a-SiO_xC_y:H switching layer. Rupture of the conductive filament leads to current conduction dominated by Schottky emission through a-SiO_xC_y:H Schottky contacts. Comparison of the switching characteristics suggests composition of the a-SiO_xC_y:H has influences on V_{FORM} and V_{SET}, and current conduction mechanisms. These results demonstrate the capability to achieve functional W/a-SiO_xC_y:H/Cu using entirely BEOL native materials for future embedded resistive memories.

Introduction

Conductive bridge resistive memories (RMs) have attracted great research interest for next-generation non-volatile memories due to potentials for down-scaling[1] and superior switching performance[2] as well as compatibility with CMOS back-end-of-line (BEOL) processes[3]. RMs have a Metal-Insulator-Metal (MIM) structure where an insulator switching layer is sandwiched between two metal layers acting as an active and an inert electrode, respectively. It was reported that the formation and disruption of nanometer-scale metal filaments[4, 5] in the switching layer lead to the low resistance state (LRS) and high resistance state (HRS), respectively. Many metal materials have been exploited for electrodes including Cu[6] and W[7]. Cu and W are advantageous due to their widespread use in BEOL interconnects[3]. By also including native BEOL dielectrics such as a-SiOC:H as the middle insulator switching layer, it is possible to fabricate RMs that could be integrated into the BEOL interconnects with the advantages of being low cost and easy implementation[8]. These RM memory cells could be potentially positioned on top of transistors based control or logic layers and thus help shorten the interconnect delay, and at the same time could also help to achieve the 3D stacked configuration for high memory capacity[9].

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Amorphous (a)-SiC based dielectrics have attracted significant interest because of their recent success in BEOL applications[10, 11] due to their low dielectric constant (k) as compared to conventional SiO_2 and SiN[12]. In particular, a-SiOC:H with k values of 3.1-4.8 has replaced SiO_2 (k≈4-4.2) as the typical interlayer dielectric and also shown promise to replace a-SiN:H (k≈6.5-7.0) in etch stop and Cu diffusion barrier applications[12]. Excellent endurance of RMs using a-SiC as the switching layer has been reported[13]. Our previous studies[14-16] also led to a-SiC based RMs with ultrahigh ON/OFF ratios of up to 10^9. Ultrahigh ON/OFF ratios present great advantages in future applications as it not only enables fast and reliable detection of the states of memory cells, simplifies the periphery circuit to distinguish the storage information[14, 15], but also provide a promising chance to achieve multilevel storage, e.g. five stable states in 10^6 ON/OFF ratios was reported[17]. However, there is little study on RMs using native BEOL a-SiO_xC_y:H dielectrics as switching layers. Fan et al.[8] reported preliminary work of RMs using porous a-SiOC:H. However, low yield and high switching currents, i.e. in mA range, and also relatively low ON/OFF ratio were reported. There are no comprehensive studies on RMs incorporating BEOL dielectrics a-SiO_xC_y:H with different compositions. It is envisaged that different compositions may affect the k-values and Schottky barrier height (SBH) at the metal/dielectric interface, all of which may play an important role in the RM performance.

In this paper, we report RMs incorporating native BEOL dielectrics, i.e. a-SiO_xC_y:H as switching layers, Cu as active electrodes and W as inert electrodes, thus fully compatible with potential BEOL processes. Three compositions of a-SiO_xC_y:H, i.e. a-$SiC_{1.1}$:H, a-$SiO_{0.9}C_{0.7}$:H, and a-$SiO_{1.5}C_{0.2}$:H were studied. Material characterisations to determine compositions, k values, and SBHs of the corresponding metal/dielectric interfaces were conducted. Subsequently, W/a-SiO_xC_y:H/Cu RMs were fabricated, and typical switching characteristics were studied and compared as a function of the composition.

Experiment

The a-SiO_xC_y:H thin films were deposited on 300 mm diameter substrates using standard BEOL processes. The bottom Si (001) wafers were initially coated with 100 nm thermal oxide (SiO_2), followed by 100 nm SiN, a thin TaN/Ta adhesion layer, and finally, an electroplated Cu layer chemically mechanically polished to a final thickness of 300 nm.[10] The Cu layers were embedded here with an intention to be used later on as active electrodes in the a-SiO_xC_y:H RMs. The a-SiO_xC_y:H layers with thicknesses of 20 nm and 40 nm, respectively were deposited on top of the Cu layer using Plasma enhanced chemical vapor deposition (PECVD). Different compositions were achieved by adjusting the organosilicon/oxidizer and reactant diluent ratios, deposition pressure, and radio

frequency power[18], as details described in previous publications[10, 11]. Thus, the final stacked layers were a-SiO_xC_y:H/Cu/Ta/TaN/SiN/SiO_2/Si.

X-ray photoelectron spectroscopy (XPS) measurement was performed on a-SiO_xC_y:H films using a Theta probe in order to determine relative atomic% (at%) of the Si, C, and O elements in a-SiO_xC_y:H, whereby x and y are the at% ratio of O/Si and C/Si, respectively. A 40 s surface sputtering was performed before XPS measurements to remove any possible native oxide or contaminations. The mass density of the a-SiO_xC_y:H films was determined from a previous work using X-ray reflectivity measurements on the same films[19]. Terminal hydrogen groups were intentionally incorporated during film deposition to introduce controlled levels of nano-porosity[12], while this work focuses on the effect of the different compositions of O and C across the three typical BEOL materials. Porosity analysis based on ellipsometric porosimetry measurements[20] and Positronium annihilation lifetime spectroscopy (PALS)[19] have also been included here to assist material characterisation.

To fabricate W/a-SiO_xC_y:H/Cu resistive memories, photolithography process was conducted to pattern photoresist on the substrates, followed by W metal deposition and subsequent lift-off. This process led to W/a-SiO_xC_y:H/Cu resistive memories with a range of device areas from 20 µm × 20 µm to 100 µm × 100 µm. Cu contact windows were exposed on the side of each device chip by scratching-off the top a-SiO_xC_y:H layer using a razor blade. Before any switching studies, the capacitance of the original W/a-SiO_xC_y:H/Cu stacking structure was measured using an Agilent 4279 C-V meter at 1 MHz. The k values of corresponding a-SiO_xC_y:H materials was then calculated from the capacitance with known device areas and insulator thicknesses[21]. The current-voltage (I-V) characteristics of the a-SiO_xC_y:H RMs were measured using an Agilent 4155C parameter analyser and a Cascade REL-3200 probe station. In all the I-V measurements, +/-V was applied to the W electrodes while the Cu electrodes have always been grounded. Since Cu was acting as the active electrode, for clarity and ease of understanding, all the I-V plots in this paper were plotted with +V applied to Cu during SET and –V applied to Cu during RESET. A 5 mV/50 ms voltage ramping rate was applied for all the switching measurements in this paper.

Results and discussion

XPS survey spectra of a-SiO_xC_y:H in Figure 1 show Si 2p, C 1s, and O 1s peaks at approximately 101 eV, 283 eV, and 532 eV, respectively, aligning with Si-C, C-Si, and Si-O bonding.[22] Relative at% of Si, C, and O elements were estimated using the areas of the Si 2p, C 1s, and O 1s peaks and sensitivity factors of 0.27, 0.25, and 0.66,

respectively.[23] Three compositions were thus determined as a-$SiC_{1.1}$:H, a-$SiO_{0.9}C_{0.7}$:H, and a-$SiO_{1.5}C_{0.2}$:H, corresponding to 0 at%, 35 at% and 55 at%. Previous work on these a-SiO_xC_y:H films[19] reported higher mass densities of 2-2.4 g/cm^3 as compared with 0.7-1.3 g/cm^3 of porous a-SiO_xC_y:H[24]. Furthermore, ellipsometry and PALS have also confirmed there is no inter-connected porosity in these a-SiO_xC_y:H films.

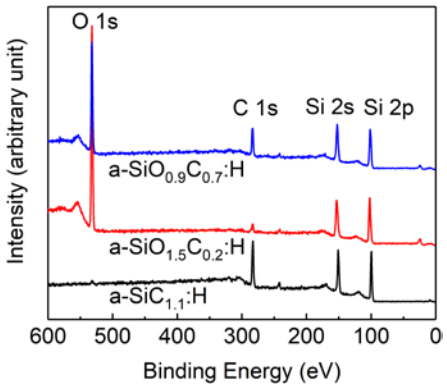

FIG. 1. XPS survey spectra of a-SiO_xC_y:H films.

Figure 2 shows a top view (FIG. 2a) and a Scanning electron microscope (SEM) cross-section image (FIG. 2b) of W/a-SiO_xC_y:H/Cu RM devices with stacking layers. K values of 5.2, 4.4, 4.3 for a-$SiC_{1.1}$:H, a-$SiO_{0.9}C_{0.7}$:H, and a-$SiO_{1.5}C_{0.2}$:H, respectively were obtained from capacitance measurements of pristine W/a-SiO_xC_y:H/Cu devices, which align with the range of 4.1-6.9 reported for non-porous a-SiO_xC_y:H materials[19]. Moreover, the decrease of k with the decrease of C content is consistent with the reported trend[25] as more Si-C bonds are likely to be replaced with Si-O bonds.[19] Figure 2(c) shows the current density (J) as a function of $|V|^{1/2}$ obtained from pristine W/a-SiO_xC_y:H/Cu devices. The linear fits suggest possible Schottky emission conduction mechanisms in the specific fitting range which follows:[26]

$$J = I/A = A^*T^2\exp\left(\frac{-q\Phi_B}{kT} + \frac{q}{kT}\sqrt{\frac{qE}{4\pi\varepsilon}}\right), \quad (1)$$

where A is the device area, A^* is the Richardson constant, T is the temperature, Φ_B is the SBH, E is the electric field, k is the Boltzmann constant, and ε is permittivity of the dielectric layer. It is worth noting that symmetrical J-V characteristics were observed across –V and +V regions (not shown here). This may be due to the existence of Fermi level pinning effect which can play a dominating role in SBHs[21]. Thus, Φ_B can be estimated from these linear fits to be 0.94 eV, 1.21 eV, and 1.09 eV for pristine a-$SiC_{1.1}$:H, a-$SiO_{0.9}C_{0.7}$:H, and a-$SiO_{1.5}C_{0.2}$:H respectively. The slightly higher Φ_B for a-$SiO_{0.9}C_{0.7}$:H and a-$SiO_{1.5}C_{0.2}$:H as compared with that of a-$SiC_{1.1}$:H may be attributable to relatively higher C at% in a-$SiC_{1.1}$:H which may promote electronic states into the band

gap of the a-SiOC:H, reducing Φ_B[11]. It is worth noting that these SBHs are lower than previous reported SBHs (1.45-1.65 eV) estimated from XPS measurements[10, 11]. This may be due to XPS being more sensitive to the energy gap between the dielectric conduction band edge (E_C) and the metal Fermi level (E_f), whereas the electrical SBH measurement is more sensitive to defects and traps within the bandgaps, leading to reduced SBH.[27] All key material characteristics are summarized in Table I.

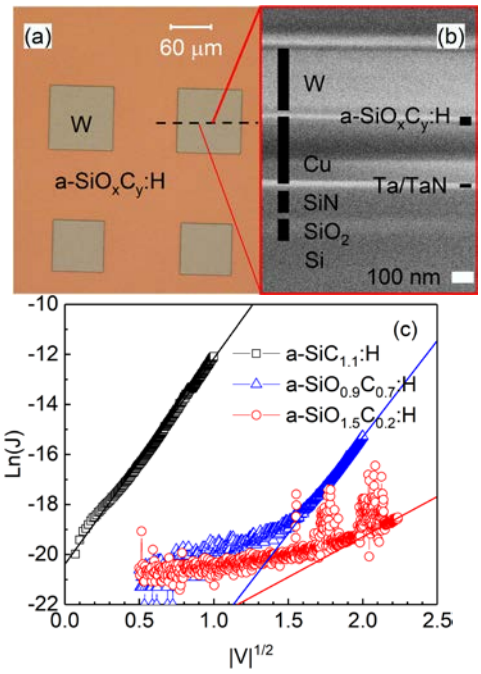

FIG. 2. (a) Top-view image and (b) SEM cross-section image of W/a-SiO_xC_y:H/Cu RMs. (c) Ln(J)-$|V|^{1/2}$ curves of pristine W/a-SiO_xC_y:H (20 nm)/Cu RMs, with respective linear fits.

TABLE I. Key material characteristics of a-SiO_xC_y:H.

Switching layer	Mass density (g/cm^3)	k	SBH (eV)
a-$SiC_{1.1}$:H	2	5.2±0.1	0.94
a-$SiO_{0.9}C_{0.7}$:H	2	4.4±0.2	1.21
a-$SiO_{1.5}C_{0.2}$:H	2.4	4.3±0.2	1.09

Figure 3 shows the typical forming (i.e. the first) and subsequent switching cycles of W/a-SiO_xC_y:H/Cu RMs with the voltage sweep sequence indicated by the arrows, respectively. All the switching cycles start at the high resistance state (HRS). The resistance of the devices at HRS is noted as R_{OFF} and was measured at 0.1 V. An applied +V sweep can induce a sharp transition from HRS to low resistance state (LRS) at the V_{FORM} (for the first cycle in FIG. 3a) and V_{SET} (for subsequent cycles in FIG. 3b), respectively. Subsequently, an applied -V sweep

induces a sharp transition from LRS to HRS at V_{RESET}. We believe the resistive-switching observed in Figure 3 is likely due to formation and rupture of Cu filaments in the a-SiO_xC_y:H dielectric layer. This is because we observed lower V_{FORM} in the +V regime than V_{FORM} in the –V regime (not shown here), which may correspond to formation of Cu and W filaments, respectively, when applying different V_{FORM} polarities. This is different from switching behaviour observed in SiO_x[28-33] based RMs whereby symmetrical V_{FORM} was mostly reported, supporting intrinsically filament mechanism. Linear fits in I-V characteristics as shown in Figure 3(c) provide further support to this with details discussed below.

Higher V_{FORM} (4.2-7.4V) as compared with V_{SET} (2.2-4.2V) is observed which has been frequently reported for RMs due to the initial formation of the metal filament in the pristine device.[1, 16] During the forming and SET processes, a 100 µA current compliance was adopted to avoid permanent dielectric breakdown of the device. The resistance of the devices at LRS is noted as R_{ON} and was measured at 0.1 V. All RMs have shown ultrahigh ON/OFF current ratio (equivalent to R_{OFF}/R_{ON} at 0.1 V) in the range of 10^6 to 10^{10}, which demonstrate significant improvement as compared with the reported ratio of 10^3 in literatures[8]. All key switching characteristics are summarized in Table II.

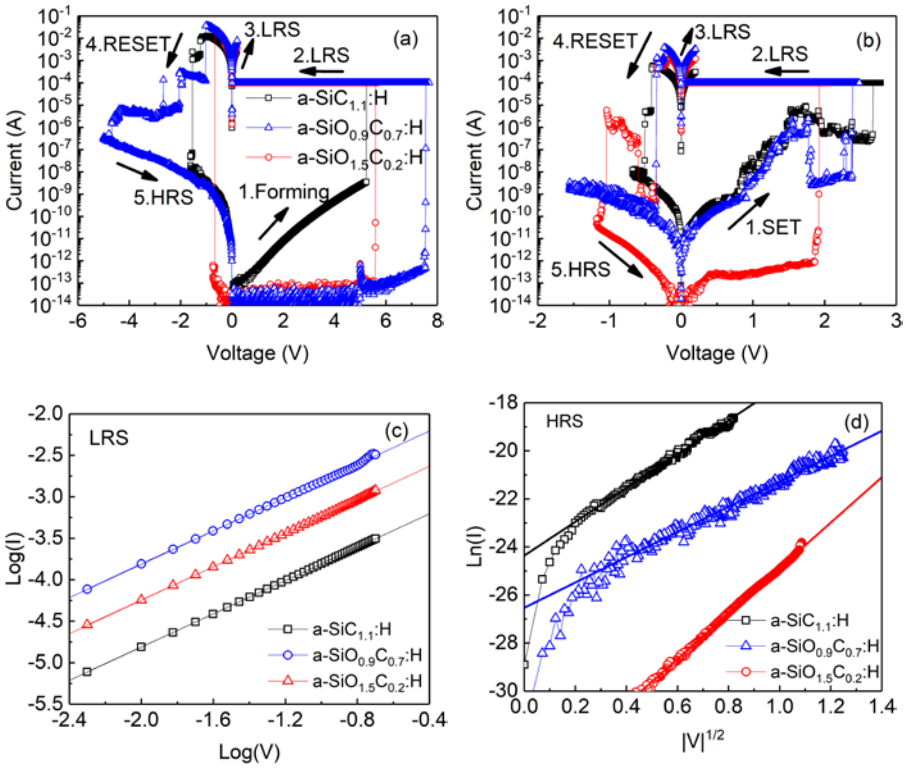

FIG. 3. I-V characteristics of the (a) first forming and (b) subsequent switching cycles of W/a-SiO_xC_y:H/Cu RMs. The labelled arrows indicate the direction and sequence of I-V sweeps. Forming, SET, RESET and corresponding

LRS, HRS are also labelled. (c) Log(I)-Log(V) curves for LRS obtained from W/a-SiO_xC_y:H/Cu RMs, with respective linear fits. (d) Ln(I)-√V curves for HRS obtained from W/a-SiO_xC_y:H/Cu RMs, with respective linear fits.

It is worth noting that our V_{FORM} values (4.2-7.4V) are generally higher than those reported (1-2 V) from RMs using porous a-SiOC:H[8]. This is likely due to the existence of interconnected pores in porous a-SiOC:H (1.2 g/cm^3) which require lower diffusion energy for Cu ions as compared with denser (2-2.4 g/cm^3) a-SiO_xC_y:H dielectrics used in this study. It has also been reported the activation energy of Cu diffusion in dense dielectrics is inversely proportional to their dielectric properties[34]. Therefore, V_{FORM} and V_{SET} (Table II) obtained from RMs having a-$SiO_{0.9}C_{0.7}$:H and a-$SiO_{1.5}C_{0.2}$:H with lower k values (Table I) are generally higher than those from W/a-$SiC_{1.1}$:H/Cu RMs. No clear dependence of V_{RESET} on the composition of a-SiO_xC_y:H is identified.

TABLE II. V_{FORM}, V_{SET}, V_{RESET}, and ON/OFF ratio of W/a-SiO_xC_y:H/Cu RMs.

Switching layer	V_{FORM} (V)	V_{SET} (V)	V_{RESET} (V)	ON/OFF ratio
a-$SiC_{1.1}$:H	4.2±1.7	2.2 ±1.5	-2.0±1.1	6.0×10^6
a-$SiO_{0.9}C_{0.7}$:H	7.4±2.1	4.2±2.6	-1.7±1.1	8.5×10^7
a-$SiO_{1.5}C_{0.2}$:H	6.5±3.4	3.5±2.6	-1.3±0.8	3.0×10^{10}

Figure 3(c) shows detailed I-V characteristics for LRS in a double logarithmic plot for the RMs. The slopes of the linear fits are all close to 1, indicating Ohmic conduction which attributes to the conduction through Cu filaments.[1, 14].The formation process of the Cu conductive filaments can be explained as when Cu active electrode is subject to a positive electric field (i.e. +V applied on Cu), Cu atoms from the Cu electrode oxidize into Cu cations and drift toward the negatively charged W electrode. The Cu cations inside the a-SiO_xC_y:H layer then reduce back to Cu atoms and these Cu atoms inside the a-SiO_xC_y:H layer then accumulate and form Cu conductive filament.[1, 16]

Figure 3(d) shows the HRS Ln(I) vs $|V|^{1/2}$ of a-SiO_xC_y:H RMs, which follow Schottky emission conduction mechanism aligning with Equation (1). The RESET mechanism has been reported as the disruption of the Cu filaments in the switching layer upon application of –V at active (i.e. Cu) electrodes. The negative electric field induces oxidation process for Cu atoms to transform into Cu cations, which subsequently drift back toward the Cu electrode[1, 16]. This could form an interface between the metal filament and a-SiO_xC_y:H at the HRS. This interface is different from the interface configuration between a-SiO_xC_y:H and metal electrodes as in the pristine state.[14] The SBH at the HRS were calculated based on the linear fits in Figure 3(d) and 0.78 eV, 0.84 eV, and 1.05 eV are obtained for RMs incorporating a-$SiC_{1.1}$:H, a-$SiO_{0.9}C_{0.7}$:H, and a-$SiO_{1.5}C_{0.2}$:H, respectively. These SBHs

in the HRS are lower than those of the pristine devices as shown in Table I. This may be attributable to the possible existence of residual Cu nanoclusters in the a-SiO_xC_y:H where the conductive filament ruptured. This may have altered the local defect charges and work functions in a-SiO_xC_y:H, thus lowering SBH.[14] SBH in HRS of a-$SiO_{0.9}C_{0.7}$:H and a-$SiO_{1.5}C_{0.2}$:H RMs (0.84-1.05 eV) is slightly higher than that of the a-$SiC_{1.1}$:H RM (0.78 eV), following a similar trend as in the pristine state. This may again be due to the relatively higher C at% in a-$SiC_{1.1}$:H introducing electronic states in the band gaps of a-SiOC:H[11].

Figure 4(a) shows the HRS and LRS current in successive switching cycles of a typical a-$SiO_{1.5}C_{0.2}$:H RM. Ultrahigh and stable ON/OFF ratios of approximately 10^8 were observed. Retention characteristic was measured at 0.1 V and room temperature, as shown in Figure 4(b). Although a-$SiC_{1.1}$:H and a-$SiO_{0.9}C_{0.7}$:H RMs have also been successfully switched multiple cycles with ultrahigh ON/OFF ratios in the range of 10^5 to 10^8 (not shown here), we observed in this work that a-$SiO_{1.5}C_{0.2}$:H RMs were relatively more stable over switching cycles. Promising retention in both LRS and HRS with negligible change in 10^5 s are observed aligning with many reported RMs[35, 36]. The stability[37] and promising retention may be attributable to the stable chemical properties of non-porous a-SiO_xC_y:H materials[12] as well as the ability of non-porous a-SiO_xC_y:H to act as Cu barriers[19].

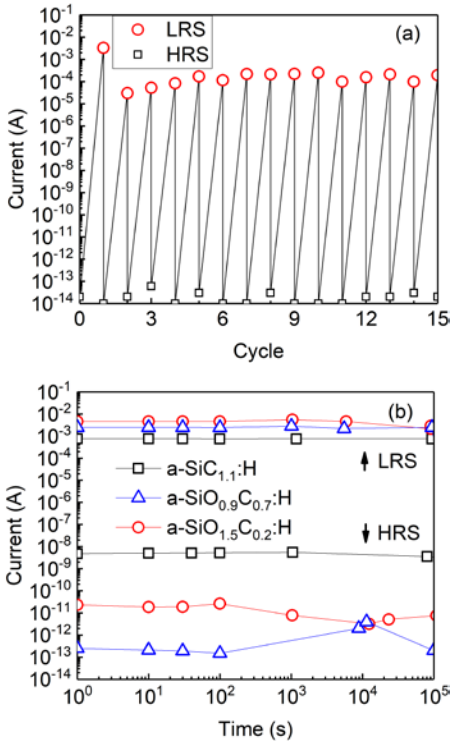

FIG. 4. (a) LRS and HRS currents in switching cycles of a W/a-$SiO_{1.5}C_{0.2}$:H/Cu RM. (b) Retention obtained from W/a-SiO_xC_YH/Cu.

Conclusion

W/a-SiO_xC_y:H/Cu RMs composed entirely of native BEOL materials were fabricated. Resistive switching with ultrahigh ON/OFF ratios in the range 10^6 to 10^{10} were observed. The analysis of detailed I-V characteristics suggests the Ohmic conduction in the LRS are attributed to the formation of Cu filament. Also, the a-SiO_xC_y:H Schottky contacts in pristine state and HRS lead to Schottky emission conduction mechanisms and ultrahigh resistance. 10^5 s retention at room temperature were measured. Long retention, supreme BEOL compatibility, and high ON/OFF ratios suggest promising application potentials of W/a-SiO_xC_y:H/Cu RMs. Moreover, the composition of the a-SiO_xC_y:H switching layer has shown influences on V_{FORM} and V_{SET}, and current conduction mechanisms.

Acknowledgements

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