UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Electronics and Computer Science

Reliability of Analogue Circuits

by

Illani Mohd Nawi

Thesis for the degree of Doctor of Philosophy

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Reliability of Analogue Circuits

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ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING
Electronics and Computer Science

Doctor of Philosophy

RELIABILITY OF ANALOGUE CIRCUITS

by Illani Mohd Nawi

The reliability of CMOS circuits has worsened due to technology scaling. From the review of previous work on reliability study for CMOS circuits, it has been found that both digital and analogue circuits were susceptible to single event effects. Single event effects although causing non-permanent errors have already been identified to have caused billion of dollars worth of lost. Single event transients have been established as one of the single event effects which may reduce the reliability of analogue circuits and safety critical systems, in general. The impact of radiation effects on analogue circuits has been investigated in this thesis using circuit-level single event transient modelling. The characterization of impact of single event transient has been investigated for several analogue circuits. These analogue circuits; namely operational amplifier and comparator, have been recognized to be susceptible to single event transients. Several influencing factors have been associated with previous works and this study to have impacts on the severity of the single event transients to these circuits. Sensitivity analysis has been completed to determine the most and the least sensitive transistor to be used in the variability analysis. The variability analysis addresses the impact of the influencing factors and this information may be used in finding the trade-off which exists between the influencing factors and single event transient. These trade-offs may also be used in mitigating the single event transient. A simple mitigation technique still at preliminary stage has also been included, as part of this study.

Contents

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To my late father and mother, I miss both of you so much and I dedicate this to both of you. To Umi, thank you for every prayers. I love you.

To my spouse, things have been rough for the past 7 years. I hope the gap left between us would be able to be patched in time.

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To my siblings and their family, as a part of the entity who made me what I am today.

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To Tracy and Christelle, I wish our friendship will not end here.

This is to the start of a new journey.

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Nomenclature

AC	Alternating Current
ADC	Analogue-to-Digital Converter
AOS	Auxiliary Offset Storage
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
BICS	Bulk Built-In Current Sensor
BWCA	Binary Weighted Capacitor Array
CERN	European Organization for Nuclear Research
CMOS	Complementary Metal-Oxide-Semiconductor
COTS	Commercial-On-the-Shelf
CPU	Central Processing Unit
DAC	Digital-To-Analogue Converter
DC	Direct Current
DCE	Digital Communications Experiment
DOE	Design of Experiments
DRAM	Dynamic Random Access Memory
DSR	Digital Store and Read Experiment
EDAC	Error Detection and Correction Circuit
EEPROM	Electrically Erasable Programmable Read-only Memory
EOC	End-of-Conversion
FIT	Failures-In-Time
FPGA	Field Programmable Gate Array
FSR	Full Scale Voltage Range
GPS	Global Positioning System
HCS	High-Conduction-State
IBM	International Business Machines Corporation
IC	Integrated Circuit
ICARE	Influence of Space Radiation on Advanced Components
ICMR	International Commission on Radiological Units and Measurements
ICS	Intermediate-Conduction-State
IOS	Input Offset Storage
LCS	Low-Conduction-State
LET	Linear Energy Transfer

LSB	Least Significant Bit
MTF	Multiple Transient Fault
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
MOSRA	Metal-Oxide-Semiconductor Reliability Analysis
MSI	Medium Scale Integrated
NBTI	Negative-Bias Temperature Instability
NMOS	N-type Metal-Oxide-Semiconductor
Op Amp	Operational Amplifier
OOS	Output Offset Storage
PMOS	P-type Metal-Oxide-Semiconductor
PWL	Pulse-Width-Length
RAL	Rutherford Appleton Laboratory
RDF	Random Dopant Fluctuations
RE	Relative Error
RHBD	Radiation-Hardening-by-Design
SAR	Successive Approximation Register
SEE	Single Event Effect
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SiGe	Silicon Germanium
SNR	Signal to Noise Ratio
SOI	Silicon-On-Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
ST	STMicroelectronics, Inc.
STFC	Science and Technology Facilities
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TSMC	Taiwan Semiconductor Manufacturing Company
VLSI	Very-Large-Scale-Integration
Q_{crit}	Critical Charge
Q_s	Charge Collection Efficiency

Chapter 1

Introduction

CMOS reliability issues emerge from the increasing scaling rate of CMOS technology. The scaling trend is in demand due to the increasing performance requirements and competition for better electronic products. These products required improved performance for meeting the speed, complexity, circuit density and size, power consumption and cost requirements, with some drawbacks. This motivates the sudden increase in the study of reliability and variability of CMOS circuits, both at pre- and post-fabrications stages.

With these scaling advancements, comes more technical challenges in the form of CMOS reliability issues as further classified by Maricau [1], the spatial and temporal unreliability effects. Spatial effects exist immediately after productions and fixed in time while temporal effects are time-varying effects, which changes based on the operating conditions of the transistor or circuit, such as the operating voltage, temperature, switching activity, presence and activities of neighbouring circuits. These spatial effects also known as hard errors, could be corrected much earlier during the fabrication process while temporal effects or soft errors may need innovative mitigating solutions. At the same time, these solutions although may reduce the soft errors, it may not satisfy the design constraints specified by users. Design trade-offs as one of the mitigation technique may be helpful in reducing the sensitivity of a particular circuit to these errors, however, there are cases where these issues are no longer preventable and have to be corrected with state-of-the-art mitigation techniques. Some of these techniques, unfortunately, are very costly.

In soft errors, new electron-hole pairs are generated from the particle strikes initiated from the radiation source. This new electron-hole pairs would not affect the circuit permanently, thus termed as 'soft' errors; as opposed to hard errors [2]. Soft errors are also termed as transient faults or single event effects (SEEs). Although soft errors are a non-permanent causal of malfunction; it has been reported that a single soft error has

caused an interleaved system farm to fail and in a different incident, halted a billion-dollar automotive factory operation; which has raised a major concern [2].

Backgrounds on the radiation effects in safety-critical systems and its impact to VLSI and analogue circuits were briefly reported in this chapter. Section 1.1 outlines the radiation effects occurring in safety-critical systems, which have been the cause of failures and potential-failures as reported by various sources. Section 1.2 briefly describes soft errors and discusses the existence of soft errors in VLSI circuits while Section 1.3 discusses the observation of single event transients for analogue circuits. On the other hand, Section 1.4 provides the overview of some of the existing soft error mitigation techniques and the current trends. Motivations and research objectives have been described in Section 1.5. The thesis organization has been described in Section 1.7. And finally, Section 1.8 listed the parts of completed work which have been submitted for publications and workshops.

1.1 Radiation Effects in Safety-Critical Systems

In this thesis, focus is only given on radiation effects which are caused by alpha particles and neutrons. This is due to the fact that soft errors caused by radiation effects contributed by alpha particles and neutrons have a higher contribution towards overall soft error rate as opposed to soft errors which were generated from electrical noise from cross talk and interference in power supply [1]. The alpha particles come from the decaying packaging and bonding materials while neutrons come from the atmosphere and its environment [2]. Further descriptions of the radiation-induced faults have been elaborated in Section 2.1.

The impact of radiation effects caused by in-orbit sources has been well documented as reported by Ecoffet in his work [3]. He mentioned that radiation effects have become a major contributor towards space anomalies, as reported by The Satellite News Digest [4]. The Satellite News Digest reported on a weekly basis, any incidents and failures both on-board electronics on satellites and on ground controllers. Although the digest is a non-official collection of satellite failures reported, the author, Klanowski [4] claimed the sources referred to are believed to be reliable. Ecoffet [3] in his work, highlighted the intense solar activity reported by [4] during October to November of 2003; which has caused at least 2 space anomalies per day from 23rd of October 2003 to 6th of November 2003. These space anomalies are caused by various radiation sources which are the protons and electrons from the radiation belts, ions and protons from solar flares and ions from cosmic rays [3]. The latest reported satellite failure caused by radiation effects was to EchoStar 8 in January 2011. The satellite has temporarily been off its course after a single event upset being detected [4]. No other satellite failures are declared

to be caused by radiation effects based on the latest weekly update checked on February 20th, 2018.

Based on the reported high degree of space anomalies in 2003, up to 10% satellites will experience operational outages from hours to days from a modest solar storm as judged by The Royal Academy of Engineering [5]. Solar storm or also known as solar flares, is a sudden eruption of matter and energy on the sun above a sunspot, believed to be caused by sudden release of magnetic energy [6, 7]. In easier definition, solar flares are high intensity radiation bursts [8]. Within few minutes, the flares will be able to reach its maximum brightness and may last for hours [6]. These flares are believed to be incapable in affecting humans on ground levels, however extreme solar flare may affect the atmosphere layer where GPS and communication signals travel [8]. The solar flare strength fluctuates in 11-year cycle, with 4 quiet years followed by 7 active years [9]. 11-year cycle is taken as the duration of a solar cycle as the sun's geomagnetic poles change direction in successive 11-year cycles [9]. The solar storm will not only trigger the outages but also increases the ageing of the satellites. Although the phenomenon of a super storm, which is the extreme solar flare event has never been encountered, the highest recorded radiation effects measured on spacecraft in October 2003 has already caused major damage to spacecraft, as reported earlier by [3, 4]. The highest intensity solar flare reported by [3, 4], was recorded by astronomers using the Solar and Heliosphere Observatory (SOHO) satellite [6]. The most recent significant solar flare has been detected on September 10th, 2017 [8]. With the limited knowledge and still ongoing research work such as by Engell et al., [10] and Murray et al., [11] in predicting the solar storm's occurrence and its impact, efforts shall be made on improving the susceptibilities of spacecraft and avionic electronics towards radiation effects.

These satellites if being used for projecting TV channels i.e. trivial communication data, non-permanent error suffered by these satellites may not be as significant as compared to being used in, for example, a real-time emergency alert system for earthquake [12] or tsunami [13]. The Great Tohoku earthquake which happened on the 11th of March 2011, has been considered a massive disaster and heartbreaking; thus a real-time emergency alert system which uses efficient, fault-free and dependable real-time GPS geophysical system may be helpful to encounter future events.

Soft errors caused by radiation sources are not only known to impact electronic devices for aerospace and avionic applications but also has given a significant impact on electronics at earth level. These devices in applications such as aerospace, avionics, automotive, medical, weaponry and nuclear systems are all classified as safety-critical systems [14]. The impact will worsen by orders of magnitude when the electronic devices are implemented in aerospace applications and in both commercial and military aircraft due to the higher atmospheric neutron flux [15]. Nevertheless, devices located at the earth level may be exposed to higher radiation effects. The sensitivity of devices may also be influenced by several factors, which have been further elaborated in Section 2.6.

1.2 Soft Errors in VLSI Circuits

Soft errors in VLSI circuits exists due to the radiation-induced particles; such as neutron in the atmosphere due to the cosmic rays and the alpha particles from the packaging materials [2]. These particles generate new electron-hole pairs which are later collected by transistor source and diffusion nodes; where a sufficient accumulated charge will invert the logic device's state, from a 1 to 0 and vice versa. This is particularly true in digital circuits. Analogue circuits on the other hand experience different effects. Studies made by injecting single transient error into analogue circuits concludes soft error will effect the analogue circuit's performance [16]. Even though analogue circuits experience different effects, the physics of charge generation, transport and collection of soft errors characterized from digital circuits, are deemed similar in any types of circuit, thus it's theoretical knowledge can also be applied to analogue circuits [17]. Koga [17] also mentioned that it is reasonable to also designate the upsets in analogue circuit as single event upsets (SEUs), similar to digital circuits. Due to this justification, the modelling of single event effects used in digital circuits is also commonly used for modelling single events in analogue circuits, as further elaborated in Section 2.5.3.

Soft errors can sometimes be mistakenly identified as a single data which may cause non-permanent changes to the circuit operation. The errors which are successfully being detected may be corrected using error correction method. It is sometimes impossible to detect the existence of these errors or to determine the actual data to be compared with, thus fault tolerant circuit is implemented. Soft errors caused at device level may have little effect due to the advancements of the packaging materials; however, as the technology being vigorously scaled down, VLSI circuits are returning to become more vulnerable [18]. Similar to the device level mitigation using packaging materials, circuit and architectural level techniques developed earlier may or may not be able to tolerate the soft errors which have increasingly become more aggressive.

1.3 Single Event Transients in Analogue Circuits

One of the types of soft errors is the single event transients (SETs). SETs in digital circuits are only visible when they are converted into single event upset; for example when the SET change the supposed output or information in a memory circuit, while SETs in an analogue circuit must be propagated to usually its digital counterparts in order to be detected as an error [19]. Comparators are commonly used in analogue to digital converters (ADCs) and sensors, as highlighted in one of the application presented by Analog Devices for space applications in Figure 1.1. Operational amplifiers on the other hand are used mostly in sensors, such as the accelerometer in Figure 1.2 developed by Analog Device, suitable for space applications. Most of the time, the SETs detected in analogue circuits will not produce any long term or continuous effects on the analogue

device but may initiate prolonged effect on the follow-on circuit especially if the error has been latched and used for consequent stages. An irradiated comparator has been observed to experience disturbance pulses which are visible at the intermediate nodes, but only being reflected either by a missing bit or having additional bit at the comparator's output. As opposed to operational amplifiers, comparators are much easier to be identified as a failure; due to the dimensionless bits.

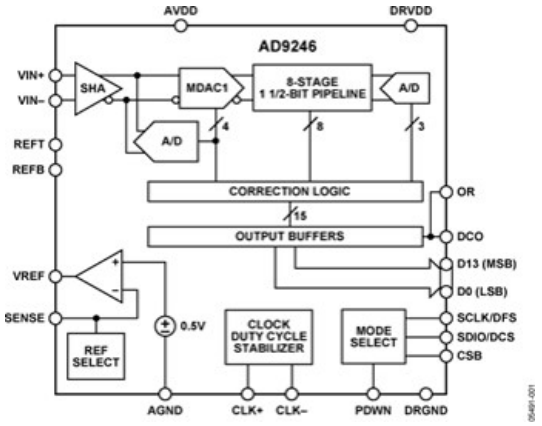


Figure 1.1: Analog Devices AD9246 Analogue to Digital Converter [20]

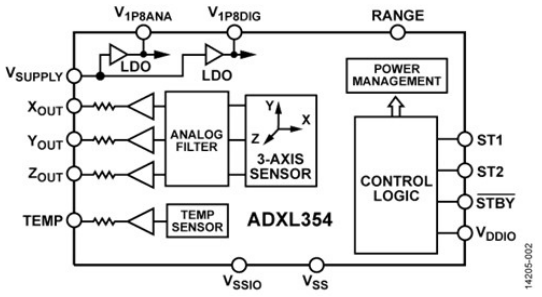


Figure 1.2: Analog Devices ADXL354 Accelerometer with Analogue Output [21]

While [16] mentioned that soft errors in particular single event transients will affect the circuit's performance, [17] has observed that operational amplifiers exhibited a short-duration disturbance pulses. In particular, Koga et al. [17] has observed single event upsets in several bipolar analogue devices; the HS3530RH, OP-05 and OP-15 operational amplifiers irradiated with heavy ions and concluded these devices have experienced either positive or negative-going short-duration disturbance pulses. The difference in pulse's amplitude values suggests that even for the same type of circuit i.e. operational amplifiers, the impact of SET to these devices varies. The differences may be due to the topology of the operational amplifier under investigation, or other influencing factors, which are discussed in Section 2.6. The varying amplitude values yield that the type of circuit alone does not guarantee the level of sensitivity a circuit portrays.

SETs are considered a threat for space electronics as transient pulses, if not corrected or filtered, will propagate from the sensitive device into the overall system and later cause either temporary or permanent failure of the electronic systems [22]. As electronic systems control most of the operations in spacecraft and other safety-critical systems, this will cause a part or the whole operation to halt. Although no official report has been published on the actual failures or serious operational problems caused by SETs in analogue electronics in other safety critical systems such as for automotive or biomedical applications; the prediction of a super storm has initiated efforts in improving the susceptibilities of other safety-critical systems, as mentioned earlier in Section 1.1.

1.4 Current Trends in Soft Error Mitigations

The mitigations of soft errors or single event effects may be repaired by error detection and correction (EDAC) circuits or algorithm in a system's software. A well-known example of EDAC is triple modular redundancy (TMR). TMR is based on the concept of using 3 similar designed circuit which is made to be able to run in parallel and compared with each other. This concept is termed as redundancy. For example, after the processing is completed for all three circuits, if one circuit provides a different answer than the other two, it is believed that the two other circuits produce the correct answer. Hence, the answer to this particular calculation or algorithm is loaded from the correct answer. The one circuit or system which produces a different answer is reset or corrected [23]. Redundancy, although proven to cost more, is commonly used in digital circuits. On the other hand, examples for error correction for analogue circuits at design or circuit-level, are the usage of analogue redundancy in the form of majority or mean voter to eliminate the error found [24, 25] or applying trade-offs such as modifications of the bandwidth and gain of an amplifier circuit using feedback resistor to reduce the sensitivity of the analogue circuit [26]. Other mitigation methods which have been used is by using the circuit techniques for reducing the imperfection of amplifier such as auto-zeroing suggested by [27] and has been implemented by [28] and [29] into comparators. In general, both digital and analogue circuits can be mitigated using a device, circuit, layout or packaging techniques; which is commonly practiced in the industry. A comparator circuit identified for characterization of its radiation effects is said to be problematic when the transient effect is latched by some memory mechanism. The latched signal may be propagated to its digital counterparts or subsequent circuit which later causes the whole system to fail or produces the wrong data. If this particular signal is unable to be detected by the error correction circuit at system-level, a lower level mitigation circuit must be implemented. The importance of finding circuit-level mitigation techniques for the selected circuits in this thesis has been further justified in Section 2.3.3.

1.5 Research Motivations and Objectives

The increasing reliability concerns motivate the study of radiation effects, particularly on CMOS circuit. The majority of radiation effects analyses are performed on commercial-on-the-shelf components (COTS) and in particular, analogue circuits; are built on bipolar technologies. Only recently, analogue electronic circuits are built on CMOS or other material such as BiCMOS or SiGe. And only recently, radiation testing has been performed on these devices. Studies made on analogue electronics under radiation effects suggested that SETs affect the performance of the analogue circuit or in some cases, exhibited short-duration disturbance pulses; which in most cases fades away during operation. The reported variations of the shape and duration of these disturbance pulses have sparked the motivation to study the impact of SETs on several selected analogue circuits, especially on influencing factors which may have impacts to the sensitivity of the circuits to SETs and may have caused the increase in failures. Based on these motivations, the following objectives have been set.

- Firstly, to clarify whether all analogue circuits suffer the same impact to the susceptibility of the circuits to radiation effects, and how SETs affect the comparator's behaviour and eventually cause failures to the device or the overall system. In general, all analogue circuits have been identified to be sensitive to single event transients, however as the disturbance pulses exhibited at the output varies for even the same type of analogue circuit; further investigations shall be made on selected circuits. Several different analogue circuits need to be selected with proper justifications. These circuits are to be characterized using circuit-level modelling.

- Secondly, to investigate whether the analogue circuit's sensitivity to single event transient worsens under variability. Variability relates to design factors which may or may not influence the sensitivity of the selected analogue circuits. From literature reviews, these factors are identified to be influencing the sensitivity of the similar circuits, either in a positive or negative way. From observing the impact of these factors, some trade-offs between these factors and performance parameters may be summarized; which later may be used in mitigating the single event transients.

- Finally, for circuits which have been identified to be sensitive to single event transients and may cause malfunctions to adjacent circuits; a simple mitigation technique shall be suggested. Mitigation technique suggested can be in the form of trade-offs between the design factors and performance parameters or corrections of the single event transients.

1.6 Contributions

The main objective of this thesis completion is to suggest on methods on improving the sensitivity of circuits or a system to soft errors by means of mitigations. There is no actual dynamic design flow or methodology in soft error mitigation published by any, however, the common practices by researchers in mitigating digital circuits using computer simulations has been summarized and reported, in Section 2.2. This thesis has been completed based on the summarized dynamic mitigation design flow.

This thesis has also concluded that

- All analogue circuits studied in this work have been identified to be sensitive to single event transients, however to different level of sensitivity.
- Certain factors have significant impact on the sensitivity of the selected circuits based on completed characterization study.
- A simple mitigation technique using capacitors on the sensitive nodes has improved the sensitivity of the overall circuit to soft errors, particularly single event transient.

1.7 Thesis Organization

Chapter 2 provides the literature and background which have been reviewed in order to complete this research. Chapter 2 further elaborates the phenomenon of radiation-induced faults and in quantifying soft errors. Some of the important terms in physical-level modelling have been introduced here. Chapter 2 reported the characterization of COTS devices and also, several non-COTS devices. The general operations of selected analogue circuits with selected topology are described in Chapter 2. Chapter 2 has also included the initial design stages for the 2-stage operational amplifier and the two comparators with some performance specifications obtained from preliminary simulations.

In Chapter 2, the chosen circuit-level modelling for single event effect is further described, together with some recently improved models. In addition to these subjects, the factors which are deemed influential to the sensitivity of a device to SETs have been described. The statistical tool used for investigating the impact of variability is also described in Chapter 2. Several circuit-level mitigation techniques have been reported briefly in Chapter 2, although not being tested on implemented device in this thesis.

Upon completion of implementation and design of amplifier and comparators, each device has been tested for its sensitivity to single event effects as reported in Chapter 3. The initial design for 2-stage operational amplifier and the two comparators are included in Chapter 3. A simple SPICE level single event modelling is described and used to model

the particle strike to these circuits. A sensitivity analysis has been performed on each device in order to identify both the most and the least sensitive transistors. The result from the sensitivity analysis is used for variability analysis in Chapter 4.

Variability analyses are performed on the two variations of comparators, hysteresis-free comparator and comparator-with hysteresis in Chapter 4. The correlations between several factors, such as scaling and impact of temperature on the severity of single event effects have been reported and presented based on Design of Experiment(DOE) technique, particularly for a hysteresis-free comparator. On the other hand, several influencing factors for comparator-with-hysteresis characterization, such as differential input voltage, hysteresis and ageing are also analyzed and reported in Chapter 4. A preliminary mitigation to the circuits using capacitor has also been reported in Chapter 4.

Chapter 5 acts as the concluding chapter on the findings from the work completed for this thesis. Future work has been suggested focusing on the influencing factors that may be used as trade-offs in the mitigation process of the circuits. On top of that, further investigations as part of future work must be performed as a continuation to the preliminary mitigation technique applied in Chapter 4.

1.8 List of Publications

Parts of this thesis have been published in the following:

Nawi, I.M, B.Halak, and M. Zwolinski, "Reliability Analysis of Comparators", Designing with Uncertainty: Opportunities and Challenges Workshop, 13th March 2015, Grenoble, France.

Nawi, I.M, B. Halak, and M. Zwolinski, "Reliability Analysis of Comparators", PhD Research in Microelectronics and Electronics (PRIME), 29th June to 2nd July 2015, Glasgow, Scotland.

Nawi, I.M, B.Halak, and M. Zwolinski, "Ageing Impact on a High Speed Comparator with Hysteresis", Workshop on Early Reliability Modelling for Ageing and Variability in Silicon Systems (ERMAVSS), 18th March 2016, Dresden, Germany.

Nawi, I.M, B.Halak, and M. Zwolinski, "The Influence of Hysteresis Voltage on Single Event Transients in a 65nm CMOS High Speed Comparator", IEEE European Test Symposium, 24 to 27th May 2016, Amsterdam, The Netherlands.

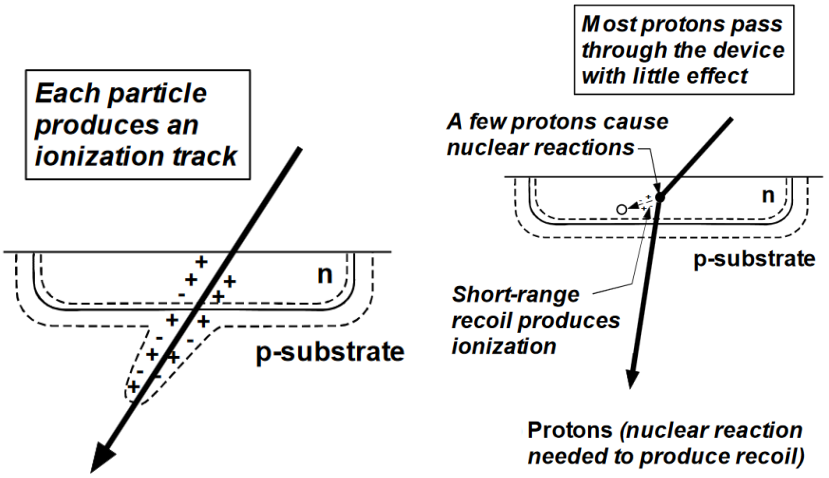
Chapter 2

Literature Review

This chapter includes the literature reviewed and background study taken to understand the basic concepts on soft errors caused by radiation sources. The impact of soft errors on analogue circuits have been reviewed and the existing characterization, modelling and mitigation of selected soft errors have also been reported. On top of that, the general operations of selected analogue circuits have also been included.

2.1 Radiation-induced Faults

Radiation-induced faults are caused by two sources, which are alpha particles and neutrons. These two particles introduce errors in the silicon chips in the same way for both analogue and digital circuits. However, the effect of particle strikes on the digital and analogue circuits may be different [2]. Alpha particles affect the semiconductor devices by creating a track of electron-hole pairs as the particles pass through the substrate of the transistor which results in ionization as illustrated as in Figure 2.1(a). If this ionization come in close contact with the depletion region of the gate, it will cause the electric field to rapidly collect the carriers; which later create a voltage or current glitch at the gate's node. If the track of electron-hole pairs is further away from the depletion region, a smaller charge will be collected hence very unlikely this will cause a current or voltage glitch [30]. But, as the distance between the track and the depletion region is reduced, the higher the charge being collected. A minimum point at which the charge required to disturb a chip's reliability or to cause a circuit to malfunction is termed as the critical charge, Q_{crit}. This value is estimated by repeatedly running a circuit with different current pulses injected until the circuit fails. If the collected charge exceeds the critical charge, then the chip may experience soft errors. A higher critical charge may reduce the soft error rate, but the chip will experience slower operation and higher power dissipation.



(a) Direct Ionization (b) Indirect ionization

Figure 2.1: Radiation-induced elements hit the silicon layers and produces ion tracks either by direct or indirect mechanisms [31]

On the other hand, neutrons do not have a direct impact on electrons to create similar ionization. When the neutrons hit the silicon layers or other atoms, secondary particles such as protons, neutrons, pions, are created [32], and later may create similar ionization track of sufficient electron-hole pairs. These secondary particles are capable of producing electron-hole pairs which may cause transient faults in a device, however, such a collision has a very low probability as compared with alpha particles. The collisions of neutrons with other heavier atoms may also create a reaction energy that being deposited along their travelling path, thus resembles direct ionization caused by alpha particles as illustrated in Figure 2.1(b). This ionization is termed as indirect ionization [32]. In addition to this, higher volumes of neutrons are required to produce the same number of transient faults exhibited by a device affected by alpha particles. In other words, alpha particles may have a greater effect in contributing towards soft errors.

2.2 Dynamic Mitigation Design Flow

Before proceeding with the mitigation process of selected circuits, a methodology needs to be properly outlined. As already stated in Section 1.6, there is no actual overall dynamic mitigation design flow published by any either in digital, analogue or mixed signal design community. Stamenkovic et al., [33] only reported the design flow focuses on applying suggested fault tolerant techniques particularly for ASICs, while Pontes et al. [34], proposed a design flow focusing on modelling single event effects at system level for digital circuits. However, after reviewing the majority of work completed by digital designers, a summary comprising the methodology normally practised in mitigating circuits under radiation; the following design flow in Figure 2.2 has been produced.

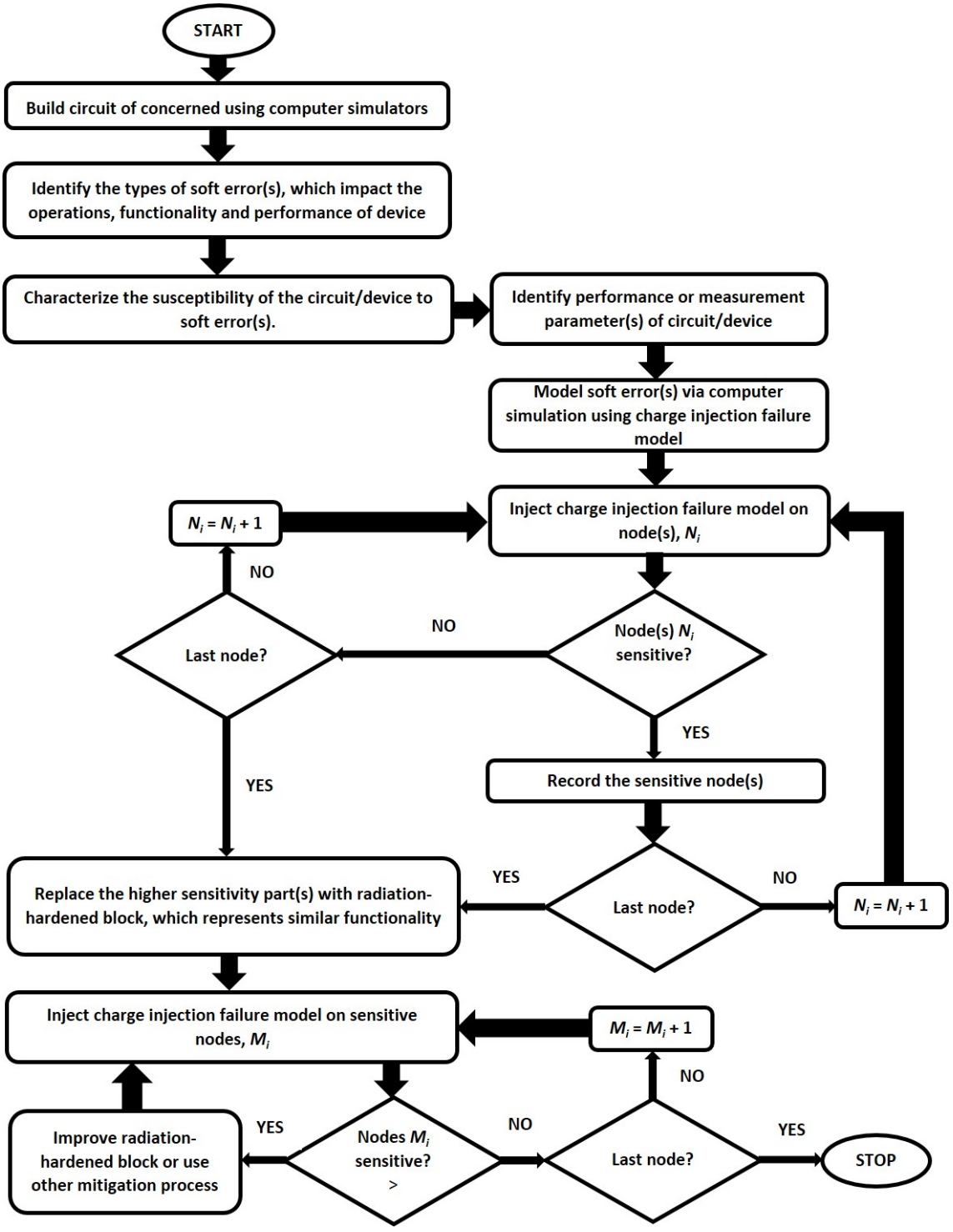


Figure 2.2: Dynamic Mitigation Design Flow

The mitigation process of selected circuits has been summarized based on a mitigation design steps on correcting digital circuits, as reported by [35, 36, 37, 2, 38] The dynamic mitigation design flow as shown in Figure 2.2, although summarized based on digital circuits, has also been used for mitigating analogue and mixed signal circuits as described by Askari and Nourani [25]. In [25] however, the improvements of sensitive parts has been

established by expanding the sensitivity analysis followed by systematic optimization of the number of redundancy blocks, as part of improving sensitivity of the mixed-signal circuit.

The mitigation methodology commonly used in improving the sensitivity of digital, analogue and mixed signal circuits has initiated several automation tools in characterization selected soft errors. [39] reported there are several tools available in analyzing the soft errors in VLSI circuits, such as GRAS (Geant4 Radiation Analysis for Space) [40] and MRED (Monte Carlo Radiative Energy Deposition) [41]. These tools have been used to analyze radiation at system level while Marquez et al. [39] proposes a fault tolerant debugging tool for analogue and mixed-signal circuits at transistor level, designated as AFTU (Analogue Fault Tolerant University of Seville Debugging System).

2.3 Single Event Transients Characterization in Analogue Circuits

Analogue circuits consist of operational amplifiers and comparators. These circuits are identified to be the components commonly used for safety-critical systems [2, 16]. Thus, it is essential to review work completed on the characterization of SETs for circuits such as amplifiers and comparators for the past few decades. Section 2.3.1 and Section 2.3.2 describes the characterizations made on operational amplifiers and comparators; which mostly are bipolar circuits. Section 2.3.3 explained on a particular topology of comparators which are deemed problematic due to its feedback mechanism. Section 2.3.3 also described an application where the comparators seemingly are liable to cause a system's failure if the comparator has been struck with the radiation fault.

2.3.1 Single Event Transients in Operational Amplifiers

Most characterization work that describes SEEs in analogue circuits are accomplished via physical experimental work either by heavy ion beams irradiation or by laser pulses injected into the analogue chips; which seems impossible to repeat in an environment with limited resources [17, 42, 43]. Koga in their work used xenon ion in irradiating the chips under test. The pulse generated by xenon ion has 6.5V peak amplitude, lasting about 100 ns and later followed by a gradual trailing section which lasts more than 1 microseconds [17]. Ecoffet supported Koga's work by applying the same test method in characterizing the transient effects onto various amplifier devices [43]. Adell, on the other hand, used both device and circuit level simulation to study the effects of radiation towards analogue circuits, particularly op-amps. Adell's work generally studied the transient effects and also to investigate the most sensitive part of the device [42]. By comparing the experimental results obtained from the Physical Nuclear Institute,

Adell's work has been able to reproduce the actual data using both device and circuit level simulation. It is worth to say that Adell's work is based on bipolar amplifier testing which may give a different impact as compared to MOSFET transistors. Most of these characterizations are performed in a well-equipped laboratory thus this has drawn a certain limitation to the majority of the ongoing SEE characterization work. With that in mind, it is essential to have a low-cost characterization platform for analogue circuit testing.

Since it is very important to be able to understand why a circuit behaved in such a way in order to design a fault-tolerant system and to characterize a device in a more accessible method, Boulghassoul et al. in both [44] and [45] has studied the response of LM124 operational amplifiers to SETs using circuit-level modelling. Boulghassoul et.al [44], used computer-simulated frequency domain analysis to study the impact of SEEs towards general purpose op-amps. [44] tried to answer the question of why such op-amps impacted with SEEs behaved in a certain way using the relationship between the frequency spectrum of SET and frequency response of the operational amplifier's internal circuit blocks. In studying the impact of frequency on SETs, it has been shown that SET's amplitude increases in high speed circuits. This is due to the findings that SET pulse-width experiences amplification through the large bandwidth offered by high speed circuits [44]. While [44] studied the frequency profile, [45] concentrated in the time domain analysis. This particular work [45] outlined the development of an accurate transistor-level model of the LM124 op-amp for analogue SETs computer simulation. An appropriate predictive SEE model has been identified to be used as part of simulation methodology to match the physical testing of radiation effects on LM124 amplifiers. The model heavily depended on datasheet specifications and laser probing testing which in the end, although suitable for broad-beam SET predictions; has been deemed still insufficient for modelling other SETs in analogue components. This is because only devices similar to the ones tested in [45] may use the same SET model specifications. This limitation of not being able to exactly model SET using just SPICE modelling, however, has not been thoroughly addressed as to date. Some other completed circuit-level characterization of SETs made on analogue circuits are by [16, 46, 47, 48]. [16, 46, 48] have characterized SET of operational amplifiers by implementing folded cascode amplifiers while [47] characterized a 2-stage amplifier.

2.3.2 Single Event Transients in Comparators

Another type of commonly used analogue electronic circuit are comparators. Johnston [49] in his work mentioned that the transients faults in comparators are more important than the transients faults in op-amps, as comparator usually drives digital circuits which in return may be triggered into an erroneous condition from a single short duration transient fault. This is particularly true in an asynchronous circuit [49]. This

is considered an exceptional case for analogue circuits since comparator is the interface between analogue circuits and the digital processing systems, particularly in analogue to digital converters (ADCs). In order to characterize the transients in a comparator, one can measure the SEEs in comparators by using single event upsets (SEUs), a well-known measure in describing soft errors in digital circuits [50]. This is supported by the fact that although analogue circuits experience different effects to single event effects, the physics of charge generation, transport, and collection of the single event effects characterized for digital circuits; are considered similar provided it originates from the same source with the same strength, as stated by [17]. Zhao [50] in his work studied the impact of radiations towards a latched comparator, particularly for SOI CMOS technology. He has chosen SOI technology due to simplicity; since generated charges from radiation will not migrate to other devices as in the case of bulk CMOS. However, SOI technology is more expensive than the conventional bulk substrates and SOI does exhibit parasitic bipolar action which limits the further reduction of soft errors within the device [51].

Earlier in Section 2.3.1, it has been mentioned that the single transient effects on operational amplifiers have been studied for decades using heavy ion injection and pulsed laser injection, which is quite impossible to repeat. Collections of data from injected pulse into the actual analogue IC provides a basis on how much charge is acquired by a chip under single event transient (SET) influence. As Section 2.3.1 reported on the physical characterization of radiation effects on operational amplifiers, some of the work which has been established to portray the actual radiation effects via irradiation of ions to comparator circuits are [49, 52]. Johnston [49] in their work have investigated the impact of radiation onto three actual comparator device using heavy ion tests. Johnston et al., have monitored the transients faults waveforms for three types of comparators by physically removing the lid of each comparator under test to be injected with different types of ions.

Johnston et al. [53] in much later work, have characterized SET in bipolar comparators, namely LM119, AD790, CMP401. Similar to Koga's characterization of LM119 [54], SET for LM119 tested by [53] has been detected with an additional observation of dependency of SET strength to the differential input voltage. When the differential input voltage, ΔV is increased, the cross section has been reduced by at least 1 order of magnitude for LM119. However, CMP401 has been observed to be less dependent on the differential input voltage, which may be due to the BiCMOS comparator design. A repetition of SET characterization of a number of 139-type comparators from several manufacturers has been completed by [55] and proven consistent with other characterizations by [53, 56]. 139-type comparators from these characterizations are believed to be highly dependable on the voltage difference of the two comparator inputs, or also known as differential mode voltage, ΔV.

139-type comparators are commonly used in space electronic applications, as reported by Harboe Sorenson [57] and Johnston [49]. Generally, 139-type comparators are designed

to operate using single power supply voltage over a wide range of voltages, with the input common mode voltage range includes ground levels. The collections of comparators operating this way have been identified as 139-type comparators [58].

Other types of comparator topology which have been investigated for its sensitivity to SETs are the comparator-with-hysteresis [59], folded cascode comparator and inverter comparator [28] and dynamic comparators [60]. Roche et al. [59] reported the flip-flop effects from the SET current strikes in a bipolar comparator-with-hysteresis, occurring when the input voltage is within the hysteresis band range. In [59], the comparator-with-hysteresis has been implemented using a LM124 op-amp with hysteresis effect added.

Both folded cascoded comparator and auto-zeroed inverter comparator proposed by Mikkola have been identified to be SET sensitive [28]. Even with auto-zeroing technique implemented, the inverter comparator exhibits a SET duration of 9 ns. For a slow clock cycle applications such as 100 MHz used in [28], the duration lasted for a single clock cycle; thus the detected SET if propagated to its digital counterparts shall be able to be detected and corrected by error detection and correction (EDAC) circuit. This becomes problematic for frequencies more than 100 MHz for this particular comparator topology, as the single error now will be sampled at a higher frequency and cause multi-cycle error.

[29] extended the work by Mikkola by comparing an auto-zeroed inverter comparator based on a folded cascode comparator and made a comparison on the sensitivity of these circuits. They have proved that the auto-zeroing inverter comparator has better tolerance to SETs as compared to folded cascode comparator. Both work by [28] and [29] observed the short disturbance pulses at its output, similar to operational amplifiers. Other types of comparator proven susceptible to SETs are dynamic comparators [60]. From [60], the SETs sensitivity of dynamic comparators depended upon circuit's topology, device's technology or structure and individual transistor's current. On the other hand, as recent as 2014; SETs in CMOS commercial open drain quad comparators, RHD5912 has been characterized by [61]; and proved that the SET sensitivity of this particular comparator is significantly better than the previous bipolar comparators i.e. LM139. This particular comparator, RHD5912, of course, has been radiation-hardened in order to meet the eligibility of space electronics which makes it logical to have an improved susceptibility to SETs. In other technology such as SOI CMOS, the comparator designed has also been confirmed on its sensitivity towards SET, particularly in the duration between reset and latch stages [50].

From the reported characterization, the majority have used the commercial-over-the-shelf (COTS) devices while only a few has looked into different topologies of amplifiers and comparators and studied them at circuit-level. As most circuit-level characterization dated almost or more than a decade and running at a larger feature size such as 90 nm for CMOS amplifiers [62] and 90 nm for CMOS comparators [60], with the belief that

technology scaling have significant impact on the sensitivity of SETs of these devices; characterization in a smaller feature size, is required.

2.3.2.1 Single Event Transients in High Sampling Circuits

As mentioned in Section 2.3.2, SETs that lasted for more than 1 clock cycle in a higher sampling systems will be mistakenly assumed as the correct bit voltage of more than a bit. This is particularly true in combinational circuits [63] and supported by [53].

High speed circuits may increase the number of SET latched or SER, however if the SET current pulse strikes the circuit and has been latched at the clock edge by its digital counterparts, the current pulse may only be visible at the analogue or mixed signal circuits and returns to its working parameters without affecting the operations at systems level. Thus, no matter what the sampling speed or operating frequency of a system where comparator or other analogue circuits resides; the sampling clock edge is the important element in latching the SET strikes. If SET current pulse-width falls onto the clock edge, the wrong current pulse will be latched and may be assumed as correct bit. The bit may resemble the right bit, though.

The SET current pulse-width has been assumed to be under milliseconds long i.e. nanoseconds long however, it has been found that the pulse-width may reach milliseconds long as reported by Boulghassoul et al. [64]. SETs portraying such characteristic would affect a device or a system for a considerable number of clock cycles. Thus, it is always possible for a SET to last more than 1 clock cycle in circuits with high sampling rate, termed as multi-cycle error or multi-cycle transient faults as used in digital circuits.

Migitation method suggested by Mikkola [28] and Tao Wang [29] reduces the pulse-width of SET to at least a single clock cycle. From such conclusion, Tao Wang [29] proposed an offset mitigation technique which has been able to eliminate the SET with a pulse-width shorter than a single clock cycle. For longer SET pulse-width, there were mitigation methods reported by Bastos et al. [65] and Inoue et al. [66], using high level synthesis.

2.3.3 SETs in Analogue Circuits with Memory Mechanisms

A SET in analogue circuits can be problematic when the transient effect is sampled by a latch or some form of memory mechanism and only when the latched signal propagates to the output and subsequently used by other circuits [67]. Comparator-with-hysteresis which is also known as Schmitt Trigger is an example of an analogue circuit which exhibits memory mechanism. Similar to digital memory cells such as SRAM and DRAM, the transient latched in the memory mechanism will cause failure or error to the next adjacent circuit. Schmitt Trigger is commonly used as a noise-compensation circuit and applicable for all the safety-critical systems mentioned earlier in Section 1.1. On

top of that, comparators either with or without memory mechanism such as the ones used in charge redistribution successive approximation register (SAR) ADC, as shown in Figure 2.3 has been identified to be causing the problem if single event transient occurred in the comparator. As opposed to comparators that may be used in a flash Analogue to Digital Converter (ADC), which may allow the SETs generated to be propagated to its digital counterparts and corrected there in parallel for each clock cycle; the SETs generated in a comparator is used as control logic for the switches shown in Figure 2.3, which will decide the next value for the negative terminal of the comparator. If the control logic from the comparator from the previous cycle is wrong, then the next output level will be affected. Either the charge redistribution architecture which comprises of the switches and capacitances must have error correction mechanism or the comparator itself must be radiation-tolerant. Any comparators which are used in application such as SAR ADC, must be mitigated on its sensitivity towards SETs, if possible at circuit-level and not at system-level, as the control logic which contains error bits may be propagated to its next cycle and subsequently passed to its digital counterparts without the system-level error correction mechanism detecting it. This is why only possible mitigation techniques implemented at circuit-level or lower were reviewed in Section 2.8. The only work which has been found to focus on mitigating the SET at the successive approximation register at circuit-level such as by [68, 39]. Other works focused at the system level such as by [69] and [70].

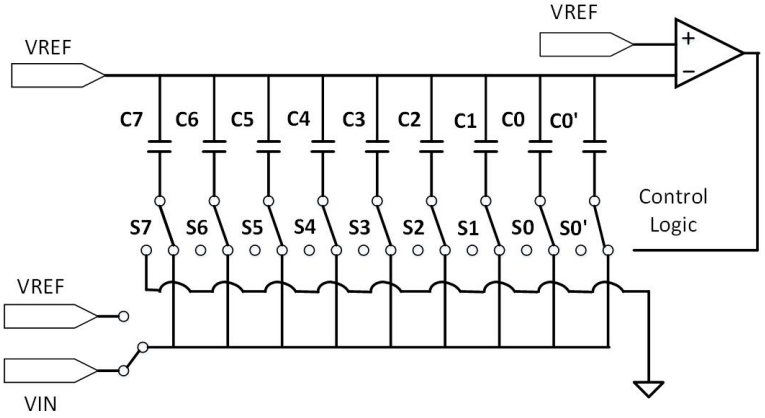


Figure 2.3: Charge redistribution architecture taken from [68]

The detection of SETs in comparator-with-hysteresis has been first realized by Roche [59] in their analysis on a bipolar device. However, as the sensitivity of a device may respond differently towards SETs for a different type of material; the comparator-with-hysteresis under characterization in this thesis has been designed using CMOS technology while Roche's [59] in bipolar technology. Roche et al. used a COTS comparator with external hysteresis mechanism implemented. In this thesis, the comparator has been implemented with a built-in hysteresis mechanism. Roche in their work found the output level of the bipolar comparator-with-hysteresis can be inverted into opposing level i.e. for supposed high-level output, the output becomes low level or vice versa. This happened during SET

injection for input voltage which falls within hysteresis band range. This observation has been termed flip flop effect by [59]. For input voltage that falls outside the hysteresis band range, the output voltage will return to its equilibrium value eventually as the SET pulse is controlled by the feedback effect and similar findings were reported in Chapter 3 and Chapter 4. The output level of this particular comparator will return to the supposed value after a certain duration. During SET injection to the comparator-with-hysteresis, the output will be pulled down to a low level regardless whether the supposed output is high or low and maintains low for as long as equilibrium has not been reached. In the sensitivity and variability analysis completed in Chapter 3 and Chapter 4 however, the hysteresis band range is only 8 mV, thus this hardly allows any space for input voltage variation. It is almost impossible for the input voltage to fall within the hysteresis band range due to the small hysteresis voltage. Hence, the subsequent analyses have been completed to focus only for input voltage outside the hysteresis band range. As characterization process went deeper, hysteresis voltage has been further increased but focus was still given on the input voltage which falls outside the hysteresis band range.

2.3.4 Selected Analogue Circuits for Investigations

From the discussions in Section 2.3.1, Section 2.3.2 and Section 2.3.3, three different circuits have been selected to be investigated for meeting the research objectives stated in Section 1.5. The circuits selected are the 2-stage operational amplifier and a pre-amplifier comparator which have been used as a hysteresis-free comparator running at a slow operating frequency and modified version of the pre-amplifier comparator running at faster-operating frequency and with hysteresis enabled.

As stated in Section 2.3.1, at least 3 groups have concentrated in studying a folded cascode amplifier built as a single stage amplifier [16, 46, 48] while only one focuses on a 2-stage amplifier [47]. Both topologies have been proven to be sensitive to single event transient. 2-stage amplifiers have some significant advantages such as it may achieve higher gain as compared to single stage amplifier and it will be able to be designed to have optimized noise level [71]. Most design requirements of the four amplifier types, which are voltage amplifier, current amplifier, transconductance amplifier and transresistance amplifier have not been able to be achieved by using single stage amplifiers [72]. In reported radiation testing compendiums and other single event transient characterizations, LM124 has been identified as the commonly used component in analogue and mixed signal circuits in space applications [42, 45, 45]. LM124 is a voltage amplifier hence, this thesis progresses to study the characterization of one of the topology of voltage amplifiers. As most practical application did not report in detail of what amplifier topology has been used and multi-stage amplifiers is a better choice in meeting the demanding requirements of amplifiers in safety critical devices, a 2-stage amplifier

has been chosen between the two reported amplifier topology which have been identified to be sensitive to single event transients.

A 3-stage pre-amplifier comparator suggested by [73] has been chosen as it has been proven it will be able to meet medium and high speed requirement of most safety critical systems, as reported by [25]. The 3-stage pre-amplifier comparator chosen has an internal hysteresis mechanism that can be enabled or disabled. Due to this reason, the same comparator will be used in characterizing analogue circuits with memory mechanism, as explained in Section 2.3.3. It is important to clarify at this point, one of the factors which may affect the sensitivity of the comparators are hysteresis, thus, it is essential for a comparator-with-hysteresis to be implemented.

2.4 General Operations and Topology of Selected Analogue Circuits

From the review made on previously radiation characterization work, operational amplifiers and comparators have been identified to be susceptible to radiation effects. This section introduces the basics of operational amplifier and comparators. The basic operations and few topologies are described in Section 2.4.1 and Section 2.4.2, respectively. The comparator basics has also been introduced in Section 2.4.3 and several topologies have been listed in Section 2.4.4.

2.4.1 Operational Amplifier Operations

Operational amplifier works by amplifying small or weak currents into larger and stronger output. Operational amplifiers can be voltage or current amplifiers and normally used for signal conditioning or at signal processing stages. Operational amplifiers receive signals from sensing devices and process the weak signals by amplification and filtering or can also perform other operations such as addition, subtraction, integration, and differentiation depending on the system requirement.

From the ideal operational amplifier illustrated in Figure 2.4, v_1 is the input voltage applied to one of the high impedance inputs, termed as non-inverting input with a positive sign while v_2 is the input voltage applied to inverting input with a negative sign. Two of the three terminals are inputs while another terminal is the output, designated as v_o. A_{OL} is the open loop voltage gain which relates the inputs; v_1 and v_2 with the amplifier's output, v_o by (2.1)

$$v_o = A_{OL}(v_1 - v_2) \tag{2.1}$$

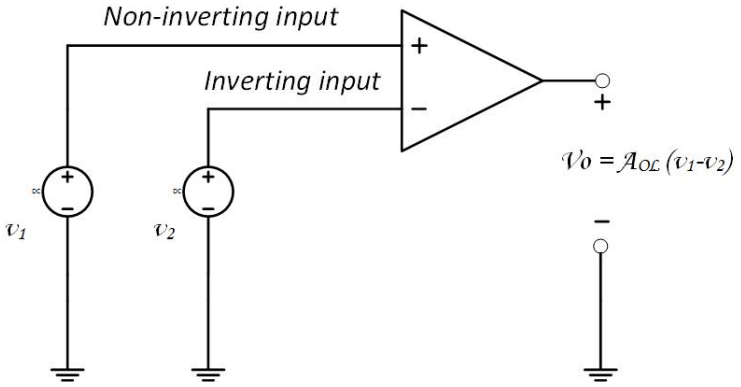


Figure 2.4: Ideal operational amplifier symbol

The inputs and output terminals will determine the types of amplifier, of either voltage, current, trans-resistance and transconductance amplifiers. Voltage amplifier is when the input and output are voltages while a current amplifier is identified when both input and output are currents. When the output is a voltage and the inputs are currents, the amplifier is identified as trans-resistance. On the other hand, when an amplifier has output current and input voltages; it is classified as a transconductance amplifier. In this thesis, the focus has been made on voltage amplifiers.

Two of the voltage amplifiers are the inverting and non-inverting amplifier. Inverting amplifier is obtained by applying a voltage signal to v_2 and the other input grounded, as illustrated in Figure 2.5, while the non-inverting amplifier is achieved by applying a voltage signal to v_1 and zero voltage level to the other input as in Figure 2.6.

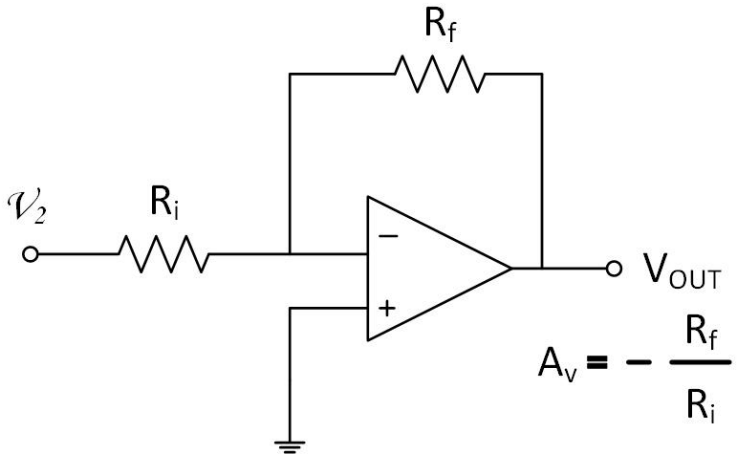


Figure 2.5: Inverting amplifier

2.4.2 Operational Amplifiers Topology

Operational amplifiers as mentioned earlier in Section 2.4.1, works by amplifying a small current into a stronger output. This can be performed by a single stage or more than 1

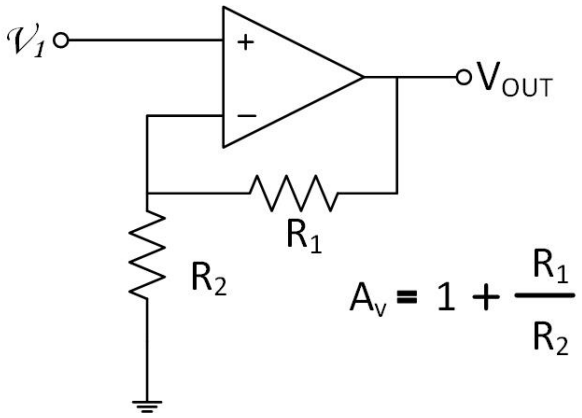


Figure 2.6: Non-inverting amplifier

stage, such as the 2-stage amplifiers. The more stages added, the more gain the amplifier able to achieve. Even though sometimes a single stage topology which commonly uses differential amplifier architecture will be able to achieve the same gain obtained by using 2-stage amplifiers, it is rather hard to minimize the noise portrayed by a single stage, as compared to the ability to optimize the noise at first stage in a 2-stage amplifier. Not only that, a 2-stage amplifier able to counter the problem of a single stage amplifier of having low voltage swing. In 2-stage amplifiers, the first stage may be optimized for lower noise, high gain whereas the second stage can be optimized for high swing voltage [74]. Based on these reasons, a 2-stage amplifier topology has been further investigated. As mentioned by Allen [75], 2-stage amplifier is one of the two major amplifier architecture that has been commonly studied. The other is folded cascode amplifier. These two topologies are frequently being modified to match the required specifications and applications. The following section described the initial design of the 2-stage operational amplifier used for investigating the research objectives.

2.4.3 Comparator Operations

Comparator is a device which produces digital binary output upon comparison between 2 analogue input levels. In particular, comparators are commonly used in ADCs. For example, comparator compares the analogue sampled input or reference voltage with the analogue output of the digital to analogue converter (DAC), produces binary signals to be used later by the successive approximation register (SAR) logic in a charge redistribution architecture. Comparator is also known as 1-bit quantizer or 1-bit ADC. Comparator can also be classified as a decision-making circuit [76].

From Figure 2.7, V_P is the input voltage applied to the positive input terminal of the comparator while V_M is the reference voltage which is a constant DC voltage applied to the negative terminal of the comparator. Ideally, when the input of voltage i.e. V_P has higher potential than the reference voltage i.e. V_M, the comparator's output is 1 while

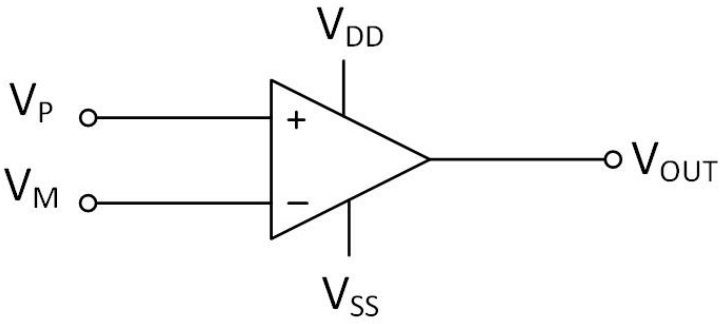


Figure 2.7: Comparator symbol

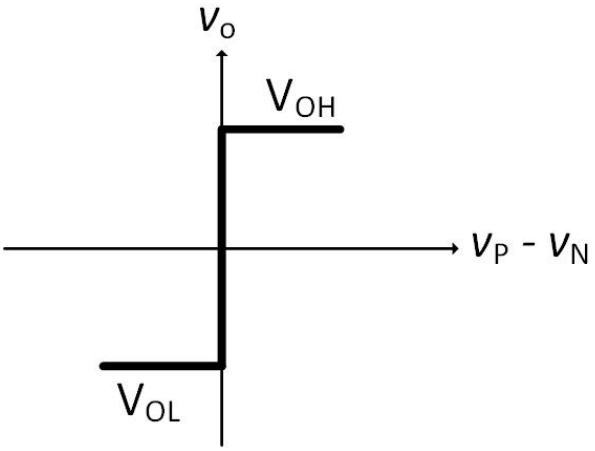


Figure 2.8: Comparator's ideal transfer characteristic

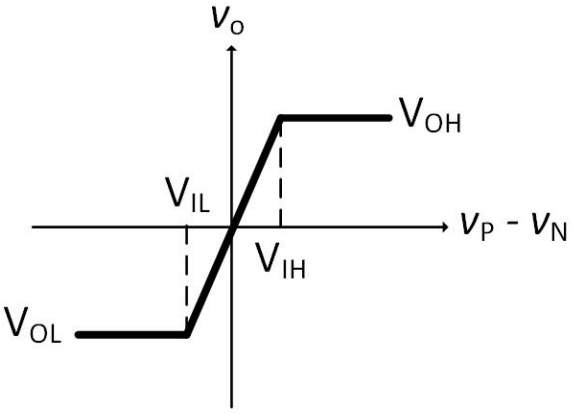


Figure 2.9: Comparator's first-order transfer characteristic

when the input voltage has lower potential than the reference voltage, the comparator's output is 0. This is illustrated as the ideal transfer characteristic in Figure 2.8. In practical application, the comparator's output becomes 1 when $V_P > V_{REF} + V_{IH}$; and it becomes 0 when $V_P < V_{REF} + V_{IH}$, as represented by the first-order transfer characteristic in Figure 2.9.

2.4.4 Comparator Topology

As operational amplifiers can be modified to act as a comparator, a 2-stage amplifier can also be used as comparators with very small modifications on the design. The major difference is at the output stage, where in amplifiers, the output stage has to be optimized for linear operation while in comparators, it needs to optimized for saturation operation [77]. Although operational amplifier can be used as comparators, it is not recommended as it has dynamic stability concerns. Other topology of comparators are pre-amplifier comparator [76], folded-cascode comparator [28, 29], inverter comparator and more innovative comparators such as dynamic comparators [60]. Further descriptions on selected pre-amplifier comparator used in this thesis have been reported in Section 3.1 and Section 3.3. In Section 3.1 and Section 3.3, the preliminary design of the two types of comparators were reported.

2.5 Characterizing Soft Errors

Single event effects (SEEs) are considered the most difficult to characterize as compared to other radiation effects in an electronic circuit. In digital circuits, well-defined measures have been well researched into as opposed to analogue circuits, which exhibits no standard methodology to quantify the radiation effects [50]. As the feature size of the aggressive technology scaling further reduces, the design and testing process at the manufacturing sites have become more complicated, time-consuming and required large resources. Even so, physical experiments are still the best choice in testing radiation features for safety-critical applications such as for space electronics or nuclear power plants. Then again, since computers are considered as the cheaper option as compared to the resources required say for example accelerator testing; device-level and SPICE circuit-level modelling can be used to overcome the limitations especially for ground-level safety-critical applications. The compendium and radiation testing on COTS and non-COTS may be able to provide some basis for the injected current in terms of its amplitude and duration to be mapped to the circuit-level model used throughout the thesis, provided the experimentations have been performed in very similar settings. It is very important to find out the most closest-fitting test data available to be mapped to the circuit-level SET model in the SET characterization study on the circuits of concern. However, in most cases, the test data are only reported and provided to the buyers or users of the component and not publicly available. Moreover, the collective compendium which reports the radiation test cannot be simply used by devices with different architecture or technology or run in a different environment. As Perez et al. [78] has said, as the testing are run under certain specifications, similar testing which have been repeated to closely follow the publicly available setup may not produce the

same transient pulse to match the same specifications used by the manufacturer. The following sections further describes the several techniques of SET characterizations.

2.5.1 Characterizations at Physical-level

The most accurate approach to simulate the generation of single event transient in a circuit or a device is to physically direct a radiation pulse initiated by heavy ions, proton, neutron or laser to the device. Accelerated testing of broad beams of heavy ions or protons or focused ion beams and pulsed laser testing are some of the methods used to characterize SETs [19]. There are three types of acceleration testing that are normally used, which are broad-beam of heavy ions, broad beam of protons and focused ion beam [19]. Broad-beam heavy ion testing has not been able to produce spatial information on the physical origins of the induced transients, thus focused ion beam has been proposed to encounter such limitation. Pulsed laser testing has its own benefits as it may be used together with circuit-level modelling to reduce the amount of ion-beam testing for semiconductor devices [79]. Buchner et al. [79] in their work found that every type of SET observed at broad-beam heavy ion acceleration testing matches the ones reproduced by pulsed laser excitation. Although pulsed laser testing has small penetration depth and some metal covers some of the sensitive areas, it is not considered a limitation for such testing. Moreover, the pulsed laser can be used to monitor whether SETs will propagate through the circuits connected to the device's output. The very important reason why pulsed laser testing is more reliable for SET characterization for analogue circuits is that the testing mechanism can be controlled. It has control over its charge injection location. By being able to control and direct the ion beam to a certain focused area; the location of SETs and its pulse amplitude and shapes can be observed [19]. Thus, test data collected from pulsed laser testing are believed to be able to provide better information in mapping SPICE-level model if required, as compared to ion-beam testing test data.

These methods have been proven useful in studying SETs as to being able to provide comprehensive information which is not being able to be provided from other single technique alone [19], however in order to use these method, one needs access to an accelerator device for example, as being used by [19], or laser testing facility, as being used by [80], all of which are located in United States of America. As of facilities closer to home, the Science and Technology Facilities Council (STFC) [81], will be able to provide the access to accelerators which belongs to the European Organization for Nuclear Research also known as CERN, located at the French-Swiss border near Geneva. As for laser facilities, STFC provides the Vulcan, Astra and Gemini high power laser, also located in RAL [82]. These facilities are free to use for academic and industry researchers, provided experimental results are published in public domain.

With the availability of instruments particularly for laser testing closer to home; the irradiation of laser or heavy-ion beams can be easily be regenerated on any selected device or circuit from already available component-over-the-shelf (COTS), provided all possible conditions or environment an irradiation would occur are made known. However, as most components available are built on bipolar technology as for example for [83], these devices cannot be used for characterization study. It may only possible to use the already available radiation data for certain analogue circuit from these facilities, which may not be helpful in studying some of the influencing factors.

One of the available devices built based on CMOS devices for comparators are by Analog Devices [84], but with no access to the detailed circuitry of the comparator, it may not be helpful in understanding the characterization process of the irradiated comparator. In order to select the best device for the characterization process, filtering process needs to take place from the list of the devices built using CMOS technology to have no additional elements such as diodes like the comparator by [85] that includes diodes in the comparator topology. This is to simplify the characterization study. With no access on detailed circuitry of comparators with adjustable hysteresis and to further aid the study of factors such as variability of transistor's width and length, a 3-stage pre-amplifier comparator with hysteresis disabled and a comparator-with-hysteresis at larger bandwidth, with an option to disable hysteresis mechanism has to be designed based on [76].The selection of a 3-stage pre-amplifier comparator has been based on the completed work by Askari et al. [25]. Askari et al. [25] has implemented the pre-amplifier 3-stage comparator in their experimentations for testing the mitigation methods proposed in their paper.

Hysteresis [59] and scaling [86, 87, 88, 89] are identified as the influencing factors in designing these comparators and VLSI circuits in general. Not only that, another reason as to why designing the comparator-with-hysteresis at circuit level is required, is as to the best knowledge, most COTS comparator designed are without built-in hysteresis mechanism. In order to include hysteresis in already existing devices, additional elements comprising of resistors in a certain configuration shall be added to the comparator.

In order to further understand the correlation between design factors and hysteresis, it is understood that the internal circuitry of a comparator in actual device shall be made accessible, where in most cases it is not. Even if it does, the actual circuit schematic used is usually not easily distributed to the public. In comparator with external hysteresis implemented; even though the hysteresis can be controlled, the internal configuration and its design variables are out of reach. The same thing applies even for a comparator with hysteresis included as for the comparators designed by Microchip [90]. In [90], the hysteresis level can not be modified which makes matters worse. Comparators with programmable or adjustable hysteresis such as from Linear Technology [91] however has no circuits included for reference. The only few COTS found with comparator topology used are for example by [85] and [92]. With these limitations, a computer simulation

modelling the comparators and its irradiation is assumed to be sufficient to characterize the susceptibility of the circuit towards SETs and on studying the synergy between influencing factors and SET sensitivity, especially for ground-level applications. This is fully supported by work by Franco et al. [93]. [93] has validated the use of SPICE micro-models in modelling single event transient phenomenon in bipolar analogue integrated circuits. The proposed micro-models have been compared with data obtained from physical experiments and demonstrated a comparable and realistic findings similar to physical modelling of single event transient impact on analogue circuits.

Although the physical experimental setup i.e accelerator device for heavy ion beam or laser testing facility can be easily accessed, the lack of information on COTS comparator with programmable or adjustable hysteresis has led this work to proceed with the design of comparator-with-hysteresis at only circuit-level and model and characterize the SET pulse using SPICE circuit level. The closer the SET modelling to the device abstraction level is, the more accurate the SET characteristics are; however, modelling SET at device level using 3D-TCAD models will require a large resource and also requires an actual 3D physics code which not easily obtained.

2.5.2 Characterizations at Device-level

The next accurate approach to simulate the generation of SETs is to model the irradiation using device modelling by computer simulations. As illustrated by Munteanu [94], the simulation methods that can be used to characterize SETs are mixed mode simulation; a numerical simulation with several discontinuous domains connected using mixed mode approach and full 3D numerical simulation with one continuous domain. In their argument, mixed mode simulation is suggested to overcome the limitation of circuit level simulation by using a physical-based device to estimate the SETs induced from an irradiated device. In mixed mode, only the device being struck is modelled at device-level while other parts are simulated at compact or SPICE model [95, 96]. Although this approach is better than a circuit-level model, it requires repetitions of device modelling for each nodes being struck, thus requires larger memory than a circuit-level simulation does. The CPU time required for a complete simulation has also increased as compared to circuit-level method [94]. A full 3D numerical simulation is the most accurate device modelling and only made possible recently. The 3D model is simulated using a 3D device physics code together with a layout geometry of the transistor or other circuit components obtained from the circuit photomicrograph and its cross section and doping densities. The physics model can be constructed from process parameters and layout file obtained from the manufacturers, although this may not be highly possible [95]. The assumption in this work is that such information will not be available. Even if the files are made available, such 3D modelling approach, however advanced, and faster

it has been due to the existence of parallel computing has not still overcome the processing time taken by circuit-level approaches, up until recent times [97]. Even then, circuit-level simulation has been the tool of choice to explore trade-offs in any specific analysis, without having the access to manufacturing test data. Circuit-level simulation can be the first-stage analysis or preliminary stage to filter out the most obvious or to identify the most sensitive or the least sensitive nodes when there is no physical data available.

2.5.3 Characterizations at Circuit-level

A circuit-level analogue circuit design with SETs being modelled at circuit-level has been deemed appropriate in the study of characterization of CMOS devices. Although SPICE or circuit-level modelling of SETs has limitations, it remains adequate for many purposes [94]. Before arriving with an appropriate circuit-level modelling, there are several terms which needs to be introduced, namely linear energy transfer, LET; critical charge, Q_{crit} and the charge collection efficiency, Q_s.

LET is defined as the energy transferred per unit length by a moving high-energy charge such as an electron or a proton, to atoms and molecules along its path [94]. When a particle has struck a particular node in a device, the track length the particle has travelled and energy loss it suffered is related to linear energy transfer. The same energy loss produced from the interaction between the particles and the silicon crystals is also quantified as the stopping power. With the assumption that all the energy absorbed is used to produce the electron-hole pair, the stopping power is comparable with the linear energy transfer (LET) [2]. Different particles exhibit different stopping power and this will quantify the varying number of electron-hole pairs in a silicon chip. The generated charge from the number of electron-hole pairs produced can only be verified to cause a malfunction or bit flip by considering two other factors, which are the charge collection efficiency, Q_s and the critical charge, Q_{crit}. Both critical charge and charge collection efficiency depend on technology as the values decrease with the reduction of the feature size of the technology [2]. On top of that, the minimum number of electron-hole pairs required for initiation of transient faults may also be described based on critical charge. By exceeding the energy produced from the electron-hole pairs, the particle strike may flip a bit in digital circuits or cause performance decrease in analogue circuits.

How good a charge being able to be collected and produces a minimal operating current in a device is a measure of its charge collection efficiency, Q_s commonly measured by a detector. A good radiation detector has an excellent charge collection efficiency. Under irradiation, the efficiency of a device to be able to collect or trap these charges reduces. With increased radiation dose, the charge collection degrades [98]. When the pairs of electrons and holes did not pass through or drift completely to the contact, this is where charge collection deficiency kicks in [99]. With these imperfections, the charge collection

efficiency is not constant throughout the device. Charge collection efficiency of a detector is the measure of actual charge collected by the detector's electrodes under specific bias to the charge; which should match with the charge that have been collected when all carrier trapping and recombinations being omitted [100]. Charge collection efficiency can be expressed as the ratio between the actual charge collected to the charge when all trapping recombinations omitted. So, when a radiation detector detects 100% of charge collection, it means it exhibits complete charge collection as opposed to, for example, 80% when additional factors impacted the charge collection process. Having only 80% charge collection will impact the critical charge of a device, by reducing the minimum value required for a radiation to cause an upset in a circuit.

Meanwhile, critical charge, Q_{crit} is defined as the minimal charge exhibited at the point when a device suffers from radiation effects or exhibits transient faults at the output. In industry or the space-electronics community, the critical charge is measured via physical characterization of a selected device. It is almost impossible to accurately model the critical charge using SPICE model without access to the physical or device characterization. Even so, a mathematical model describing the critical charge is required in understanding the physics behind single event effects.

Several models have been proposed in characterizing critical charge,Q_{crit} and one of the model was proposed by [101]; which is a simplified mathematical model based on the 3D device simulations performed in 0.35 μm technology. The mathematical model has been obtained by comparing whether the current pulse resembling the actual radiation induced in modelling the single event transient produces a charge equivalent to Q_N; the charge that corresponds to the lower limit of the integrated current produced at sensitive nodes. The charge Q_N is quantified as the product of equivalent struck node capacitance, C_N and the power supply voltage, VDD. From the 3D-device simulation, Q_{crit} can be expressed as (2.2), as follows

$$Q_{crit} = C_N \cdot VDD + I_{DP} \cdot T_F \tag{2.2}$$

where C_N is the node capacitance, VDD is the voltage supply, I_{DP} is the maximum drain conduction current of the PMOS (with assumption that the strike is made at an OFF NMOS drain) and T_F is the flipping time of the cell. The flipping time, T_F is calculated based on 3D device simulation where the transient voltage of opposite node which is not struck by the particles initiated by the current source has been monitored at the time of cell flipping. To model the critical charge by SPICE circuit-level simulation, the additive term, $I_{DP}.T_F$ is neglected resulting in a slight under estimation of the critical charge, Q_{crit}. Thus, by ignoring the additive term, there is no requirement to calculate the flipping time, T_F. The critical charge, Q_{crit} can now be approximated by (2.3),

$$Q_{crit} = I_O \cdot \exp(-\tau) \tag{2.3}$$

where (I_0) is the magnitude of the strike current and τ is the duration of strike. (2.3) is however only valid for a strike duration of less than 20 ps for 0.35μ technology. With a possible longer duration strike current, (2.3) may no longer be valid. Not only that, [101] only considered peak currents and this is not realistic for a time-varying restoring current [37].

Freeman [102] in his work proposed another critical charge model meant for bipolar memory devices and alternatively presented as (2.4) to model the current pulse induced into the device's node [103]. Q_{crit} is the threshold value of Q_{tot} for the point of soft error occurrence and τ is the pulse width of the current. Q_{tot} in this model is the total amount of collected charge [104]. This particular model has also been used for critical charge estimations for CMOS SRAM cells as in [101].

$$I_t = (\frac{2}{\sqrt{\pi}}) \cdot (\frac{Q}{\tau}) \cdot (\sqrt{\frac{t}{\tau}}) \cdot exp(\frac{-t}{\tau}) \tag{2.4}$$

Rossi et al. [30] and Cazeaux et al. [105] in their work have suggested a similar linear model to estimate the minimum charge required to generate SET, with a term also known as the critical charge, Q_{SET} and Q_{crit}, respectively. The critical charges modelled by both [30] and [105] are expressed as linear functions of the transistor sizes of the driving and fan-out symmetrical gates. In [30], the model has two different representation for high and low logic gate values, while for [105], it seems the model does not consider the conditions for different logic levels. Rossi's [30] critical charge model has also been extended into usage for non-symmetrical gates while Cazeaux's model can also be used for complex circuits similar with Rossi's. However, as both these models have only been verified on combinational circuits, these model may not be applicable for analogue or mixed signal circuits.

Similar to [101, 106, 107] which produced models based on SRAM cells, Jahinuzzaman [108] has proposed another critical charge model and claims that this model is better than the ones proposed by [101, 106] in terms of being more accurate and realistic. At the same time, the model of [108] uses an exponential current pulse as the particle inducing current generator as it is believed an exponential current pulse produces a better representation of the physical characterization of radiation effects as opposed to the rectangular current pulse used by [107]. By using a rectangular current pulse, the model suggested by [107] has maximum 11% discrepancy. Thus, as [37] suggested, the most agreed SPICE model and commonly used i.e. double exponential model is still believed to closely represent radiation effects although it will never be able to match the powerful modelling of transient effects using device modelling unless further improved

to reflect the 3D dynamic representation of the device. By using double exponential model of $\tau_r = 1ps$ and $\tau_f = 50ps$ as inducing current generator, the discrepancy reduces to less than 5% [108]. With the recent development [109, 93, 110] of circuit-level SET model particularly for double exponential model, there are however hope in improving the model to be used extensively in analysis of SET.

2.5.3.1 Modelling critical charge using double exponential model

The double exponential model has been first introduced by [111] to closely approximate the response from the characterization of charge collected at the junction nodes of integrated circuits from the ionization track occurred due to radiation. The response obtained from the characterization resembles an exponential model as depicted in (2.5), and later given a different representation by [109] as (2.6) to aid in determination of realistic parameters. I_0 is approximately the maximum current or transient current pulse while $1/\alpha$ is the collection time constant of the junction and $1/\beta$ is the time constant for initially establishing ionization track. In (2.6) on the other hand, Q_p is the total charge collected (C) while t is the time (ns), τ_r is the rising time of the injection current and τ_f as the falling time.

$$I(t) = I_0(e^{-\alpha t} - e^{-\beta t}) \tag{2.5}$$

$$I(t) = \frac{Q_p}{\tau_f - \tau_r}(e^{-t/\tau_f} - e^{-t/\tau_r}) \tag{2.6}$$

One can denote the total charge, Q_p from $I(t)$ by solving (2.6) using simple integration to obtain (2.7).

$$Q_p(t) = \int_0^\infty I_p(t)dt = I_0(\tau_f - \tau_r) \tag{2.7}$$

Kobayashi in their work, [112] has raised again that using double exponential model may generate inaccurate SET current pulses due to the voltage dependency of the transient currents has not been properly implemented. Veeravalli et al. in a workshop, [113] has stressed the need to perform in-depth research for the already available SET current injection models, particularly double exponential models due to its limitations to exactly represent the actual current injection caused by radiation particles. As claimed by [109] in 2014, although the double exponential model has been widely used to model the current injection; by far none has produced any characterization analysis which compares the double exponential model with the physical model. Their previous work [114] in 2013 has started an investigation on the comparison characterization process

by modelling the SET using both diffusion model and double exponential model. From [114], it has been revealed that the current shape has little influence to the cross-section and the SER. The validation process has been based on a simulation of a 90 nm drain electrode, using a detailed diffusion model and by using Monte-Carlo technique. Even so, the rise and fall time and the collected charge for the double exponential model are only known approximately thus the analysis only makes sure the double exponential waveform shape is as realistic as possible. As a conclusion, the validation experiment performed suggested that the double exponential current shape is acceptable in modelling the injected radiation current and there is a correlation between the parameters of double exponential and diffusion models obtained from TCAD analysis.

Prior to reaching the conclusion of there is a correlation between double exponential and diffusion model, a simulation to investigate the transient current by using diffusion model has been completed [109]. From diffusion modelling, the required parameter is the final current pulse as a function of time. This is obtained from the numerical division of ion track into smaller fragments by the diffusion model. These small fragments then spherically diffuse their charges. The drain electrode collected a portion of the electrical charges which have been diffused by smaller fragments earlier. From these integrations of collected charge along the ion track and over the drain surface provides the final pulse as a function of the time required, also termed as transient current as shown as an example of plotted diffusion transient current in Figure 2.10.

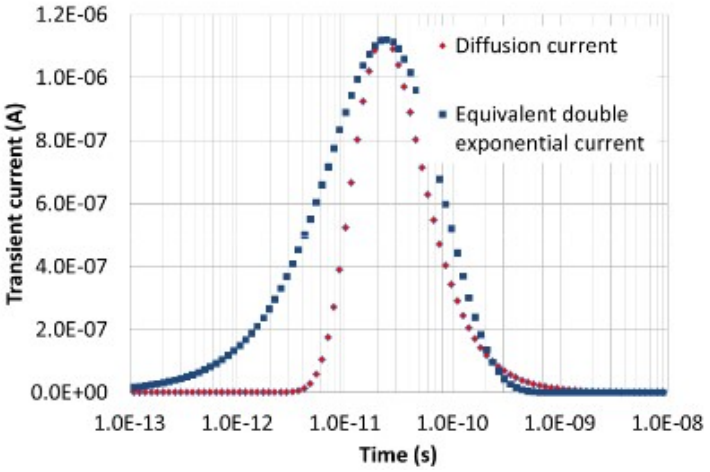


Figure 2.10: Diffusion transient current plotted in log-log scale with the corresponding double exponential representation, taken from Wrobel [109]

For each of the current pulse, information such as total collected charge, Q_p, the maximum current, I_{max}, and time lapse needed to reach the current peak, T_{max} have been extracted; which later used to map the double exponential model into a simplified model of diffusion model; as illustrated in the same Figure 2.10. Thus, generating the double exponential model as the simplified diffusion model allow both models being able to be consistently compared with each other.

By vanishing the derivatives of the double exponential model,(2.8) is obtained to relate the maximum current, I_{max} and the rising time, τ_r and falling time, τ_f;

$$T_{max} = \frac{\ln(\frac{\tau_r}{\tau_f})}{\frac{1}{\tau_f} - \frac{1}{\tau_r}} \tag{2.8}$$

In order to solve for rising time, τ_r and falling time, τ_f; another relationship is obtained as (2.9) with $t = T_{max}$.

$$I_{max} = \frac{Q_p}{\tau_f - \tau_r}(e^{-\frac{T_{max}}{\tau_f}} - e^{-\frac{T_{max}}{\tau_r}}) \tag{2.9}$$

By numerical methods, (2.8) and (2.9) are solved for rising time, τ_r and falling time, τ_f; thus these values can be used in modelling the SET based on double exponential waveform. On the other hand, total collected charge, Q_p, can be obtained using (2.7).

2.5.3.2 Modelling critical charge using simplified double exponential model

As described earlier in Section 2.5.3.1, the parameters for double exponential model are not easily obtained. Thus, [109] has investigated on the possibility of further simplifying the double exponential model as first introduced as (2.5) into a relationship which only depends on at most 2 parameters.

The total collected charge, Q_p, is an important parameter thus, shall be kept. The two parameters left to be evaluated are rising time, τ_r and falling time, τ_f. The tabulation of rising time versus falling time has been plotted in order to find an approximated relationship between the two. A linear fitting curve relating the rising time and falling time indicates an approximation of falling time being 5 times of the rising time. From this approximation, (2.6) can be rewritten as (2.10).

$$I_0 = \frac{5Q_p}{4\tau_f}(e^{-\frac{t}{\tau_f}} - e^{-\frac{5t}{\tau_f}}) \tag{2.10}$$

2.5.3.3 Modelling critical charge using dual-double exponential model

The most recent improved SET model; dual-double exponential current model [110] has been proposed to encounter some of the limitations exhibited by double exponential model. As claimed by Black et al. [110], when SET pulse is modelled with a single double exponential current source, the voltage transient resulted from simulation will overdrive the circuit at a significant rate or have a very slow leading edge; dependent on selected parameters. By over-driving the circuit, this will over predict the amount of

charge needed to have a longer SET width. Thus, the circuit now has been portrayed to have better resilient to transient effects. The over estimation may also affect the SER estimations. The dual-double exponential model proposed is based on the device characterization taken from [115]. In this device-level simulation results of Figure 2.11, it has been observed that there is both short and high current peaks, which may be modelled by two exponential components combined in parallel; as illustrated by Figure 2.12. The combination of dual-double exponential source is noted to be applicable only for devices with the current profiles projected as in Figure 2.11.

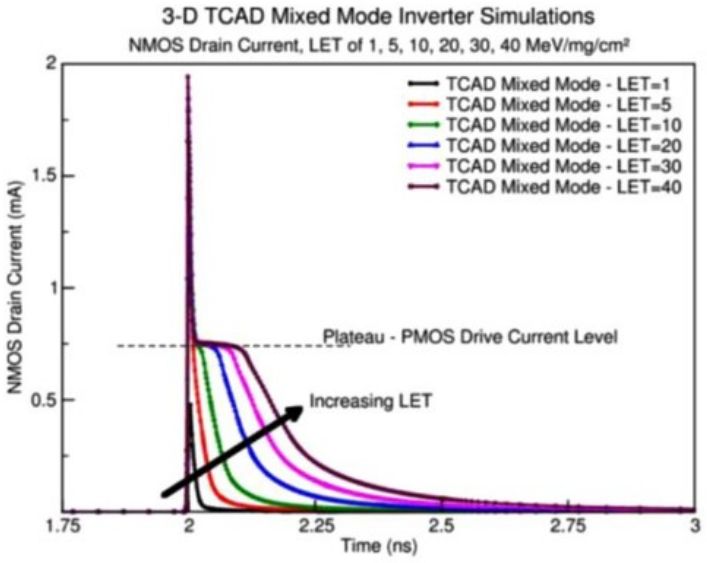


Figure 2.11: NMOS TCAD simulation results portraying both short and high current peaks (after DasGupta:2007 [110])

The short duration current source as in Figure 2.12 is represented by $I_{prompt}(t)$ while long duration or sustained-duration current source is represented by $I_{hold}(t)$. There are a total of 4 parameters that needs to be determined for each current source; which are I_{Peak}, $(t_{d2} - t_{d1})$, τ_1 and τ_2. Three of the parameters for the short duration current source, which are all the time parameters; $(t_{d2} - t_{d1})_p$, τ_{1p} and τ_{2p} are acquired from the results of TCAD simulations while for the long duration current source, two of the time parameter values; τ_{1h} and τ_{2h} can be postulated from a 90-nm modelling. The other time parameter, $(t_{d2} - t_{d1})_h$ is used as a variable which depends on deposited charge.

Peak currents, I_{Peak-p} and I_{Peak-h} respectively for short and long duration current sources are determined with transistor-level simulations using SPICE. The total sum of peak current, I_{Peak-t} is obtained from the summation of I_{Peak-p} and I_{Peak-h} by running a SPICE simulation using a short duration, double exponential current source. The time parameters used to model the double exponential model here has not been mentioned on how it has been determined. The time parameters have been set to certain values which have not been justified in the paper.

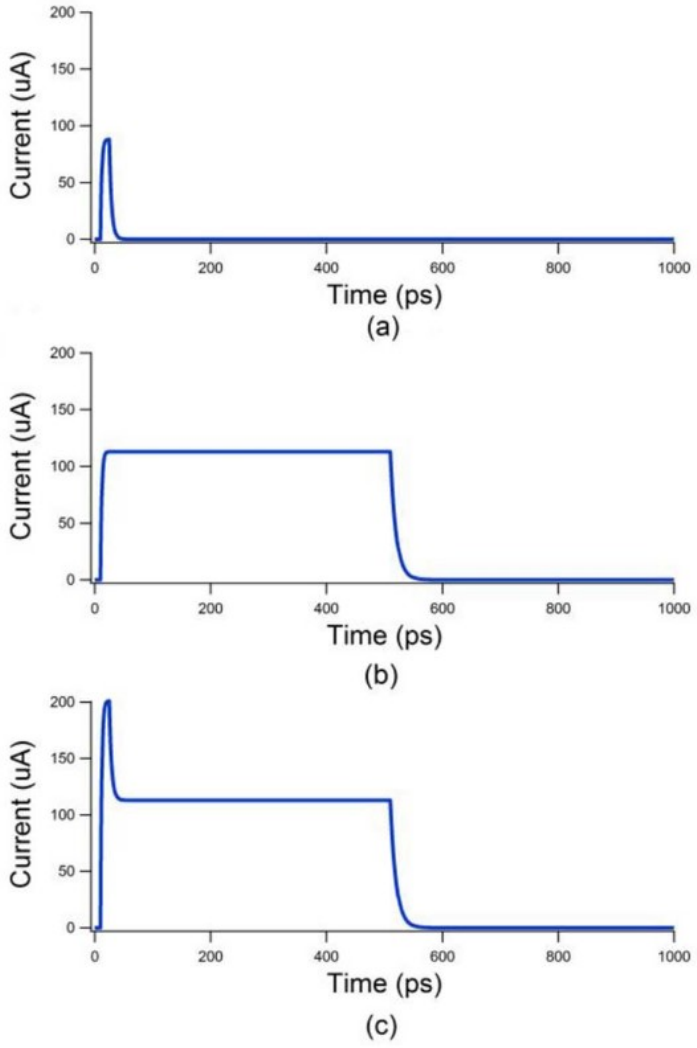


Figure 2.12: Combination of (a) short double exponential current source and (b) long double exponential current source producing (c) a dual double exponential current source, after Black [110]

On the other hand, peak current for long duration current source, I_{Peak-h}, is determined by using dual-double exponential current source and now, $I_{Peak-p} = I_{Peak-t} - I_{Peak-h}$. The short duration current source,$I_{prompt}(t)$, is then again set with values acquired from the timing parameters of a particular CMOS technology. For the long duration current source,$I_{hold}(t)$, two of the time parameter values;τ_{1h} and τ_{2h} are based on the timing parameters from a 90-nm modelling. $(t_{d2} - t_{d1})_h$ is determined from the amount of deposited charge.

Once both short duration current source,$I_{prompt}(t)$ and long duration current source are known,$I_{hold}(t)$; it is time to calculate the total charge of the injected current. This is defined as the sum of the charge from $I_{prompt}(t)$ and $I_{hold}(t)$, as represented by (2.11).

$$Q_{Total} = Q_{Prompt} + Q_{Hold} \tag{2.11}$$

In order to calculate these charges, (2.12) is applied to (2.13) by using $(t_{d2} - t_{d1})$ as a variable which depends on the deposited charge.

$$Q_{Total} = I_{Peak}[\tau_1 + \tau_2 + (t_{d2} - t_{d1}) - \tau_1 e^{-\frac{t_{d2}-t_{d1}}{\tau_1}}] \tag{2.12}$$

$$Q_{Hold} = Q_{Total} + Q_{Prompt} \tag{2.13}$$

Both Q_{Prompt} and Q_{Hold} are calculated by using (2.12), however for calculation of Q_{Prompt}; the last term inside the bracket of (2.12) is omitted. Lastly, by solving (2.12) used for calculating Q_{Hold}; the final time parameter unknown, $(t_{d2} - t_{d1})$ is obtained.

2.5.3.4 Limitations in modelling critical charge at circuit-level

Work which describes the development of these current injection model as in Section 2.5.3.1, Section 2.5.3.2 and Section 2.5.3.3 are typically used to quantify soft errors. Even though it has been constantly repeated that it is very important to use 3D device simulator to produce the physical data to be used to model heavy ion strikes as the stimuli characteristics are technology dependent; [116] thought otherwise. In particular, injection current models which exhibit fast timing characteristic may provide a good approximation in soft error rate (SER) estimations; especially when 3D simulation data is not accessible although underestimations will always be the case [116]. This underestimation has been identified to be partly contributed by purposely ignored factor in the simplified current injection model as (2.2) proposed by Roche [101], as previously explained. For this reason, this thesis's objectives have been completed using the circuit-level characterization method.

2.5.4 Soft Error Rate, SER

Soft error rate (SER) is the rate of how often a soft error occurs, normally expressed in terms of Failures in Time (FIT), calculated as the number of failures per 10^9 hours of operation [94]. FIT/Mbit or FIT/chip are two of the terms normally used to quantify the SER. FIT/Mbit in this context refers to quantification unit of SER for memory devices while FIT/chip applies generally for all device's SER measurements [94]. For example, in safety-critical applications, the SER may need to be as low as 1 FIT/Mbit or less. (2.14) is the relationship used to quantify SER FIT rate, with $\chi^2(1 - C.L, 2r + 2)/2$ as the one-sided chi-square function, r as number of failures, $1 - C.L$ as hazard ratio also identified as ϵ, $2r + 2$ as the degree of freedom, $C.L.$ as the confidence level, n as total number of devices and h as the operation hours [117]. χ^2 values can be obtained from Table 3.1 of [117]. Typically a confidence level of 60% is required for commercial

devices and 90% for safety-critical applications such as military, space, avionics, nuclear power plant systems and large-scale computer systems. (2.14) is aimed to quantify SER provided the number of failures and its operation hours has been made known.

$$FIT = \frac{\chi^2(1 - C.L, 2r + 2) \times r \times 10^9}{2 \times n \times h} \tag{2.14}$$

It is necessary to note that SER is defined as the number of upsets rather than the number of errors or fault [117]. It is also necessary to note that the faults are essential to produce errors but a fault existence would not necessarily produce an error [2]. When a fault is masked or tolerated, an error does not exist at the output. An error will be identified as a failure depending where it strikes or occurs and the functionality of the system [117].

(2.15) is the estimation of SER calculated with consideration of both critical charge and charge collection efficiency, where K is the scaling factor, F is the neutron or alpha flux in particles ($cm^{-2} \times s^{-1}$) and A is the circuit area that is sensitive to the particle strikes [2].

$$SER = K \times A \times F \times exp - \frac{Q_{crit}}{Q_s} \tag{2.15}$$

Although this thesis will not quantify the soft error rate of analogue circuit studied, the definition of soft error rate (SER) as (2.15), is given here to stress the importance of critical charge and charge collection efficiency in estimations of SER at chip-level. SER can also be quantified at other abstraction level such as at system-level, as previously described by (2.14). Besides, SER is usually quantified by governing the total error experienced by a particular device and not only focusing on transient effects, thus quantifying error rate exhibited by analogue circuits in a system is trivial.

2.6 Factors influencing Single Event Transients

A device's response towards radiation particle strike is deemed complex and influenced by several factors; which includes the device's parameters such as polarity [95], geometry (scaling/supply voltage) [87, 118], location (parasitics) [119], the particle's criterion such as doping or ionization dose (total ionizing dose) [120, 121], carrier lifetimes [95], the energy and LET of the radiation particle [95], environmental factors such as temperature [122, 123, 124] and altitude (closer to gravitational radiation), the circuit's parameters such as biasing conditions [125] and differential input voltage [49], application (speed) and topology (hysteresis, feedback, symmetry), load resistors [126, 127], feedback resistors [26], and may also be influenced by other faults caused by radiation such as the

temporal faults i.e. NBTI (negative-biased temperature instability) [128, 129] or spatial faults i.e. RDF (relative dose factor) [130].

Some of these factors are able to be simulated at circuit-level such as scaling, supply voltage, temperature, biasing conditions, feedback and NBTI while others such as parasitics, polarity, doping or total ionization dose, carrier lifetimes, energy and LET of the particles and RDF need to be addressed at physical-level or device-level modelling. In this thesis, focus has been given on factors which can be simulated or modelled at circuit-level.

While major studies are made on digital circuits, on the various factors which affected the single event transient (SET) characteristics [89, 122]; just to name a few, a limited number of works has been reported on the parameters or design factors which lead to variations of SET shapes or characteristics on analogue or mixed signal circuits. It is of interest to be able to summarize the existing factors which have been reported to impact the characteristics of SETs, and to investigate whether some of these parameters have the same influence on selected analogue circuits.

2.6.1 Device-related Factors

2.6.1.1 Technology scaling

The geometry of the device itself has been proven to be a significant influence on the severity of SET for a device, as it is linked with scaling. As devices become smaller, less charges are stored at the circuit nodes, thus the energy needed to cause an upset at a certain node reduces. Because of CMOS technologies scaling, the spacing between transistors, which defines the distance between diffusion regions that stabilize the well potential, decreases almost linearly with feature size, so this effect will become more significant in future technology. In 1996, Petersen et al. summarized that the critical charge, Q_{crit} is related to the feature size (t) by (2.16), where Q_C is the critical charge expressed in pC and t in microns.

$$Q_C = 0.023t^2 \tag{2.16}$$

With technology scaling, the nodal capacitances and lower supply voltage may decrease the minimal critical charge required to induce a SET [97]. This is very obvious that as technology node has decreased aggressively, this allows for more SETs with the sufficient pulse width and amplitude to be detected and cause an upset [86]. With smaller feature size, the transistor size and voltage supply reduces by 30% [131]. Smaller feature size reduces the exposed area to radiation particles, thus increases the tendency of SET being captured due to the reduced critical charge. With increased SET width; increased

number of SET detected at its digital counterpart as sampling took place. Moreover, with the increased sampling rate or operating frequency will latch higher number of SETs.

Meanwhile, SETs have been investigated on its correlation to technology scaling for example by [86, 87, 88, 89]. Although these analyses have been performed on digital circuits, some parameters which are related to technology scaling does apply to analogue circuits. One example is the work by Benedetto et al. [86], which data concludes a significant increase in digital SETs pulse width, parallel with CMOS technology scaling. Not only that, they have concluded that a higher operating frequencies have resulted in a longer SET pulse width. In [87], it has been mentioned that [86] and [132] predicted that for each technology node advancement, the SET pulse width will increase; but there are contradictions in the published data, further supported by [89]. [87] explained this inconsistency by comparing [86], [132], [133] and [134]. Benedetto et al. [86] measured SET width up to a 2 ns in 130 nm bulk technology while [133] measured SET width of less than 500 ps for the same technology. There after, [132] measured SET widths which exceeds 1 ns while Cannon [134] measured widths of less than 400 ps in 90 nm technology. In [86, 132], the widths increases as technology is further scaled but on the other hand, in [133, 134], the widths reduces.

With these contradictions, Gadlage et al. [87] ran simulations on 65 nm technology which presents a shorter SET widths as compared to similar circuits as Narasimham's [132]. However, with further considerations on other factors, the resulting SET widths gets more complex. With several other factors which have been proven to influence the SET width, it can no longer be assumed that technology scaling is the only sole contributor in variations of SET widths. With the debate in the digital world, similar investigations on impact of scaling on analogue and mixed signal circuits are required. A part of this thesis, [135] has reported earlier on the investigation of the impact of channel length and width variations on the SET characteristics based on [136] by measuring the recovery time, which is the time taken for the comparator to return to its normal operation.

As to date and to the best of knowledge, there are no significant work that has been reported on the study of the impact of technology scaling towards SET sensitivity of analogue circuits, particularly for operational amplifiers and comparators. This may be due to the fact that variability in analogue circuits are normal due to the design trade-offs and design flexibility exhibited. However, in analogue circuits which is connected to digital counterparts; the impact of technology scaling on SETs shall be addressed and investigated as the error propagated may impact the overall system if undetected.

2.6.1.2 Parasitics

As the feature size of CMOS technology further decreases, the device becomes induced to parasitics; as the gap between the structures are reduced. Parasitics have been found to affect the severity of SET in an analogue device [137, 119]. Sternberg et al. [119], has measured two different COTS comparators; LM119, LM111 and an op-amp, LM124 in studying the influence of the parasitic elements to SETs. All three components have been built based on bipolar technology. Results for LM119 appear insignificant that it needs to properly modelled before a reliable result obtained from the analysis. Meanwhile, in LM111; the modelling of base resistance has significant impact on the SETs. The parasitic element i.e biasing resistor in LM124 has been identified as the most sensitive element towards SETs, however nothing has been reported on how these parasitics impacted the op-amp.

As critical charge estimation is inter-related to SET modelling, the impact of parasitics on the critical charge, Q_{crit} has been looked into by [103]. Heijmen et al. [103] reported that by including the back-end parasitic capacitances in critical charge simulation will affect the estimation of critical charge, Q_{crit} of the SRAM cell studied. In the particular SRAM cell design, characterization of SET under parasitics increases the critical charge, Q_{crit} for about 1 fC. By increasing the critical charge, it is believed that a device will be less sensitive to particle strikes which were applied before when the critical charge is smaller.

2.6.2 Environmental Factor

2.6.2.1 Temperature

It has been revealed in [138], that physical testing performed on p-n structures under increased temperature causes a decrease in SET amplitude but causes an increment to the pulse width. From this findings, several characterization of device under elevated temperature have been completed. Dakai Chen and his team, [124] has found that the SET pulse widths induced from pulsed-laser experiments increases with increasing temperature, particularly for LM124 operational amplifier. In addition to this, increasing SET pulse amplitude has been observed with escalation of temperature for almost all of the transistors for LM139 voltage comparator, except for one.

2.6.3 Device's Parameter and Topology Factor

2.6.3.1 Biasing conditions

Koga et al. [125], concluded in their work, that certain types of linear microcircuits are strongly affected by their biasing conditions. In their investigations on a LM111 voltage comparator, the SETs depended on the input voltage difference, ΔV ; where the smaller the ΔV is, the higher the SET sensitivity is. Such observation is only applicable for circuits where the biasing conditions are directly affected by the voltage levels at the positive and negative inputs of the device. A similar conclusion with Koga et al. has been reported by [19], where the characteristics of SETs induced in comparators also depends on the operating conditions, in particular the differential input voltage. Again, if the differential input voltage is sufficiently large, the overall SET sensitivity of the comparator can be effectively reduced. Another study performed by Johnston et al. [53], in earlier work than Buchner's also comes to the same conclusion, where transients in different models of high-speed comparators are strongly affected by differential input voltage, except for BiCMOS device. The various high speed bipolar comparators used in the investigations, have switching speed of below 80-ns. The very similar conclusion of dependencies on differential input voltage for different models of comparators, suggested that for any voltage comparators which has a differential stage, the strong correlation of the input voltage difference on the SET characteristic applies. In a non-dynamic comparator, a signal amplitude variation could lead to signal distortions and degradation of signal-to-noise-ratio (SNR). In a dynamic or clocked comparator, the output signal will be very sensitive to single event effects (SEEs) during active clock sampling; termed as signal transition state effect. Both signal amplitude variations and signal transition state effect are exhibited from analogue circuits suffering from soft errors i.e transient errors [16].

2.6.3.2 Positive feedback

Positive feedback or hysteresis is a mechanism which is used to reduce the noise elements from a device. Roche et.al, [59] in their work has investigated the impact of hysteresis on the SETs shapes on their selected circuit, which is a linear analogue comparator with hysteresis, also known as Schmitt Trigger. They have concluded that this kind of circuit's response to SET are sensitive to the hysteresis effects. They have observed that the SET may latch the output into a non-desired state when the input voltage falls within the hysteresis band range. As claimed by Roche et.al. [59], their work is considered the pioneer in studying how the hysteresis or the positive feedback may impact the SET shapes. Upon reviewing any more recent work on comparators with positive feedback, none has reported similar work. From their investigation, the state

of the output can be changed by the SET induced in the circuit, not only by the input voltage, but also with the different levels of the injected energy.

2.6.4 Temporal Unreliability Effects Factor

2.6.4.1 Ageing - NBTI

In addition to the increased vulnerability to SETs, the aggressive scaling of CMOS devices has also increased the vulnerability to ageing, as reported by [139, 140, 141, 142]. [139] and [140] reported the impact of ageing on digital circuits while [141, 142] focused on the impact of ageing on analogue circuits.

While SETs and NBTI have been individually investigated for their impact on CMOS devices, limited work has been done on the interaction between ageing and SETs [143]. Rossi et al., [144], reported that NBTI reduces the critical charges on the nodes of combinational and sequential circuits while Harada et al.,[128], reported that ageing has a significant impact on the effect of SETs and Bagatin et al., [140], stated that NBTI degradation does not significantly affected the single event upset sensitivity of SRAM as long as the parametric drift caused by ageing does not exceed 10%. Additionally, El Moukhtari et al., [145], has indicated a decrease in SET sensitivity under the influence of NBTI for chain of inverters and the same authors, [146], reported a fast increase of SRAM SET vulnerability under ageing.

2.7 Design of Experiments Methodology

Design of Experiments (DOE) is a statistical methodology for determining the correlation between factors which may or may not affect an operation of a system and the impact of factors on the output of a system, systematically [147]. It is usually used in industrial or manufacturing systems, as an improvement scheme in process performance or product quality [148]. DOE allows designers to find out the interaction between factors simultaneously. Not only that, an individual factor can be identified to be more significant than the other from the completion of DOE methodology. Some examples to easily understand the concept of DOE has been described in [147, 149].

DOE is an efficient tool to investigate the relationship between at least 2 input factors and its output or outcome. All selected factors may be studied by using several statistical methodologies. These statistical methodologies are used specifically in producing the design matrix and analyzing the correlation between factors and the output. The design of experiments techniques which are available ranges from factorial, response surface methodology (RSM) and mixtures of techniques. The DOE technique which is the simplest to implement is the factorial design.

Full factorial designs are used for running preliminary experiments, in deciding the significant factors, also known as screening experiment. On the other hand, response surface methodology designs are used in describing the relationship between vital factors and its responses. Full factorial designs require a higher number of experiments, as to come up with identification of significant factors while response surface methodology produces the optimum number of experiments in order to describe the relationship between these significant factors. Saleem's work [150] illustrated the concept of using factorial modelling as screening experiments and response surface methodology as optimization technique in relating important factors and its responses. In this thesis, selected factors have already been decided based on reviewed literature, thus, full factorial design has not been performed as part of screening experiments under the variability study. Full factorial designs can also be used to model the relationship between factors, however full runs of every possible experiments need to be completed while response surface methodology design models the relationship using optimized number of experiments. Thus, response surface methodology has been selected over factorial modelling in summarizing the relationship between significant factors, in this thesis. One direct comparison between response surface modelling and full factorial designs has been reported back in 1968, in the area of agricultural research by Williams and Baker [151]. In this comparative work [151], response surface methodology has been justified to being able to model the true response of relationships between factors similar to factorial designs, but at reduction of number of experiments.

A short example on using full factorial mechanism has been included in Section 2.7.1. Under RSM, there are several choices of experimental design that can be used. Only central composite design (CCD) has been reviewed in detail in Section 2.7.2 while another statistical technique such as Box-Behnken is reviewed briefly in the same section. Response surface modelling has been used in reliability analysis for one of the circuit, as reported in Chapter 4.

2.7.1 Full factorial

Full factorial designs specifically suggested running experiments for all possible combinations. This is a very efficient statistical tool. Although this technique is the easiest approach, running all possible combinations of experiment has deemed too costly.

In general, after identifying the problem statement and selecting the design variables and classifying them into categorical and continuous variables, the number of levels for each factor has to be decided based on this. The selection of levels is based on historical data and in-depth knowledge of how this system works. An example of 2-level categorical variables is gender (male, female), skin colour (dark, fair) while 2-level continuous variables are temperature (30,42) and pressure (80,100). The design variables

if represented in coded levels will have 2 possible settings, the high and low levels [149]. High is commonly coded as +1 while low can be coded as -1.

As an easy example, in a 2-level 2-factor experimental design, a simple relationship; 2^n is used to design the number of experiments required. 2 factors will yield 4 experiments, and 3 factors will yield 8 experiments and so on. Table 2.1 represented the design matrix which listed all the possible combinations of high and low for each design variables. These design variables are meant for running an evaluation test of a machining device in a manufacturing setting. In this test, there are 3 factors which are under investigation, as specified in Table 2.2.

Table 2.1: The total number of experiments from 3 factors

Run #	Factor A	Factor B	Factor C
Run 1	-1	-1	-1
Run 2	-1	-1	1
Run 3	-1	1	-1
Run 4	-1	1	1
Run 5	1	-1	-1
Run 6	1	-1	1
Run 7	1	1	-1
Run 8	1	1	1

Each high and low-level values for all factors must be decided realistically. The following matrix in Table 2.2 detailed out what factors will be investigated and the realistic high and low levels of each factor. The base of the design variable shall also be selected and included in the matrix. Once the design matrix has been realistically decided as Table 2.3, the next phase will be the assembly of the experiment setup and the testing of the experiments which have been planned and designed. The output response or performance parameter of the system which has been identified as the diameter of a drilled hole in a metal is to be observed. Table 2.4 listed the sample of the result of the evaluation test of the machining device.

Table 2.2: Factors under investigation and realistic high and low-level values

Design Variables		Low level (-1)	Base (0)	High level (+1)
Factor A	Machining Temperature (C)	120	160	200
Factor B	Machining Pressure (psi)	50	75	100
Factor C	Machining Speed (m/s)	5	15	25

Once a complete result have been obtained from the testing, the result shall be examined for correlations between the factors and the impact of the factors to the performance of the system measured at the output response. These results are best tabulated and sorted to produce a more comprehensive conclusion by the interaction effects plot. The mean response for all combinations of the factors, temperature, pressure and speed are calculated and plotted using the main effects plot. If the lines are intersecting with

Table 2.3: Possible experimental combination for evaluation testing of machining device

Run #	Factor A	Factor B	Factor C
Run 1	120	50	5
Run 2	120	50	25
Run 3	120	100	5
Run 4	120	100	25
Run 5	200	50	5
Run 6	200	50	25
Run 7	200	100	5
Run 8	200	100	25

Table 2.4: Evaluation testing based on the diameter of a drilled hole by the machining device

Run #	Temperature	Pressure	Speed	Hole's diameter (mm)
Run 1	120	50	5	101
Run 2	120	50	25	103
Run 3	120	100	5	107
Run 4	120	100	25	103
Run 5	200	50	5	111
Run 6	200	50	25	111
Run 7	200	100	5	106
Run 8	200	100	25	103

each other, this signifies that there are interactions between the lines. On the other hand, lines in parallel indicated that there is no direct interaction between the factors or between the factor and the output response.

The results from Table 2.4 have been processed by Minitab ® and three main effects plots are produced as Figure 2.13, Figure 2.14 and Figure 2.15. Both speed and pressure reduce the drilled hole's diameter for increasing speed and pressure while temperature increases the hole's diameter by increasing temperature. If the objective of the experiment is to find out which factor(s) increases the hole's diameter; then the temperature has been identified as the significant factor. Main effects plot is one of the tools to analyze the results. There are many others depending on the objective of the system.

From the example of DOE using a full factorial technique, the relationship between the main effects or design variable with the output response has been identified. From this conclusion, with the contributing variables or factors have been identified; correction or improvement on this particular factor if possible can be performed.

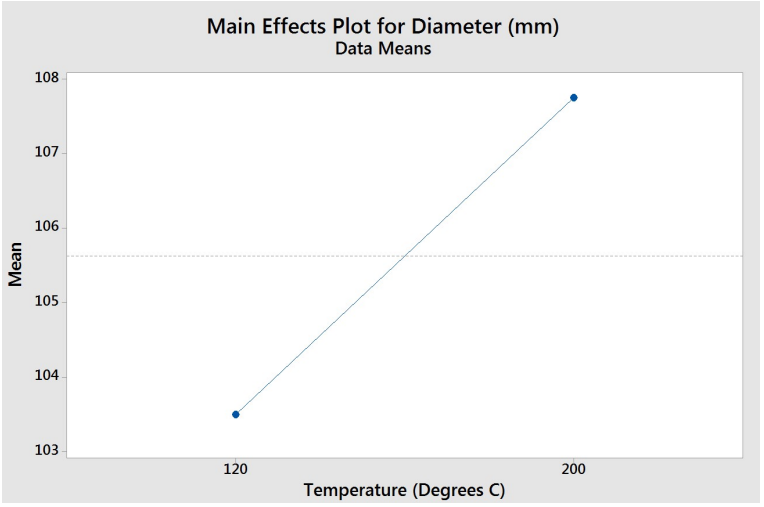


Figure 2.13: Main effects plot for temperature on the drilled hole's diameter

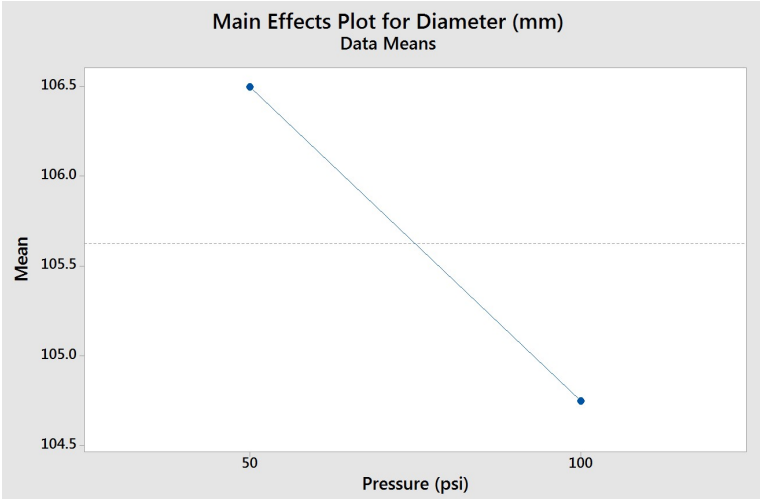


Figure 2.14: Main effects plot for pressure on the drilled hole's diameter

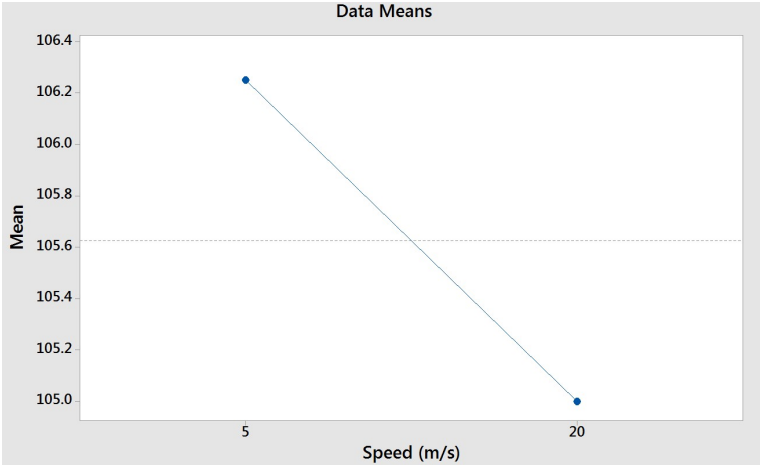


Figure 2.15: Main effects plot for speed on the drilled hole's diameter

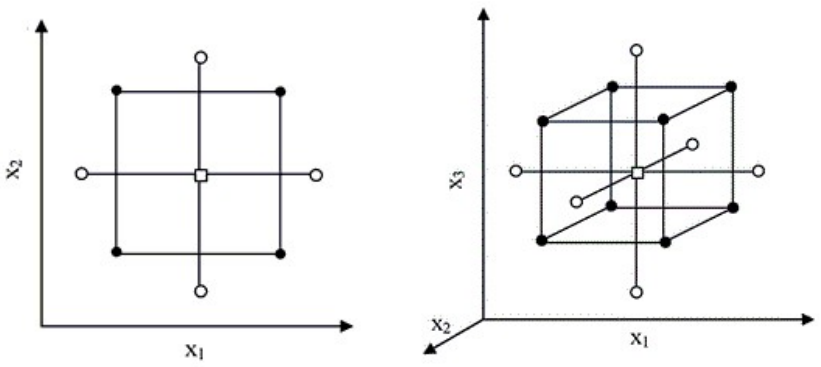
2.7.2 Response Surface Methodology

Response surface methodology (RSM) is a collection of techniques based on mathematical and statistical contexts in fitting a polynomial equation for the compiled data [152]. The equation obtained shall be able to define the relationship or behaviour of the collection of data. A linear relationship may also be fitted to the compiled data. The behaviour of the data collected is best described when the output response(s) are influenced by several input factors. Without these tools, the behaviour of these variables towards the output response can still be analyzed but using RSM or something similar reduces the complexity of experiment to be completed.

Response surface methodology has been first introduced by Box and Draper [153], to model experimental responses. Response surface methodology allows an efficient design of experiments. By saying that the complexity of the experiments can be reduced earlier, carefully designing the experiments will optimize the number of runs required to observe the system's behaviour. The design optimization will definitely reduce the expensive analysis which may be done in large scale. By optimizing the number of runs required to identify which design variables affected the output response the most and used this information to improve the designed system, the cost will be reduced and yet, the behaviour of the optimized experiments will likely still match the conclusion from a full run of the experiment. This is performed by carefully selecting the design variables which has major effects and design an appropriate experiment, as already described in Section 2.7. The screening process shall be based on researcher's prior knowledge, the objective of the analysis or based on preliminary experiments.

Once the design variables are determined, the optimum number of experiments to be carried out has to be decided by using MiniTab ®. This is the main objective of design of experiments, which is to decide the selection of points where the output response should be evaluated [153]. This stage is also known as an optimization in design of experiments. In MiniTab ®, the design variables have been inserted into a new response surface design. By creating new design, two variants of response surface models are given; either by using Central Composite or Box-Behnken. Both Central Composite and Box-Behnken exhibits the optimization of the critical factors, where these techniques will try to fit the experimental results into a model which represents the true behaviour of the investigated subject.

The Central Composite Design (CCD) is one of the most popular response-surface designs, which is also known as Box-Wilson designs. CCD is a second-order factorial designs which include the centre point and the axial points. In order to obtain the optimum number of experimental runs, $N = 2^x + 2x + n$ is used [154]. x in this relationship is the number of the design variables while n is the number of repeats exhibited by the central point. Figure 2.16(a) is an example of central composite design for 2 variables while Figure 2.16(b) for 3 design variables at 2 levels.



(a) 2 design variables at 2 levels (b) 3 design variables at 2 levels

Figure 2.16: Central composite design model [155]

Box-Behnken is a full quadratic rotatable model; which for a small number of factors (4 factors or less); require fewer runs than the central composite model does. The optimum number of experimental runs based on Box-Behnken is determined using, N = $2x(x-1)$ + C_0, where C_0 is the number of central points while x is the number of design variables [156]. Figure 2.17 is an example of Box-Behnken design for 2 variables.

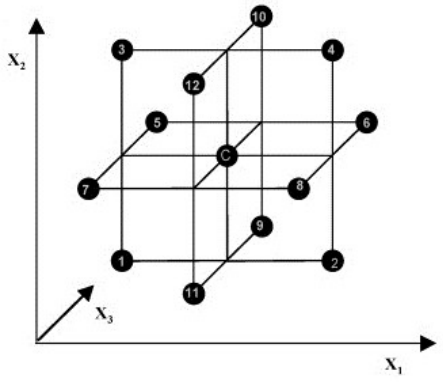


Figure 2.17: Box-Behnken design for 2 variables [156]

2.7.3 General Steps in Completing Design of Experiments

Before proceeding with either full factorial analysis or response surface methodology described in Section 2.7.1 and Section 2.7.2,respectively; the general steps in completing a DOE is as follows [148]:

- Planning phase
- Designing phase
- Conducting phase

- Analyzing phase

2.7.4 Planning Phase

In the planning phase, a problem needs to be recognized and formulated. The inputs and output(s) influencing the problem or system needs to be fully understood, before drafting the problem statement [149]. The problem statement must list down the measurable response or outcome towards achieving the purpose of a particular design or in general the goal of a company [147]. It is preferable for a response to be a variable [149]. During the planning phase, the selection of critical response is important. The response must be measurable and can be in the form of length, width, thickness, temperature etc. Once the selection of responses is complete, the experiment shall be defined to further understand what to measure, the environment for measurement taking place, the person-in-charge in performing the measurements, to name a few. Once the required response and measurement system has been defined, the design parameters are identified. Determining the important design parameters are crucial as leaving behind a potential significant parameter would produce inaccurate results.

These design parameters need to be classified into controllable and uncontrollable input factors. Controllable factors are factors which can be varied and modified during the experiment or process while uncontrollable factors are variables which are unalterable. This can be parameters from unknown sources which may be a nuisance and unwanted but can not be avoided, such as ambient temperature or moisture content in a manufacturing of a device or raw material fluctuations. There are several ways to contain these uncontrollable parameters, such as by using blocking, randomization, and replication; as described in [157]. Figure 2.18 illustrated the system's process, input parameters both controllable and uncontrollable and its responses. Design variables or design parameters or the common term factor, n; are also classified into continuous and categorical factors. Categorical factors or qualitative variable ranges over classifications such as colors, gender, city, race; while continuous factors or also known as quantitative variable are identified when the values continuously range between a definite minimum and maximum level.

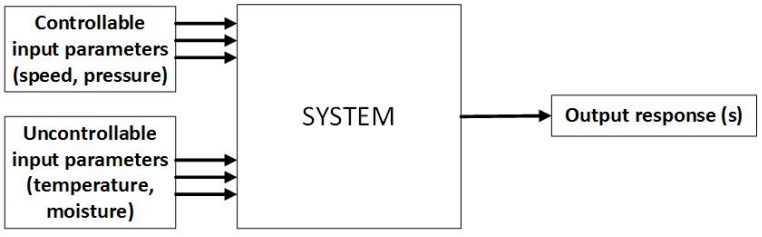


Figure 2.18: A system's process, design variables and response under DOE considerations

In the planning phase, it will be favourable to visualize the interaction between factors or design variables two-order interactions, which can be related using (2.17) taken from [148] , where n is the number of factors.

$$N = \frac{n \times (n-1)}{2} \tag{2.17}$$

2.7.5 Designing Phase

In [158], planning and designing phases are classified as a single phase i.e. design phase. It does not matter on the sub-classifications of stages involved in completing a DOE but for each DOE system completed, there must be the critical design phase, the experiment phase, and the evaluation phase.

Designing phase involved producing a design matrix which contains the design variables under investigations. Design matrix will decide the number of experiments that shall be performed in order to be analyzed after, based on the number of design variables or commonly known as the factor, n. There are several statistical methods commonly used in deciding the design matrix, for screening designs such as Placket-Burmann and factorial, which may be further reviewed in [148] or by optimization designs; the factorial [148], the response surface [159], Taguchi [160] or a mixture of these DOE techniques.

2.7.6 Conducting Phase

Running the experiments require a proper planning prior to making sure that no external factors will affect the procedures [148]. In most cases, these external factors which have been identified to possibly affect the experiments or testing would have been included as on of the design variables. This mostly applies to the industrial sector where manufacturing may take place. However, care must be given to avoid other unforeseen factors which may impact the experimental process. Proper monitoring and preventive measures must be administered before, during and after the experiments. Accurate measurements and observations are required to ensure favourable results.

2.7.7 Analyzing Phase

During analyzing phase, the results obtained are reviewed to establish whether any design variables contributed significantly towards the performance of a system or a device or a process. In addition to this, design variables which influence the variability of the device, system or process are identified. The interaction results between factors and between factors and the outcome may be used to improve the performance of the system under investigation.

It is tedious to analyze the interactions of the results without the help of statistical DOE tools such as Pareto plot and normal probability plot of factor effects, interaction plots, main effects plot and cube plots [148]. Further explanations on some of these tools have been explained when being used in analysis, such as main effects plot in Section 2.7.1 or the linear regression plot used in analyzing the reliability testing of a circuit under investigation Chapter 4.

2.8 Mitigations of Single Event Transients

The mitigation techniques may fall under error corrections or fault tolerance. Error corrections or in some work being referred to as fault corrections are techniques applied to either correct the existing errors i.e soft errors concurrently or via off-line. Fault tolerant system or radiation-hardened system, on the other hand, is a system or circuit which has been designed to have a higher tolerance towards single event transients. Most radiation hardened techniques have been implemented at the device level and usually done in fabrication facilities which not necessarily benefit due to the high cost; although, in long run, this may reduce. Radiation hardened techniques can be classified into radiation-hardened-by-design (RHBD), radiation-hardened-by-process (RHBP) and radiation-hardened-by-shielding (RHBS). Mitigation techniques may also fall into three categories, which are device, circuit and system level. Device level techniques aimed to reduce and alleviate the SET effects at the point of particle strike, which is usually being done at fabrication level. Circuit level, on the other hand, focuses on modifications at circuit level while system level focuses on system's architecture modifications and may include some redundancy in the design process.

In analogue circuits, the SETs are mitigated mostly at the digital counterparts using error detection and correction circuits (EDACs). EDACs have been proven to be more efficient and have a lower power consumption as compared to implementing, for example, triple modular redundancy (TMR) of analogue devices for SET mitigation. In spacecraft or safety critical applications which required a high reliability, however, TMR technique still reigns although it is very expensive to implement. For ground level devices, however, other mitigation techniques have been proposed and may be at par with TMR techniques. Other techniques used for mitigation of analogue circuits are analogue checksum [24] or a technique similar to TMR, the mean voting [161] or analogue voting scheme [162]. A particular correction method implemented for comparators and operational amplifiers is by using auto-zeroing circuit [28, 29], a popular technique used to improve the imperfection of operational amplifier designs. Apart from EDACs and auto-zeroing technique at the circuit level, the SETs in linear analogue circuits have been mitigated using other fault tolerance mechanisms at device level, dealing with CMOS structure and additional materials which may react better towards SETs. As the focus

of this thesis is more on dealing with the reduction of SET sensitivity at circuit level, device and system level mitigations have been put aside at the moment.

2.8.1 Auto-zeroing Technique

As SET can be viewed as a random transient offset signal which exists in a certain period of time, methods used to reduce the offset effects i.e imperfections, in an operational amplifier are believed to be able to aid the efforts in designing a fault tolerant comparator. Two basic techniques in reducing the offset and low-frequency noise of operational amplifiers, as reported by Enz and Temes; are auto-zeroing and chopper stabilization technique [27]. Auto-zeroing technique has been implemented to a comparator to improve the impact of single event upsets [29, 28].

Auto-zeroing technique based on the basic circuit in Figure 2.19 works by running under two phases, which are sampling and signal processing phase. During sampling, the unwanted noise or offset is sampled and stored while during signal processing technique, an offset-free environment shall be made available for operation [27]. The signal path to the amplifier or comparator is disconnected while its inputs being short-circuited and set to appropriate common-mode voltage. The offset is cancelled by using a certain feedback configuration, with the control value is being sampled and stored in analogue signal as in Figure 2.20 or in digital as in Figure 2.21. The output voltage now has been forced to a small value. Then, the amplifier is reconnected to its signal source which will ideally be free of the offset. Auto-zeroing technique shall be able to sample out the offset and later removes this unwanted signals from the instantaneous point of the affected signal, either at the input or output of the operational amplifier. Auto-zeroing or auto-cancellation technique can also be performed at any intermediate nodes.

In [29], they have designed three types of SET tolerant folded cascode comparator, which are input offset storage (IOS), output offset storage (OOS) and auxiliary offset storage (AOS). IOS and OOS method however introduces capacitance in the signal path; triggering another serious issue in analogue electronic circuits. AOS comparator circuit as illustrated by Figure 2.22 on the other hand isolates the signal path from the capacitance by adding 3 auxiliary amplifiers. Although the SET impact is further amplified by the pre-amplifier gain, the SET voltage or energy is stored in two additional capacitors. As AOS comparator has negative feedback, the total error at the output reduces. AOS comparator has also shown the SET effect is shorter than then cancellation period. Figure 2.23 illustrated the differential output voltage of the AOS folded cascode comparator with SET injection where during SET injection labelled as SETs error, the output now has reduced impact from SETs. Similar to Mikkola's [28] work, the SET effect has been contained within only one clock cycle. Work by [29] improved the approach by [28] by making a direct comparison of the same topology under auto-zeroing and without auto-zeroing. In both Tao Wang's and Mikkola's SET tolerant comparator

design, it has been proven that auto-zeroing can be used to prevent the prolonged effect of SET injection to exceed more than 1 clock cycle as illustrated earlier in Figure 2.23 and Figure 2.24. It is interesting to investigate a better way to thoroughly cancel out the SET effect on the comparator rather than containing the SET in one clock cycle.

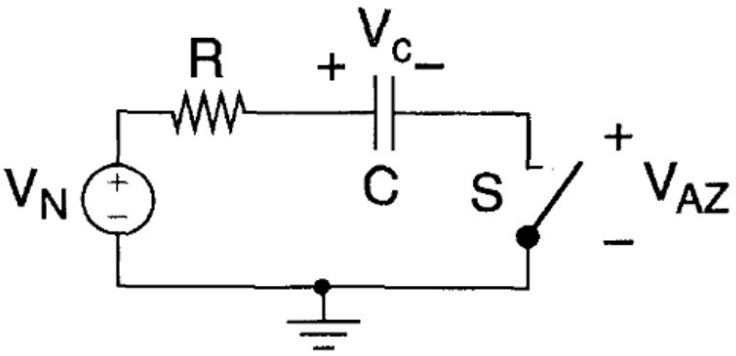


Figure 2.19: Basic Auto-zeroing circuit from [27]

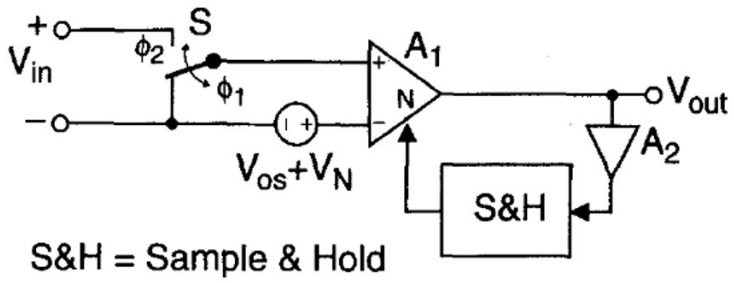


Figure 2.20: Auto-zeroing technique with an analogue offset control storage suggested by [27]

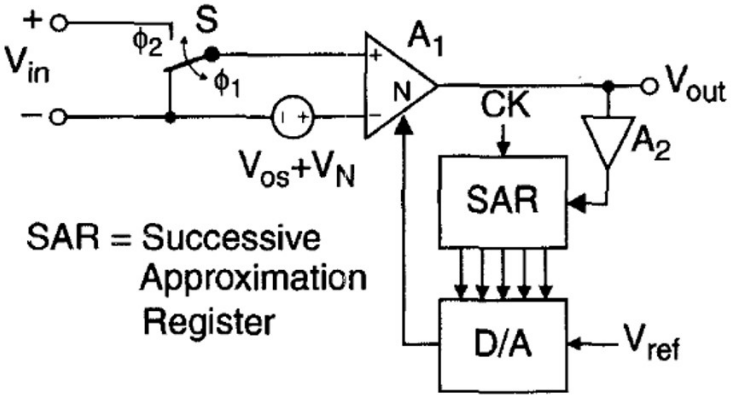


Figure 2.21: Auto-zeroing technique with a digital offset control storage suggested by [27]

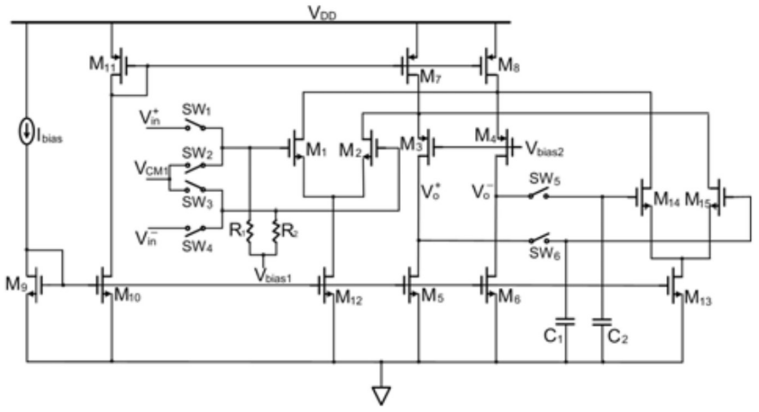


Figure 2.22: Auxiliary offset storage folded cascode comparator from [29]

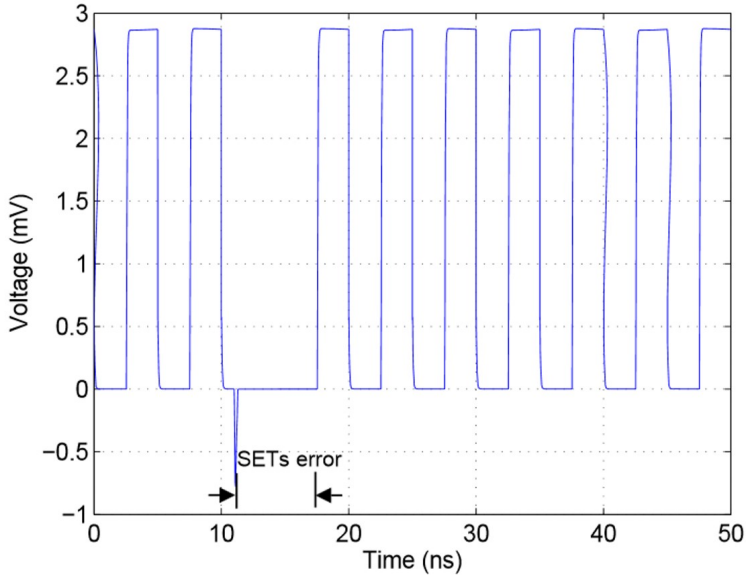


Figure 2.23: Differential output voltage with AOS folded cascode comparator with SET effect for only 1 clock cycle from [29]

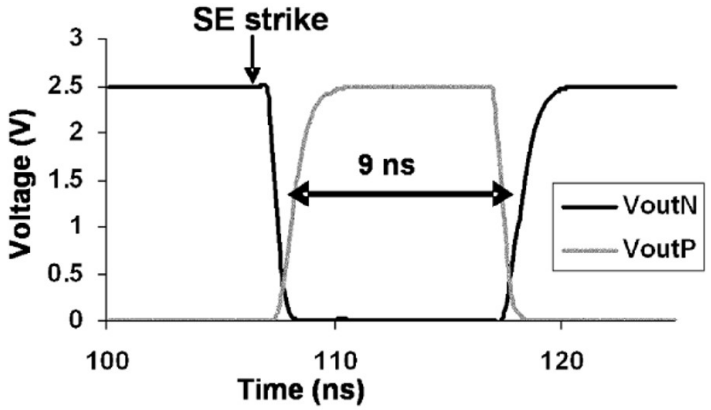


Figure 2.24: SET for auto-zeroed inverter comparator only prolongs for as long as 9 ns, less than 1 clock period taken from [28]

2.8.2 Analogue Voting

Analogue voting or analogue checksum or also known as redundancy technique has been considered as an efficient method of error corrections. Digital systems have been widely using redundancy to correct both catastrophic and parametric faults. Redundancy has some major drawbacks, which are area overhead and the importance of designing a low-power, scalable, linear and a high bandwidth voter circuit.

Although redundancy has the disadvantages of area overhead, the requirement to design a reliable low power, scalable and linear voting circuit; in critical applications in space, automotive and nuclear, exceeds the disadvantage of overhead. It has been shown that in digital applications, majority voting circuit with high redundancy factor is less efficient than median or mean voters in terms of area, power and complexity [163]. Onwards, researchers have looked into the possibility of designing efficient voter circuit, based on this finding. Askari and Nourani [25] tested whether the same findings is concluded in analogue and mixed signal circuits, and came up with better design of mean voter circuit, for improved efficiency redundancy methodology. The analogue voter designed shall not contribute towards the system's operations and the AC, DC and transient characteristics of the system. The area overhead is due to additional circuitry added which are analogue voter and duplicated circuits. The voter shall also be designed as small as possible.

As reported by Askari et al. [25], work which have been done on analogue voting does not consider the failure of DC operating point, which may result failure in operation for various ADC or did not consider the catastrophic faults on analogue circuits caused by transient errors and did not address the sensitivity analysis of the system [164]. Askari and Nourani, in their work, has established a design methodology to accurately decides the optimal redundancy factor for a fault-tolerant mixed and analogue circuits using redundancy technique. Prior to designing a redundant analogue circuit, a sensitivity analysis has been performed. Similar to this work, sensitivity analysis has already been completed and sensitive transistors have been recognized. Askari has then replaced the sensitive points in their circuits with the N-mean voters. Their mean voter as shown in Figure 2.25 has been claimed to portray fast decision making and is low cost.

The sensitive points of a circuit has been replaced with analogue N-mean voter together with the duplicated circuitry of that particular circuit block. The optimal factor of the mean voter, N has been determined using an algorithm, as in Figure 2.26, which compares the most sensitive analysis to the next sensitive point in the circuit. The relative error, RE of the circuit has been used as the metric to measure the reliability of the circuit, given by (2.18). The algorithm started with the most sensitive circuit or section or nodes or transistor. The redundancy factor of that particular section is increased by one and the relative error has been calculated. If the relative error improves but still does not meet the specifications, the redundancy factor is further increased by

one. If the relative error remains the same, the last determined factor is considered the redundancy factor of the tested circuit. Other critical circuit or point is analyzed for next subsequent cycle.

The algorithm established by Askari and Nourani [25] is decided by hand. An example which [25] has tested, is the 4-bit flash ADC. The 4-bit flash ADC uses 16 comparators, built based on 3-stage pre-amplifier comparator by Baker [73]. Prior to using the algorithm, the output of the ADC has been characterized for its missing codes, quantization error, percentage code error and integral non-linearity (INL). To determine the sensitivity of sub-circuits, particularly comparators, the 16 comparators have been divided into 4 sub-circuits or termed as sub-modules, consisting of 4 comparators each. Then, sensitivity of each of the sub-modules has been determined by injecting charge resembling particle strikes. The sub-modules has been sorted in decreasing order of sensitivity. The redundancy factor (N) of each sub-modules is decided using the algorithm by hand. For the most sensitive sub-module, the optimal redundancy factor has been expected to be 4 while the least sensitive sub-module, N is 1. Replacing the sub-modules with N-mean voter and its redundancy circuitry, the relative error, RE shall now be improved. The number of iterations for different sub-modules differs as the optimal redundancy factor depends on the relative error, RE. For example, the most sensitive sub-module requires 4 iterations to reach better relative error, RE, while the least sensitive requires only 1 iteration to reach better relative error, RE.

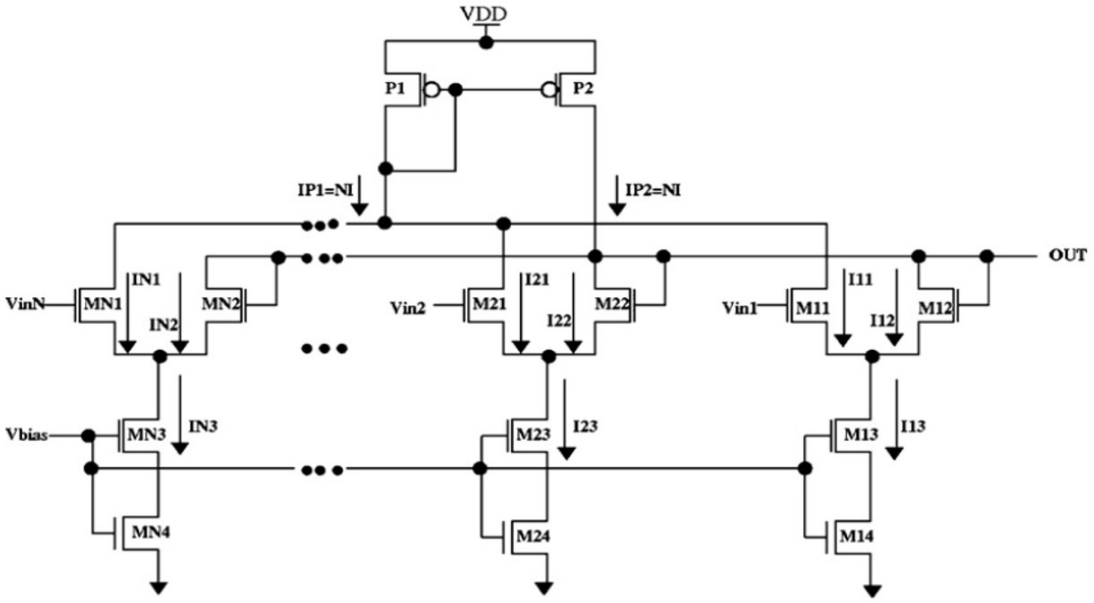


Figure 2.25: N-mean voter circuit suggested by [25]

$$RE = \frac{Erroneous\ (Output) - Expected\ (Output)}{Expected\ (Output)} \tag{2.18}$$

2.9 Summary

From the review of completed work by the comprehensive lists, it is concluded that analogue circuits suffer the same like any other VLSI circuits in under radiation effects. Most radiation testing have been performed on bipolar COTS components and only recently, some radiation testing has been performed on CMOS COTS components. With the limited access to the radiation data which resembles the closest specifications for selected analogue circuits, modelling of SETs is approximated based on the closest available radiation data as has be reported in Chapter 3. The modelling of SETs in subsequent chapters is completed using circuit-level simulations.

Amplifiers are identified to be sensitive to radiation by experiencing a temporary short disturbance pulses. Comparators investigated by scholars have also been identified to exhibit the temporary short disturbance pulses. Similar to digital circuits, analogue circuits are expected to be affected by various influencing factors while under irradiation. These factors have been identified to have either given a much worse transient fault or improved some of it, have been investigated and reported in Chapter 4. Several topologies of amplifiers and comparators have been investigated previously on their sensitivity to SETs. Analogue circuits used in memory mechanism has the tendency for the fault to be latched and propagated into its digital counterparts. Three separate circuits, 2-stage operational amplifier, and 2 comparators have been implemented and reported on its initial design and characterized in Chapter 3 and Chapter 4.

The variability studies of a hysteresis-free comparator in Chapter 4 have been investigated using the design of experiments described in this chapter. The relationship between the correlating factors has also been further elaborated in Chapter 4. The design of experiments described in this chapter and much later in Chapter 4, improved the efficiency of running the experiments.

The auto-zeroing technique used in mitigating SETs in analogue circuits, as suggested in Section 2.8 is claimed able to reduce the duration of recovery time taken for the circuits to return to normal operation. Auto-zeroing uses a sampling technique to cancel or reset the unwanted noise. The circuit which have been used comprises of switches that stores and discharge the unwanted errors. By discharging, components such as capacitors may be used. With this in mind, the next task is to test the use of capacitors to mitigate the SET captured in selected analogue circuit in Chapter 4, if possible thoroughly cancel the SET effect.

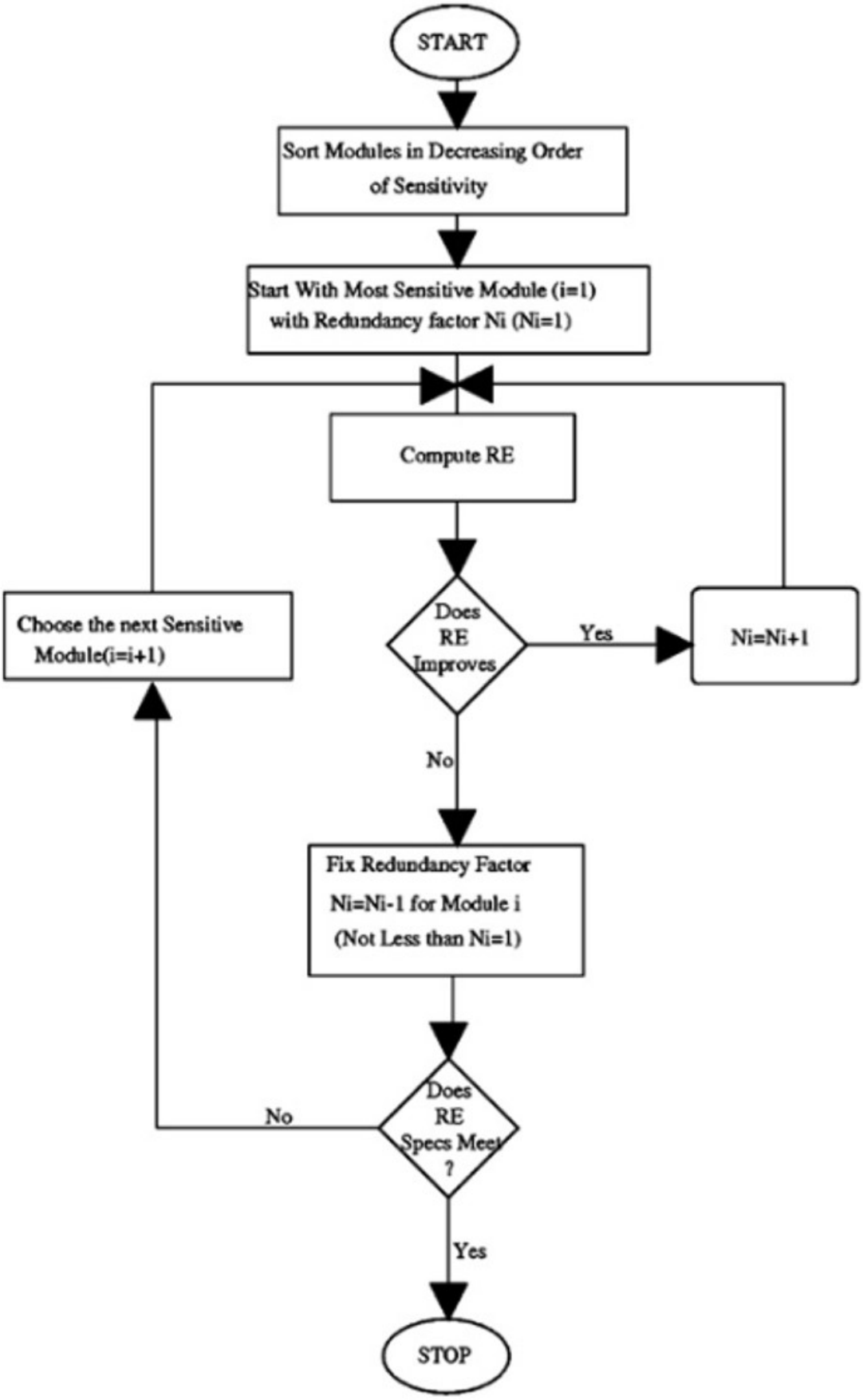


Figure 2.26: Redundancy factor determination algorithm by [25]

Chapter 3

Characterization of CMOS Analogue Electronic Circuits

The first issue which has been addressed in this work as outlined in Section 1.5, is to clarify on whether all analogue circuits suffer the same impact to the susceptibility of the circuits to radiation effects and how SETs affect the comparator's behaviour and eventually causes failure. This chapter reported whether the three selected analogue circuits, a 2-stage operational amplifier and 2 comparators will suffer the same impact as other analogue electronic circuits, using circuit-level characterizations. Before the characterization takes place, the design of hysteresis-free comparator, comparator-with-hysteresis and 2-stage operational amplifier are reported in Section 3.1, Section 3.3, and Section 3.5, respectively before each characterization analysis.

3.1 Hysteresis-free Comparator Design

The illustrated figure in Figure 3.1 is a 3-stage pre-amplifier comparator as based on [76], with the simplified block diagram as in Figure 3.2. The comparator comprises of 3 stages, which are input pre-amplifier, a positive feedback decision stage and the last stage is the output buffer. It has the capability to be implemented with or without hysteresis. The hysteresis is built-in within the circuit's topology; which has allowed the implemented hysteresis-free comparator to be reused in the faster comparator-with-hysteresis with some modification included, which later has been explained in Section 3.3.

The pre-amplifier stage acts as an amplification stage for the input signal in improving the comparator's sensitivity. The pre-amplifier will increase the minimum input signal of which a comparator will be able to make a decision. The pre-amplifier's output is needed to drive the decision stage; hence the pre-amplifier designed shall be able to convert the input voltages to minimum current level for decision making. The pre-amplifier also

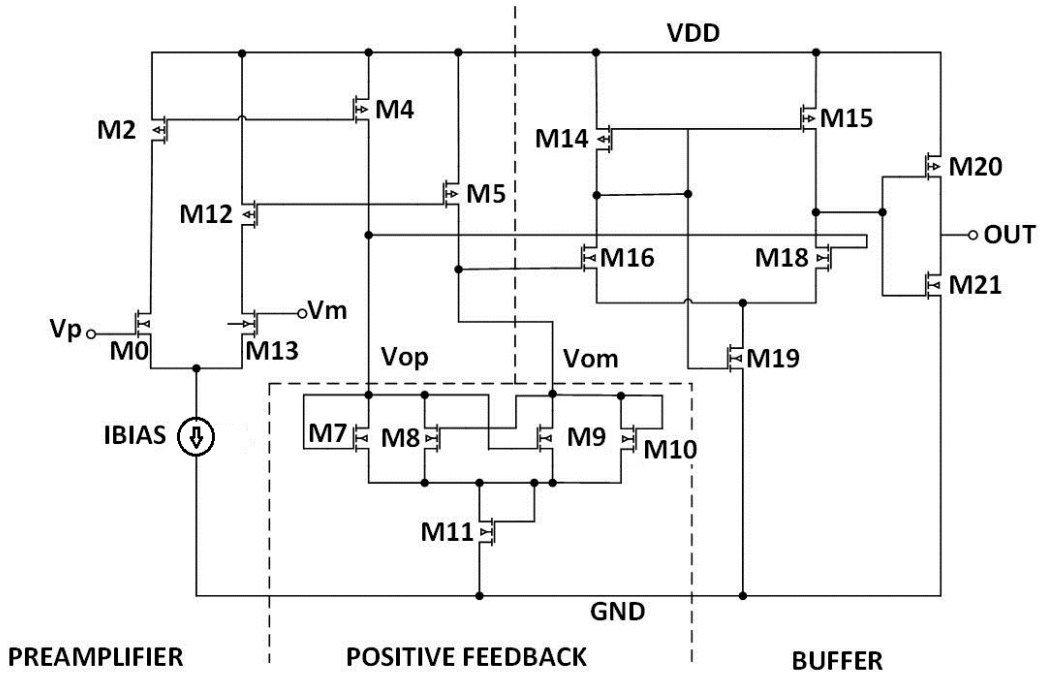


Figure 3.1: 3-stage pre-amplifier comparator

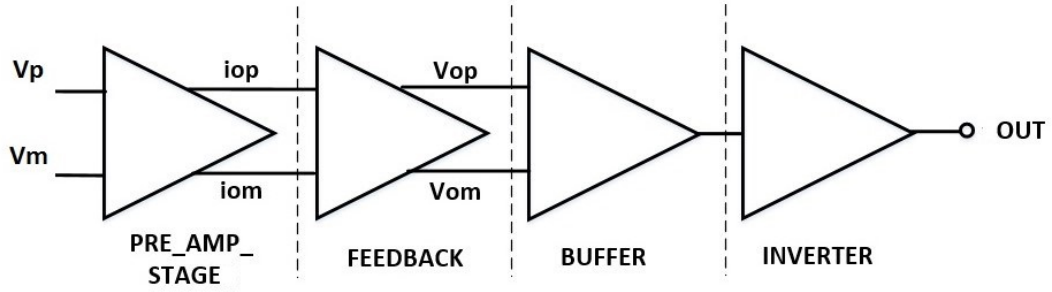


Figure 3.2: Simplified block diagram for 3-stage comparator

shall be able to isolate the input of the comparator from the switching noise, also known as kickback noise. The next stage, positive feedback circuit will determine which signal is larger between the two inputs. And finally, the output buffer stage will further amplify the results from the positive feedback circuit and converts the signal into a digital signal; which later may be used as an input into its digital counterpart circuit.

There are several actual applications which may be exposed to single event transients, such as the high sensitivity telescope used for the measurement of high energy particles in the radiation belt, as reported by Parker et al. [165]. Figure 3 in [165] illustrated a 9-bit ADC used in the telescope's electrical system. Apart from the work by Parker et al., Dietrich et al. [166] in 2014 completed a 9-bit SAR ADC design with a sampling rate of 10 MHz based on 180-nm CMOS technology for automotive applications while Polesakova [167] in July 2017 implemented a 9-bit SAR ADC for automotive sensor applications. Other reported work is by Qi et al., [168] which has proposed a 9-bit

ADC to be used in the GNSS (Global Navigation Satellite System) Receiver. These applications have initiated this work to be based on a 9-bits system.

Table 3.1 listed the related process parameters while Table 3.2 outlined the design specifications which have been used in the initial stage of the hysteresis-free comparator design. The process parameters have been taken from the Predictive Technology Model (PTM) for 130-nm CMOS technology.

Table 3.1: Process parameters for hysteresis-free comparator

Parameters	
Process (nm)	130 nm
Lmin (nm)	1200 nm
u (PMOS)	0.00835
u (NMOS)	0.05928
tox (PMOS)	2.35×10^{-9}
tox (NMOS)	2.25×10^{-9}

Table 3.2: Design specifications for hysteresis-free comparator

Parameters	
VDD	1.2
VSS	0
Voltage gain (DC gain) (dB)	48
Resolution (bits)	9

As the comparator is to be designed for a 9-bit application, the total quantization levels the system has is $2^N = 512$ levels. With 512 levels, the comparator needs to be designed to be able to discriminate a voltage difference of LSB, as expressed in (3.1). With a 9-bit resolution, the comparator's minimum gain is as (3.2).

$$\Delta V_{in} = LSB = \frac{FSR}{2^N} = \frac{2.4V}{2^9} = 4.6875mV \tag{3.1}$$

$$A_V = \frac{V_{OH} - V_{OL}}{\Delta V_{in}} = \frac{1.2V - 0V}{4.6875mV} = 256 = 48.165dB \tag{3.2}$$

The comparator shall be designed to meet at least 48 dB for a successful discrimination of voltage difference of 4.6875 mV.

As for the operation speed of comparator, the delay must be as fast as it can achieve without the operation being compromised. For offset voltage, by using 130-nm CMOS

technology; the pre-amplifier used in this comparator usually exhibits less than 20 mV offset voltage [169].

3.1.1 Designing the input stage: pre-amplification

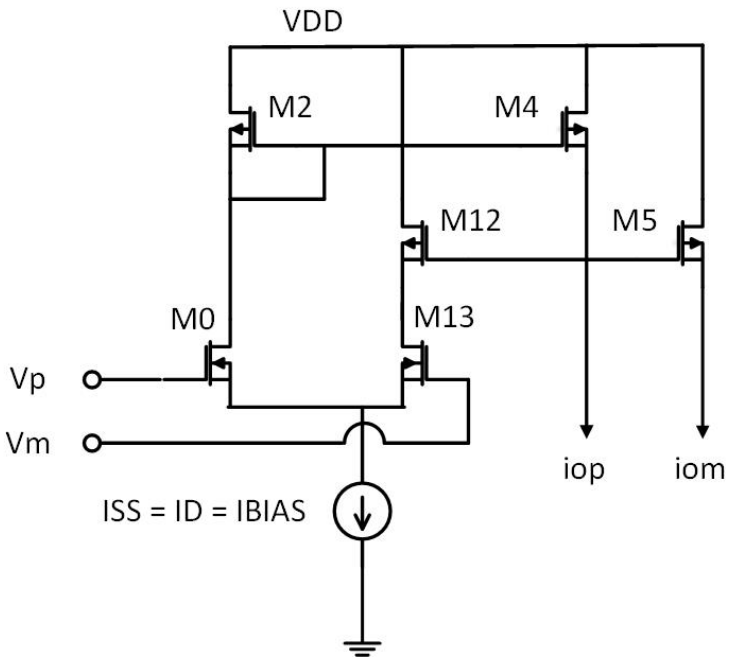


Figure 3.3: Differential amplifier with active load

The input stage is a differential amplifier with active loads, as in Figure 3.3. Input voltages, V_p and V_m; are converted into output currents, i_{op} and i_{om}. With assumptions that the circuit is symmetrical; the bias current, IBIAS is split evenly between two sections, one with M0 and the other with the M13 transistor. With a matching pair, equations as follows applies, (3.3) and (3.4).

$$\begin{aligned} g_m &= g_{m1} = g_{m2} \\ g_m &= \sqrt{2K_{(n@p)}\frac{W}{L}I_D} \end{aligned} \tag{3.3}$$

$$IBIAS = I_{D1} + I_{D2} \tag{3.4}$$

Sizes of M0 and M13 are determined by using the differential amplifier's transconductance, g_m, and the intended biasing current, IBIAS. The transconductance will set the gain of the input stage. The circuit chosen has no high-impedance nodes hence this circuit ensures a high-speed operation. Based on the process parameters of the Predictive Technology Model (PTM) 130-nm CMOS process as in Table 3.2, the size of M0 and

M13 have been initially calculated using (3.3). On the other hand, assumption method of initial selection of W/L ratio of M1 and M2 can always be an easier way to initiate the design process, as follows.

Initially selecting W/L ratio of M0 and M13 to be 10/2 and selecting bias current to be $40\mu A$ provides (3.7), with the assumption that the differential pair is balanced. Balanced differential pair gives $I_{D0} = I_{D13} = 20\mu A$. This ratio has only been used for initial design stage and has been adjusted to meet the required specifications by parametric analysis.

$$\begin{aligned} Cox_n &= \frac{\epsilon_{SiO2}}{tox_p} \\ &= \frac{3.9 \times \epsilon_0}{tox_p} \\ &= \frac{3.9 \times 8.854 \times 10^{-12}}{2.2 \times 10^{-9}} \\ &= 15.69572 \times 10^{-3} \end{aligned} \tag{3.5}$$

$$\begin{aligned} K_n &= \mu_p \times Cox_p \\ &= 0.05928 \times 15.69572 \times 10^{-3} \\ &= 0.9304422816 \times 10^{-3} \\ &\approx 930 \times 10^{-6} \end{aligned} \tag{3.6}$$

$$\begin{aligned} g_{mn} &= \sqrt{2K'_n \frac{W}{L} I_D} \\ &= \sqrt{2 \times 930 \times \frac{\mu A}{V^2} \times \frac{10}{2} \times 20\mu A} \\ &= \sqrt{1860 \times 100 \frac{\mu^2 A}{V^2}} \\ &= \sqrt{18600 \frac{\mu^2 A}{V^2}} \\ &\approx 431.219 \frac{\mu A}{V} \end{aligned} \tag{3.7}$$

The small signal equivalent circuit for M0 is shown in Figure 3.4. From the small signal circuit, M0 converts V_{GS0} into output current. Here, the input voltages can be related to the output currents by (3.8). From (3.8), it can be concluded that when V_p is larger than V_m, i_{op} is positive while i_{om} is negative and vice versa.

$$i_{op} = \frac{g_m}{2}(V_p - V_m) = IBIAS - i_{om} \tag{3.8}$$

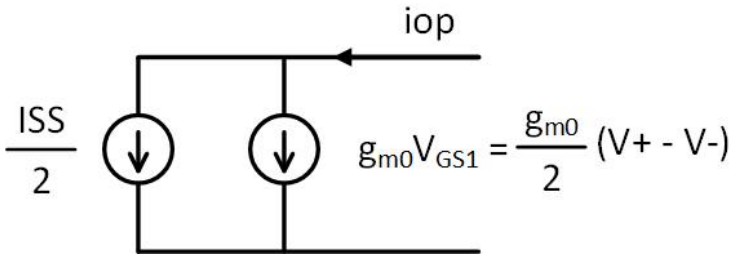


Figure 3.4: The small signal equivalent circuit for M0, with symmetrical assumptions

On the other hand, M4 and M5 have been determined using the same method for calculating W/L ratio of M0 and M13. The ratio W/L of M4 and M5 is selected as 30/2.

$$\begin{aligned} Cox_p &= \frac{\epsilon_{SiO2}}{tox_p} \\ &= \frac{3.9 \times \epsilon_0}{tox_p} \\ &= \frac{3.9 \times 8.854 \times 10^{-12}}{2.35 \times 10^{-9}} \\ &= 14.6938723 \times 10^{-3} \end{aligned} \tag{3.9}$$

$$\begin{aligned} K_p &= \mu_p \times Cox_p \\ &= 0.00835 \times 14.6938723 \times 10^{-3} \\ &= 0.1226938 \times 10^{-3} \\ &\approx 122.6 \times 10^{-6} \end{aligned} \tag{3.10}$$

$$\begin{aligned} g_{mp} &= \sqrt{2K'_p \frac{W}{L} I_D} \\ &= \sqrt{2 \times 122.6 \times \frac{\mu A}{V^2} \times \frac{30}{2} \times 20\mu A} \\ &= \sqrt{245.2 \times 20 \frac{\mu^2 A}{V^2}} \\ &= \sqrt{73560 \frac{\mu^2 A}{V^2}} \\ &\approx 271.21946 \frac{\mu A}{V} \end{aligned} \tag{3.11}$$

This g_{mp} and g_{mp} are calculated based on process parameter from Table 3.2. All these values obtained have been used at the initial design stages of the comparator and has been adjusted accordingly to the stated design specification to meet the 9-bit resolution.

3.1.2 Designing the decision stage: decision circuit

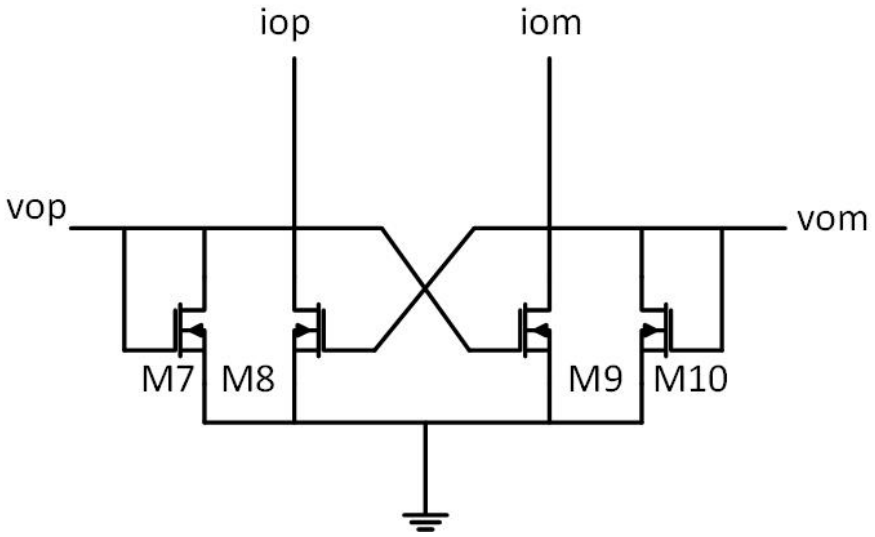


Figure 3.5: Positive feedback circuit as decision making stage

Decision circuit shall be designed to be able to discriminate mV input signals. In practical cases, a decision circuit shall also include hysteresis to reject noise in signals; but in this particular hysteresis-free comparator, hysteresis has been disabled. The decision circuit used this comparator is a bistable cross-coupled circuit, as illustrated in Figure 3.5. This configuration can only portray a single state at one time; of which being determined based on the magnitude of the input currents, i_{op} and i_{om}. Before proceeding with the rest of decision circuit analysis, (3.8) is used to determine i_{op}, provided V_p = 1.2 V and V_m = 1.0 V.

$$\begin{aligned} i_{op} &= \frac{g_{m0}}{2} \times (V_p - V_m) \\ &= \frac{431.219 \times 10^{(}-6)}{2} \times 0.2 \\ &= 43\mu A \end{aligned} \tag{3.12}$$

$$\begin{aligned} i_{om} &= IBIAS - i_{op} \\ &= 40\mu - 43\mu \\ &= -3\mu A \end{aligned} \tag{3.13}$$

From (3.12) and (3.13), it has been proven that when V_p is larger than V_m, i_{op} is positive and i_{om} is negative. Since $i_{op} \geq i_{om}$, transistor M8 and M10 are now off while M7 and M9 are on, as shown in Figure 3.6. The following qualitative analysis provides the V_{op} for this condition. (3.14) and (3.15) illustrates these conditions.

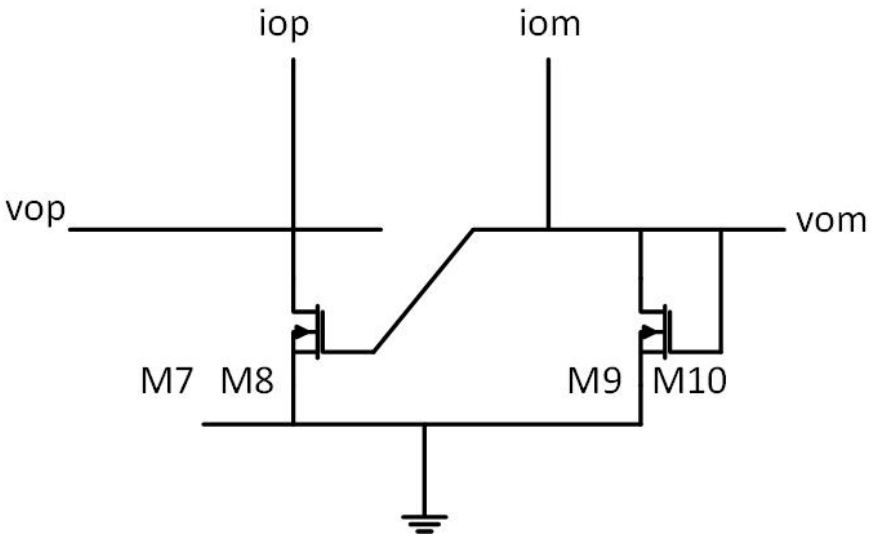


Figure 3.6: The equivalent circuit when V_{op} is greater than V_{om}.

$$I_{op} = I_8 + I_7 = 0 + I_7 = I_7 \tag{3.14}$$

$$I_{om} = I_10 + I_9 = 0 + I_9 = I_9 \tag{3.15}$$

In this condition, $V_{om} = V_{DS9} \approx 0$. V_{op} is determined from V_{GS7} when $I_{op} = I_7$. (3.16) relates output voltage, V_{op} with I_{op},with assumption that $\beta_A = \beta_7 = \beta_10$.

$$I_{op} = I_7 = \frac{\beta_5}{2}(V_{GS7} - V_{TN})^2 = \frac{\beta_A}{2}(V_{op} - V_{TN})^2 \tag{3.16}$$

If state change is required, current I_{om} is increased, which eventually decreases I_{op} and will cause V_{op} to decrease as well. As V_{op} decreases, transistor M9 will shut off. The V_{op} value just before M7 shuts off is being determined with relation to (3.17). It is also assumed that $\beta_B = \beta_6 = \beta_7$.

$$I_{om} = I_9 = \frac{\beta_7}{2}(V_{GS7} - V_{TN})^2 = \frac{\beta_B}{2}(V_{op} - V_{TN})^2 \tag{3.17}$$

By dividing (3.16) with (3.17), output current I_{om} is given by (3.18).

$$I_{om} = \frac{\beta_A}{\beta_B} I_{op} \tag{3.18}$$

The V_{op} value now can be determined from (3.19), which is based on (3.16) and (3.26).

$$V_{op} = \sqrt{\frac{2I_{op}}{\beta_A}} + V_{TN} \tag{3.19}$$

In an opposite case, where V_p = -1.2 V and V_m = 1.0 V, i_{om} is larger than i_{op}; as shown in (3.20) and (3.21). Since $i_{om} \geq i_{op}$, transistor M8 and M10 are on while M7 and M9 are off as illustrated by Figure 3.7. (3.22) describes I_{om} while (3.23) describes I_{op}.

$$\begin{aligned} i_{op} &= \frac{g_{m0}}{2}(V_p - V_m) \\ &= \frac{431.219 \times 10^{(}-6)}{2} \times -0.2 \\ &= -43\mu A \end{aligned} \tag{3.20}$$

$$\begin{aligned} i_{om} &= IBIAS - i_{op} \\ &= 40\mu - (-43)\mu \\ &= 83\mu A \end{aligned} \tag{3.21}$$

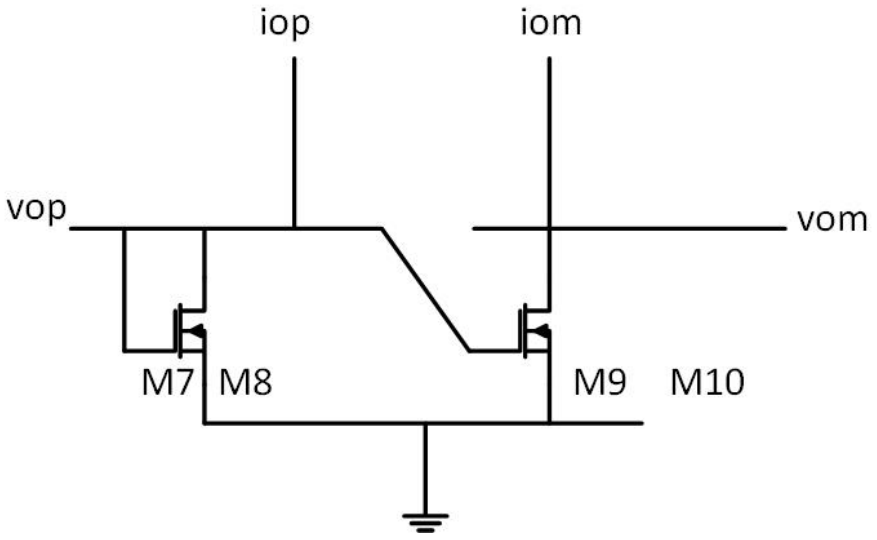


Figure 3.7: The equivalent circuit when V_{om} is greater than V_{op}.

$$I_{om} = I_10 + I_9 = I_10 + 0 = I_{10} \tag{3.22}$$

$$I_{op} = I_8 + I_7 = I_8 + 0 = I_8 \tag{3.23}$$

In this condition, $V_{op} = V_{DS8} \approx 0$. V_{om} is determined from V_{GS10} when $I_{om} = I_(10)$. The following qualitative analysis relates output voltage, V_{om} with I_{om},with assumption that $\beta_A = \beta_7 = \beta_{10}$.

$$I_{om} = I_{10} = \frac{\beta_8}{2}(V_{GS10} - V_{TN})^2 = \frac{\beta_A}{2}(V_{om} - V_{TN})^2 \tag{3.24}$$

If a state change is required, current I_{op} is increased, thus decreasing I_{om} which will cause V_{om} to decrease as well, related by (3.24). As V_{om} decreases, transistor M8 will shut off. The V_{om} value just before M8 shuts off is being determined with relation to (3.25). It is also assumed that $\beta_B = \beta_8 = \beta_9$.

$$I_{op} = I_8 = \frac{\beta_8}{2}(V_{GS8} - V_{TN})^2 = \frac{\beta_B}{2}(V_{om} - V_{TN})^2 \tag{3.25}$$

By dividing (3.24) with (3.25), output current I_{op} is given by (3.26).

$$I_{op} = \frac{\beta_B}{\beta_A} I_{om} \tag{3.26}$$

The V_{om} value now can be determined from (3.27), which is based on (3.24) and (3.26).

$$V_{om} = \sqrt{\frac{2I_{om}}{\beta_A}} + V_{TN} \tag{3.27}$$

Both V_{op} and V_{om} obtained can be bounded to less than $2 \times V_{TN}$, by adjusting the β_A value.

For hysteresis-free comparator, $\beta_A = \beta_B$, thus $I_{op} = I_{om}$. This means all the transistors, M7, M8, M9, M10 have been implemented with the same W/L ratio. For initial design, it has been decided that $(\frac{W}{L})_7 = (\frac{W}{L})_8 = (\frac{W}{L})_9 = (\frac{W}{L})_{10} = \frac{10}{1}$.

3.1.3 Designing the output stage: post-amplification

The post-amplification or the output buffer is purposely built to convert the output of the decision circuit into a logic signal. The output buffer shall be designed to be able to accept a differential input and not limited by slew-rate. A self-bias differential amplifier suggested by [76], represented by M14, M15, M16 and M18 in Figure 3.8 has been improved by adding a gate-drain connected device, M19 to make sure the decision phase

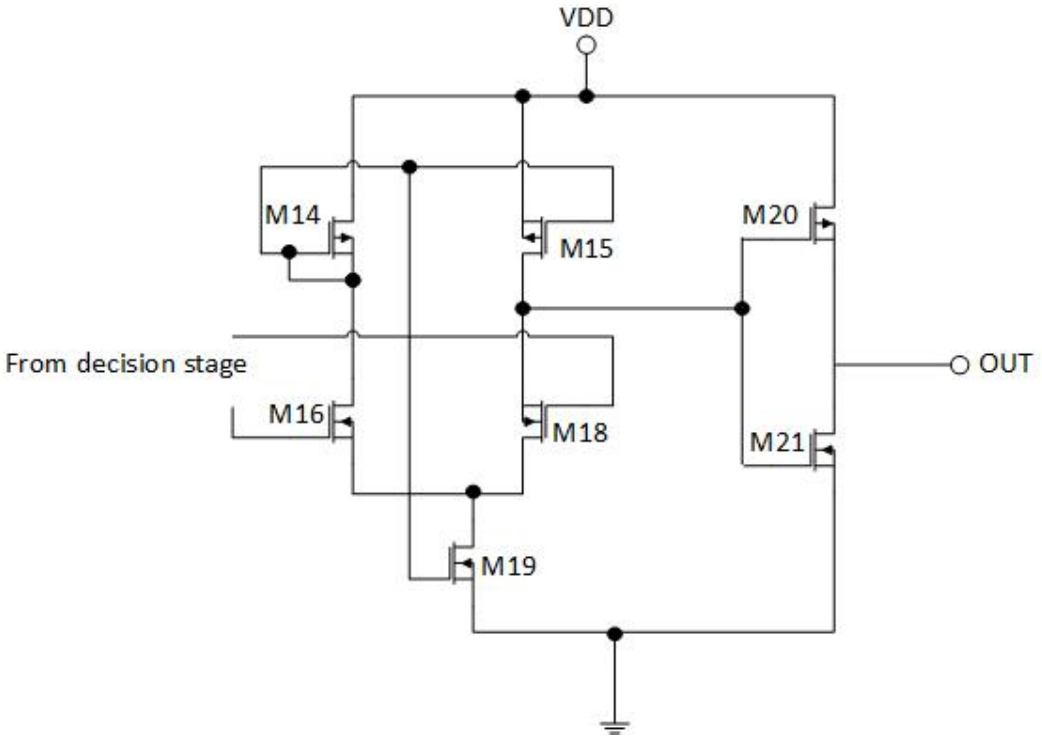


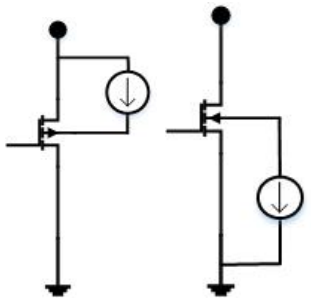
Figure 3.8: Self bias differential amplifier as buffer

moved into the common-mode range of the differential amplifier. It is termed as self-bias because it does need any external element to set the current in the circuit apart from the voltage inputs. This simple differential amplifier takes up the difference between the two inputs, and amplify it before producing a logic signal. If the voltage input to M18 is larger than the voltage to M16, the logic is 1 and will be 0, when the voltage input to M18 is smaller than the voltage input to M16. An inverter is seen here being added to improve the gain and isolate the load capacitance from the self-biasing amplifier [76]. Additional inverter stage may be added to increase the overall comparator gain but will delay the output arrival.

Before implementing the self-bias differential amplifier to the hysteresis-free comparator, it has been tested on an individual basis. The differential amplifier has been tested whether it operates as it should be, able to amplify the differences between the two voltage inputs. The initial W/L ratio for M14 and M15 is selected to be 10/2 while for M16 and M18 as 5/2. On the other hand, $(\frac{W}{L})_{19} = 5/2$, $(\frac{W}{L})_{20} = 20/2$ and $(\frac{W}{L})_{21} = 10/2$ have been selected for the testing of the output buffer. After successfully obtaining the correct operation of the self-biased differential amplifier; it has been connected to the decision-making circuit and the preamplifier circuit. The circuit has been simulated and all the related performance specifications were now summarized in Table 3.3. The detailed DC, AC and transient simulations to obtain the stated performance speciications for the hysteresis-free comparator has been attached in Appendix A.

Table 3.3: Performance specification of hysteresis-free comparator

Parameters	
Process (nm)	120
Lmin (nm)	1200
VDD (V)	1.2
VSS (V)	0
Voltage gain (dB)	48.85
AC Gain (dB)	52.16
Resolution (bits)	9
Propagation delay (nanoseconds)	26.654
Offset voltage (mV)	15.96
Input current	40 μA



(a) PMOS (b) NMOS

Figure 3.9: SET modelling for PMOS and NMOS transistors

3.2 SET Circuit-level Characterizations for Hysteresis-free Comparator

As introduced in Section 2.5.3, there are several SET models which are available to be used to resemble the particle strikes for circuit-level characterization. Even though dual-double exponential model proposed by [110] has been claimed to no longer model the particle strike by over-driving it like the double exponential model, with both models relying on the 3D-TCAD modelling of the device and dual-double exponential model having some extra terms which so far unable to be obtained from any completed characterization work; the SET characterization in this thesis has been completed by using double exponential model. As illustrated in Figure 3.9(a), in a PMOS transistor, the SET is represented by an exponential current connected between the concerned node, for example bulk and VDD while for NMOS transistors; the current source is connected to the concerned node i.e. bulk and GND, as in Figure 3.9(b) [170].

As explained in Section 2.5 and Section 2.5.3, the modelling of the single event transients required some parameters which are only available from a physical experimentation i.e. test data from running robustness test on space-qualified devices on similar technology and environment. As the testing has been completed under certain specifications, the similar testing which has been repeated to closely follow the publicly available setup may not produce the same transient pulse to match the same specifications used by the manufacturer [78]. Thus, in this thesis, the current pulse parameters chosen has been based on values used to represent the closest technology with assumptions that the device is tested in the same environment. On an additional note, the strength of the transient pulse differs depending on the environment, the structure and types of material where particle strike has been directed to. So, it is quite impossible to model the closest circuit-level SET model for the designed analogue circuits, without at least running a 3D-TCAD characterization. For a particular model of current pulse injected, the amplitude of the pulse is typically varied to identify the critical current level of which the device will be suffering from transient faults [103]. The total amount of charge governed by this particular critical current level is termed as critical charge, Q_{crit}, as previously described in Section 2.5.3.

3.2.1 Standard Testing Parameters for SET Characterizations

Once it has been decided of the model to be used in portraying single event transient pulse or particle strikes, the test parameter values have been selected based on completed work by Pouget et al. [171] and Duran [46]. 12 sets of SET are to be applied to all the transistors, with 4 currents level and 3 biasing conditions, the high conduction state (HCS), intermediate conduction state (ICS) and low conduction state (LCS). Four currents, 200 μA , 500 μA , 1 mA and 2 mA have been selected as SET injection pulses based on the data collected by Pouget et al. [171] in their measurement of real responses of SET current strikes on MOSFETs . Different point of biasing have been identified to have impact on the SET effects on analogue circuits [111]. In digital circuits, there are 2 biasing conditions, which are the on and off condition or high and low voltages. In analogue circuits however, [46] has found out three biasing points which provides significant impact on how a device reacted to SETs. HCS, LCS and ICS are the three biasing conditions identified by Duran [46]. HCS corresponds to the state when the drain current reaches its highest value while LCS is the state when the drain current has the lowest value. The ICS, on the other hand corresponds to the state where the drain current is nearly the same for a complementary pair of PMOS and NMOS transistors. HCS has been identified at the point of injection of 300 ns, while ICS is 520 ns and LCS 800 ns. The 12 sets of characterization which consists of 200 μA, 500 μA, 1 mA, and 2 mA as current pulse and three different biasing conditions i.e. point of injection; HCS = 300 ns, ICS = 520 ns and LCS = 800 ns are simulated with V_p a sinusoidal signal of 1.2 V amplitude and 1 MHz frequency and V_m is a DC voltage of 1.0 V, which represents

5/6 of VDD. IBIAS is selected as $40\mu A$. The transient simulation time has been selected to be 100 μseconds.

3.2.2 Preliminary SET Characterizations

In the preliminary SET characterization of the hysteresis-free comparator, testing parameters are as in outlined in Section 3.2.1. However these current pulses are injected at selected arbitrary points and not at the three different biasing points. Preliminary SET characterization has been completed only to clarify that hysteresis-free comparator is sensitive to single of transients. Referring to the heavy-ion tests under 130-nm technology performed by [132] as shown in Figure 3.10, the varying SET widths measured for a range of LET provides a picture that particle strikes for different strength produce different SET widths. Although the standard deviation data shows that SET widths lasted anything below 1 ns, using longer pulse duration of 10 ns in the characterization analysis of hysteresis-free comparator is to overcome the issue being brought up on double exponential model which overestimates the impact of SET to a device. By overestimating, the device has been deemed less sensitive to SETs. Thus, by increasing the pulse duration of the SET model applied to the transistor, the overestimation may be overcome. Using the several current pulse levels suggested by [46] are to support the fact that by varying the amplitude of the pulse which may represent several LET strength, the output response may be observed for variations. Injection points can be selected at any logical points as radiation effects can occur at any time. It can be selected at certain biasing points as implemented in [46]. The duration of the pulse varies depending on the source of radiation strikes, as investigated by [172]; but variation in pulse duration is negligible when the pulse duration is significantly shorter than a circuit's response time.

The only issue will be if the pulse duration is longer, the number of clock cycles the transient fault lasted may also increase. The increased number of clock cycles for a transient fault may increase the tendency of the transient fault being latched into digital circuits. Buchner et al. [172] also mentioned that different SET test facility provides pulses with unique wavelengths, pulse widths, and spot sizes. With the different specifications used at different test facilities, it is very difficult to identify the most realistic parameter to be used in modelling the SET impact on the comparator. The initial characterization of single event transient using Duran's, [46] parameter values gave the transient response as illustrated by Figure 3.11. The SET model has been injected at transistor M5.

The different strength of the pulse strikes may have also been contributed by Auger process, as mentioned by Buchner et al. [172]. Buchner et al. stated that high level of injected charge via Auger process may also impact the robustness analysis of a circuit. In atomic physics, a vacancy in the inner-shell of an atom caused by electron collision as illustrated by Figure 3.12(a) will be filled up with another electron, which later releases energy and quickly produces X-ray or also known as photon emission [173]. Sometimes

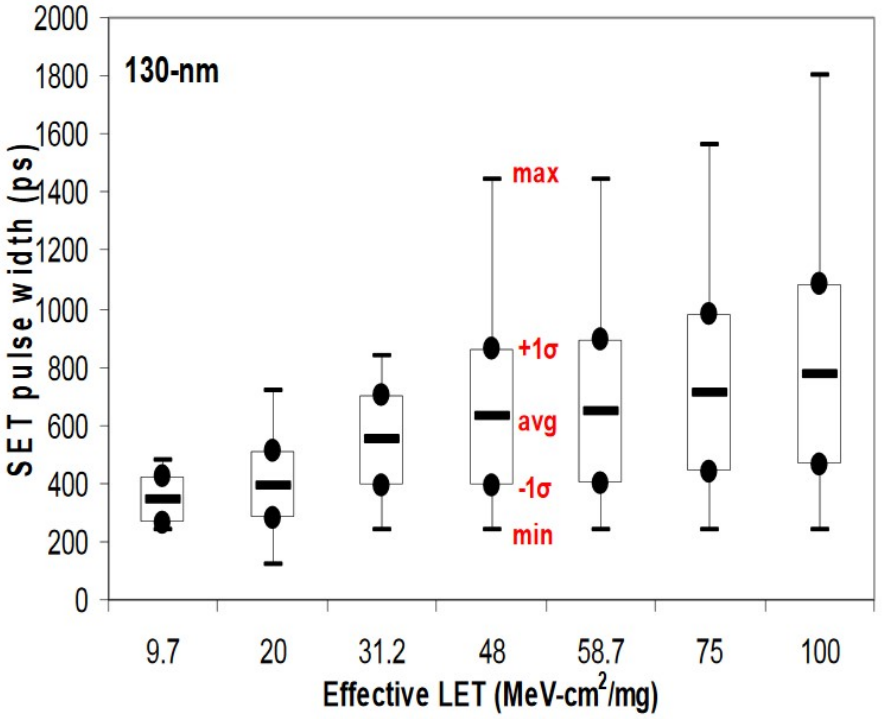


Figure 3.10: SET pulse widths from heavy ion tests under 130-nm CMOS technology after Narasimham [132]

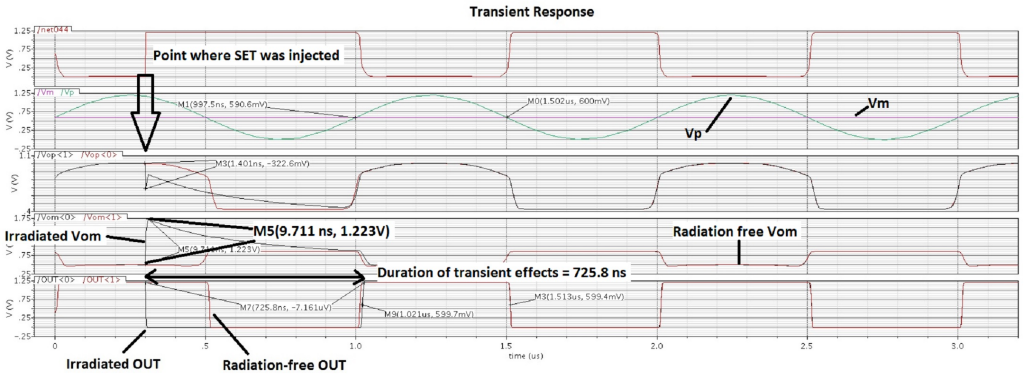
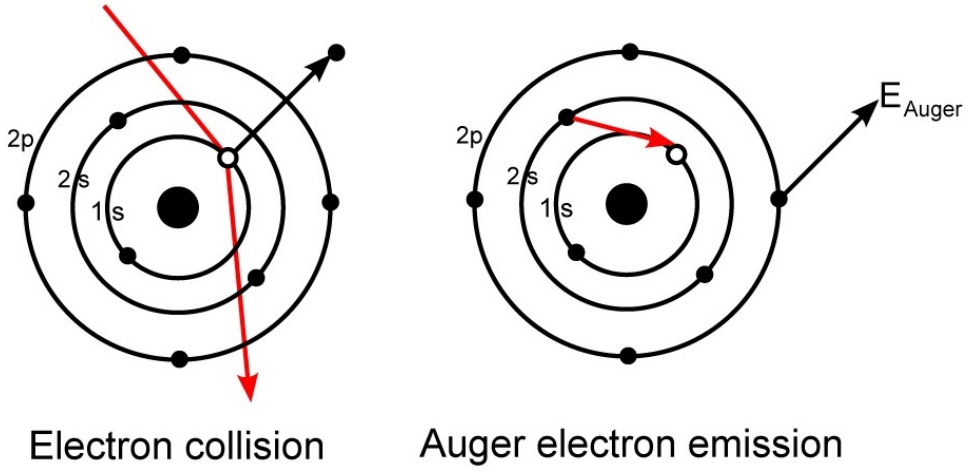


Figure 3.11: Transient effects exhibited from injecting SET to transistor M5

however, the energy is high enough that it is capable of causing an electron from nearby shell to be expelled, as shown in Figure 3.12(b) and the residual atom now has 2 electron vacancies, at least. Thus, the high level of energy portrayed by Auger process may significantly impact how a circuit reacted to electron strikes.



(a) ElectronCollision (b) AugerProcess

Figure 3.12: Auger Effect in Semiconductors [174]

3.2.3 Sensitivity Analysis on Hysteresis-free Comparator

A sensitivity analysis has been performed to identify the vulnerable transistors and also to observe the impact of a SET on the comparator's reliability. The sensitivity analysis monitors the variations of intermediate voltages, V_{op} and V_{om} between a radiation-free and irradiated response and the recovery time taken for the comparator to return to normal operation. The testing parameter values has been based on descriptions in Section 3.2.1.

A maximum voltage variation of 2.275 V at V_{op} has been observed for SET injection to M7 during the high conduction state (HCS), as illustrated in Figure 3.13. The maximum voltage variation of 2.204 V at V_{om} has been observed for SET injection to M9, also at HCS. Recovery time for a particular transistor is measured from the point where SET current is injected until the intermediate voltages, V_{op} and V_{om} returns to their crossing points. These crossing points represent the points where an output change will occur. The longest recovery time of 1.244 μs occurred under low conduction state (LCS) with a SET current of 2 mA injected into M12, at 300 ns, as illustrated in Figure 3.14. Figure 3.14 not only shows the transient effects at the worst case obtained from recovery time but also suggests a single event upset which occurs at the output of the comparator, as discussed in earlier work by Koga [17]. Table 3.4 listed the relevant effects which include the maximum and minimum intermediate voltages, V_{op} and V_{om}, and the maximum and minimum recovery time at different injection current. From the analysis, a general observation has been made that maximum variations of voltage are obtained from injecting M7, M8, and M9 transistors, the positive feedback circuit. They not only exhibit the maximum voltage variation but also high recovery time with an average of at least 0.600 μs.

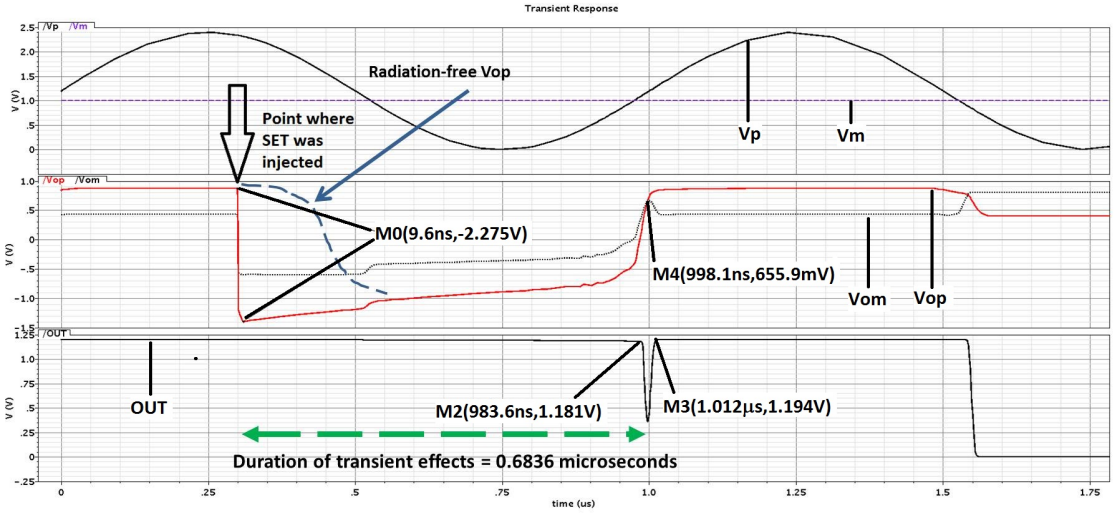


Figure 3.13: Maximum voltage variation displayed by transistor M7

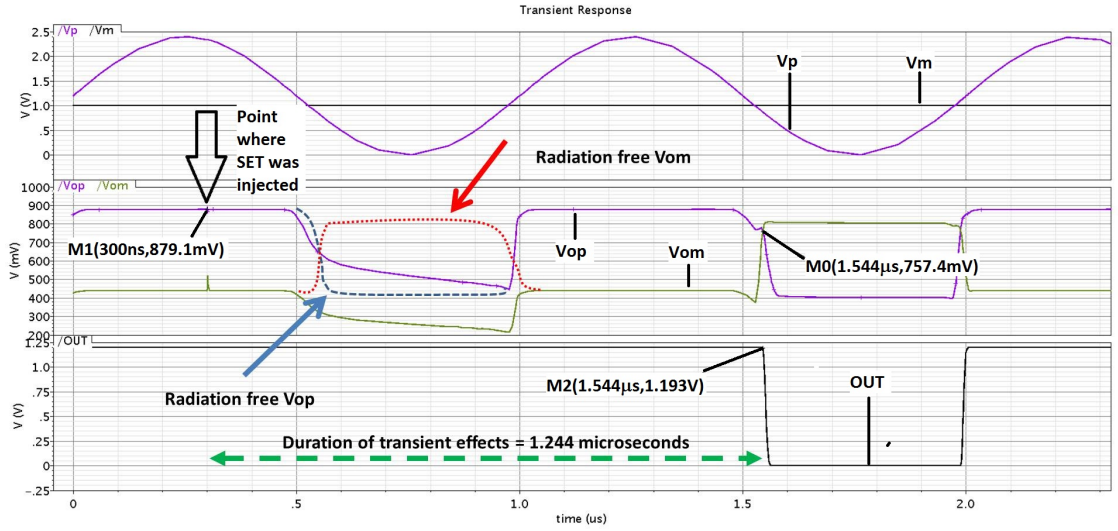


Figure 3.14: Worst transient effects

From this analysis, a consideration of which device are more sensitive has been looked into, by observing the PMOS or NMOS devices under injection. Although the largest voltage variation error has been exhibited by an NMOS device, most of the SET events affected PMOS devices more. Even the longest effect of SET has been experienced by a PMOS transistor. PMOS transistors are designed to have a larger dimension than NMOS devices, thus this may contribute towards being more sensitive to SET currents. Duran in his work has also stressed the higher sensitivity of PMOS devices towards SET currents as compared to NMOS devices [46]. This is particularly important for efforts which have been made in designing radiation-hardened devices to put more concentration on PMOS.

Table 3.4: Relevant effects for sensitivity analysis for hysteresis-free comparator

	Injection Current	200 μ A	500 μ A	1m	2m
Maximum	Voltage (Vop) Transistor	1.9859 V M7 @ HCS	2.0779 V M8 @ LCS	2.1549 V M8 @ LCS	2.275 V M7 @ HCS
	Voltage (Vom) Transistor	1.9224 V M9 @ HCS	2.0224 V M9 @ HCS	2.0924 V M9 @ HCS	2.2074 V M9 @ HCS
	Recovery Time Transistor	1.025 μ s M12 @ ICS	1.026 μ s M12 @ ICS	1.244 μ s M12 @ LCS	1.244 μ s M12 @LCS
Minimum	Voltage(Vop) Transistor	0.0755 M12 @ LCS	0.1545 V M12 @ HCS	0.1448 V M12 @ HCS	0.1446 V M12 @ HCS
	Voltage(Vom) Transistor	0.0427 V M2 @ HCS	0.1257 V M4 @ ICS	0.004 V M2 @ HCS	0.0181 V M4 @ ICS
	Recovery Time Transistor	0.167 μ s M3 @ HCS	0.1738 μ s M3 @ HCS	0.1737 μ s M3 @ HCS	0.1722 μ s M3 @ HCS

3.3 Comparator-with-hysteresis Design

As mentioned earlier in Section 3.1, the 3-stage pre-amplifier comparator by [76] can be implemented with hysteresis or without. The hysteresis-free comparator which has been implemented previously in 120-nm technology has limitations as it is only able to accept sinusoidal wave input signal of up to 20 MHz before the output swing has been skewed [135]. The purpose of designing a comparator-with-hysteresis is to investigate the impact of hysteresis and other factors which may require higher input signal frequency and faster operation. Similar to the hysteresis-free comparator, the design of comparator-with-hysteresis is based on a 9-bit system.

For this purpose, a 3-stage pre-amplifier as shown in Figure 3.15 as outlined in [175] has been added to the comparator suggested by [76] shown in Figure 3.16, and have boosted the input signals. Figure 3.17 on the other hand illustrated the overall block diagram of the comparator-with-hysteresis built for faster operation. On top of this, the design uses CMOS 65-nm technology. The transistor sizing for the overall improved comparator-with-hysteresis circuit is listed in Table 3.5. These W/L ratio have been adjusted to meet similar design specification for hysteresis-free comparator to meet the 9-bits resolution.

With the additional pre-amplifier and smaller technology, the comparator now will be able to operate correctly for sinusoidal wave input frequency up to 1 GHz before output has been skewed, provided the input voltage difference amplitude meet the minimum voltage swing. The preliminary design has been completed without hysteresis mechanism

enabled. Once the comparator has been verified to be operating correctly, the hysteresis has been enabled following the procedures explained in Section 3.3.1. Table 3.6 listed the performance specifications of the comparator-with-hysteresis without the hysteresis being enabled. The detailed DC, AC and transient simulations to obtain the stated performance specifications for the comparator-with-hysteresis has been attached in Appendix B. The hysteresis will be enabled during preliminary SET characterization and sensitivity analysis in Chapter 3 and variability analysis in Chapter 4.

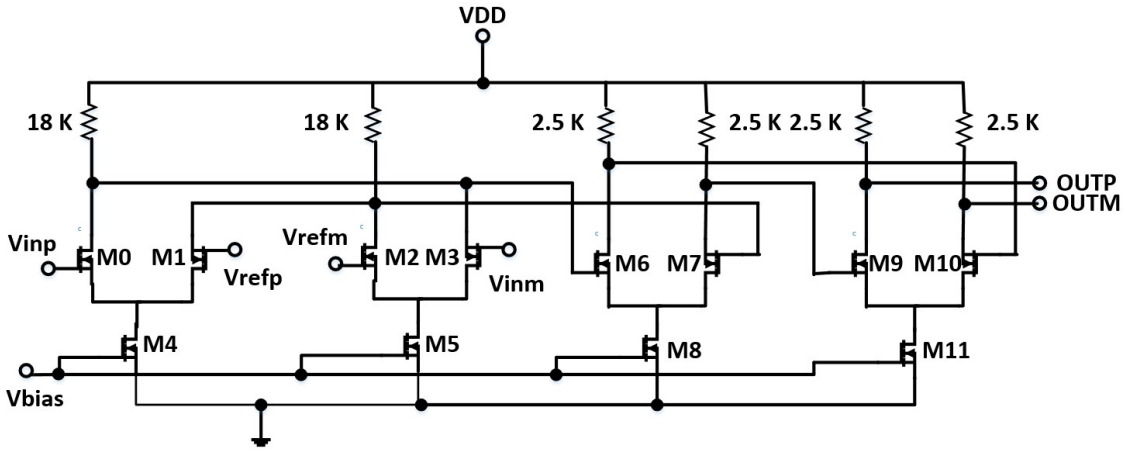


Figure 3.15: 3-stage preamplifier

Table 3.5: Transistor sizing

Transistors	W/L
M0, M1, M2, M3, M16, M19, M22, M23	2/2
M4, M5	33.33/2
M6, M7	16.67/2
M8, M9, M10, M11	33.33/2
M13, M17, M12, M25, M27, M24, M28, M26	5/4
M15, M21	15/4
M14	3.33/2
M18	41.67/2
M20	10/2
M29	8.33/2
M30	4.167/2

3.3.1 Hysteresis

Baker [76] has came up with a simple mechanism to convert a hysteresis-free comparator into a comparator-with-hysteresis in his work. For the comparator to behave like Schmitt trigger, the switching currents, i_{op} and i_{om}, as shown in Figure 3.16 must not be equivalent. If both i_{op} and i_{om} have equal currents, then the comparator does not exhibit any hysteresis. In this particular comparator topology, the hysteresis effect is

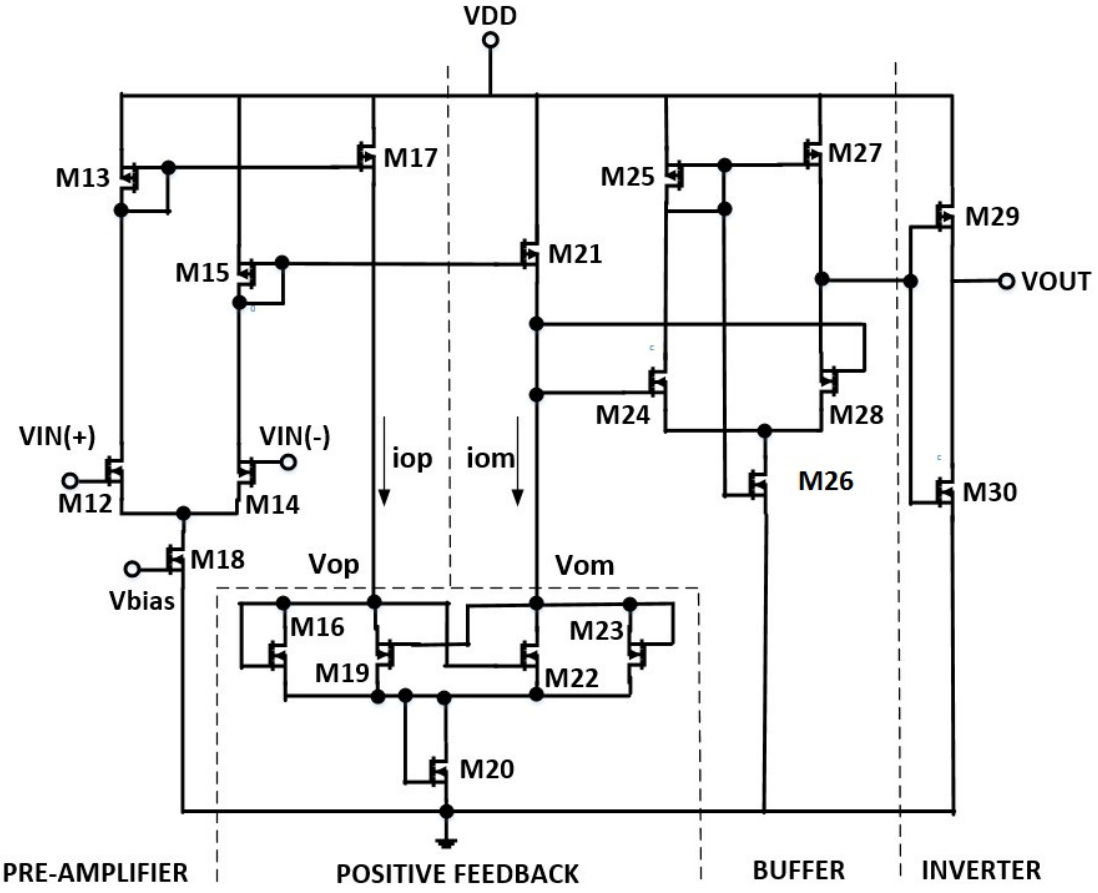


Figure 3.16: 3-stage comparator-with-hysteresis

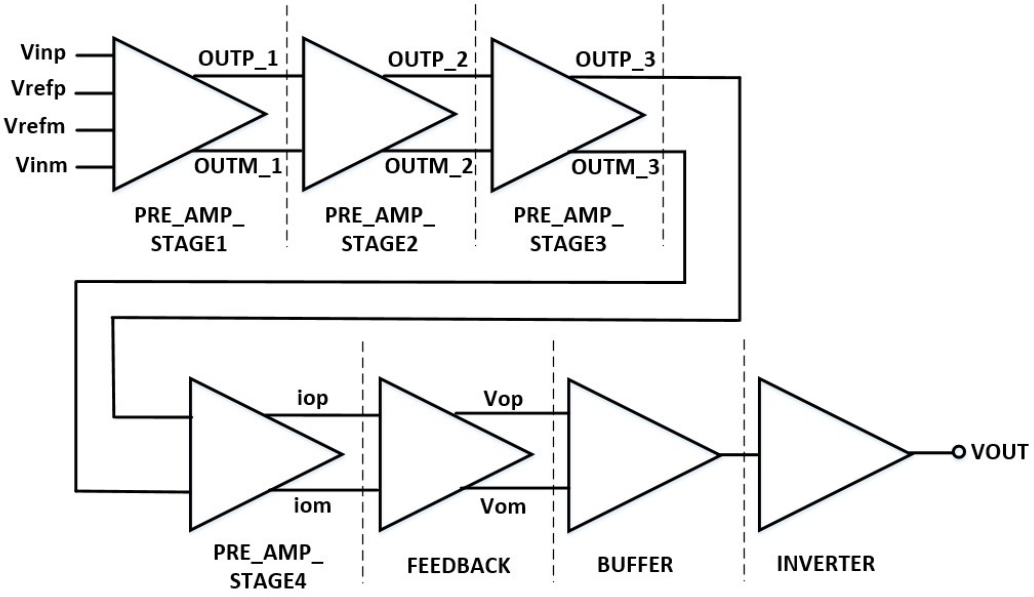


Figure 3.17: Overall block diagram of improved comparator-with-hysteresis

realized by the modifications of transistor size of M19 and M22 of the positive feedback subcircuit as illustrated in Figure 3.16 , which controls the hysteresis voltage level.

Table 3.6: Performance specifications for comparator-with-hysteresis

Parameters	
Process (nm)	65
Lmin (nm)	120
VDD (V)	1.2
VSS (V)	0
Voltage gain (DC gain) (dB)	49.5
3 dB frequency (GHz)	1.597
Bandwidth (GHz)	5.925
Resolution (bits)	9
Propagation delay (nanoseconds)	26.654
Offset voltage (mV)	4.418

Both M19 and M22 must not have the same transistor size as M16 and M23 in order to produce unequal transconductance, β. Based on Figure 3.16, $\beta_A = \beta_{16} = \beta_{23}$ and $\beta_B = \beta_{16} = \beta_{23}$. The inequality of transconductance, $\beta_A \neq \beta_B$ cause the existence of hysteresis.

In this thesis, it has been found that analogue circuits with hysteresis or memory mechanism is subjected to be affected by SETs; thus the comparator is designed to have a minimum level of hysteresis. Further increment of hysteresis is required in the variability experiments, later in Chapter 4. The transistor size of M16 and M23 is set to the minimum size, which is 120 nm while M19 and M22 have been set to 4 times of the transistor size of M16 and M23, which is 480 nm. Anything less than 4 times, did not produce any hysteresis. Even if it does, it has not been reflected during DC analysis. The minimum hysteresis value has been decided by running a preliminary parametric design by monitoring the first existence of hysteresis on the designed comparator-with-hysteresis.

The comparator has been simulated under DC analysis to obtain the hysteresis voltage of the circuit, shown by Figure 3.18. The transfer curve shown in Figure 3.18 exhibits the hysteresis effect by the change of state at two different values, designated higher and lower threshold voltage. For this particular hysteresis, the higher threshold voltage is determined from the change of state from high to low for increasing input voltage while lower threshold voltage from low to a high state for decreasing input voltage. From the transfer curve, the higher threshold voltage is 768 mV, while the lower threshold voltage is 760 mV. The hysteresis voltage is obtained from the difference of these voltages. Figure 3.19 shown the variations of transistor sizes of M19 and M22, reflecting the hysteresis voltages, with the minimal value of 8 mV. A typical hysteresis voltage recommended for space electronic components is 300 mV peak-to-peak was reported in 1998 [176], for a digital satellite positioner.

The requirement of hysteresis in safety critical components does not change much for the last 20 years. This is proven by the nominal hysteresis voltage required by a solution used as gas gauge and protection in high charge current applications [177]. This system has an analogue front end with 2 independent ADCs, developed by Texas Instruments in June 2017 and required a nominal hysteresis voltage of 250 mV. Although various other methods have been introduced to reduce the noise in a circuit without the need of hysteresis, the impact of scaling may further increases the exposure of a circuit to noises. Bu et al. [178] found that low frequency noise of MOSFETS increases with the scaling down of CMOS devices. This is supported by a study by Tan [179]. In Tan's thesis [179], the noise parameters in sub-100nm MOSFETS device will actually increase due to increment in the resistance of MOSFET's gate device. Chew et al. [180] also concluded that noise spectrum of MOSFET devices increases with the reduction of active device area. However for 45-nm CMOS technology, the noise performance would have improved [181]. The likelihood of increasing noise depends not only on the device size, thus; it is not conclusive whether hysteresis requirement in scaled down CMOS devices will increase or maintained as seen in current practical applications [177].

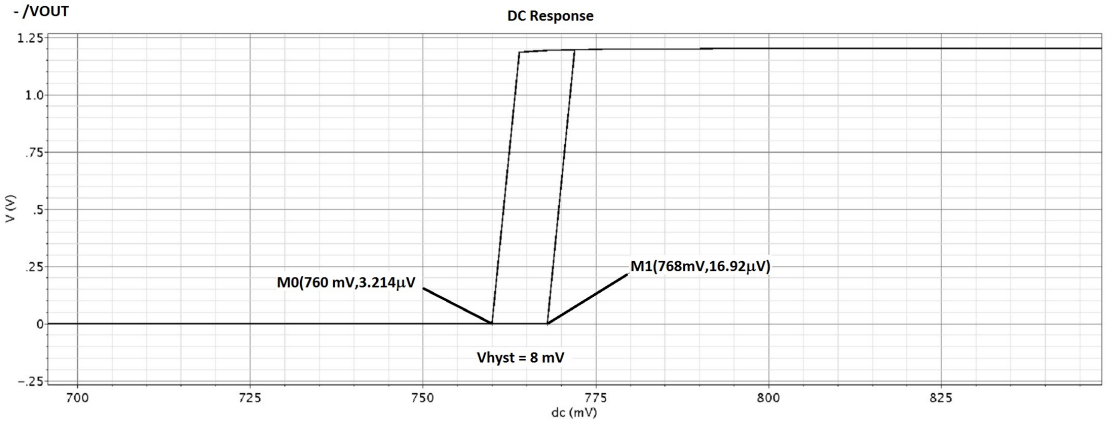


Figure 3.18: Measured hysteresis voltage

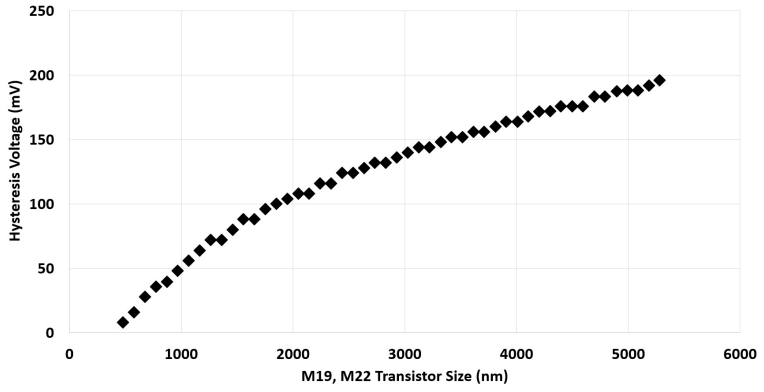


Figure 3.19: Variations of transistor sizing of positive feedback's transistor, M19 and M22 with matching hysteresis voltage (mV)

3.4 SET Circuit-level Characterizations for Comparator-with-hysteresis

Earlier in Section 3.2, the SET has been modelled based on [46]. After further investigations on more recent work on SET modelling which has been claimed as being a more realistic approach by [109]; the SET in this chapter has been modelled with Ipulse = 2 mA, τ_r = 50 ps, and τ_f = 164 ps. Based on [109], rise time, τ_r, of a double exponential model can be approximated to be one-fifth of the τ_f; thus from the compilations of TCAD models for a particular CMOS technology; even if one of the time parameters is known, it will be enough to model the SET using double exponential model realistically. The current pulse selected, Ipulse = 2 mA, however, has been based on [46], as [109] did not reveal the actual current pulse used in the investigation completed. As previously described in Section 3.2, Heijmen [103]; stated the current pulse in physical experiments such as heavy ion or laser testing, has been varied to identify the minimum current pulse at which a device will be impacted by SETs. So, the current pulse value in a circuit-level modelling can be varied as being done previously in Section 3.2, following the work by [46].

However, with the rests of the analysis in this chapter, only a single current pulse value has been used. In this analysis, a current pulse of 2 mA has been selected based on work by [132]. On the contrary, although the rise time,τ_r and fall time,τ_f, for the model used in Wrobel's investigation is based on 90-nm CMOS technology, this is by far the closest specification which has been found published. An earlier heavy ion tests as shown in Section 3.20 performed by [132], suggested average SET width to be also less than 1 ns. As opposed to SET pulse duration in Section 3.2 which is selected to be larger than the standard deviations of a 130-nm heavy ion tests to overcome estimation, SET pulse for comparator-with hysteresis has been selected to be the measured value. An assumption has been made that the 90-nm CMOS technology has almost similar TCAD model to the 65-nm CMOS technology used in this thesis. The injection point marks the point of radiation strikes on the device. As described by [109], the injection point is actually the rise time, τ_r. For the injection point, similar to the analysis completed in Section 3.2; it can actually be selected arbitrarily as SETs or other radiation effects can occur at any time or point. The significant parameters in modelling the SETs are the length measured between the current pulse's rise time to the current pulse's fall time and the current pulse's amplitude.

Although the comparator-with-hysteresis able to produce a non-skewed output when given an input voltage or input signal frequency of 100 MHz as modelled in Figure 3.21, some of the analysis in Chapter 4 are performed on various slower input signal frequencies for better illustration. Using different input signal frequency will not impact the sensitivity of a device to SETs, as proven by varying the input voltage or input signal

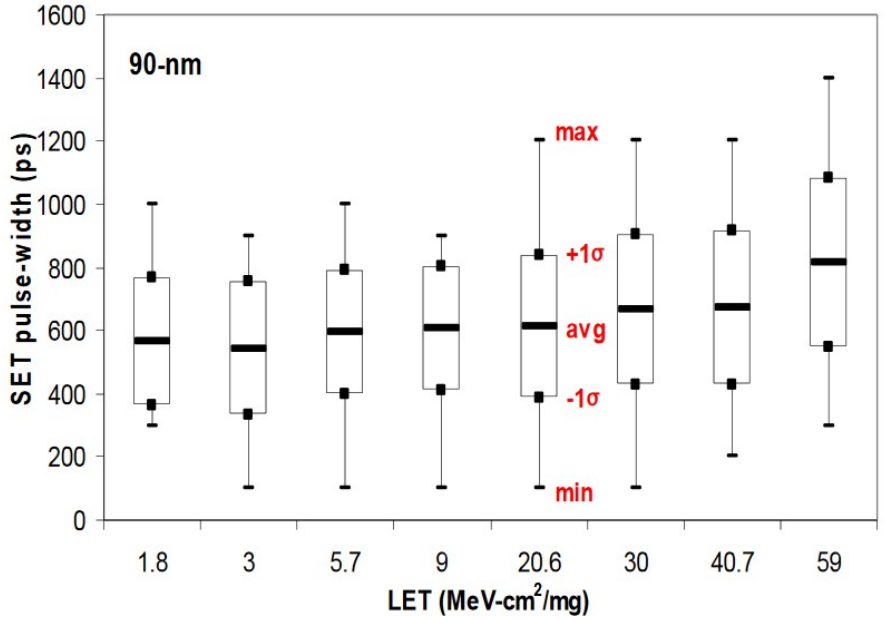


Figure 3.20: SET pulse widths from heavy ion tests under 90-nm CMOS technology after Narasimham [132]

frequency, the recovery time or the length of output error maintained for different input signal frequency.

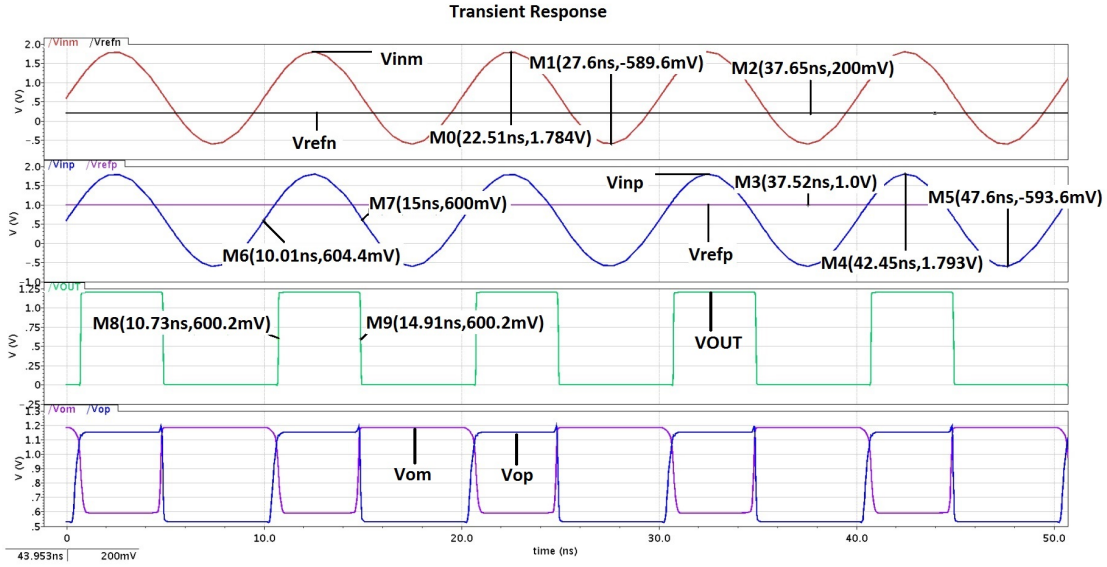


Figure 3.21: Transient response of the output of comparator-with-hysteresis

3.4.1 Preliminary SET characterizations

For initial investigation in characterizing the SETs in comparator-with-hysteresis, both input signals followed the standard testing conditions as outlined in Section 3.2.1, except with input signal frequency of 50 MHz frequency. The voltage references, Vrefp and Vrefn are 1.0 V and 0.2 V, respectively while Vbias, has been selected initially as 770 mV. Using Vbias = 770 mV, however has skewed the output and has reduced the maximum VOUT to only 230 mV, thus Vbias has been changed to 1V to obtain a maximum output voltage swing of 1.2 V.

The double exponential model parameters, are set as Ipulse = 2 mA, τ_r = 50 ps, τ_f = 164 ps and injection point at 50 ps. As a comparison, the preliminary SET investigation has also been performed with the parameters values used by [46], with Ipulse = 2 mA, τ_r = 100 ns, τ_f = 110 ns.

The initial characterization of single event transient using Wrobel's, [109] and Duran's, [46] parameter values have produced the transient response as illustrated by Figure 3.22 and Figure 3.23, respectively.

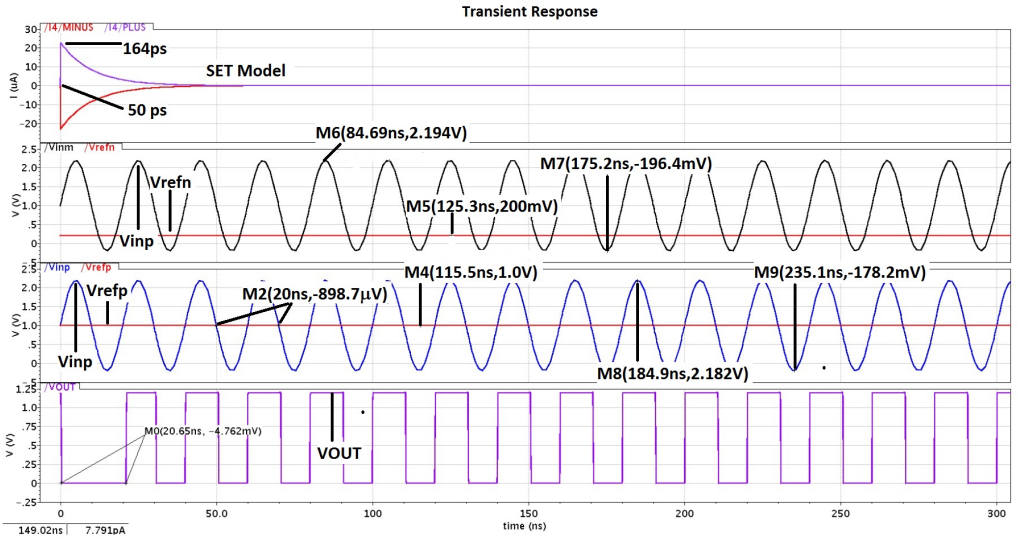


Figure 3.22: Recovery time exhibited by transistor M16 at input voltage frequency of 50 MHz and hysteresis voltage of 8 mV, using Wrobel's parameter values

By varying the input voltage or input signal frequency, the recovery time or the length of output error remains the same for different input signal frequency. The comparison of the recovery time for similar simulation settings, for different input signal frequency are illustrated by Figure 3.24 and Figure 3.25.

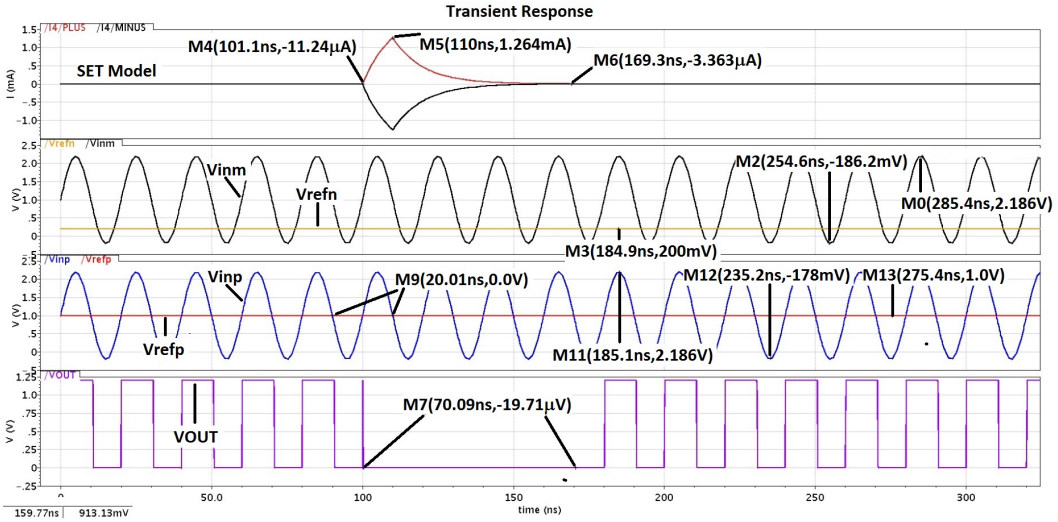


Figure 3.23: Recovery time exhibited by transistor M16 at input voltage frequency of 50 MHz and hysteresis voltage of 8 mV, using Duran's parameter values

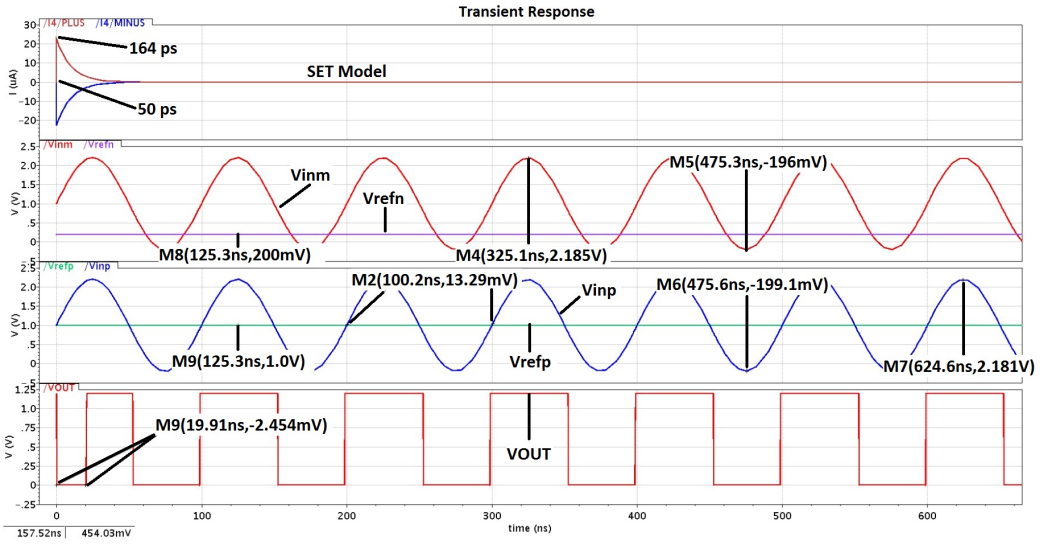


Figure 3.24: Recovery time exhibited by transistor M16 at input voltage frequency of 10 MHz and hysteresis voltage of 8 mV, using Wrobel's parameter values

3.4.2 Sensitivity Analysis on Comparator-with-hysteresis

In order to proceed with other analysis, a sensitivity analysis has been performed on comparator-with-hysteresis to identify the most sensitive transistor. Each transistor has been injected with a SET model and simulated with Wrobel's parameter values, as used

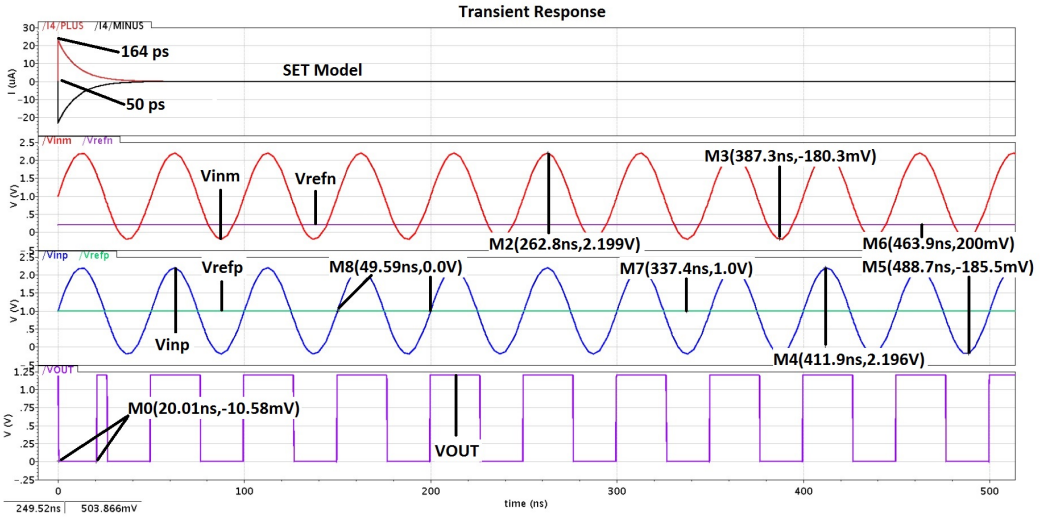


Figure 3.25: Recovery time exhibited by transistor M16 at input voltage frequency of 20 MHz and hysteresis voltage of 8 mV, using Wrobel's parameter values

in Section 3.4. The input signal frequency has been set similar to Section 3.4, except for its input signal frequency of 10 MHz. The input signal frequency is not significant as the recovery time for different input signal frequency values remained the same. The most sensitive transistor of the comparator-with-hysteresis designed belongs to the second stage pre-amplifier transistor, M21; with a 27.9 ns recovery time, illustrated by Figure 3.26. The summary of the relevant sensitivity analysis has been tabulated as in Table 3.7. The most sensitive transistor in comparator-with-hysteresis is a pre-amplifier transistor which is similar to the hysteresis-free comparator reported in Section 3.2.3.

As a comparison, the hysteresis has been disabled and the following Figure 3.27 has been included. It can be observed that the recovery time for comparator-with-hysteresis with enabled hysteresis mechanism has longer recovery time as compared with the ones without.

3.5 2-stage Operational Amplifier Design

A 2-stage amplifier consists of a cascade of voltage to current converters and current to voltage converters in its stages. As shown in Figure 3.28, a differential amplifier converts the differential input voltages, Vin1 and Vin2 to differential currents through M1 and M2 [75]. A current-mirror load represented by M3 and M4 recovers the differential voltage by converting the differential currents. The differential amplifier and current-mirror load builds the first stage of the 2-stage amplifier. The differential voltage recovered has now become the input voltage to the second stage of the 2- stage amplifier. The input voltage

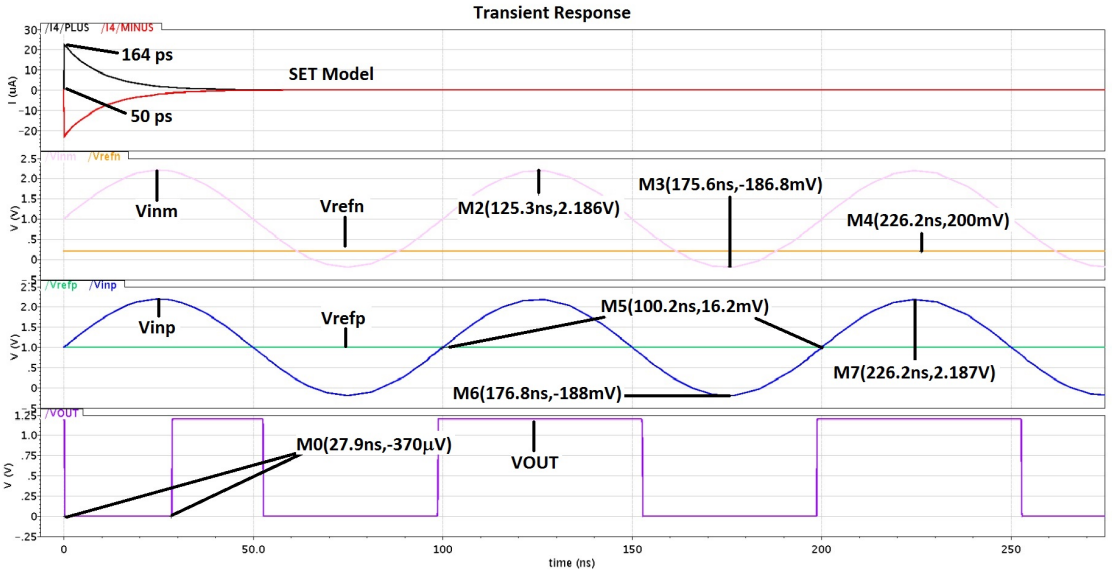


Figure 3.26: Maximum voltage variation displayed by transistor M21, for hysteresis voltage of 8 mV under input signal frequency of 10 MHz

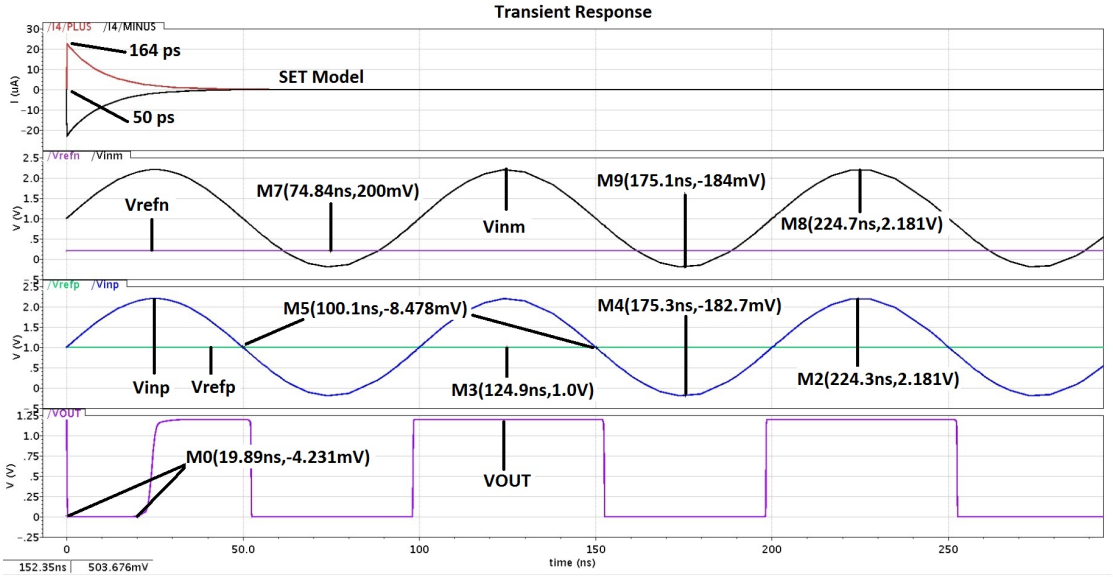


Figure 3.27: Maximum voltage variation displayed by transistor M21, for zero hysteresis voltage under signal frequency of 10 MHz

is converted into currents by the common-source MOSFET represented by M6, which later being reconverted back to voltages by a current-sink load, represented by M7.

In order to design the 2-stage amplifier, there are some important parameters which need to be decided prior to designing stages. This amplifier which is used for radiation

Table 3.7: Relevant effects of sensitivity analysis for comparator-with-hysteresis

		Vhyst	0 mV	8 mV
Most sensitive	**Pre-amplifiers**	**Recovery time (ns)** **Transistor**	**19.89** **M21**	**27.9** **M21**
	Positive feedback	**Recovery time (ns)** **Transistor**	**17.46** **M16**	**20.01** **M16**
	Buffer	**Recovery time (ns)** **Transistor**	**15.47** **M24**	**15.76** **M24**
	Inverter	**Recovery time (ns)** **Transistor**	**14.75** **M30**	**14.99** **M30**
Least sensitive	**Pre-amplifiers**	**Recovery time (ns)** **Transistor**	**0** **Various**	**0** **Various**
	Positive feedback	**Recovery time (ns)** **Transistor**	**0** **M23**	**0** **M23**
	Buffer	**Recovery time (ns)** **Transistor**	**0** **M26**	**0** **M26**
	Inverter	**Recovery time (ns)** **Transistor**	**0** **M29**	**0** **M29**

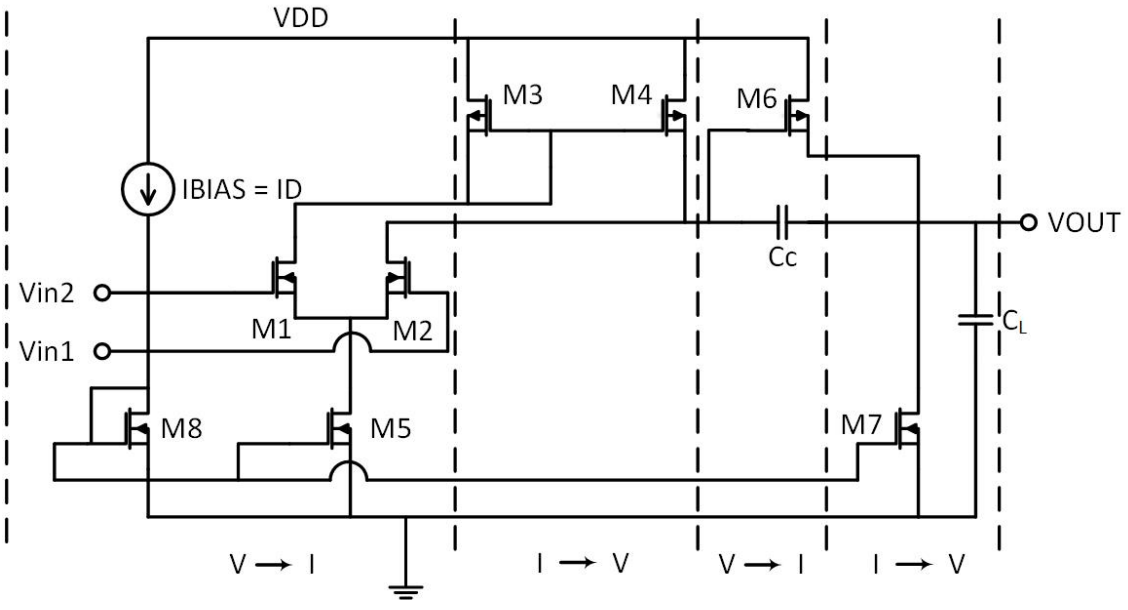


Figure 3.28: 2 stage amplifier

effect analysis has been implemented based on suggested procedures by Allen [75]. In order to understand the operation of the 2-stage operational amplifier, the initial design of the amplifier has been completed as follows. The initial specifications and the process parameters for CMOS 65-nm technology for designing the amplifier have been listed in Table 3.8. The design procedures are divided into two sections, the input, and output stage.

Table 3.8: Design specifications and process parameters for 2-stage amplifier

Parameters	
Voltage gain (DC gain)	1000 (60 dB)
Bandwidth	40 MHz
Phase margin	60 degrees
Slew rate	10 $\frac{V}{\mu secs}$
ICMR (+) (Common mode range (+))	1 V
ICMR (-) (Common mode range (-))	0.8 V
Load capacitance	1.5 pF
Process	65 nm
Lmin	200 nm
VDD	1.2
VSS	-1.2
μ (PMOS)	0.01818
μ (NMOS)	0.02161
tox_p (PMOS)	2.8 $\times 10^{-9}$
tox_n (NMOS)	2.6 $\times 10^{-9}$

3.5.1 Designing stage 1: input stage

The input stage consists of M1, M2, M3, M4, M5 and an additional current mirror circuit of transistor M8 and a current source which produces the current pulse, I_D required for biasing the stages. The first element which needs to be calculated is the compensation capacitor, C_C, as in (3.28). The load capacitance specified in Table 3.8 has been based on [182].

$$\begin{aligned} C_C &\geq (2.2/10) \times (C_L) \\ &\geq (2.2/10) \times (1.5pF) \\ &\geq 0.33pF \\ &\geq 330fF \end{aligned} \tag{3.28}$$

A value of 600 fF which far exceeds the calculated value is selected for the next step of obtaining the required current, I_D. This is entirely based on the findings reported in a lecture note by [183], stating the exact compensation capacitor to be significantly higher, up to 1.5 times of the estimated value. With the assumption of M8 being properly mirrored to the M5 transistor, the current which flows through M5 shall match the current that goes through M8. Thus by finding I_D from (3.30), the current I_5 is obtained. The slew rate of the circuit, SR is required in order to calculate current I_D, as shown in (3.29), which is given as 10 $\frac{V}{\mu secs}$. Reorganizing (3.29) produces (3.30).

$$SR = \frac{I_5}{C_C} \tag{3.29}$$

$$\begin{aligned} I_D = I_5 &= SR \times C_C \\ &= 10\frac{V}{\mu secs} \times 600fF \\ &= 6000 \times 10^{-9} \\ &= 6 \times 10^{-6}A \end{aligned} \tag{3.30}$$

The next few steps are taken to estimate the appropriate transistor sizes for transistors in input stages. M1 and M2 can be estimated by (3.31). Prior solving (3.31), gm_1, is calculated using (3.32), which required the gain bandwidth (GBW), already specified in Table 3.8. I_5 has been chosen as $10 \times 10^{-6}A$. As a reminder, $I_5 = I_1 + I_2$.

$$(\frac{W}{L})_1 = (\frac{W}{L})_2 = \frac{(gm_1)^2}{2K'_n I_1} \tag{3.31}$$

$$\begin{aligned} gm_1 &= GBW \times C_C \times 2\pi \\ &= 40MHz \times 600fF \times 2\pi \\ &= 150.796 \times 10^{-9} \\ &\approx 150.8\mu S \end{aligned} \tag{3.32}$$

It is best to choose a larger gm_1. If the designed amplifier is an ideal device, then it will be acceptable to use the calculated value, however, this is never the case. gm_1 has been chosen as 160 μS to calculate the M1 and M2 sizing. Before solving for the transistor sizing, K'_n has been calculated using (3.33) and (3.34).

$$\begin{aligned} Cox_n &= \frac{\epsilon_{SiO2}}{tox_n} \\ &= \frac{3.9 \times \epsilon_0}{tox_n} \\ &= \frac{3.9 \times 8.854 \times 10^{-12}}{2.6 \times 10^{-9}} \\ &= 13.281 \times 10^{-3} \end{aligned} \tag{3.33}$$

$$\begin{aligned} K_n' &= \mu_n \times Cox_n \\ &= 0.02161 \times 13.281 \times 10^{-3} \\ &= 287.00241 \times 10^{-6} \\ &\approx 287 \times 10^{-6} \end{aligned} \tag{3.34}$$

$$\begin{aligned} (\frac{W}{L})_1 = (\frac{W}{L})_2 &= \frac{160^2}{2 \times 287 \times 10^{-6} \times 10 \times 10^{-6}} \\ &= \frac{25600}{2870} \\ &= 8.919 \end{aligned} \tag{3.35}$$

Therefore, $(\frac{W}{L})_1 = \frac{W}{L}_2$ has been selected to be 10.

For obtaining the transistor sizing of M3 and M4 on the other hand, (3.36) is used with the aid of an initial DC simulation of the 2-stage amplifier to obtain the threshold voltages. ICMR in (3.36) is the input common mode range while $|Vt3|_{max}$ and $VT1_{min}$ are the threshold voltages for M3 at maximum and at M1 at a minimum, respectively. $|Vt3|_{max}$ and $VT1_{min}$ have been obtained from analyzing the DC simulation result as shown in Figure 3.29. To run this initial DC simulation, arbitrary transistor sizing for M3 and M4 have been selected, as long as it is larger than M1 and M2. The positive input has been assigned a DC voltage of 0.2 V while the negative input has been grounded. The ratio of M6 and M7 size must be larger than the input stage's transistor sizing. From the DC simulation, the threshold voltage for M3 is 559 mV while the threshold voltage for M1 is 520.7 mV. Since $VT1_{min}$ requires the minimum threshold voltage possible at M1, a lower value than measured voltage has been chosen while for $|Vt3|_{max}$, a maximum threshold voltage possible is required. $VT1_{min}$ has been estimated to be 500 mV and $|Vt3|_{max}$ as 570 mV.

$$(\frac{W}{L})_3 = (\frac{W}{L})_4 = \frac{2 \times I_3}{\mu_p \times Cox_p(V_{DD} - ICMR_{max} - |Vt3|_{max} + VT1_{min})^2} \tag{3.36}$$

Given VDD = 1.2 V and ICMR(+) = 1.0 and the two threshold voltage; (3.36) is solved as (3.39). The K_p' has been determined using (3.38) while Cox_p using (3.37).

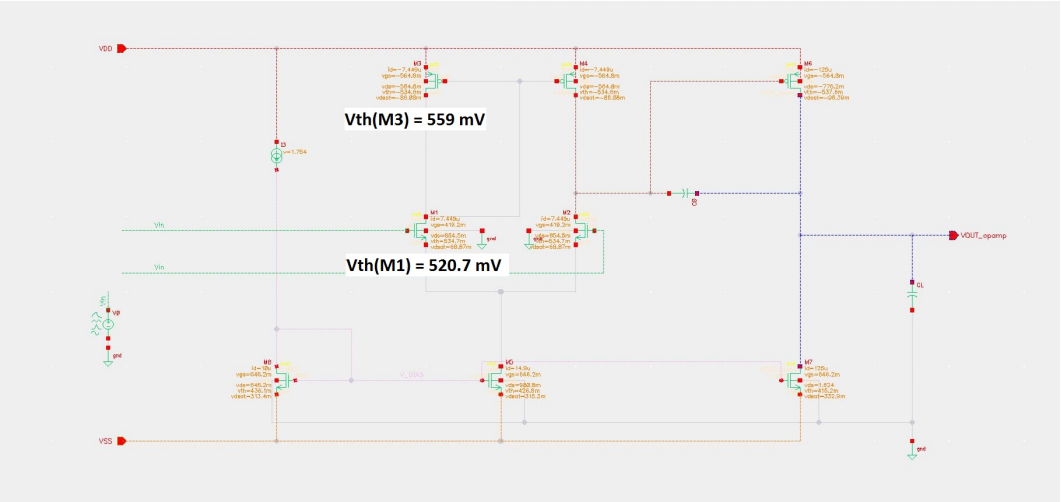


Figure 3.29: The simulated DC operating points illustrating the saturation conditions experienced by all transistors of 2-stage operational amplifier

$$\begin{aligned} Cox_p &= \frac{\epsilon_{SiO2}}{tox_p} \\ &= \frac{3.9 \times \epsilon_0}{tox_p} \\ &= \frac{3.9 \times 8.854 \times 10^{-12}}{2.8 \times 10^{-9}} \\ &= 12.33235 \times 10^{-3} \end{aligned} \tag{3.37}$$

$$\begin{aligned} K'_p &= \mu_p \times Cox_p \\ &= 0.01818 \times 12.33235 \times 10^{-3} \\ &= 224.202123 \times 10^{-6} \\ &\approx 224 \times 10^{-6} \end{aligned} \tag{3.38}$$

$$
\begin{aligned}
(\frac{W}{L})_3 = (\frac{W}{L})_4 &= \frac{2 \times I_3}{\mu_p \times Cox_p(V_{DD} - ICMR_{max} - |Vt3|_{max} + VT1_{min})^2} \\
&= \frac{2 \times 5 \times 10^{-6}}{224 \times 10^{-6}(1.2 - 1.0 - 0.57 + 0.5)^2} \\
&= \frac{10 \times 10^{-6}}{224 \times 10^{-6}(0.13)^2} \\
&= \frac{10 \times 10^{-6}}{224 \times 10^{-6}(0.0169)} \\
&= \frac{10 \times 10^{-6}}{3.7856} \\
&= 2.6416
\end{aligned} \tag{3.39}
$$

A higher ratio of 3 has been selected for $(\frac{W}{L})_3 = (\frac{W}{L})_4$.

In determining the transistor sizing for M5, similar DC simulation has been carried out, with the positive input set at higher DC voltage of 1 V and negative input maintained to ground. The threshold voltage simulated for M1 is 635.7 mV. Based on (3.40), the only value unknown is VDS_{SAT}. (3.41) determines the value of VDS_{SAT} which is later used to solve for $(\frac{W}{L})_5$, as accomplished in (3.42). In (3.42), a maximum threshold voltage for M1 is required, thus 640 mV is selected.

$$
(\frac{W}{L})_5 = (\frac{W}{L})_8 = \frac{2 \times I_5}{\mu_n \times Cox_n \times (VDS_{SAT})^2} \tag{3.40}
$$

$$
\begin{aligned}
VDS_{SAT} &\geq ICMR(-) - \sqrt{\frac{2 \times I_1}{\mu_n \times Cox_n \times (\frac{W}{L})_1}} - VT1_{max} \\
&= 0.8 - \sqrt{\frac{2 \times 5 \times 10^{-6}}{287 \times 10^{-6} \times 10}} - 0.64 \\
&= 0.8 - \sqrt{0.003484} - 0.64 \\
&= 0.8 - 0.059027 - 0.64 \\
&= 0.219 \times 10^{-3}
\end{aligned} \tag{3.41}
$$

$$
\begin{aligned}
(\frac{W}{L})_5 = (\frac{W}{L})_8 &= \frac{2 \times I_5}{\mu_n \times Cox_n \times (VDS_{SAT})^2} \\
&= \frac{2 \times 10 \times 10^{-6}}{287 \times 10^{-6}(0.219 \times 10^{-3})^2} \\
&= \frac{20 \times 10^{-6}}{287 \times 10^{-6}(0.219)^2} \\
&= \frac{20 \times 10^{-6}}{287 \times 10^{-6}(0.047961)} \\
&= \frac{20 \times 10^{-6}}{13.764922} \\
&= 1.4529686
\end{aligned}
\tag{3.42}
$$

A higher ratio of 2 has been selected for $(\frac{W}{L})_5 = (\frac{W}{L})_8$.

3.5.2 Designing stage 2: output stage

Transistors, M6 and M7 makes up the output stage, which is just a simple common source amplifier. The output stage is responsible for boosting the strength of the input voltage by increasing the output voltage swing. In digital circuits, for example in 2-stage gates; the output stage's transistor sizing or second stage shall at least be doubled of the input stage or first stage's transistor sizing. This may be used as first-hand rule of designing similar circuits. As 2-stages amplifier exhibited two dominant poles, it's relatively easy for the amplifier to maintain good stability and avoiding oscillations. As laid out in Allen [75], a phase margin of 60 °, is required to achieve stability. By assuming the phase margin of the 2-stage amplifier being 60 °, transconductance gm_6 can be obtained using (3.43), where it can be assumed that gm_6 to be approximately ten times than gm_1.

$$
\begin{aligned}
gm_6 &\geq 10 \times (gm_1) \\
&\geq 10 \times 160 \times 10^{-6} \\
&\geq 1600 \times 10^{-6}
\end{aligned}
\tag{3.43}
$$

It can be assumed that $V_{SG4} = V_{SG6}$, by achieving proper mirroring of the current-mirror load, M3 and M4. Using standard formula for gm and the assumption that $V_{SG4} = V_{SG6}$, then (3.44) follows.

$$
(\frac{W}{L})_6 = (\frac{W}{L})_4 \times \frac{gm_6}{gm_4} \tag{3.44}
$$

From the standard gm equation, obtaining gm_4 is straight forward as depicted in (3.45)

$$\begin{aligned} gm_4 &= \sqrt{\mu_p \times Cox_p \times (\frac{W}{L})_4 \times 2 \times I_4} \\ &= \sqrt{224 \times 10^{-6} \times 3 \times 2 \times 5 \times 10^{-6}} \\ &= \sqrt{6720 \times 10^{-12}} \\ &= 82.0125 \times 10^{-6} \end{aligned} \tag{3.45}$$

From (3.44), solve for $(\frac{W}{L})_6$.

$$\begin{aligned} (\frac{W}{L})_6 &= ((\frac{W}{L})_4) \times (\frac{gm_6}{gm_4}) \\ &= 3 \times \frac{1600 \times 10^{-6}}{82.0125 \times 10^{-6}} \\ &= 58.276 \end{aligned} \tag{3.46}$$

A ratio of 60 has been selected for $(\frac{W}{L})_6$.

Finally, (3.47) determined the current flowing through M6, I_6 and used this current to determine the transistor sizing for $(\frac{W}{L})_7$ by solving (3.48).

$$\frac{(\frac{W}{L})_6}{(\frac{W}{L})_4} = \frac{I_6}{I_4} \tag{3.47}$$

$$\frac{(\frac{W}{L})_7}{(\frac{W}{L})_5} = \frac{I_7}{I_5} \tag{3.48}$$

$$\begin{aligned} I_6 &= \frac{(\frac{W}{L})_6}{(\frac{W}{L})_4} \times I_4 \\ &= \frac{60}{3} \times 5 \times 10^{-6} \\ &= 100 \times 10^{-6} \end{aligned} \tag{3.49}$$

It has been established that the current which flows through transistor M6, is the same as the current flowing through M7. Thus, $I_6 = I_7$.

$$\begin{aligned}
\frac{(\frac{W}{L})_7}{(\frac{W}{L})_5} &= (\frac{I_7}{I_5}) \\
(\frac{W}{L})_7 &= \frac{I_7}{I_5} \times (\frac{W}{L})_5 \\
(\frac{W}{L})_7 &= \frac{100 \times 10^{-6}}{10 \times 10^{-6}} \times 2 \\
(\frac{W}{L})_7 &= 20
\end{aligned} \tag{3.50}$$

The transistor sizing of all transistors and other design specifications i.e. related currents have been summarized as Table 3.9. And all the related performance specifications are summarized in Table 3.10, from the preliminary simulations, which consists of DC, AC and transient analysis. The detailed DC, AC and transient simulations to obtain the stated performance speciications for the 2-stage operational amplifier has been attached in Appendix C.

Table 3.9: Transistor sizing and related calculated currents

Parameters	
$I_5 = I_8$	10 μ A
$I_1 = I_2$	5 μ A
$I_3 = I_4$	5 μ A
$I_6 = I_7$	100 μ A
$M_1 = M_2$	10
$M_3 = M_4$	3
$M_5 = M_8$	2
M_6	60
M_7	20
VDD	1.2 V
VSS	-1.2 V

3.6 SET Circuit-level Characterizations of 2-stage Operational Amplifier

In characterizing the 2-stage amplifier, the same model used in Section 3.4 has been used. The same characterization procedure completed for comparators have also been implemented for the 2-stage operational amplifier.

3.6.1 Preliminary SET characterizations

In the 2-stage operational amplifier, it has been observed that for every transistor which has been irradiated with the SET model; the performance of the amplifier worsen. From

Table 3.10: Performance specification of 2-stage amplifier

Parameters	
Process (nm)	65
Lmin (nm)	200
VDD (V)	1.2
VSS (V)	-1.2
Voltage gain (DC gain) (dB)	32
Bandwidth (MHz)	21.24
ICMR (+) (Common mode range (+)) (V)	1
ICMR (-) (Common mode range (-)) (V)	0.8
Propagation delay (μ seconds)	9.3185
Offset voltage (mV)	100
Load capacitance (pF)	1.5
Input current (mA)	10

the observation of the output response, the output voltage swing has been reduced to a substantial amount as compared to the output from a radiation-free 2-stage amplifier, as shown by Figure 3.30 and Figure 3.31. As a comparison, the model by [46] has been used, too; as illustrated by Figure 3.32. There is not so much difference between the output response caused by Duran's SET model [46] and Wrobel's SET model [109]. This is very different from the observation obtained from the analysis performed by Duran [46], as shown by Figure 3.33. The observation on the 2-stage operational amplifier reported in this thesis, however, supported the fact that performance of amplifier worsens while under irradiation, implied by [16]. The temporary positive or negative-going short-duration disturbance pulses which claimed has occurred in operational amplifiers investigated by Koga et al. [17], Duran et al. [46] and Langalia et al. [47] has not been observed in the 2-stage operational amplifier designed for this thesis. Koga's and Duran's amplifier [17, 46] use folded cascode amplifier while Langalia et al. [47] as mentioned earlier in Section 2.3.1.

The 2-stage operational amplifier produced by Langalia et al. [47] has been designed using 90-nm, 130-nm and 180-nm CMOS technology, while the 2-stage operational amplifier in this thesis used 65-nm CMOS technology. Both Langalia's and the 2-stage operational amplifier in this thesis portrays exact same topology, however a big difference between these 2 simulations are the current pulse injected or modelled into the circuit. Comparisons are made between 90-nm CMOS technology 2-stage operational amplifier by Langalia and 65-nm CMOS technology 2-stage operational amplifier designed in this thesis, as both design required approximately 31 to 32 dB open loop gain. In Langalia's work, it is stated that the current pulse plays a major role in the output

of the operational amplifier. The radiation testing applies a minimum of 15 mA current pulse injection to a maximum of 95 mA; while the characterization of the 2-stage operational amplifier in this thesis has been injected with a maximum of 2 mA. Additional analysis has been performed by using 95 mA as current pulse injection amplitude, on the same transistor radiated in Langalia's 2-stage operational amplifier. There is no significant difference between injecting 2 mA and 95 mA current pulse to M7 transistor. The transient response exhibited by the 2-stage amplifier designed in this thesis injected with 95 mA is as shown in Figure 3.34. The point of injection for the 2-stage operational amplifier in this thesis has been set at 50 ps by using Wrobel's model, while in Langalia, it has not been mentioned on the point of injection. Additional analysis has been performed, by injecting 15 mA and 95 mA at 100 ns for 10 ns. No difference on the output voltage amplitude, similar to injecting 95 mA at 50 ps.

Further increasing the current injection pulse amplitude up until 25 A at 50 ps on M7 finally produces changes to the output voltage of the operational amplifier, as illustrated in Figure 3.35. 25 A current pulse injection amplitude has never been reported as being exhibited by radiation source, thus it is impossible to inject such amount of current modelling single event transient. From the additional analysis, nothing conclusive could be summarized, except that very large current pulse shall be injected into the designed 2-stage operational amplifier for it to match the output voltage characteristics exhibited by the 2-stage operational amplifier designed by Langalia et al. [47]. It can be viewed that the output voltage of 2-stage operational amplifier in this thesis exhibited a temporary negative-going short-duration disturbance pulse when injected with 25 A current pulse. In order to arrive to a better reasoning of why the amplifier in this thesis has less sensitivity to single event transient, an extension of this analysis shall be performed. Various influencing factors affected the sensitivity of a circuit, as reported in Section 2.6.

3.6.2 Sensitivity Analysis on 2-stage Operational Amplifier

Similar sensitivity analysis like the analysis completed for comparators has been performed on the 2-stage operational amplifier. The following Table 3.11 summarizes the sensitivity analysis results. It can be seen that the most sensitive transistors are M5 and M8, as the output response during irradiation of these transistors causes the most reduction in the output voltage swing from approximately 1.6 V swing to just 0.879 mV. The least sensitive transistors are M6 and M7. The significant reduction of the output voltage swing needs to be looked into as part of extension of this work, as this has caused the operational amplifier to have reduced gain and unable to amplify small signals.

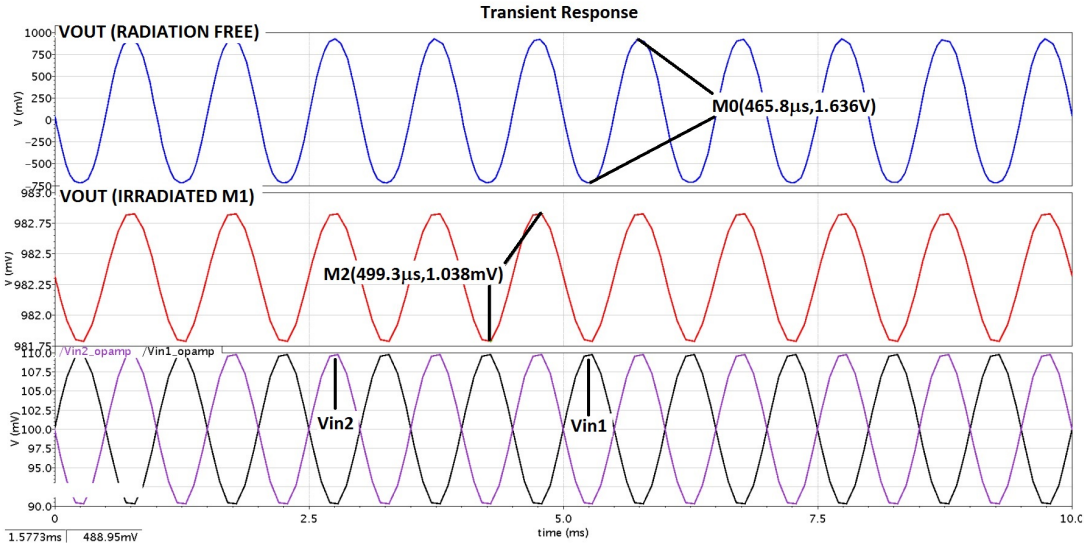


Figure 3.30: Reduced voltage swing has been observed for irradiation at transistor M1 of 2-stage operational amplifier

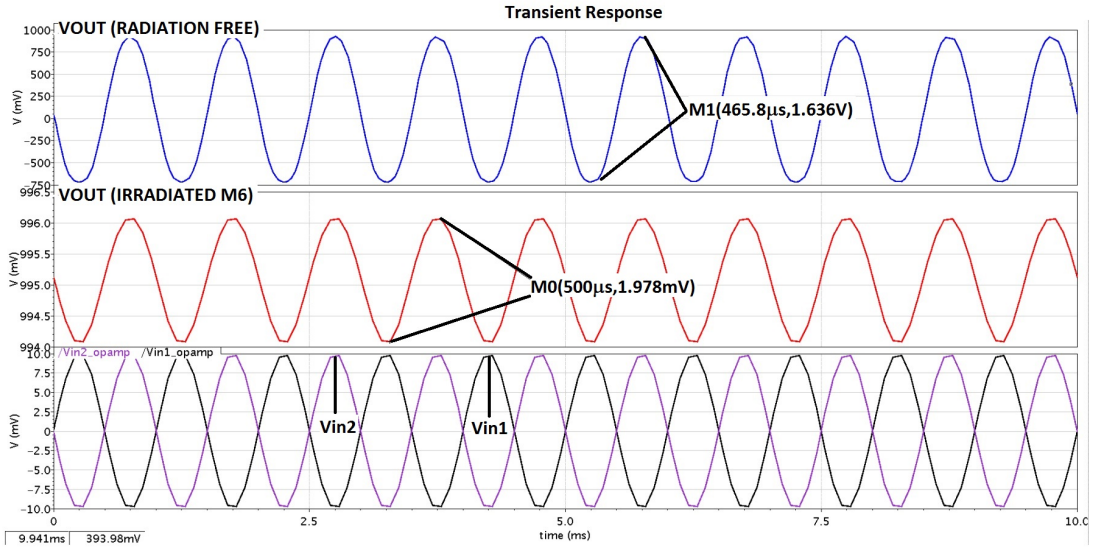


Figure 3.31: Reduced voltage swing has been observed for irradiation at transistor M6 of 2-stage operational amplifier

3.7 Using Different SET Model Parameters

All analyses performed on hysteresis-free comparator have applied SET model parameter by [46] while all other analyses in Chapter 4 and this chapter have applied SET model parameter by [109]. This section tested on what will happen to the same setting of

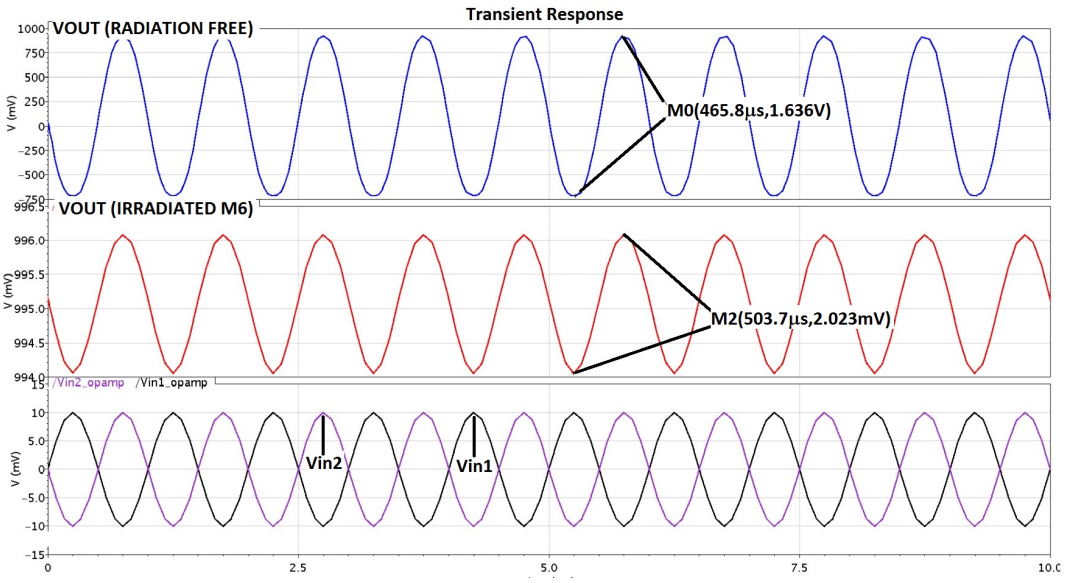


Figure 3.32: Reduced voltage swing has been observed for irradiation at transistor M6 of 2-stage operational amplifier using Duran's SET model

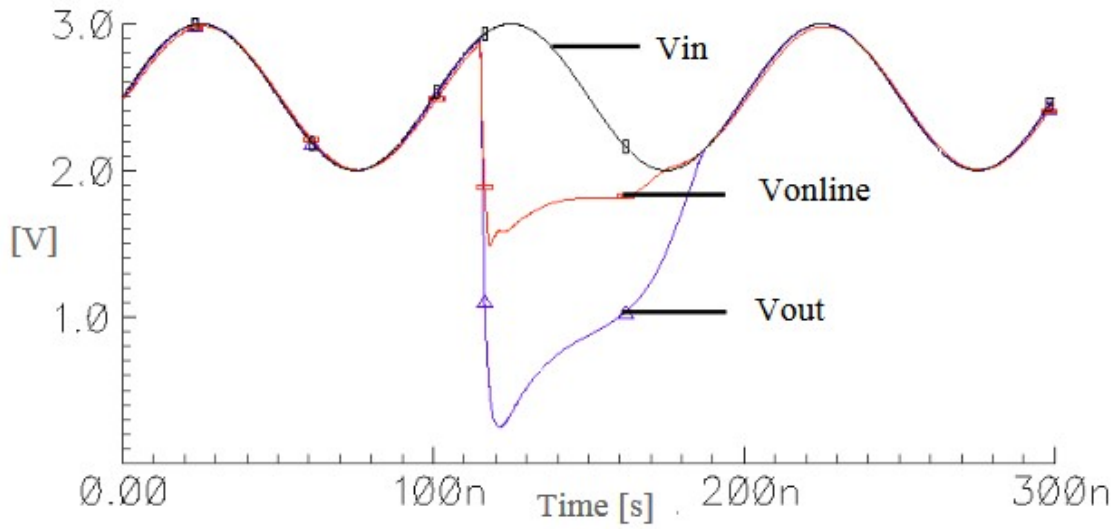


Figure 3.33: Observation of largest effect which corresponds to SET injected at one of the transistor, M3 for folded cascode comparator, from [46]

the device, using [46] illustrated in Figure 3.36 as compared to the model by [109], as shown in Figure 3.37. This section is reported to highlight that the duration of the pulse will decide the length of the recovery time. It is also believed that the point of injection marks the biasing points and may decide the length of the recovery time, too. Figure 3.22 and Figure 3.23 have already shown the differences between using these 2 SET model parameter values. From the observations, the ratio of changes to recovery time between Wrobel's and Duran's SET model parameter values are approximately 3.6. This means

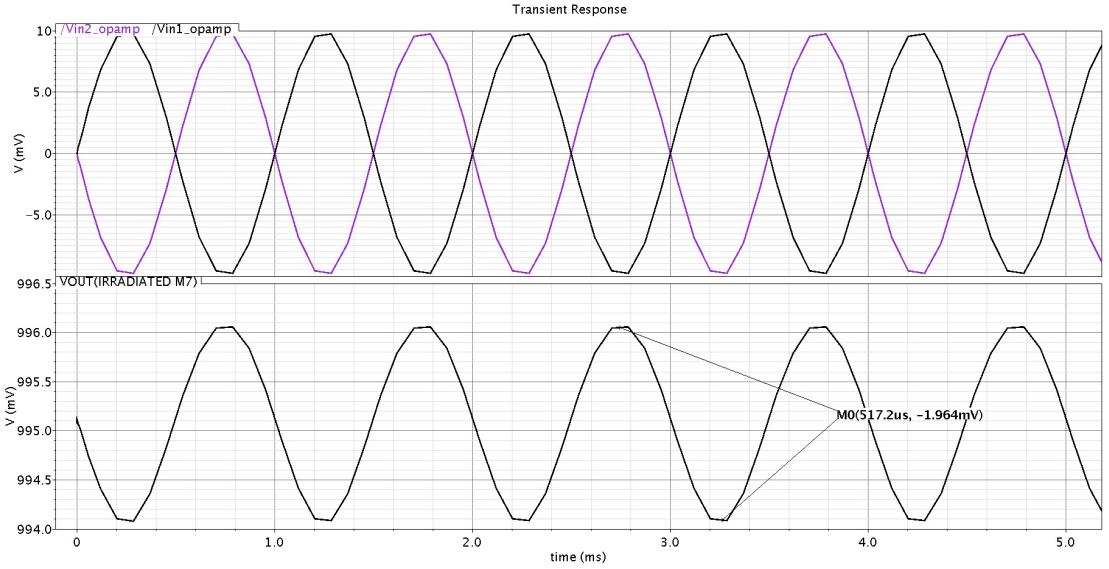


Figure 3.34: Reduced voltage swing has been observed for irradiation at transistor M7 of 2-stage operational amplifier using 95 mA current pulse

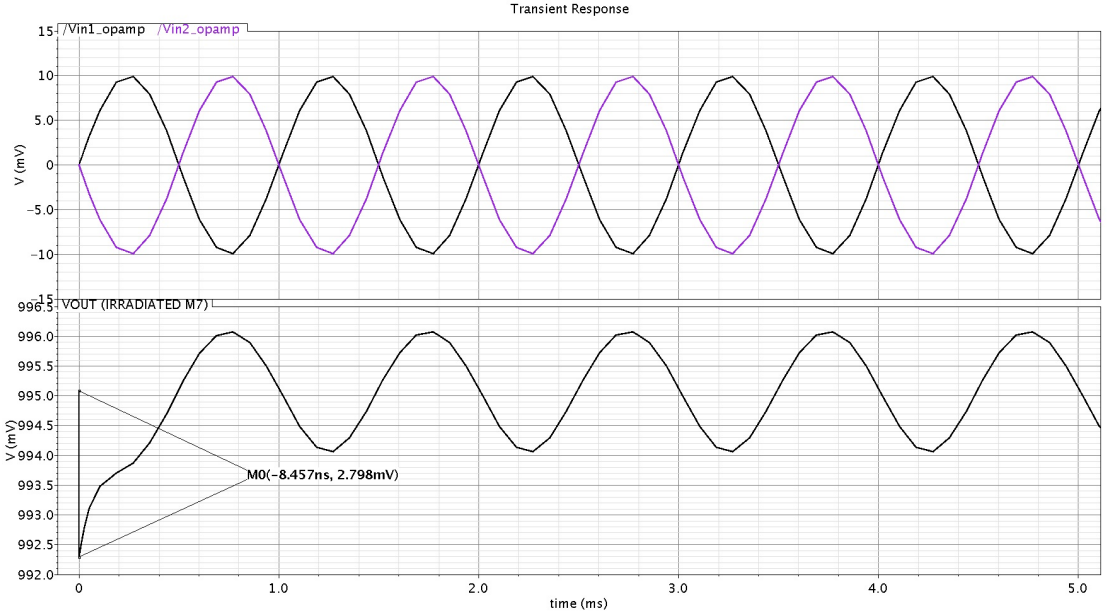


Figure 3.35: Reduced voltage swing has been observed for irradiation at transistor M7 of 2-stage operational amplifier using 25 A current pulse

that for X recovery time produced by circuit under Wrobel's injection model, the circuit under Duran's injection model has a longer recovery time, 3.6X. This ratio only applies for this particular circuit, as there are several other influencing factors in concluding the ratio of recovery time for a circuit, injected with 2 different SET current injection model. Duran's injection model has a longer SET pulse-width as compared to Wrobel's pulse-width. The duration of the current pulse will decide the length of recovery time of the output signals in analogue circuits. At the same time, the injection points at different biasing conditions will also decide the recovery time of a device under injection

Table 3.11: Relevant effects of sensitivity analysis for 2-stage operational amplifier

	Transistor	Output voltage swing	
		Wrobel's model (mV)	**Duran's model (mV)**
Input stage	**M1**	**1.038**	**NIL**
	M2	**1.038**	**NIL**
	M3	**1.038**	**NIL**
	M4	**1.038**	**NIL**
Output stage	**M5**	**0.879**	**NIL**
	M8	**0.879**	**NIL**
	M6	**1.978**	**2.023**
	M7	**1.978**	**2.023**

of SET current pulse. The ratio 3.6X only clarifies that the SET injection model using Duran's specifications has longer recovery time. Duran's specification may be used for milliseconds long SET modelling while Wrobel's may be used for nanoseconds long SET current pulse.

As discussed in Section 3.2, the pulse duration of a model may not affect the way a circuit responded to a SET. However, so far in all analyses; longer SET pulse duration exhibits longer recovery time for the device. In SET model used in all analyses for hysteresis-free comparator, the current pulse amplitude ranges from 200 μ A to 2 mA and its pulse duration was set to 10 ns while the pulse duration for the SET model parameter based on Wrobel et al. [109] is approximately 114 ps. Its current pulse amplitude has been chosen to be 2 mA for easier comparison in this section.

As compared to simulation on result as Figure 3.37, with the difference in the pulse duration of SET modelled, the transient fault in Figure 3.36 lasted longer, i.e. 111.8 ns than the analysis which have used Wrobel's pulse duration. In Figure 3.37, the transient fault lasted for only 30.22 ns.

It can not be concluded whether the pulse duration has been a significant factor in how the comparator responded or whether this is due to the different CMOS technology with a different critical charge in use. As addressed by [172], it is very important to select the correct parameter, for example, the wavelength of emitted light of pulsed laser specification in SET testing, as the wavelength of emitted light is a significant factor in determining the profiles of the charge deposition distribution. The charge track density particularly its longitudinal and lateral profiles will mimic the focused laser beam. From this experiment, longer SET duration prolonged the recovery time taken by the comparator-with-hysteresis.

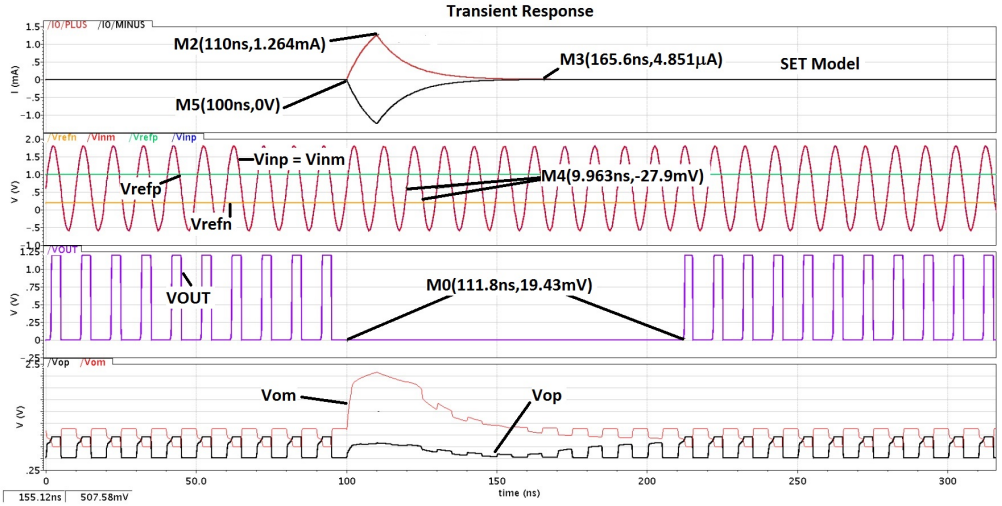


Figure 3.36: Observed output from radiation effect analysis on comparator-with-hysteresis, with input signal frequency of 100 MHz, using Duran's SET model

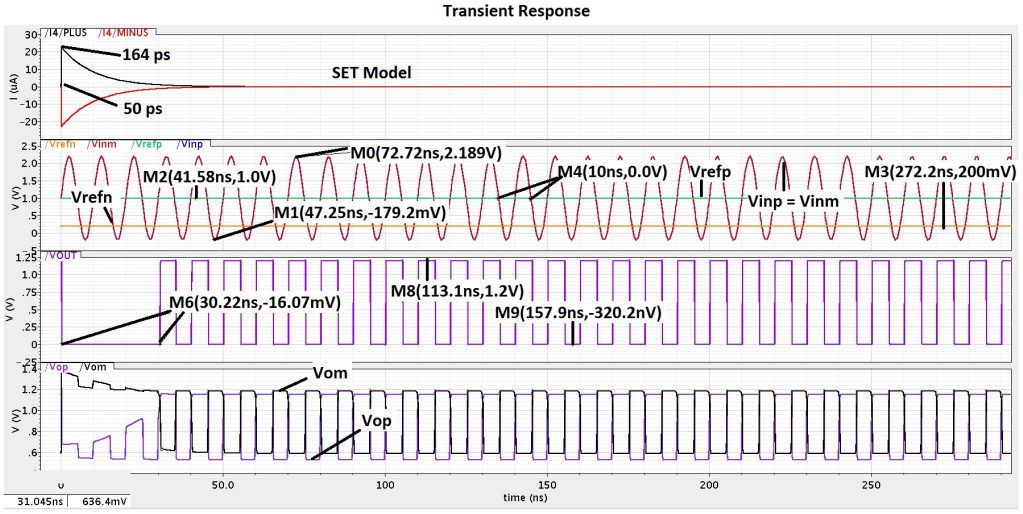


Figure 3.37: Observed output from radiation effect analysis on comparator-with-hysteresis, with input signal frequency of 100 MHz using Wrobel's SET model

3.8 Summary

This chapter reports the circuit-level modelling of SET using the double exponential model based on two different specifications. These models are based on the closest publicly available radiation testing data and by variation method. The hysteresis-free comparator has been injected with Duran's SET model [46] which has longer pulse duration; while comparator-with-hysteresis and 2-stage operational amplifier has been injected with Wrobel's SET model [109] with shorter pulse duration but matches more to the SET pulse widths obtained from the heavy-ion test made to a 90-nm technology device. From using different SET models with different pulse duration, the transient fault under Duran's SET model lasted longer than under Wrobel's SET model. This is very logical as SET pulse with longer duration and the same current amplitude as the SET pulse with shorter duration has higher charges as compared to the pulse with shorter duration, provided everything else remained constant. Even so, it is believed that the duration of the SET pulse injected may not be a major factor in deciding the sensitivity of a circuit to SETs. The critical charge of a device is deemed more important as in the case of high critical charge, a stronger SET injection pulse is required to disturb the operations of a device. The SET injected will not impact much if the device has a high critical charge to overcome and strong stopping power.

From the analyses completed on comparators, the output has been observed to have suffered a temporary short-duration pulse; similar to what has been concluded from work by [28] and [29]. On the other hand, the radiation analysis performed on 2-stage amplifiers showed that the performance of the amplifier worsens under SET injection. The output voltage swing of the 2-stage operational amplifier has been reduced as the SET injected into the amplifier. This definitely does not match the temporary positive or negative-going short-duration disturbance pulses suffered by amplifiers investigated by [17] and [46]. From the observation of the comparators, the failure of each comparator has been defined from the missing bits at every occasion. The 2-stage operational amplifier investigated has been identified as a failure for not being able to amplify the input signals and not by any disturbance pulses.

The sensitivity analysis provided the basis for running the variability analysis in Chapter 4. By identifying the most sensitive node or transistor, the focus may be given in analyzing and mitigating this particular transistor(s), which have been done by Askari et al. [25]. From the sensitivity analysis, not only the most sensitive transistor has been identified, the least sensitive transistor has also been identified to be used in the variability analysis in Chapter 4. Both the most and the least sensitive transistor have been further investigated whether variability to the extreme side will further accentuate the severity of the device to SETs. Not only that from the sensitivity analysis, PMOS has been identified as the device which is more sensitive than NMOS. This is a good information in radiation hardening the devices at fabrication level.

Chapter 4

Variability Analysis of CMOS Comparators

The second objective which has been outlined in Section 1.5, is to investigate whether the selected analogue circuit's sensitivity to SETs will increase due to variability. While the selected circuits being injected with the SET current pulse, design factors have been varied. The variability analysis for hysteresis-free comparator has been investigated using response surface modelling, a statistical tool using the design of experiments. The variability study on comparator-with-hysteresis has been observed on the correlation between design factor(s) and the sensitivity of selected circuit, particularly the two comparators to SETs. At the end of this chapter, a simple mitigation technique has been tested on the comparator-with-hysteresis in Section 4.3.

4.1 Variability Analysis of Hysteresis-free Comparator

4.1.1 Response Surface Methodology In Optimizing No. of Experiments

As described in Section 2.7.2, one needs to carefully select design variables which may have major effects on a given circuit. This, for the hysteresis-free comparator, the selected design variables are transistor's length and width, voltage supply and operating temperature. Following the design steps completed in Section 2.7.1, the design variables are tabled as Table 4.1. In particular, the variability study focused on the 10 % variations of length and width of the transistor, the voltage supply, VDD and operating temperature.

Central Composite has been selected from the two different designs described in Section 2.7.2 and the optimum number of experiments or runs which have been decided are

Table 4.1: Design variable parameters

Factors (Variables)	Max	Base	Min
WIDTH (nm)	108	120	132
LENGTH (nm)	1080	1200	1320
VDD (V)	1.08	1.2	1.32
Temperature (C)	24.3	27	29.7

25, using MiniTab ®, based from the 4 design variable. The variations of input design variables for the 25 runs are as illustrated in Table 4.2. These 25 variations are used for subsequent analysis in Section 4.1.2, Section 4.1.3 and Section 4.1.4.

The variability study has been divided into two sections, with one looked into how variability affected the comparator under no radiation effects as reported in Section 4.1.2 while the other looked into how variability affected the comparator under radiation effects for the most sensitive transistor as described in Section 4.1.3 and the least sensitive transistor in Section 4.1.4.

4.1.2 Modelling and Impact of Variability for Radiation-free Hysteresis-free Comparator

Similar specifications for running the hysteresis-free comparator has been used based on Section 3.2. No SET has been modelled into any of the transistors. In this experiment, the output width of the negative square pulse of the hysteresis-free comparator has been measured, as highlighted in Figure 4.1. The experimental output results in nanoseconds have been recorded in Table 4.3 in the second column. The results from Table 4.3 are analyzed by RSM for its output response in MiniTab ® and produced a response surface regression analysis. The relationship between the tabulated output responses and the design variables are reflected by the coefficients obtained from the polynomial expression from the RSM analysis. The relationship of these experimental results also produces coded coefficients for easier analysis.

The response surface regression analyses output have been fitted into 4 different linear regression fitted line plot, to interpret the individual impact of each design variables. The coefficients in the regression fitted line plot represent the mean change of the output response for 1 unit of change in the design variable while keeping all other design variables constant. From Figure 4.2, it can be seen that the coefficient for length in nanometers is 0.2088. This means that for every additional 1 nanometer in length, the output width is expected to increase by an average of 0.2088 nanoseconds. From Figure 4.3, it shows that for every additional 1 nanometer in width, the output width is expected to increase by an average of 0.0037 nanoseconds. On the other hand, for every additional 1V of VDD, the output width decreases by 251.5 nanoseconds; as in Figure 4.4 and finally, in

Table 4.2: Experimental runs

StdOrder	RunOrder	LENGTH (nm)	WIDTH (nm)	VDD (V)	D (Temp)
21	1	120	600	1.08	27
13	2	108	540	1.32	29.7
22	3	120	600	1.32	27
12	4	132	660	1.08	29.7
15	5	108	660	1.32	29.7
23	6	120	600	1.2	24.3
17	7	108	600	1.2	27
20	8	120	660	1.2	27
19	9	120	540	1.2	27
5	10	108	540	1.32	24.3
25	11	120	600	1.2	27
2	12	132	540	1.08	24.3
24	13	120	600	1.2	29.7
3	14	108	660	1.08	24.3
11	15	108	660	1.08	29.7
6	16	132	540	1.32	24.3
9	17	108	540	1.08	29.7
16	18	132	660	1.32	29.7
18	19	132	600	1.2	27
10	20	132	540	1.08	29.7
1	21	108	540	1.08	24.3
8	22	132	660	1.32	24.3
4	23	132	660	1.08	24.3
7	24	108	660	1.32	24.3
14	25	132	540	1.32	29.7

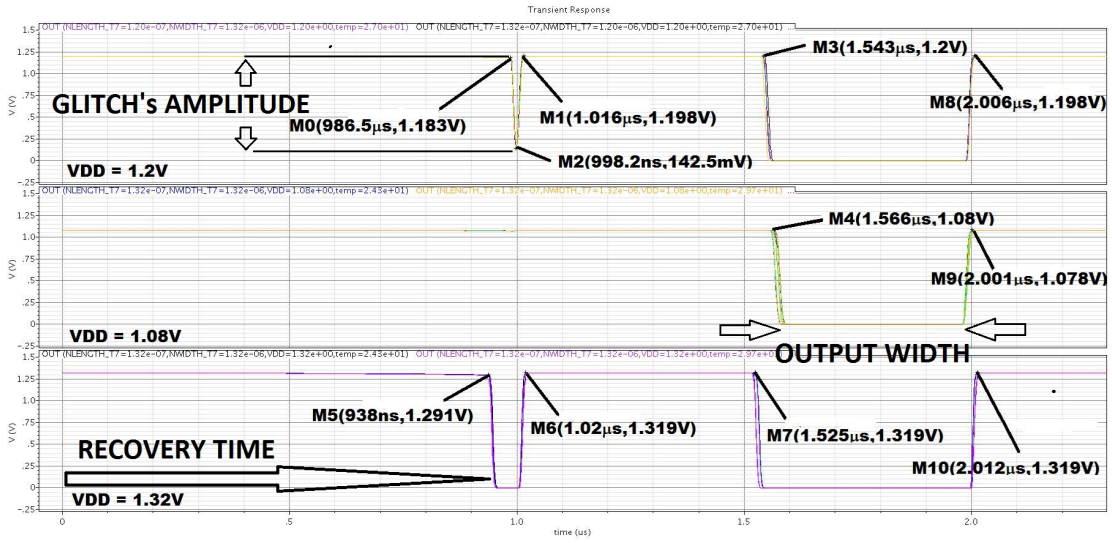


Figure 4.1: The measurement of output responses

Figure 4.5, the output width will decrease by 0.150 nanoseconds for every additional 1 degree in temperature. This suggests that VDD has the most significant impact on the output width, where for decreasing VDD, the output width increases. Temperature and transistor's width have an almost negligible effect on the output width.

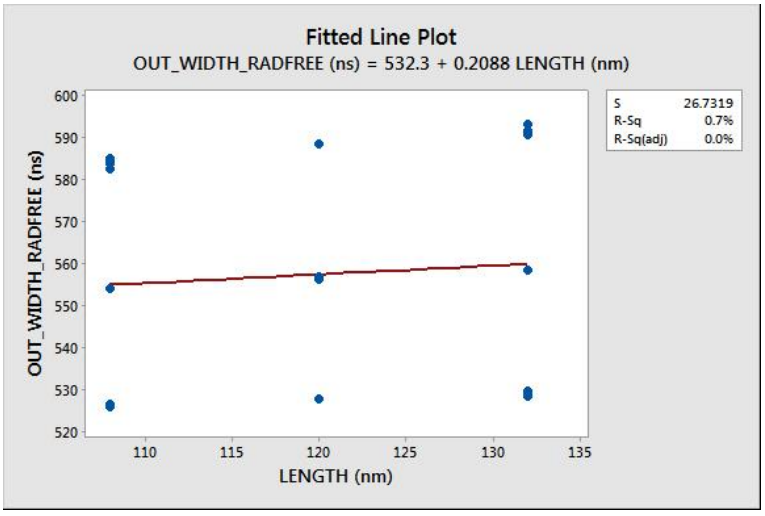


Figure 4.2: Fitted line plot for impact of transistor's length to output width of radiation-free hysteresis-free comparator

4.1.3 Modelling and Impact of Variability on Most Vulnerable Transistor

In this section, an investigation on an irradiated comparator has been completed to address whether variability increases the sensitivity of the comparator to SETs. This experiment has been completed with the same number of runs which have been decided

Table 4.3: Measurement results for variability analysis

RunOrder	OUTPUT_WIDTH_RADFREE (ns)	GLITCH_AMP_SETM3 (ns)	RECOVERYTIME_SETM7 (ns)
1	588.6	101.9	989
2	526	0.9083	871.9
3	527.8	36.23	944.5
4	591.5	74.34	1580
5	526.1	0.1072	858.7
6	556.6	55.23	993.5
7	554.2	22.35	921.7
8	556.9	48.31	989.7
9	556.1	90.54	990.1
10	526.4	0.6564	866.9
11	556.5	66.93	993.5
12	591.1	122.8	1576
13	556.7	67.84	993.9
14	585.2	65.4	974.8
15	582.5	64.18	975.3
16	528.7	69.55	991.3
17	583.8	140	975.3
18	528.3	38.35	970.6
19	558.5	69.92	1548
20	590.6	112	1572
21	584.3	148.7	974.2
22	529.5	37.09	975.5
23	593.2	83.09	1576
24	526.3	0.09739	852
25	528.5	70.94	989.7

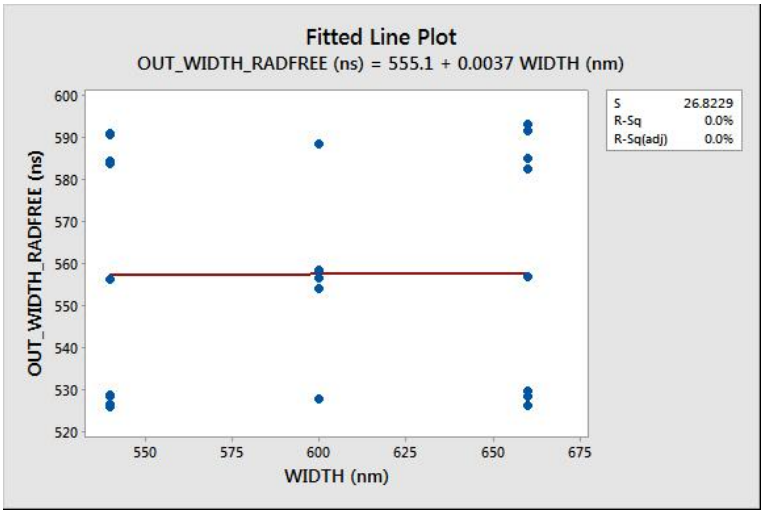


Figure 4.3: Fitted line plot for impact of transistor's width to output width of radiation-free hysteresis-free comparator

in Section 4.1.1 and the variation of design variables as in Table 4.2. In this section, the investigation targeted the most sensitive transistor of the comparator. The selected transistor is one of the transistors which exhibit the maximum voltage variation and recovery time in the previous sensitivity analysis as listed in Table 3.4; M7. In this

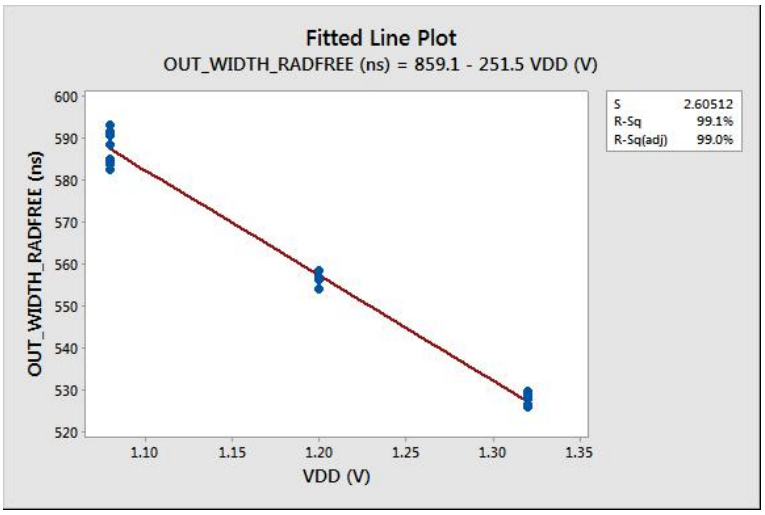


Figure 4.4: Fitted line plot for impact of VDD to output width of radiation-free hysteresis-free comparator

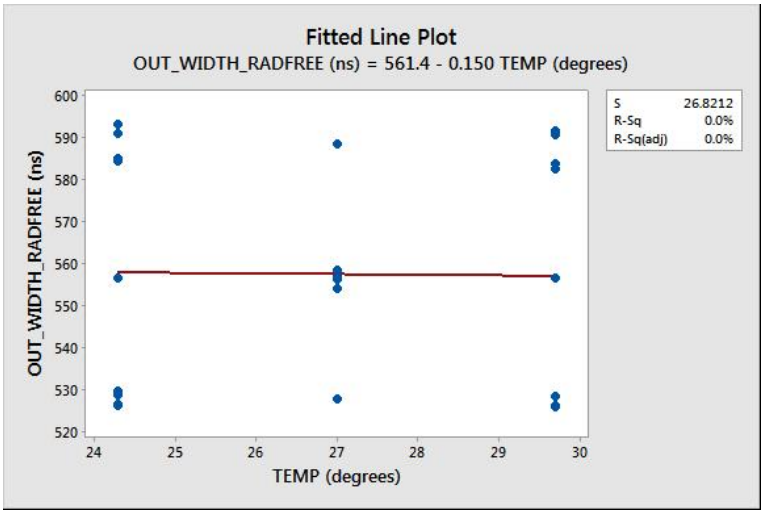


Figure 4.5: Fitted line plot for impact of temperature to output width of radiation-free hysteresis-free comparator

analysis, the recovery time, which is the duration of the comparator output to recover from the impact of SET injection has been observed and recorded in the fourth column of Table 4.3. Note that the recovery time is the time taken for the comparator to return to its normal operation, which differentiates the irradiated circuit from a radiation-free, as highlighted in Figure 4.1. The results have been recorded in nanoseconds. The response surface regression analysis obtained earlier also included the regression model for recovery time for the irradiated transistor, M7.

Similar to previous analysis, the obtained response surface regression analysis have been fitted into 4 different linear regression fitted line plot, to interpret the individual impact of each design variables. From Figure 4.6, for every additional 1 nanometer in length, the recovery time is expected to increase by an average of 16.24 nanoseconds. From

Figure 4.7, it shows that for every additional 1 nanometer in width, the recovery time is expected to decrease by an average of 0.0051 nanoseconds. On the other hand, for every additional 1V of VDD, the output width decreases by 1329 nanoseconds; as in Figure 4.8 and finally, in Figure 4.9, the recovery time will increase by 0.150 nanoseconds for every additional 1 degree in temperature. This again suggests that VDD has the most significant impact on the output width, where for decreasing VDD, the recovery time increases.

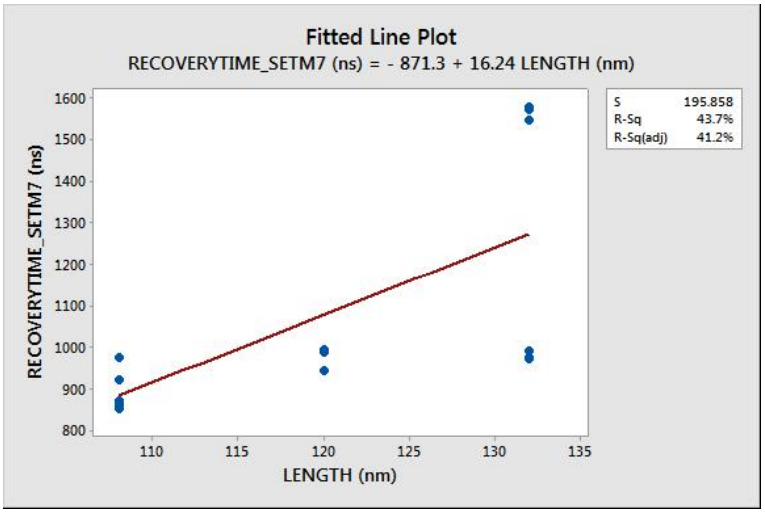


Figure 4.6: Fitted line plot for impact of transistor's length to recovery time for irradiated most sensitive transistor in hysteresis-free comparator

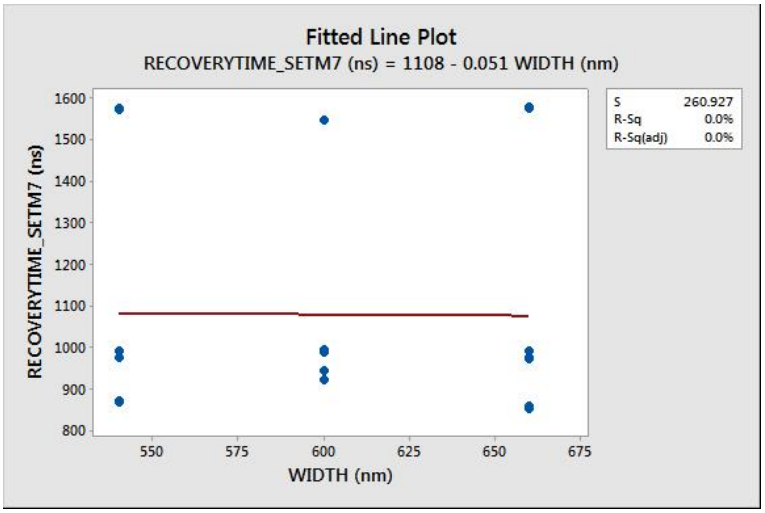


Figure 4.7: Fitted line plot for impact of transistor's width to recovery time for irradiated most sensitive transistor in hysteresis-free comparator

While running the variability analysis on the most sensitive transistor, it has been observed that for VDD = 1.08 V, generally there is no longer any glitch as been observed for VDD = 1.2 V and a wider glitch or shorter recovery time for VDD = 1.32 V; as illustrated in Figure 4.10. This resembles a missing bit for VDD = 1.08V; which has been classified as a failure in a comparator. From this analysis, it has been discovered

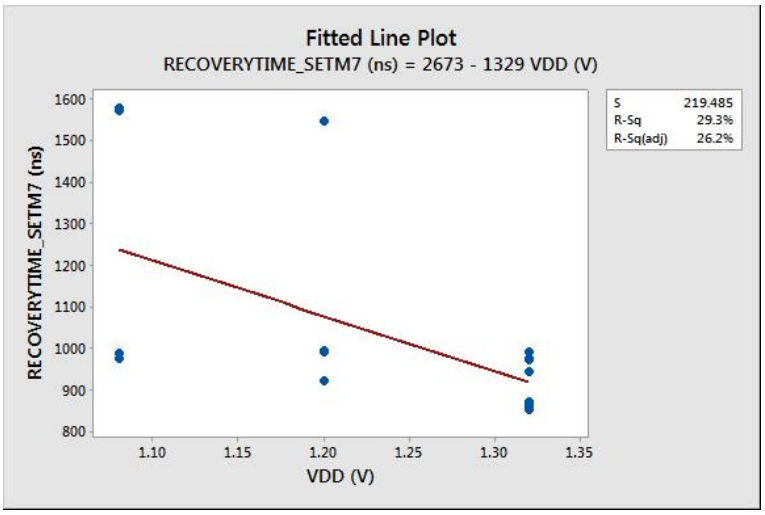


Figure 4.8: Fitted line plot for impact of VDD to recovery time for irradiated most sensitive transistor in hysteresis-free comparator

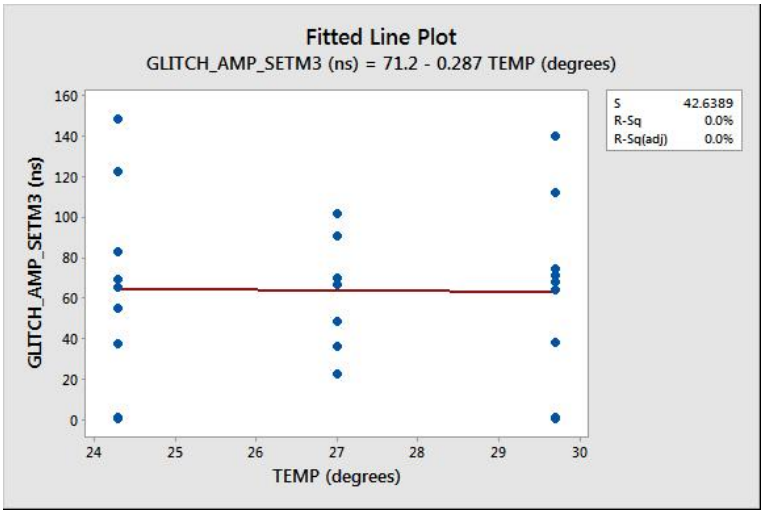


Figure 4.9: Fitted line plot for impact of temperature to recovery time for irradiated most sensitive transistor in hysteresis-free comparator

that the recovery time is more dependent on the transistor's length. The recovery time lengthens as the transistor's length increases.

4.1.4 Modelling and Impact of Variability on Least Vulnerable Transistor

Finally, another variability simulation has been completed for the least sensitive transistor. The selected transistor is one of the transistors which exhibit the minimum voltage variation and recovery time in our previous sensitivity analysis as listed in Table 3.4; M3. In this simulation, the recovery times are all at approximately the same point thus, an additional response is measured to characterize the output. The glitch's amplitude

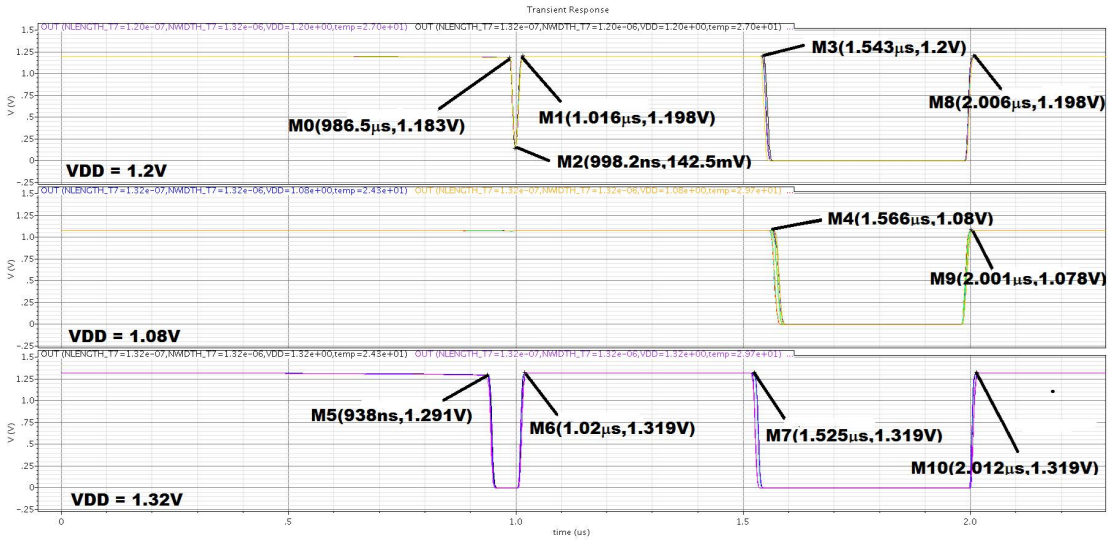


Figure 4.10: Observed output of comparator under variability during SET injection to M7

has been observed at the point highlighted in Figure 4.1 and has been measured and recorded in the third column of Table 4.3.

4 different linear regression fitted line plots have been produced based on the obtained response surface regression analysis to interpret the individual impact of each design variables, similar to previous analysis on radiation-free variability analysis. From Figure 4.11, for every additional 1 nanometer in length, the glitch's amplitude is expected to increase by an average of 1.091 nanoseconds. From Figure 4.12, it shows that for every additional 1 nanometer in width, the glitch's amplitude is expected to decrease by an average of 0.3196 nanoseconds. On the other hand, for every additional 1V of VDD, the glitch's amplitude decreases by 304.9 nanoseconds; as in Figure 4.13 and finally, in Figure 4.14, the glitch's amplitude will decrease by 0.287 nanoseconds for every additional 1 degree in temperature. This again suggests that VDD has the most significant impact on the output width, where for decreasing VDD, the glitch's amplitude increases.

4.2 Impact of Selected Influencing Factors on SET for Irradiated Comparator-with-hysteresis

In this section, selected influencing factors, such as input common mode voltage, positive feedback or hysteresis, ageing and additional capacitances have been investigated on their impact on the sensitivity of the comparator-with-hysteresis. The purpose of the investigation is to find trade-offs of the influencing factors, which may be used in mitigating the SETs in comparator-with-hysteresis. Each individual factor has been investigated against the measurement of the recovery time from the particle strike, SET to the most sensitive transistor, M21.

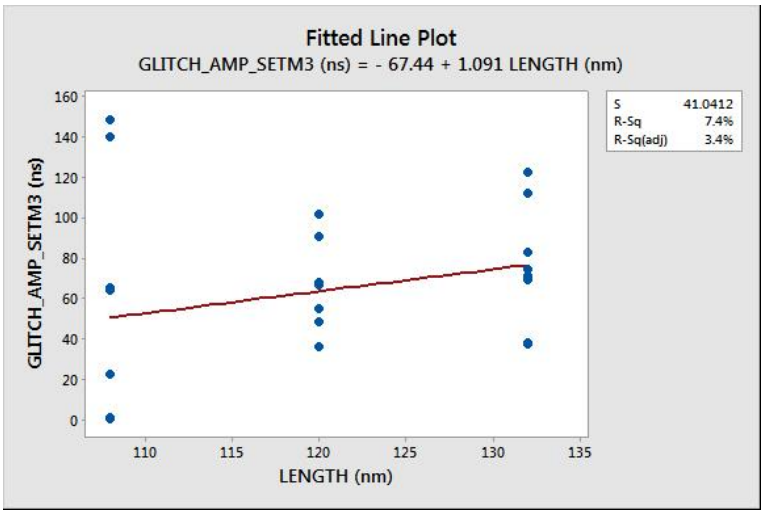


Figure 4.11: Fitted line plot for impact of transistor's length to glitch's amplitude for irradiated least sensitive transistor hysteresis-free comparator

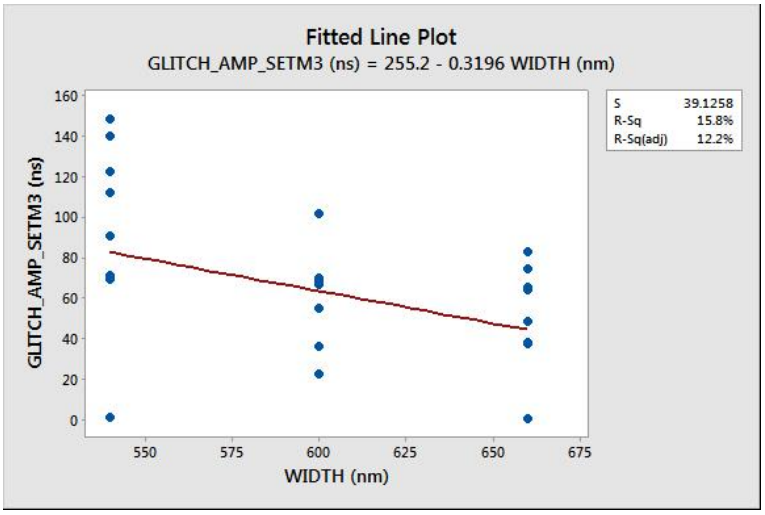


Figure 4.12: Fitted line plot for impact of transistor's width to glitch's amplitude for irradiated least sensitive transistor hysteresis-free comparatorr

4.2.1 Impact of differential input voltage amplitude or common mode voltage

As reviewed in Section 2.6.3.1, [125] has investigated that the severity of SETs in LM111 voltage comparators has been governed by input voltage difference, Δ V or the common mode voltage, V_{CM}. When the common mode voltage is reduced, it has been revealed that SET sensitivity increases. The impact of input common mode voltage to the sensitivity of comparator-with-hysteresis to SETs has been investigated to verify if the same conclusion may be exhibited.

A range of input common mode voltage from 100 mV to 2V has been applied to the inputs of the comparator-with-hysteresis. Input voltage frequency of 10 MHz has been selected,

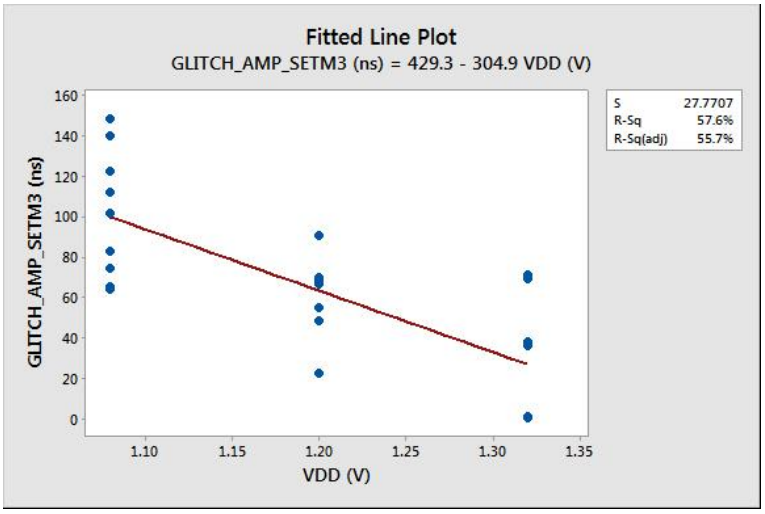


Figure 4.13: Fitted line plot for impact of VDD to glitch's amplitude for irradiated least sensitive transistor hysteresis-free comparator

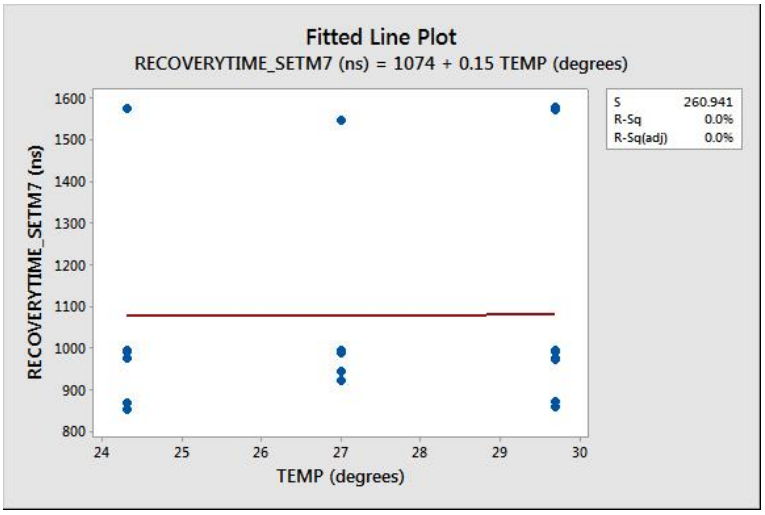


Figure 4.14: Fitted line plot for impact of temperature to glitch's amplitude for irradiated least sensitive transistor hysteresis-free comparator

with VDD = 1.2 V, V_{bias} = 1 V, Vrefp = 1 V and Vrefn = 200 mV and transient time of 100 μ s. The SET model injected to this transistor is similar as being used in Section 3.4. Figure 4.15 relates the differential input amplitude or the common mode voltage to the recovery time. As [125, 19, 53] concluded, for reduced common mode voltage amplitude, a comparator's sensitivity to SETs increases. Investigation performed in the comparator-with-hysteresis in this theses arrives with the same conclusion. To improve the sensitivity of the designed comparator, a minimum common mode voltage shall be determined as long as the operation of the comparator has not been compromised.

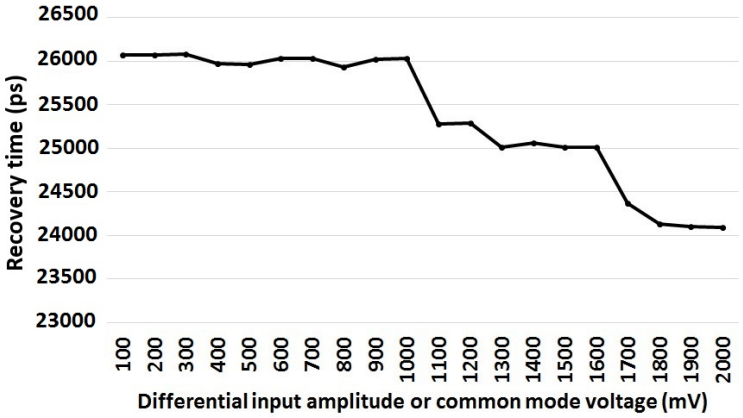


Figure 4.15: The influence of common mode voltage to the sensitivity of comparator-with-hysteresis to SETs

4.2.2 Impact of hysteresis voltage

The very first work which has studied the impact of positive feedback was by [59] and has been reviewed in Section 2.6.3.2. Roche et.al, [59] in 2013 concluded that positive feedback mechanism, in their case an external hysteresis circuit; increases the sensitivity of the COTS comparator used in their investigations. Hysteresis or the positive feedback mechanism is widely used in Schmitt trigger circuit to reduce the noise which exists in a device. It is a normal practice to implement a small hysteresis to any comparator, as the noise may affect the signal which is latched as output. Noise may be mistakenly latched as output if it is strong enough. The impact of a built-in internal hysteresis to the sensitivity of the comparator-with-hysteresis to SETs has been investigated.

In order to enable the hysteresis, Section 3.3.1 has clearly explained the simple mechanism suggested by [76]. In Section 3.3.1, the size of the M16 and M22 transistors are set to the minimum sizing of 120 nm, while M19 and M22 have been varied on its transistor sizing. The variations of the transistor sizes of M19 and M22, which reflected the hysteresis voltage ranges from 0 mV to 200 mV has been represented in Figure 3.19, located in Section 3.3.1. An almost linear relationship between the transistor sizes of M19 and M22 and its hysteresis voltage can be observed from Figure 3.19. The level of hysteresis needed for a particular circuit or application depends on the level of noise to be mitigated in the system. Hysteresis voltage ranging from 8 mV to 56 mV have been applied to the comparator-with-hysteresis, and the experimental result is illustrated in Figure 4.16. The experiment has been performed with input voltage frequency of 25 MHz, VDD = 1.2 V, V_{bias} = 1 V, VCM (differential input amplitude) = 400 mV, Vrefp = 1 V, Vrefn = 200 mV and transient time of 20 μ s. SET model used is similar to the model reported in Section 3.4. The higher the hysteresis voltage is, the more sensitive the device is to SETs.

It is noted that only hysteresis voltage from 8 mV to 56 mV have been investigated because, anything higher has caused the comparator-with-hysteresis to have failed operation. Figure 4.17 illustrated the point of failures for various hysteresis voltages. Although high hysteresis voltage has not been used as recommended by [176]; even by implementing low hysteresis voltage of less than 56 mV to the comparator-with-hysteresis, the influence of hysteresis has shown significant effects to the severity of SETs. The output errors represented in Figure 4.17 is calculated by taking the ratio of recovery time measured to selected sampling frequency. This output error is the number of clock cycles the recovery time should last in the sampling frequency. In this particular figure, the input signal frequency ranges from 1 MHz to 100 MHz. Some improvement on this designed comparator-with-hysteresis must be done if this particular circuit is to be implemented for higher noise immunity.

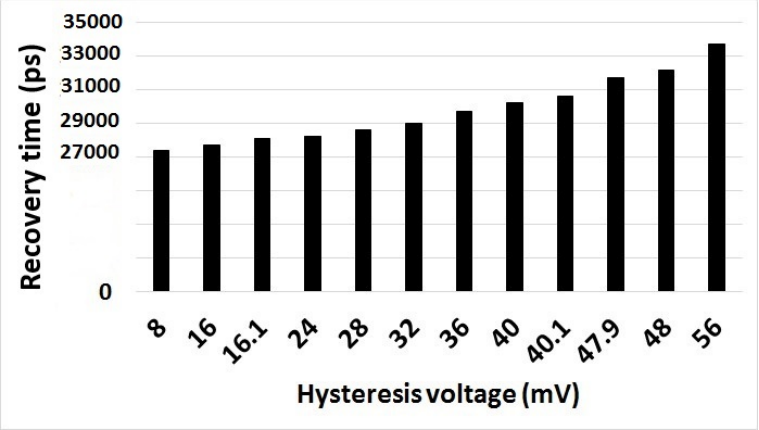


Figure 4.16: The influence of hysteresis voltage to the sensitivity of comparator-with-hysteresis to SETs

An additional investigation has been completed to observe the correlation of differential input voltage or common mode voltage with hysteresis voltage on the sensitivity of the comparator to SETs. Figure 4.18 suggested that the comparator-with-hysteresis under the influence of increased hysteresis voltage and reduced common voltage will suffer from an increased sensitivity to SETs. Roche et.al, [59] has identified that hysteresis worsens the sensitivity of the bipolar comparator and this section extends the investigation with the conclusion that the higher noise immunity required in a system, the higher the vulnerability of SETs in a comparator-with-hysteresis. However, Roche et.al, [59] has observed flip-flop effects at the bipolar comparator's output while in the comparator-with-hysteresis designed in this thesis, a short-duration disturbance pulse has been observed. Thus, trade-offs between reducing the noise suffered by the comparator must also meet the level of sensitivity acceptable for the comparator design.

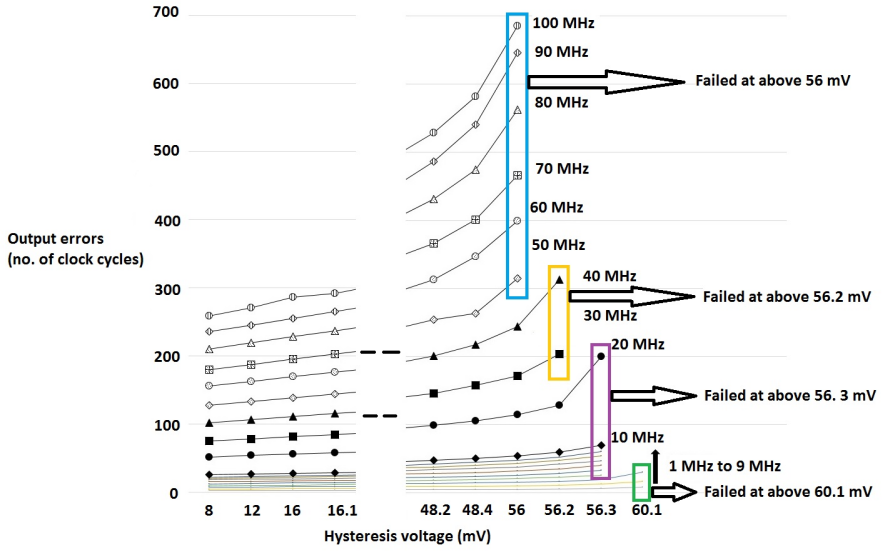


Figure 4.17: Point of failures for various hysteresis voltages at different input voltage frequencies

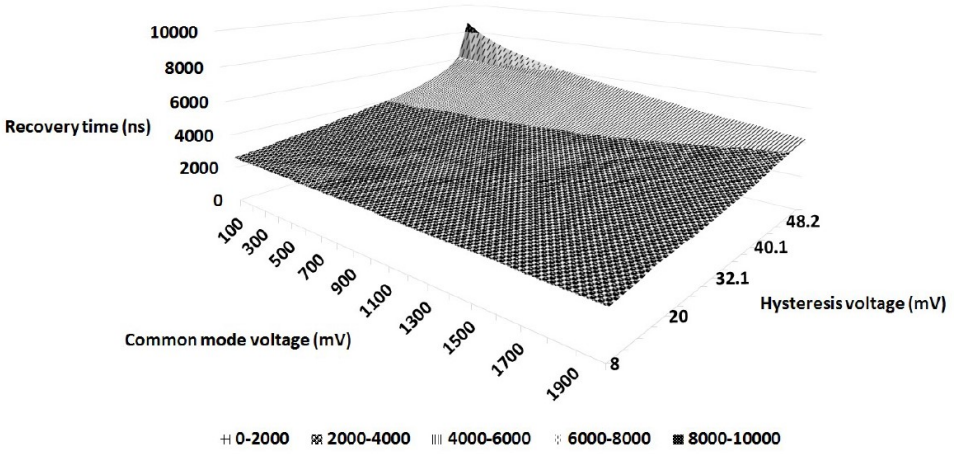


Figure 4.18: Recovery time versus hysteresis voltage for various differential input amplitude or common mode voltage

4.2.3 Impact of NBTI

As described in Section 2.6.4.1, ageing has significant impacts on the effect of SETs; particularly for digital circuits, as reported by [144, 140, 129, 146]. In this section, the comparator-with-hysteresis has been irradiated at its most sensitive transistor, M21 under ageing process. The impact of NBTI on SETs on the comparator-with-hysteresis has been analyzed using the MOSFET Model Reliability Analysis (MOSRA) Tool, which is made available with HSPICE. One of the available MOSFET levels provided in MOSRA has been used in this investigation.

The model covers two-stages of simulation, which are the fresh simulation and post-stress simulation stage [184]. At time = 0 (fresh), the stress of selected MOS transistors is calculated based on the behaviour of the circuit and the HSPICE built-in stress model provided. Meanwhile, the degradation effect is simulated at the post-stress stage is based on the information provided from the fresh stage. The degradation effect in this study has been set to the maximum parameter drift allowed, which is usually specified as a 10% decrement by foundries, [140]. Based on this information, 10% decrement means the saturation drain current of the aged PMOS transistor decreases by 10% when the PMOS is switched on for 10 years. It is assumed all PMOS transistors are under stress.

The experiment has been performed with VDD = 1.2 V, V_{bias} = 0.8 V, VCM (differential input amplitude) = 400 mV, input voltage frequency of 100 MHz, Vrefp = 1 V and Vrefn = 200 mV. Similar to Section 4.2.1 and Section 4.2.2, the SET model uses the model by Wrobel [109], described earlier in Section 3.4. The stress test has been performed by running the MOSRA tool with HSPICE ®. The ageing experiments have been completed under no hysteresis and with hysteresis for observation whether hysteresis and ageing have any correlation. The fresh simulation for Vhyst = 64 mV is shown as in Figure 4.19. The post-stress simulation of time = 1 is as Figure 4.20. The rests of the results together with the fresh simulation are tabulated as in Figure 4.21. Subsequent analysis has been performed under a range of hysteresis voltage, from 8 mV to 64 mV, and the fresh and post-stress simulation results are also included in Figure 4.21. Similar to Figure 4.17, the recovery time measured in the transient responses of the comparator-with-hysteresis has been converted into output errors. From the measurement results, it has been observed that there is no significant impact of NBTI on the SET sensitivity of the comparator for the various hysteresis voltages. These results may have been influenced by the selection of parameter drift of 10% for the stress model, which matches the conclusion by Bagatin [140]. [140], stated that NBTI does not significantly affect the SETs as long as the parametric drift is within 10%.

4.3 Using Capacitance to Mitigate Single Event Transients for Comparator-with-hysteresis

In order to come up with a radiation hardened analogue circuit, this thesis followed the dynamic mitigation flowchart as described in Section 2.2. After identifying the most sensitive parts of the selected analogue circuit, a mitigation technique has been tested on the most sensitive circuit. As suggested by Heijmen et al. [103], including a back-end parasitic capacitance in SRAM cell design, has increased the critical charge measured at that node thus, the device requires more energy to cause an upset from a particle strike. Using capacitors to reduce the charge collected at a particular node has also been used by [39] to improve the robustness of SAR ADC. With this simple idea, capacitors with a small amount of capacitance have been located at the 4 terminals of the most sensitive

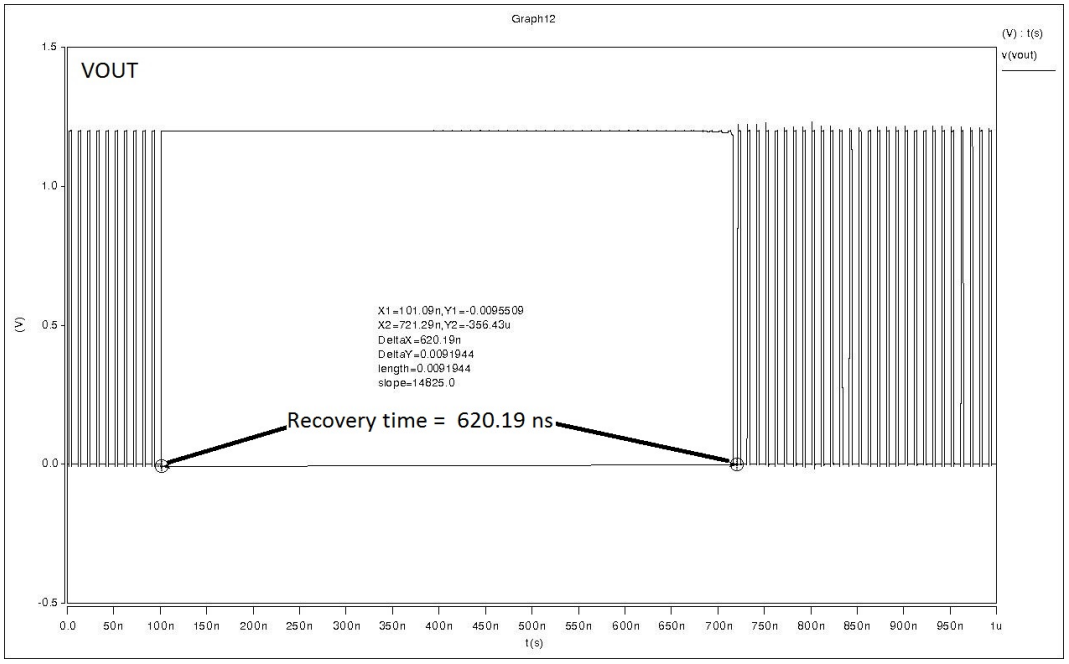


Figure 4.19: Fresh simulation of the comparator's output response with Vhyst = 64 mV, under radiation and under ageing

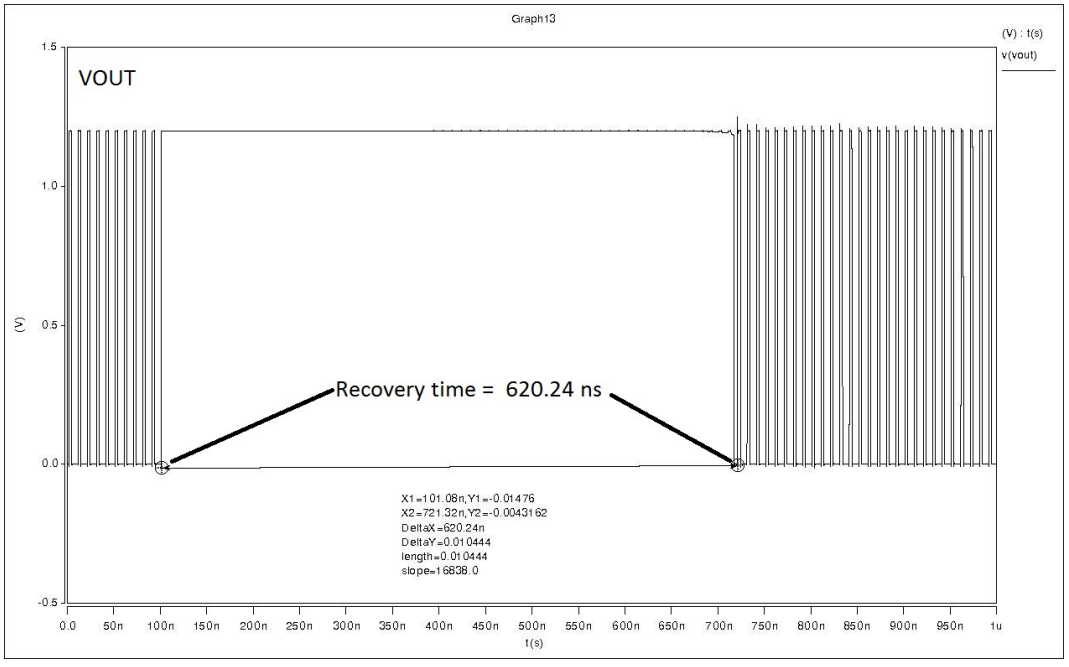


Figure 4.20: Post-stress simulation at time = 1 of the comparator's output response with Vhyst = 64 mV, under radiation and under ageing

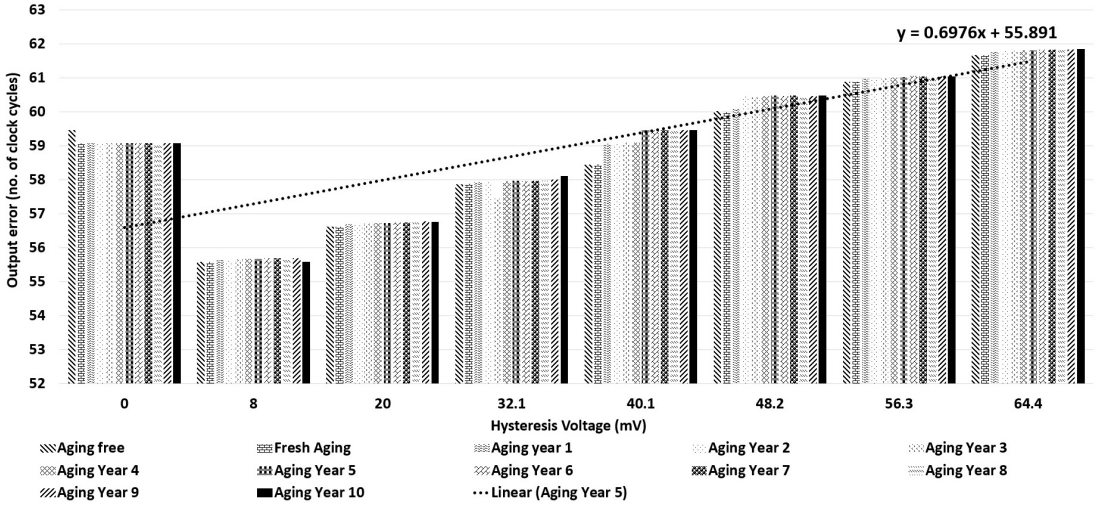


Figure 4.21: Output error versus hysteresis voltage under ageing impact, including ageing-free for freq = 100 MHz

transistor, M21. The similar SET model has been used as described in Section 3.4. Parametric analysis has been performed for all the terminals to determine the optimum capacitance values which reduce the recovery time portrayed by the comparator-with-hysteresis when M21 is struck with SET. The connection of a capacitor to bulk failed to improve the sensitivity of the comparator to SETs, while the connection of a capacitor to drain of the transistor, has successfully reduced the recovery time to zero. Zero recovery time means the comparator seemed to be radiation-tolerated. The particle strike from the SET model may have been discharged through the capacitor. The parametric analysis on obtaining the optimum value of capacitor produced the following results in Figure 4.22. From Figure 4.22, it can be observed that the optimum value of the capacitor is approximately 0.256 pF. This particular capacitor value only valid for the comparator-with-hysteresis designed in this thesis. As the strength of the current differs for different biasing voltages and different charges collected, capacitor values will vary as design changes. Further work shall be performed in providing a reconfigurable capacitive mechanism or an algorithm to decide the optimum value of the capacitor to discharge the current collected from the particle strikes.

As a qualitative comparison, the work completed by [39], uses 200 fF as part of output capacitance at each of pre-amplifier circuits in the SAR ADC designed to mitigate the impact of single event transients. Using 200 fF however only reduces the single event transient pulse's amplitude into half, while placing capacitors valued less than 0.3 pF at the most sensitive point in comparator-with-hysteresis as on this thesis, thoroughly eliminates the effects from single event transients. On the other hand, auto-zeroing

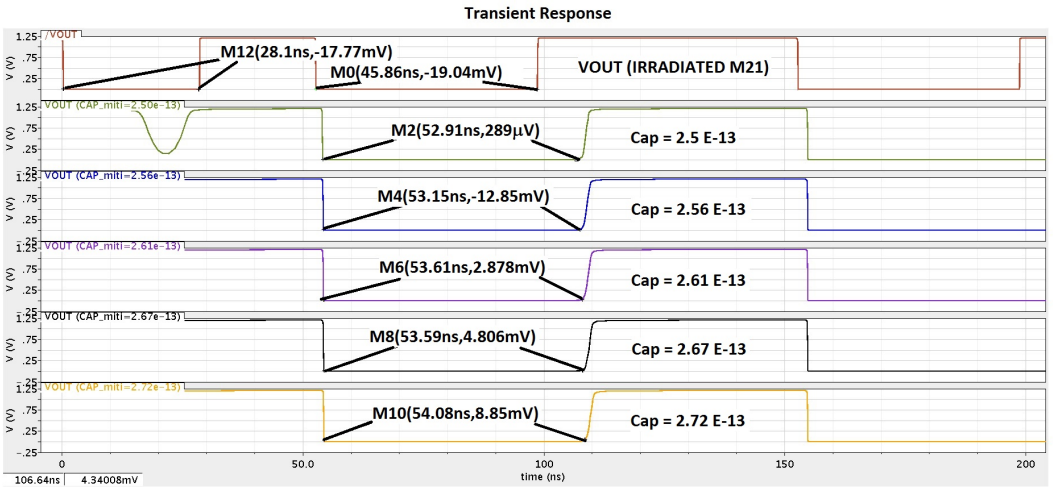


Figure 4.22: Observed outputs responses for different capacitor values

methodology suggested by Tao Wang et al. [29] implemented switched-capacitor circuits at either the input, output or auxiliary stage of the folded cascode comparator. The switched capacitor circuit at the input and output stages uses 2 capacitors and several switches while switched capacitor circuit at the auxiliary stage uses 2 resistors and several switches. Auto-zeroing technique implemented by [29] also required additional circuitry which portrays larger area post-mitigation design stage than suggested mitigation technique for comparator-with-hysteresis in this thesis. The auto-zeroing technique implemented using switched capacitors at these stages however only reduces the impact of single event transient to a duration less than the cancellation period, as compared to placing an optimum valued capacitor at the most sensitive point which thoroughly cancels the impact of single event transients.

4.4 Summary

The design of experiments of the variability analysis on hysteresis-free comparator has been completed with modelling the input variables, namely device's length and width, voltage supply and operating temperature using central composites, a well-known response-surface design. From the optimized number of runs, the experiments have been completed and analyzed using regression plots. From the analyses, it has been concluded that the sensitivity of the hysteresis-free comparator increases due to technology scaling for both the most sensitive and least sensitive transistors. The variability analysis on radiation-free hysteresis-free comparator has been performed as the control scheme; in case no correlation has been observed between the factors and radiation. Voltage supply

has been identified to be the main contributor in increasing the sensitivity of SETs together with the next significant factor which is the device's length. The other two input variables or factors; device's width and operating temperature has the least impact.

The analysis of the impact of single event transients (SETs) on comparator-with-hysteresis has concluded that hysteresis worsens the impact of single event transients on this type of comparator at an almost linear relationship. Meanwhile, for dependence of transients in differential input amplitude, it is worsen for smaller amplitude. This study has proven the needs to mitigate this type of circuit, with considerations on optimized input voltage parameters, especially smaller input voltage amplitudes. To improve the sensitivity of the designed comparator, a minimum differential input voltage shall be determined as long as the operation of the comparator has not been compromised.

The hysteresis voltage has been proven to have an impact in increasing the sensitivity of the device to SETs. The compromise between the SET immunity and noise immunity played a big role in designing a reliable comparator-with-hysteresis in safety-critical applications, thus a point of trade-offs between both noise immunity and the susceptibility of the device to SET shall be investigated under actual physical experimentations. SPICE modelling may not be sufficient to determine the realistic trade-off point for this circuit, as both noise immunity and SET tolerance are important.

The investigation of the impact of NBTI on the SETs on comparator-with-hysteresis has concluded that NBTI has no significant impact on the SET sensitivity. As for the NBTI effects on the comparator-with-hysteresis, the findings will only match devices which are within the maximum parameter drift values. This particular study may only be applicable for devices within standard operating voltages, [140]. Hence, as part of future work, similar analyses shall be extended to be modelled to have parameter drift exceeding 10%, in order to have a better understanding of the relationship between NBTI and SETs. A reliable correlation between hysteresis voltage and SET immunity under NBTI influence shall be obtained hopefully by using more extreme stress model.

The influencing factors which have been investigated; the differential input amplitude, hysteresis voltage, and ageing provides different conclusions towards providing the first step in making the comparator radiation-tolerant. Differential input voltage and hysteresis voltage needs to be designed for trade-offs; as both parameters are equally important in the operation of comparators. The differential input voltage provides the biasing of the comparator while the hysteresis voltage provides noise immunity for comparators. The impact of NBTI on the severity of comparator to SETs has not been concluded, yet. Further investigations must be carried out using better model, which is not available first hand. Finally, by implementing capacitors at transistor's terminal, the temporary short-duration current pulse has been assumed to be fully discharged through the capacitor. If the capacitor can be made reconfigurable, any analogue circuits would be able to

use this simple concept. A reconfigurable system will likely cost more power and time to process. These design trade-offs shall be looked into in designing such mechanism.

Chapter 5

Conclusions and Future Work

As first introduced in Chapter 1, the purpose of this thesis is to address the increasing CMOS reliability issues which have raised due to technology scaling. Similar to digital circuits, analogue circuits have suffered from the tendency to be impacted by single event effects, particularly single event transients. The CMOS reliability has been a great concern especially in safety-critical systems, such as for space applications and has also increased gradually in terms of its reliability study in ground level applications, due to technology scaling. Not only that, with the expectation of super storm to happen; all circuits must be designed to be radiation-tolerant.

5.1 Conclusions

The objectives listed in Section 1.5 have been discussed in this section. The methodology used to reach these objectives has been reported together with obtained conclusions.

5.1.1 Objective 1

The first research objectives or question which needs to be addressed in this thesis is to clarify whether all analogue circuits experiences the same impact from radiation effects, and how SETs affect the comparator's behaviour and eventually causes failure. Three different analogue circuits have been identified from literature reviews and implemented for SET characterization analysis. The 2-stage operational amplifier has been selected, with a hope that it can be compared with previous studies. The comparators implemented for this thesis on the other hand has been aimed to be used in memory mechanism or in a charge-redistribution architecture, as justified in Section 2.3.3. The 2-stage operational amplifier and comparator-with-hysteresis have been implemented with 65-nm CMOS technology while the hysteresis-free comparator has been implemented with

120-nm CMOS technology. The initial designs of the amplifier and comparators have been reported in Chapter 2. Both the 2-stage operational amplifier and hysteresis-free comparator runs at slower input signal frequency while the comparator-with-hysteresis runs at faster input signal frequency.

After identifying the selected topology for the analogue circuits based on articles reviewed in Chapter 2 and implementing these circuits, the modelling technique of the radiation effects on these circuits must be identified. With the limitation on the actual radiation data for the selected circuit, the modelling of radiation effects on these circuits has been completed with circuit-level simulations. The single event transient has been modeled with a double-exponential model, normally used to represent the SET modelled in digital circuits. Two different SET model parameters based on work completed by [46] and [114] have been used in the characterization of the operational amplifier and comparators, as clarified in Chapter 3. Preliminary characterizations using double exponential SET model have been completed for the three circuits.

In previously completed work, 2-stage operational amplifier has been identified to be susceptible to single event transients by experiencing a short-duration disturbance pulse at its output voltage however; in this thesis, it has been observed that the performance of designed 2-stage amplifier has been affected by the reduction of output voltage swing from V range to mV range, as reported in Chapter 3. This definitely does not match with the previous work completed on amplifiers which experience temporary short disturbance pulses at the output by [17] and [46]. The reduced output voltage swing suffered by the 2-stage operational amplifiers reduces the output gain portrayed by the amplifier. As 2-stage operational amplifier has not been identified to have the non-permanent short-duration disturbance pulses which may be captured if propagated to digital circuits; the only thing left to do is to redesign the amplifier with higher gain; in order to contain the impact of SET. On the contrary, the comparators investigated in this thesis has been observed to have suffered temporary short-duration pulses at its output and matched with the findings from [28] and [29]. The only difference between the two comparators is the duration of the recovery time. The hysteresis-free comparator has been injected with a longer current pulse duration which is 10 ns and the recovery time lasted more than hundreds of nanoseconds while the comparator-with-hysteresis used a short pulse duration of about 100 ps and the recovery time observed only lasted for an average of 20 ns. The differences between the recovery time exhibited by these comparators may be caused by several factors, such as the different topology, bandwidth, or the SET model pulse duration. Even for a single comparator, there are many design factors which may have affected the SET recovery time. Having 2 different comparator circuits may increase the number of design factors responsible for the sensitivity of the circuits to SETs. Using statistical tools to obtain a correlation between these factors and the sensitivity of the circuits to SETs is considered a good step in the near future, in figuring out the trade-offs to be used as mitigation techniques for analogue circuits. However,

in the meantime, a strong conclusion has been achieved. The implemented comparators have been identified to experience sensitivity to single event transients and required mitigations while the 2-stage operational amplifier although affected by SETs, should be redesigned for higher gain to overcome the impact of SETs.

5.1.2 Objective 2

The second research objective for this thesis is to investigate whether the analogue circuits selected worsen under variability. From Chapter 2, it is found that both analogue and digital circuits suffered from increased sensitivity due to several influencing factors, which have led this work to investigate selected factors on the comparators implemented in this thesis. The investigations on the variability of these factors and its impact on the sensitivity of the device to SETs have been completed using the statistical tool, DOE; particularly for hysteresis-free comparator while individual factors have been investigated on its impact to the sensitivity of the comparator-with-hysteresis in Chapter 4. The 2-stage operational amplifier has not been investigated for its variability as influencing factors such as scaling may worsen the output voltage swing reduction; which is already really low. The 2-stage operational amplifier shall be redesigned to have higher gain before being tested again. Perhaps a 2-stage operational amplifier with a very high gain may not be affected by SETs.

The factors investigated for hysteresis-free comparator are the transistor's length and width, voltage supply and operating temperature; while for comparator-with-hysteresis; the factors investigated are differential input voltage, hysteresis voltage, and ageing. Before conducting the variability study on the selected design factors; the sensitivity analysis has been completed to identify the most and the least sensitive transistors for each comparator circuits. The most sensitive transistor(s) for both comparators belongs to the pre-amplifier sub-circuit while the least sensitive transistor varies.

DOE statistical tool has been used to determine the optimum number of experimental runs required for statistical analysis. The hysteresis-free comparator is once again characterized under SET injections at the most and the least sensitive transistors. Once the experimental runs are completed, the results are tabulated and analyzed using response surface modelling, which finds out the correlations between the design factors and the sensitivity of the hysteresis-free comparator to SETs. As the feature size further decreases, the variability investigation of the hysteresis-free comparator in Chapter 4 has concluded that SET has worsened due to technology scaling for both most sensitive and least sensitive transistors. The most significant factor in contributing to the sensitivity of SETs is the voltage supply. The next significant factor is the device's length. Both width and operating temperature have the least impact on the sensitivity of the hysteresis-free comparator. On top of that, variability analyses for radiation-free hysteresis-free comparator have been completed as the control scheme, in case the investigation on the

correlations between the design factors and the output did not provide any conclusive results.

For the hysteresis-free comparator, the SET has been injected to the most and the least sensitive transistor. For comparator-with-hysteresis, the variability study is conducted by injecting SET current pulse to the most sensitive transistor only. For comparator-with-hysteresis, the factors which have been considered in the variability studies are the hysteresis voltage, differential input voltage and ageing. Hysteresis is used to increase the noise immunity of a device, but from the analysis completed; hysteresis has been identified to worsen the impact of SET to a device when further increased. The need for higher noise immunity may have increased the sensitivity of a device to SETs. In designing this type of comparator, a balance between required noise immunity and minimized SET recovery time shall be obtained. In the analysis of the impact of the differential input voltage to the sensitivity of the comparator-with-hysteresis, smaller differential input voltage increases the sensitivity of the comparator-with-hysteresis to SETs. The comparator shall be designed to be able to accept a large differential input voltage, as the more differential input voltage the comparator has, the less sensitive the comparator is to SETs. As for ageing, its impact on the severity of SETs to the comparator has not reached any conclusion, thus it is best to leave it there until a proper ageing model is obtained.

Both the comparators are impacted by the influencing factors either positively or negatively, however running the experiments using better SET modelling may have increased the confidence in the correlations between the influencing factors and the sensitivity of the circuits to SETs. The hysteresis-free comparator can be investigated for its correlation to the hysteresis voltage, differential input voltage and ageing similar with comparator-with-hysteresis and vice versa where comparator-with-hysteresis can be investigated for its correlation to the transistor's width and length, voltage supply and operating temperature. However, the correlations between design factors may have been more reliable if the SET has been modelled using at least 3D-TCAD modelling.

5.1.3 Objective 3

The final objective of this thesis is to suggest simple mitigation technique be implemented in the circuits which have been identified to be sensitive to single event transients and could cause malfunctions to its digital counterparts. The short disturbance pulses observed from both comparators will only be visible as an error when it is propagated to its digital counterparts. As mentioned earlier, the comparators implemented for memory mechanism or as part of a charge redistribution architecture, will have higher potential to cause mistaken bits at its digital counterparts and its overall systems. The variability analysis studying the correlations between the design factors and its output created a venue to understand the trade-offs which have occurred during the analysis. Trade-offs

between the factors and SET sensitivity as discussed earlier may be used in mitigating the single event transients. For occasions which trade-offs can no longer contain the sensitivity of a device to SETs, error correction circuit shall be implemented. By studying the existing error correction technique used for mitigating SETs in analogue circuits such as auto-zeroing, analogue checksum and the impact of back-end capacitances by [103], a simple mitigation technique has been suggested for comparator-with-hysteresis.

The comparator-with-hysteresis has been tested on its impact of SETs under the influence of a capacitor linked to the 4 terminals of the most sensitive transistor, one at a time. By including a capacitor to the drain of the transistor, it has been assumed that by the disappearance of the short-duration disturbance pulse previously observed, the charge collected from the particle strike has been fully discharged through the capacitor. The optimum capacitor value which has successfully mitigate this particular pulse for the designed comparator-with-hysteresis has been obtained from running parametric analysis. As mentioned earlier in Chapter 4, the captured short-duration disturbance pulses will differ based on the several factors; the capacitor value obtained from the parametric analysis is only for this particular comparator-with-hysteresis with the same specifications. If only the capacitor can be made reconfigurable and switched-on when the SET has been detected, this simple idea may have been great solution for a low-cost mitigation of SETs in analogue circuits. Auto-zeroing resembles this simple concept by using a sampling technique to reset the disturbing pulses. However, in the completed mitigation techniques on comparators by [28] and [29], the duration of the disturbing pulse has only been reduced to one clock cycle for a 100 MHz clock frequency. If these comparators by [28] and [29] are used in a system with a higher clock frequency, say GHz; the disturbance pulses may have lasted more than one clock cycle and eventually created multi-cycle of errors. Thus, as the simple technique to include a capacitor at the drain of a transistor under irradiation has shown the total disappearance of the short-duration disturbance pulse; it may be used in developing a mechanism to mitigate the circuit in larger scale.

5.2 Description of Publications

Parts of this thesis have been published in several workshop and conferences, as listed in Section 1.8. The following describes the content of each of the publications.

5.2.1 Reliability Analysis of Comparators

The paper "Reliability Analysis of Comparators" firstly has been presented in "Designing with Uncertainty: Opportunities and Challenges" workshop running simultaneously with DATE 2015 in Grenoble, France. This paper later has been published in IEEE, after being presented again in PRIME 2015 in Glasgow, Scotland.

"Reliability Analysis of Comparators" reported the first and second objectives of this work, particularly on hysteresis-free comparator implemented on 120-nm CMOS technology as in Section 3.2, Section 3.2.2 and Section 3.2.3 .

5.2.2 Ageing Impact on a High Speed Voltage Comparator

"Ageing Impact on a High Speed Voltage Comparator" on the other hand reported the impact of ageing, particularly NBTI on the sensitivity of both hysteresis-free comparator and comparator-with-hysteresis implemented on 65-nm CMOS technology, as described in Section 4.2.3. This paper has been presented at the Workshop on Early Reliability Modelling for Ageing and Variability in Silicon Systems (ERMAVSS), running with DATE 2016 in Dresden, Germany.

5.2.3 The Influence of Hysteresis Voltage on Single Event Transients in a 65 nm CMOS High Speed Comparators

"The Influence of Hysteresis Voltage on Single Event Transients in a 65 nm CMOS High Speed Comparators", has been published in IEEE based on the presented content at the IEEE European Test Symposium in Amsterdam, The Netherlands. This particular paper reported the influence of hysteresis voltage on the sensitivity of implemented comparator-with-hysteresis, as described in Section 4.2.2.

5.3 Potential Journal Publication

This thesis can be extended into a journal provided an extension of discussion and additional experiments on mitigation technique proposed has been included as part of the journal. This thesis rewritten in a journal format may be suitable under topics of methodologies in mitigating analogue and mixed signal circuits. As outlined in Section 2.2, this thesis follows a dynamic mitigation flowchart in arriving with the suggested mitigation method for reducing the sensitivity of the comparator to single event transients. The outline of a journal structure of this thesis may be as follows.

- Section 1 Introduction (Taken from Chapter 1 of this thesis.)
- Section 2 Background (Taken from Chapter 2 of this thesis.)
- Section 3 Selection of Analogue Circuit of Interest (Additional section which outlines on selection of analogue circuits, together with possible design and applicable systems.)

- Section 4 Design of Selected Analogue Circuit (Taken from a part of Chapter 3 of this thesis, with extension of possible applicable systems.)
- Section 5 Modelling of Single Event Transients (Reorganizing a part of Chapter 3 of this thesis, to focus on selection of single event transient modelling based on available data and justification on the selection of model.)
- Section 6 Characterizations of Single Event Transient Effects on Selected Analogue Circuits (Taken from a part of Chapter 3, focusing on characterization of single event transient effects,identifying the most and least sensitive nodes or parts of the circuit and discussion of the outcome from the experiments while relating to existing related work.)
- Section 7 Study of Variability on Single Event Transient Effects on Selected Analogue Circuits (Taken from Chapter 4, focusing on several selected influencing factors, and may be extended for other factors as well. A discussion on impact of these influencing factors may also be included.)
- Section 8 Conclusion (Summarizing the motivation behind this work, objectives achieved, selection of analogue circuits to be investigated, single event transient model used, characterization experiments outcome and impact of influencing factors on the severity of single event transient effects on selected analogue circuits.)

5.4 Limitations

Before concluding this thesis, few limitations on this research have been discussed. In common practice, a device needs to be characterized using physical experimentations or radiation testing. Due to such limitation of access to radiation testing data, the SET in this thesis has been modelled using simple circuit-level double-exponential model, which may cause the findings from this thesis to be unrealistic for further mitigation investigations. The parameters used in this SET model has been based on two different approaches. The first model used for characterization of the hysteresis-free comparator has been based on modelling the expected particle strikes by varying the current pulses [46]. With the uncertainty caused by the increasing smaller-scale solar storm and too many variations from the actual radiation data, the particle strike representing the SET could be modelled in a wide range of parameters.

The second model is based on assumptions that only one of the parameter in the double exponential model needs to be known, to obtain the realistic value for the SET model [109]. The second model used the radiation data of 90-nm device assumed to have the closest resemblance to the 65-nm device. As a comparison, both models are run using the same pulse amplitude but with different pulse duration. The longer SET pulse portrayed by the first model produces a longer disturbance pulses as compared

to the second model which uses shorter pulse duration. The other limitation of the analogue electronic circuits implemented in this thesis was all of it has been designed parasitics-free.

These limitations even if resolved, may only cause the observation from the characterization of these circuits change in terms of SET level sensitiveness. These circuits have already been identified to be susceptible to SET in all cases. The only difference will be in how the influencing factors will affect the level of sensitiveness of these devices to SETs. Even so, if these devices are designed under parasitics influences; the impact of SET may worsen as per reported in Section 2.6 which marks the same conclusion that the device will still need to be mitigated from the impact of SETs. Modelling the characterization of SETs based on actual radiation data, on the other hand, may have improved the level of confidence in the study of correlation of influencing factors in deciding the trade-off points in mitigating the impact of SETs.

5.5 Scalability of the Dynamic Mitigation Flowchart used throughout the thesis

Although with the limitations which have been outlined in Section 5.4, this thesis did follow a systematic dynamic mitigation flowchart. As described in Section 2.2, a dynamic mitigation flowchart has been summarized which represents the steps used in analyzing, characterizing and mitigating analogue circuits such as comparators and operational amplifiers. This mitigation flowchart has been followed closely for both comparators. However, for operational amplifier implemented in this thesis, mitigation has not been performed as the operational amplifier's reaction toward SET differs from completed work by Koga et al. [17] and Duran et al. [46]. The operational amplifier in this thesis is only been affected on its performances i.e. reduced voltage swing. Such characteristic may be easily mitigated using existing analogue design tools. The dynamic mitigation flowchart now can be easily applied to other analogue circuits in achieving radiation hardened circuits. As previously described in Section 2.2, several automation tools have been developed in characterizing soft errors. The dynamic mitigation flowchart summarized in Section 2.2 can be implemented into characterization tool similar to the reported tools.

5.6 Future Works

5.6.1 Using Actual Radiation Data for 120-nm and 65-nm CMOS Devices

As part of future work, it is recommended to extend this study using actual radiation data for a realistic SET modelling in characterizing the dependencies of SET sensitivity on the influencing factors. At least some completed radiation testing data for both 120-nm and 65-nm technology devices shall be obtained to run a 3D-TCAD device modelling simulation. A mixed-mode simulation of a 3D-TCAD device simulation with SPICE-level circuit simulation is much better than running SPICE simulation alone in characterizing both analogue and digital circuits. With access to actual radiation data or the closest radiation data; the correlation investigations hopefully shall achieve better confidence level.

5.6.2 Extending The Correlation Investigations for Other Design Factors

The correlation study shall be extended to include all possible design factors or design variables. Design factors which have been investigated are differential input voltage amplitude, hysteresis voltage, transistor's width and length, operating temperature, voltage supply, and ageing. Other identified design factors are polarity, the particle's criterion such as doping or ionization dose (total ionizing dose), carrier lifetimes, the energy and LET of the radiation particle, altitude, speed of the fault injection, load resistors, feedback resistors, or spatial faults such as the RDF (relative dose factor). As mentioned in Section 2.6, several variables stated can be modelled at circuit-level but some can only be modelled using physical characterization. Further investigations shall be completed in finding out if these variables which are normally investigated at physical characterization can actually be modelled at circuit-level. As stated in Section 5.6.1, with access to actual radiation data or the closest radiation data; the correlation investigations may be extended and produce better correlations or relationships to be used as a basis in implementing the trade-offs for mitigating purposes.

5.6.3 Extending The Impact of Ageing On Sensitivity of Circuits to SETs

In addition to this, as the completed ageing analysis on the device under radiation effects has not been able to reach any conclusion; it is good to extend the ageing study using better ageing model, that has parameter drifts exceeding 10%. The circuits shall also be tested under radiation-free environment. It has slipped from the simulation to-do

list to include a control scheme for comparison; to make sure that the ageing model implemented is usable. As there was no work which has been completed on studying the impact of ageing on single event transients which occurred in analogue circuits apart from what this thesis has completed, this work may be a good starting ground.

5.6.4 Extending The Preliminary Mitigation Technique using Capacitors Connected to Transistor Terminals

Another recommendation is to rerun the preliminary mitigation technique using capacitors to the drain of transistors under a better SET modelling; which is again to have access to actual or the closest radiation data available. Further investigations on how to make capacitor reconfigurable or at least being able to be switched on automatically when a particle strike has been detected shall also be looked into. An interesting work is by [185] which have introduced a configurable analogue transistor. The configurable transistor has been proposed to maximise the post-fabrication yield. The configurable analogue transistor uses switching techniques to negotiate the required number of transistors for specific performance. Some algorithm needs to be further investigated to understand whether this same concept may be used to make the capacitors reconfigurable. The other concept which may be used will be node-splitting [186], which divides the total component values into several critical paths. When in radiation-free environment, all the circuit path are working but when a particle strike has occurred, the path which has been affected was disabled and the other paths run as it should be. Another work by [29] and [28] which may be used in implementing switching the capacitor when it is required, focus on sampling techniques. The unwanted pulse is sampled during the sampling phase and during signal processing technique, an offset-free environment is made available for correct operation. One important issue though which have not been understood yet is how the circuit proposed identifies the offset or particle strikes when it occurs. There may be some built-in current sensor in their work which is implemented to detect the disturbance pulse.

5.6.5 Redesigning The Comparators under Parasitics Considerations

Finally, the comparators shall be redesign to consider the parasitics. It might be possible that parasitics may not give any changes or just worsens the impact of SET to these comparators. If parasitics improve the sensitivity of these circuits to SETs, then one more trade-off may be used in designing analogue circuits.

Appendix A

Hysteresis-free Comparator Analysis

These are the tools which have been used for the circuits' implementations.

1. CADENCE Virtuoso Schematics (Transistor-level architecture)
2. CADENCE Analogue Design Environment (Circuit simulations)
3. Design Kit IC6141 IBM8RF (130-nm)

To make sure that the comparator designed is within the specification range; various analysis shall be performed such as DC, AC and transient analysis. Input signals for the comparator, V_p is a sinusoidal signal of 1.2 V amplitude and 1 MHz frequency while V_m is a DC voltage of 1.0 V, which represents 5/6 of VDD. IBIAS is selected as $40\mu A$.

A DC analysis provides the offset voltage and the gain of the comparator. A DC response also allows the investigation of application of hysteresis in a particular comparator, which has been used in Appendix B. As mentioned earlier, in an unmatched differential pair i.e. practical application, hysteresis is often applied in a noisy environment or in a condition where comparator is undesirable to toggle continuously between states [187].

The offset voltage of the comparator can be obtained from taking a DC response from applying a DC input of 600 mV (half of VDD) to V_m while V_p is swept between 0.5 to 0.7 V, with a step size of 4 mV. The DC response waveform for obtaining the offset voltage is as Figure A1. It can be seen clearly that the offset voltage for the comparator designed is approximately 20 mV. The voltage obtained is a systematic offset voltage.

The transfer curve waveform of Figure A1 is taken its derivative to represent the comparator gain and consequently, the resolution of the comparator can be known as well. Figure A2 represents the derivative of the waveform in Figure A1, which shows the

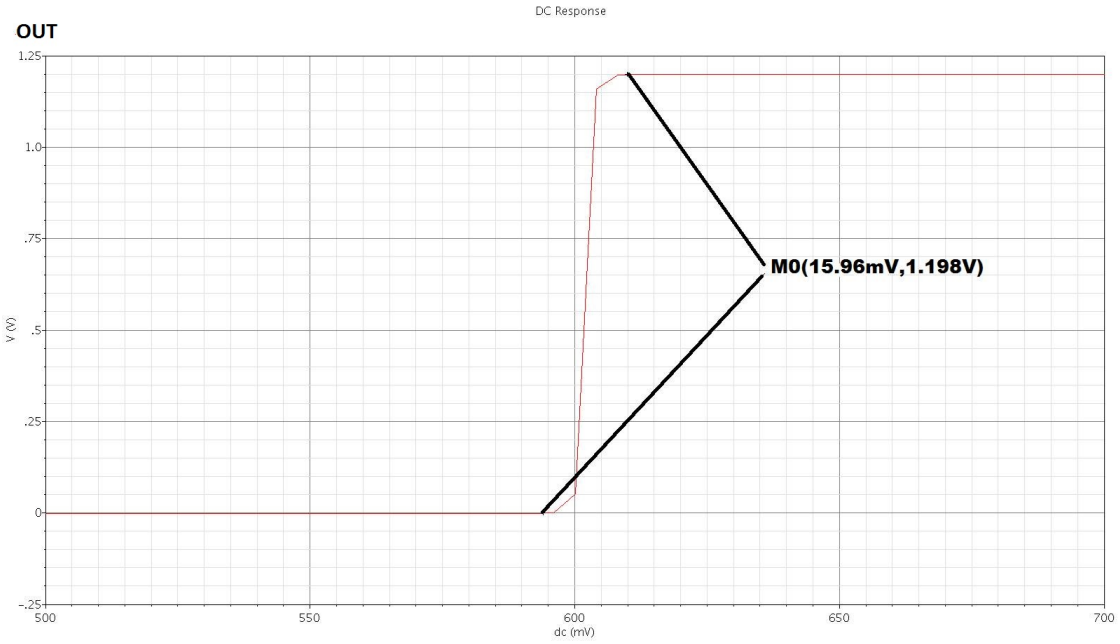


Figure A1: DC response to obtain input offset voltage for hysteresis-free comparator

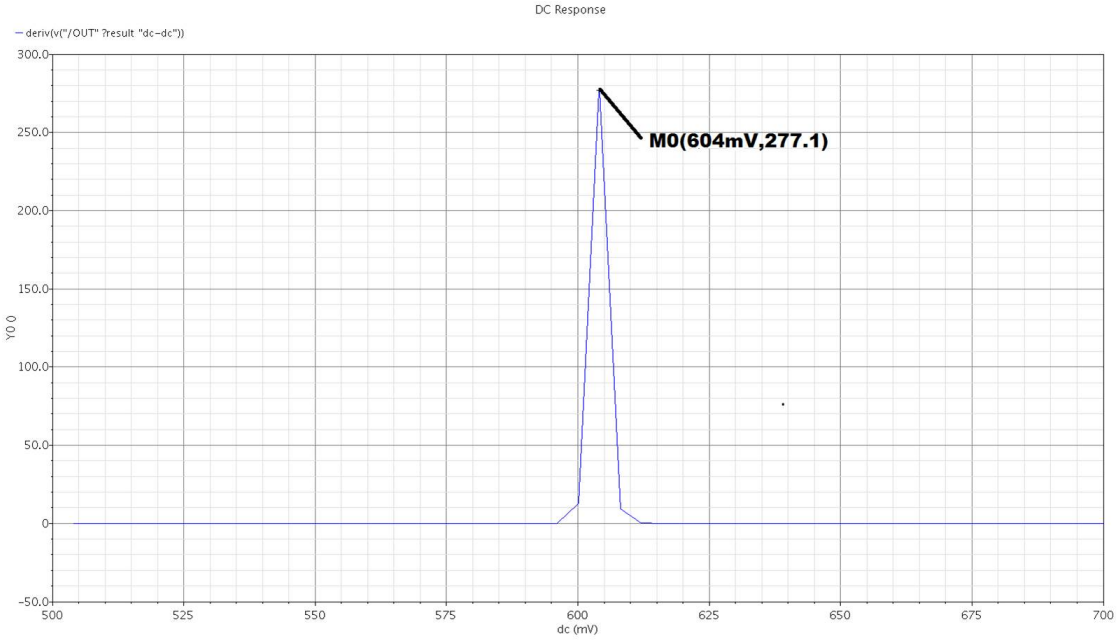


Figure A2: The derivatives of the DC response to obtain voltage gain for hysteresis-free comparator

voltage gain of the comparator. Figure A3 represents its decibel equivalence of a 9-bit comparator.

The AC response for hysteresis-free comparator as illustrated in Figure A4, highlighting the AC gain as 52.16 dB.

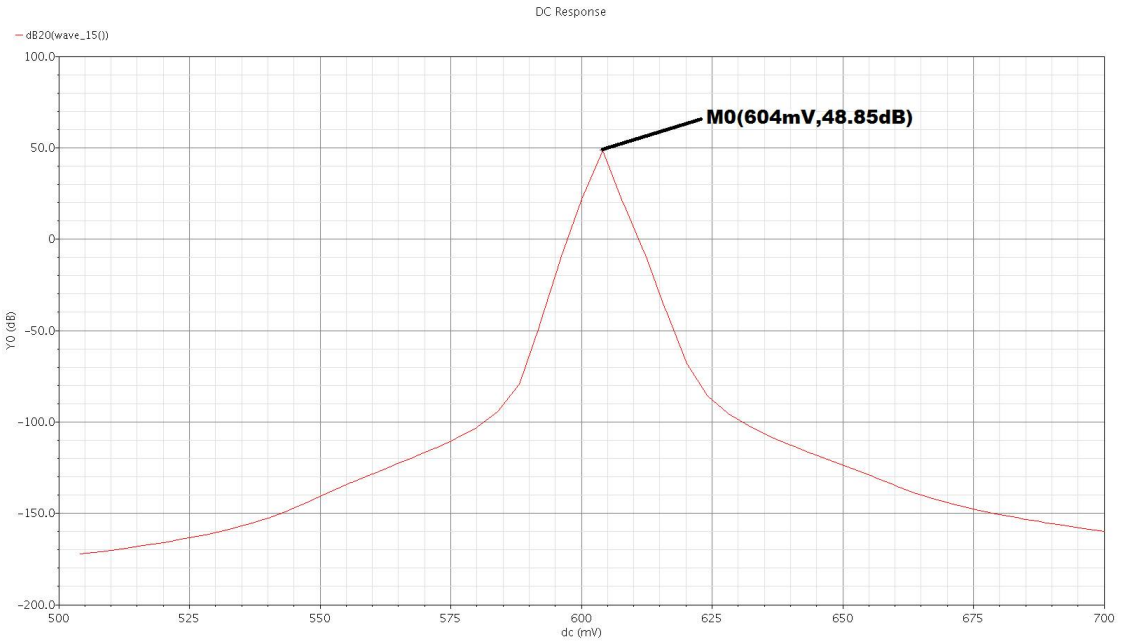


Figure A3: Voltage gain in decibel for hysteresis-free comparator

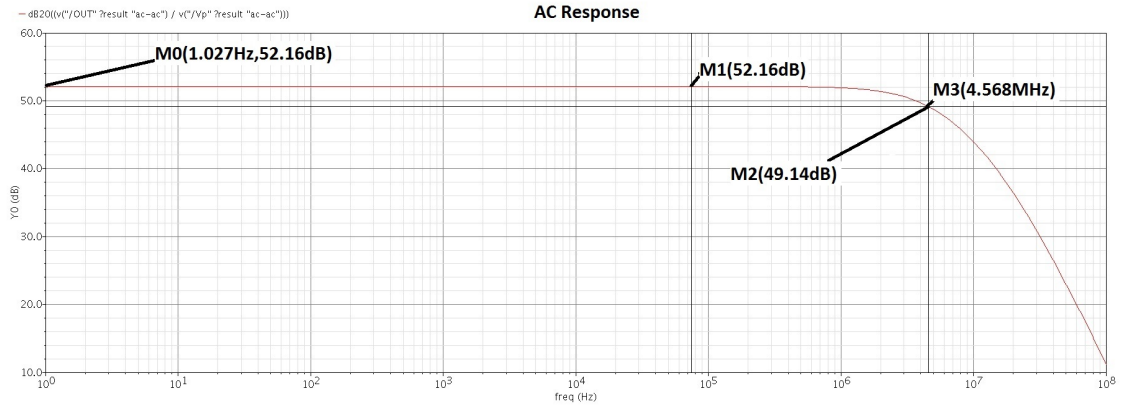


Figure A4: Frequency response highlighting the 3dB frequency for hysteresis-free comparator

Transient or time domain analysis is applied to a system or a circuit to obtain the propagation delay and to monitor the required output of the comparator. Propagation time delay is quantified with (A.1), with tr_{pd} and tf_{pd} represent rising propagation delay and falling propagation delay, respectively. Rising propagation delay also known as low-to-high propagation delay, $Tplh$ is the time taken between a change of input and a low to high change to the output while falling propagation delay, also termed as high-to-low propagation delay, $Tphl$ is the time taken between a change of input and a high to low change to the output. Both the rising and falling delays, are measured from the 50% point on the input signal to the 50% point on the output signal, as illustrated by Figure A5. .

$$t_{pd} = \frac{tr_{pd} + tf_{pd}}{2} \tag{A.1}$$

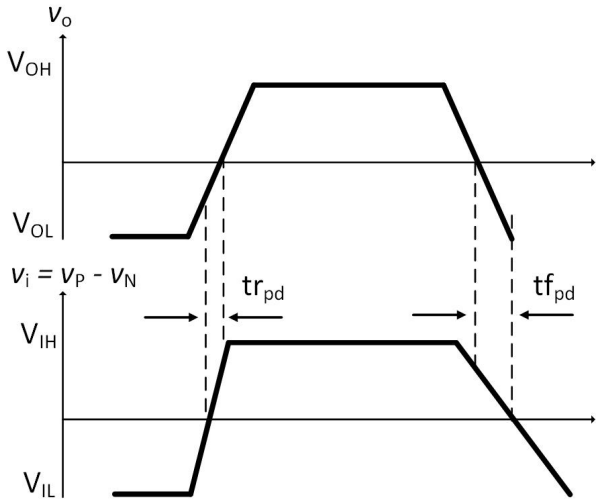


Figure A5: Propagation delay time for rising and falling edge of comparator

The rise and fall time are calculated from the transient waveform as in Figure A6. The propagation delay of 26.654 ns for the comparator is calculated using the propagation delay equation as previously stated, with measured fall time as 47.1 ns and rise time as 6.208 ns. The target propagation delay for this comparator is less than 40 ns. The output of the comparator is monitored from running a transient analysis, as illustrated in Figure A7. It can be seen that the crossing points of intermediate outputs, V_{op} and V_{om}; are the points where the change of output levels of HIGH or LOW occurred.

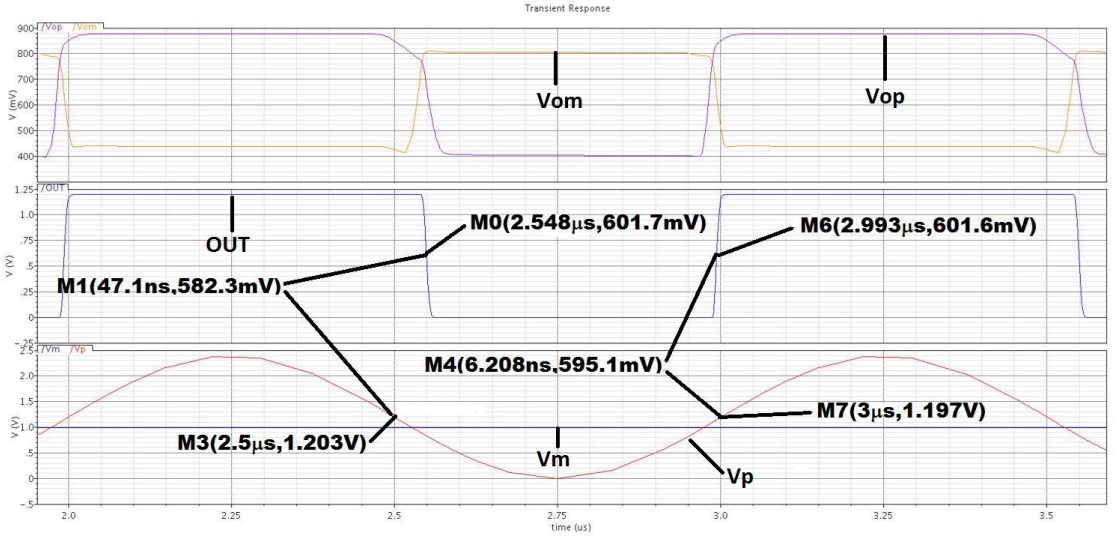


Figure A6: Rise and fall time of comparator

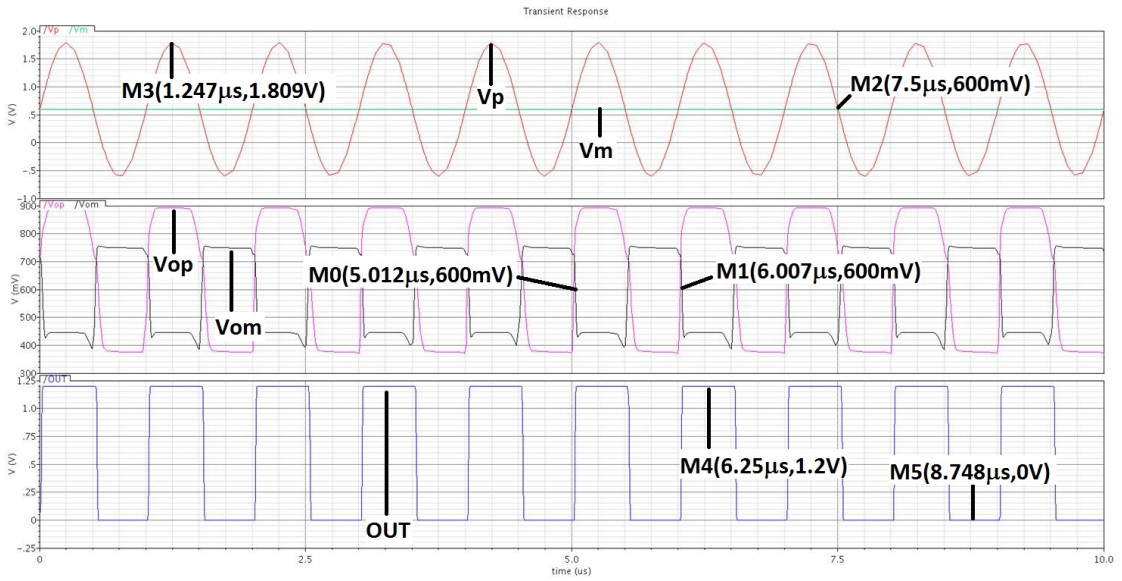


Figure A7: Transient response of the output of comparator

Appendix B

Comparator-with-hysteresis Analysis

These are the tools which have been used for the circuits' implementations.

1. CADENCE Virtuoso Schematics (Transistor-level architecture)
2. CADENCE Analogue Design Environment (Circuit simulations)
3. Design Kit IC6141 TSMC65RF (65-nm)

Similar to hysteresis-free comparator, in order to make sure that the comparator designed is within the specification range; various analysis shall be performed such as DC and transient analysis. Input signals for the comparator, Vinp is a sinusoidal signal of 1.2 V amplitude, and 100 MHz frequency while Vinm is a a sinusoidal signal of 1.2 V amplitude with the same frequency. Both sinusoidal input is set at 1V DC voltage and AC amplitude of 1V. The voltage references, Vrefp and Vrefn are 1.0 V and 0.2 V. Vbias, initially was selected as 1 V. After running the DC response, the Vbias has been selected from the midpoint of VDD.

The offset voltage of the comparator can be obtained from taking a DC response from applying a DC input of 600 mV (half of VDD) to Vrefp and Vrefn while Vinp is swept between 0 to 3.9 V, with a step size of 4 mV. Vinm is set to zero during DC analysis. Vbias has been set initially to 1 V for this particular Dc analysis. The DC response waveform for obtaining the offset voltage is as Figure B1. The offset voltage for the comparator designed is approximately less than 5 mV.

The transfer curve waveform of Figure B1 is taken its derivative to represent the comparator gain and consequently, the resolution of the comparator can be known as well. Figure B2 represents the derivative of the waveform in Figure B1, which shows the

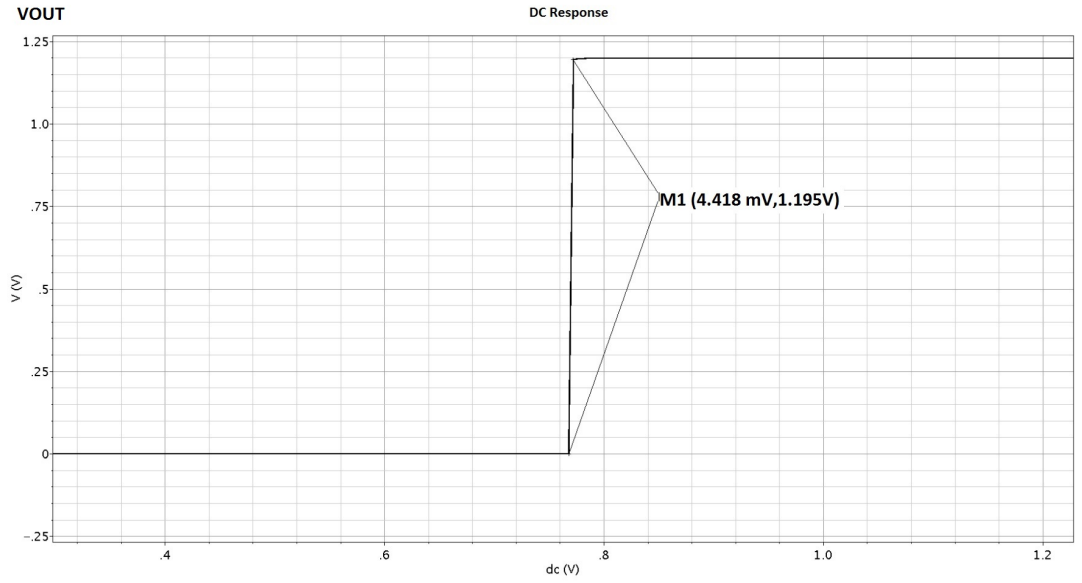


Figure B1: DC response to obtain input offset voltage for comparator-with-hysteresis

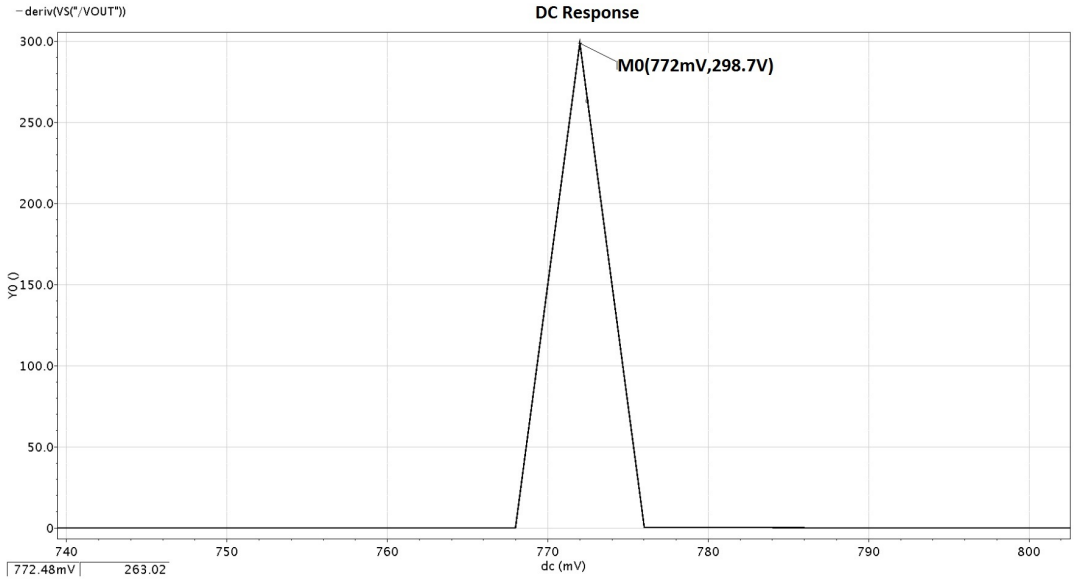


Figure B2: The derivatives of the DC response to obtain voltage gain for comparator-with-hysteresis

voltage gain of the comparator. Figure B3 represents its decibel equivalence of a 9-bit comparator.

In order to run AC analysis, a definite value of Vbias is required. This can be obtained from running a DC response, as completed in Appendix A. By marking the midpoint of

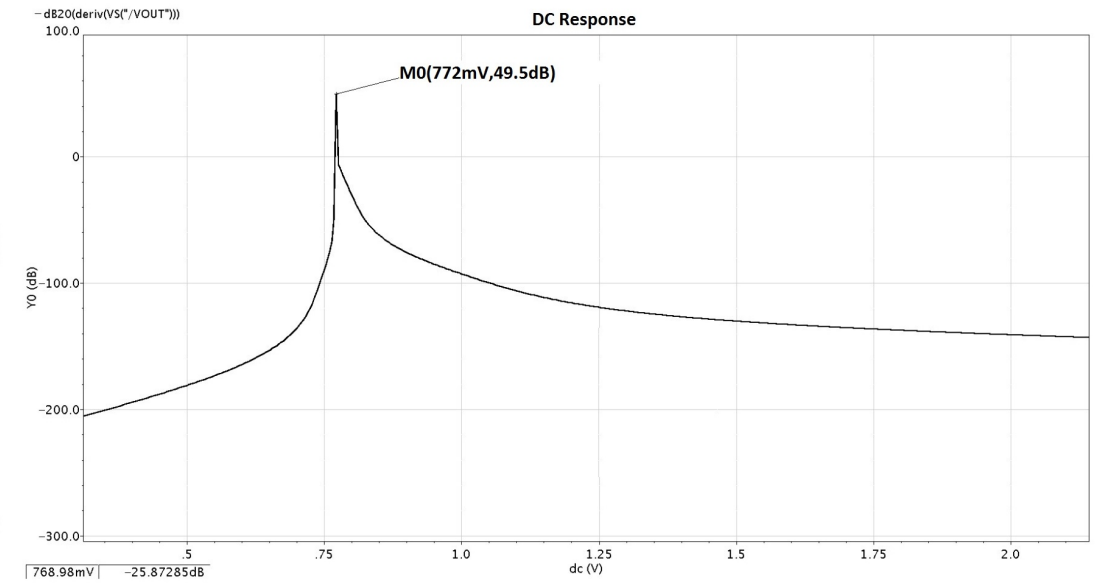


Figure B3: Voltage gain in decibel for comparator-with-hysteresis

VDD, 0.6V on the DC response gave the supposed Vbias value, which is approximately 770 mV, as illustrated in Figure B4. By setting Vbias as 770 mV, the AC analysis was performed. The sweep range of the frequency response has been set to and for logarithmic plot. The frequency response from the AC analysis is as shown in Figure B5.

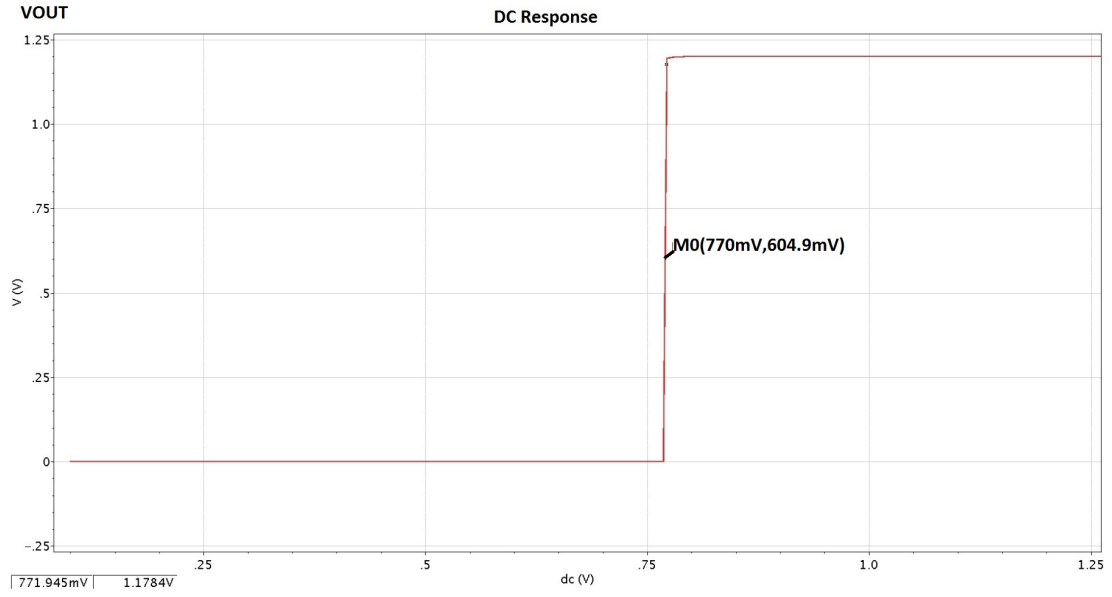


Figure B4: Identifying V_{bias} for AC analysis

Transient or time domain analysis is applied to a system or a circuit to obtain the propagation delay and to monitor the required output of the comparator. The output of the

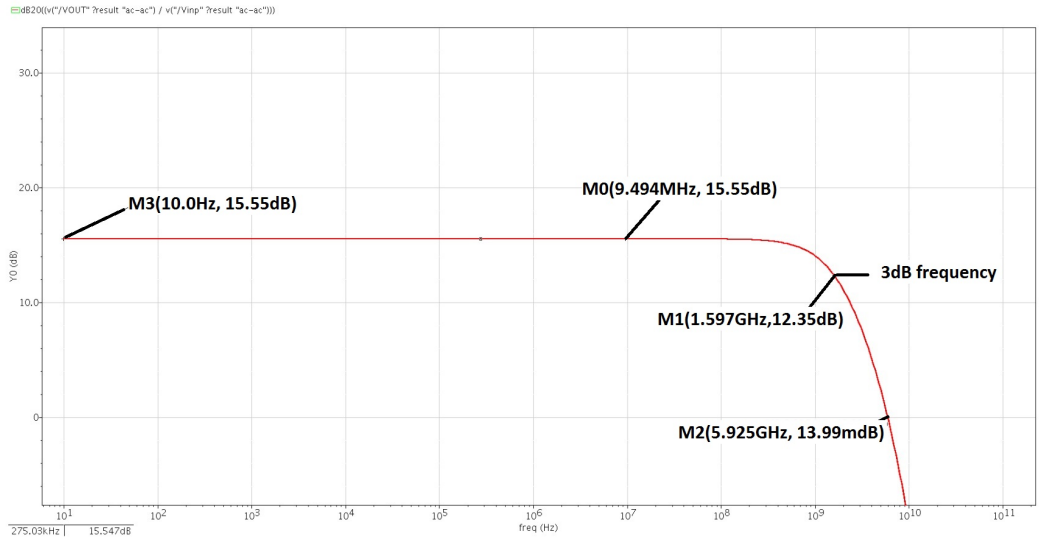


Figure B5: Frequency response highlighting the 3db frequency and bandwidth

comparator is monitored from running a transient analysis, as illustrated in Figure B6. The rise and fall time are calculated from the transient waveform as in Figure B7. The propagation delay of 420.65 ps for the comparator is calculated using the propagation delay equation in Appendix A, with measured fall time as 118.5 ps and rise time as 722.8 ps. It can be observed that the crossing points of intermediate outputs, V_{op} and V_{om}; are the points where the change of output levels of HIGH or LOW occurred.

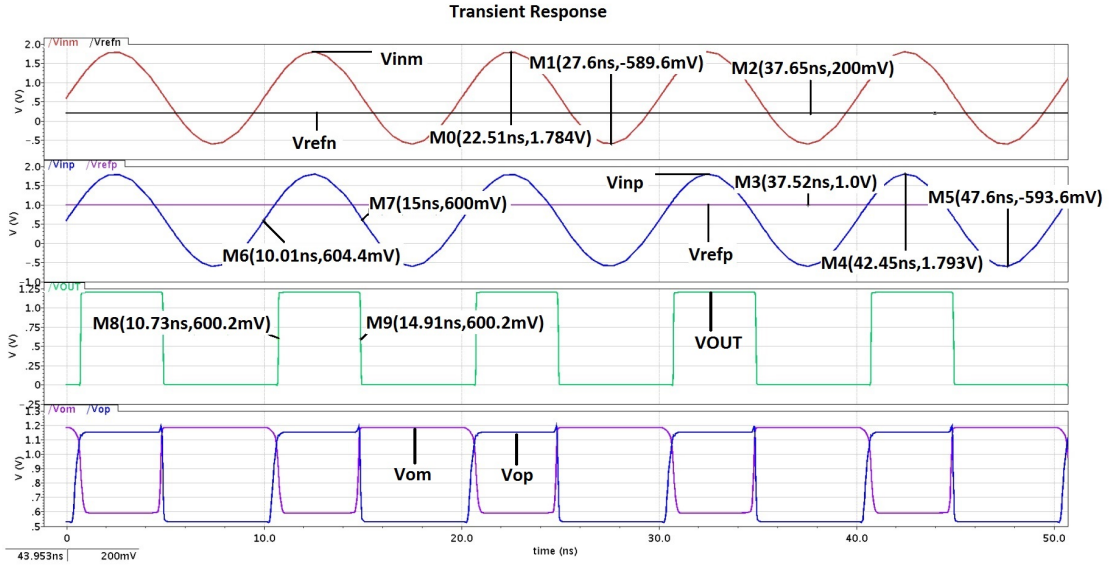


Figure B6: Transient response of the output of comparator-with-hysteresis

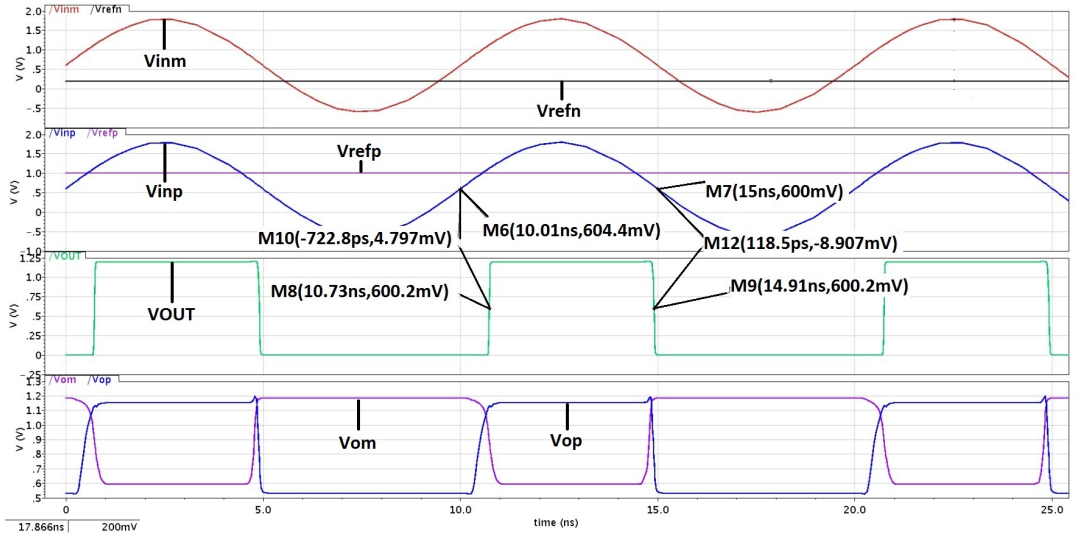


Figure B7: Rise and fall time of comparator

Appendix C

2-stage Operational Amplifier Analysis

These are the tools which have been used for the circuits' implementations.

1. CADENCE Virtuoso Schematics (Transistor-level architecture)
2. CADENCE Analogue Design Environment (Circuit simulations)
3. Design Kit IC6141 TSMC65RF (65-nm)

Earlier in Section 3.5.1, the DC analysis response was used to determine the threshold voltage exhibited by M1 and M3; which were used in obtaining the transistor sizing of M1, M2, M3 and M4. The same DC response has also been observed to make sure that all the transistors are in saturation, by making sure that $V_{DS} > V_{GS}$ - Vth, for each individual transistor. Annotating the DC operating point provides the required V_{DS}, V_{GS} and Vth. In general, DC analysis was performed to check the biasing condition of the transistors. On top of that, DC biasing could also be used to determine the offset voltage of the amplifier and its DC gain as displayed in Figure C1 and Figure C2, respectively. In order to obtain the voltage gain, the transfer curve of Figure C1 has been taken its derivative to represent the amplifier's gain and its decibel equivalence, as shown in Figure C2. The amplifier's systematic offset voltage has been determined from a DC response which was simulated by applying a DC input of 600 mV (half of VDD) to Vin2 while Vin1 is swept between 0.1 to 1.2 V, with a step size of 1 mV. The offset voltage measured for this particular amplifier is reasonably large which is approximately 100 mV, with the voltage gain of 40 that is equivalent to approximately 32 dB.

The AC response for the 2-stage operational amplifier is as illustrated in Figure C3, which highlighted the 3dB frequency as 453.4 kHz and the bandwidth as 21.24 MHz. The AC analysis was performed using Vin1 (amplitude) = Vin2 (amplitude) = 1.2 V,

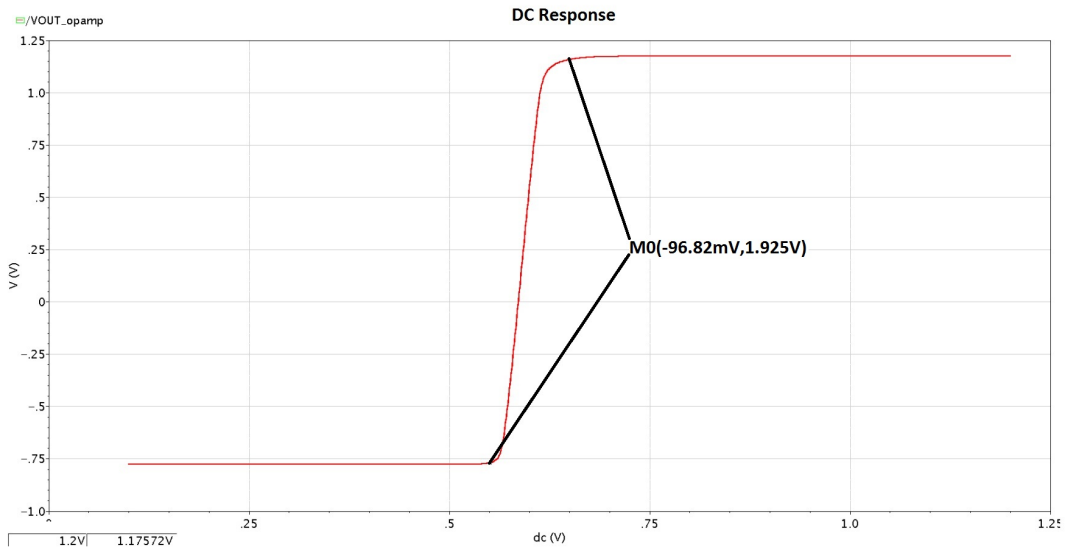


Figure C1: DC response illustrating the input offset voltage for 2-stage amplifier

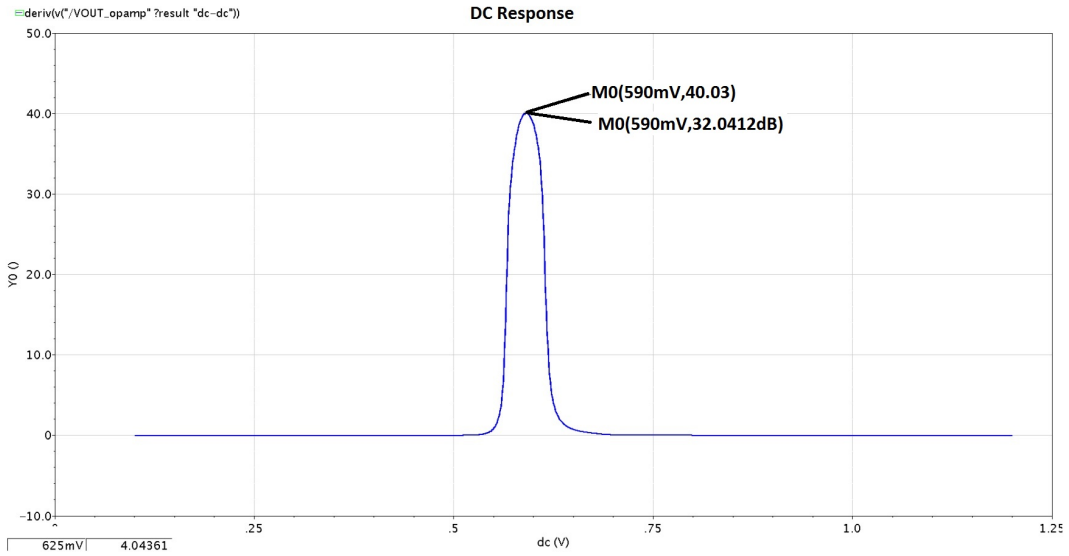


Figure C2: The derivatives of the DC response illustrating the voltage gain for 2-stage amplifier

Vin1 (frequency) = Vin2 (frequency) = 1 kHz and the design specifications of Table 3.8 and Table 3.9.

Transient analysis was performed to observe the behaviour of the 2-stage amplifier and to measure the amplifier's propagation delay. The transient analysis was performed using Vin1 (amplitude) = Vin2 (amplitude) = 1.2 V, Vin1 (frequency) = Vin2 (frequency)

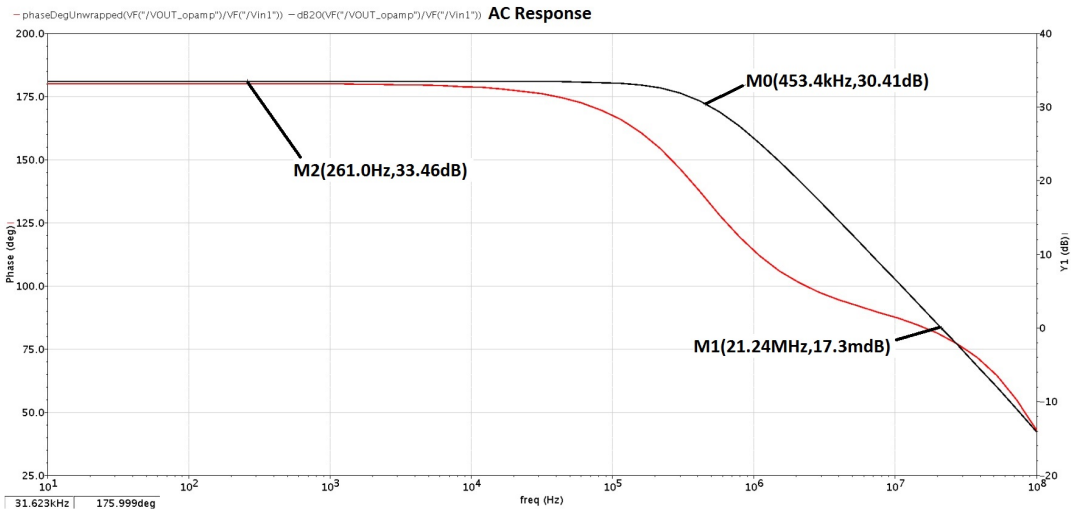


Figure C3: Frequency response of 2-stage operational amplifier

= 1 kHz and the design specifications of Table 3.8 and Table 3.9. The rise time or rising propagation delay and fall time or falling propagation delay are calculated from the transient waveform of Figure C4. The propagation delay of the amplifier is 9.3185 μ s has been calculated using the propagation delay equation in Appendix A, with measured falling propagation delay as 9.158 μ s and rising propagation delay as 9.479 μ s; as illustrated in Figure C5. The 2-stage operational amplifier works at slow speed.

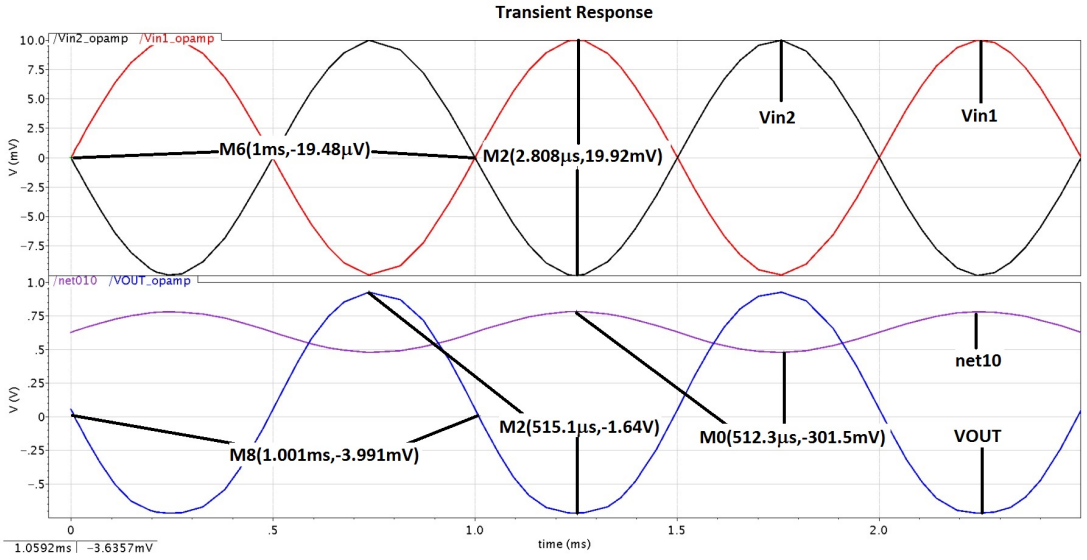


Figure C4: Transient response of 2-stage operational amplifier

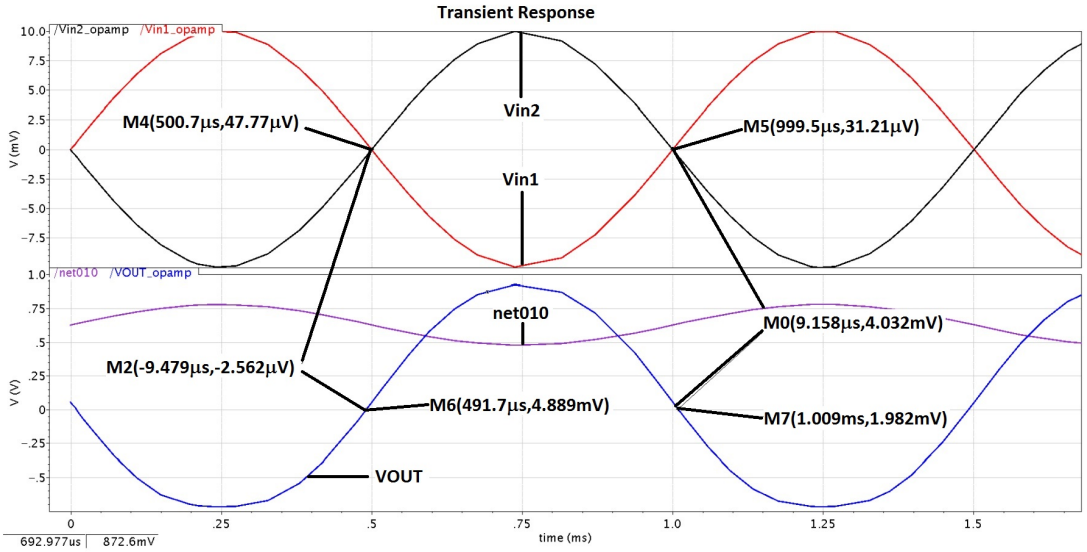


Figure C5: Transient response of 2-stage operational amplifier for measurements of propagation delay

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