56 Gbps Si/GeSi integrated EAM

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ABSTRACT

The growing demand for fast, reliable and low power interconnect systems requires the development of efficient and scalable CMOS compatible photonic devices, in particular optical modulators. In this paper, we demonstrate an innovative electro absorption modulator (EAM) developed on an 800 nm SOI platform; the device is integrated in a rib waveguide with dimensions of a 1.5 µm x 40 µm, etched on a selectively grown GeSi cavity. High speed measurements at 1566 nm show an eye diagram with dynamic ER of 5.2 dB at 56 Gbps with a power consumption of 44 fJ/bit.

1. INTRODUCTION

The modern communication infrastructure can be divided in two categories, the Long-Haul C-band (LHC) and the Short-Haul O-band (SHO) mixed electro-optic systems. LHC advantages derive from the use of single mode fibers (SMF) and high-quality optic fibers amplifiers that allow transmission over hundreds of kilometers without signal regeneration. SHO, on the other end, by implementing cheaper multi-mode fibers (MMF) and optic sources (SLED, VCSEL) is more cost effective, hence, it is vastly used in datacenters.
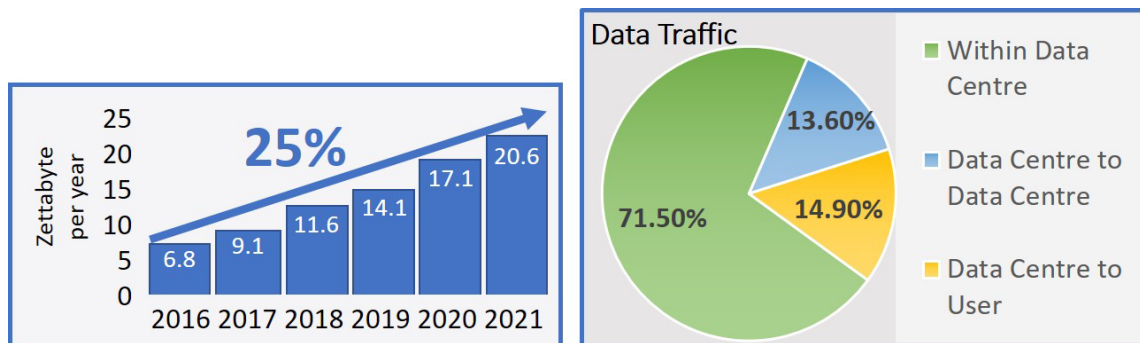

Figure 1 Cisco Annual IP growth Prediction (left) and Data traffic ratios (right)[2].

The SHO bandwidth, however, is limited by the MMF's modal dispersion and represents a bottleneck for aggregate multi wavelength systems with data rate from 200 Gb/s and connection distances beyond 500 m (802.3bs standard[1]). To emphasize further the future scalability requirement needs, a recent Cisco Report[2] has predicted that by 2021 the annual IP traffic will exceed the 20 Zettabyte (left graph of Figure 1), with most of the traffic within the datacenter (right pie chart of Figure 1). In a decade datacenters will require, therefore, link speed approaching 800 Gb/s or 1.6 Tb/s, as envisioned by the Ethernet Alliance's Roadmap[3] (Figure 2).
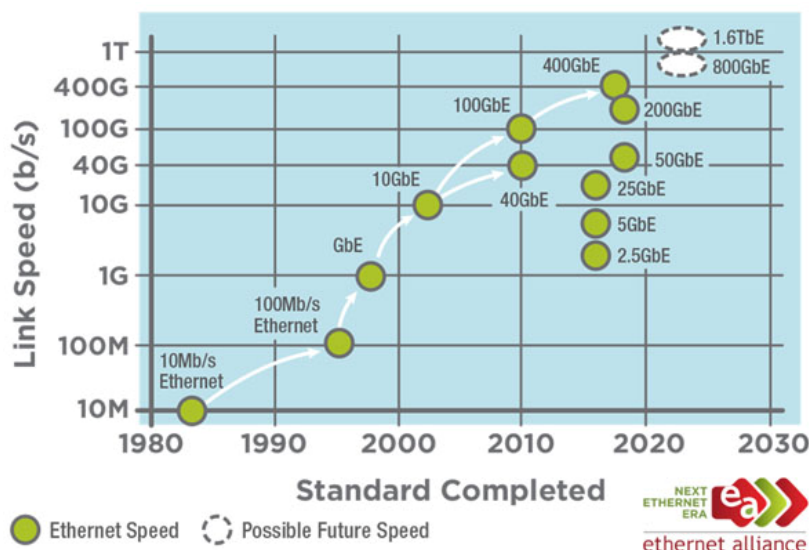
Figure 2 Ethernet Alliance's roadmap for the Terabit Ethernet[3]

That is why companies are investing in reduction of single mode fibers (SMF) deployment costs[4] and integrating Silicon Photonic Circuits (Si-PIC) into transceivers[5] to boost the bandwidth in datacenters. Si-PICs can, indeed, reduce the power consumption of transceivers through high-density integration, increase data rate for long short to mid-range distance and reduce latency by avoiding conversion from/to electric signals and reduce the use of copper wires. Compatible materials for this technology are based on group IV compounds, which exploit the CMOS knowhow and do not require the conversion of exiting fabrication facilities, making Silicon Photonics very attractive to the industry. So far, integrated silicon and multilayer based systems[6]-[8] including high speed photodetectors[9],[10], wavelength division multiplexing (WDM) filters[11] and in particular optical modulators[12]-[13] have been successfully demonstrated.

In silicon, Plasma Dispersion Effect[14]-[17] based modulators achieve high speed but at the expense of a relatively large footprint ($\sim$mm^2) and power consumption (pJ/bit) and this makes high density integration challenging. To alleviate those limitations highly resonant devices have been developed[18],[19]. However, these devices have limited operational optical bandwidth and suffer high temperature tolerances due to the high thermo-optic coefficient of silicon ($\sim$1.9 X 10^{-4} K^{-1})[20] and the wavelength selectivity of ring resonators.

Through the use of Ge and GeSi, Electro Absorption Effect based modulators[21]-[23] (Franz-Keldysh Effect[24],[25] in bulk for the C/L-band and the Quantum Confined Stark Effect[26] in quantum well materials for the O to C Band) offer the best trade-offs in terms of speed, footprint and power consumption for highly integrated Si-PICs and short/medium-haul applications. For bulk FK based modulators, Thermal Anneal[27] (RTA) or Rapid Melt Growth[28],[29] (RMG) techniques can be used to integrate arrays of modulators working at different bandgap energy or wavelengths by tuning of the material composition. These techniques offer the potential to overcome the limited optical bandwidth ($\sim$35 nm) of this class of modulators.

Here, we present an integrated rib waveguide modulator[30] realized on a selectively grown Si/GeSi cavity on 800 nm SOI wafer; the active area is a wrap-around PIN hetero-structure with dimension 1.5 μm x 40 μm, which enables electric field independency from the rib width and the possibility to tailor the waveguide dimension to provide better optical mode confinement and propagation for both polarizations. High speed measurements show a dynamic ER of 5.2 dB at a data rate of 56.2 Gbps, power consumption of 44 fJ/bit and modulation bandwidth of 56 GHz. This design, therefore, provides a highly customizable and simple platform for compact-high-speed electro absorption modulators.

2. MODULATOR DESIGN

Simulations were carried to optimize the design and develop the process for integrating a vertical PIN diode in a standard rib waveguide. The platform used for simulations is summarized in the graph of Figure 3, upon defining a set of parameters such as rib width, doping levels and distances, the cross-section process first and the electric field distribution after, are simulated (yellow squares, S1 and S2). By extrapolating the electric field map, the absorption coefficient due to

FKE is calculated (material simulation) by using a mathematical model[31], then, the complex refractive index in the cross-section mesh is retrieved with the Kramers-Kronig relations[32] (M1). The electric and the material simulations are finally used in the mode solver (M2) to find the optic mode distribution and calculate the Insertion Loss (IL), the Extinction Ratio (ER), the device speed and power consumption.
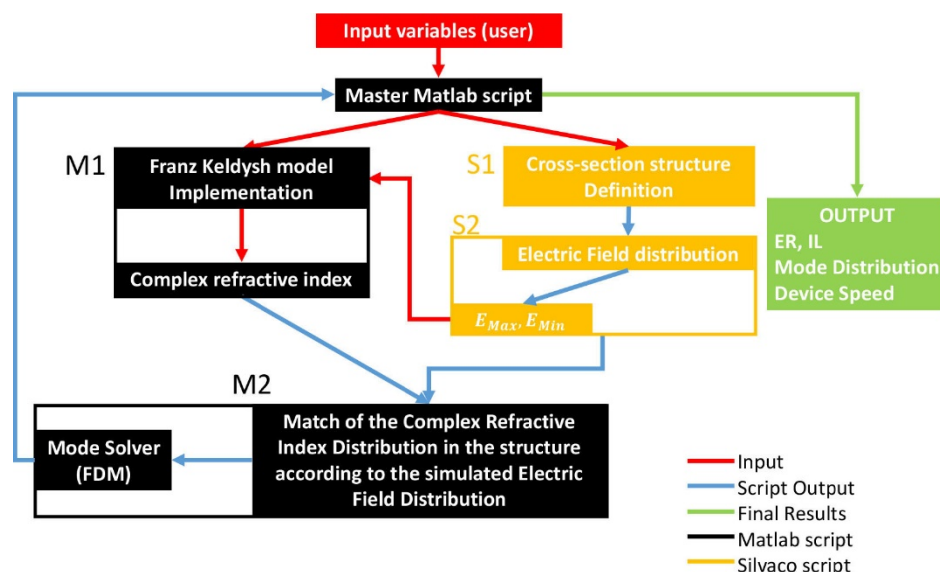

Figure 3 Simulation Platform Schematics

After optimizations, a wrap-around PIN Si/GeSi hetero-structure integrated in a 1.5 µm wide rib waveguide has been adopted, this is shown in the left picture of Figure 4. The P doping of the diode is defined in a 100 nm thick silicon layer (light brown), whereas the 600 nm thick intrinsic region comprehends the Ge buffer layer (black) and a GeSi area (purple). The N doping (orange/red area) is, instead, defined on the top and right side of the rib with a thickness of ~100 nm. The advantages of this approach can be seen in the simple process and the independency of the electric field strength from the rib width which allows to realize wide waveguides. The high customizable design permits, also, the device to support either TE or TM modes (in this first run TE mode has been chosen) but more importantly to confine better the optical mode. In the right picture of Figure 4, the overlap between the optical mode and the electric distribution is depicted, showing an electric field of about 40 kV/cm where the optical mode is mostly confined.
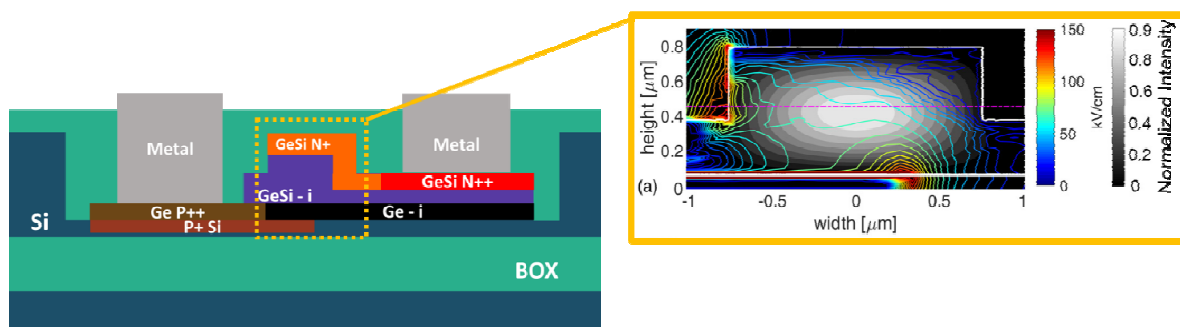

Figure 4 (Left) cross-section design. (Inset) electric field and optical mode overlap and distributions; in rainbow the electric field strength in kV/cm, instead in grey tone the normalized optical power of the propagating TE mode.

3. FABRICATION

Once the design has been fixed, the process is implemented with the fabrication steps depicted in Figure 5. The fabrication process requires three etches and four implantations.
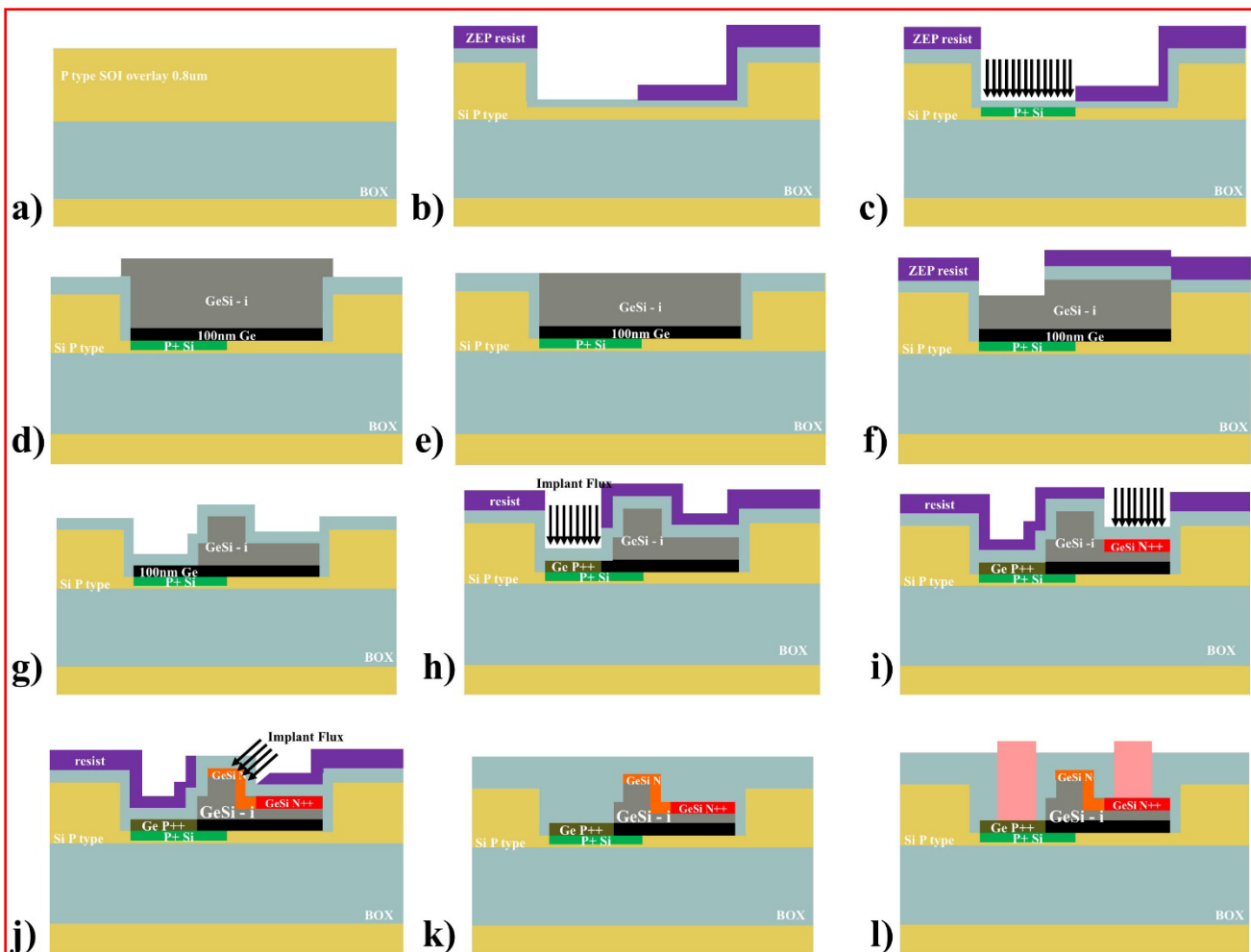
Figure 5 Principal Process Steps

The SOI wafer used for the fabrication of this device has an 800 nm thick Si overlayer; GeSi epitaxy cavities with a size of 50 μm x 40 μm are etched with a depth of 700 nm leaving approximately 100 nm of Si where the P side of the vertical PIN structure is realized using Boron implantation with a concentration of $\sim 10^{18}$ cm^{-3} (Figure 5 a to c). After doping, the cavity is filled with GeSi using a two steps selective epitaxial growth; first ~100 nm of Ge buffer layer is deposited in the cavity trench, then a uniform GeSi layer of about 600 nm thickness is deposited. Chemical Mechanical Polishing, to remove any GeSi excess and planarize the wafer, precedes the waveguide etch step (Figure 5 d, e) that is defined by a two etch process. In the first step (f) only the left side of the cavity is etched with a depth of 200 nm, then the waveguide is etched to a depth of about 400 nm to realize the rib as shown in Figure 5 g. On the left side of the rib only 100nm of Ge is left, whereas on the right side of the rib, a 300 nm thick slab is obtained. The waveguide etch technique adopted is self-aligned because the Si and the GeSi waveguides are etched on the same time (Figure 6, picture on the left), reducing interface mode mismatch. The simulated interface optical loss is about 0.3 dB per facet. During the waveguide definition, coupling gratings at the waveguide extremities and silicon normalization waveguides close to the device waveguide are, also, defined.

High dose ion implantations to define the ohmic contacts, are then performed. On the left side slab, BF$_2$ (P++) with a concentration of $\sim 10^{20}$ cm^{-3} is implanted in the thin Ge layer (Figure 5 h); on the slab on the right (Figure 5 i), the GeSi layer is doped with a $\sim 10^{19}$ cm^{-3} concentration of Phosphorus (N++). The doping to define the N side of the PIN junction is realized on the top and right side of rib with an angled implantation (45^0) using Phosphorus with a concentration of $\sim 10^{18}$ cm^{-3} and an estimated implantation depth of 100 nm (Figure 5 j). Finally, Rapid Thermal Anneal is performed to activate the doping. The oxide deposition, VIA definition and metal deposition are shown in Figure 5 (k, l); in Figure 6, instead, the top view (left) and the FIB cut (right) of the realized device are shown.
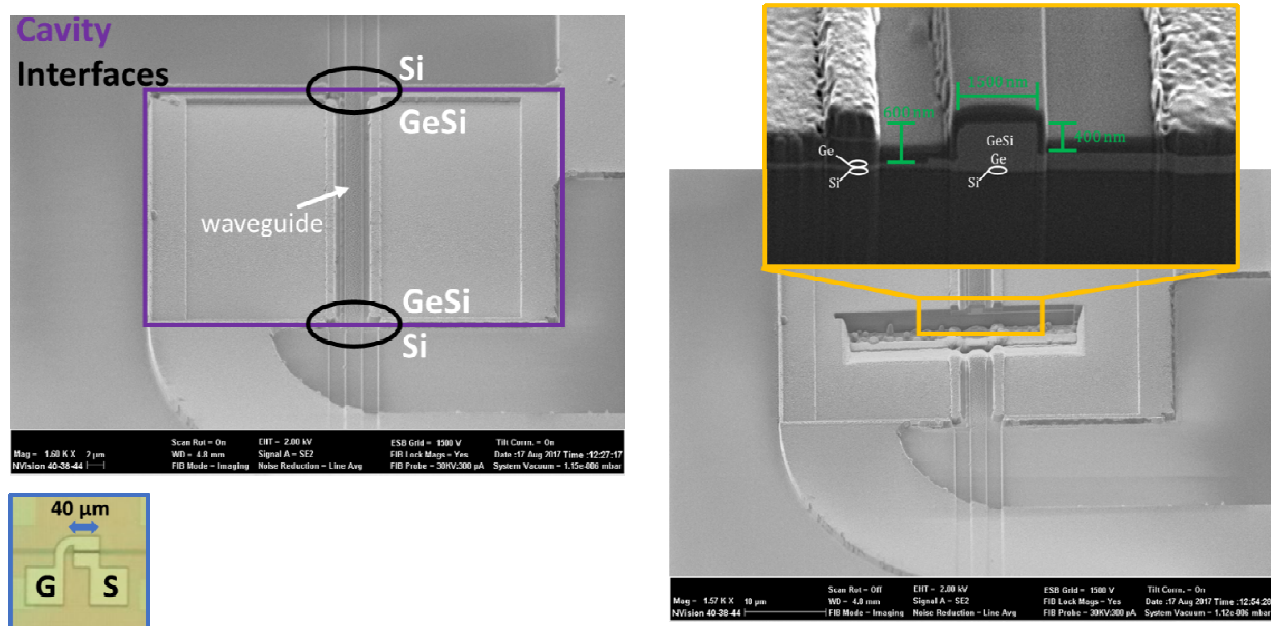
Figure 6 Top view and FIB cut (yellow inset) of the realized device

4. DC AND HIGH-SPEED MEASUREMENTS

To assess the electro-optic effect, DC measurements are performed; for this purpose, a semi-automatic setup (diagram in Figure 7) is built using the Agilent 8163B Lightwave Multimeter with laser module 81949A and Power Meter 81630B, the Keysight 2400 source meter and tungsten tip DC probes from Cascade Microtech. The setup is controlled with Matlab routines.
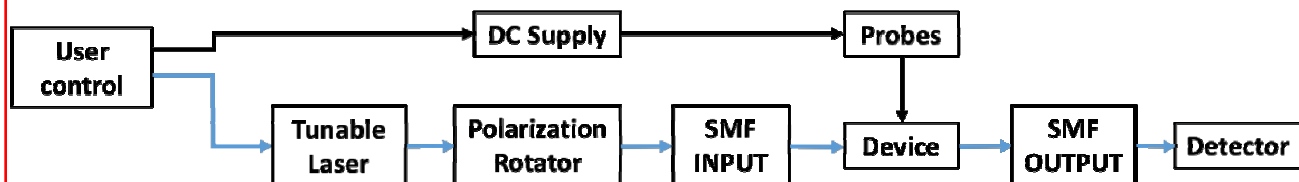

Figure 7 DC Measurements Bench Schematics

The IV curve has been measured to assess the electric performances of the PIN diode and measure the dark current at reverse biases. Mainly caused by surface current and defects in the crystal, dark current affects the device performances by increasing the power consumption. To limit the dark current, a passivation layer is deposited before metallization to prevent current surface paths. The measured IV is shown in Figure 8, at -4 V the dark current is about 10 µA, better epitaxial growth and the passivation layer would lead to its reduction.
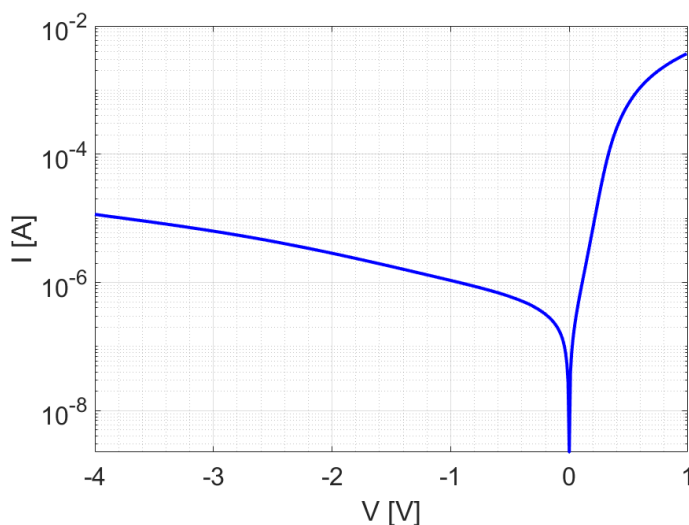
Figure 8 IV curve

The electro-absorption effect, is then tested by measuring optical transmission spectra while applying DC biases. The resulting cavity Insertion Loss (IL) and Extinction Ratio (ER) are shown in Figure 9. The IL measures the optical loss between the laser input and the detector, hence it comprehends coupling loss, propagation loss, losses at the Si-GeSi interfaces and material absorption in the cavity. By using the silicon normalization waveguides and estimating, through simulation, the losses at the Si-GeSi interfaces it is possible to retrieve the IL of the cavity, dominated by material absorption. For this first prototype the presence of the Ge buffer layer is responsible for a higher IL, due to background and undesirable absorption in the wavelength range of interest. Insertion Loss can be improved by using Rapid Thermal Anneal[27] before the device is realized to diffuse silicon into the Ge buffer layer to obtain a homogenous GeSi layer, or growing GeSi layer with epitaxial techniques that do not require any Ge buffer layer[28],[29].

However, the ER, measured by the absorption difference between the high and low states, reaches considerable values and shows a secondary peak for wavelength above 1570 nm confirming the effect of the Ge buffer layer. For a reverse bias of 1 V the ER is 3 dB at 1540 nm, at higher reverse biases it increases up to 7.5 dB (bias = - 4 V); an incremental ER rate of about 1.5 dB/V is found around 1540-1545 nm.
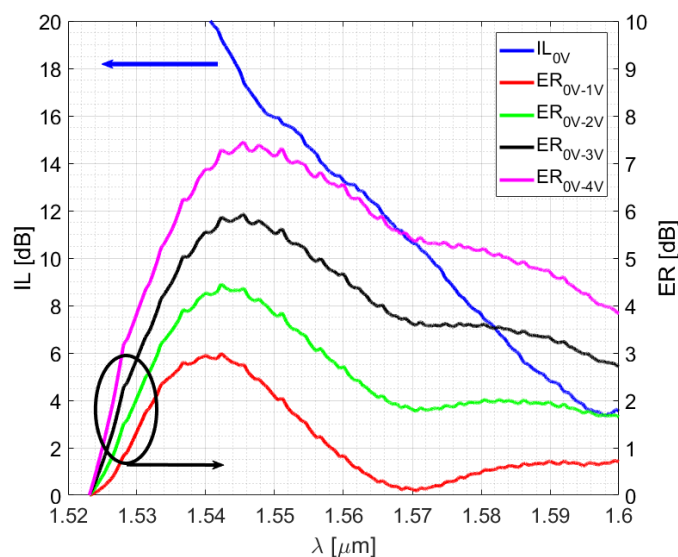

Figure 9 (left) IL and ER, (right) for different reverse biases

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High-speed measurements are conducted by including in the DC setup a pseudorandom binary sequence (PRBS) generator, RF amplifier and attenuators, an EDFA, an optical filter and a DCA as shown in Figure 10. The PRBS is coupled to the RF amplifier and the in-line RF attenuators to generate the electric bitstream with the required voltage swing; the DC and RF electrical signals are, then, mixed with a bias-T and fed into the modulator using GS probes not-50-ohms terminated. At the modulator output, the low noise EDFA and bandpass filter are used to amplify the modulated optical signal, which is finally analyzed by the DCA.
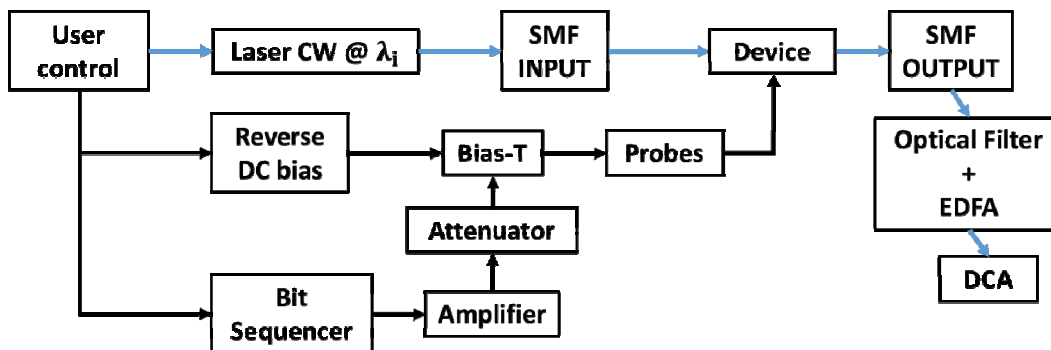

Figure 10 High-Speed Measurement Bench Schematics

Several tests are conducted to find the electro-optic parameters that offer the best performances; first, measurements to investigate the maximum speed supported by the device are performed, then by fine tuning the parameters the highest dynamic ER at maximum speed is found. It must be noted that, the probes were not resistively loaded and caused RF reflections at the modulator ports increasing the Vpp. The optical bandwidth of the EDFA and optical filter used in the setup also limited the measurement of the modulation at a wavelength of 1570 nm.

By choosing a modulation wavelength of 1566 nm and applying a bias of -2.7 V and 2.2 Vpp, an ER of 5.2 dB at 56.2 Gbps is recorded (Figure 11), which represents the best performance of this first prototype.
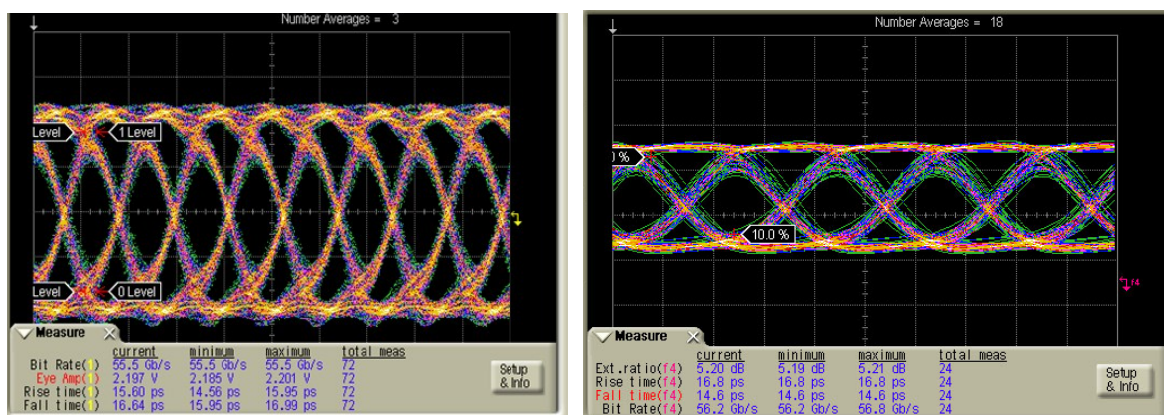

Figure 11 (Left) Electrical Eye at 56 Gbps and 2.2 Vpp. (Right) Output optical eye with a measured dynamic ER of 5.2 dB at 56.2 Gbps at wavelength of 1566 nm

The maximum speed recorded is, however, not limited by the device but by the setup used. In fact, the EO bandwidth, estimated as the reciprocal of the device rise time: $\tau_r = \sqrt{(\tau_o^2 - \tau_e^2)}$ (with τ_o the rise time of the optical eye and τ_e the rise time of the electrical input eye) is found to be ~56 GHz, making possible rate speed higher than 56 Gbps by using NRZ modulation.

The last set of measurements investigated the EAM electric equivalent circuit (Figure 12) by mean of S11 measurements and numerical fitting.
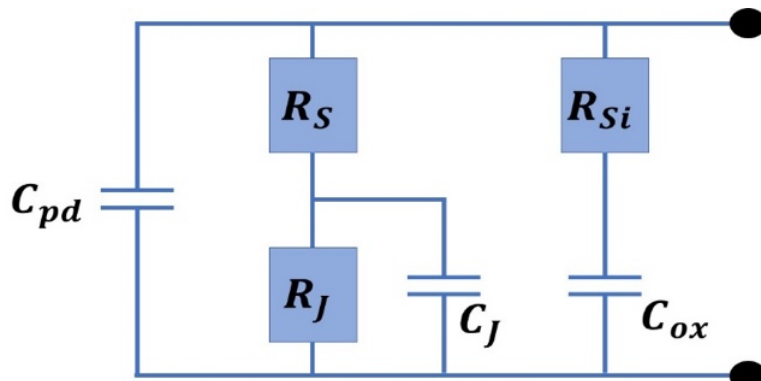
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Figure 12 EAM Equivalent electric circuit

The device is modelled with six lumped elements, the capacitance due to the metallic pads C_{pd}, the series resistance R_S, the resistance R_J and capacitance C_J of the PIN junction, the BOX capacitance C_{ox} and the substrate resistance R_{Si}. The fitted values are shown in Table 1.

Table 1 Equivalent lumped elements fitted with S11 measurements

C_{pd} (fF)	R_S (Ω)	R_J (Ω)	C_J (fF)	C_{ox} (fF)	R_{Si} (Ω)
5	150	1500	11	30	350

The power of the EAM is, then, found to be $C_J Vpp^2/4 = 44$ fJ/bit at 56 Gbps, considering the increased Vpp (~4 V) due to RF reflections caused by not terminated RF probes.

5. CONCLUSION

A high-speed low power consuming and compact footprint (60 μm^2) GeSi EAM on an 800 nm SOI platform has been designed, fabricated and characterized. The novel vertical PIN diode allowed the realization of an integrated rib modulator with a height-to-width ratio of ~2.4, permitting a better optical confinement and tolerant design parameters due to the independency of the electric field strength from the rib width. Successfully working at 1566 nm, the demonstrated rate speed of 56.2 Gbps with dynamic ER of 5.2 dB is only limited by the setup, in fact an EO bandwidth of 56 GHz is calculated. Finally, S11 measurement and fitting revealed a power consumption of about 44 fJ/bit. Therefore, this concept demonstrated to be a viable solution to integrate optic switches in a CMOS photonic circuits for short reach communication in the C and L bands.

6. FUNDING AND ACKNOWLEDGMENTS

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