Random-Telegraph-Noise and Wave-Particle Duality Found in a Silicon Nano-Wire

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Abstract; The observation of Random-Telegraph-Noise (RTN) in double-gate Silicon Nanowire transistor at room temperature is reported. The device showing no RTN when the channel is fully inverted exhibits RTN upon application of negative voltage on the double gates forming a Quantum Dot (QD) in the nanowire. The particle nature of an electron explicitly appears in the electron transport characteristic where its wave nature is the dominant mechanism to account for.

1. Introduction

Modern electronic devices that employ the state-of-the-art Silicon (Si) technology utilise either the particle nature or wave nature of an electron. One of the most striking phenomenon of its particle nature is Coulomb blockade due to single electron charging in a Quantum Dot (QD), usually observed at low temperatures [1]. The electron's particle nature is also expected to be useful towards the new definition of Ampere in the SI unit using a single electron pump [2]. On the other hand, the conventional Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) are based on its wave nature and a standard fluid model based on drift-diffusion is valid [3]. In this framework only the average number of electron matters, and single electron characteristic is completely neglected. The wave-particle duality, the essential consequence of quantum mechanics, should play a role as the scaling of Si technology goes further down, and understanding the transport mechanism under presence of the both natures is crucial for future device architect.

In this study, we report that the wave-particle duality was observed in the form of Random-Telegraph-Noise (RTN) of drain currents in a Si nano-wire double gate transistor at room temperatures, and we demonstrate that the RTN can be controlled by potential barriers created by gates.

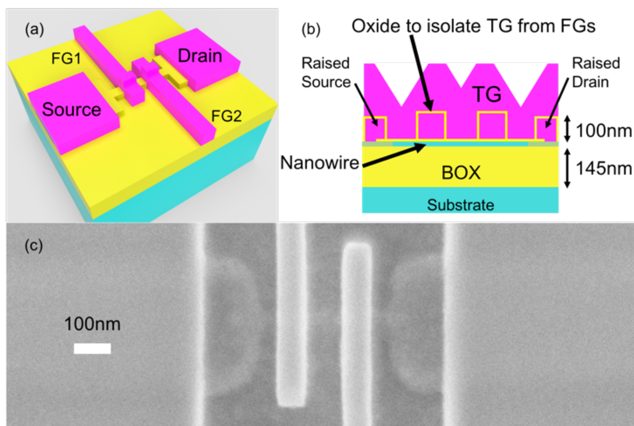

Fig. 1 (**a**) 3D Schematic of the device. TG is not shown. (b) Schematic of the device's cross section with all layers. (c) SEM image of the device, before TG deposition. Nanowire is covered by oxide.

2. Device fabrication

A cross section view of the device and a SEM image are shown in Fig. 1 and 2, respectively. The Si nano-wire was defined on 145-nm thick buried oxide (BOX) using a Si-on-Insulator (SOI) wafer by electron-beam (E-beam) lithography followed by anisotropic wet etching. This enables the surface of the nanowire to be (111) orientation with the atomically flat interface. After gate oxidation to decrease the width of the nanowire down to sub-30-nm and opening dopant windows by E-beam, polycrystalline-Si (poly-Si) was deposited using Low-Pressure Chemical-Vapour-Deposition (LPCVD). Phosphorous was heavily doped to poly-Si by Spin-On-Dopant for the gates. At the same time, the source-drain region was doped and the deposited poly-Si works as raised source-drain. E-beam lithography was performed to define the first gates (FGs), followed by Inductively-Coupled-Plasma (ICP) etching to realise the vertical profile of the gate. 9-nm thick thermal oxide was grown on top of the poly-Si gates, and another poly-Si gate layer was deposited by LPCVD, followed by doping and dry-etching to form the top gate (TG).

3. Results

Oue device was measured at room temperatures using a Cascade M150 probe station with a Keysight B1500 semiconductor device analyser. The nanowire is 30nm wide, and the FG1 and FG2 are 125nm apart. SOI height is 14nm.

Fig. 3 shows the transfer characteristic of the device, which clearly shows the RTN under the application of negative voltages to FGs to form barriers to create a QD at the centre. The same voltage, V_{FG}, was applied on FG1 and FG2. Fig. 4 shows the time domain measurements, under the applications of 50mV to the TG. The current remains constant when the positive bias was applied to the FGs, since no barrier would be created in this case. On the other hand, RTN was observed when negative voltage was applied.

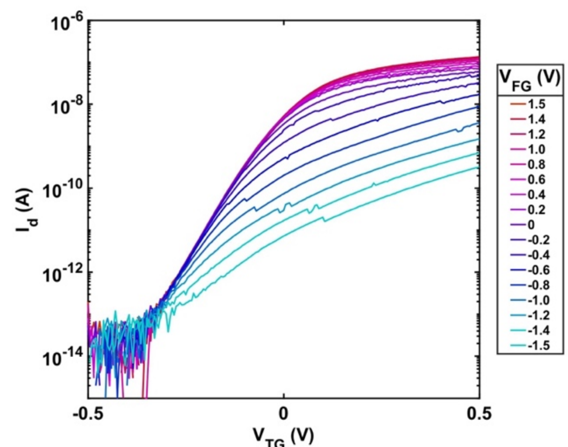

Fig. 3 Transfer characteristic of the device. V_{SD} was 50mV, and different voltages, V_{FG}, were applied on the FGs.

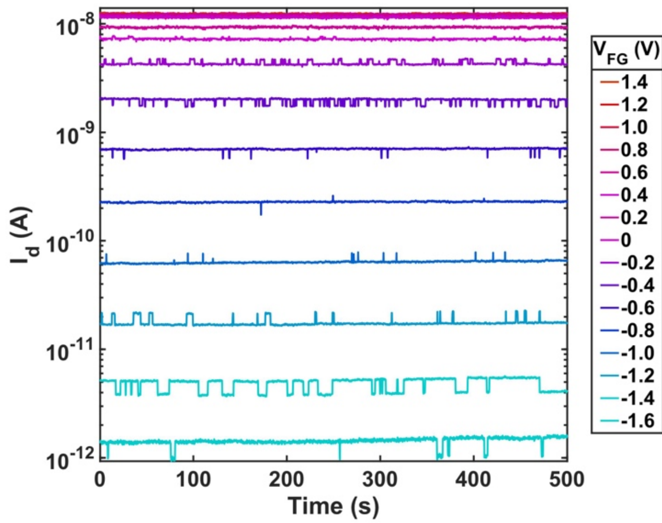

Fig. 4 The results of time domain measurement at V_{TG} = 50mV.

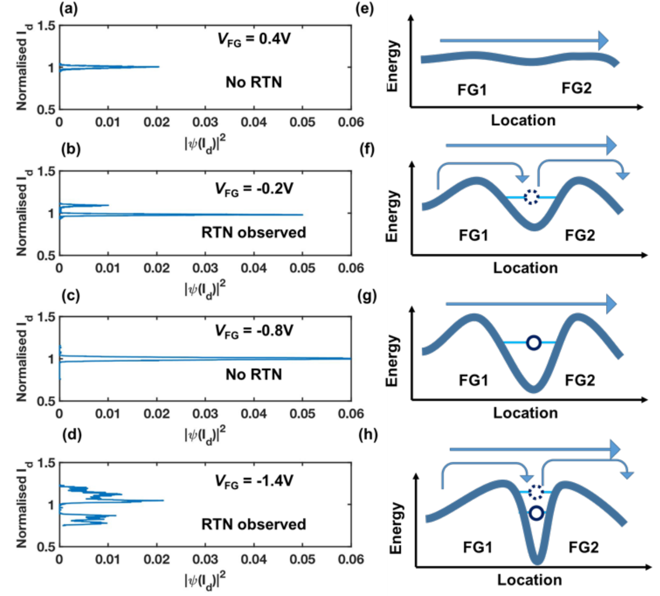

Fig.5 Measured probability distribution at V_{FG} = 0.4V (**a**), -0.2V (**b**), -0.8V (**c**) and -1.4V (**d**) as a function of normalised I_d by its mean value. Corresponding energy diagrams are shown in (**e**), (**f**), (**g**), (**h**) respectively.

4. Discussions

The RTN was observed only when the negative voltage was applied on the FGs, and this can be explained by a charge being trapped/de-trapped in the QD formed by the FGs. In Fig.3, positive shifts in the threshold voltage (V_{th}) can be clearly seen when the negative voltage applied on the FGs, for example -1.5V, -1.4V and -1.2V. This can be explained by the floating-body effect [4], where the electronic potential of the SOI gets higher due to a charge being trapped, resulting in extra gate voltage required for the same output current, hence the positive V_{th} shift. The proposed scenario of a charge trapped/de-trapped in the QD causing RTN exactly follows this model. The measured V_{th} shift should be related to the coupling capacitance of the QD with the gate, which is 8.8aF. This is in reasonable agreement with the capacitance calculated from the V_{th} shift, 10aF and 16mV respectively. This strengthens the suggestion that the RTN is caused by a charge trapped in the QD that we deliberately fabricated.

The observed RTN only appears when the QD is formed, meaning that we can deliberately introduce the particle nature of an electron in the carrier transport mechanism where its wave nature is dominant. To highlight the impact of its particle nature on the transport characteristic, probability to find I_d to be in a certain value during the measurement time is calculated, which is defined by

$$P(I_d) = |\psi(I_d)|^2, \quad (1)$$

where $\psi(I_d)$ is a corresponding wave-function of the system [5]. $P(I_d)$ is calculated from histogram of the time domain measurement. (**a**), (**b**), (**c**) and (**d**) in Fig. 5 show the $P(I_d)$ when 0.4V, -0.2V, -0.8V and -1.4V were applied on the FGs. When no barrier was present, like (**a**), as expected from typical MOSFET operation, $P(I_d)$ has only one peak. Once the barrier was formed, like (**b**), distribution of the probability has two peaks, due to an electron being trapped/de-trapped in the QD, and this cannot be captured by the standard MOSFET model relying on the wave nature of an electron. This shows that the carrier transport mechanism is qualitatively altered by the presence of a single charge in the QD, hence the particle nature of electrons.

Another interesting feature found in Fig. 4 is that the absence of RTN was also observed even when the barrier is formed. At V_{FG} = -0.8V, RTN was not observed as is seen in Fig. 4 and (**c**) in Fig. 5. However, at V_{FG} = -1.4V corresponding to even higher barrier being formed, RTN was observed again. This V_{FG} dependence of presence/absence of RTN can be explained by the existing of multi levels in the QD at room temperatures, and when the first empty state is occupied, another energy state was formed, and start being trapped/de-trapped, causing RTN in I_d, as seen in Fig. 5.

5. Conclusions

We observed RTN in our Si nanowire transistor, only when negative voltages were applied on the FGs. From the V_{th} shift, the origin of this RTN is identified as the trap/de-trap of a charge in the QD between the FGs. This RTN can be understood as the manifestation of the wave-particle duality of an electron, as the presence of a single charge in the QD qualitatively alters the transport characteristic, which is based on its wave nature.

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References

[1] M. Devoret *et al*. *Single Charge Tunnelling* 1 (1992).

[2] S. P. Giblin *et al*. *Nat*. *Com*. **3**, 930 (2012).

[3] T. Yuan *et al*. *Fundamentals of modern VLSI devices*. Cambridge university press, 2013.

[4] J. Choi *et al*. *IEEE Trans*. *Electron Device*. **38.6**, 1384 (1991).

[5] Z. Li *et al*., *Sci*. *Rep*. **8**, 250 (2018).