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Resistive random access memories (RRAMs) are considered as key enabling components for a variety of emerging applications due to their capacity to support multiple resistive states. Deciphering the underlying mechanisms that support resistive switching remains to date a topic of debate, particularly for metal-oxide technologies, and is very much needed for optimizing their performance. This work aims to identify the dominant conduction mechanisms during switching operation of Pt/TiO$_{2\text{-}x}$/Pt stacks, which is without a doubt one of the most celebrated ones. A number of identical devices were accordingly electroformed for acquiring distinct resistive levels through a pulsing-based and compliance-free protocol. For each obtained level, the switching current-voltage (I-V) characteristics were recorded and analyzed in the temperature range of 300 K–350 K. This allowed the extraction of the corresponding signature plots revealing the dominant transport mechanism for each of the I-V branches. Gradual (analogue) switching was obtained for all cases, and two major regimes were identified. For the higher resistance regime, the transport at both the high and low resistive states was found to be interface controlled due to Schottky emission. As the resistance of devices reduces to lower levels, the dominant conduction changes from an interface to the core-material controlled mechanism. This study overall supports that engineering the metal-oxide/metal electrode interface can lead to tailored barrier modifications for controlling the switching characteristics of TiO$_2$ RRAM. © *2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* https://doi.org/10.1063/1.5040936

Metal-oxide (MO) resistive random access memories (RRAMs) have attracted significant attention as potential candidates for next generation nonvolatile memories[1] that enable applications in neuromorphic[2–4] systems and reconfigurable[5,6] electronics. This interest is fueled by their competitive to standard technology attributes, such as their simple 2-terminal structure and scalability,[7] along with their ability to change their resistive levels by proper biasings.[8,9] Further maturing the technology requires a thorough understanding of the physics underlying the resistive switching (RS) effect which will eventually pave the way towards commercialization of the envisioned applications through device performance optimization and enhanced reliability.

Bias induced RS effects are typically attributed to either modification of the metal/MO interfacial properties or to the formation and rupture of conductive nano-filaments.[10–12] However, switching is observed on a variety of MO based systems, and depending on the employed core- and electrode materials, these can be classified into different categories including electrochemical (ECM), valence change (VCM), and thermochemical (TCM) memories.[13] The dominant mechanism thus appears to be case-dependent, but metal-MO interactions strongly affect the RS. Particularly for VCM cells, the application of an electric field results in oxygen exchange reactions, inducing oxygen vacancies.[14,15] A targeted study revealed that introduction of interlayers that

suppress oxygen redox reactions significantly affects the switching dynamics.[16] On the contrary, utilization of layers[17,18] or electrodes[19,20] favouring oxygen exchange was found to improve device switching characteristics, further highlighting the importance of metal/MO interfaces. In addition, it is also worth recognizing the important role of the initial electroforming process, typically performed by utilizing current compliance, as it may bring identical devices to discrete resistive levels[21] potentially attained due to different mechanisms. To date, the majority of reports studying the underlying RRAM mechanisms are focused on a single post-forming condition and are typically performed at room temperature.[10,21–25]

This work aims to shine more light on the governing RS mechanisms at discrete resistive levels obtained on identical TiO$_2$-based RRAM devices by studying the conduction mechanisms dominating the transport across the Pt/TiO$_{2\text{-}x}$/Pt stacks. Our study is performed via a pulsing-based and compliance-free electroforming process followed by temperature dependent current–voltage (I-V) characterization. Considering a similar field dependence of the various potential conduction mechanisms in wide bandgap materials,[26] this temperature study allows identifying the dominant ones, through the corresponding signature plots.

The electrical measurements were performed on Ti(5 nm)/Pt(10 nm)/TiO$_{2\text{-}x}$/Pt(10 nm) devices fabricated on an oxidized (200 nm SiO$_2$) six-inch Si wafer. The oxide films were deposited by reactive sputtering (Helios XP, Leybold optics) from a Ti target in an oxygen plasma environment by

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our standard recipe, described in Ref. 27. The film thickness was calculated using a "Woollam MD2000D Ellipsometer" to be $24.09 \pm 0.16\,nm$,[28] and the roughness after the bottom electrode (BE) deposition and atop of the oxide film was $2.322 \pm 0.1321\,nm$ and $1.434 \pm 0.08461\,nm$, respectively.[29] The material level characterization study performed previously[30] on films/stacks fabricated using the same recipe revealed an amorphous sub-stoichiometric nature of the $TiO_{2-x}$ films with x in the range of 0.05–0.10. The current vs voltage (I-V) characteristics were obtained from $20 \times 20\,\mu m^2$ standalone RRAM cells using our in-house memristor characterization platform ArC ONE[TM31] by applying biases to the Pt top electrode (TE) with respect to the Pt bottom electrode (BE) that was continuously kept at ground potential. All experiments were performed on a Cascade SUMMIT 12000B semi-automatic probe station that incorporates a thermal chuck, whose temperature can be controlled by an ESPEC ETC-200L unit. Measurements were carried out in the range of 300 K–350 K, with a 10 K step.

Devices in their pristine state exhibit resistance in the GΩ range attributed to very high interface barriers (Fig. S1 in the supplementary material). Prior to further characterization, the devices underwent a pulsing-based and compliance-free electroforming process at room temperature, as depicted in Fig. 1. This is performed by applying a bespoke time-width train of pulses with progressively increasing amplitude until the device resistance reaches a set limit. This experimental protocol is then repeatedly applied by modifying the resistance limit that allows reaching distinct resistive levels.

For our $Pt/TiO_{2-x}/Pt$ prototypes presented in this work, three stable resistive levels were attained. Level #1 exhibits resistance on the order of MΩ, level #2 tens of kΩ, and level #3 of kΩ. Fine tuning and programming to specific resistive states around these levels are possible as demonstrated previously.[9] The room temperature I-V curves, shown in Fig. 2(a), reveal two major operation regimes. The first one corresponds to levels #1 and #2 and thus to higher resistances and is characterized by an asymmetric signature with respect to
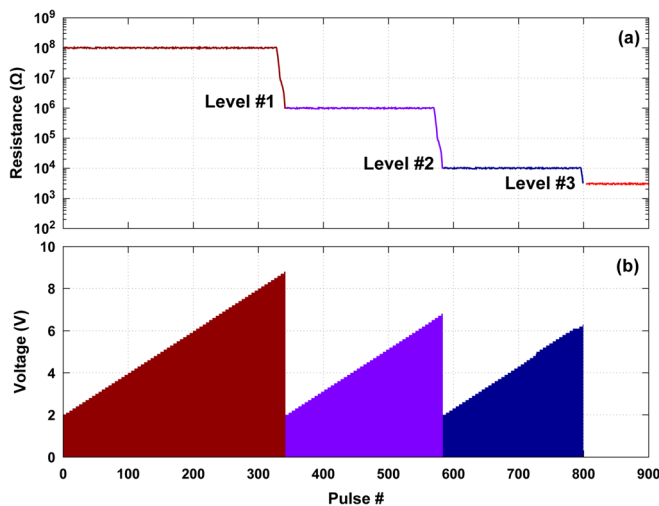


FIG. 1. Representation of our compliance-free, pulsing-based electroforming protocol applied through ArC ONE[TM]. This protocol forced identical devices to attain distinct resistive levels. The top graph (a) illustrates the attained resistive levels, and the bottom graph (b) depicts the causal pulsing stimuli.
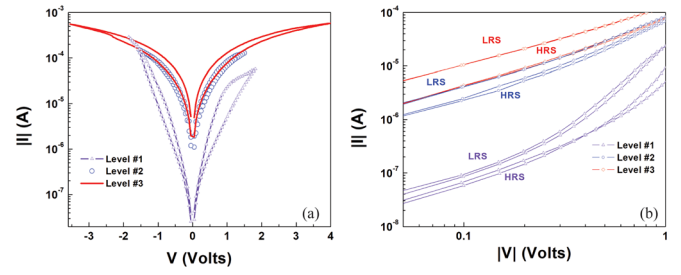


FIG. 2. Room temperature I-V curves presenting the switching operation for each of the stable resistive levels attained by our pulsing-based compliance-free electroforming process in the $Pt/TiO_{2-x}/Pt$ RRAM stacks (a). The absolute current vs voltage plots highlight the asymmetric/asymmetric and the symmetric/asymmetric character of the LRS and HRS respectively, showcasing two different operation regimes in identical devices (b).

the applied bias polarity for both their high resistive state (HRS) and low resistive state (LRS). The second one, for the lower resistances of level #3, shows an asymmetric characteristic signature for the HRS, transformed into symmetric for the LRS regime [Fig. 2(b)]. For a metal-insulator-metal (MIM) stack, the asymmetry in the I-V is an important indication of interface-controlled transport in contrast to the symmetric performance that typically arises by the core film area determined conduction.[32] This is a preliminary qualitative observation (should be confirmed by the signature plots) which showcases that dissimilar mechanisms are responsible for the RRAM operation at these resistive levels.

In order to shine more light on the responsible mechanisms underneath, the current voltage characteristics have been recorded with temperatures spanning from 300 K to 350 K. This temperature analysis allows for reliable separation between dissimilar conduction mechanisms. For wide bandgap materials, these exhibit a characteristic temperature dependence.[26] The dependence can be extracted through the corresponding signature plots, and thus, any potential misinterpretation is minimized.

The device operation at level #1 (corresponding to the MΩ range), apart from being asymmetric, also exhibits a temperature activated conductivity at both LRS and HRS [Fig. 3(b)]. This behavior is a strong indication for transport dominated by Schottky barriers formed at the metal/$TiO_2$ interfaces that can be described by the following equation:[26]

$$I = AT^2 e^{-\frac{\Phi_{B0} - \alpha\sqrt{V}}{KT}}, \quad (1)$$

where $K$ is the Boltzmann constant, $T$ is the absolute temperature, $\Phi_{B0}$ is the zero bias potential barrier, $A$ includes the area and the Richardson constant, and $\alpha$ is the barrier lowering factor. To verify this, each branch of the I-V [1–4 in Fig. 3(a)] has been assessed independently following the temperature analysis discussed in Ref. 33. The signature plots (Fig. S2 in the supplementary material) lead to the estimation of the apparent barrier that results in the zero bias potential barrier (intercept) and the barrier lowering factor "$\alpha$" (slope) for each interface [Fig. 3(c)]. The Schottky barrier appears to change from 0.17 eV (branch 2) and 0.2 eV (branch 3) (HRS) to 0.1 eV (branch 4) (LRS) during switching. Moreover, all branches comply with the constant temperature signature plots. This provides strong evidence in support of an
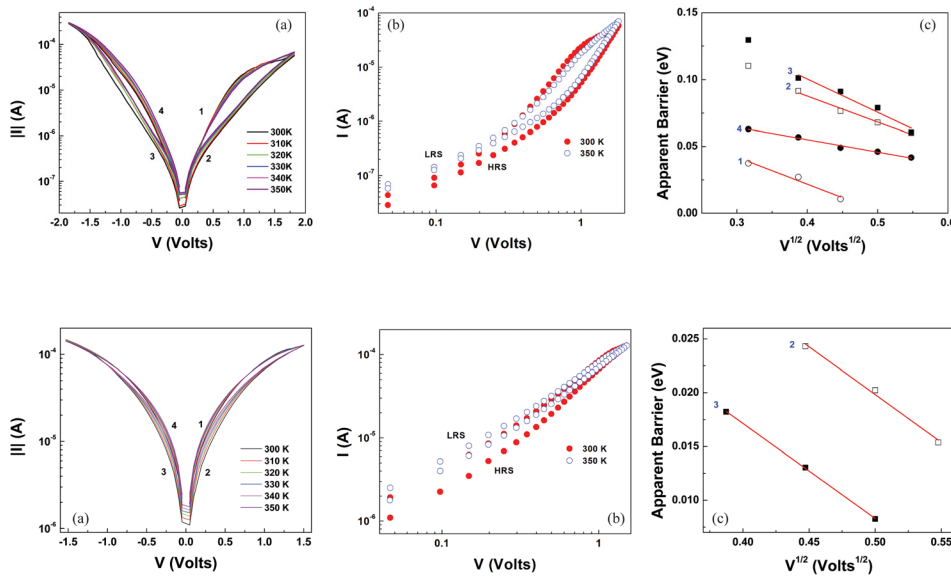
FIG. 3. I-V curves recorded at resistive level #1 and for the temperature range of 300 K–350 K (a). Apart from asymmetry, both HRS and LRS demonstrated thermally activated conductivity (b). Signature plots indicated interface controlled transport and allowed for the estimation of the interface barrier for each one of the I-V branches (c).
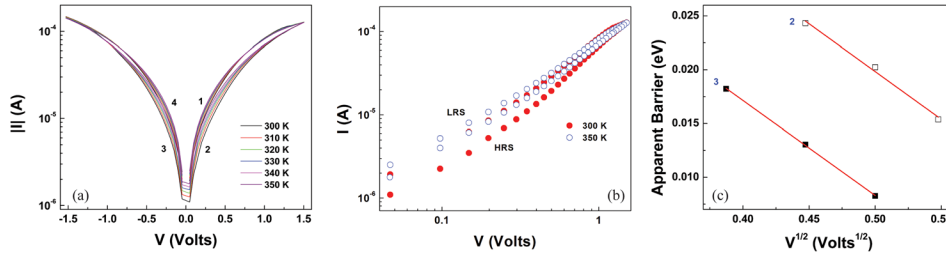


FIG. 4. I-V curves recorded at resistive level #2 and for the temperature range of 300 K–350 K (a). HRS demonstrated asymmetric thermally activated conductivity (b). The LRS showed similar but attenuated behavior with temperature. The HRS regime only allowed for the estimation of the interface barriers for branches (2–3) shown in the I-V branches (c).

interface controlled RS mechanism in the operation regime which corresponds to level #1.

Level #2 exhibits clear Schottky type characteristics in the HRS (Fig. 4), allowing for the calculation of the interface barrier [0.065 eV (branch 2) and 0.055 eV (branch 3)] through the corresponding analysis (Fig. S3 in the supplementary material). Regarding the LRS, this is found to be thermally activated [Fig. 3(b)], showing however very low asymmetry [for Fig. 2(b)], making it difficult to draw clear signature plots and thus calculating the barrier. Considering also the LRS characteristics of level #3, such a behavior can be interpreted as a boundary case at the transition between the two regimes, corresponding to a very low interface barrier.

Following from this, level #3 also demonstrates interface controlled transport for the HRS [Figs. 2(b) and 5 and Fig. S4 in the supplementary material], but the case is different for the LRS. The transport is then dominated by the core-film rather than the interfaces, as demonstrated by the highly symmetric [Fig. 2(b)] and practically temperature independent I-V curves [Fig. 5(b)]. In this case, where the I-V can be expressed as $I \sim V^{n+1}$, the conductivity is either ohmic ($n = 0$) or governed by space charge limited currents (SCLC). Considering also the temperature dependence, an ohmic conductivity should exhibit an Arrhenius type activation, whist the SCLCs typically show a very weak or a negligible temperature variation.[26] Based on the latter and despite the exponent value, in our case, we may conclude that

SCLCs are the most suitable mechanism to describe the conduction mechanism in this regime. Overall, at level #3, the transport switches from the interface to the core-material controlled mechanism which can be considered also as a form of interface controlled RS. Comparable operation was reported previously in similar devices that were electroformed using current compliance. This process leads them directly to resistance and switching characteristics corresponding to level #3. For these stacks, the X-ray absorption study did not reveal any structural changes during RS[30] which along with our temperature analysis further highlights the important role of the interfaces.

Thus, we may assume that our pulsing-based forming protocol progressively and gently modifies the interfacial barriers. These are further modulated during the I-V sweep by the bias induced charge (due redox processes, electronic trapping/de-trapping, and ionic motions), resulting in RS. The barrier in HRS reaching level #3 (below 20 kOhms, level #2 is considered as the boundary case) appears to be low enough so that the bias induced charge is sufficient to nearly eliminate it (thus, carriers may freely overcome it or to tunnel through it), and therefore, it is the core-film that determines the transport in the LRS.

The control of RS in interfacial RRAM devices by the Schottky barrier offers broad opportunities for optimization. This is because the macroscopically obtained resistance states could be considered as
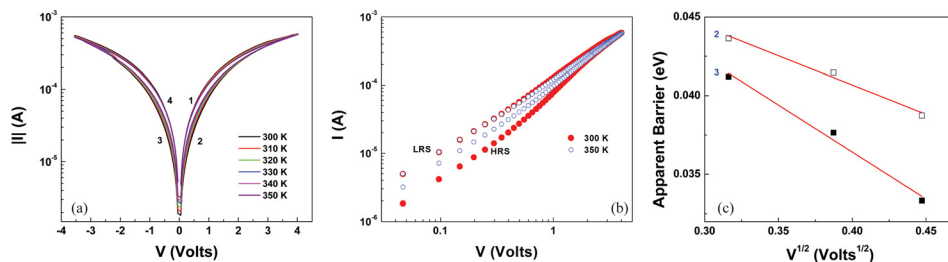


FIG. 5. I-V curves recorded at resistive level #3 and for the temperature range of 300 K–350 K. HRS demonstrated asymmetric thermally activated conductivity in contrast to the LRS that showed symmetric temperature independent behavior. Signature plots supported interface controlled transport for the HRS regime only and allowed for the estimation of the interface barrier for the I-V branches (2–3).

$$R = \frac{V}{I} \sim e^{\Phi_{APP}}. \tag{2}$$

For a conventional Si-based Schottky type contact, the barrier height $\Phi$ is determined by the metal work function, by the doping level, and by the total charge at the interface states and the depleted area ($W$).[26] For the case of metal-$TiO_2$ contact, we need to consider the metal electronegativity ($X_M$) instead of its work function[28,34] and the oxygen vacancies ($V_{ox}$) as equivalent to doping[35] and to bear in mind the important role of the interface states ($N_{it}$) as pointed out by recent reports[28,34] on partial Fermi pinning. Qualitatively, this can be expressed as

$$\Phi_{B0} \sim aX_M - \int_0^W bV_{ox}dx - \int_E^{E_f} cN_{it}dE, \tag{3}$$

where $a$, $b$, and $c$ are constants having the appropriate units and $E_f$ the Fermi level. Each of the terms in Eq. (3) highlights the directions towards resistive switching engineering in $TiO_2$ based devices. In particular, defect engineering could turn out to be of great interest along with establishing appropriate biasing schemes that may offer analog performance through bespoke modification of the interfacial barriers.

In summary, a detailed electrical characterization study of the conduction mechanism at different resistive levels of the Pt/$TiO_{2-x}$/Pt stack was presented. These levels were attained via a pulsing-based compliance-free forming protocol. The analysis of the temperature dependence for each branch of the I-V switching characteristics of the various resistive levels provides deeper insights into the underlying switching mechanism, and two major regimes were identified. For higher resistive levels, the transport in both HRS and LRS was found to be interface controlled. For the lower resistive level, the transport diverges from the interface to the core-material controlled mechanism for HRS and LRS, respectively. This study supports the argument that bespoke modification of the interface barrier can be obtained, rendering $TiO_2$ based RRAM as more suitable and reliable for emerging applications.

See supplementary material for the I-V curve of a pristine (pre-electroformed) device and for the signature plots supporting the conduction mechanisms discussed.

All data supporting this study are openly available from the University of Southampton repository at http://doi.org/10.5258/SOTON/D0657.

[1]C. Yoshida, K. Tsunoda, H. Noshiro, and Y. Sugiyama, Appl. Phys. Lett. **91**, 223510 (2007).

[2]M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, Nature **521**, 61 (2015).

[3]A. Serb, J. Bill, A. Khiat, R. Berdan, R. Legenstein, and T. Prodromakis, Nat. Commun. **7**, 12611 (2016).

[4]A. Mehonic and A. J. Kenyon, Front. Neurosci. **10**, 57 (2016).

[5]A. H. Edwards, H. J. Barnaby, K. A. Campbell, M. N. Kozicki, W. Liu, and M. J. Marinella, Proc. IEEE **103**, 1004 (2015).

[6]M. Zidan, Y. J. Jeong, J. H. Shin, C. Du, Z. Zhang, and W. Lu, "Field-programmable crossbar array (FPCA) for reconfigurable computing," IEEE Trans. Multi-Scale Comput. Syst. (published online).

[7]A. Khiat, P. Ayliffe, and T. Prodromakis, Sci. Rep. **6**, 32614 (2016).

[8]W. Kim, A. Chattopadhyay, A. Siemon, E. Linn, R. Waser, and V. Rana, Sci. Rep. **6**, 36652 (2016).

[9]S. Stathopoulos, A. Khiat, M. Trapatseli, S. Cortese, A. Serb, I. Valov, and T. Prodromakis, Sci. Rep. **7**, 17532 (2017).

[10]J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, Nat. Nanotechnol. **3**, 429 (2008).

[11]R. Waser and M. Aono, Nat. Mater. **6**, 833 (2007).

[12]A. Sawa, Mater. Today **11**, 28 (2008).

[13]I. Valov, Semicond. Sci. Technol. **32**, 093006 (2017).

[14]M. H. Lee, S. J. Song, K. M. Kim, G. H. Kim, J. Y. Seok, J. H. Yoon, and C. S. Hwang, Appl. Phys. Lett. **97**, 062909 (2010).

[15]A. Schönhals, C. M. M. Rosário, S. Hoffmann-Eifert, R. Waser, S. Menzel, and D. J. Wouters, Adv. Electron. Mater. **4**, 1700243 (2018).

[16]M. Lubben, P. Karakolis, V. Ioannou-Sougleridis, P. Normand, P. Dimitrakis, and I. Valov, Adv. Mater. **27**, 6202 (2015).

[17]H. Y. Jeong, J. Y. Lee, and S. Y. Choi, Adv. Funct. Mater. **20**, 3912 (2010).

[18]U. Celano, J. Op De Beeck, S. Clima, M. Luebben, P. M. Koenraad, L. Goux, I. Valov, and W. Vandervorst, ACS Appl. Mater. Interfaces **9**, 10820 (2017).

[19]Y. H. Do, J. S. Kwak, Y. C. Bae, J. H. Lee, Y. Kim, H. Im, and J. P. Hong, Curr. Appl. Phys. **10**, e71 (2010).

[20]P. Bousoulas, I. Michelakaki, and D. Tsoukalas, Thin Solid Films **571**, 23 (2014).

[21]X. Cao, X. M. Li, X. D. Gao, Y. W. Zhang, X. J. Liu, Q. Wang, and L. D. Chen, Appl. Phys. A: Mater. Sci. Process. **97**, 883 (2009).

[22]D. S. Jeong, H. Schroeder, and R. Waser, Phys. Rev. B **79**, 195317 (2009).

[23]E. Hernández-Rodríguez, A. Márquez-Herrera, E. Zaleta-Alejandre, M. Meléndez-Lira, W. D. La Cruz, and M. Zapata-Torres, J. Phys. D: Appl. Phys. **46**, 045103 (2013).

[24]G. Sassine, S. La Barbera, N. Najjari, M. Minvielle, C. Dubourdieu, and F. Alibart, J. Vac. Sci. Technol. B **34**, 012202 (2016).

[25]S. Srivastava, J. P. Thomas, N. F. Heinig, and K. T. Leung, ACS Appl. Mater. Interfaces **9**, 36989 (2017).

[26]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons, 2006).

[27]A. Serb, A. Khiat, and T. Prodromakis, Nat. Commun. **9**, 2170 (2018).

[28]L. Michalas, A. Khiat, S. Stathopoulos, and T. Prodromakis, J. Phys D: Appl. Phys. **51**, 425101 (2018).

[29]A. Khiat, S. Cortese, A. Serb, and T. Prodromakis, Nanotechnology **28**, 025303 (2017).

[30]D. Carta, G. Mountjoy, A. Regoutz, A. Khiat, A. Serb, and T. Prodromakis, J. Phys. Chem. C **119**, 4362 (2015).

[31]R. Berdan, A. Serb, A. Khiat, A. Regoutz, C. Papavassiliou, and T. Prodromakis, IEEE Trans. Electron Devices **62**, 2190 (2015).

[32]L. Pintilie, I. Vrejoiu, D. Hesse, G. LeRhun, and M. Alexe, Phys. Rev. B: Condens. Matter Mater. Phys. **75**, 104103 (2007).

[33]L. Michalas, M. Trapatseli, S. Stathopoulos, S. Cortese, A. Khiat, and T. Prodromakis, IEEE Trans. Nanotechnol. **17**, 867–872 (2018).

[34]N. Zhong, H. Shima, and H. Akinaga, Appl. Phys. Lett. **96**, 042107 (2010).

[35]V. C. Anitha, A. N. Banerjee, and S. W. Joo, J. Mater. Sci. **50**, 7495 (2015).