Novel electronic packaging method for functional electronic textiles

Menglong Li, John Tudor, Jingqi Liu, Russel Torah, Abiodun Komolafe and Steve Beeby

***Abstract*—A novel packaging method that enables the reliable mounting and protection of bare die within a textile yarn has been investigated. The reliability of electronic textiles is highly challenging given the flexibility of the fabric and the rigours of typical applications. Achieving reliable operation requires novel packaging approaches. In order to maximize the reliability and to minimize stresses in the electronic package, the die should be located as close as possible to the neutral axis of the packaged assembly. The die is bonded to a bottom Kapton substrate which contains patterned conductive interconnects and bond pads forming the functional circuit. The circuit is protected by a moulded Kapton film that has recesses formed where the die is located. This approach has been compared with three other traditional packaging technologies during washing, twisting and cyclical bending tests. The novel electronic packaging method shows the best performance in all tests surviving up to 45 wash cycles.**

***Index Terms*— electronic textile, flexible electronic packaging, washing, twisting and cyclical bending experimental test.**

I. Introduction

Electronic textiles (e-textiles) are fabrics with electrical interconnections and electronic devices embedded in them [1]. The functionality of e-textiles include sensing, data processing, communication, actuation, storage and heating [2, 3]. The concept of combining textiles with electronic functionality is not new and many examples of the technology have been demonstrated. Early medical sensing vests, for example, incorporated knitted electrodes for ECG monitoring and piezoresistive motion detection [4]; sweat monitoring sensors were also located in a silicone patch that was subsequently mounted on the textile [5]. However, electronics functionality was provided by conventional printed circuit board (PCB) modules located in pockets and connected by cables. Commercial electronic textiles offer similarly limited integration of the electronic circuit functionality within the textile. The limitation of rigid electronics in flexible applications was addressed in part by the FP7 project STELLA. This project developed stretchable meandering copper interconnections and embedded ultra-thin silicon die in silicone [6]. These stretchable circuit boards still contain rigid islands and have to be subsequently attached to textiles and the use of silicone reduces the breathability of the textile. Recently, there has been increased research interest in embedding bare die in textiles to achieve low-cost and flexible e-textiles [7]. Several approaches for embedding components have been demonstrated. For example, Zysset et al. used unpackaged bare die instead of packaged electronic components in an electronic textile to increase flexibility [8]. The surface area of the bare die is less than that of small outline integrated circuits (SOIC) or larger packaged electronic components. Therefore, when incorporated into a fabric there is less impact on the flexibility and feel of the e-textile. The researchers from ETH Zurich demonstrated the weaving of circuits into fabric. In this project [9], they fabricated a 4.5 × 10 cm textile containing five e-stripe yarns with 1 – 3 bare die sensor ICs on each e-stripe, resulting in a total of 10 sensors in the textile [9]. It was claimed that this e-textile will be both flexible and stretchable, but, with the ICs mounted onto a polyimide substrate and encapsulated basing glob topping, robustness would appear to be a concern. In tests, they found that the contacts between the ICs and the e-strip were able to withstand shear forces of at least 20 N, and bending rigidity was increased by 30% compared to a textile solely consisting of textile threads [9]. The work used standard die sizes and thicknesses leading to large bumps in the textile. In these examples, the bare die is not located within the core of the yarn which provides added mechanical protection and the ability to withstand washing was not investigated.

This paper focuses on realizing a reliable electronic packaging method for die mounted onto a flexible circuit using flip-chip bonding [10]. The novel electronic bare die in plastic package (EDIP) is shown schematically in Figure 1. The package comprises six layers which are: top moulded Kapton cover, top adhesive, embedded silicon die, adhesive under-fill, conductive adhesive/ solder and Kapton substrate layer with conductive tracks. The flexible circuit is in the form of a long and very thin strip as shown in Figure 2. In further investigation, this flexible circuit strip can be surrounded by textile fibres and connected to conductive wires to form an electronic yarn as shown in Figure 2. Reliability, washability and flexibility are essential factors to achieve a durable practical wearable e-textile [11]. The novel EDIP package described in this paper aims to maximize the reliability, flexibility and the washability of the overall

assembly compared with three other electronic packaging approaches. The three alternative packaging approaches are:

- Type 1: mount die on the Kapton substrate using conductive adhesive without under-fill,
- Type 2: mount die on the Kapton substrate using conductive adhesive and under-fill,
- Type 3: mount die using conductive adhesive, under-fill and glop-top adhesive to cover die.

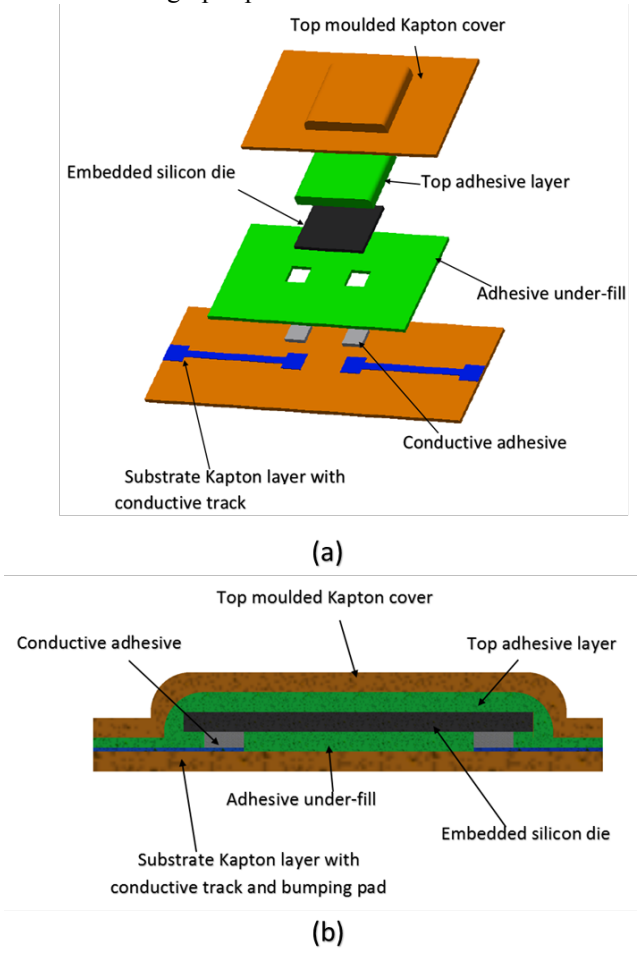


Figure 1. Schematic of novel packaging method for a two contact test chip, (a) six layers comprising the EDIP package, (b) cross-section of EDIP package.

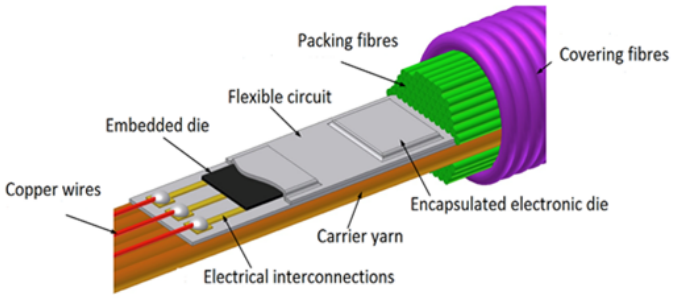


Figure 2. Schematic of proposed e-yarn structure and cut away showing the embedded die.

Section two of this paper introduces the EDIP die package in more detail including the materials used. The experimental methods for testing the packaged electronic die are presented in section three. Section four discusses the washing, twisting and cyclical bending test results and compares the four electronic assembly methods. The bending simulation for type 3 and EDIP packaging method are described in section five to prove bending experiment results. Finally, section five presents the conclusions.

II. Electronic Packaging Method and Materials

Figure 1(b) shows an idealized cross-section through the die which has been completely encapsulated using a thin top Kapton layer. In order to minimize the stresses and thereby increase reliability, the die should be located as close as possible to the central axis of the overall assembly. The non-conductive adhesive is injected into the empty space between die and substrate to act as under-fill. Under-fill is used in standard electronic die packaging to increase the mechanical reliability by providing additional mechanical support, reduce thermal stresses caused by the thermal expansion coefficient mismatches between the silicon die and the substrate and improve the ability to withstand mechanical shocks [12]. Circuits were assembled using flip chip bonding, which is a widely-used method of bonding an electronic die to a substrate or package carrier [13]. Conductive adhesives or solder bumps formed on the chip pads on the top side of the wafer can be used to electrically connect the die to a substrate with the bumped die area placed facing downward [14]. The test results of the EDIP packaging have been compared to type 1, 2 and 3 packaging assemblies which are shown schematically in Figures 3, 4 and 5.

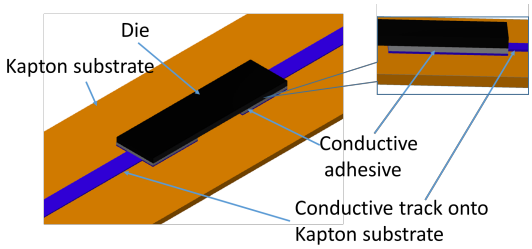


Figure 3. Type 1: Die mounted on the Kapton substrate using conductive adhesive without under-fill.

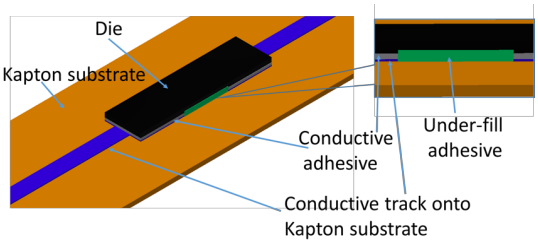


Figure 4. Type 2: Die mounted on the Kapton substrate using conductive adhesive and under-fill.

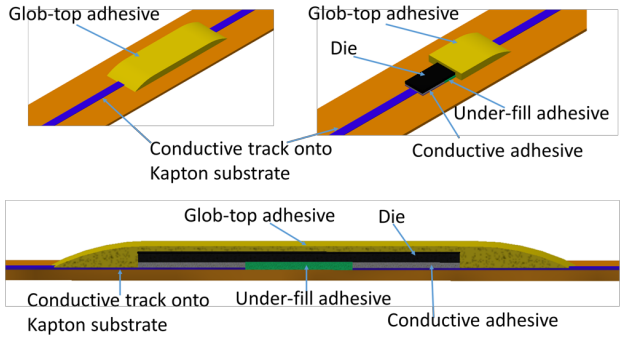


Figure 5. (a) Type 3: Mount die using conductive adhesive, under-fill and glop-top adhesive to cover die, (b) cut away type 3 package showing the embedded electronic die, (c) schematic cross section through type 3 package.

In the EDIP package (as shown in Figure 1), the top Kapton cover has the same thickness as the Kapton substrate and the thickness of the under-fill and top adhesive layer is identical in order to form a symmetrical assembly and locate the die on the neutral axis of the EDIP package.

The photograph of the EDIP packaged strip test circuit is shown in Figure 6(a) containing one packaged die. Figure 6(b) is a scanning electron microscope (SEM) photo of a cross section of the assembly that clearly shows the layers of the EDIP package and the symmetrical configuration.

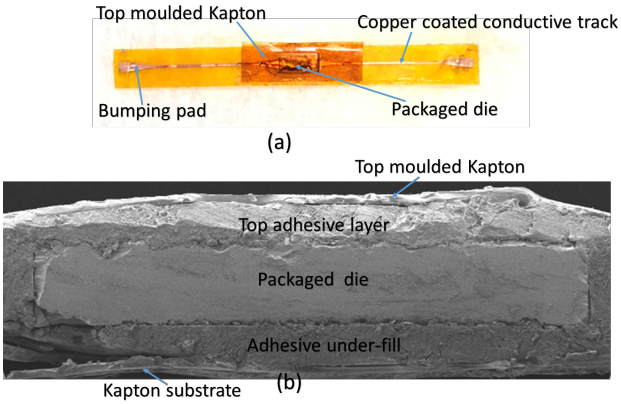


Figure 6. (a) Electronic strip with one packaged electronic die, (b) SEM photo in the cross-section to show all layer of EDIP package.

A die size of 2 mm x 1 mm x 0.1 mm has been used for all experiments, these were mounted using silver conductive adhesive with a 50 g weight used to provide a constant pressure to the chip after placing the chip on the substrate. Stainless steel test chips were used in this investigate since they can be used to form a basic conductive test circuit for exploring durability. Changes to the die interface will cause an increase in the resistance of the circuit with total failure being indicated by an open circuit condition. A Kapton substrate of dimensions 80 mm x 3 mm x 0.05 mm was used for all four packaging methods. The EP37-3FLF under-fill adhesive was used in type 2, type 3 and EDIP packages. The adhesive and substrate materials used have been previously identified as an optimum combination under shear and bending loads [10]. The properties of the under-fill adhesive, Kapton substrate, conductive adhesive and glob-top adhesive materials are given in Table I.

TABLE I
THE PROPERTIES OF MATERIALS USED FOR ALL PACKAGING METHOD [15-18]

Materials	Young's Modulus (MPa)	CTE (k^{-1})	Density (gcm^{-3})	Tensile Strength (MPa)
Under-fill adhesive (EP37-3FLF)	344	0.00009	1.05	35
Substrate (Kapton)	2500	0.00002	1.42	231
Conductive adhesive (RS1863616)	760	NA	1.9	<13.7
Glob-top adhesive(EC-9519)	317	0.000069	0.96	<30

The conductive adhesive is a two part thermosetting material with an epoxy resin adhesive base which contains silver flakes. The manufacture's datasheet only quotes joint strength and density of the conductive adhesive.

A. Two types Kapton substrate with circuit

Two types of metallisation were evaluated for the fabrication of the Kapton test circuit used for all four packaging methods: a screen printed silver polymer and adhesively bonded copper. Figure 7 shows the screen printed silver polymer circuit. The bonding of electronic components onto printed inks using solders can be challenging due to the temperature of the soldering process (typically 150-350°C). In contrast, components can be attached routinely using conductive adhesives. As circuit complexity increases, the required feature size shrinks beyond the limits of standard screen printing (around 0.1 mm) [19], but this approach is fine for the basic circuit design used here since the minimum feature size required for the silver polymer is 0.2 mm.

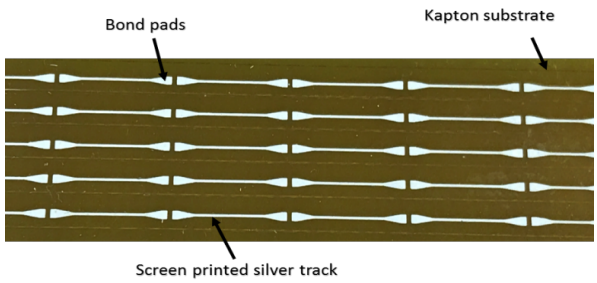


Figure 7. Screen printed silver polymer circuit onto Kapton substrate for five chips test.

Figure 8 shows the copper circuit substrate formed using commercial copper clad Kapton sheets. The circuit was patterned using a wet copper etch and a resist masking layer. The AZ9260 positive photoresist was spin coated for 30 seconds and oven baked for 3 minutes at 110 °C. An EVG 620T contact mask aligner was used to expose the resist and AZ400K developer with water in a 1:4 solution used to remove the exposed resist. The PCB etch crystal solution (Sodium Peroxidsulfate) was used to remove the exposed copper forming the tracks shown in Figure 8.

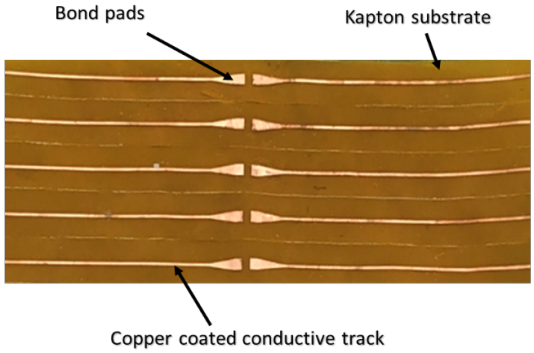


Figure 8. Copper coated circuit onto Kapton substrate for single chip test.

The two types of Kapton circuit without chips were experimentally compared in a wash test. The circuit substrates were sewn on to a T-Shirt and placed in a standard household washing machine using a 41 minutes, 30 °C wash cycle including a spin dry at 900 rpm. The resistance of the screen printed silver polymer conductive track was found to significantly change from 2 Ω to 38 Ω after 20 wash cycles, whereas the copper tracks were unaffected. Copper coated Kapton circuits where therefore used throughout the remainder of this investigation.

B. Fabrication process for deformed Kapton cover

In order to achieve the symmetrical assembly shown in Figure 1(b), a moulding process has been used to form a recess in the top Kapton film into which the die is located. Heating it up can soften the Kapton and a series of experiments were performed to determine the minimum temperature and time to deform different Kapton thicknesses (0.025 mm, 0.05 mm, 0.075 mm and 0.125 mm). For this work 0.05 mm thick Kapton was used to match the thickness of the substrate since a 0.05 mm thick Kapton substrate was previously identified as the optimal thickness under bending and shear tests [10]. The moulding process for 0.05 mm thick Kapton requires a minimum temperature of 360 °C applied for 60 seconds.

Figure 9(a) shows the jig used to deform the top Kapton film. The strip width was 7 mm and a round centre feature with a radius of 7 mm was initially included to compensate for any shrinkage and narrowing of the Kapton during the moulding process. At the centre of the circular feature is the rectangular recess with dimensions of 10.1 mm x 5.1 mm x 0.3 mm forming one half of the mould. The top part of the jig matches the bottom with a rectangular flange to fit in the recess in the bottom part of the jig with dimensions of 10 mm x 5 mm x 0.2 mm.

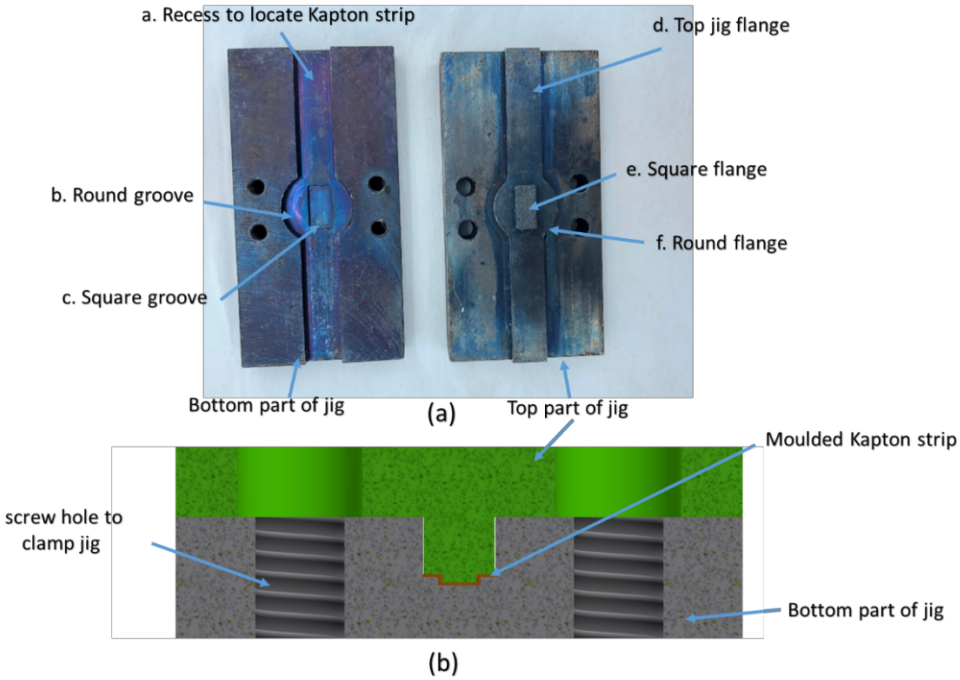


Figure 9. (a) Jig used to deform top cover Kapton for packaging single chip, (b) schematic cross-section of two part jigs with a moulded Kapton strip.

Figure 9(b) shows the cross-section of the jig assembly with a moulded Kapton strip. During initial tests the circular part of the Kapton strip was compared before and after moulding to measure the degree of shrinkage. Figure 10(a) shows the circular feature of Kapton film has a diameter of 14.38 mm before moulding, and Figure 10 (b) shows the circular feature of the moulded Kapton film has shrunk to 14.27 mm. This comparison indicates that there is only a small degree of shrinkage and this is not enough to be a concern. Therefore the circular feature was not included in later designs.

Different circuit designs will require a corresponding jig to match component location. Figure 11 shows a more complex jig used to deform Kapton to packaging an electronic circuit that contains multiple electronic chips.

Figure 10. The diameter of circular feature for a Kapton film (a) before moulding and (b) after moulding.

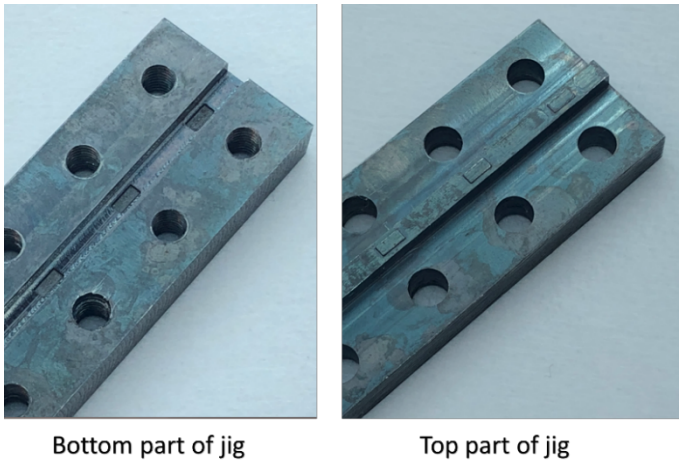


Figure 11. Jig used to deform Kapton for packaging multiple chip.

III. Experimental Methods

The three test methods used were washing, twisting and cyclical bending which represent the stresses experienced in typical applications of wearable electronic. Further test determining reliability to other typical textile processes such as ironing, tumble drying and dry cleaning are beyond the scope of this work. For the wash test, the packaged circuits were attached to a woven textile using overstitching (or couching), as shown in Figure 12. Each Kapton strip contained one test die for all samples. The test die formed a conductive path that bridges the gap in the test circuit. All wash tests used a 41 minutes cycle at 30 °C including a 4 minute spin dry at 900 rpm and 20 mL of laundry detergent is used for each wash cycle. After each washing cycle, the tested sample was hung to dry at room temperature.

The cyclical twist test involved a repeated 180° twist to replicate the type of strain that could be experienced in use. Figure 13 shows the PROWHITE twist tester which provided 180° twisting at a controlled twisting speed of 9.09 cycles/sec. Two clamps were used to fix the circuit strip with the die being located 50 mm away from right twist clamp as shown in Figure 13. A copper wire was soldered to each end of the electronic strip to enable the resistance to be continuously monitoring during the test using a multimeter.

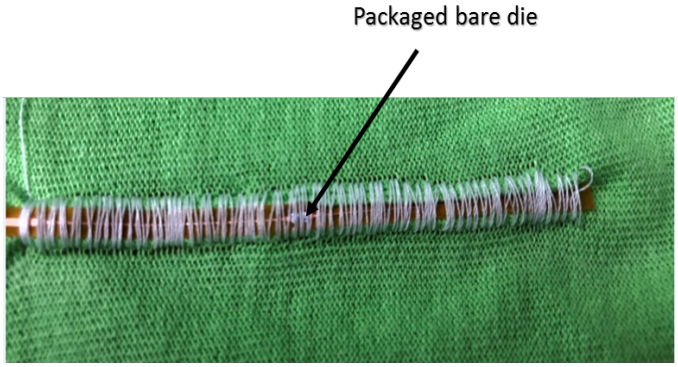


Figure 12. Packaged electronic strip knitted to the textile.

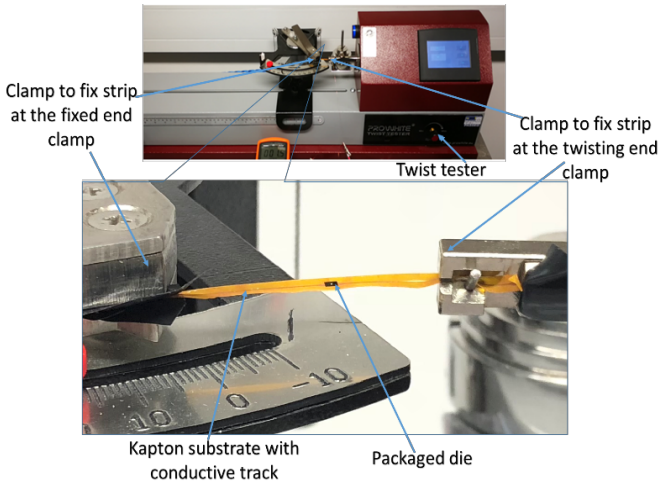


Figure 13. PROWHITE twist tester with two clamps to fixed electronic strip.

Cyclical bending was used to replicate bending forces commonly encountered in textile processes (e.g. knitting) and the bending test rig is shown in Figure 14. The electronic strip was clamped at the top end and during the test the clamp moves back and forth a distance of 30mm with a 200 g weight attached to the other end of the test strip to keep it in tension.

The circuit passes around a roller of radius 3.5 mm. A multimeter was connected to the electronic strip in parallel to measure the resistance of the strip.

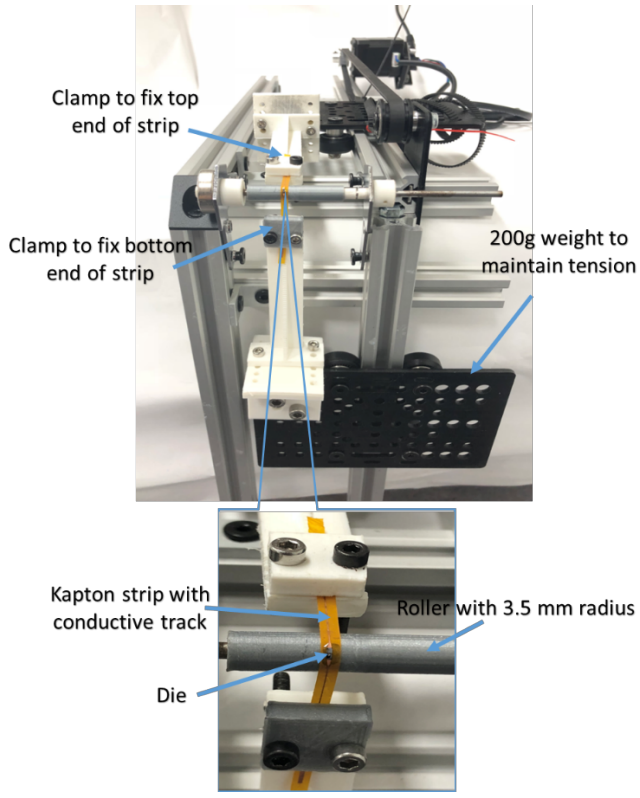


Figure 14. A bending test rig used for cyclical bending tester.

IV. Experimental Results

Table II shows the washing test results for five type 1 samples. Before washing all the samples had resistances in the range of 2.3 Ω to 13.4 Ω. The difference in the measured resistance across the five samples is due to variations in the amount of conductive adhesive and the thickness of the cured joints. The resistance of the five samples increased by 5 to 25 times after the first wash cycle. Samples 1, 3, and 5 failed after the second wash cycle, and samples 2 and 3 failed after the third washing cycle. All samples fail because the conductive adhesive delaminates at one or both ends as shown in Figure 15.

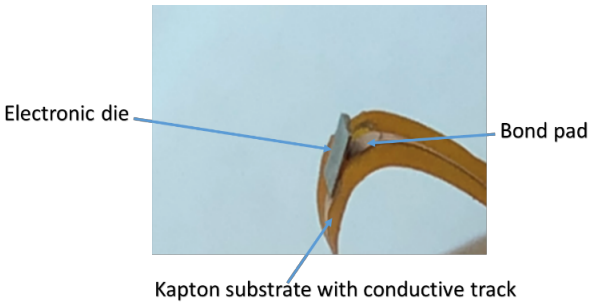


Figure 15. Conductive adhesive failure at one end between the electronic die and the contact pad on Kapton.

TABLE II
WASHING TEST RESULT FOR TYPE 1 PACKAGING METHOD

Sample	Resistance (R) before wash (Ω)	R after 1st wash cycle(Ω)	R after 2nd wash cycle(Ω)	R after 3rd wash cycle(Ω)
1	12.5	48	Fail[a]	
2	2.5	57	72	Fail[a]
3	13.4	136	Fail[a]	
4	4.8	154	168	Fail[b]
5	2.3	43	Fail[a]	

Fail[a] indicates a failure at one end only.
Fail[b] indicates a failure at both ends.

Table III. The type 2 samples had resistances in the range of 1.2 Ω to 5.7 Ω and these increased by 70% to 200% after the 1st wash cycle. Sample 5 failed after the 3rd wash cycle, samples 1, 2 and 3 failed after the 4th washing cycle, whilst the resistance of sample 4 increased to 2600 Ω.

Table IV shows washing test results for five type 3 samples that had initial resistances in the range of 1.0 Ω to 23 Ω. The resistance increased by 20% to 50% after the 1st wash cycle, and by 3 to 60 times after the 5th wash cycle. All samples survived at least 18 washing cycles with sample 2 failing after the 19th wash cycle, sample 3 failed after the 24th wash cycles and sample 4 failed after the 27th wash cycles.

TABLE III
WASHING TEST RESULT FOR TYPE 2 ELECTRONIC PACKAGING METHOD

Sample	Resistance (R) before wash(Ω)	R after 1st wash cycle (Ω)	R after 2nd wash cycle (Ω)	R after 3rd wash cycle (Ω)	R after 4th wash cycle (Ω)
1	1.2	3.5	225	614	Fail[a]
2	3.4	6.4	238	783	Fail[b]
3	3.3	6.9	195	642	Fail[a]
4	2.2	3.7	76	394	2600
5	5.7	7.5	1500	Fail[a]	

Fail[a] indicates a failure at one end only.
Fail[b] indicates a failure at both ends.

The washing test results for five EDIP package samples are shown in Table V. The initial resistances were in the range of 1.0 Ω to 28.6 Ω, which increased by 10% to 30% after the 1st wash cycle, and by 2 to 16 times by the 5th wash cycle. All samples survived at least 39 wash cycles, with sample 5 failing after the 41st cycle. Sample 3 failed after the 42nd and sample 4 failed after the 44th wash cycles. Sample 2 has the longest life and survived 45 wash cycles. Compared with the type 1, 2 and 3 packages, the EDIP performed the best in the washing test.

TABLE IV
WASHING TEST RESULT FOR TYPE 3 ELECTRONIC PACKAGING METHOD

Sample	R(Resistance) before wash(Ω)	R after 1st wash cycle(Ω)	R after 5th wash cycle(Ω)	R after 10th wash cycle(Ω)	R after 15th wash cycle(Ω)	R after 20th wash cycle(Ω)	R after 25th wash cycle(Ω)	R after 27th wash cycle(Ω)
1	23	26.5	86	268	2300	Fail[a] after 18th cycles		
2	2.7	3.2	37	68	1310	Fail[a] after 19th cycles		
3	21	23	73	263	1530	2610	Fail[b] after 24th cycles	
4	1.0	1.5	62	79	522	638	4150	Fail[a]
5	13	18	114	365	3200	Fail[b] after 18th cycles		

Fail[a] indicates a failure at one end only.
Fail[b] indicates a failure at both ends.

TABLE V
WASHING TEST RESULT FOR EDIP ELECTRONIC PACKAGING METHOD

Sample	R (Resistance) before wash(Ω)	R after 1st wash cycle (Ω)	R after 5th wash cycle (Ω)	R after 10th wash cycle (Ω)	R after 15th wash cycle (Ω)	R after 20th wash cycle (Ω)	R after 25th wash cycle (Ω)	R after 30th wash cycle (Ω)	R after 35th wash cycle(Ω)	R after 40th wash cycle(Ω)	R after 50th wash cycle(Ω)
1	28.6	32.1	46	134	175	221	276	321	432	Fail[a] after 39th cycle	
2	1.0	1.3	17	23	31	37	49	83	103	853	Fail[b] after 46th cycle
3	2.7	2.8	26	30	38	47.3	65	105	168	1690	Fail[b] after 42nd cycle
4	1.6	2.2	23	45	53.4	63	78.5	98	143	1235	Fail[a] after 44th cycle
5	14.7	18.6	34	82	128	145	178.5	196	245	4200	Fail[a] after 41st cycle

Fail[a] indicates a failure at one end only.
Fail[b] indicates a failure at both ends.

TABLE VI
TWISTING TEST RESULT FOR TYPE 1 AND 2 PACKAGING METHOD

Sample	R(resistance) before test (Ω)	R after 100 cycles (Ω)	R after 1000 cycles (Ω)	R after 5000 cycles (Ω)	R after 10000 cycles (Ω)	R after 15000 cycles (Ω)	R after 20000 cycles (Ω)	R after 30000 cycles (Ω)	R after 35000 cycles (Ω)
1 (Type 1)	8.1	10.2	63.2	Fail[a]					
2 (Type 1)	6.3	7.4	58.4	Fail[a]					
3 (Type 1)	1.5	1.8	33	Fail[a]					
4 (Type 1)	3.1	5.4	36.8	Fail[a]					
5 (Type 1)	10.5	13.6	89.2	Fail[a]					
1 (Type 2)	1.5	1.6	2.3	40.2	83	138	206	516	Fail[a]
2 (Type 2)	10	11.7	14.2	68.3	109	164.9	365	735	Fail[a]
3 (Type 2)	2.0	2.1	3.0	52	102	153.3	268	415	6300
4 (Type 2)	1.2	1.6	2.6	46.3	96.5	142.1	232	643	Fail[a]
5 (Type 2)	4.2	4.8	6.9	63.2	112.7	187.5	394	982	Fail[a]

Fail[a] indicates a failure at one end only.

Five samples for each package type were twist tested. Table VI shows the twist test results for the type 1 and 2 samples. The resistance of the five type 1 samples increased by 15% to 80% after 100 twisting cycles and further increased by a factor of 8 to 32 times after 1,000 twisting cycles. All type 1 samples electrically fail after 5,000 twisting cycles. These samples failed because the electrical connection at the twisting end breaks.

The resistance of the five type 2 samples increased by 8% to 20% after 100 twisting cycles, and further increased by 50% to 150% after 1,000 twisting cycles. All samples failed after 35,000 twisting cycles. Table VII shows the twisting test results for the type 3 and EDIP packages. The resistance of the five type 3 samples increase by 10% to 25% after 1,000 twisting cycles, and further increased by a factor of 15 to 20 times after 150,000 twisting cycles. All EDIP package samples have small resistance change (< 5%) after 1,000 twisting cycles. The EDIP samples all survived 200,000 twisting cycles and the resistance only increased by a maximum factor of 10. The EDIP package exhibits the least change in resistance during the twist test indicating the conductive adhesive joints are well protected against twisting stresses.

Cyclical bending tests were also undertaken on five samples from each of the four package types. Table VIII shows the cyclical bending test results for the type 1 and 2 package. Initial resistances in the range of 3.7 Ω to 9.2 Ω for the type 1 samples, increased by 4 to 8 times after 10 bending cycles, and further increased by 40% to 100% after 20 bending cycles. All samples failed after 40 bending cycles. The resistance of the five type 2 samples increased by 80% to 220% after 10 bending cycles, and further increased by 20% to 90% after 20 bending cycles. Samples 4 and 5 failed after the 66th and 69th bending cycle respectively and all failed by the 74th bending cycle.

TABLE VII
TWISTING TEST RESULT FOR TYPE 3 AND EDIP PACKAGING METHOD

Sample	R(resistance) before test (Ω)	R after 1000 cycles (Ω)	R after 10000 cycles (Ω)	R after 30000 cycles (Ω)	R after 50000 cycles (Ω)	R after 70000 cycles (Ω)	R after 100000 cycles (Ω)	R after 150000 cycles (Ω)
1 (Type 3)	4.6	5.1	20	38	46	59	68	97
2 (Type 3)	4.0	4.3	16	37	43	56	64	84
3 (Type 3)	6.9	7.8	26	42	57	73	85	103
4 (Type 3)	9.7	11.5	32	53	61	82	96	112
5 (Type 3)	12.6	15.8	39	64	76	97	107	131
1 (EDIP)	4.9	5.1	6.8	15.4	26	32	36	42
2 (EDIP)	3.4	3.5	4.6	13.8	24.5	28.9	32	37
3 (EDIP)	2.5	2.6	3.2	12.9	20.6	26	29	33
4 (EDIP)	7.6	7.8	8.7	20	31	40	49	58
5 (EDIP)	13.1	13.3	14.8	23	36	44	51	74

TABLE VIII
CYCLICAL BENDING TEST RESULT FOR TYPE 1 AND 2 PACKAGING METHOD

Sample	R(resistance) before test (Ω)	R after 10th cycle(Ω)	R after 20th cycle(Ω)	R after 30th cycle(Ω)	R after 40th cycle(Ω)	R after 50th cycle(Ω)	R after 60th cycle(Ω)	R after 70th cycle(Ω)	R after 75th cycle(Ω)
1 (Type 1)	3.7	36	58.2	99	Fail[a] after 33th cycle				
2 (Type 1)	8.6	42.5	63	114	Fail[a] after 31th cycle				
3 (Type 1)	9.2	53	75.5	Fail[a] after 30th cycle					
4 (Type 1)	6.8	24.8	49	86.3	Fail[a] after 37th cycle				
5 (Type 1)	8.9	39	56	108	Fail[b] after 35th cycle				
1 (Type 2)	10.7	18.5	24.3	29.4	42.5	57.3	97.2	143	Fail[a] after 74th cycle
2 (Type 2)	4.2	14.1	21	28	35.4	43	84.1	136	Fail[a] after 72th cycle
3 (Type 2)	12.5	20.3	28.7	30.8	43.2	55.6	89	121	Fail[a] after 71th cycle
4 (Type 2)	8.2	17.6	23.9	31.4	49.8	58.7	107	Fail[b] after	

								66th cycle	
5 (Type 2)	14.3	29.6	36.8	42.3	53.1	64.8	123	Fail[a] after 69th cycle	

Fail[a] indicates a failure at one end only.
Fail[b] indicates a failure at both ends.

TABLE IX
CYCLICAL BENDING TEST RESULT FOR TYPE 3 AND EDIP PACKAGING METHOD

Sample	R(resistance) before test (Ω)	R after 10th cycle(Ω)	R after 100th cycle(Ω)	R after 500th cycle(Ω)	R after 1000th cycle(Ω)	R after 1300th cycle(Ω)	R after 1400th cycle(Ω)	R after 1500th cycle(Ω)
1 (Type 3)	6.8	7.5	18.6	92	Fail[a] at 812th cycle			
2 (Type 3)	3.1	4.3	10.6	59.8	Fail[a] at 913th cycle			
3 (Type 3)	2.7	3.6	9.1	53.2	Fail[b] at 981th cycle			
4 (Type 3)	5.2	6.1	15.7	74.1	Fail[a] at 886th cycle			
5 (Type 3)	4.3	5.7	13.5	68.3	Fail[a] at 946th cycle			
1 (EDIP)	1.7	1.8	4.9	23.8	64.3	97.5	Fail[a] at 1390th cycle	
2 (EDIP)	2.6	2.7	9.0	36	83.2	132	Fail[a] at 1348th cycle	
3 (EDIP)	1.6	1.8	3.6	27.1	68.6	102	Fail[a] at 1357th cycle	
4 (EDIP)	4.3	4.5	6.3	32.4	72.8	89.4	103	Fail[a] at 1470th cycle
5 (EDIP)	3.8	3.9	5.9	29.5	73.5	95.8	Fail[a] at 1364th cycle	

Fail[a] indicates a failure at one end only.
Fail[b] indicates a failure at both ends.

Table IX shows the cyclical bending test results for the type 3 and EDIP package. The resistance of the type 3 samples increased by 10% to 40% after the 10th bending cycle, and further increased by 120% to 160% after the 100th bending cycle. The five samples survived an average of 908 bending cycles. The cyclical bending test results for EDIP package shows that the resistance of all samples are increased by 5% to 15% after the 10th bending cycle, and by 15% to 80% after the 100th bending cycle. Compared to the type 3 package, the resistance of the EDIP samples increases at a lower rate. The five samples survived an average of 1386 bending cycles. The EDIP package offers the best performance in cyclical bending.

V. BENDING SIMULATION RESULTS

The three point bending simulations have been undertaken to determine the stresses at the conductive adhesive layer of packages since all samples fail because the conductive adhesive delaminates in the experiments. ANSYS Finite element analysis (FEA) has been used to perform the bending simulations. The 5N external bending force is applied in all simulations with a Kapton substrate of dimensions 80 mm x 3 mm x 0.05 mm and the stainless steel die size of 2 mm x 1 mm x 0.1 mm. The material properties used in the model are taken from the data sheets of the under-fill adhesive, conductive adhesive and glob-top materials used in the experimental work.

Figure 16 shows the shear and von-Mises stresses in the conductive adhesive layer for type 1 and 2 packaging method. Compared to type 1, the type 2 package shows better shear and von-Mises stress performance when a same external bending force applied.

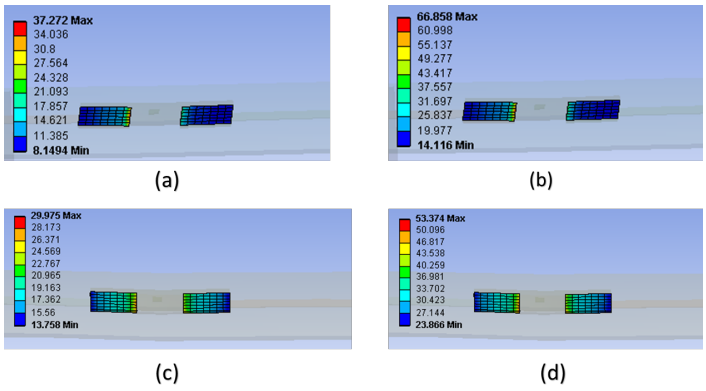


Figure 16. Shear and von-Mises stress simulations for type 1 and 2 packaging method, (a) shear stress in the conductive adhesive layer for type 1, (b) von-Mises stress in the conductive adhesive layer for type 1, (c) shear stress in the conductive adhesive layer for type 2, (d) von-Mises stress in conductive adhesive layer for type 2.

The shear and von-Mises stress simulation results for type 3 and EDIP package are shown in Figure 17 with the type 3 package shows better stress performance than the type 1 and 2 packages. The EDIP package shows the best stress performance. These simulations results indicate the stress induced in the conductive adhesive is lowest for the EDIP and this is consistent with its experimental performance. This validation exercise provides confidence in the experimental analysis and suitability of the EDIP packaging method.

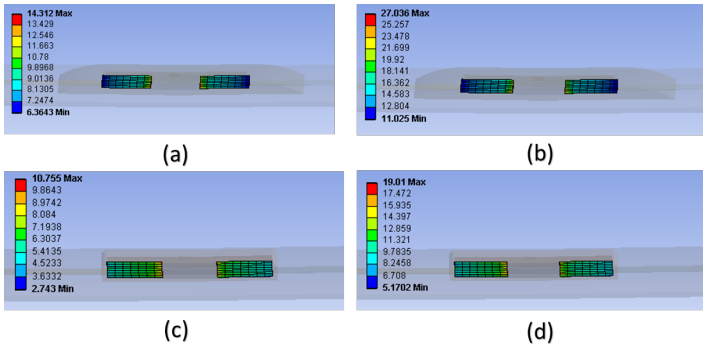


Figure 17. Shear and von-Mises stress simulations for type 3 and EDIP packaging method, (a) shear stress in the conductive adhesive layer for type 3, (b) von-Mises stress in the conductive adhesive layer for type 3, (c) shear stress in the conductive adhesive layer for EDIP, (d) von-Mises stress in conductive adhesive layer for EDIP.

VI. Conclusion

E-textiles in wearable applications are subject to human motion and as such the integrated electronic components can experience different kinds of stresses such as bending and twisting. The type 1 packaging approach performed the worst in all tests. Compared to the type 1 package, the type 2 package demonstrate improved durability which indicates the benefits of the additional under-fill. However the durability remains poor and this is significantly improved by the addition of the glob top encapsulation. Glob top encapsulation is simple to implement but the resulting mechanical assembly is difficult to control. The EDIP package provides a repeatable encapsulation method that can be designed to minimise stresses in the assembly. This is evidenced by the results presented here.

The failure of all EDIP samples in wash testing, twisting and cyclical bending caused by the failure of the conductive adhesive between die and substrate. Higher adhesion strength material, such as solder would further improve the reliability of the EDIP package. The failure of the chips occurs at the electrical connection and the reliability could be further improved by moving the neutral axis as close as possible to the chip/die interface. This would be done by thinner the moulded Kapton and thicker the substrate Kapton.

Acknowledgment

This research funded by Engineering and Physical Sciences Research Council project (EPSRC EP/M015149/1) “Novel manufacturing methods for functional electronic textiles (FETT)” https://www.fett.ecs.soton.ac.uk/. Thanks for Dorothy Hardy and Tilak Dias who helped with the twisting and cyclical bending machines. Data published in this paper are available from the University of Southampton repository at 10.5258/SOTON/D0691.

Reference

1. Martin, T., et al. *Modeling and simulating electronic textile applications*. in *ACM Sigplan notices*. 2004. ACM.
2. Curone, D., et al., *Smart garments for emergency operators: the ProeTEX project.* IEEE Transactions on Information Technology in Biomedicine, 2010. **14**(3): p. 694-701.
3. Stoppa, M. and A. Chiolerio, *Wearable electronics and smart textiles: a critical review.* Sensors, 2014. **14**(7): p. 11957-11992.
4. Paradiso, R. and D. De Rossi. *Advances in textile technologies for unobtrusive monitoring of vital parameters and movements*. in *Engineering in Medicine and Biology Society, 2006. EMBS'06. 28th Annual International Conference of the IEEE*. 2006. IEEE.
5. Coyle, S., et al., *BIOTEX—Biosensing textiles for personalised healthcare management.* IEEE Transactions on Information Technology in Biomedicine, 2010. **14**(2): p. 364-370.
6. Gonzalez, M., et al., *Design and implementation of flexible and stretchable systems.* Microelectronics Reliability, 2011. **51**(6): p. 1069-1076.
7. Rajoo, R., et al. *Embedding of 15um thin chip and passives in thin flexible substrate*. in *Electronics Packaging Technology Conference (EPTC), 2010 12th*. 2010. IEEE.

8. Zysset, C., et al. *Woven electronic textiles: An enabling technology for health-care monitoring in clothing*. in *Proceedings of the UbiComp*. 2010.
9. Zysset, C., et al., *Integration method for electronics in woven textiles.* IEEE Transactions on Components, Packaging and Manufacturing Technology, 2012. **2**(7): p. 1107-1117.
10. Li, M., et al., *Stress analysis and optimization of a Flip chip on flex electronic packaging method for functional electronic textiles.* IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018. **8**(2): p. 186-194.
11. Katragadda, R.B. and Y. Xu, *A novel intelligent textile technology based on silicon flexible skins.* Sensors and Actuators A: Physical, 2008. **143**(1): p. 169-174.
12. Chang, S., K.I. Loh, and E.S. Ibe. *Underfill and edgebond for enhancing of board level reliability (IMPACT)*. in *Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 9th International*. 2014. IEEE.
13. R.G. Werner, D.R.F., J.DeRose and E.Sorongon *Flip chip packaging.* International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces, Proceedings, 1999: p. 246-251.
14. Rinne, G.A. *Solder bumping methods for flip chip packaging*. in *Electronic Components and Technology Conference, Proceedings. 47th*. 1997.
15. Masterbond. *EP37-3FLF datasheet* https://www.masterbond.com/tds/ep37-3flf [cited 2016 May].
16. DUPONT. *Kapton Datasheet* http://www.dupont.com/products-and-services/membranes-films/polyimide-films/brands/kapton-polyimide-film.html/ [cited 2016 June].
17. RS. *Conductive Adhesive Epoxy datasheet*. https://uk.rs-online.com/web/p/conductive-adhesives/1863616/ [cited 2017 April].
18. ECM. *EC-9519 Datasheet* http://www.conductives.com/biosensors.php [cited 2017 July].
19. Hyun, W.J., et al., *Screen printing of highly loaded silver inks on plastic substrates using silicon stencils.* ACS applied materials & interfaces, 2015. **7**(23): p. 12619-12624.

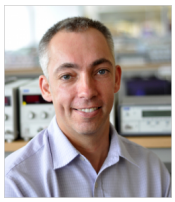
Menglong Li received the B.Eng. degree in electronic engineering from University of Southampton, Southampton, UK in 2014. He is currently pursuing the Ph.D. degree with the department of Electronic and Computer Science, University of Southampton, Southampton, UK. His current interests include wearable electronics, flexible electronic packaging method, screen printing, dispenser printing, ultra-thin chip fabrication, and reliability test of electronic packaging.

John Tudor received the Ph.D. degree in physics from the University of Surrey, Guildford, U.K. He is currently a Principal Research Fellow with the University of Southampton, Southampton, U.K. His current research interests include smart fabrics, screen printing, dispenser printing, MEMS, microsystems, energy harvesting, sensors, resonant sensors, inkjet printing, and wireless sensors.

Jingqi Liu received the B.Eng. degree in electronic engineering from University of Southampton, Southampton, UK in 2014. She is currently pursuing the Ph.D. degree with the department of Electronic and Computer Science, University of Southampton, Southampton, UK. Her current interests include printed electronics, Nano materials, thin film semiconductor devices and wearable electronics.

Russel Torah received the Ph.D. degree in electronics from the University of Southampton, Southampton, U.K., in 2004. He is currently a Senior Research Fellow with the University of Southampton. His current research interests include smart fabric development but he also has extensive knowledge of energy harvesting, sensors, and transducers.

Abiodun Komolafe received the PhD degree from University of Southampton, Southampton, UK in 2015. He is currently a Research Fellow with the University of Southampton. His current interests include ultra-thin chip fabrication, reliability test of electronic packaging and wearable electronics.



Steve Beeby received the Ph.D. degree from the University of Southampton, Southampton, U.K., in 1998. He is currently a Professor with the Department of Electronics and Computer Science, University of Southampton where he is Head of the Electronics and Electrical Engineering Group. He holds ten patents and has co-founded three companies. He has published 114 refereed journal papers and letters, 140 refereed conference papers, 5 review papers, 5 books, 11 chapters within books and he has an h-index of 43. His current research activities include e-textiles, energy harvesting and printed low temperature active materials for flexible and textile substrates.