UNIVERSITY OF SOUTHAMPTON

Single Electron Manipulation in Silicon Nanowires for Quantum Technologies

by

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A thesis submitted for the degree of Doctor of Philosophy
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ABSTRACT

FACULTY OF PHYSICAL SCIENCE AND ENGINEERING
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Doctor of Philosophy

by Zuo Li

A redefinition of the Ampere based on the quantum metrology triangle is required to improve the accuracy of the unit. The Si single electron pump is considered a promising candidate for the single electron source in the quantum metrology triangle due to its compatibility with the state-of-art CMOS manufacturing platform. However, the fabrication processes have not been fully established, and the performance impact factors and reliability of Si single electron pumps have not been fully addressed.

In this project, I successfully fabricated Si electron pumps with atomically flat surfaces, using the advanced facilities in Southampton Nanofabrication Centre. I observed current plateaus with the width of 18 meV and uncertainty of 0.828% when the single electron pump is operated at 125 MHz in the National Physical Laboratory, showing the possibilities for the applications of current calibration. The reliability issues were investigated by measuring Si quantum dot devices and the single electron pumps fabricated. The impact of charge traps in quantum devices were addressed by investigating the random telegraph noise in the devices. I demonstrated that the charge traps can impact the device reliability by resonant tunnelling, which will help scientists to understand further about the reliability impact factors of silicon quantum devices.

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Academic Thesis: Declaration Of Authorship

I, Zuo Li, declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research, *Single Electron Manipulation in Silicon Nanowires for Quantum Technologies*.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. Either none of this work has been published before submission, or parts of this work have been published as:

   Li, Z., Husain, M.K., Yoshimoto, H., Tani, K., Sasago, Y., Hisamoto, D., Fletcher, J.D., Kataoka, M., Tsuchiya, Y. and Saito, S., 2017. Single carrier trapping and de-trapping in scaled silicon complementary metal-oxide-semiconductor field-effect transistors at low temperatures. *Semiconductor Science and Technology*, **32(7)**, p.075001.

   Li, Z., Sotto, M., Liu, F., Husain, M.K., Yoshimoto, H., Sasago, Y., Hisamoto, D., Tomita, I., Tsuchiya, Y. and Saito, S., 2018. Random telegraph noise from resonant tunnelling at low temperatures. *Scientific reports*, **8(1)**, p.250.

   Li, Z., Sotto, M., Liu, F., Husain, M.K., Zeimpekis, I., Yoshimoto, H., Tani, K., Sasago, Y., Hisamoto, D., Fletcher, J.D. and Kataoka, M., 2017, February. Random-telegraph-noise by resonant tunnelling at low temperatures. In Electron Devices Technology and Manufacturing Conference (EDTM), 2017 IEEE (pp. **172-174**). IEEE.

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Chapter 1

Introduction

The accurate calibration is significant for the state-of-the-art industry, especially when more and more components are integrated into a product. The fundamental science associated with the accuracy and calibration is metrology. The concept of metrology is defined by the International Bureau of Weights and Measures (BIPM) as ***the science of measurement, embracing both experimental and theoretical determinations at any level of uncertainty in any field of science and technology***[1].

The classical metrology is based on SI (Le Systme International d'Units) units, which are considered as international standards worldwide[2]. SI units are established on the MKS system, in which metre, kilogram and second are considered as fundamental units to derive all other mechanical units[3]. However, some original definitions of these units limit the intrinsic achievable accuracy. For example, in 1956, the definition of second was initially based on the tropical year. The best accuracy ever achieved using this definition was only 1 ppm[4]. Today, with the help of quantum mechanics, the definition of second is based on optical atomic clock and the relative uncertainty is as small as 2.5×10^{-11}[5]. The accuracy has been improved by almost one million times compared with the original definition.

The electronic industries are basically based on the electricity. High resolutions of the electrical current are often required in the sensors to ensure the stability of the system. Therefore, calibration of ampere, the unit of electrical current, is very important. The definition of ampere is '***The ampere is that constant current which, if maintained in two straight parallel conductors of infinite length, of negligible circular cross section, and placed 1 metre apart in vacuum, would produce between these conductors a force equal to*** 2×10^{-7} ***newton per metre of length.[6]***' The classical realisation of this definition is by measuring forces between two conductive coils. There are many limiting factors that put caps on the accuracy, for example, the difficulty to calculate the actual distribution of current flowing through a wire with definite diameter. The best accuracy ever achieved so far with this conventional definition

was 0.3 ppm[7], which is far below the accuracy already achieved by the definition of second and metre, with the help of quantum mechanics.

As a result, scientists began searching for a new definition of ampere connecting to a natural constant. The idea is called quantum metrology, which is defined as ***'the study of making high-resolution and highly sensitive measurements of physical parameters using quantum theory to describe the physical systems, particularly exploiting quantum entanglement***[8]'. A natural idea is associating the current with the elementary charge. In the quantised current, integer number of electrons flow through a circuit in a certain period of time. As a result, quantised current source with high accuracy is required. One of the most attractive and promising quantised current sources is the single electron pump[9], which is modulated by an AC signal. In this device, only one single electron is pumped through the circuit within a period of tuning AC signal. There are mainly two kinds of single electron pumps, which are based on metallic island and semiconductor quantum dot respectively. Metallic single electron pump has been investigated since 1990s, and accuracy up to 0.02 ppm has been achieved[10]. However, it is extremely hard to achieve high current in metallic single electron pump because the operation frequency of adiabatic pumping is limited by the RC constant of the oxide tunnelling junctions. It is almost impossible to overcome the large RC time constants of the tunnelling junctions[11].

With non-adiabatic pumping, which is only achievable in semiconductor quantum dot pumps, it is possible to achieve high-speed operation to overcome this frequency limit. Due to the compatibility with the state-of-the-art CMOS fabrication platform, the Si single electron pumps have the potential to realise mass reliable fabrication and parallel operations to enhance the current. These advantages make the Si single electron pump be a promising candidate to achieve the quantum standard of ampere.

There are still many issues need to be solved to achieve the accurate quantum current source. Single electron transport can only be observed at cryogenic condition (usually below 20 K) in nano-scale structure (usually less than 100 nm), and high magnetic field (usually in the level of 10 T) is often required to achieve high accuracy[12]. The small scale induce challenges in the fabrication of single electron pumps, and the extreme operation environment makes the measurement difficult. Besides, the device physics to explain the transportation is still not very clear at the moment. Some models have been introduced, but the deviation still exists especially when the temperature is as low as 100 mK[13]. As a result, the performance limiting factor of Si single electron pumps has not been fully investigated yet. Much work is still required in this research field.

The aim of my PhD project is to understand the operation of single electron devices, learn the fabrication processes of the Si single electron pumps, and measure the pumps in National Physical Laboratory to address the reliability limiting factors of single electron pumps. Practically, I would like to

(a) Fabricate a batch of silicon single electron pumps, using the facilities from Southampton Nanofabrication Centre.

(b) Demonstrate a successful operation of the single electron pump, showing the ability for the device to calibrate the current.

(c) Understand the reliability impact factors of the silicon single electron pumps and other related silicon quantum dot devices.

In order to achieve this target, in my PhD project, I have read literatures to understand the operation of single electron transistors and previous work in single electron pumps by other groups, which are summarised in chapter 2. The fabrication of our single electron pump lot will be introduced in Chapter 3. I designed all the e-beam lithography masks for the single electron pumps, have successfully fabricated single electron pumps together with Dr. Muhammad Khaled Husain, the research fellow in our group, and tested the devices at room temperatures to analyse the yield. The measurement results of single electron devices are summarised in Chapter 4. I have measured some Si devices at low temperatures to investigate on the characteristics and performance limiting factor for the Si single electron devices based on quantum dots. I observed single electron transistor characteristics and current peaks in advanced conventional MOSFETs, and investigate on the current peaks observed in the experiment to study the impact of charge traps on the devices. I also measured our single electron pumps in NPL, and observed unstable single electron pump characteristics. I investigated on the spectrum of quantum dot and identified the impact of charge traps to understand the performance limiting factor in Si single electron pumps. Conclusions of the researches in my PhD study have been made in Chapter 5. Some of the work I have done, such as processes development, are introduced in the appendix.

In total, I have successfully fabricated Si single electron pumps, using the facilities in the University of Southampton Nanofabrication Centre. I have investigated on the characteristics and performance limiting factors in Si quantum dot devices, and the results were published in full article in *IOP Semiconductor Science Technology* and *Nature Scientific Reports*, respectively. Based on the knowledge obtained in these measurements and devices fabricated, I measured our single electron pumps in National Physical Laboratory, observed unstable pumping characteristics, and investigated the performance limiting factor in detail. The results have been summarised, and submitted for publication.

Chapter 2

Background Research

2.1 Quantum Metrology Triangle

In order to redefine ampere with the quantised single electron source, logically, existing ammeters cannot be used to calibrate the generated current. As a result, a null-current circuit is required. In the null-current circuit, I only use null-current detector to identify the presence of the current. Therefore, an accurate voltage source and a precise resistor are both mandatory for its realisation.

After both Josephson effect[14] and Quantum Hall effect[15] had been observed, people began to establish the practical realisation of the current redefinition. Likrahev and Zolin proposed an idea[16] to build a standard voltage source with the help of Josephson effect[17], calibrate an accurate resistor using Quantum Hall Effect[18], and use a single electron current source[19] with an error-counting scheme[20] in the null-current circuit in order to balance the current flowing through the accurate resistor. The idea was given the name of Quantum Metrology Triangle[21]. The schematic set-up of the quantum metrology triangle is shown in Fig. 2.1.

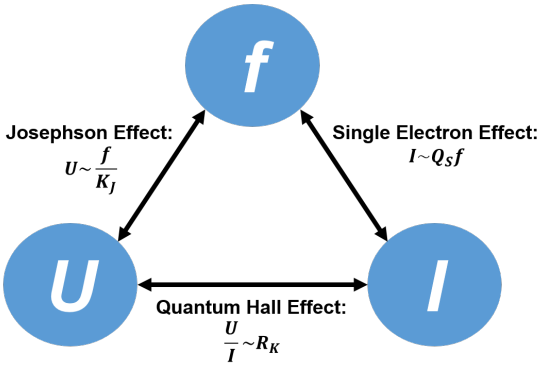

FIGURE 2.1: Schematic Diagram of Quantum Metrology Triangle. The links between the three parameters, frequency f, current I and voltage U are shown.

In order to realise this schematic set up, a practical circuit diagram is required. A typical circuit diagram of experimental quantum metrology triangle is shown in Fig. 2.2.

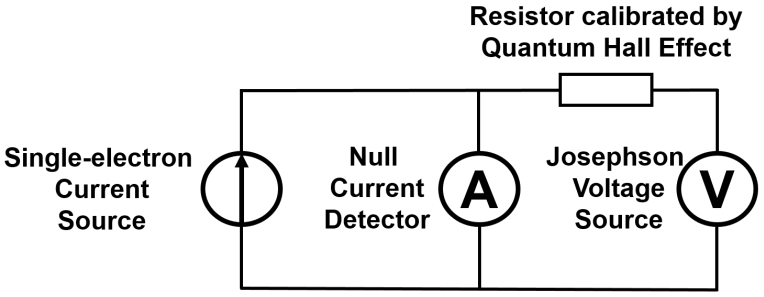

FIGURE 2.2: Quantum Metrology Triangle Experimental Set-up.

In this null-current circuit, the current generated by Josephson voltage source will be balanced by the single-electron current source. If there is no current flowing through the null-current detector, a balance is achieved, and I can establish the quantum standards of electrical units based on this circuit.

A practical issue with this design is the low current level of single-electron current source, which is usually ∼nA level in practical. It is normally not enough to balance the current generated by Josephson Voltage source (usually ∼mV) and a resistor with the exact quantum hall resistance(∼kΩ), which is about μA level. In order to solve the problem, a high-precision amplifier is used to enhance the current generated by single electron source[22, 23] or a larger cryogenic resistor calibrated by quantum hall resistance is required[24, 25].

In order to make the redefinition practical and reasonable, the single electron source need to reach two certain limits in accuracy and current level (equivalent to operation frequency):

(1) The error of the single-electron current source should be no more than 0.05ppm.

It is an agreement made by metrologists[26]. The definition of electric current should only be changed when the uncertainty of one parameter in quantum metrology triangle is less than 0.02 ppm and the rest two are less than 0.05 ppm. Since the uncertainty in Josephson voltage source and Quantum Hall Resistance have both met the requirement of 0.02 ppm, the uncertainty in single-electron current source, therefore, should be less than 0.05 ppm.

(2) The current level of current source should be at least in the magnitude of 100 pA, i.e., the pump must be able to operate with gigahertz-level frequency.

The level of current generated by single-electron source should be large enough, so that the Johnson Noise[27] (coming from thermal agitation of charge carriers) would not have significant impact on the measurement result.

Idefine the total current as I_S. The error created by Johnson Noise, δI_S, can be expressed by

$$\delta I_S = \sqrt{\frac{4k_B T}{tR}}, \tag{2.1}$$

where T is the ambient temperature, k_B is the Boltzmann constant, t is the time taken for each point in the measurement, and R is the total coupling resistance of the system. Therefore, the related error is:

$$\frac{\delta I_S}{I_S} = \sqrt{\frac{4k_B T}{tR{I_S}^2}}. \tag{2.2}$$

In a practical quantum metrology measurement, I can assume R$\sim R_K$, which is the quantum resistance, 25.kΩ. The related error of the system, $\delta I_S/I_S$, should be less than 5×10^{-8}, t=24 h and T=10 mK. As a result, the current level must be larger than 314.7 pA according to equation (2.2), which is equivalent to 2 GHz operation frequency.

Scientist have already succeeded in performing high-accuracy measurements on Josephson voltage ($\sim$0.03 ppm)[28] and Quantum Hall Resistance ($\sim$45 ppb)[29]. However, at the moment, both the operation frequency ($\sim$670 MHz) and accuracy ($\sim$0.2 ppm) of single electron source[30] must be improved in order to meet the requirement of quantum metrology triangle measurement.

2.2 Device Physics: Single electron transport

2.2.1 Fundamental Physics for Single Electron Transport

The current originated from the movement of individual carriers is usually not observable. At room temperatures, the movement of individual carriers are dominated by their individual thermal kinetic energy[31]. As a result, although the average movement of large amount of carriers will generate electrical current, the movement of each individual carrier is random and unobservable. If I would like to observe the current originated from the movement of each individual carrier, the charging energy for each electron/hole must be larger than the thermal kinetic energy in order to dominate its movement.

In order to discuss the experimental condition to observe single electron transport, I will consider an RC-model, where the coupling resistance between the electron and the environment is R and coupling capacitance is C, as shown in Fig. 2.3:

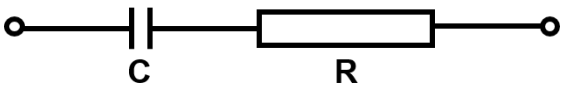

FIGURE 2.3: The schematic RC circuit model to describe the coupling between the electron to the ambient. Resistance and Capacitance are in series.

As stated in the previous paragraph, in order to observe single electron effect, the impact of electrostatic energy, E_c, should be larger than the impact of thermal fluctuation[32], therefore:

$$E_c = \frac{e^2}{2C} \gg k_B T, \tag{2.3}$$

, where C is the coupling capacitance of the system, e is the elementary charge, k_B is the Boltzmann constant, and T is the ambient temperature. Equation 2.3 shows that the ambient temperature must be low enough to suppress the random movement dominated by thermal kinetic energy. In order to have a rough idea of the scale required to observe single electron characterisitics, I will assume the system is put in a liquid helium environment where the temperature is 4.2 K. Under this circumstance, the minimum capacitance of the system, C_0, should be:

$$C_0 = \frac{e^2}{2k_B T} = 0.22\text{fF}. \tag{2.4}$$

Considering the dielectric layer of the tunnelling capacitor is 10 nm silicon dioxide, the dimension of the electrode should be around

$$a < \sqrt{\frac{C_0 t_{OX}}{\varepsilon_0 \varepsilon_{OX}}} = 241\text{nm}. \tag{2.5}$$

From the rough estimation showing in equation 2.5, I can see the scale of the system must be on the magnitude of 241 nm or less in a liquid-Helium environment.

Another important factor is the uncertainty principle[31]. The electrostatic energy of a single electron must be well defined in the whole transportation process in order to observe the single electron tunnelling. Otherwise, the intrinsic uncertainty is even larger than the electrostatic energy itself, and single electron effects therefore cannot be observed. As a result,

$$\frac{e^2}{C}.RC > h. \tag{2.6}$$

From equation 2.6, I know the coupling resistance must be larger than:

$$R > \frac{h}{e^2} = 25.8\text{k}\Omega = R_K \tag{2.7}$$

This value is usually named quantum resistance.

From (2.3) and (2.7), I can summarise the following three requirements in the real world to observe single electron characteristics:

(1) The temperature of the system must be low enough.

(2) The dimension of the system must be small enough.

(3) The resistance of the system must be high enough.

The three requirements can be achieved in both metallic tunnelling junctions[33] and semiconductor quantum dots[34]. They will be introduced separately in the following part.

2.2.2 Single Electron Transport in Metal Oxide Tunnelling Junction

The electrons in the metal can be described as Fermi liquid[35]. As a result, the free electrons in the metal, whose energy is above the Fermi level, can be described as non-interactive quasiparticles. Therefore, the metallic tunnelling junction can be described using mesoscopic capacitor model[32].

The schematic diagram metallic tunnelling junction structure is shown in Fig. 2.4:

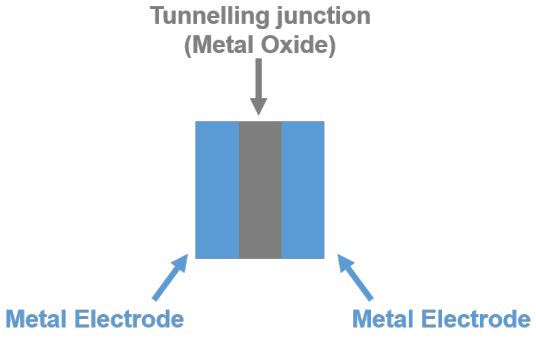

FIGURE 2.4: Schematic Diagram of a Metallic Tunnelling Junction.

In reality, Aluminium is often used as the electrode due to the great interface quality of Aluminium oxide[36]. The most fundamental single electron tunnelling structure is shown below, which is usually called single electron box[37]. By assuming the parameters as shown in Fig. 2.5, I can study the relationship between the bias applied and the number of electrons stored in the box, n,:

$$Q_\text{t} - Q_\text{g} = ne. \tag{2.8}$$

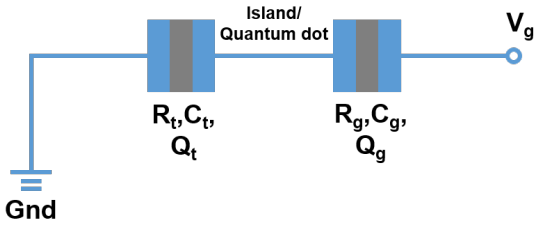

FIGURE 2.5: Schematic Diagram of a Single Electron Box.

$$\frac{Q_{\mathrm{g}}}{C_{\mathrm{g}}} - \frac{Q_{\mathrm{t}}}{C_{\mathrm{t}}} = V_{\mathrm{g}}, \tag{2.9}$$

where V_{g} is the voltage applied on the gate electrode, C_{g} is the tunnelling capacitance between the electrode and the island, and C_{t} is the tunnelling capacitance between the island and the ground. The charging energy of the system can be written as

$$W_{\mathrm{charge}}(n) = \frac{{Q_t}^2}{C_t} + \frac{{Q_g}^2}{C_g}. \tag{2.10}$$

Two major parts contribute to the total charging energy. The first part, which is coming from gate bias, can be expressed by

$$W_{\mathrm{A}}(n) = \int I(t) V_{\mathrm{g}} dt = V_{\mathrm{g}} Q_{\mathrm{g}}. \tag{2.11}$$

The second part, which is coming from free electrons inside the system, can be expressed by

$$W_{\mathrm{F}}(n) = W_{\mathrm{charge}}(n) - W_{\mathrm{A}}(n). \tag{2.12}$$

If n electrons are maintained in the system, a mandatary condition is that any electron tunnelling into/outside the system will result in the energy increase of free electrons inside the system. Therefore, the following condition,

$$W_{\mathrm{F}}(n) < W_{\mathrm{F}}(n \pm 1), \tag{2.13}$$

must be satisfied. By solving equation (2.8) to (2.13), I can establish the relationship between bias and the number of electrons,

$$(n - \frac{1}{2})\frac{e}{C_{\mathrm{g}}} < V_{\mathrm{g}} < (n + \frac{1}{2})\frac{e}{C_{\mathrm{g}}}. \tag{2.14}$$

The single electron box can only store the electrons. It is not possible to switch the circuit, i.e., the single electron box is not a transistor. The metallic single electron transistor is actually two single electron boxes sharing the same island. The equivalent circuit diagram of a single electron transistor is shown in Fig. 2.6. Here I assume the tunnelling capacitance between the drain electrode and the island as C_{d}, and tunnelling capacitance between the source electrode and the island as C_{s}.

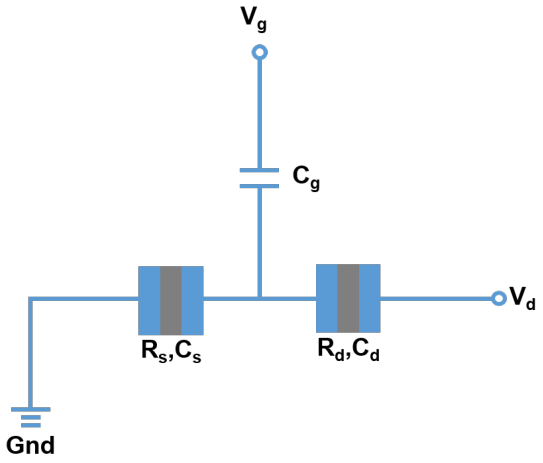

FIGURE 2.6: Equivalent Circuit Diagram of a Single Electron Transistor.

In order to find the 'block' state for the single electron transistor, I can use Thevenins theory to investigate on the effective circuit. If I focus on the electrons coming from drain reservoir, by applying equation (2.14), the following condition must be satisfied:

$$(n-\frac{1}{2})\frac{e}{C_{\mathrm{g}}+C_{\mathrm{d}}} < \frac{C_{\mathrm{g}}V_{\mathrm{g}}+C_{\mathrm{d}}V_{\mathrm{d}}}{C_{\mathrm{g}}+C_{\mathrm{d}}} < (n+\frac{1}{2})\frac{e}{C_{\mathrm{g}}+C_{\mathrm{d}}}. \tag{2.15}$$

If I focus on the electrons coming from the source reservoir, using the same way I can obtain:

$$(n-\frac{1}{2})\frac{e}{C_{\mathrm{g}}+C_{\mathrm{s}}} < \frac{C_{\mathrm{g}}V_{\mathrm{g}}}{C_{\mathrm{g}}+C_{\mathrm{s}}} - V_{\mathrm{d}} < (n+\frac{1}{2})\frac{e}{C_{\mathrm{g}}+C_{\mathrm{s}}}. \tag{2.16}$$

In the bias conditions described by (2.15) and (2.16), the system was 'blocked'. The 'blocked' regime is roughly drawn in Fig. 2.7.

As I can see from Fig. 2.7, in the blue region, only one particular number of electron is allowed to stay in the island. Therefore, the sequential tunnelling process is blocked. This phenomenon is usually called Coulomb blockade[38]. Since the shape of bias conditions for the block state in the stability diagram is a diamond, it is often called 'Coulomb diamond'. Coulomb diamond is the unique sign of the single electron transistors[39].

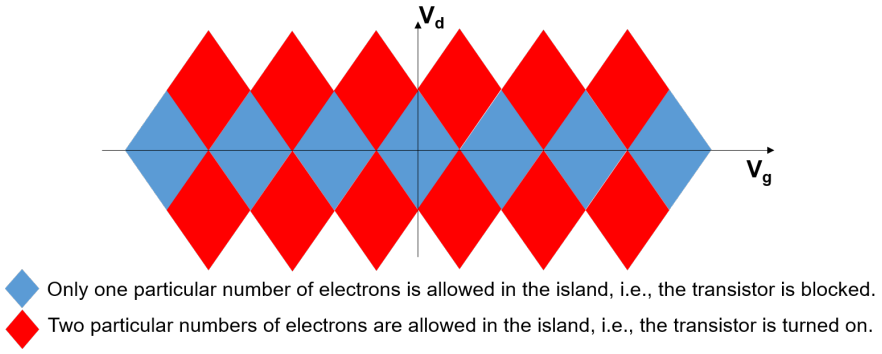

FIGURE 2.7: Ideal Stability Diagram of a Metallic Single Electron Transistor.

There is no simple solution to the current-voltage characteristics of single electron transistor. In order to analyse the sequential tunnelling current outside the Coulomb diamond regime, first, I need to calculate the change in free energy when an electron tunnels into/outside the island through the drain, $\Delta F_{\mathrm{d}}^{\pm}(N)$, and through the source, $\Delta F_{\mathrm{s}}^{\pm}(N)$, as shown in the equation (2.17) and (2.18),

$$\Delta F_{\mathrm{d}}^{\pm}(N) = \frac{e}{C_{\Sigma}}[\frac{e}{2} \pm (Ne - Q_0) \mp (C_{\mathrm{g}} + C_{\mathrm{s}})V_{\mathrm{d}} \pm C_{\mathrm{g}}V_{\mathrm{g}}], \tag{2.17}$$

and

$$\Delta F_{\mathrm{s}}^{\pm}(N) = \frac{e}{C_{\Sigma}}[\frac{e}{2} \mp (Ne - Q_0) \mp C_{\mathrm{d}}V_{\mathrm{d}} \mp C_{\mathrm{g}}V_{\mathrm{g}}], \tag{2.18}$$

where N is the number of electrons in the island. Applying Fermi's golden rule[31], I could obtain the tunnelling rate of single electron into/out through source, $\Gamma_{\mathrm{s}}^{\pm}(N)$ and into/out through drain tunnelling junction, $\Gamma_{\mathrm{d}}^{\pm}(N)$,

$$\Gamma_{\mathrm{d}}^{\pm}(N) = \frac{1}{R_{\mathrm{d}}e^2}[-\frac{\Delta F_{\mathrm{d}}^{\pm}(N)}{1 - \exp(\frac{\Delta F_{\mathrm{d}}^{\pm}(N)}{k_{\mathrm{B}}T})}], \tag{2.19}$$

and

$$\Gamma_{\mathrm{s}}^{\pm}(N) = \frac{1}{R_{\mathrm{s}}e^2}[-\frac{\Delta F_{\mathrm{s}}^{\pm}(N)}{1 - \exp(\frac{\Delta F_{\mathrm{s}}^{\pm}(N)}{k_{\mathrm{B}}T})}], \tag{2.20}$$

where C_{Σ} is the total coupling capacitances of the charging island. R_{s} and R_{d} are effective tunnelling resistances between the island to the source and drain respectively, which are related to the density of the states in the system and the transmission coefficient of the tunnelling barriers. After obtaining the tunnelling rate, the master equation of the probability that N electrons occupy the island can be expressed as

$$\frac{\partial p(N,t)}{\partial t} = p(N+1)[\Gamma_{\mathrm{s}}^{+}(N+1) + \Gamma_{\mathrm{d}}^{-}(N+1)] - p(N)[\Gamma_{\mathrm{s}}^{-}(N) + \Gamma_{\mathrm{d}}^{+}(N)]. \tag{2.21}$$

In the steady state, the probability is not assosiated with time, so

$$\frac{\partial p(N,t)}{\partial t} = 0. \tag{2.22}$$

The drain current is therefore expressed as

$$I = e\Sigma_{N=-\infty}^{N=\infty} p(N)[\Gamma_{\mathrm{s}}^{+}(N) - \Gamma_{\mathrm{s}}^{-}(N)]. \tag{2.23}$$

By solving equation (2.17) to (2.23), I could numerically calculate the drain current outside the Coulomb Blockade regime.

The major error source has originated from co-tunnelling[40, 41]. Co-tunnelling process could be observed even at the Coulomb blockade region[42, 43]. A schematic diagram of co-tunnelling process is shown below:

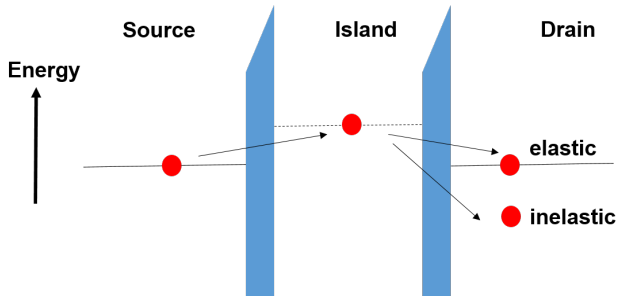

FIGURE 2.8: A schematic diagram of the Co-tunnelling Process. Electrons tunnel from the source to the drain through a virtual state.

In the first step, the electron will tunnel from the source to an intermediate virtual state in the island. Then, another electron, which was initially inside the island, tunnel from the island to the drain. Co-tunnelling processes can be divided into two categories : elastic co-tunnelling, with no energy loss for the electrons, and inelastic co-tunnelling, with energy loss for the electrons[41]. Co-tunnelling was firstly observed by L. Geerligs[44], and is usually considered one of the main error contributors in single electron devices[45].Since the total co-tunnelling rate depends exponentially on the number of tunnelling junctions, it is possible to suppress the co-tunnelling by adding more junctions in the metallic single electron devices[46, 47, 48, 49].

The maximum frequency allowed for single electron operation, roughly around 10 MHz, is limited by the RC constant of tunnelling junction[10] (practically, Aluminium oxide). It is very difficult to overcome the frequency limit. As a result, this issue puts a cap on the actual application of metallic single electron devices.

2.2.3 Single Electron Transport in Semiconductor

In the semiconductor-based device, the single electron transport can also be observed in 2-D electron gas in the conducting layer[50].

I will do a rough estimation of the electron-electron distance in 2-D electron gas and Bohr radius. Usually, the free carrier concentration is around 10^{12} cm^{-2} in 2-D electron gas, corresponding to 10 nm electron-electron distance[51]. The Bohr radius can be calculated by $a_0{=}4\pi\varepsilon_r\varepsilon_0/m_e e^2$. Considering the case of silicon, where ε_r is 11.9 and the effective electron mass is $0.26m_0$, the Bohr radius is around 2.4 nm. Since the interaction parameter r_0/a_0 is around 4, the electron-electron interaction is weak in semiconductor quantum dot[52]. As a result, mesoscopic model still gives a reasonable description of the system.

However, there are several key differences between the metallic case and semiconductor case:

First of all, the electron-electron distance in quantum dot is much larger than the case of metal ($\sim$0.5 nm). As a result, the carrier density is lower, and fewer number of energy levels is allowed in the quantum dot. That enhances the impact of level spacing originated from quantum confinement[53]. Therefore, non-equilibrium effect in quantum dot is much stronger than that in metallic structure[34].

Secondly, unlike the case in the metal, the parameters of quantum dots in semiconductor structures are tuneable by external voltage. As a result, the dynamics of the electrons inside the quantum dot still depends strongly on the confining potential of the quantum dot, and Density-of-State (DOS) fluctuations can have a visible impact on the single-electron transportation characteristics[54]. Therefore, Mesoscopic capacitor model will give some deviation when describing the characteristics of electrons inside quantum dots, due to the fluctuation on the Density-of-State (DOS) and the change of wavefunction for the electron states. The geometry must be considered in order to get an accurate theoretical description of quantum dots.

At last, error sources in the single electron transport are not fully understood due to the complicated operation mechanism[11]. As a result, scientists do not have a clear image regarding the accuracy limitation and error source on the single electron transport. But it is expected to be improved through reducing the size.

The unique advantage of the quantum dot structure compared with the metallic part is the tuneable parameters for the quantum dots and the tunnelling barrier. The tuneability gives flexibility in device operation, which makes high-frequency operation possible. As a result, non-adiabatic transportation is achievable in the semiconductor-based structure, which is the fundamental operation principle for the semiconductor single electron pump[19].

Non-adiabatic transport is a much more complicated process compared with the conventional adiabatic effects. If the confining potential of quantum dot is controlled by a AC signal, the coupling strength between quantum dot and the environment will be changed. If the frequency of AC signal is much higher than the time constant of single electron tunnelling, the electron is not able to catch the change in the coupling strength, and therefore the full process is non-adiabatic. Mesoscopic model is not enough to describe the electron transport in this process.

A physics model called decay cascade model, which is proposed by Vyacheslavs Kashcheyevs and Bernd Kaestner[55, 56], is introduced to describe the single electron transport through dynamic quantum dot in this non-equilibrium situation.

The model is shown below, considering the quantum dot and environment is resistively coupled initially, and N electrons stay in the quantum dot when the time scale is t_0.

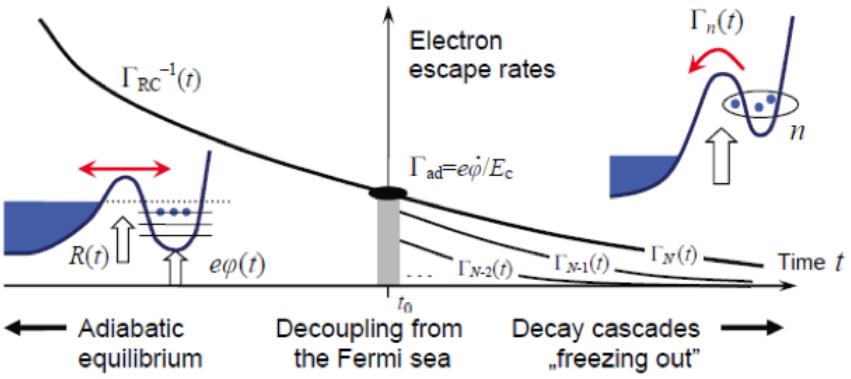

FIGURE 2.9: Decay-Cascade Process in the non-adiabatic single electron transfer.[55]

The intrinsic relaxation rate of electron inside the quantum dot can be expressed by:

$$\Gamma_{\mathrm{Re}} = (RC)^{-1}. \tag{2.24}$$

R and C are the coupling resistance and capacitance regarding the environment, respectively. If I define the quantum dot electrostatic potential to be φ, then the ejection rate of single electron inside the quantum dot would be

$$\Gamma_{\mathrm{ej}} = \frac{e}{E_{\mathrm{c}}}\frac{d\varphi}{dt}. \tag{2.25}$$

Where E_{c} is the electrostatic energy of electron inside the quantum dot. The equilibrium condition is

$$\Gamma_{\mathrm{ej}} \leq \Gamma_{\mathrm{Re}}. \tag{2.26}$$

If equation (26) is not satisfied, the non-equilibrium condition will dominate the transportation of electron. In the non-equilibrium condition, I define the probability of n electrons staying in the island to be P_{n}, the ejection rate of single-electron when n electrons stay in the island to be Γ_{n}. As a result, the kinetic equation of the system could be written as

$$\frac{dP_{\mathrm{n}}(t)}{dt} = -\Gamma_{\mathrm{n}}(t)P_{\mathrm{n}}(t) + \Gamma_{\mathrm{n+1}}(t)P_{\mathrm{n+1}}(t). \tag{2.27}$$

The boundary conditions of this equation are

$$P_{\mathrm{n}}(t_0) = \delta_{\mathrm{n,N}}, \tag{2.28}$$

which represents the initial case as N electrons stay in the island, and

$$\lim_{t\to+\infty} \Gamma_{\mathrm{n}}(t) = 0, \tag{2.29}$$

which shows the solution of the system should be convergence.

A general solution of equation is:

$$P_{\mathrm{n}}(t) = \int_{t_0}^{t} e^{-\int_{t'}^{t}\Gamma_{\mathrm{n}}(\tau)d\tau}\Gamma_{\mathrm{n+1}}(t')P_{\mathrm{n+1}}(t')dt' \tag{2.30}$$

It is not enough to find a solution simply from the equations, and further assumptions must be made.

(1) No further loading of electrons is allowed when t>0.

In this condition, I would like to talk about the process where the quantum dot and environment is initially coupled and then decoupled. This assumption would simplify the situation.

(2) For m>n, all the $P_{\mathrm{m}}(t)$ will only vary in a very small time scale compared with the variation of $P_{\mathrm{n}}(t)$ itself.

If I assume the change of value in time domain of P_{n} is abrupt compared with the change of value in time domain of $P_{\mathrm{n-1}}$, as shown above in Fig. 2.10, I can assume the deviation of $P_{\mathrm{n}}(t)$, $dP_{\mathrm{n}}(t)$/dt, is a delta function when I mathematically process equation (2.30).

(3) The tunnelling rate is well defined in the whole process.

The electron energy level is usually in the magnitude of ∼1 meV. The equivalent photon frequency is in the magnitude of ∼300 GHz, which is much faster than the operation frequency range I are interested in (∼GHz). As a result, I can assume tunnelling rate is well defined in the whole process.

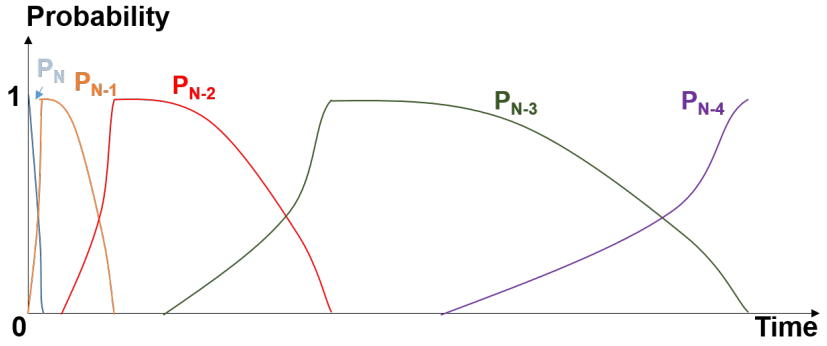

FIGURE 2.10: Decay of probability distribution. The timescale for the Nth electron tunnels out the quantum dot is much smaller than the (N-1)th electron.

Based on the above approximation, by summation over all the integers m>n in equation (2.27), I know that:

$$\Gamma_{n+1}(t)P_{n+1}(t) = -\frac{d}{dt}\sum_{m>n} P_m(t) \tag{2.31}$$

And therefore based on assumption (2):

$$\int_{-\infty}^{+\infty}[-\frac{d}{dt}\sum_{m>n} P_m(t)]dt = 1 - \sum_{m>n} P_m(+\infty) \tag{2.32}$$

Therefore, I can assume

$$\frac{d}{dt}\sum_{m>n} P_m(t) = [1 - \sum_{m>n} P_m(+\infty)]\delta(t_0 - t) \tag{2.33}$$

If I define X_n=$\int_{t_0}^{+\infty}\Gamma_n(\tau)d\tau$, then from equation (2.30), (2.32), and (2.33), I can estimate the probability distribution when the system is stable:

$$P_n(+\infty) = e^{-X_n}(1 - \sum_{m>n}^{N} P_m(+\infty)) \tag{2.34}$$

From (2.34), I can establish the relationship between $P_n(+\infty)$ and $P_{n+1}(+\infty)$. Based on that, I can solve (2.34) to get

$$P_n(+\infty) = e^{-X_n}\prod_{m=n+1}^{N}(1 - e^{-X_m}) \tag{2.35}$$

This is the probability distribution of the number of electrons inside the quantum dot after the decay cascade process.

2.3 Single Electron Pump: Design and Realisation

2.3.1 Adiabatic Pumping

Adiabatic single electron pumping is the operation mechanism of metallic single electron pumps. The single electron adiabatic pumping is based on the single electron sequential tunnelling process. A schematic diagram of a conventional metallic single electron pump is shown in Fig. 2.11:

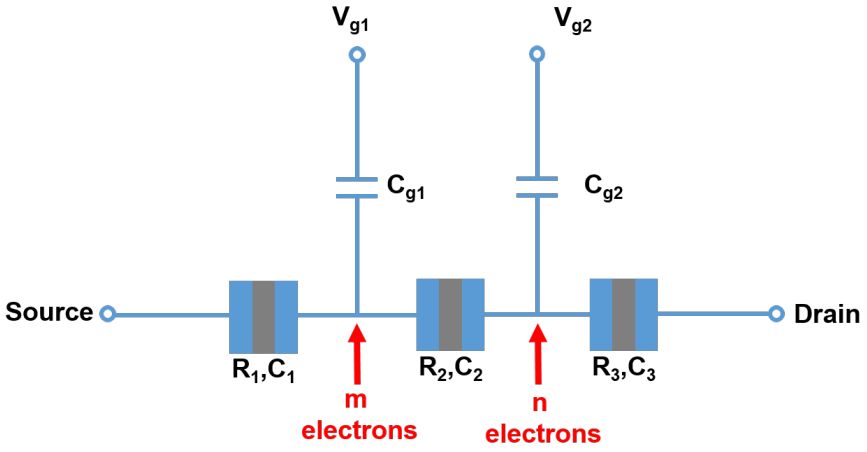

FIGURE 2.11: Schematic diagram of a metallic single electron pump.

The stability diagram of the two gates when both drain and source electrodes are biased at 0 is shown in Fig. 2.12.

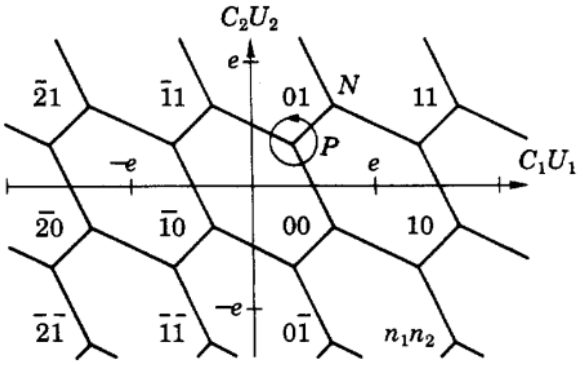

FIGURE 2.12: Stability diagram of a metallic single electron pump at 0 drain bias.[57]

For simplicity point of view, the state of the system when m electrons stay in the left island and n electrons stay in the right island will be called (m,n). At the beginning

of the pumping process, the energy favourable state is (0,0). Each gate electrode is modulated with an AC signal. As shown in Fig. 2.12, When the bias (V_{g1}, V_{g2}) passes the first degeneracy line under the modulation of both AC signals, the energy-favourable state becomes (1,0), and one single-electron tunnels from the source to the left island[57]. Then when the bias (V_{g1}, V_{g2}) passes the second one, the electron tunnels from the left island to the right island because the stable state turns to be (0,1). When (V_{g1}, V_{g2}) switches back to the initial state, the stable state is (0,0) again, which means the electron must tunnel to the drain lead. By switching of the energy-favourable states of the system under the control of two AC signals, a single electron is transferred from the source to the drain[57].

However, as stated in the previous part, although the error mechanism for the adiabatic transport in the metallic pumps is well studied, the operation frequency is limited by the RC constant of the metallic tunnelling junction. In order to raise the current to meet the requirement of quantum metrology, non-adiabatic pumping, along with the semiconductor quantum dot structure, is used and investigated.

2.3.2 Non-adiabatic Pumping

A schematic diagram of adiabatic single electron pump based on semiconductor quantum dots is shown in Fig. 2.13:

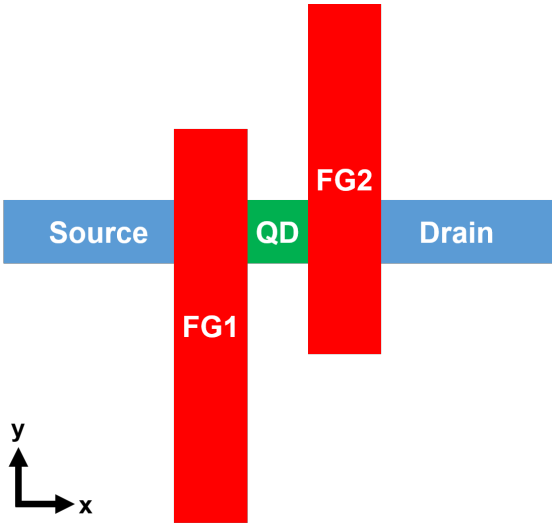

FIGURE 2.13: General schematic model of semiconductor single electron pump

There are basically five parts in the device: source reservoir, drain reservoir, two gates (FG1 and FG2) and a quantum dot. Usually, one of the FGs is controlled by a bias tee connected to both DC and AC signal, while the other FG is biased at a fixed voltage. For some of the designs, especially silicon devices, the quantum dot is also modulated by an external bias (top gate or back gate) to give a precise control to enhance the single particle energy spacing.

The full operation process of non-adiabatic single electron pump can be divided into 4 processes: loading, back-tunnelling, trapping and ejecting[30, 58].

(1) Loading

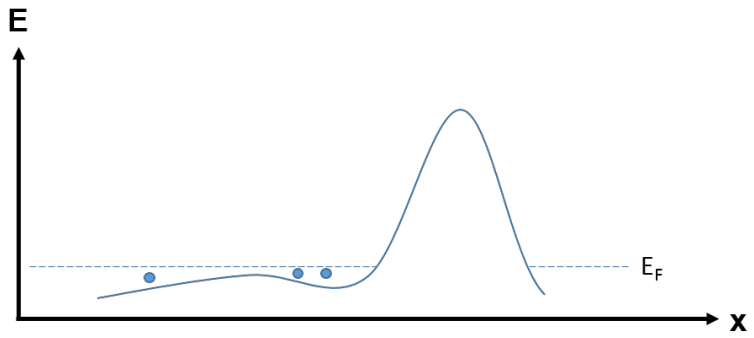

FIGURE 2.14: Loading Process of the non-adiabatic single electron pump. The source and quantum dot are metallically connected.

The schematic energy versus distance diagram is shown in Fig. 2.14. The barrier height of entrance is lowered by the AC signal from FG1. As a result, no barrier is formed between the source and quantum dot, and the electrons can classically move from source to quantum dot. In this process, the quantum dot becomes 'metallic'.

(2) Initialisation

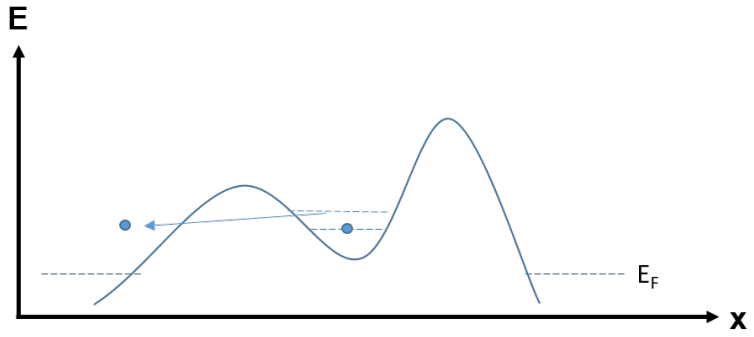

FIGURE 2.15: Initialisation Process of the non-adiabatic single electron pump. The electrons in the quantum dot back-tunnel to the source through quantum-mechanical processes.

The schematic energy versus distance diagram is shown in Fig. 2.15. In this process, the barrier between the source and the quantum dot is raised by FG1. After the tunnelling coupling resistance between source and quantum dot is larger than the quantum resistance, the electrons inside the quantum dot will back-tunnel to the source reservoir through the quantum-mechanical process. At the end of the step, the barrier height is very high so that the coupling between the source reservoir and the quantum dot becomes very weak and therefore can be neglected. At the end of this process, the number

of electrons stay in the quantum dot should be an integer determined by the parameter of the quantum dot, described by the decay cascade model[59, 60].

This process is a non-adiabatic process, which means the operation frequency could be higher than the RC constant of the tunnelling barrier. However, if the operation frequency is too high, the non-adiabatic excitation would become significant, and it will have a huge impact on the transport accuracy.

(3) Trapping

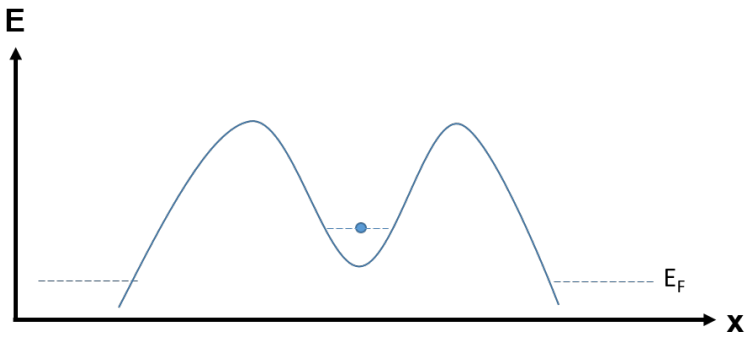

FIGURE 2.16: Trapping Process of the non-adiabatic single electron pump. One single electron is trapped in the quantum dot, and decoupled from both source and drain.

The schematic energy versus distance diagram is shown in Fig. 2.16. At this step, the quantum dot and both source/drain lead becomes uncoupled. A single electron is trapped inside the quantum dot, and is not able to escape.

(4) Ejecting

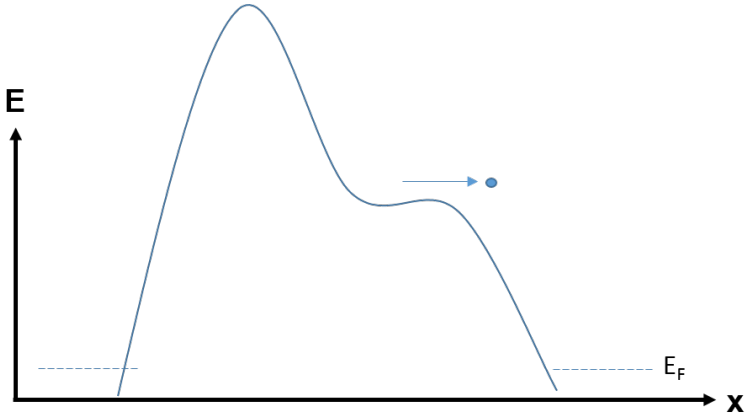

FIGURE 2.17: Ejecting Process of the non-adiabatic single electron pump. The electron trapped in the quantum dot is ejected to the drain reservoir, and the single electron transfer process is completed.

The schematic energy versus distance diagram is shown in Fig. 2.17. When the barrier height is further increased, because of the coupling between the FG1 and the quantum dot, the energy level of the single electron in the quantum dot is raised, and the barrier

between the quantum dot and drain reservoir is lowered. When the energy of the single electron coupled inside the quantum dot is large enough, the electron is able to go over the exit gate barrier. Therefore, the single electron transfer process is completed.

I will describe the operation of the single electron pump theoretically based on the decay cascade model[61]. The pump current could be expressed by:

$$I = ef \sum_{n} nP_{\mathrm{n}}(+\infty) \tag{2.36}$$

From the quantum mechanics[53], I know that the tunnelling rate usually depends exponentially on the height of tunnelling barrier, which is directly controlled by the external bias. If I introduce a fitting parameter α to show this dependence, and another fitting parameter δ to reveal the energy spectrum of the system, I can write the following equation,

$$\ln X_{\mathrm{n}} = -\alpha V + \sum_{1}^{n} \delta_{\mathrm{i}}, \tag{2.37}$$

where V is the external gate bias. In this equation, the constant α is actually showing the dependence between the tunnelling rate and external bias, and δ_{i} reveals the tunnelling rate difference between different electron states inside the quantum dot, which actually corresponds to the addition energies of the quantum dot. The theoretical expression of δ_{n} is:

$$\delta_{\mathrm{n}} = \ln \frac{X_{\mathrm{n}}}{X_{\mathrm{n-1}}} \tag{2.38}$$

Practically, X_{n} is much larger than $X_{\mathrm{n-1}}$. Therefore, I can ignore all the number m>n+1 in the multipling series in equation (2.35). As a result, equation (2.35) can be further simplified as:

$$P_{\mathrm{n}}(+\infty) \approx e^{-X_{\mathrm{n}}} - e^{-X_{\mathrm{n+1}}} \tag{2.39}$$

By substituing (2.39) to (2.36), I can derive the total current for the single electron pump, I_{pump},

$$I_{\mathrm{pump}} = ef \sum_{n} n[\exp(-\exp(-\alpha V + \sum_{i=1}^{i=n} \delta_{\mathrm{i}})) - \exp(-\exp(-\alpha V + \sum_{i=1}^{i=n+1} \delta_{\mathrm{i}}))], \tag{2.40}$$

α and δ are very important parameters regarding the performance of the single electron pumps. In order to understand how these two parameters impact the device performance, I will plot equation (2.40) with some typical values for α and δ to see the impact of each parameter. Usually, the 1st plateau is the most important one, so I will just try to observe the characteristics of the 1st plateau. For simplicities, all the δ_i will be the same, and the unit of α will be chosen as V^{-1} I will select three groups of (α,δ) to be (4,15),(10,15) and (4,6). The result is shown in Fig. 2.18:

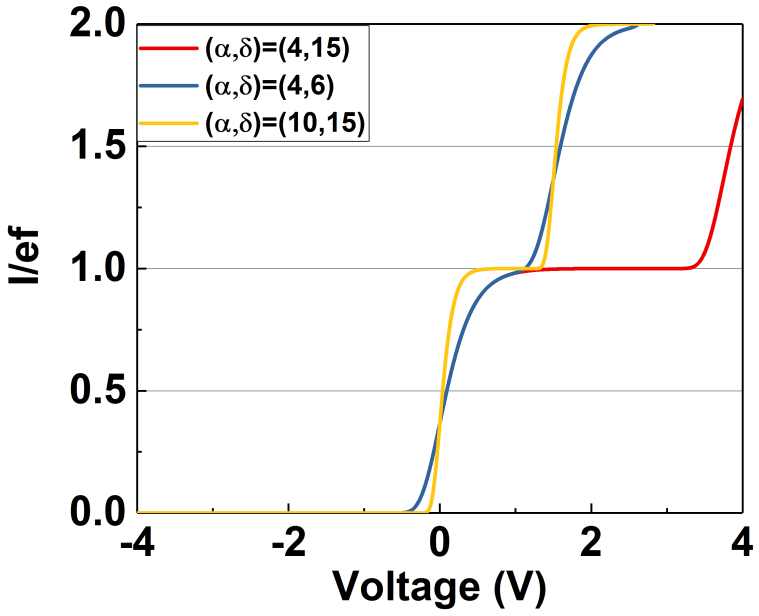

FIGURE 2.18: Simulation of decay cascade model with different fitting parameters α and δ.

From this graph, it can be noticed that both parameters α and δ are very important. δ determines both width and flatness of the plateau of the single electron pump (by comparing (4,15) and (4,6)) while α would have an impact on the width and position of the plateau(by comparing (4,15) and (10,15)). For a good single electron pump, plateau needs to be both long and flat to ensure a stable and accurate operation. As a result, α needs to be small while δ should be as large as possible. As stated in equation (2.37), the α reveals dependence of tunnelling rate on the external voltage, while δ reveals the addition energy of the 1st electron into the system. As a result, I need to fabricate single electron pump with small quantum dots and wide tunnelling barriers, to suppress α while increase δ.

If I assume the size of the device as L, the charging energy will be inversely proportional to area, i.e., propotional to L^{-2}. When the thickness of the Si nanowire is not comparable with the inversion layer thickness, 3nm[62], the electrons will be confined in 2-D region. Since the quantisation energy is proportional to L^{-2} as well, the charging energy and quantisation energy are comparable. As a result, they both play important role on

the value of δ. If I scale the device down further so that the Si nanowire thickness is comparable to the inversion layer thickness, the 2-D confinement assumption is no longer valid and the quantisation energy is proportional to L^{-3}. It will increase much faster as the device is scaled, and therefore dominate δ in the case of ultrascaling to 3nm.

The error in the single-electron pump operation comes from several sources:

First is the thermal-assisted tunnelling. If the temperature is high, the thermal kinetic energy will have a high impact on the Hamiltonian of the single electrons in the system, resulting in larger deviation from the decay cascade model. This error source can be controlled by reducing the ambient temperature to ∼10 mK).

Second, as stated, is the systematic error in the initialization step. The intrinsic flatness of the plateau significantly depends on δ in the decay cascade model. If the energy level spacing of different electron states in the quantum dot is not large enough, i.e. the scale of the device is large, the intrinsic error will be the dominant error source, especially in low frequency operation.

Third error source is coming from non-adiabatic excitation due to high operation frequency. When the operation frequency is high, the electron inside the quantum dot may be excited in this non-adiabatic process, and causes unwanted back-tunnelling in the process. This will also result in deviation from decay cascade model. This will be the dominant factor when the device is operated at a high frequency.

Several ways to suppress this error source have been proposed, first, I can use special control wave to reduce the non-adiabatic excitation and other high-frequency related errors.

If I use a standard sine wave, as shown in Fig. 2.19, the four processes will be very close to each other in the time domain[30]:

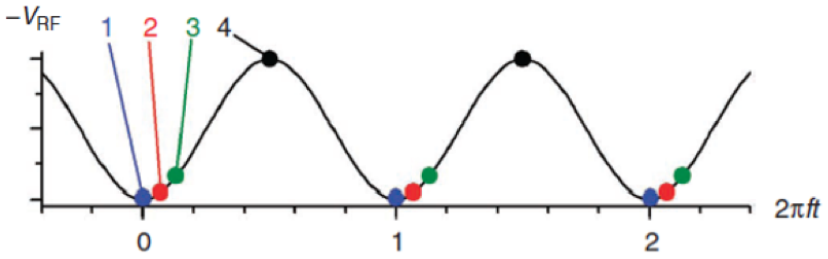

FIGURE 2.19: The timescale of the loading, initialisation, trapping and ejection event of non-adiabatic pumping while operating with a sine wave. The 1, 2, 3, 4 points shown in the figure correspond to the loading, initialisation, trapping and ejection event, respectively.[30]

This means the actual equivalent frequency of initialisation step is actually higher than the operating frequency. A simple idea is to spread the time-scale difference between

the four steps. The idea was realised by NPL, they use a special wave called 'arbitrary wave'. The wave of the AC signal is shown as below:

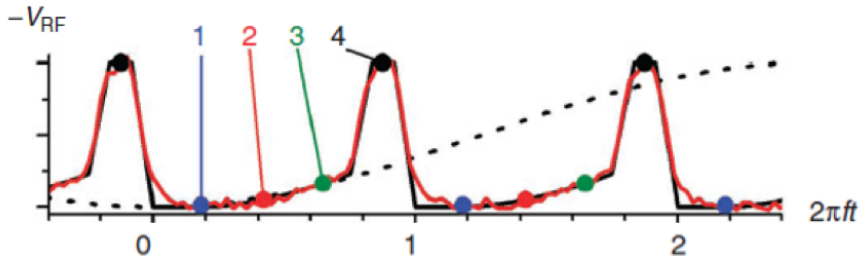

FIGURE 2.20: The timescale of the loading, initialisation, trapping and ejection event of non-adiabatic pumping while operating with a specially-designed arbitrary wave. The 1, 2, 3, 4 points shown in the figure correspond to the loading, initialisation, trapping and ejection event, respectively.[30]

In the specially designed AC signal, the time-scale difference between the four steps is almost the same. The slope initially between 1,2 and 3 is actually equivalent to a sinewave with one fifth of the operating frequency, and NPL has proven that this will enhance the maximum operation frequency up to 5 times with the same transportation accuracy[30].

Second, I can also apply high perpendicular magnetic field in order to enhance the performance of single electron pump[63, 64]. With the applications of magnetic field, the electrons will be confined at the edge of the channel, and therefore the addition energy of the 1st electron will also increase. Also, the tunnelling rate will be less sensitive to the electrical field due to the additional impact of magnetic field. Therefore, the plateau will become flatter and wider.

NPL group has investigated on the influence of magnetic field on the output characteristics of single electron pump both theoretically and experimentally.

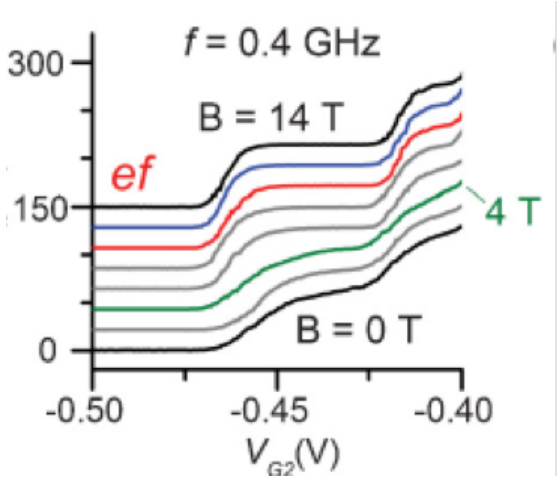

FIGURE 2.21: Influence of Magnetic Field on the current-voltage characteristics of the single electron pump.[65]

As shown in Fig. 2.21, the flatness and width of the plateau is significantly increased with higher magnetic field when the magnetic field is below 10 T. When the magnetic field is above 10 T, the flatness of plateau seems to be saturated in the experiment.

They explain the results theoretically by estimating the back-tunnelling rate in the decay cascade model[65].

Assuming the barrier potential profile is a Gaussian one, they find that the back-tunnelling rate in the initialization step is reduced and more sensitive to the value of barrier height at the high magnetic field due to the extra confinement to the single electron in the quantum dot. The quantum confinement energy is also increased, resulting in larger value of δ in decay cascade mode. As a result, the plateau becomes flatter.Also, from the derivative curve of the I-V characteristics for the single electron pump, they find the small peaks found at high frequency operation caused by non-adiabatic excitation is suppressed by high magnetic field. They claim this improvement is due to extra enhancement on confinement added by magnetic field as non-adiabatic excitation depends strongly on the strength of perturbation of the wave function.

Third, scientists can suppress the high-frequency error by parallel operation[66]. If several single electron pumps can be run parallelly, I could get the same current with much lower frequency. Therefore, high-frequency error coming from non-adiabatic process can be suppressed.

In total, the accuracy of non-adiabatic single electron pump is mainly limited by the excitation of single electrons originated from the high-frequency operation. Based on the solutions, scientists and engineers have proposed many device structures for the single electron pumps. They will be introduced in the next part.

2.3.3 Variations of Designs

Many designs of single electron pumps, based on GaAs or Si quantum dot structure, have been given by different groups.

GaAs devices and silicon devices are both widely used for this application. The advantage of GaAs device is due to high electron mobility in HEMT(high-electron-mobility-transistor) structure, and the advantage of silicon device is the compatibility with CMOS platform and more likely to achieve parallel operation due to the well-established CMOS fabrication technology. I will introduce some typical designs for both two groups.

For the GaAs devices, a most typical design is given by NPL and the structure is shown in Fig. 2.22:

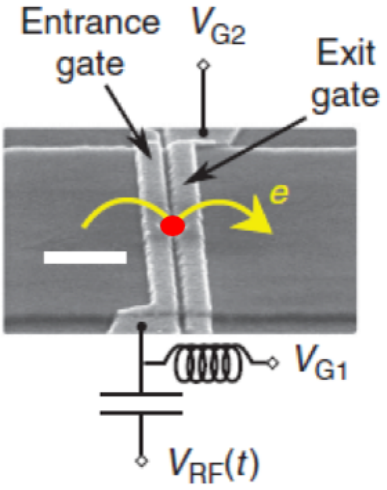

FIGURE 2.22: A conventional GaAs pump design from NPL. The quantum dot is drawn as a red spot in the figure. The RF signal is connected to the entrance gate.[30]

In this design, they were using the coupling between entrance gate and quantum dot to control the quantum dot in 2-D electron gas. The device was fabricated on a GaAs/-GaAlAs hetero structure. The conducting channel was 2 μm wide. The carrier concentration was 2.7×10^{15} m^{-2} at 1.5K and the mobility corresponding was 70 m^2/V.s.

The design was simple and straight-forward, almost the same as the schematic diagram in Fig. 2.13. The device was able to be operated at 630 MHz with the accuracy of 1.2 ppm, which was equivalent to 1.2 aA[30].

A group from Korea Research Institute of Standards and Science gave a more complex design for GaAs pumps with better gate confinement of the quantum dot[67, 68]. The shematic diagram and SEM images of the devices are shown in Fig. 2.23[69, 70]:

This design was more complex compared with the design in NPL. The quantum dot was controlled by four gates: a trench gate and three side gates. The shape of the potential well inside the HEMT structure could be sharper and deeper under the control of the trench gate, therefore energy level spacing between different electron states was increased. That would help increase the δ_n value in the decay cascade model, and therefore improve the performance. The side gates, GP, also gave extra confinements on the quantum dot, and they found the confinement of electron was significantly enhanced while asymmetric potential profile was applied on side gates. They claim it was because the asymmetric potential profile effectively reduced the size of the quantum dot by pushing the single electron to one side in 2-D electron gas.

The devices were measured at 300 mK with 13.5 T external magnetic field, and achieved the accuracy of 0.3 ppm with the operation frequency of 500MHz. The result was improved compared with the designs of the simplest design given by NPL, which revealed

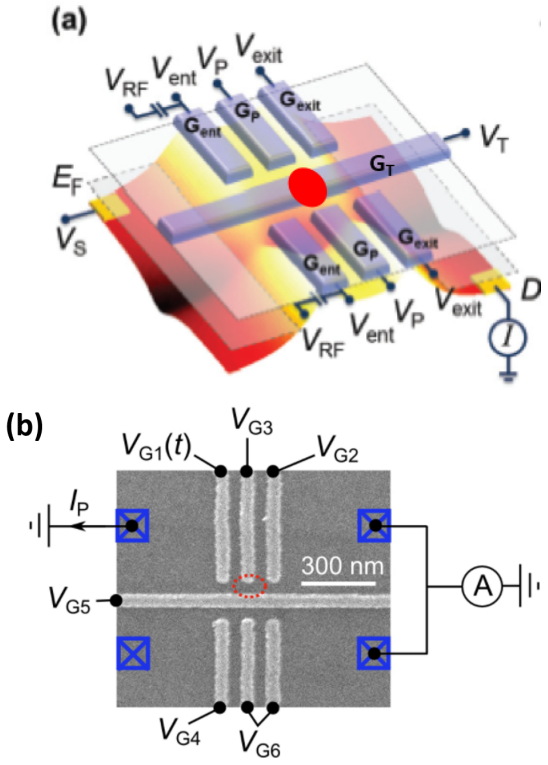

FIGURE 2.23: A GaAs pump design from South Korea. The quantum dot is drawn as a red spot in (a). The RF signal is connected to the entrance gate. (a) shows the schematic diagram while (b) shows the SEM image of the device. The quantum dot is modulated by both trench gate and the side gate.[69,70]

that the optimisation of the single electron pump designs was able to enhance the performance of the single electron pump.

For the silicon device, A. Fujiwara from NTT first achieved a Si single electron pump in 2001[71]. The device structure is shown below:

The device was based on nanowire FET and fabricated on an SOI chip with 200 nm buried oxide layer to reduce the leakage and parasitic capacitor, which were potential limiting factors of the device performance. The gate length of their devices were around 50 nm while the spacing of gates were around 125 nm. The nanowire was 30 nm wide and 30 nm thick. The thickness of polysilicon gate was around 125 nm.

In their device design, they used double-layer gate to provide better control of the quantum dot[72]. The quantum dot was mainly controlled by the upper gate shown in the graph above. They were able to operate the device with 2.3 GHz frequency, at 20 K and with no magnetic field. The uncertainty was limited by the resolution of the equipment[73].

French group from Leti fabricated single electron pump using industrial CMOS platforms with similar structure. The difference was that they were using back-gate to control the

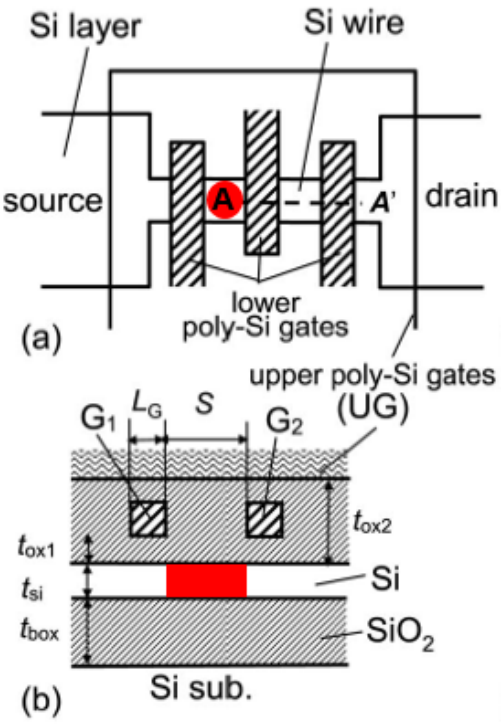

FIGURE 2.24: A conventional Si pump design from NTT. The quantum dot is drawn as a red spot in the (a), and shown as red regime in (b). The RF signal is connected to the lower gate G1. The quantum dot is modulated by the upper poly-Si gate.[73]

quantum dot rather than top-gate to reduce the complexity of fabrication, and made the device more compatible with the CMOS fabrication platform[74].

They could successfully operate the device in 0.5 K environment with no magnetic field at 650 MHz with the uncertainty level 0.15%, which was limited by the resolution of measurement system[75].

Unlike conventional MOSFET structure, the UNSW group introduce a side-gate controlled 2-D electron gas structure to build silicon single electron pump[76]. An SEM image of their device is shown in Fig. 2.26.

All the gates were Aluminium and they were using Aluminium Oxide as the isolation between different gates. The device was measured at 80mK with no magnetic field. They successfully operated the device at 0.5 GHz with the uncertainty of 29 ppm[77].

In the above part, I listed several designs of single electron pumps, where the quantum dots have originated from the gate-defined structures. From the result shown above, I can see the complex gate designs can enhance the device performance by extra control of the quantum dot. However, complex structure is also a trade-off due to the difficulty in reliable fabrication.

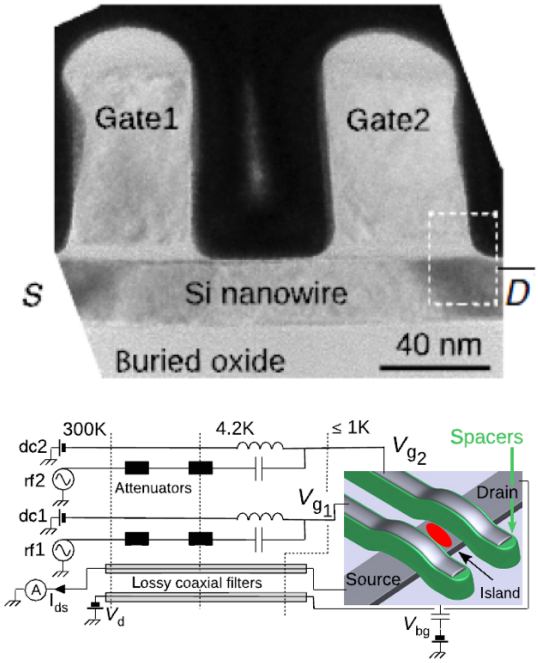

FIGURE 2.25: A conventional Si pump design from LETI. The quantum dot is drawn as a red point in (b). Both gates are connected to an individual RF source. The quantum dot is modulated by the back gate connected to the substrate.[75]

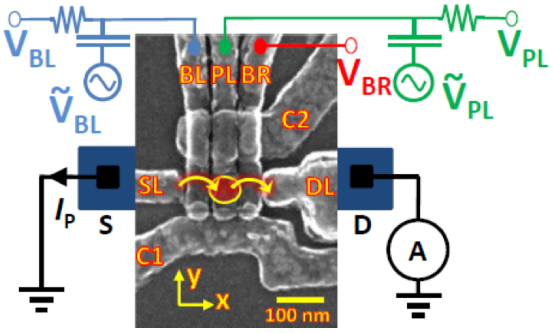

FIGURE 2.26: A Si pump design from UNSW. The quantum dot is drawn as a red point. Both gates BL and BR are connected to an individual RF source. The quantum dot is modulated by the PL.[77]

The quantum dot can also come from natural-defined structures, such as dopants and charge traps. They are also used as the quantum dot in the single electron pumps. NTT contributes a lot to this area. They tried to deliberately place a single dopant by ion implantation as shown in Fig. 2.27[78]:

In this device design, they used arsenide atom as the quantum dot. They show that the threshold voltage of the I-V characteristics would be shifted with back-gate bias to prove the single electron transfer was through the single dopant rather than quantum dot formed by gates[78]. The performance was not good compared with the gate-defined structures, possibly coming from the large scale of the device.

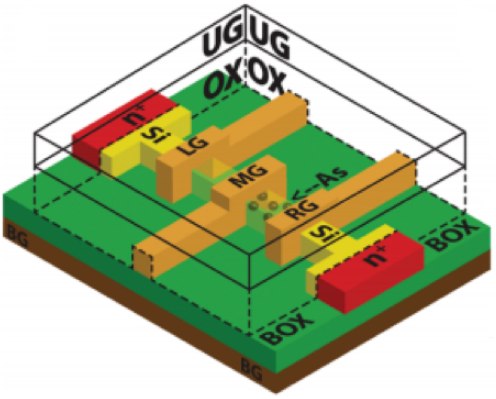

FIGURE 2.27: A Si dopant pump design from NTT. The quantum dot is the As dopants between MG and RG. The quantum dot is modulated by the upper poly-Si gate.[78]

In 2014, instead of using deliberately positioned atom, they tried to find devices with natural-formed trap as the quantum dot[79, 80]. The device structure was similar as the ordinary single electron pump they fabricated:

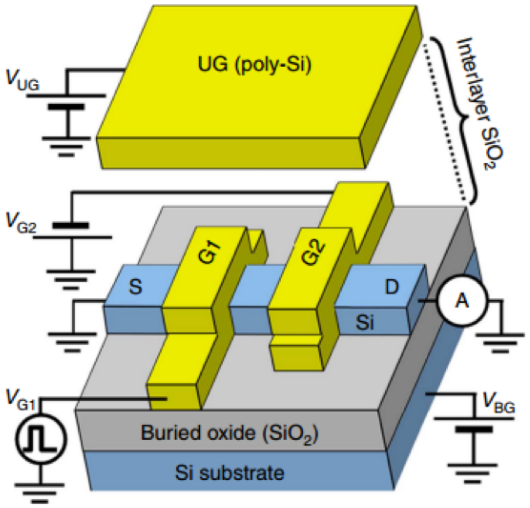

FIGURE 2.28: A Si trap pump design from NTT. The quantum dot is a trap located between G1 and G2. The quantum dot is modulated by the upper poly-Si gate. The G1 is connected to an RF source.[79]

The device was measured at 300 mK with 1 GHz operation, and the accuracy was found to be around 0.92 ppm[81]. The activation energy of the charge trap was estimated to be 37 meV according to their model.

However, the yield of this kind was extremely low: 1 per 100 devices. The fabrication of the trap-based pump was very unreliable at the moment. Scientists are trying to find methods to precisely place single dopant, but is it still far from reliable fabrication[82, 83].

As discussed in the quantum metrology triangle, the electron-counting scheme is required in the ideal design for the single electron pump. Although it is not mandatory regarding the operation of the single electron pump, it will help scientists monitor the number of

electrons in the island, and therefore have a better understanding on the non-adiabatic single electron transfer process in the single electron pump. The basic idea of the electron-counting scheme is shown in Fig. 2.29:

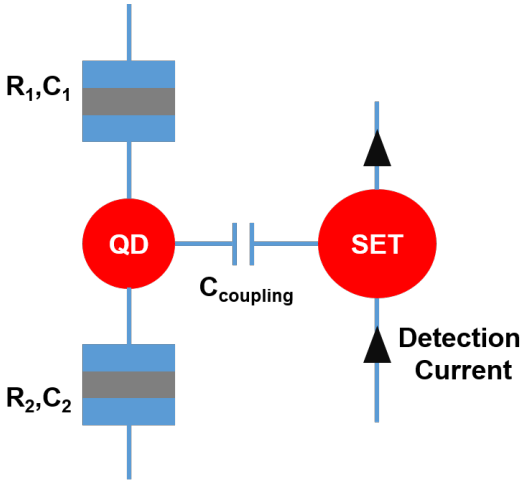

FIGURE 2.29: Schematic of circuit diagram for charge detection scheme. The SET is used as a current sensor.

A detector, which is usually a single electron transistor, is capacitively coupled with the quantum dot. The parameter of detector should be carefully designed to make sure it is working at its most sensitive point when there is one electron in the island. If a transfer error occurs during the operation, ideally, I could observe the error by the shift of detect current[84, 85]. In this way, I could estimate the error rate and improve the accuracy of the system. Besides, this structure is able to detect loading and ejection processes separately, and scientists are able to investigate the device physics with more details.

However, practically, the detection bandwidth of the detector usually limits the operation of single electron pump[86, 87]. The operation frequency still needs to be improved to satisfy the requirement for the quantum metrology triangle[88].

NTT groups have fabricated a single electron pump with a CMOS-compatible silicon single electron transistor as the charge detector[89]. The device design is shown in Fig. 2.30:

They successfully operated the device with a properly working detector at 10 MHz. The error rate was around 100ppm. They could clearly see when the transfer error happens by looking at the detection current flowing through single electron nanowire FET, and they find the error was dominated by error in the loading process[90].

UNSW group was also able to make a pump using their side-gate structures with single electron counting scheme. The result is shown in Fig. 2.31:

The counting scheme was also a single electron transistor in their design. The unique feature of their design was that they added a PID controller in the detection system[91]. The PID controller was used to fix the operating point of the detecting single electron

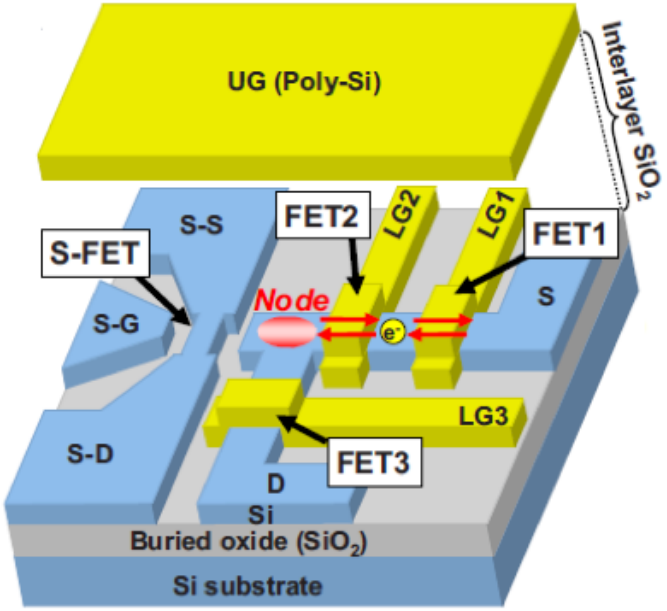

FIGURE 2.30: A Si pump design with charge-detection scheme from NTT. The charge detection scheme is a Si single electron transistor capacitively coupled to the electron node.[89]

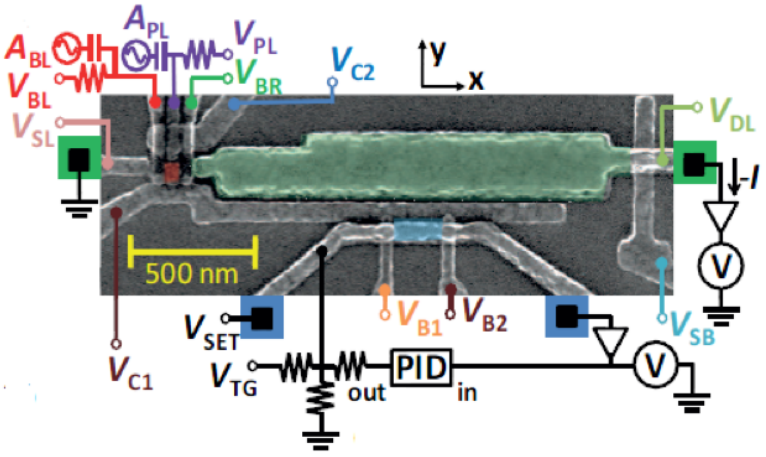

FIGURE 2.31: A Si pump design with charge-detection scheme from UNSW. The charge detection scheme is a Si single electron transistor, controlled by B1 and B2, and capacitively coupled to the electron node.[91]

transistor to make sure it is working at its most sensitive point. They claimed that this design would help to reduce the low-frequency noise and give a better performance.

The device was measured and only achieved the accuracy of around 10%. The problem was the weak coupling between the single electron transistor and single electron pump actually limited the operation.

In total, the detection bandwidth is limited by the weak coupling between the detection

single electron transistor and the single electron pump. This requires a lot of effort of improvement in fabrication in order to reduce the distance between the detection part and single electron pump, which will enhance the coupling between them.

2.4 Fabrication of Si nanowire device

From the designs introduced in the previous part, I could find that one of the key elements of silicon single electron pumps is the silicon nanowires.

Silicon nanowire is usually defined as a quasi-one-dimensional structure with its cross-section dimension of 100 nm or less[92]. The surface to volume ratio is extremely large in silicon nanowire, which results in much better control of the potential level than devices based on bulk silicon[93]. The silicon nanowire has been used in the design of many different devices, e.g., single electron devices[94], tunnelling-field-effect-transistor[95], solar cells[96] and so on.

The way to fabricate silicon nanowire devices can be classified into two categories: top-down processes and bottom-up processes.

Top-down process is the conventional way to fabricate silicon nanowire[97]. It is a more mature process compared with the bottom-up process, and is therefore much more reliable thanks to the compatibility with the state-of-the-art CMOS fabrication platform[98, 99]. However, it is not a self-aligned process and therefore hard to form complex structures[100]. A typical top-down process to fabricate silicon nanowire is shown as below:

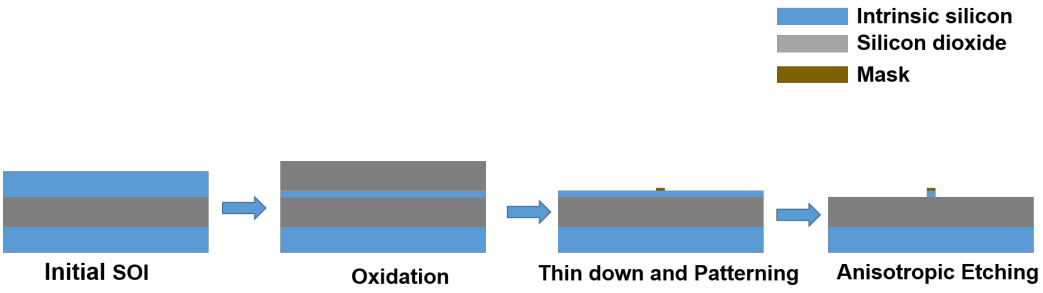

FIGURE 2.32: Schematic Diagram of a Top-Down Process. The thin-down process is achieved by oxidation and HF etching. The wire is finally formed by anisotropic etching process.

The fabrication of silicon nanowire is usually based on a silicon-on-insulator (SOI) wafer. The thin-down process is normally achieved by oxidation and following HF wet etching. After the thin-down process of silicon nanowire, the mask is patterned, and anisotropic etching is applied to define the nanowire regime. Reactive Ion based etching has a better vertical profile, while wet etching gives less roughness and charge traps at the nanowire surface[101]. Silicon nanowire is a quasi-1-D dimension structure, so it is very sensitive

to the surface properties. Compared with dry etching, anisotropic wet etching is easier to realise good performance and reliability.

For silicon, one of the most common wet etchant is TMAH (tetramethyl ammonium hydroxide), which is metallic-free, nontoxic and IC-compatible[102]. TMAH will etch silicon <100> plane and the boundary of etching area is defined by <111> plane, and will create undercut on the mask as shown below:

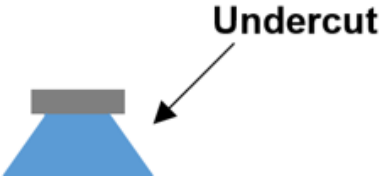

FIGURE 2.33: Schematic Diagram of TMAH Undercut in a <100>-oriented SOI wafer.

The undercut of TMAH etching is one of the main issues in TMAH application. The undercut depends strongly on the selectivity between <111> and <100> plane: the higher the selectivity, the smaller the undercut. The reason for this anisotropic etching is not fully understood at the moment, but has been confirmed to have relationship with the density of atoms between planes. The active energy required to remove an atom from <111> plane is also larger than <100> plane, which may also contribute to the selectivity[103].

One of the most common method to improve the performance is using IPA as the solution of TMAH instead of traditional water solution[104]. The undercut and smoothes are both significantly improved with the additive of IPA.

It is also possible to grow the Si nanowire by the bottom-up process. The bottom-up process is firstly developed by Wagner and Ellis[105]. They use VLS (vapour liquid solid) growth to form silicon nanowire as shown below:

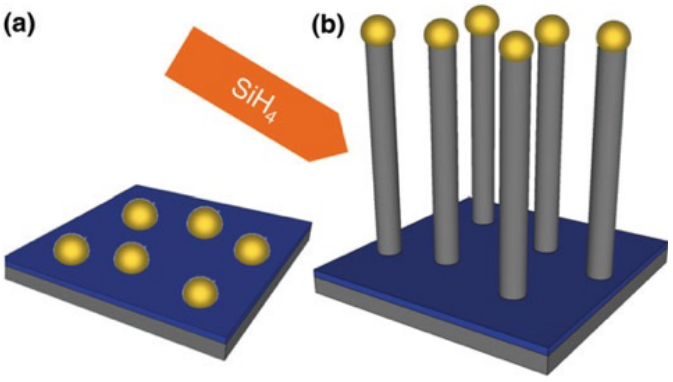

FIGURE 2.34: Schematic Diagram of Bottom-up Process. The nanowire is grown by using gold particle as catalyst.[105]

In the bottom-up process, first, physical vapour deposition process is applied to form an ultra-thin gold layer, and then the surface is annealed to generate single catalyst

particles. The catalyst particles are therefore placed on top of the surface in the first step and will act as a silicon collector. Then, high-order silane gas flow is sent to the system, and silicon nanowire will automatically start to grow on the particle.

There are several advantages of this process[106]. Unlike top-down way where nanowire can only form on top of oxide layer, silicon nanowire is able to be grown on different types of substrates. Besides, bottom-up process is able to achieve vertical silicon nanowire, which is very difficult to fabricate with top-down processes.

However, the high-precision placement of the gold particles is still a significant problem and therefore reliability of this method is much poorer than bottom-up processs. Also, gold is a very dangerous particle in silicon fabrication process due to its large diffusion coefficient which would potentially cause device failure, so it is still not fully compatible with the modern CMOS fabrication. Some gold-free process has been proposed to avoid this problem[107, 108].

Reliable fabrication of silicon nanowire remains a problem in the semiconductor industry. The difficulties stay in many processes including alignment, doping, contact, dielectric and so on.

The alignment of silicon nanowire is critical. E-beam direct writing lithography is usually used to fabricate silicon nanowire. However, it is not practical in the actual industry manufacturing due to the extremely low writing speed. For the bottom-up process, people usually use a damascene process[109] to form silicon nanowire. They would create patterns in the dielectric to form slots, and grow silicon nanowire in these slots to align the fabrication with the pattern. Traditional CVD can only form poly-crystalline silicon nanowires using this technique, and catalyst must be used to form single-crystalline silicon. Several techniques on alignments, such as electric-field alignment[110] and microfluidic alignment[111], have been proposed, but they all have either yield problem or integration density limitation.

The doping of silicon nanowire is also a significant issue. The small size makes it very difficult to implant precisely. Besides, ion implantation will also damage the surface of crystalline silicon, and is hard to recover due to the thin nanowire. In-situ doping bottom-up processes have been proposed[112], but high doping concentration is still difficult to be achieved.

It is also not easy to form a good Ohmic contact with silicon nanowire[113]. Usually silicide is used to solve the problem[114].

The gate dielectric is one of the most challenging and activing research field in silicon nanowire. The gate dielectric must be fabricated very carefully to avoid any traps in silicon-oxide interface, as silicon nanowire is a quasi-one-dimensional structure and extremely sensitive to the surface roughness or charge traps. Silicon dioxide was used in the

early stage due to its good interface quality[114]. High-k dielectric atomic layer deposition is also a good choice in fabricating when the device is scaled[115], but the interface quality and mobility degradation are significant issues and limiting the performance of silicon nanowire devices[116, 117].

In total, there are many challenges in the actual fabrication of Si nanowire devices, including alignment, doping, dielectric quality and so on. As a result, I need to take extra care of the fabrication for the single electron pump, which is based on Si nanowire.

In our device design, in order to modulate the quantum dot more precisely, I will choose similar structures with NTT group design, with double-layer triple gates. In this case, I have an individual top gate to modulate the potential and give extra confinement to the electrons in the quantum dot. This design is CMOS-compatible fully-Si process, and therefore has the potential for mass production.

I can still make some improvements based on their design. First, the Si nanowire in NTT group design is formed from anisotropic dry etching. It is not easy to control the interface condition in dry-etching, as it is easy for the plasma to damage the surface and therefore form traps. In our device, I will use TMAH to perform anisotropic wet etching, in order to create an atomically-flat nanowire surface. This will reduce the trap density and improve the reliability of the device. Second, they use deposited SiO_2 as the insulating oxide between lower gates and the top gate. In order to reduce the leakage, significant thickness of oxide is required. In our design, I will oxidise the poly-Si to create insulating oxide. This thermal Poly-Si oxide will have a better quality, and therefore thin insulating oxide can be achieved. This will improve the scaling ability of our design.

Based on all these discussions and understandings, I will fabricate our own single electron pumps. The fabrication processes of my single electron pumps will be shown in detail in chapter 3.

Chapter 3

Fabrication of Single Electron Pump

I have successfully fabricated a batch of single electron pump, using the facilities from Southampton Nanofabrication Centre. In the following part, I will introduce the mask design and layout for the single electron pumps, and then go through the fabrication process flow to show the actual fabrication process of single electron pumps based on our design.

3.1 Overview of the device layout design

As discussed in the previous part, my single electron pumps will be similar to the NTT device structure. However, I will use TMAH wet etching to form an anisotropic nanowire surface, and use thermal poly-Si oxide as the insulating oxide between the gates. Schematic diagrams of the device structure in the key operation region are shown in Fig. 3.1.

Seven e-beam lithography steps are required in this lot: Alignment Mask Layer (A), Silicon Nanowire Layer (L), Dopant Layer (D), Polysilicon First Gate Layer (FG), Top Gate Layer (TG), Contact Window layer (Cont), Metal Layer (M1). The general mask layout of a die in the wafer is shown in Fig. 3.2.

There are totally 8 types of designs for the single electron pumps. and I will briefly introduce them here to show the motivation of the designs.

First, the difference is about the metal layer layout. For one categories of the design, the metal layer is made very large, so that only one device is allowed in a 2.5 mm $\times$ 2.5 mm subchip. These categories are named as 'Primary design' in Fig. 3.2. For the

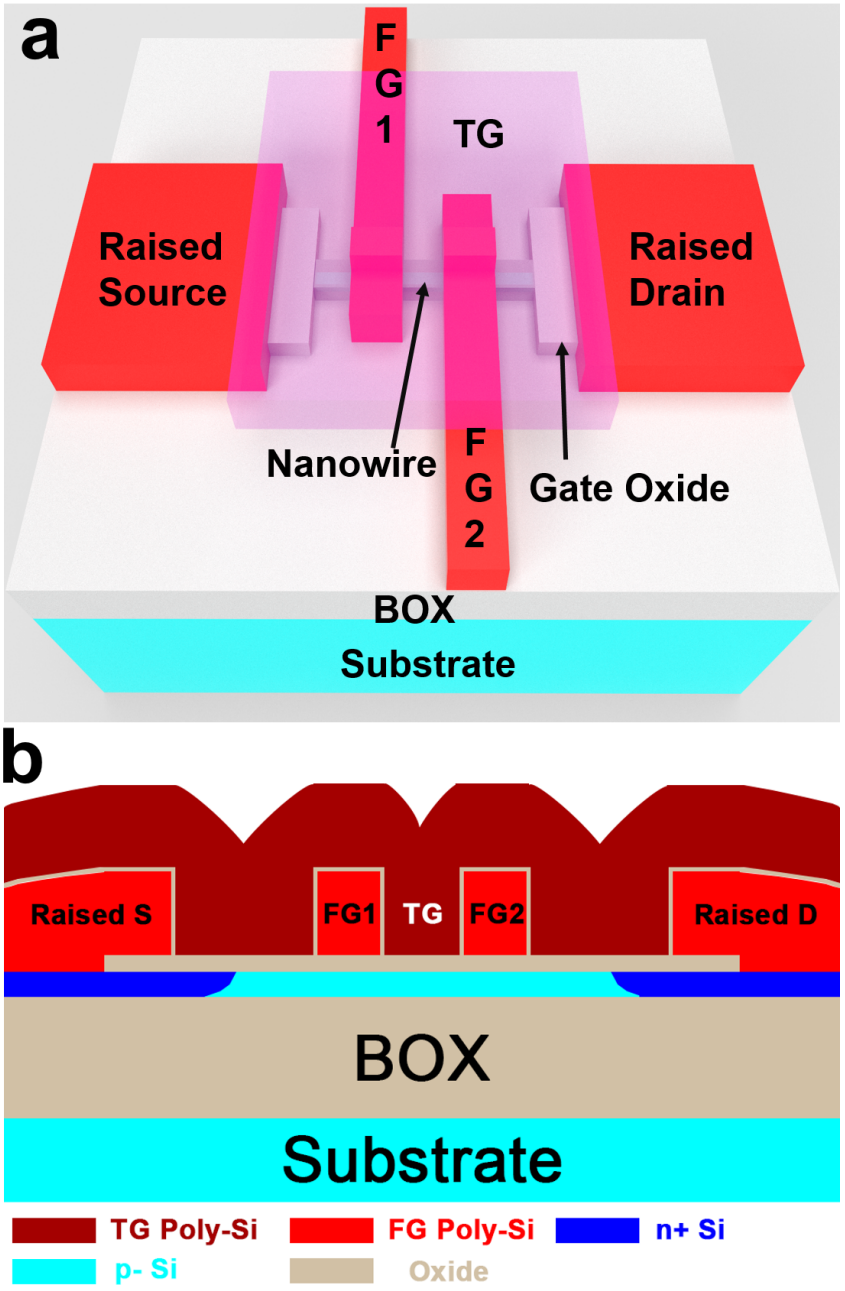

FIGURE 3.1: Schematic diagram of the device design in the key operation region. (a) shows the 3-D view of the proposed device structure, while (b) shows the ideal cross-sectional structure of the device. The metal connection part is not shown in the schematic diagram.

other categories, the metal layer is made small enough so that 16 devices are allowed in a subchip. These categories are named as 'Secondary design' in Fig. 3.2.

For one type of the design, I does not directly connect the large Si source/drain pads to the Si nanowires. Instead, I first connect the Si source/drain pads to Si pads with wide wires, and then connect the wide wires to the real Si nanowires. The purpose of

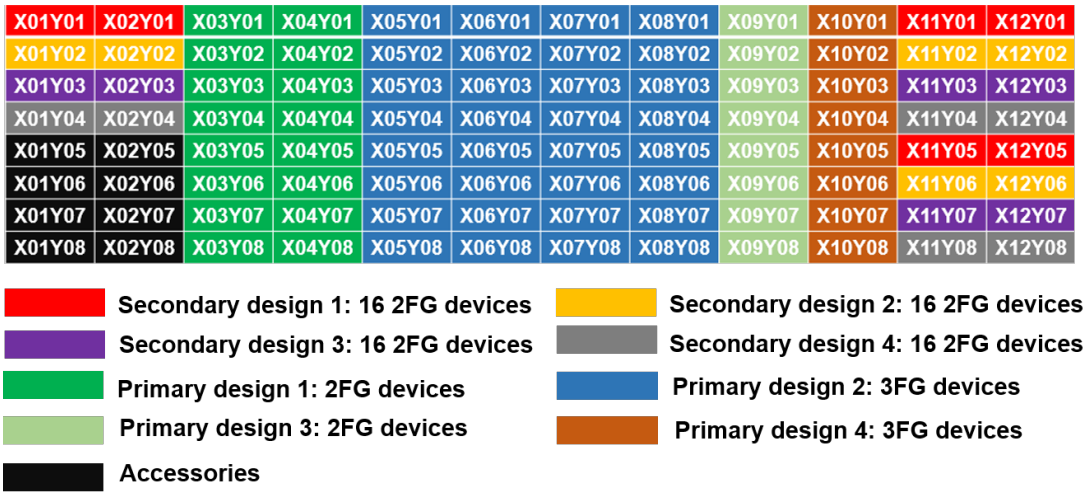

FIGURE 3.2: Layout arrangement of the mask design. The designs that each sub-chip will carry is shown in the figure.

this design is to minimise the e-beam diffraction on the Si nanowires. 'Primary design 1' and 'Secondary design 1' are realisations of this type.

For one type of the design, I expand the size of the large Si source/drain pads so that it will be directly connect to the Si nanowires. The purpose of this design is to reduce the resistance between the doped source/drain pads and the nanowires. 'Secondary design 2' is the realisation of this type.

For one type of the design, I expand the size of the Si nanowires so that it will be directly connect to the Si source/drain pads. The purpose of this design is to eliminate the e-beam diffraction on the Si nanowires. 'Secondary design 3' is the realisation of this type.

For one type of the design, I fixed the position of the dopant windows. As a result, the distance between the edge of the dopant windows and the Si nanowire will be different (while it is the same for the other designs.). The purpose of this design is to investigate the dopant diffusion length. 'Secondary design 4' is the realisation of this type.

For one type of the design, instead using two first gates, I will use three first gates. This design will help investigate the characteristics of the ejected electrons in the non-adiabatic operation. 'Primary design 2' is the realisation of this type.

For one type of the design, I will make a topological quantum dot in the same region where a quantum dot should be formed in the Si nanowire. This design will help investigate the characteristics of the quantum dot. 'Primary design 3' is the realisation of the two first gates version and 'Primary design 4' is the realisation of the three first gates version.

A detailed description of the design parameters, and the actual L-edit layouts, will be introduced in the appendix.

3.2 Fabrication Process Flow

The wafers used to fabricate single electron pumps are 6-inch <100> SOI wafers with 145 nm buried oxide layer. The thickness of silicon layer is around 100 nm. I have four wafers, wafer 1 (W1), wafer 2 (W2), wafer 3 (W3), wafer 4 (W4). The W4 is successfully fabricated, so in this part I will just introduce the fabrication process flow on W4. The detailed silicon thickness profile for the four wafers are shown in Fig. 3.3, respectively:

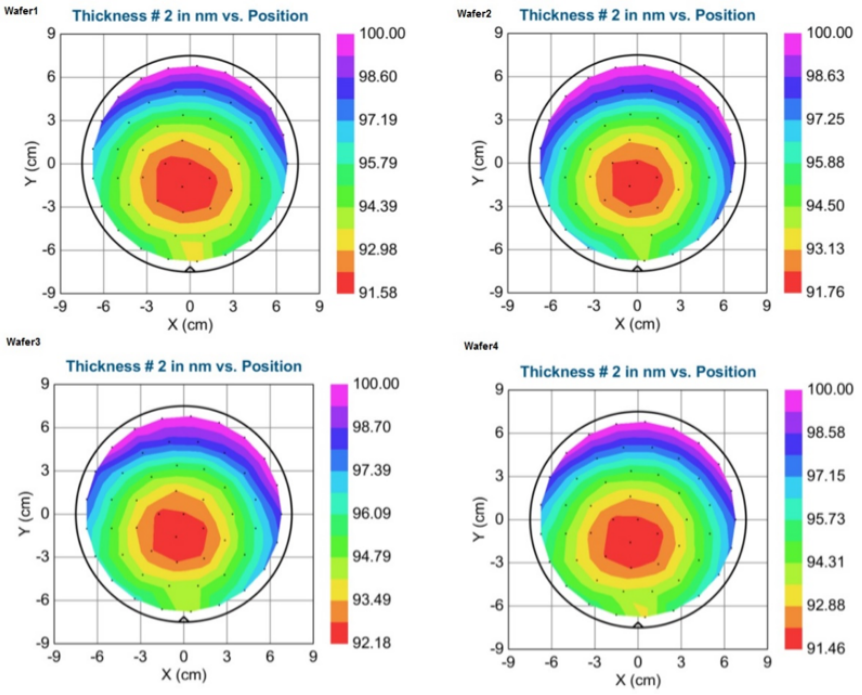

FIGURE 3.3: SOI thickness profile of the four wafers.

There are four dies, A, B, C and D, on W1, W2 and W3, while only A and B are fabricated on W4. The position for the four dies on the wafer are shown in Fig. 3.4.

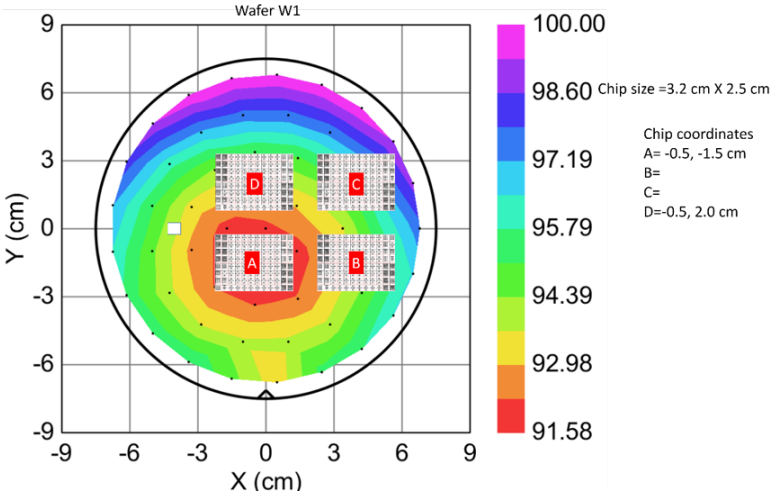

FIGURE 3.4: Position of dies on a single wafer.

A general fabrication process flow is shown in Fig. 3.5 as an example:

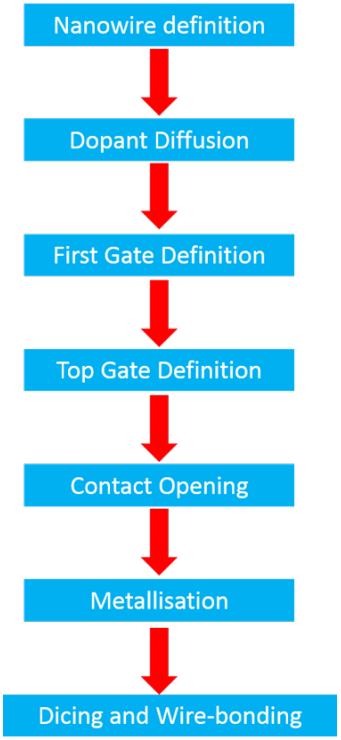

FIGURE 3.5: General fabrication process flow of the device designs, based on the e-beam lithography required.

3.2.1 Nanowire definition

As discussed in the background research part, the definition of nanowire include two steps: thin-down (vertical direction) and etching (planar direction).

The thin-down process was done by oxidising the silicon layer at 1000° C and remove the SiO_2 by HF. In our wafer, 54 nm-thick silicon layer was removed in this process. In order to achieve precise control, I removed the proposed silicon layer in two steps. 27 nm-thick silicon layer was removed in each step. In this way, the thin-down process is precisely monitored. Then I oxidised the Si surface to grow 20 nm oxide, which were used as hard mask in the e-beam patterning step.

Then I patterned the silicon nanowire, and reduced its size in the planar direction. The resist was 30 nm-thick HSQ (2% concentration), which was a negative resist and can be etched by SiO_2 etchant. After the patterning and developing of resist using e-beam lithography, I used RIE etching to etch the silicon oxide layer. However, the selectivity regarding HSQ and SiO_2 is poor (2:1) due to the intrinsic oxide property of HSQ. As a result, the etching process was performed in multiple steps to allow the precise control of Si dry etching. At the end of the etching process, there was only 5 nm SiO_2 covered on the nanowire regime.

After the e-beam patterning and dry-etching, I cleaned the surface using FNA, and then apply TMAH wet etching to define the width of nanowire. I used 25% TMAH etching with IPA, and applied 1500% over-etching in order to get a clean surface with no roughness at the edge. The schematic diagram of the structure after TMAH etching is shown below:

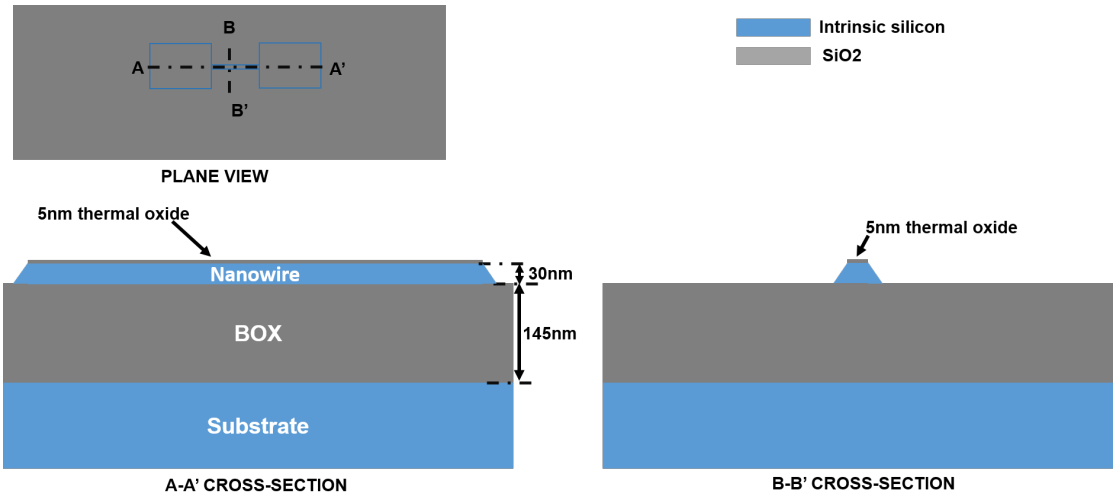

FIGURE 3.6: Schematic diagram in the nanowire definition step. Atomically-flat <111> nanowire surfaces are formed by TMAH etching.

An SEM image of a nanowire fabricated at this step (with the design nanowire width to be 50 nm) is shown below:

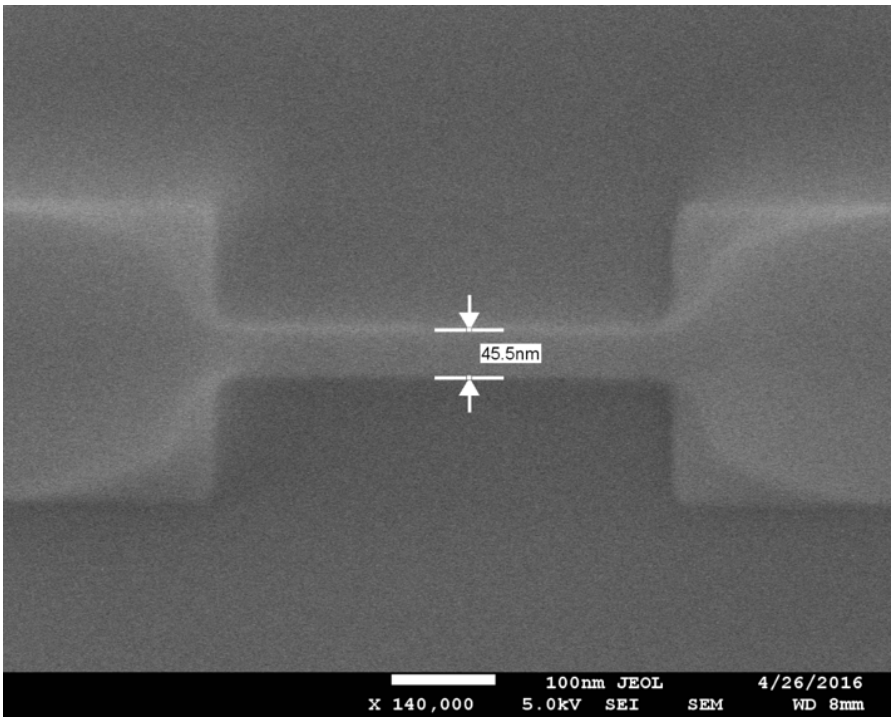

FIGURE 3.7: SEM image in the nanowire definition step. The HSQ mask is still covering the Si nanowires, and the width of Si nanowire is measured.

The width of nanowire measured from the SEM image was 45.5 nm, which was close to the design value. This shows a good alignment between fabrication and design.

3.2.2 Dopant diffusion Window

After the nanowire definition step, I removed the 5 nm SiO_2 hard mask, and then re-oxidised the silicon nanowire to form the 20 nm gate oxide. In this process, the scale of the device was also reduced in both vertical and lateral directions due to the thermal oxide.

In this single electron pump, I used raised source/drain technique in order to protect the S/D surface. As discussed in the literature review part, the doping of Si nanowire was difficult and might damage the surface. In our device, I deposited poly-silicon from LPCVD directly on top of S/D regime to protect the S/D nanowire surface, and useed the Poly-Si as the diffusion media.

In the actual fabrication step, after patterning of the dopant diffusion layer with PMMA950, I used wet process to remove the SiO_2 in order to get a clean and undamaged surface. However, the total etching time must be accurately controlled. Significant over-etching of SiO_2 will etch all the BOX layer underneath Si nanowire, and lift it off. In our fabrication process, I chose 50% over-etching to avoid this potential problem. An SEM image after the patterning process is shown in Fig. 3.8:

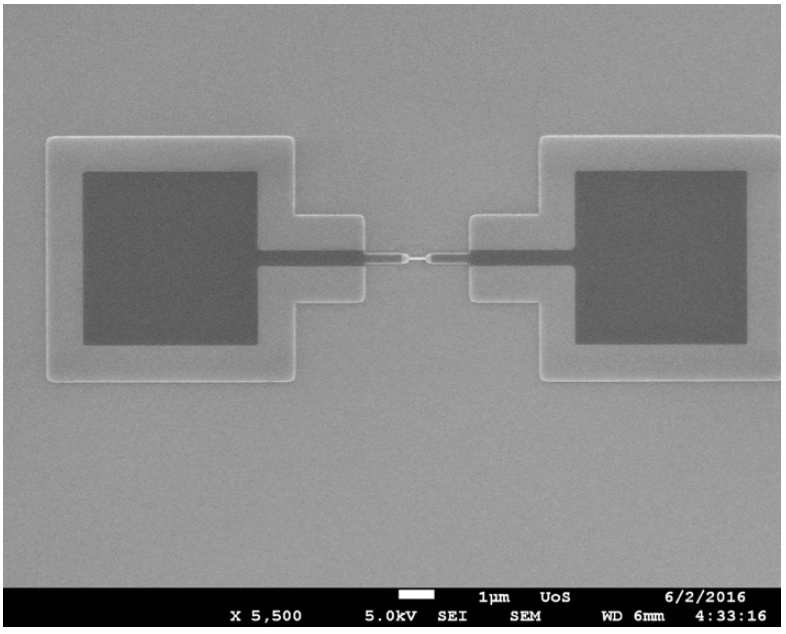

FIGURE 3.8: SEM image of a device before the dopant window opening step. The dopant window is shown as dark region in the SEM image.

After the patterning process, I used diluted HF to remove the native oxide, followed by depositing Poly-Si immediately to avoid the re-growth of native oxide. Then, I

will perform the dopant drive-in process using RTA. The dopant used for this drive-in process is P507 manufactured by Filmtronics, with 4% concentration of phosphorus. The diffusion time for this step is 1 minute, at 950° C, in N_2 environment. The time was determined by a test, which is introduced and summarised in the appendix. After this drive-in process, the remaining dopants at the Poly-Si surface were removed by 20:1 HF. At this point, the Poly-Si should be fully metallised.

A schematic diagram of the device structure up to this step is shown below in Fig. 3.9:

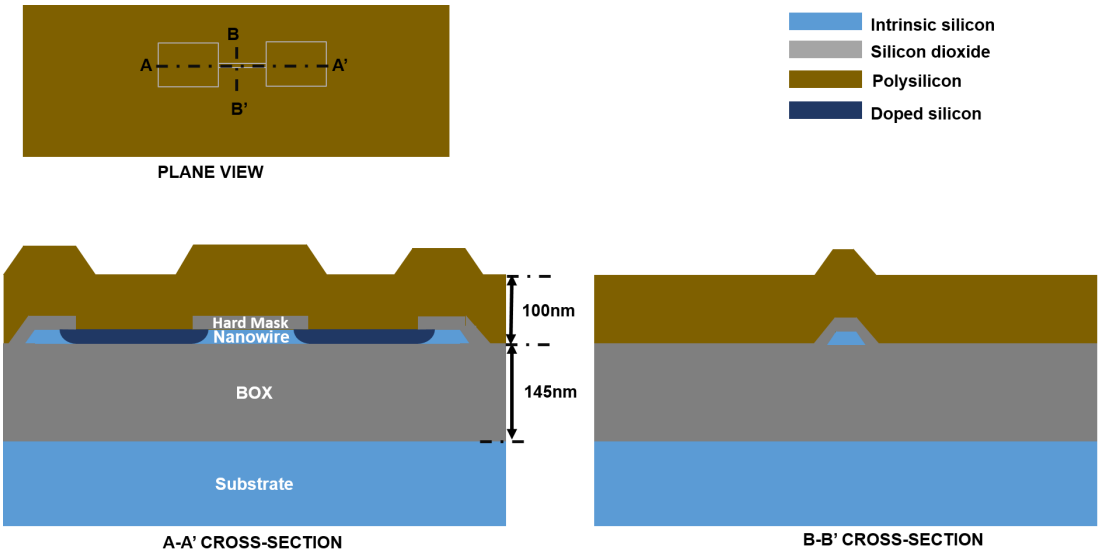

FIGURE 3.9: Schematic diagram of the device after the polysilicon deposition step. Direct connection between metallised poly-Si and crystalline-Si are made to allow the dopant diffusion.

3.2.3 First gates definition

After the dopant drive-in and metallisation process, I patterned the first gate layer along with the raised S/D regime. The e-beam resist used in this step is 100nm-thick HSQ (6% concentration). Thick resist is used to cover the steps originated from the step-height of Si nanowire. After patterning, I will use a carefully-developed ICP vertical etching recipe. This gas used for this ICP etching are HBr and O_2 plasma. I were able to achieve >30:1 selectivity between Si and SiO_2, with a vertical etching profile. The detailed information about this dry-etching recipe is included in the appendix. I applied the recipe to pattern the Poly-Si layer with 100% over-etching. The high-selectivity recipe was applied to make sure the gate oxide is well protected.

I confirmed that 50 nm/50 nm Line/Space is the minimum size that can be achieved with this e-beam resist and the ICP etching recipe, according to the SEM images obtained in the test.

A schematic diagram of the device structure up to this step is shown in Fig. 3.10:

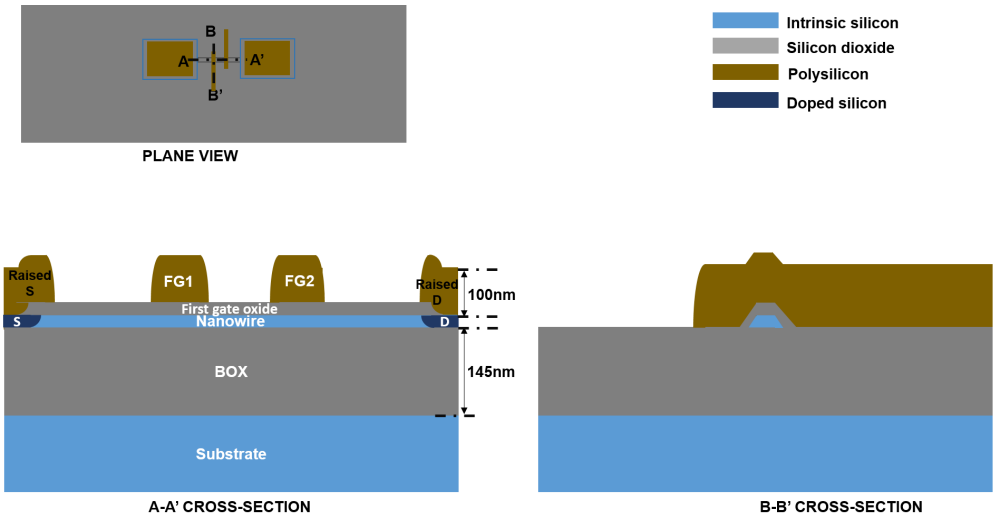

FIGURE 3.10: Schematic diagram of the device after the FG definition step. Two first gates are formed by ICP dry etching.

In Fig. 3.11, two SEM images of a device are shown in different scales, respectively. The device was with 50 nm designed nanowire width, 50nm gate length and 100nm gate spacing. I confirmed a good definition of FG gates, raised source and drain by the SEM images.

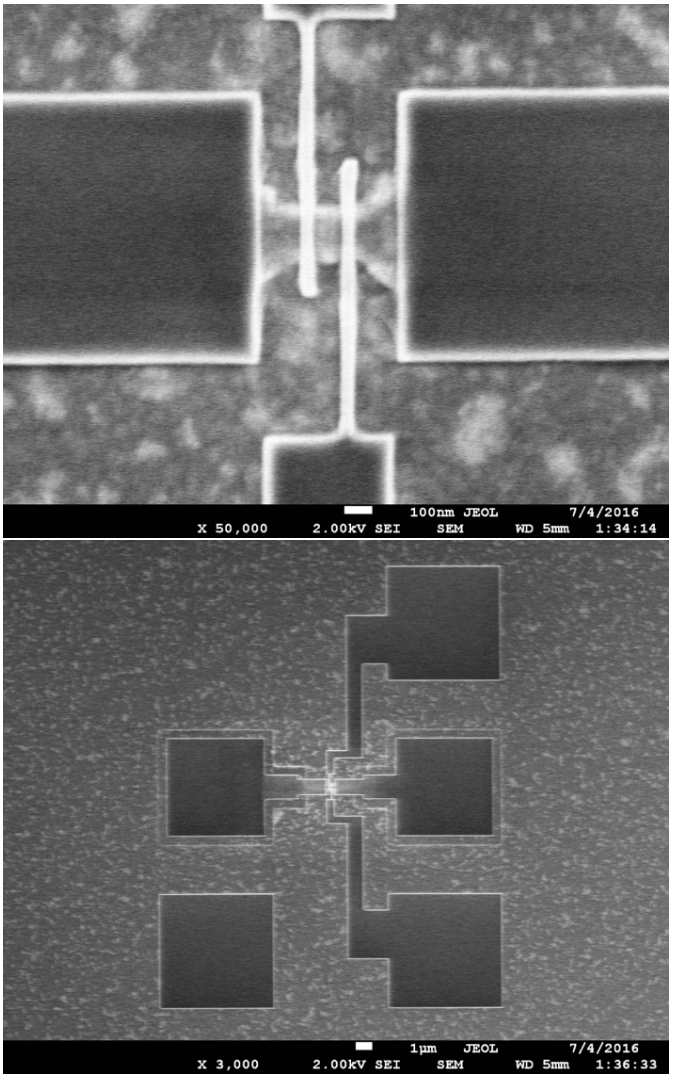

FIGURE 3.11: SEM image of the device after the FG definition step. Two first gates were clearly observed in the SEM image.

3.2.4 Top gates definition

After the FG gate definition, I used dilute HF to remove the damaged oxide ($\sim$ 5nm) in the previous step, and then perform an RTA oxidation (950° C for 3 minutes) to oxide the Poly-Silicon. This oxide is 6 nm, and was used as the insulating oxide between FG and TG layer.

After RTA oxidation, LPCVD Poly-Si were deposited. After the deposition process, dopant drive-in process was performed at 950° C for 1 minute in N_2 ambient using RTA. Next, the dopant was removed by HF, and the TG layer was patterned using 100 nm-thick HSQ (6% concentration). The high-selective HBr/O_2 ICP vertical etching recipe was applied again to pattern the top gate. A schematic diagram of the device structure up to this step is shown in Fig. 3.12:

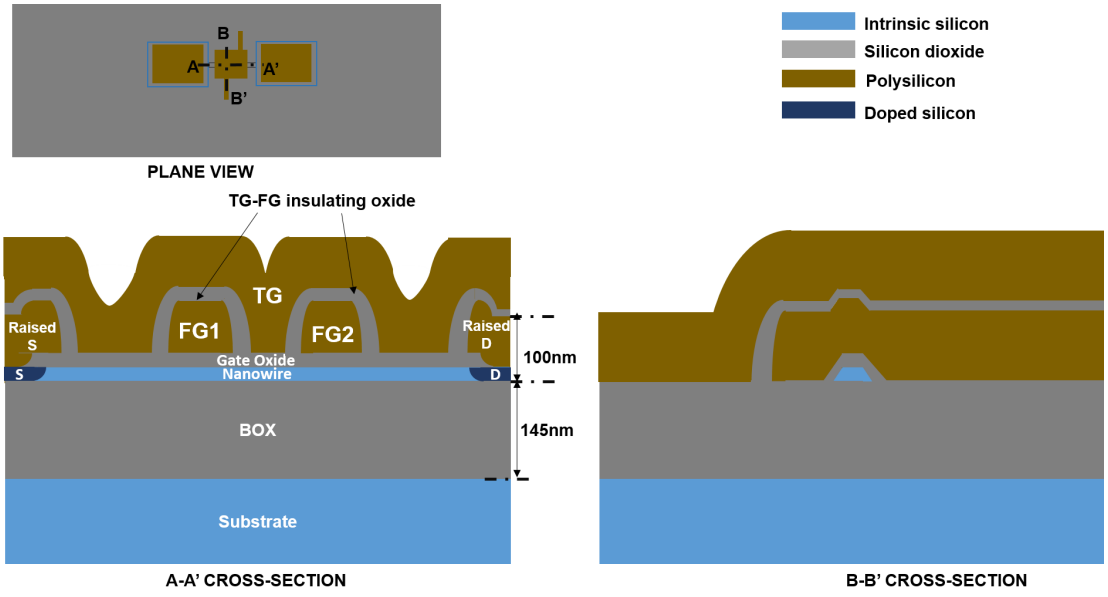

FIGURE 3.12: Schematic diagram of a device after the TG definition step. The insulating oxide is created by RTA thermal oxidation.

An SEM image of a device after the patterning of TG is shown in Fig. 3.13. From the SEM image, I confirmed a good definition of the top gate layer by the SEM images.

3.2.5 Contact Opening

After the forming of the top gate layer, I needed to deposit 250 nm PECVD oxide on the TG layer in order to passivate the device region and protect the devices from being contaminated. After that, I opened windows on the oxide regime covered raised S/D, FG and TG layer. The contact windows were used to form the direct contact between the metal and Poly-Si layer.

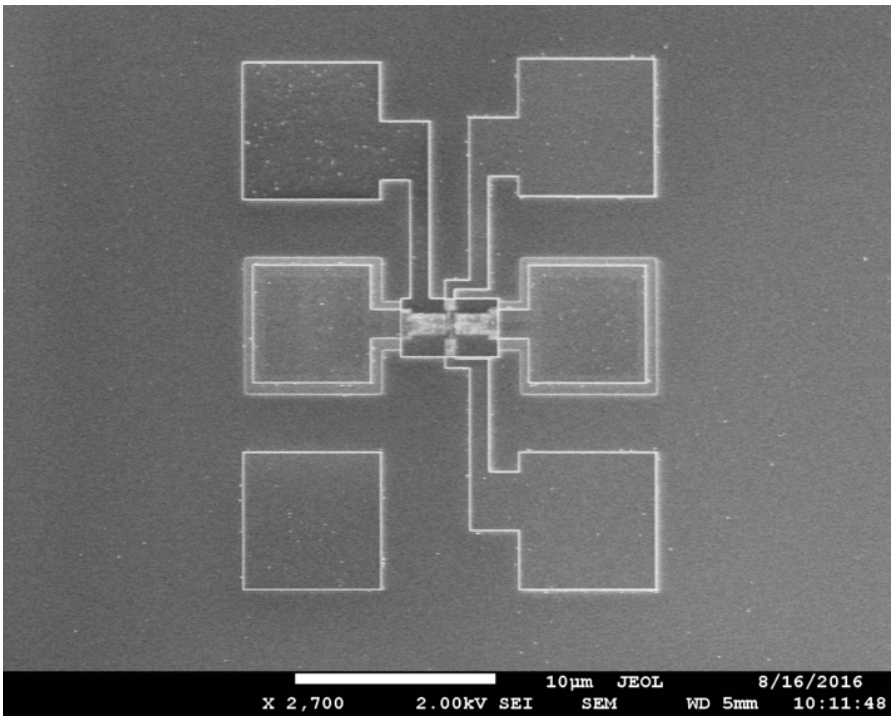

FIGURE 3.13: SEM image of a device after the TG definition step. Clearly-defined TG were observed.

ZEP was used as the resist for the e-beam patterning. After successful patterning of the cont layer, wet etching was applied to remove the SiO_2 covering the windows. Wet-etching was preferable than dry etching because it did not damage the Poly-Si surface and it will create smooth surface for the metal to cover. The time for the wet etching must be controlled accurately. If the wet etching was not enough, the metal was unable to form direct contact with the poly-Si layer. If the over-etching was too much, the contact would be larger than the area of the SOI layer, which will cause the possible short-circuit issue when patterning metals.

I chose 100% over-etching to make sure that a good contact is formed and the over-etching is not significant enough to form a short-circuit. An optical image of the device structure up to this step is shown in Fig. 3.14:

3.2.6 Metallisation

After the contact opening, I used lift-off process to pattern the metal layers. 300 nm PMMA/MMA is used as the e-beam resist. After successful patterning, I used HF to remove the native oxide on top of Poly-Si layer for a good quality metal-semiconductor contact, followed by immediately deposition of the metal by evaporation. The metal contained 180 nm Aluminium and 20 nm Titanium. Titanium was used as the barrier metal to stop the fast diffusion of Aluminium into Si layer.

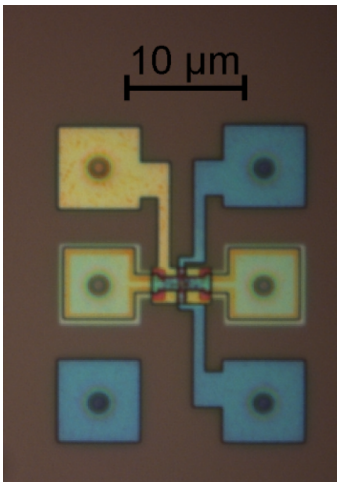

FIGURE 3.14: Optical image of the device after the Contact opening step. Wet-etched round contacts can be observed.

After depositing of Aluminium, I performed the lift-off process. NMP was used as the lift-off developer. Due to the insufficient thickness of resist (ideally should be three times the thickness of metal layer), I had to apply ultra-sonic wave to assist the lift-off process. However, this damaged the contact of Aluminium, which reduces the yield of the device.

After that, I performed the last step, which was forming gas annealing. As discussed in the background research, slight diffusion will help increase the contact quality, but significant diffusion would result in short-circuit. As a result, the annealing time must be well controlled. The devices were annealed at 450° C in H_2 and N_2 environment for 7 minutes. An optical image of the device after final metallisation is shown in Fig. 3.15.

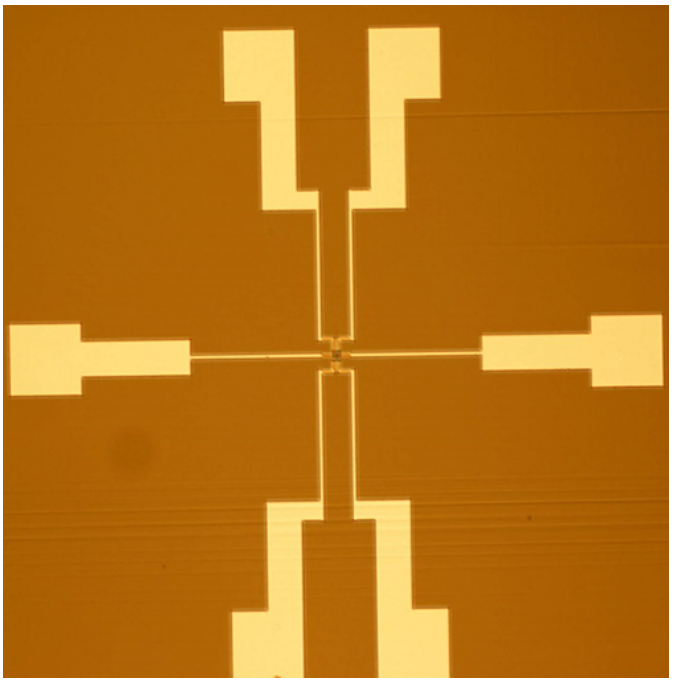

FIGURE 3.15: Optical image of the device after the metallisation. Metal layers can be observed.

3.3 Yield Analysation and summary

After the successful fabrication of the devices on the wafers, I performed the room temperature measurement to check the yield of the device. The result is summarised in Fig. 3.16.

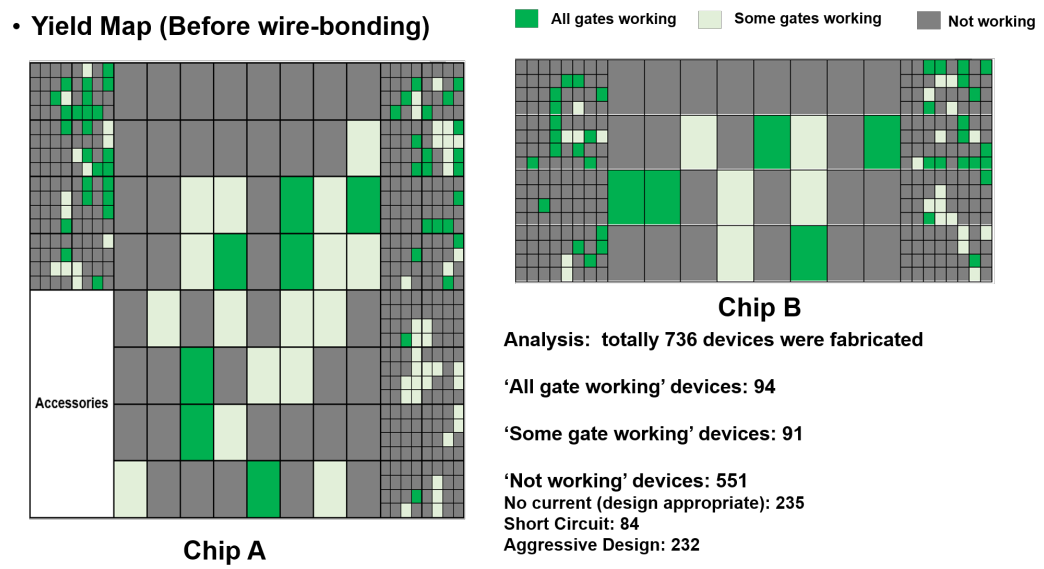

FIGURE 3.16: Yield summary of the wafer W4. The functionalities of each individual device are marked in a schematic die layout. 94 devices show complete functionalities.

736 devices were measured at room temperatures to confirm if the device is working. I found 94 devices are 'fully-working', which means all the FGs and TGs are functional and can turn off/on the device individually. For these devices, successful fabrication is confirmed, and the device has the potential to work as single electron pumps at low temperatures.

A typical output characteristics of the 'fully-working device' is shown in Fig. 3.17.

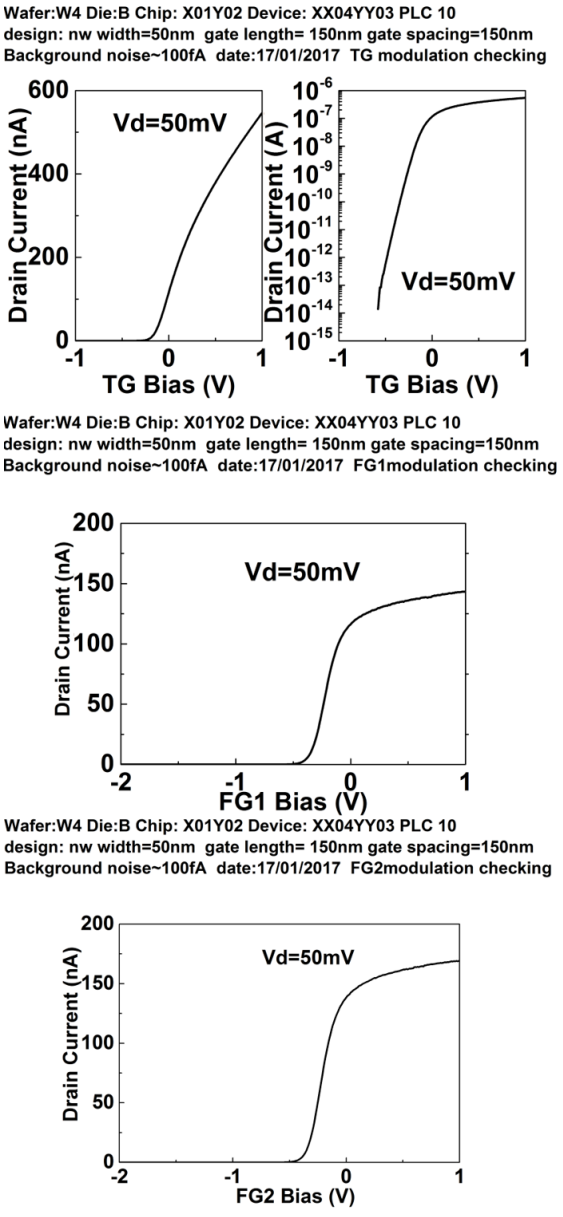

FIGURE 3.17: A demonstration of a fully-working device. All the gates are able to turn ON/OFF the transistor, showing ability to modulate the potential in the device channel.

91 devices have some gates working working, which means some FGs are functional while others cannot turn on/off the device individually. For these devices, the fabrication is not successful. The failure reason is attributed to the bad contact between the metal and poly-Si gates.

A typical output characteristics of the 'fully-working device' is shown in Fig. 3.18.

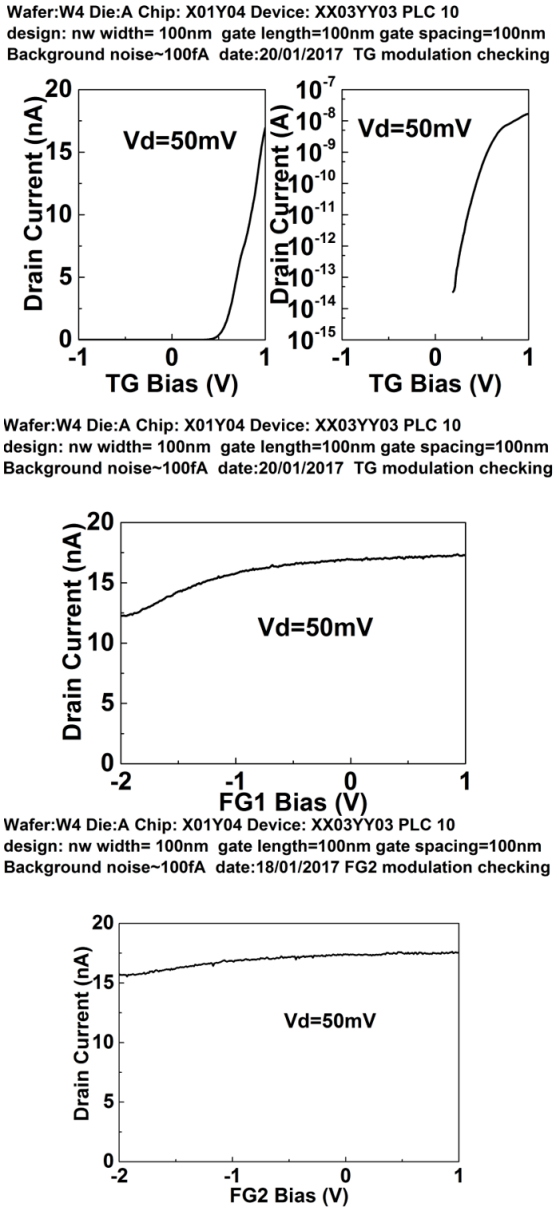

FIGURE 3.18: A demonstration of a partially-working device. The top gate is able to turn ON/OFF the transistor while both first gates are difficult to turn OFF the transistor.

551 devices were not working at all, i.e., no transistor characteristics were confirmed. The reasons are summarised below:

(1) For 232 devices, the failure reason is because of the aggressive design.

I include some designs with aggressive parameters, which were very hard to achieve due to the technique limit. For example, some devices are with 20 nm-wide Si nanowire, which will be fully oxidised due to the small scale. Some devices are with 50nm gate line-and-space, which is also very difficult to achieve with 100 nm-thick HSQ resist.

(2) For 235 devices, no current can be observed in the measurement, i.e., open circuit. This is because of the poor contact between source/drain electrode and poly-Si gate. One example is shown in Fig. 3.19, I can find damaged metal layers by optical microscope.

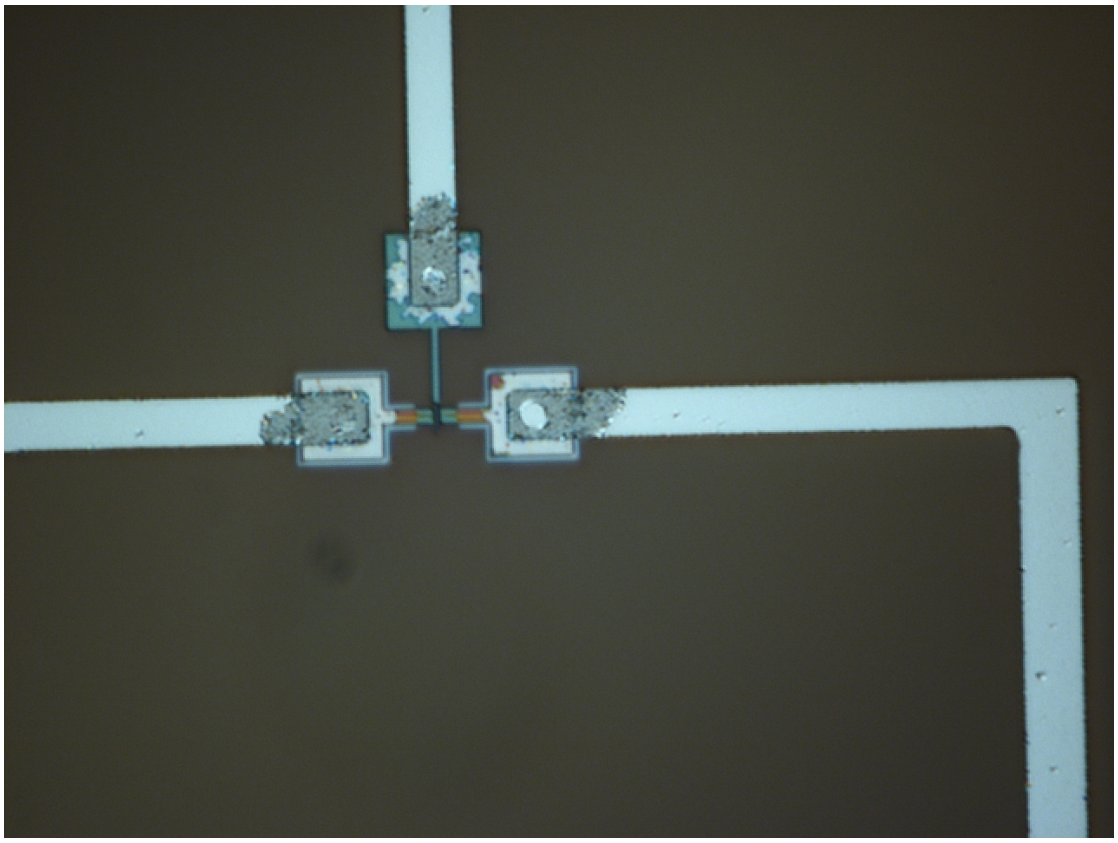

FIGURE 3.19: Failure mode: broken metal. The metal parts were broken due to the ultrasonic wave used in the lift-off process.

The typical output characteristics for a open-circuit device is shown in Fig. 3.20.

(3) For 84 devices, short-circuit have been observed in the measured. This is because of the poor interface quality of Titanium in the metallisation process. We think it is due to the large grain size of Titanium, for some devices, the Aluminium is able to diffuse and penetrate through all the Si nanowires because of the absence of the barrier metal. Therefore, the device is short-circuit. Further tests need to be performed to confirm this guess.

The typical output characteristics for a short-circuit device is shown in Fig. 3.21.

(4) For the other two devices, I found the gate oxide broken. This may be because of static charge or poor-quality oxide.

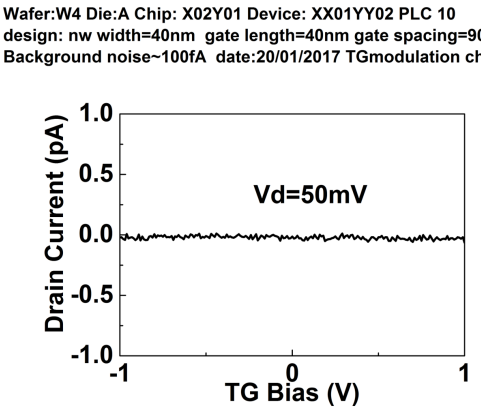

FIGURE 3.20: A demonstration of an open-circuit device. No current was detected in the device.

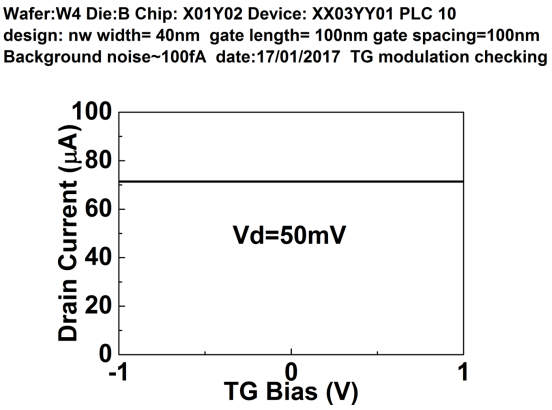

FIGURE 3.21: A demonstration of a short-circuit device. Large current was detected in the device.

The total yield is estimated to be 94/736=12.5%, which is not good enough for the standard of a reliable fabrication.

In total, in order to improve the yield and fabrication reliability, the following processes should be done and improved:

(1) I need to accurately estimate the fabrication limit in our facilities based on the outcome from this fabrication lot, and optimise the design parameters to avoid associated failure.

Basically, the design needs to be optimised to avoid the huge amount of failure device due to careless designs.

(2) I need to improve the metal patterning technique, to avoid the damage due to ultra-sonic in lift-off process.

There are several strategies to improve:

First way is to use optical lithography istead of e-beam, with thicker optical resist like S1813, which is roughly 1 μm. With thicker resist, it will be easier to lift-off all the

Aluminium layer, and no ultra-sonic is required. In this way, the quality of metal contact is protected. The drawback of this strategy is the larger design tolerance required due to the thicker resist. Also, the alignment is not easy due to the limit of photo-lithography.

Second way is to use dry etch instead of Aluminium. I can use HBr/Cl_2 gas-based ICP dry etch to pattern the Aluminium layer. In this way, I do not need ultra-sonic so the metal layer will be protected. Also, it is the standard process in the industry for CMOS patterning. The drawback of this strategy is the HBr/Cl_2 recipe also etches Si, therefore any mistake in actual operation will result in unrecoverable failure. I need to process very carefully and deposit thick-enough resist to protect the device.

(3) I need to improve the surface quality of barrier metal and check the suitable annealing time carefully.

In this fabrication lot, many failure is due to the short-circuit between source and drain. In order to improve that, I need to improve the quality of barrier metal, i.e., optimising the deposition recipe or use sputter to deposit TiN. Also, I need to check the suitable time for the forming gas annealing, so that the time is enough to passive all the charge traps in the oxide, and no significant penetration will be observed.

By following all the three points listed above, the yield and quality of the single electron pump fabrication will be significantly improved, which will be a future target and work for this project.

Chapter 4

Measurement of Single Electron Devices

The measurements in section 4.2 were carried under the supervision of Dr. Jonathan Fletcher, Dr. Stephen Giblin and Dr. Masaya Kataoka in NPL.

The Si single electron pump is based on gate-defined quantum dots. In order to achieve the target of mass-production for the single electron pumps, the device characteristics and reliability impact factors of the Si quantum dot devices must be understood. I will start from analysing the characteristics of naturally-formed quantum dots in Si MOSFET structures, and the reliability impact factors of the Si quantum dot devices. The results are shown in section 4.1. Then, I will directly investigate the device characteristics of single electron pump fabricated in Chapter 3, try to demonstrate the quantised current, and analyse how the reliability of the single electron pumps will be affected. The results are summarised in section 4.2.

4.1 Measurement of Si quantum dots in advanced MOSFETs

The key component of Si single electron pumps I fabricated is based on the conventional MOSFET structure. In order to have a better understanding about Si single electron devices based on conventional MOSFET structures and their performance impact factors, I measured some short-channel, industrial-level MOSFETs, which were fabricated by Hitachi, at cryogenic temperature. By analysing the measurement results, I will have a better understanding about the characteristics and performance impact factor of single electron pump devices at low temperatures.

Three of the MOSFET devices have been successfully measured, and the information of the devices are shown in Tab. 4.1:

TABLE 4.1: Successfully measured devices

No.	Device Type	Channel width	Channel length	Gate Oxide Thickness
1	PMOS	10 μm	55 nm	2.4 nm
2	NMOS	10 μm	75 nm	2.4 nm
3	PMOS	10 μm	75 nm	2.4 nm

They are both wide-and-short-channel devices. The short-channel is for the observation of single electron characteristics, and the scale is similar to the device I fabricated; The wide-channel is for the larger chance to find the impact of charge traps or surface roughness, in order to investigate the performance limit factors.

4.1.1 SET Characteristics and Investigation

The drain current (I_d) on the gate bias (V_g) of device 1 (p-type MOSFET, 10 μm wide and 55 nm long) and and device 2 (n-type MOSFET, 10 μm wide and 75 nm long) were measured at room temperatures and 5 K, and is shown in Fig. 4.1[118].

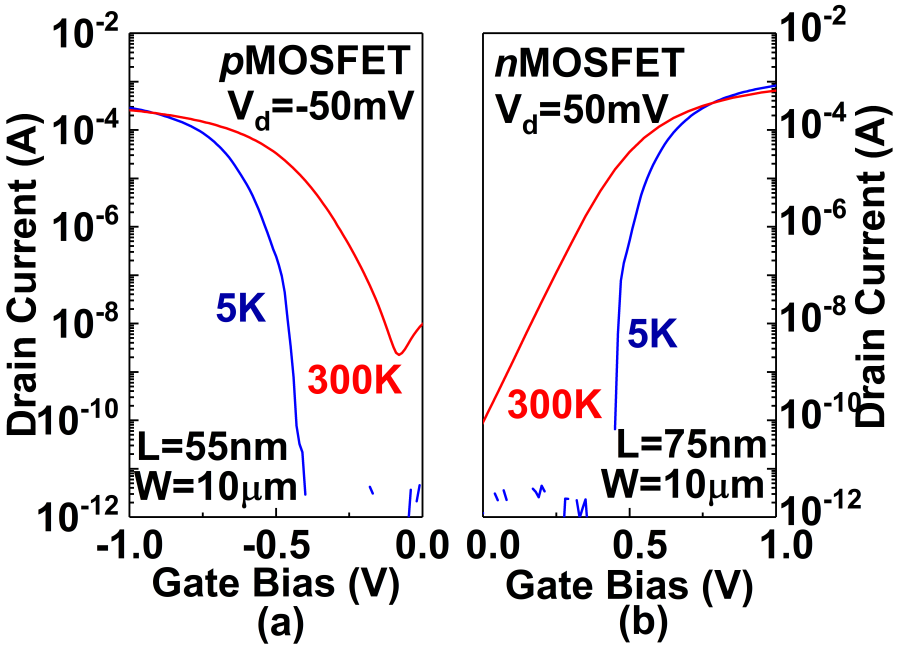

FIGURE 4.1: I_d-V_g characteristics of device 1 at cryogenic and room temperatures.[118]

The threshold voltage was -0.45 V at 300 K and -0.60 V at 5 K for the pMOSFET, and 0.47 V and 0.62 V for nMOSFET, respectively. The on-currents were higher at 5 K for both devices because of the increase in both mobility[119] and saturation velocity[120]. The subthreshold slope was 82.4 mV/decade at 300 K and 14.9 mV/decade for the pMOSFET, 80.3 mV/decade at 300 K and 5.7 mV/decade for the nMOSFET. The resistance at sub-threshold regime is larger than 25.8kΩ, which is a necessary condition to observe single hole/electron effect.

Current blockade due to single-electron/hole effects was observed in both devices at 5 K, as shown in Fig. 4.2.

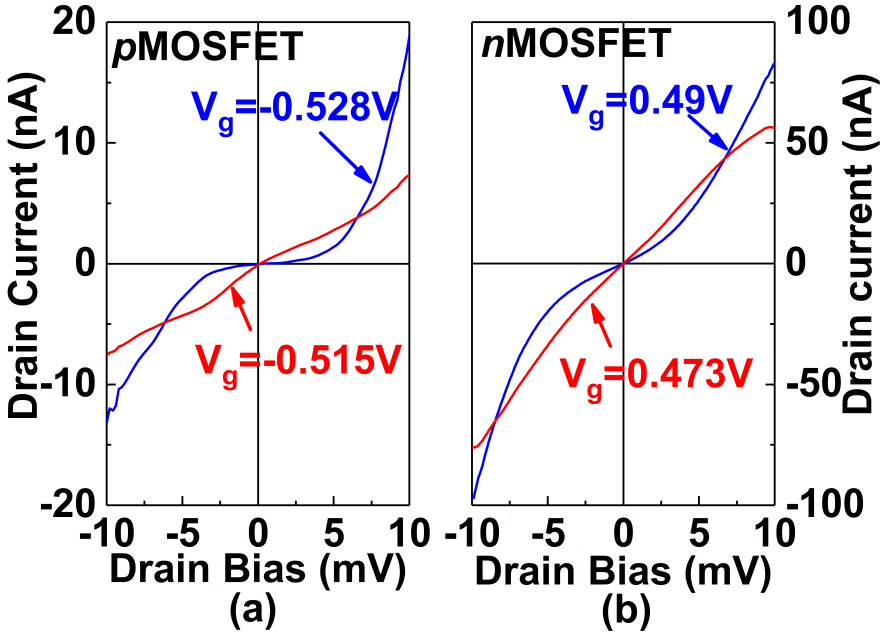

FIGURE 4.2: I_d-V_d characteristics of device 1 at cryogenic and room temperatures.[118]

It is clear that the current was shifting between ON/OFF states in both devices. In the *p*MOSFET, as shown in Fig. 4.2(a), when the gate is biased at -0.53 V, I_d was clearly blocked between -2.5 mV and 2.5 mV. When the gate is biased at -0.515 V, no blockade on the system was observed, and I_d was therefore clearly at ON state. Similar characteristics can be observed in the *n*MOSFET, as shown in Fig. 4.2(b). This dependence of the non-linear I_d-V_d characteristics on the gate bias, which has most likely originated from the Coulomb blockade phenomenon, implies the presence of quantum dot in the channels of both devices.

The Coulomb diamonds were observed in both *p*MOSFET and *n*MOSFET respectively, as shown in the figure in Fig. 4.3. This confirmed the presence of quantum dot in the channel. The Coulomb diamonds in Fig. 4.3(a) are overlapped with each other, which implies the possibilities for multi-dot charge transport. For simplicities, I will treat it as a single quantum dot. I observed four hole states for the quantum dot in the *p*MOSFET, which were named as H_0, H_1, H_2, H_3, as shown in Fig. 4.3(a). However, only two electron states were observed in *n*MOSFET, which was named as E_0 and E_1, as shown in Fig. 4.3(b).

By studying the characteristics of the Coulomb diamonds, I can obtain information about the quantum dots in the device channels. The carrier concentration was around 10^{10}~10^{12} cm^{-2} in typical two-dimensional electron gas in Si MOSFET[121]. This range of carrier concentration corresponds to the electron-electron distance of 10~100 nm. This is much larger than the Bohr radius of electron in Si, 5.2 nm, and on the same

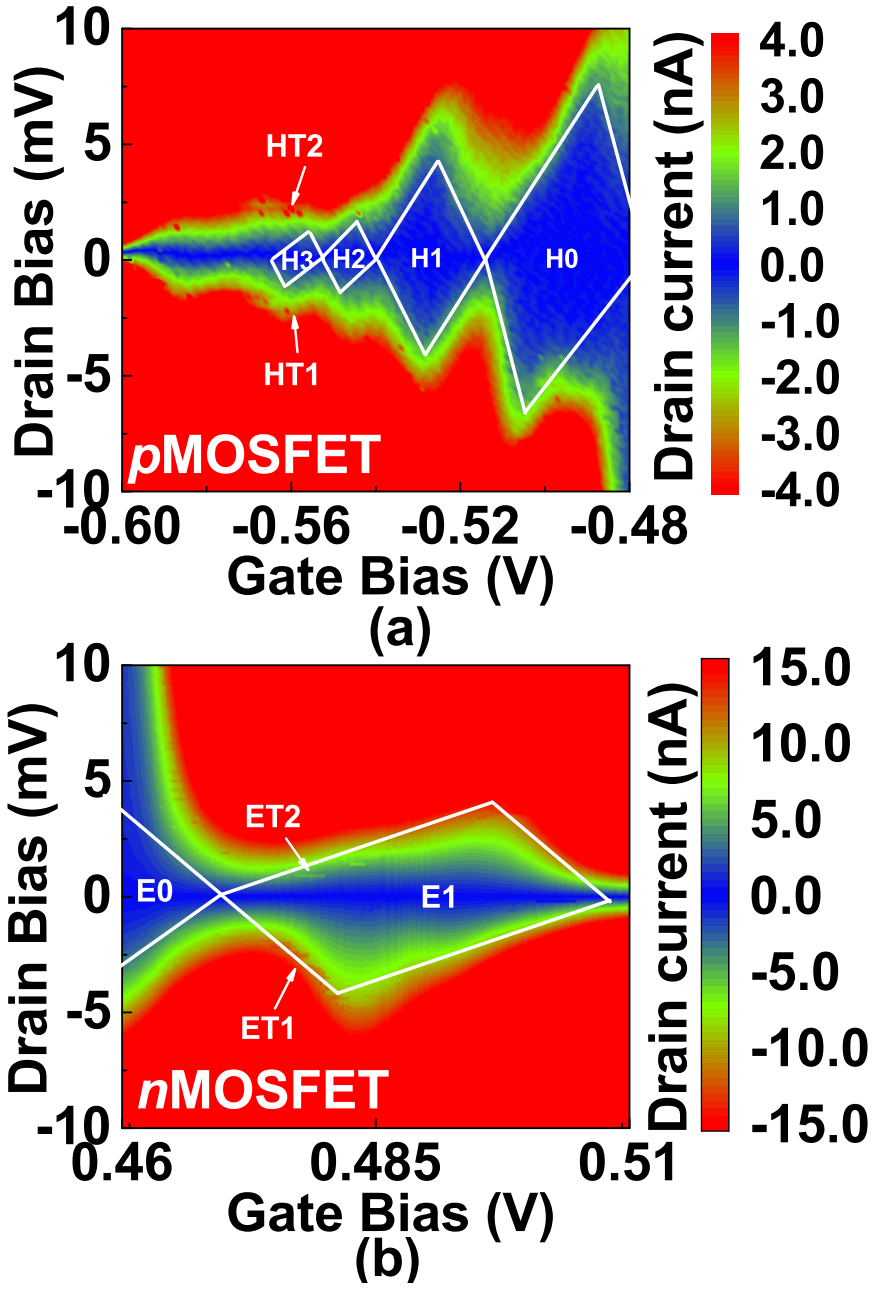

FIGURE 4.3: Contour plot of drain current versus gate voltage and drain voltage in (a) *p*MOSFET and (b) *n*MOSFET at 5 K. The border of the Coulomb diamonds were extracted by fitting with the standard mesoscopic model.[118]

magnitude as thermal de Broglie length of electron in Si at 5 K, 133 nm. As a result, the electrons trapped in quantum dot can be treated as non-interactive electrons.

At sub-threshold regime, in both devices, the current contributed by the single electron transistor characteristics dominate the total channel current. Therefore, the carrier concentration in the channel can be roughly estimated as[118]

$$N_{\text{channel}} \approx \frac{1}{WL} = 1.8 \times 10^{8}\text{cm}^{-2}. \tag{4.1}$$

Due to the low carrier concentration, the impact of Poly-Si depletion layer is negligible. However, the thickness of the inversion layer, which is coming from the quantum confinement near the SiON/channel interface, cannot be neglected due to the thin oxide of both devices. The thickness of inversion layer is 2nm[121, 122, 123]. Based on this value, I can roughly estimate the total capacitive effective thickness,

$$t_{\text{eff}} = t_{\text{ox}} + \frac{\varepsilon_{\text{ox}} t_{\text{inv}}}{\varepsilon_{\text{Si}}} = 3.1\text{nm}, \tag{4.2}$$

where ε_{ox} is the dielectric constant of SiO_2 and ε_{Si} is the dielectric constant of Si.

I can use the standard mesoscopic model[11] to extract the coupling capacitances of hole/electron states of quantum dots in pMOSFET and nMOSFET, respectively. The circuit model is shown in Fig 4.4(a). From Fig. 4.3, I observed that the coupling capacitances for each hole state were different. The coupling capacitance increases as |Vg| increased. Considering the formation of inversion layer in Si MOSFETs, this implies that the inversion layer capacitance is associated with the total coupling capacitance[124]. When the depletion layer reaches its maximum width, the channel will start to be inverted[125]. Therefore, the total gate capacitance (Cg) can be expressed as the series-connected inversion layer capacitance and oxide capacitance, as shown in equation (4.3).

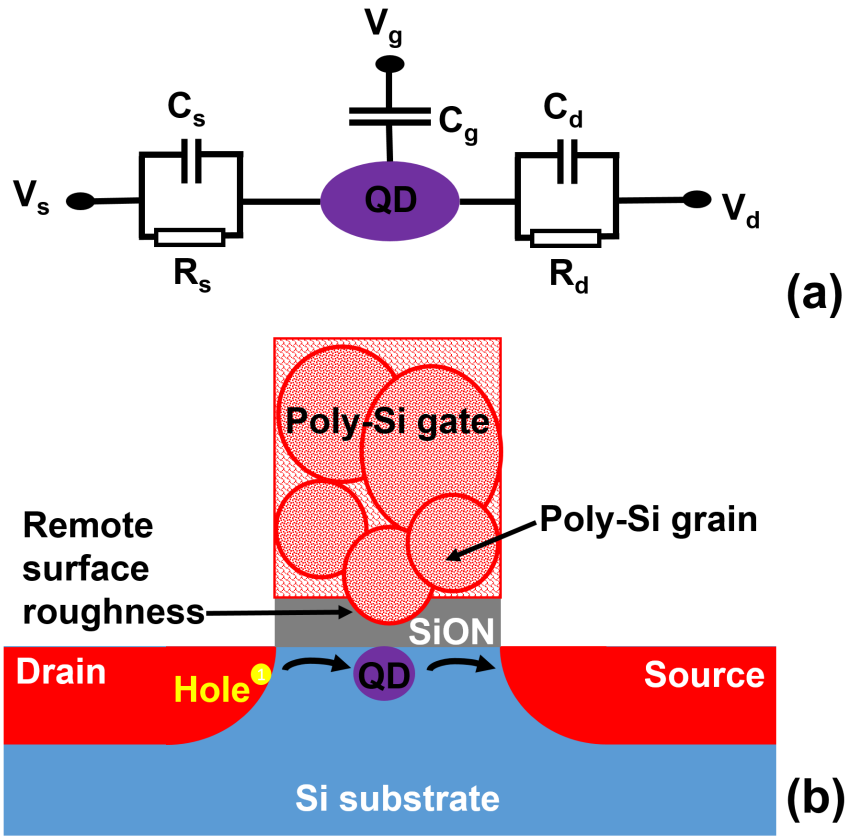

FIGURE 4.4: Circuit model and physical model of the quantum dot. (a) shows the standard equivalent circuit model and (b) shows a schematic diagram of the assumed remote poly-Si roughness for the quantum dot structure.[118]

$$\frac{1}{C_g} = \frac{1}{C_{ox}S} + \frac{1}{C_{inv}S}, \tag{4.3}$$

where S was the area of the quantum dot, C_{inv} is the inversion layer capacitance per unit area, and C_{ox} is the oxide capacitance per unit area. I can extract C_g from the periodicity of Coulomb oscillations related to each Coulomb diamond, ΔV_g,

$$C_g = \frac{e}{\Delta V_g}. \tag{4.4}$$

All the coupling capacitances extracted are summarised in the Tab 4.2 and Tab 4.3 for pMOSFET and nMOSFET respectively.

TABLE 4.2: Coupling Capacitances for device 1

Diamond	H3	H2	H1	H0
Gate Capacitance (aF)	13.4	12.6	6.2	4.2
Drain Capacitance (aF)	34.7	33.8	15.8	6.4
Source Capacitance (aF)	62.0	52.8	22.8	10.7
Inversion Layer Capacitance (aF)	N/A	211.1	11.5	6.1
Charging energy (meV)	1.5	1.6	3.7	7.5

TABLE 4.3: Coupling Capacitances for device 2

Diamond	E1
Gate Capacitance (aF)	4.2
Drain Capacitance (aF)	11.6
Source Capacitance (aF)	23.5
Charging energy (meV)	4.1

The size of the quamtum dot in pMOSFET can be estimated by extracting from the coupling capacitance of the state H_3. At the state H_3, the gate bias is very close to the threshold voltage shown in Fig. 4.1(a), and the carrier density is therefore the highest among all the hole states. Therefore, C_{inv} in H_3 is much larger than the C_{ox}, and I can neglect the contribution of C_{inv} to C_g. Assuming the shape of quantum dot is a circle, the diameter of quantum dot, d, can be extracted

$$d = \sqrt{\frac{4C_g(H_3)}{\pi\varepsilon_{ox}/t_{eff}}} = 38.5\text{nm}. \tag{4.5}$$

The charging energy of state H_0 is 7.5 meV, which is much smaller the value previously reported in single dopant transistors[126, 127, 128]. It is unlikely that the quantum dots have originated from the single dopants in the channel. The diameter of the quantum dot implies that the quantum dots are defined by the surface roughness of Poly-Si grains[129]. Poly-Si is a meterial with grain boundaries, and the remote surface roughness originated from grain boundaries results in local variations of equivalent oxide thickness[62, 130].

The variations of oxide thickness will form a dip in the surface potential. In this way, a quantum dot is formed and single electrons/holes are confined in this dip regime. The dimension of Poly-Si grain boundaries can be around 50 nm[131], which is comparable to the estimated size of the quantum dot.

The increase of drain and source coupling capacitance with the changing of V_g can be explained by the changes of tunnelling barrier height and forming of the inversion layer. The barrier height was reduced if I increased V_g , therefore the capacitance coupling was also enhanced. Also, the formation of inversion layer also contributes to the increase of C_g. The inversion layer starts to expand from Source to Drain if I increase $|V_g|$.

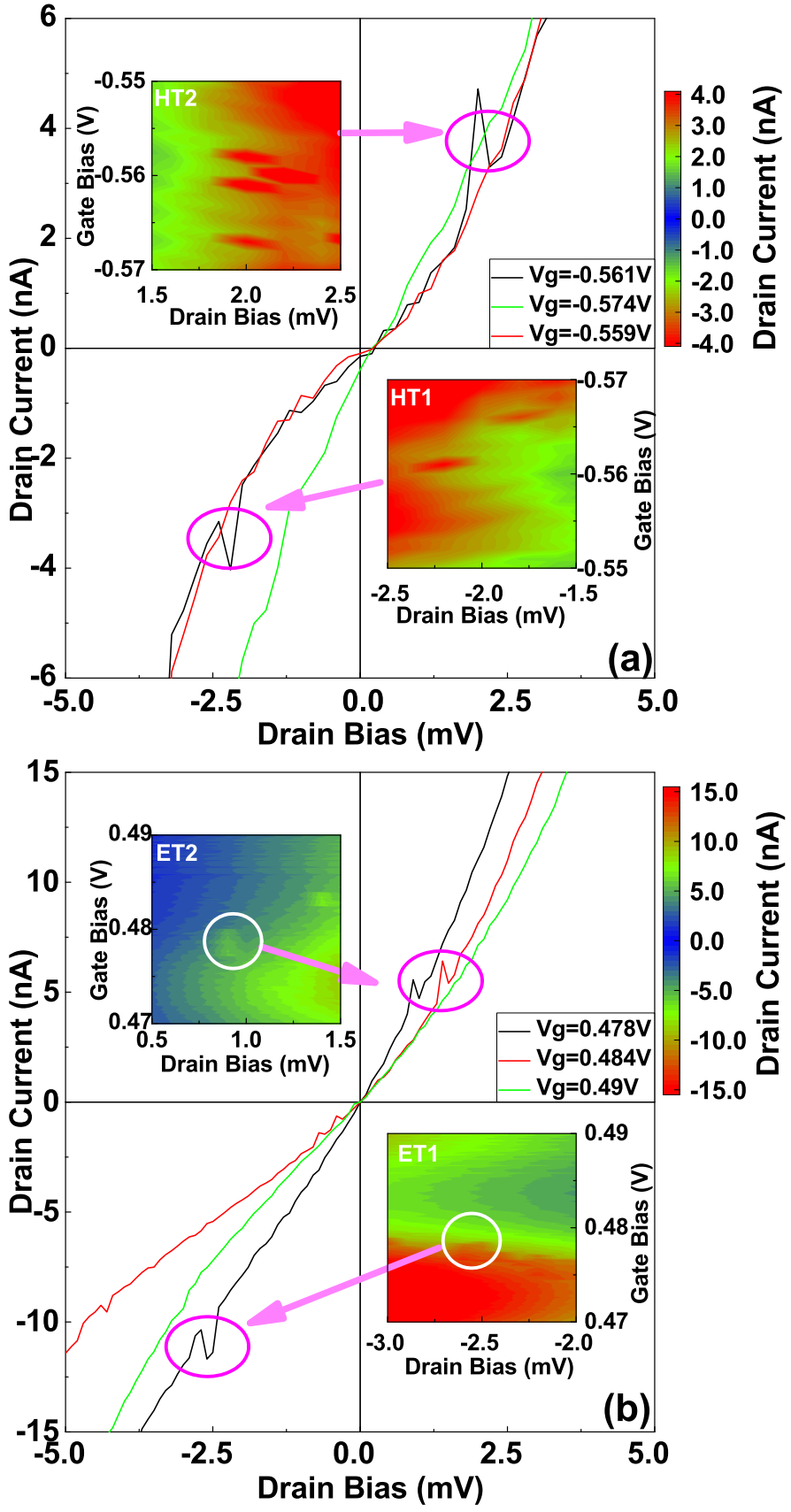

FIGURE 4.5: Sharp current peaks observed at the edges of Coulomb diamond. The current peaks are shown in both current map and I_d - V_d characteristics. (a) indicates the influence of a single charge trap in *p*MOSFET with different gate bias. (b) shows the influence of a single charge trap in *n*MOSFET with different gate bias.[118]

In Fig 4.3, I could observe some current peaks at the edge of the Coulomb Diamond Regime, which were marked as HT2 and HT1 in Fig. 4.3(a), and ET1 and ET2 in Fig. 4.3(b). A detailed investigation of the characteristics of current peaks is shown in Fig. 4.5. The current peaks was only observed in a narrow bias condition in both devices. clear current peaks was observed at Vd of -4 mV if I biased Vg at -0.561 V in the *p*MOSFET. However, it was not observed at -0.559 V and -0.574 V, which shows the gate bias window to observe the current peak is less than 15 mV, and the drain bias window of $\sim$ 0.5 mV. Similar current peaks were observed in the *n*MOSFET, with a gate bias window of 12 mV and drain bias window of $\sim$ 0.5 mV. The current peaks reveal the presence of charge traps. The sharp bias conditions to observe the current peaks implie that the resonant tunnelling may be responsible for the current peaks. This will obviously affect the performance and reliability of Si single electron devices.

In total, in this measurement, I observed single electron characteristics in advanced conventional CMOSFETs, which confirms that the conventional MOSFET structures can behave as single electron devices at low temperatures. I used standard mesoscopic capacitor model to investigate on the single electron characteristics, and confirmed that the coupling capacitances for different hole/electron states can be significantly affected by the changing of gate bias through the formation of inversion layer. I observed current peaks at the edge of Coulomb diamond, which shows the impact of charge traps on the performance and characteristics of Si single electron devices. A manuscript based on this measurement result has been published in *IOP Semiconductor Science and Technology*[118], and has been selected as the Highlights of 2017 of the journal.

In order to investigate on the origin of the current peaks to have a clear image of how the charge traps will impact the single electron devices, I measured the time domain characteristics at the peak bias conditions, at a different device. The measurement results are summarised in the following part.

4.1.2 RTN Characteristics and Investigation

In order to study investigate the current peaks in detail, I measured the device 3, which will be called *p*MOSFET in this section. The stability diagram of the devices is shown in Fig. 4.6[132].

I observed the single hole transistor characteristics and open Coulomb diamonds in the stability diagram as shown in Fig. 4.6(a). This implies several quantum dots in series or in parallel were responsible for the drain current, I_{d}. The single hole transistor characteristics are likely to have originated from the Poly-Si grains, which was discussed in the previous part.

In order to investigate on the current peaks in detail, due to the narrow bias conditions in the previous measurement, I run the measurement in a very precision sweep (500

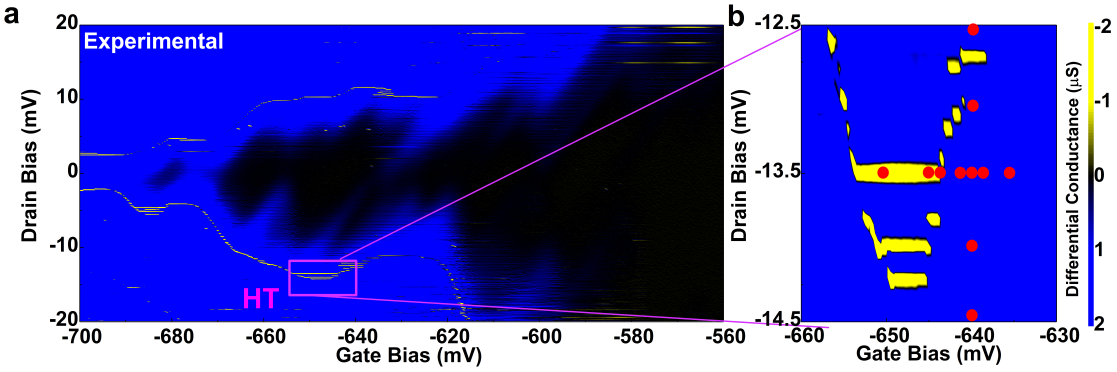

FIGURE 4.6: Bias condition to observe current peaks. (a) shows the stability diagram of the *p*MOSFET at 2 K. The regime where current peaks can be observed (negative differential conductance) was shown. (b) shows the extended view of HT region and the bias conditions where RTNs were measured.[132]

μV). The value of current at each bias was obtained after averaging over 10^5 sampling taken with the duration of 2 μs for each point. By measuring the I_d in such a slow pace, I would be able to find the time domain characterisitcs of I_d. The background noise was less than 4 pA, in a bandwidth of 5 Hz. Current peaks are observed at the edge of Coulomb diamond, as shown in Fig. 4.6(a). Particularly, at some bias conditions, the current peaks were much denser than the other regime. One of them was marked as HT. I measured the drain current at some bias conditions marked as red dot in (b) to find the bias dependence. The result is shown in Fig. 4.7:

Random telegraph noise(RTN) was observed in the time domain characteristics of I_d. One example of the time domain characteristics, which was measured at V_g of -640 mV and V_d of -13.5 mV, is shown in Fig. 4.7(a). Two types of RTN could be identified from the time domain characteristics, and they were named as RTN1 and RTN2, respectively. RTN1 shows larger amplitude and longer average switching time, while RTN2 behaves in the opposite way. This trend implies that the trap corresponding to RTN1 is a deep oxide trap, while RTN2 might come from the shallow trap/traps in the SiON/substrate interface.

The amplitude of RTN1 can be roughly by estimated by extracting from the number of carriers inside the channel[133, 134, 135], $N_0{=}k_\mathrm{B}TC_\mathrm{gate}/e^2{=}k_\mathrm{B}T\varepsilon_\mathrm{ox}\varepsilon_0\mathrm{WL}/t_\mathrm{eq}e^2{=}11.6$, where k_B is the Boltzmann constant, e is the value of elementary charge, ε_ox is the dielectric constant of SiO_2, ε_0 is the permittivity in vacuum, W is the width of the channel, L is the length of the channel and t_eq is the capacitive equivalent thickness of SiON layer. Then the relative amplitude of RTN1 can be estimated as $\Delta I/I{=}1/N_0{=}8.6\%$, which was roughly in agreement with the experimental data. At higher temperatures, RTN1 could not be observed, which was shown in Fig. 4.8. This is due to the increasing of the increasing in number of carriers at higher temperatures[136, 137], which implie that the random telegraph noise is assosiated with single-hole effects.

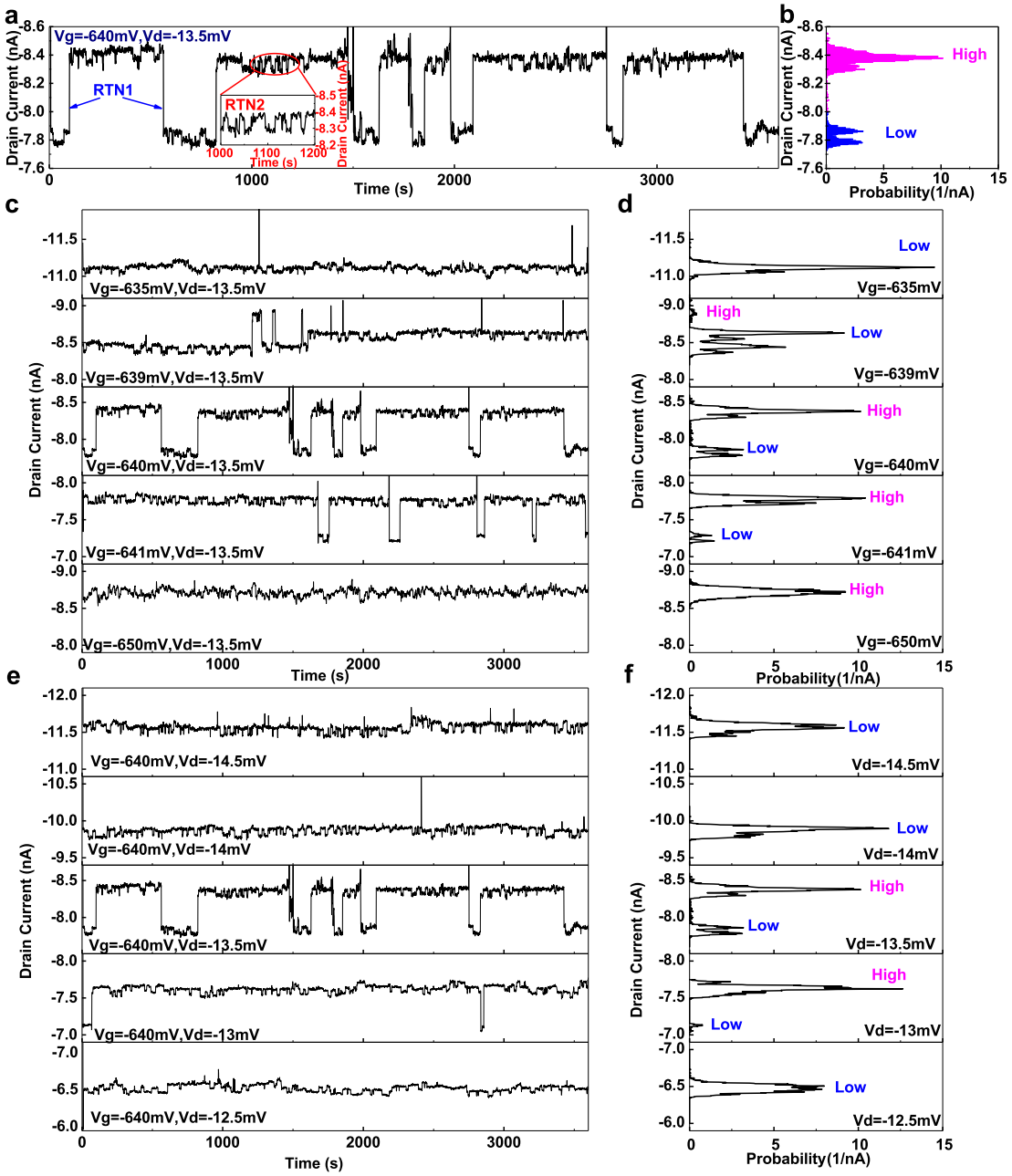

FIGURE 4.7: Time domain characteristics of I_d. (a) shows the time domain characteristics of I_d measured at V_g of -640 mV and V_d of -13.5 mV. RTN1 and RTN2 are marked. (b) shows the probability distribution of current versus its value. The state 'High' and 'Low' regarding RTN1 is marked. (c) shows the dependence of RTN on V_g if V_d is biased at -13.5 mV, and (d) shows the probability distribution of current accordingly. (e) shows the dependence of RTN on V_d if V_g is biased at -640 mV, and (f) shows the probability distribution of current accordingly.[132]

I investigated the statistics of I_d by analysing the frequency with which I observed I_d at certain ranges, with the minimum step of 4 pA. The result of the example at V_g of -640 mV and V_d of -13.5 mV, is shown in Fig. 4.7(b). This is the quantum mechanical probability finding the system under a certain current state, $P(I_d)$, which reveals the information about the wave function of the single hole in the charge traps, $\psi(I_d)$, as

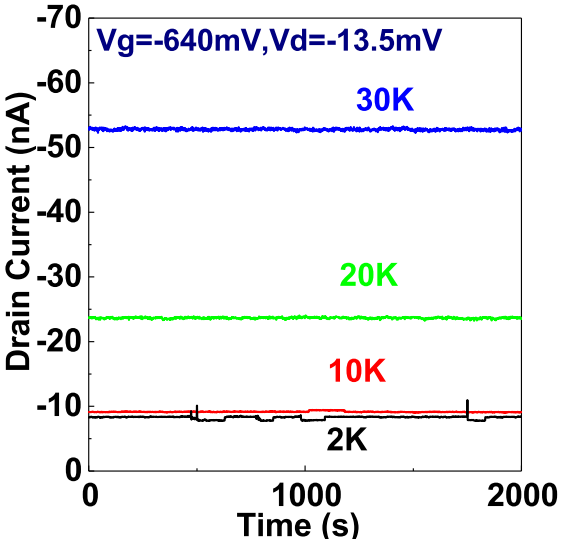

FIGURE 4.8: Temperature dependence of RTN1. The RTN1 was not observed at temperatures higher than 10 K.[132]

$$P(I_{\mathrm{d}}) = |\psi(I_{\mathrm{d}})|^2. \tag{4.6}$$

The bias dependences of I_{d} at different bias conditions is shown in Fig. 4.7(c) and 4.7(e), respectively. The corresponding statistics of I_{d} is shown in Fig. 4(d) and (f). From Fig. 4.7.(c), RTN1 was only observed when V_{g} is between -635 mV and -650 mV. I observed that I_{d} was more likely to be in the high current state if I increased $|V_{\mathrm{g}}|$. This showed the shifting of charge trap occupancy. The V_{d} dependence on time domain characteristics is shown in Fig. 4.7.(e). The high current state was only observed between V_{d} of -13 mV and -13.5 mV. This implies the presence of resonant tunnelling, which was in agreement with the previous measurement result on other two devices.

I also checked the time domain characteristics of I_{d} at other regime with similar density of current peaks. RTN was also observed, as shown in Fig. 4.9.

Next I will investigate on the probabilities to observe the high current state and the low current state, regarding RTN1, in Fig. 4.7, using Markov model[132]. The probabilities are extracted by fitting the experimental data with Gaussian distribution functions. The amplitude of RTN is determined by the difference of the peak values. If the probability distribution function corresponding to the high current state in Fig. 4.7 is $p_{\mathrm{h}}(I_{\mathrm{d}})$, and the probability distribution function corresponding to the low current state in Fig. 4.7 is $p_{\mathrm{l}}(I_{\mathrm{d}})$, P_{h} and P_{l} are derived from

$$P_{\mathrm{h}} = \frac{\int_{-\infty}^{\infty} p_{\mathrm{h}}(I_{\mathrm{d}})dI_{\mathrm{d}}}{\int_{-\infty}^{\infty} p_{\mathrm{h}}(I_{\mathrm{d}})dI_{\mathrm{d}} + \int_{-\infty}^{\infty} p_{\mathrm{l}}(I_{\mathrm{d}})dI_{\mathrm{d}}}, \tag{4.7}$$

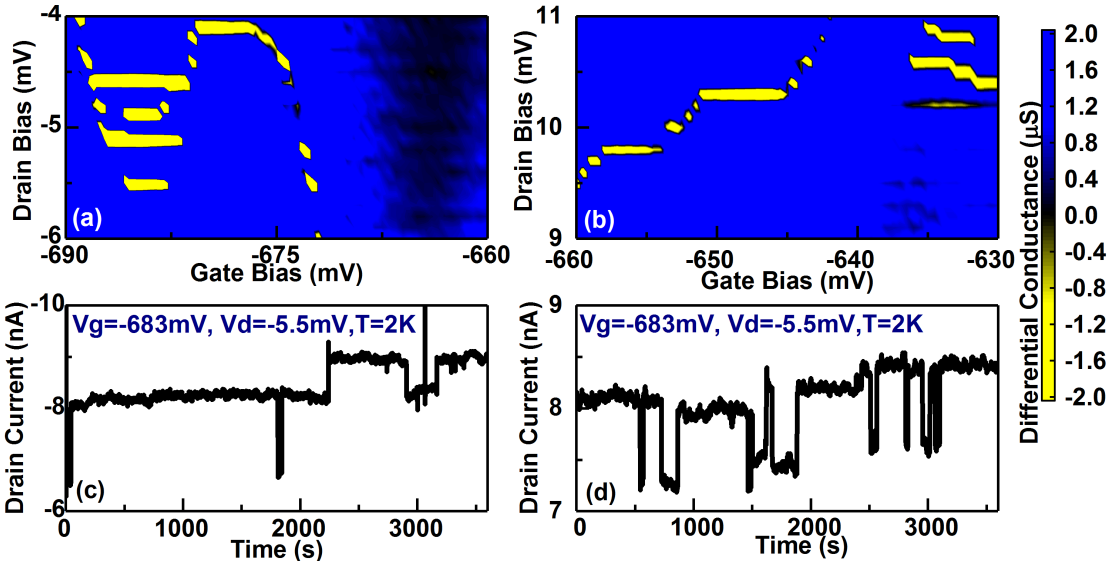

FIGURE 4.9: RTN characteristics at other bias conditions.[132]

and

$$P_{\mathrm{l}} = \frac{\int_{-\infty}^{\infty} p_{\mathrm{l}}(I_{\mathrm{d}})dI_{\mathrm{d}}}{\int_{-\infty}^{\infty} p_{\mathrm{h}}(I_{\mathrm{d}})dI_{\mathrm{d}} + \int_{-\infty}^{\infty} p_{\mathrm{l}}(I_{\mathrm{d}})dI_{\mathrm{d}}}, \tag{4.8}$$

which correspond to the shaded areas (magenta and blue, respectively) in Fig. 4.7(b). The P_{h} and P_{l} dependence on gate and drain biases are shown in Fig. 4.10(a) and Fig. 4.10(b), respectively.

I_{d} was more likely to be in the high current state if $|V_{\mathrm{g}}|$ was large, and the preferred I_{d} state changes sharply near V_{g} of -640 mV. This sharp transistion of preferred I_{d} states on V_{g} reveals the charge trap corresponding to RTN1 is located in the SiON layer of the *p*MOSFET. The high current state was only observed at V_{d} of -13 mV and -13.5 mV accroding to Fig. 4.10(b), implying the presence of resonant tunnelling. The bias dependence of amplitude were shown in Fig. 3(c) and Fig. 3(d), respectively. Almost no dependence of amplitude can be found on both V_{g} and V_{d}. Since the I_{d}- V_{g} characteristics is non-linear in the subthreshold regime, if the RTN1 is coming from the shift of threshold voltage, the amplitude of RTN1 will have dependence on V_{g} and V_{d}. However, it is in agreement with the experimental data, as shown in Fig. 4.10(c). Therefore, it is unlikely that RTN1 has originated from the shift of threshold voltage, which is the reason for RTN in MOSFETs at room temperatures. I could use a similar method to investigate the characteristics of RTN2, as shown in Fig. 4.11. The dependence of RTN2 on biases was complex, which implies RTN2 came from a shallow trap near SiON/substrate interface.

Due to the intrisic quantum behaviour, the wavefunction of single hole resulted in an extra noise in I_{d}. In order to understand the wavefunction of the single hole as shown in Fig. 4.8(d) and Fig. 4.8(f), I need to study the bias dependence of this extra noise.

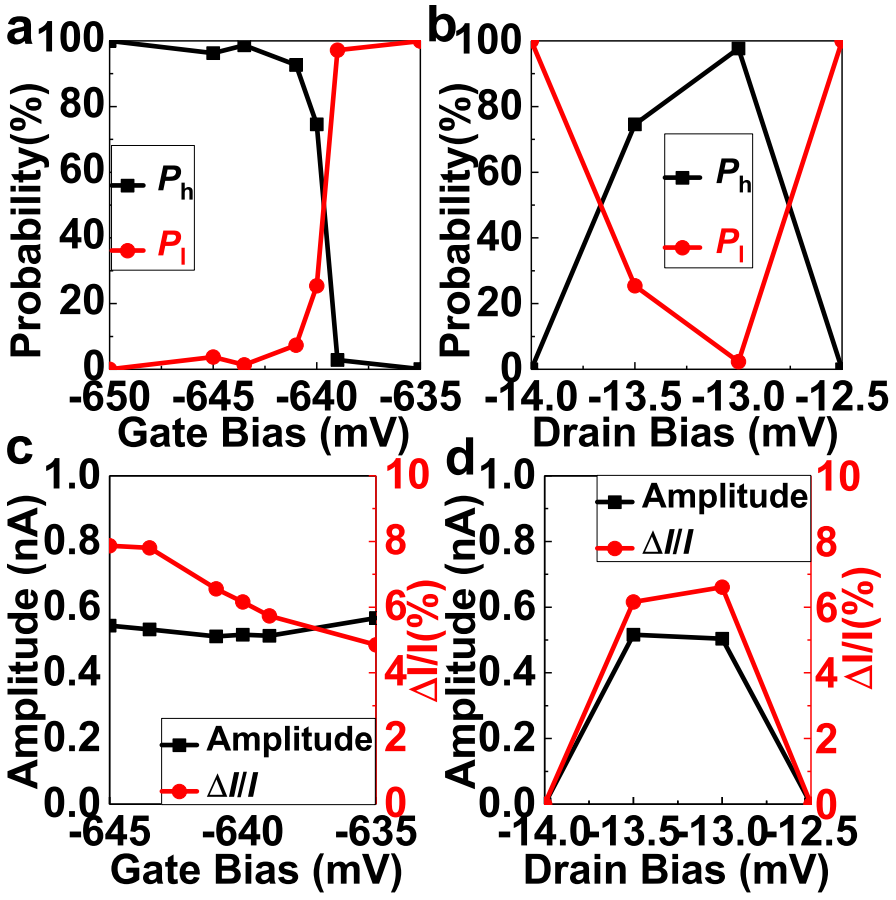

FIGURE 4.10: The bias dependence of RTN1. (a) and (b) shows the dependence of P_h and P_l on V_g and V_d, respectively. (c) and (d) shows the dependence of RTN1 amplitude on V_g and V_d, respectively.[132]

The extra noise, which is revealed from the differential current, ΔI_d, is defined as

$$\Delta I_d = I_d(t+1) - I_d(t), \tag{4.9}$$

where t is time with the unit of second. The bias dependences of its probability distribution are shown in Fig. 4.12(a) and (b), respectively. The standard deviation of ΔI_d was extracted by fitting the distribution of ΔI_d with the Gaussian distribution function.

The probability distribution function of ΔI_d had very weak dependence on V_g, as shown in Fig. 4.12(a), while it showed more significant dependence on V_d, as shown in Fig. 4.12(b). Since the change of I_d value is similar between Fig. 4.12(a) and Fig. 4.12(b), the more significant dependence of the probability distribution function on V_d implies that the coupling between the quantum dot and energy level created by charge trap was mainly modulated by V_d. I observe that the standard deviation of probability distribution showed a peak value at V_d of -13.5 mV. This reveals that the wavefunction of the single hole in the channel became the 'broadest' at this bias condition. This shows the strongest correlation between two energy levels in the channel, in agreement with the assumption of resonant tunnelling. The resonant level is likely to have originated

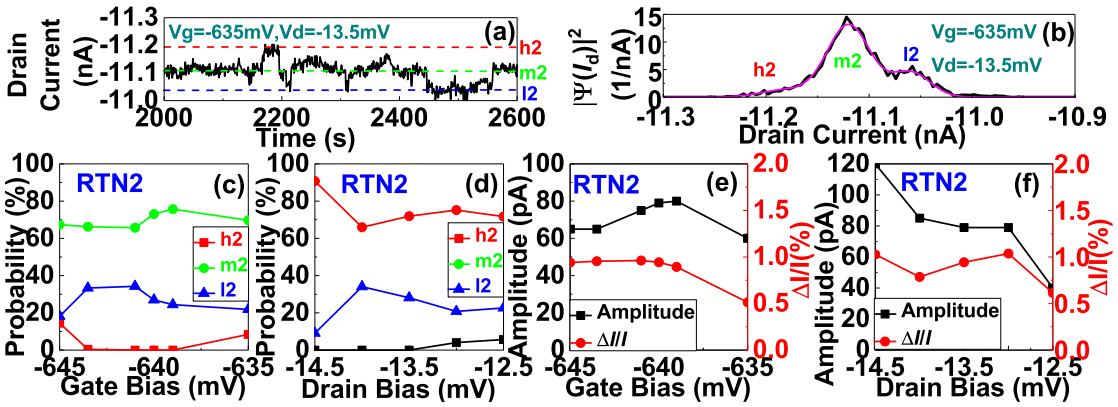

FIGURE 4.11: Investigation on RTN2. (a) shows the time domain characteristics of I_d at certain time range if V_g was biased at -635 mV and V_d was biased at -13.5 mV and (b) shows the corresponding wavefunction. The three current states, h2, m2 and l2, corresponding to RTN2, are marked in (b). (c) and (d) shows the dependence of probability on V_g and V_d, respectively. (e) and (f) shows the dependence of RTN2 amplitude on V_g and V_d, respectively.[132]

from the charge traps. The Johnson noise[27, 138] of this system was calculated to be $\sim$20 fA/$\sqrt{Hz}$, which was negligible compared with the noise coming from wavefunction.

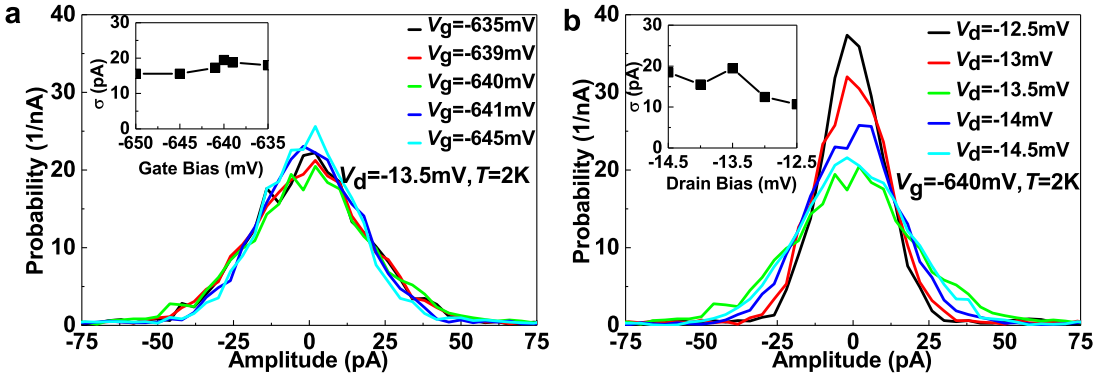

FIGURE 4.12: The dependence of experimental parameters on wavefunction broadening. (a) and (b) shows the dependence of wave function broadening on V_g and V_d, respectively. The V_g and V_d dependence on standard deviation of the corresponding Gaussian wave function, σ, is shown in subfigures inside (a) and (b), respectively.[132]

lag plots[139] of I_d are drawn to investigate its correlation behaviour. This will help to understand the fractal nature[140] of the two charge traps. the time lag, Δt, were selected to be 1s, 10s and 100s, as shown in Fig. 4.13(a), (b) and (c) respectively.

The diagonal fractal shape was observed when Δt is 1s, which reveals the strong positive autocorrelation behaviour of I_d in this time scale, as shown in Fig. 4.13(a). When Δt was increased to 10s, the shape of lag plot remained diagonal in the major regime. However, within each small area, the fractal shape becomes rectangular, which means the lost of correlation behaviour regarding RTN2, as shown in Fig. 4.13(b). The fractal shape of lag plot became rectangular in Fig. 4.13(c), which reveals the extinction of correlation behaviour for both RTN1 and RTN2 when Δt was further increased to 100 s.

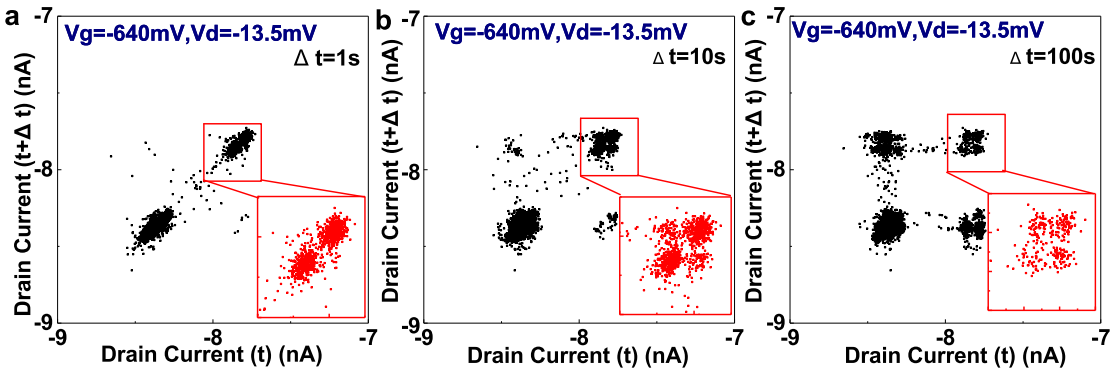

FIGURE 4.13: Fractal nature of the charge traps. The lag plot of I_d with different time lag shows fracture nature of charge traps. (a), (b) and (c) shows the correlation behaviour of I_d if time lag was 1s, 10s and 100s, respectively.[132]

By investigating the lag plot, I could have a rough understanding of the fractal nature of the charge traps.

The Fourier transformation and correlation function of I_d were shown in Fig. 4.14(a) and (b), respectively. The symmetry of correlation function reveals that the process is a energy-conservative process. The 1/f dependence of power density was shown in Fig. 4.14(b). As shown in Fig. 4.14(b), the power density is almost flat if the frequency is below 0.05 Hz. After that, the power density show 1/f dependence. This reveals the crossover between RTN and 1/f noise in the Si quantum dot device, which was previously reported to be observed in magnetic nanodot system[141].

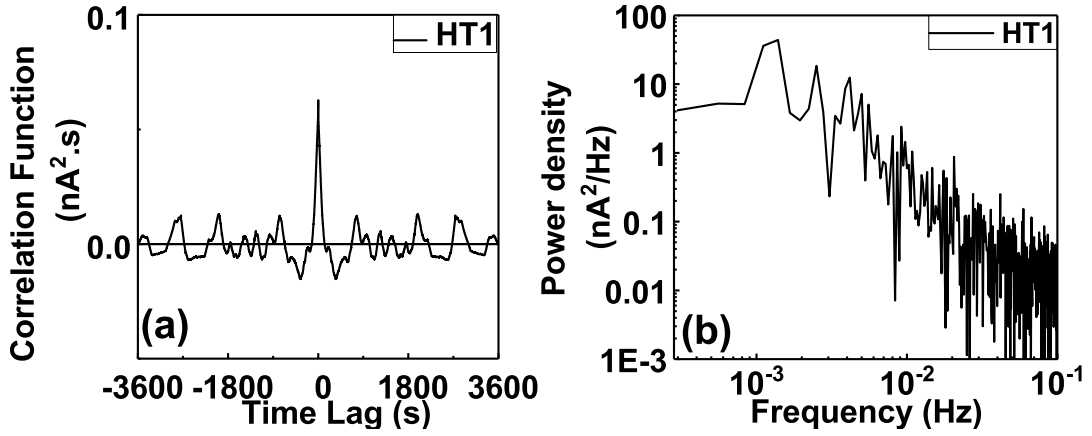

FIGURE 4.14: The correlation function of the I_d. The time domain characteristics were shown in (a) while (b) gives information about the power density obtained from Fourier transformation.[132]

Based on the information extracted, I could establish a physical model to describe the RTN1, as shown in Fig. 4.15. A schematic 3-D diagram of the device and its physical model is shown in Fig. 4.15(a). As stated in the previous part, it is possible that the I_d is contributed by multiple series or parallel dots. In the following part I will assume that there are two dots in series resposible for the I_d. The I_d has originated from sequential

tunnelling through two quantum dots in series, QD1 and QD2, which are coming from the remote surface roughness caused by Poly-Si grains.

For the series quantum dots system, the stability diagram was simulated using the master equations. I used mesoscopic capacitor model, with different effective coupling capacitances in different hole states, as an approximation to describe the system.

The way to calculate the current of single electron transistors[142, 143] based on mesoscopic model has already been introduced in the background research part. In this device, the effective coupling capacitances are different for different states. Therefore, if I assume the gate capacitance, drain capacitance, and source capacitance when n holes occupy a quantum dot in the channel to be $C_{\mathrm{g}}(\mathrm{n})$, $C_{\mathrm{d}}(\mathrm{n})$ and $C_{\mathrm{s}}(\mathrm{n})$, the change in free energy when a hole tunnels out through the electrode drain, $\Delta F_{\mathrm{d}}^{-}(n)$, or tunnels out through the electrode source, $\Delta F_{\mathrm{s}}^{+}(n)$, can be expressed as

$$\Delta F_{\mathrm{d}}^{-}(n) = F_{\mathrm{d}}(n-1) - F_{\mathrm{d}}(n) = -\frac{(n-1/2)e^2 - e[(C_{\mathrm{s}}(n) + C_{\mathrm{g}}(n))V_{\mathrm{d}} - C_{\mathrm{g}}(n)V_{\mathrm{g}}]}{C_{\Sigma}(n)}, \tag{4.10}$$

and

$$\Delta F_{\mathrm{s}}^{+}(n) = F_{\mathrm{s}}(n-1) - F_{\mathrm{s}}(n) = \frac{(n-1/2)e^2 + e[C_{\mathrm{d}}(n)V_{\mathrm{d}} + C_{\mathrm{g}}(n)V_{\mathrm{g}}]}{C_{\Sigma}(n)}. \tag{4.11}$$

I could easily obtain the expression of $\Delta F_{\mathrm{d}}^{+}(n) = F_{\mathrm{d}}(n+1) - F_{\mathrm{d}}(n)$, and $\Delta F_{\mathrm{s}}^{-}(n) = F_{\mathrm{s}}(n+1) - F_{\mathrm{s}}(n)$ from equation (6) and (7). Therefore, using Fermi's golden rule, the tunnelling rate through the drain and source can be expressed as

$$\Gamma_{\mathrm{d}}^{\pm}(n) = \frac{1}{R_d e^2}[-\frac{\Delta F_{\mathrm{d}}^{\pm}(n)}{1 - \exp(\frac{\Delta F_{\mathrm{d}}^{\pm}(n)}{k_{\mathrm{B}}T})}], \tag{4.12}$$

and

$$\Gamma_{\mathrm{s}}^{\pm}(n) = \frac{1}{R_s e^2}[-\frac{\Delta F_{\mathrm{s}}^{\pm}(n)}{1 - \exp(\frac{\Delta F_{\mathrm{s}}^{\pm}(n)}{k_{\mathrm{B}}T})}]. \tag{4.13}$$

The master equation can be expressed as

$$\frac{\partial p(n,t)}{\partial t} = p(n+1)[\Gamma_{\mathrm{s}}^{+}(n+1) + \Gamma_{\mathrm{d}}^{-}(n+1)] - p(n)[\Gamma_{\mathrm{s}}^{-}(n) + \Gamma_{\mathrm{d}}^{+}(n)]. \tag{4.14}$$

The drain current is therefore expressed as

$$I = e\Sigma_{n=-\infty}^{n=\infty} p(n)[\Gamma_{\mathrm{s}}^{+}(n) - \Gamma_{\mathrm{s}}^{-}(n)]. \tag{4.15}$$

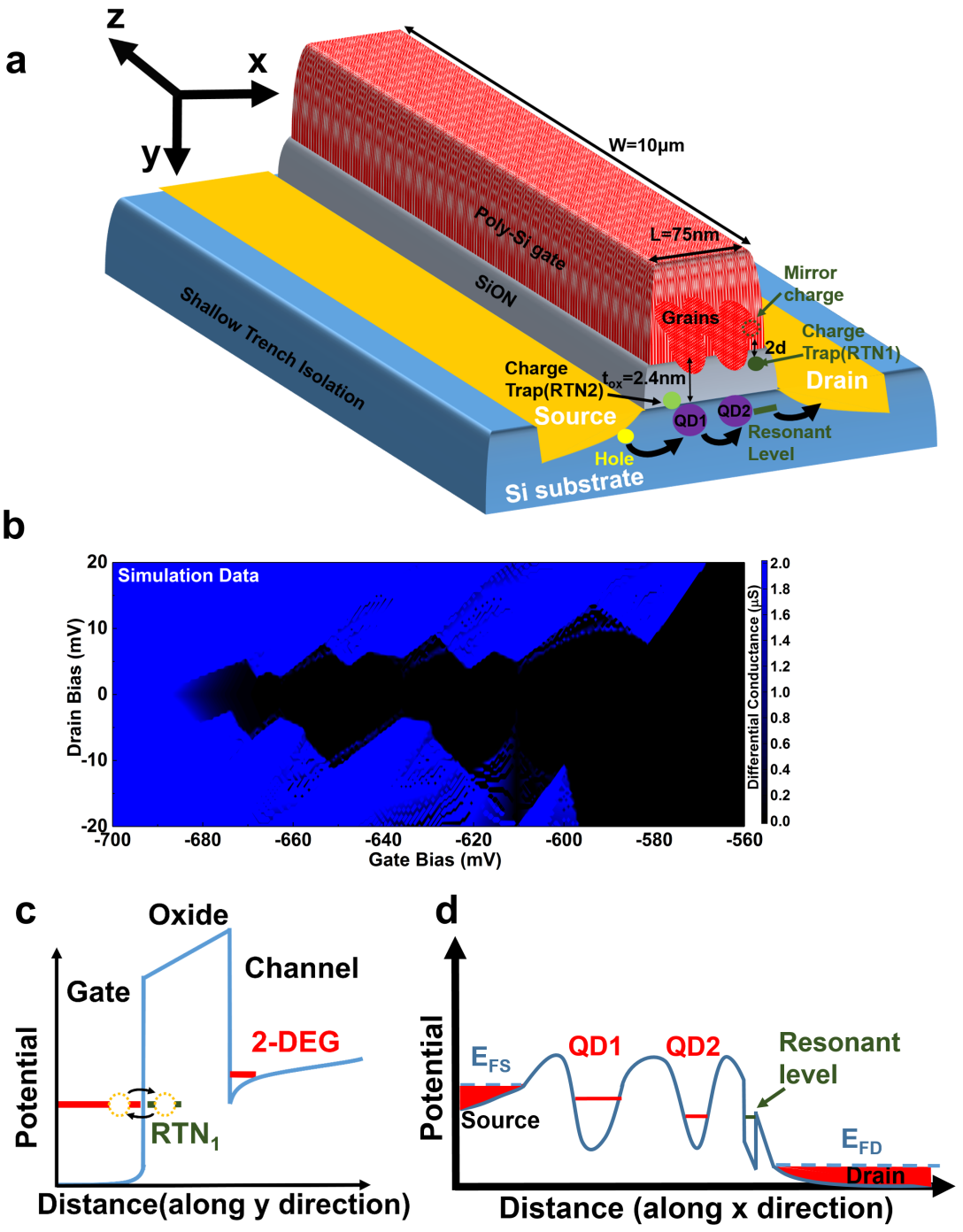

FIGURE 4.15: The physical model for the RTN. (a) shows the schematic physical model of the device. Series quantum dots are assumed to be responsible for the drain current, and the resonant level was formed by the trap 1, presumably a Boron ion. (b) shows the simulated stability diagram based on the series quantum dots model. (c) shows the schematic potential diagram across the oxide layer associated with the charge trapping and de-trapping process. (d) shows the schematic diagram of the potential across the channel. The deep and sharp potential well is formed by the electron dipole in the SiON layer.

The simulation result is shown in Fig. 4.15(b), which is roughly in agreement with the experimental data obtained in Fig. 4.7(a). The impact of inversion layer when V_g is near the threshold voltage is considered. The extracted coupling capacitances for the two quantum dots are summarised below in Tab. 4.4 and Tab. 4.5.

TABLE 4.4: Extracted coupling capacitances of single-hole states in QD1.

State	C_g(aF)	C_d(aF)	C_s(aF)
H0(QD1)	0.90	0.85	0.06
H1(QD1)	1.92	1.40	3.64
H2(QD1)	2.63	1.93	4.99
H3(QD1)	3.28	2.39	6.22
H4(QD1)	3.86	6.00	14.0

TABLE 4.5: Extracted coupling capacitances of single-hole states in QD2.

State	C_g(aF)	C_d(aF)	C_s(aF)
H0(QD2)	0.73	0.71	1.94
H1(QD2)	1.77	2.43	4.73
H2(QD2)	2.46	2.43	5.81

Using similar way as our previous investigations on the measurement result, physical diameter of the quantum dot is estimated about 20.7 nm for QD1 and 16.5 nm for QD2.

The trap corresponding to RTN1 can be located in SiON layer or in the device channel. It can either be an ionised charge trap in the SiON layer, or a middle-gap charge trap in the device channel. In the following part, I will first build the physical model based on the SiON layer assumption. By investigating on the V_g dependence, the charge trapping/de-trapping process has likely originated from the tunnelling of holes between the poly-Si gate and the charge trap inside the SiON, as shown in Fig. 4.15(c). If $|V_g|$ is decreased, the trap was easier to be occupied due to lower effective tunnelling barrier height. This corresponds to the trend observed in Fig. 4.10(a).

The different current states have originated the opening/closing of the charge-trap-induced resonant level[144, 145, 146] in the channel. The strong V_d dependence implies the resonant level is located in the tunnelling barrier between QD2 and the drain reservoir. As a result, the resonant level is strongly coupled with QD2. Due to the relatively much larger distance between the resonant level and QD1, the coupling between the resonant level and QD1 can be neglected.

A schematic diagram of the potential profile across the channel is shown in Fig. 4.15(d). If no single hole occupies the charge trap, it was ionic, and therefore generates mirror charge in the Poly-Si gate. As a result, the trap and the corresponding mirror charge generates an electric dipole, and therefore forms a potential well in the channel. Under certain bias conditions, the intrinsic energy level inside this potential well is aligned with the energy level in the QD2. Under that circumstance, resonant tunnelling makes tunnelling barrier between QD2 and drain reservoir more transparent. The resistance of

the tunnelling junction is therefore reduced, and the high current state can be observed.. If the charge trap is occupied by a single hole, the charge trap will become neutral. Therefore no resonant level will be formed in the channel, and the tunnelling barrier becomes less transparent. Only the low current state can be observed. This resonant-tunnelling-based model can explain the reason for the narrow V_g and V_d bias condition to observe RTN. Besides, the transmission coefficient and wavefunction of single hole in the channel were mainly modulated by the V_d, which explains the fact the strong dependence of wavefunction on V_d, as shown in Fig. 4.12.

The depth of the resonant level implies the vertical position of charge trap in SiON layer. A rough estimation can be made by assuming the depth of the potential well, ΔV, to be 13.5 mV. The distance between trap and Poly-Si/SiON interface, d, can be derived from[132]

$$e\Delta V = \frac{2e^2 d}{4\pi\varepsilon_{ox}\varepsilon_0 {t_{eff}}^2}. \tag{4.16}$$

I can roughly estimate d to be ∼0.2 nm from equation (4.16). This is the same magnitude with the SiON lattice constant. This estimation is in agreement with the assumption that the charge trap is located on the top side of SiON. As a result, I think a charge trap located near the Poly-Si/SiON interface, which was presumbaly a boron ion coming from the ion implantation process, is responsible for the resonant level in the channel.

The resonant tunnelling can also have originated from resonant tunnelling through a mid-gap trap level in the device channel. Since the SiON layer is very thin, it is possible that the holes in the Poly-Si gate can directly tunnel to the channel. If the ionised trap is not occupied, the resonant level stays in the channel, and therefore I observe the High-Current State. If the ionised trap is occupied by a hole and then becomes neutralised, no resonant level exists in the channel, and therefore I observe the Low-Current State. This is also a possible physical model to explain the RTN1.

In conclusion, I successfully demonstrate that I could identify the nature of the trap by measuring the RTN and investigating its bias dependence at low temperatures. I found that the charge trap can affect the reliability of single electron devices by resonant tunnelling between the energy level formed by charge trap and the quantum dot. I observed the cross-over between RTN and 1/f noise. Also, in this way, I can systematically invesigate the characteristics of charge traps, which will pave the way for scientists to understand the impact of charge traps and nature of RTN. A manuscript based on this measurement result has been published in *Nature Scientific Reports*[132].

Based on the two experiments, I now have a clear understanding about the output characteristics for a Si quantum dot device naturally formed in a Si device, originated from Poly-Si grains. I have found that the charge trap is able to impact the reliability of Si quantum dot devices by creating a resonant level in the channel, resulting in extra

tunnelling current from resonant tunnelling. This will help me understand about a gate-defined quantum dot device and its reliability impact factor. In order to check the actual device operation of a gate-defined Si quantum dot device, i.e., in my case single electron pump, and study the impact of charge traps, I carried the experiments in section 4.2 to investigate the single electron pump characteristics.

4.2 Measurement of single electron pump devices

From the measurement of the single electron pump devices, I have a further understanding of the output characteristics for the Si quantum dots, and investigate on the reliability and performance impact factor for them. After gaining enough knowledge, I measured a Si single electron pump device fabricated in Southampton Nanofabrication Centre.

A schematic diagram of the device measured is shown in Fig. 4.16.

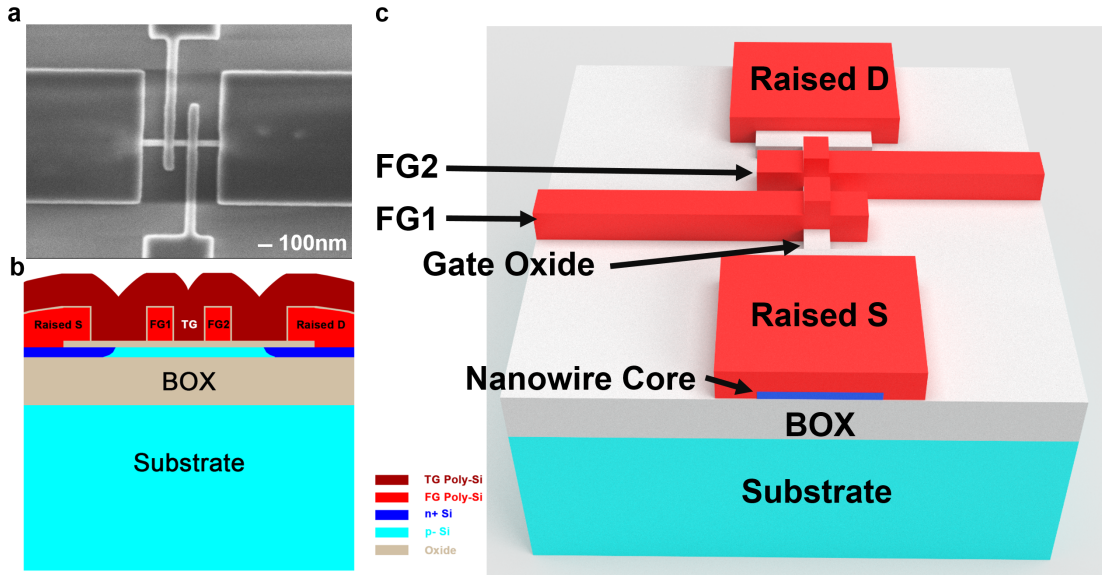

FIGURE 4.16: Images and Schematic Diagrams of the device I measured. (a) shows the SEM image of the plane view before the top gate was patterning. (b) shows the schematic cross-secton image of the device. (c) shows the schematic diagram of the device 3-D structure before the top gate was patterning.

The device I measured is the subchip XX04YY01 in the chip X12Y01, which is secondary design (a), with 75 nm designed width of Si nanowire, 75nm gate length and 100 nm gate spacing. After thermal oxidation, the width of the Si nanowire is estimated to be 50 nm.

In order to have a better understanding of the single electron pump device physics, I would like to investigate on the QD energy level spectrum. A method to investigate on the QD spectrum is by double-quantum-dot measurement. If two quantum dots were

put in series, the quantum dot close to the high level lead is served as a pass-filter to detect the spectrum of the other quantum dot through resonant tunnelling[147]. By converting gate voltage to energy using the level-arm factor[148], I would obtain the energy spectrum of the quantum dot. In that case, I would be able to detect with the precision even better than the thermal kinetic energy.

I swept over FG1 and FG2 to investigate on the spectrum of the quantum dots, formed by FG1 and FG2. The TG was biased to give the device a slight barrier. The spectrum measurement results are shown in Fig. 4.17(a).

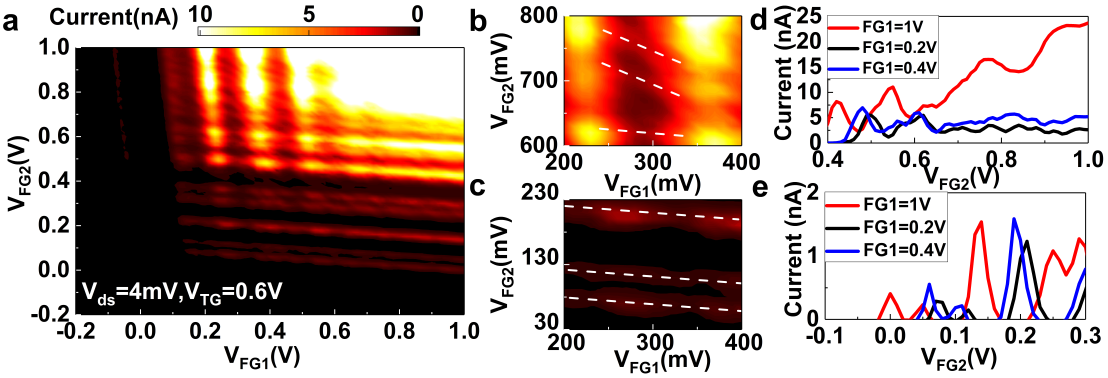

FIGURE 4.17: Investigation on the spectrum of Si quantum dots. (a) shows the energy spectrum measurement result of the quantum dots. (b) shows the transition between localised quantum dots and strongly coupled quantum dots. (c) shows the spectrum of the quantum dot measurement. (d) shows the vanish of resonant tunnelling at large FG1 bias. (e) shows the current peaks from resonant tunnelling.

From Fig. 4.17(b), I observed the shifting of the system states: localised quantum dots and strongly-coupled quantum dots. From Fig. 4.17(d), this was a very sensitive effect and vanished at very high V_{FG1}, which implied small transfer energy between two dots.

From Fig. 4.17(c), I observed three current peaks, which were shown in detail in Fig. 4.17(e). The peaks implie the peaks were associated with resonant tunnelling between quantum states in two quantum dots, not only charging effects.

The stability diagram regarding V_{FG2} and V_{ds}. Fig. 4.18(a) shows the experimental data. I can extract the charging energies to be 3.2 meV and the single particle spacing for the first electron to be 4 meV. This gives an addition energy of 7.2 meV. The simulation results based on these extracted parameters are shown in Fig. 4.18(b), and matches well with the experimental data. The size of the quantum dot was estimated as 49nm, which is in agreement with our design parameters.

After investigating on the characteristics of the quantum dot, I switched to AC measurement. First, I would like to check the transmission of RF signal. In order to check the transmission, I biased the FG2 with an RF signal, and changed the RF power to check the shift of threshold voltage. When I applied the RF signal, the device was switched 'ON' when the DC bias was at V_{th}-V_{amp}. By carefully checking the shift of threshold

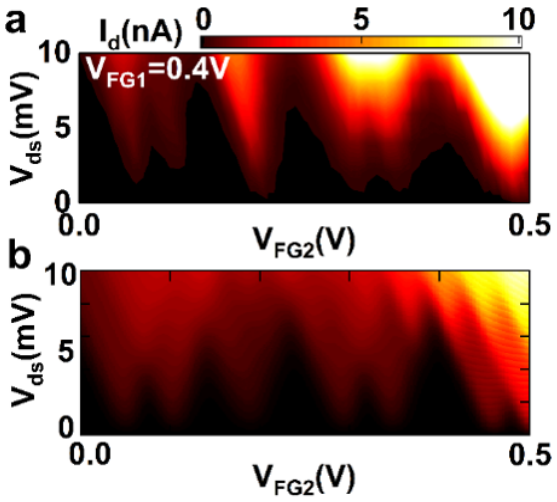

FIGURE 4.18: Stability diagram regarding V_{FG2} and V_{ds}. (a) shows the experimental results and (b) shows the simulation result based on the extracted parameters. Simulation results show good agreement with the experimental data.

voltage, I could estimate the transmission of the RF signal[149]. The measurement result is shown in Fig. 4.18.

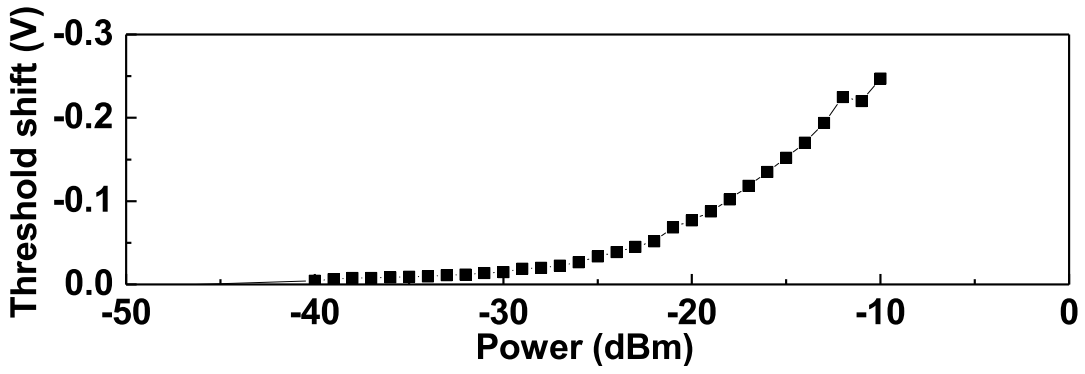

FIGURE 4.19: Shift of threshold voltage versus the RF power.

From Fig. 4.18, I observed that the RF signals have been successfully transmitted to the gate terminal. Under that circumstance, the RF signal was able to modulate the surface potential.

In order to find the bias conditions to observe single electron pumps, I checked the dependence of output characteristics on the exit barrier height. The current and differential conductance contour plot are shown in Fig. 4.19 and Fig. 4.20, respectively.

The V_{FG1} was biased at -0.2 V, -0.25 V, -0.3 V, -0.35 V for Fig. 4.19(a), (b) and 4.20(a), (b), respectively. The RF power was 0dBm and the frequency was 125 MHz. By comparing the graphs, I saw the bias conditions where I could see RF-modulated current became narrower if I increased the barrier height. This is because the electrons ejected from the quantum dot had certain energy distributions. If the exit barrier became high, then the tunnelling probability for the single electron in the ejection step

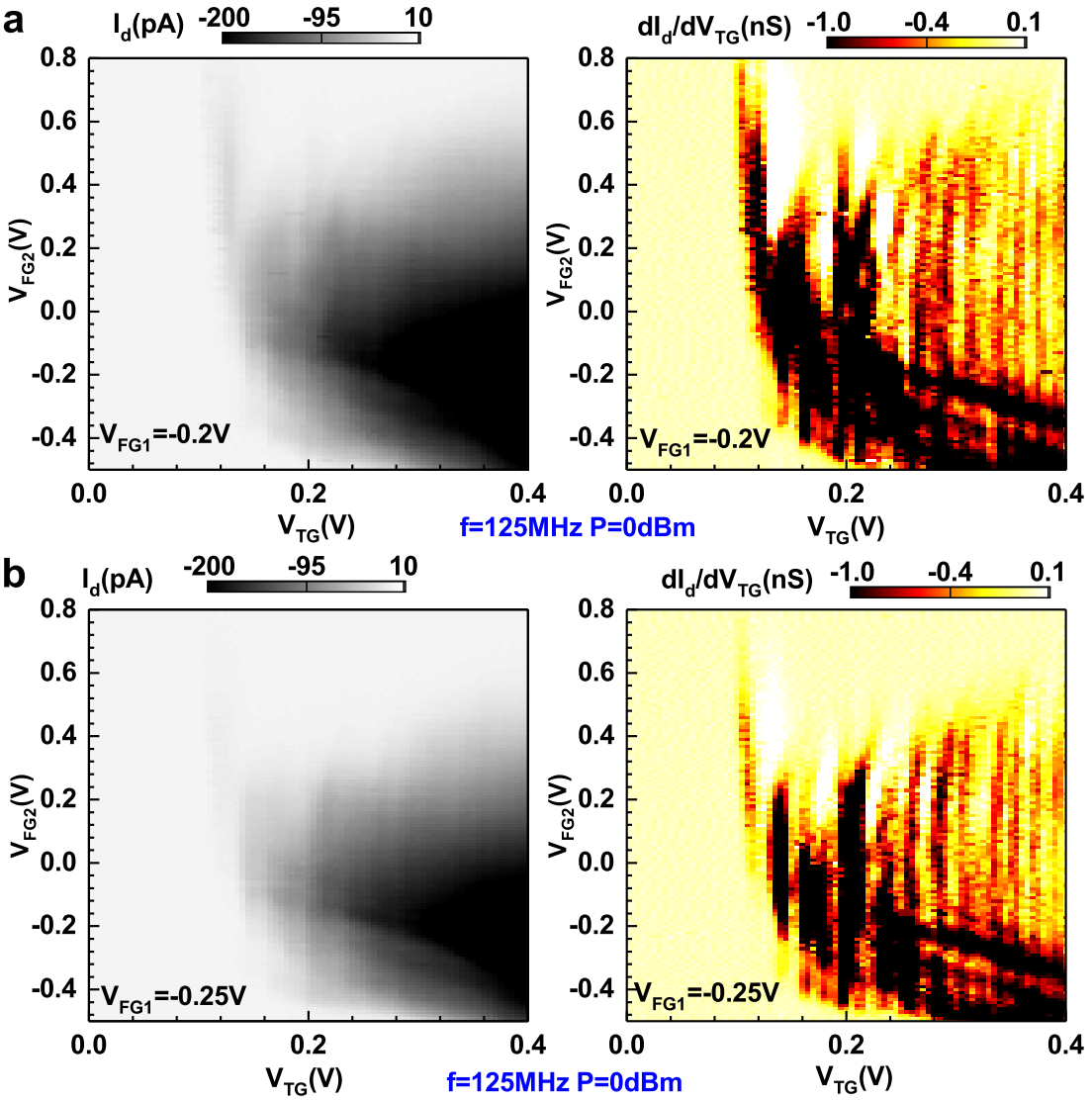

FIGURE 4.20: Current and differential conductance stability diagram of the single electron pump with RF signal on FG2. In (a) FG1 was biased at -0.2V, (b) FG1 was biased at -0.25V.

was reduced from 1, and quantised current was not observed. If the exit barrier was too low, then the electron would eject from the drain before the back-tunnelling process has completed. As a result, I must carefully choose the exit gate bias, as it significantly influence the device performance.

I also checked the dependence on the RF power, and the measurement result is shown in Fig. 4.21.

The RF power was 0 dBm and -1 dBm for Fig. 4.21(a) and (b), respectively. If the RF power was reduced, the bias conditions to observe RF-modulated current became narrower as well. This was in agreement with the fact that the reducing energy levels of trapped electron in the quantum dot. I also needed to carefully choose the RF power,

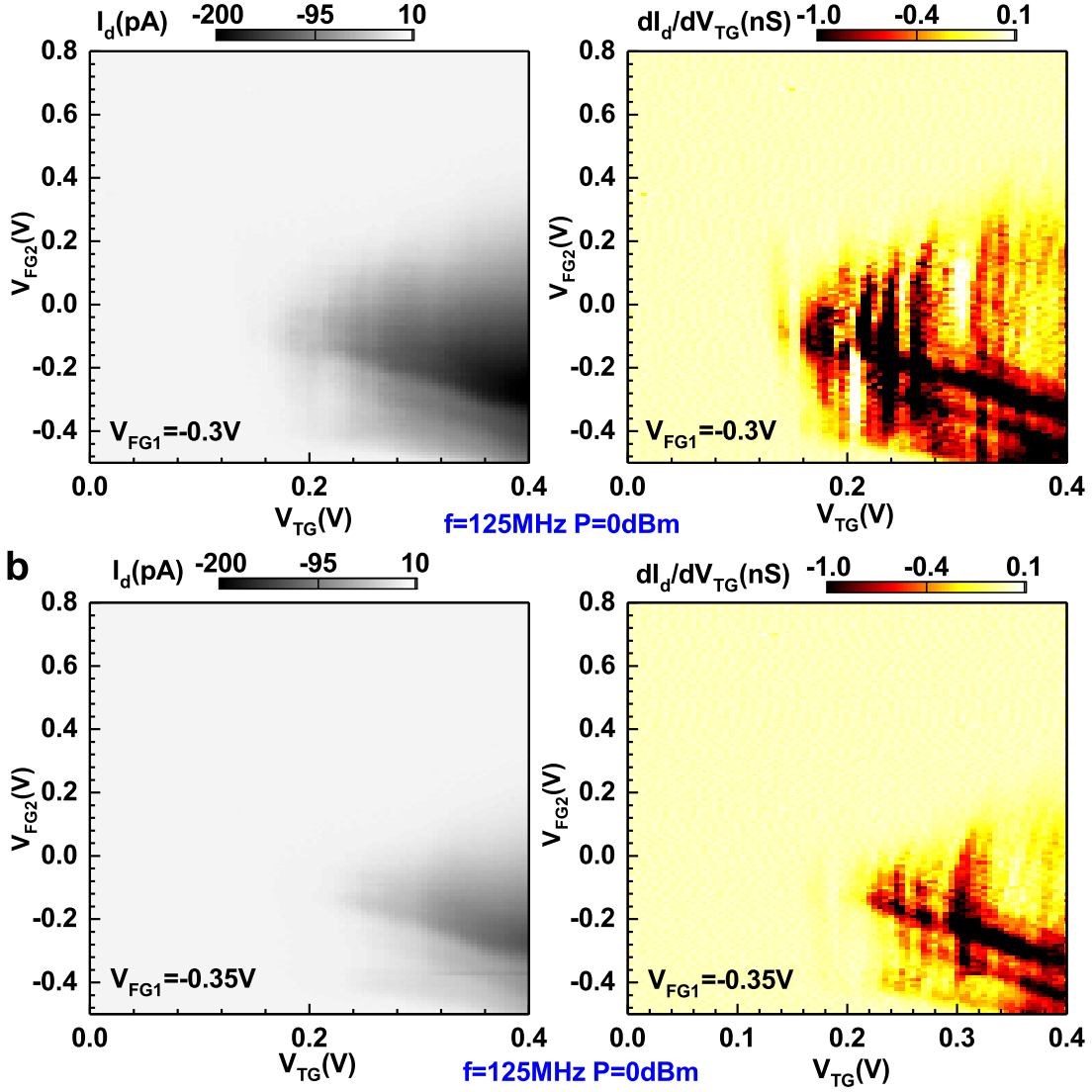

FIGURE 4.21: Current and differential conductance stability diagram of the single electron pump with RF signal on FG2. In (a) FG1 was biased at -0.3V, (b) FG1 was biased at -0.35V.

to make sure one and only one electron would be ejected from the quantum dot in the ejection process.

By observing the stability diagram very carefully, I could identify several 'plateaus' in the stability diagram if the RF power was -1 dBm. In order to confirm the single electron pump characteristics, I checked the I_{d}-V_{TG} characteristics when V_{FG2} is 0.04 V, which just passed several of the plateaus. The result is shown in Fig. 4.22.

In Fig. 4.22, I observed a current plateau at 1ef, near the V_{TG} of 0.2 V, at 125 MHz RF frequency and -1 dBm RF power. The FG1 was biased at -0.25 V and FG2 was biased at 0.04 V. The width of the plateau was roughly 18 mV. By calculating the average I_{d} on this plateau, I could estimate the error rate to be $\sim$ 0.828%, at the temperature of 4.2 K, with no magnetic field.

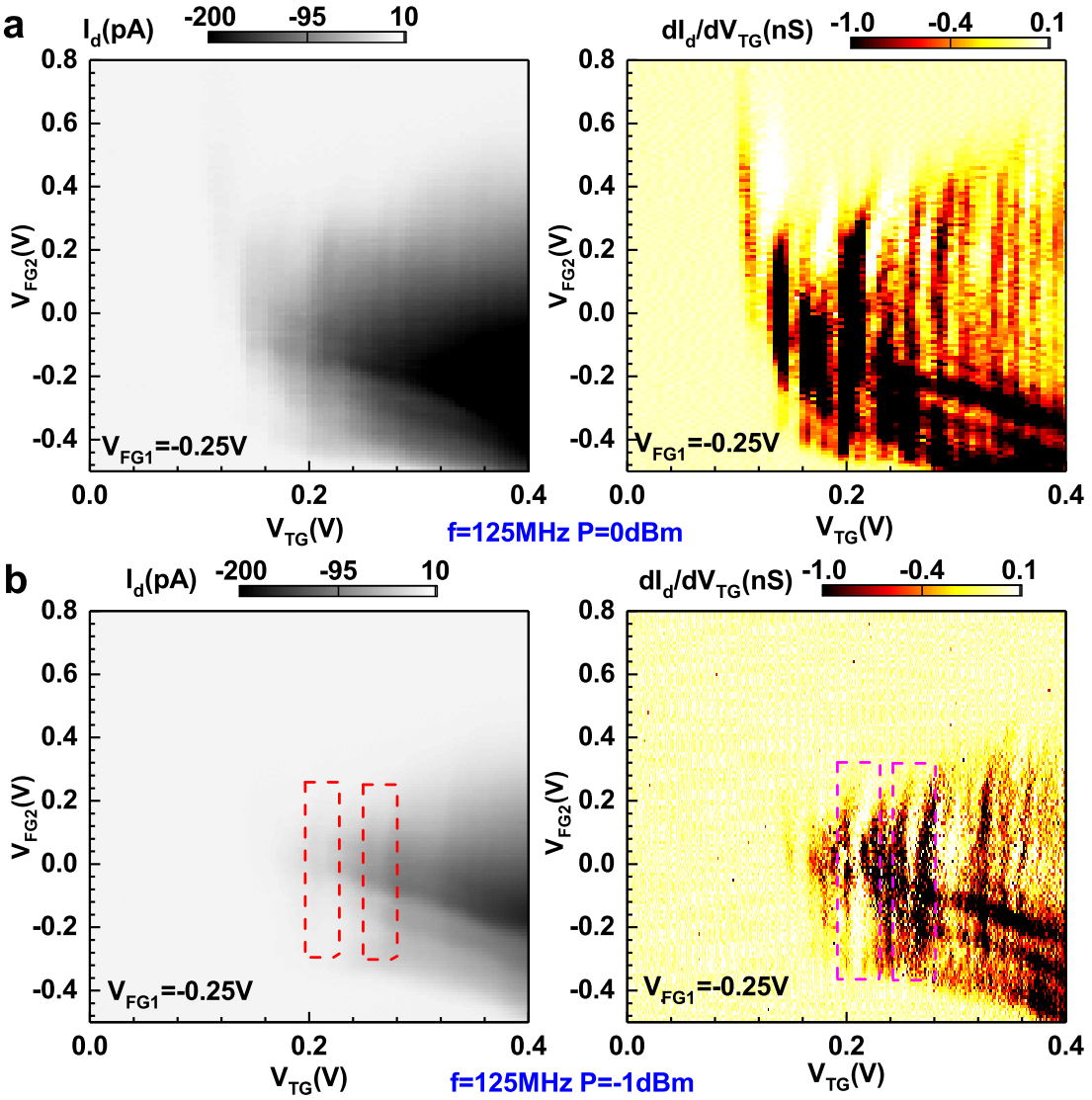

FIGURE 4.22: Current and differential conductance stability diagram of the single electron pump with RF signal on FG2. In (a) RF power was 0 dBm, (b) RF power was -1 dBm.

In order to have a better understanding of the device performance, I apply the decay cascade model[55, 56] to fit the data and extract parameters. In decay cascade model, the I_{d}-V_{TG} characteristics can be expressed in equation (4.17).

$$I_{\mathrm{pump}} = ef\sum_{n} n[\exp(-\exp(-\alpha V + \sum_{i=1}^{i=n}\delta_{\mathrm{i}})) - \exp(-\exp(-\alpha V + \sum_{i=1}^{i=n+1}\delta_{\mathrm{i}}))], \qquad (4.17)$$

The fitting result is shown in Fig. 4.23.

The decay cascade model gave a good fitting on the plateau regime and beyond, but showed some deviation between the 0-electron ejection and 1st plateau regime. The

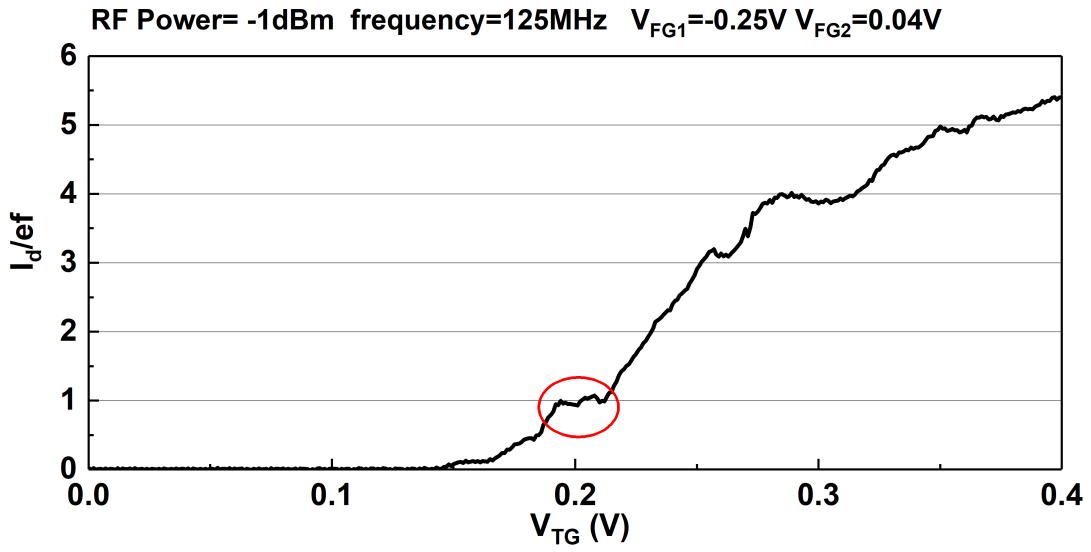

FIGURE 4.23: Plateau characteristics of the drain current.

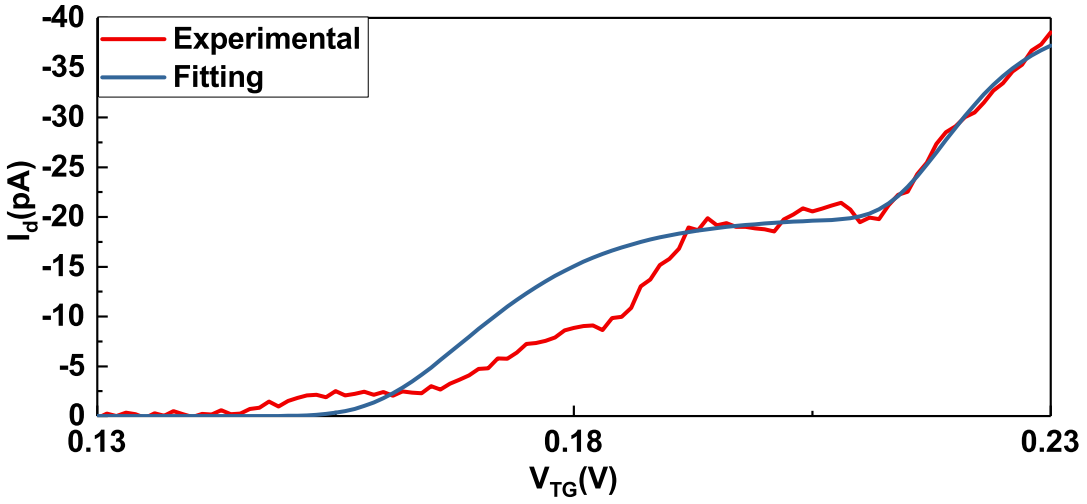

FIGURE 4.24: The fitting of decay cascade model with the experimental data.

deviation may come from the excitation states. I extracted the α to be 107 /mV and δ_1 to be 8.1, respectively.

After that, I would like to perform a repeatability test to check the reliability of the performance of the single electron pump device. However, I found poor repeatability of the current plateau, as shown in Fig. 4.24.

I measured the device characteristics at the same bias condition as Fig. 4.22, and found poor repeatability of the plateau. This shows significant reliability issue, which implies the presence of the charge trap. In order to understand the origin of the poor repeatability, I somehow recovered the plateau by sweeping up and down the gate bias many times to stabilise the device, and performed a measurement on the time domain

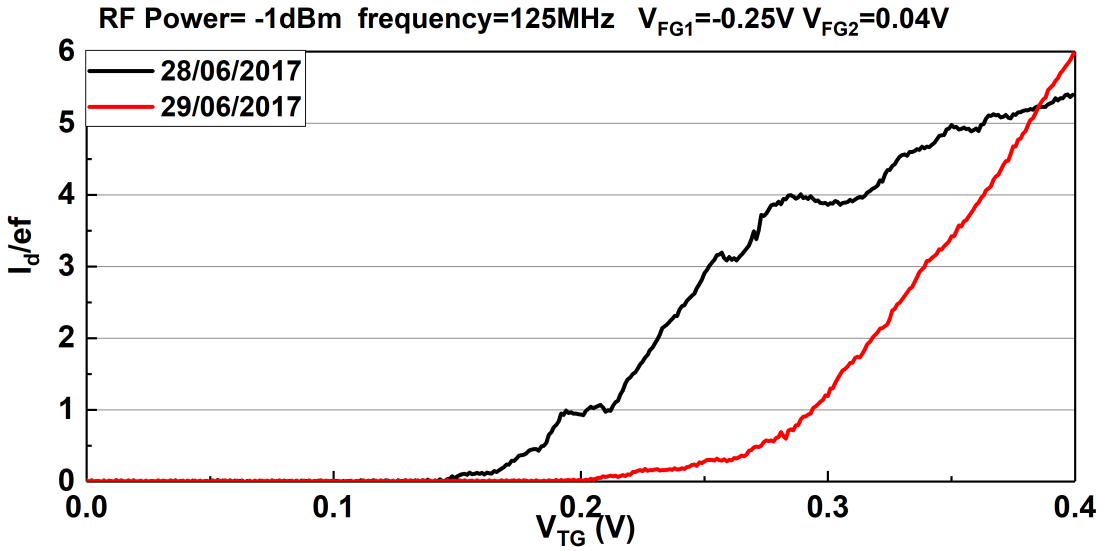

FIGURE 4.25: Repeatability test of the plateau.

characteristics of I_{d} at a bias condition where I could observe the plateau at 1ef. The time domain characteristics of I_{d} is shown in Fig. 4.25.

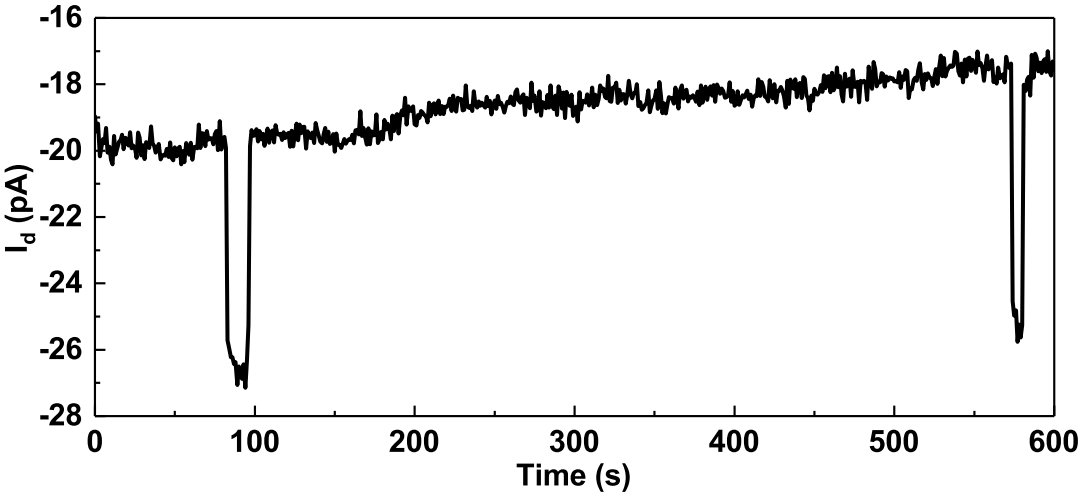

FIGURE 4.26: Time domain characteristics of drain current.

From Fig. 4.24, I observed the current was relatively stable in the first 50s. At $\sim$ 90 s, I observed RTN, and then the current started to shift slowly with continuous measurement on the time domain characteristics. This could be due to negative bias temperature instabilities(NBTI)[150, 151]. The NBTI and RTN implied that the instability of the device performance has very likely originated from charge traps.

Previously, in the work of NTT group, they demonstrated that the charge trap can be used as the quantum dot to pump electrons with high accuracy[79, 80, 81]. This time, I demonstrated that the charge trap can also be a negative factor for the single

electron pump. Since the amplitude of RTN is small ($\sim$ 6pA) and the drain bias is set to be 0, it was more likely coming from the impact of the threshold voltage shift by carrier trapping/de-trapping process. A trapped electron can shift the potential by e/C_{TG}, which was roughly 100 mV. This was much longer than our plateau width, therefore significantly affect the device characteristics. The long switching time implied the charge trap is located in the gate oxide, possibly coming from the RF stress during the experiments.

In order to check the RF dependence, I also measured the device at several other frequency points to observe the current. The average value of I_{d} at the plateau versus frequency was shown in Fig. 4.27. The device fails to show any plateau at frequencies larger than 125 MHz, which reveals weakness in RF response characteristics. There are several possible reasons responsible for this poor RF performance. First, the addition energy for the first electron in the quantum dot is not large enough to eliminate the impact from quantum excitations, as stated in the background research chapter. Second, the impact of parasitic capacitance is not carefully investigated in this design. The extra parasitic capacitance will result in extra RC constant in the system, which reduces the maximum response frequency achievable in the system. For the future work, investigations on the RF response is mandatory, and the device performance may be improved by careful designs to reduce the parasitic capacitance.

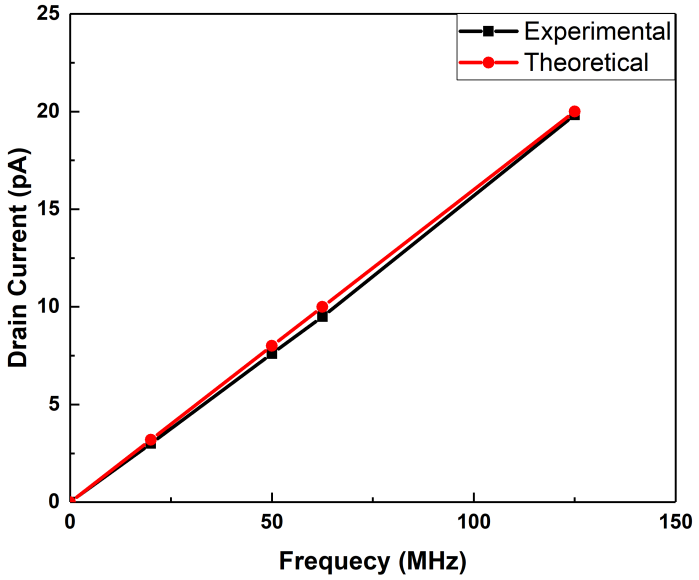

FIGURE 4.27: The RF response of the drain current. The drain current shows a rough linear dependence on frequency below 125 MHz. No plateau has been found at frequencies above 125MHz.

In conclusion, I understand that the charge trap is also a very important performance

impactor in the single electron pump. It will significantly degrade the device performance, resulting in significant reliability issue. The charge trap can be induced by the RF stress in the experiments[152]. This means I must improve the quality of oxide layer in the fabrication process, in order to improve the reliability and reach mass production level to achieve parallel operation for the single electron pumps. Also, I can also improve the RF reponse by optimising the designs to reduce the parasitic capacitance.

Chapter 5

Conclusions

In summary, we have successfully fabricated the Si single electron pump devices based on atomically flat [111] nanowire, using the facilities in Southampton Nanofabrication Centre. However, the yield is not high, only 94 out of 736, which is 12.8%. The major issue is due to the damage from the ultrasonic in the lift-off process and the metal diffusion in the final annealing process. We measured the characteristics of Si quantum dots based on advanced MOSFETs, and investigated on the reliability of the device. We measured one of the single electron pumps, confirmed the current plateau with the error rate of 0.828%, at 4.2 K, with no magnetic field. We found the unstable performance, which is due to random telegraph noise originated from carrier trapping/de-trapping process.

The achievements in my PhD project can be concluded into the following points:

First, we demonstrated that the advanced short-channel Si MOSFETs have the potential to show Si quantum dots at low temperatures.The Poly-Si grain boundaries can result in the thickness variation of dielectric layer, which will result in significant potential variations in the device channel, forming quantum dots. This effect can be observed at low temperatures and in the devices with thin dielectric.

Secondly, we showed that the charge trap can also affect the reliabilities of Si quantum dots through resonant tunnelling. The charge trap in the gate oxide can generate a narrow potential dip in the channel. The eigenstate of the electrons trapped in the channel can be in resonance with the eigenstate in the quantum dot, and significantly affect the device performance. We demonstrated that by measuring the device characteristics at low temperatures with precise bias sweep, we could identify the resonant peaks in the device and investigate the nature of charge trap systematically. This will provide a way for scientists and engineers to address the reliability issue.

At last, we showed that the oxide quality is a very important issue in Si single electron pump fabrication process. Single electron pumps require RF signal to drive, which will

result in stress in the oxide layer, and may generate charge traps. We demonstrate that the charge traps can also affect the reliability of the single electron traps by generating random telegraph noise and negative bias temperature instabilities in the channel. As a result, we must improve the oxide quality to achieve target of mass production and high operation frequency.

There are still many issues need to be addressed and processes needed to be improved. I summarise the most important of them below:

First, our fabrication process can be improved to increase the yield, performance and reliability. For example, we can include thinner nanowire and gate oxide design to reduce the step height, in order to achieve better scaling in the gate line and spacing. Also, the metal patterning processes can be improved to avoid issues originated from the ultrasonic wave, for example, optical resist based lift-off or metal dry etching. We could also use TiN as the barrier metal to stop the metal diffusion, which results in significant failure of the device. Besides, we could also adjust the annealing conditions for the oxide to reduce the number of traps and improve the quality of gate oxide, which will allow high-frequency RF operations.

Secondly, by improving the fabrication process, we could test the variation of the device parameters. For the parallel operation point of view, it is mandatory that the variation of the device parameters is not significant. In this device, we got the plateau width to be 18mV, which means the variations of the threshold voltage should be within 9mV. This is a challenge, especially for the scaled devices in University Fabrication grade.

Thirdly, we could check the dependence of the plateau width and other output characteristics for the single electron pumps on the other parameters in detail, for example, barrier height(controlled by gate bias), nanowire width, gate length and spacings, etc., in order to obtain a clearer image on the device physics for the single electron pump. As discussed, the decay cascade model still shows deviation with the experimental data in some bias conditions, and we could improve it by investigating further.

In total, unique contributions were made in this PhD project, especially regarding the charge traps and reliability issues linked to Si quantum dots and Si single electron pump. There are still many things to investigate on, and many challenges to overcome, for the single electron pumps, and for the completion of the quantum metrology triangle to establish a new definition for Ampere.

Appendix A

Gate dry etching recipe development

In order to pattern the Si single electron pumps, a well established gate dry etching recipe with vertical profile is mandatory.

First, we need to estimate the selectivity required for this single electron pump lot. The thickness of Poly-Si is about 100 nm, and we will apply 100% overetch, to make sure that all the Poly-Si side walls are removed in the process. However, we should not damage the oxide layer too much, in order to avoid issues from charge traps created from the damage of plasma. We need to etch Poly-Si gate layer for twice: FG layer and TG layer, respectively.

If we consider FG layer, we should not damage more than half of the FG layer in order to avoid any further damage to the oxide layer near the oxide/nanowire interface. As a result, the selectivity should be larger than 100 nm/10 nm=10. If we consider the TG layer, we should not damage the protective layer above the FG. Since the thermal oxide thickness above Poly-FG is roughly 5nm, the selectivity should be larger than 100 nm/5 nm=20. In that case, we need to improve the recipe to reach at least 20:1 selectivity, for the successful fabrication of the gate layer.

HBr/O_2 plasma gas is considered as a good candidate for Poly-Si etching[153, 154, 155]. There are three key parameters for the recipe: gas flow rate, ICP power and RF power. For the gas flow rate, I fix the gas flow rate to be 45 sccm for HBr and 5 sccm for O_2. I tested the ICP power, and found instabilities of the chamber condition (significant re-deposition observed) when the ICP power is larger than 400 W for this recipe. As a result, we fix the ICP power to be 400 W, and investigate on the dependence of etching rate of Poly-Si and SiO_2, and the selectivity between them on RF power. The measurement results are shown in Fig. A.1.

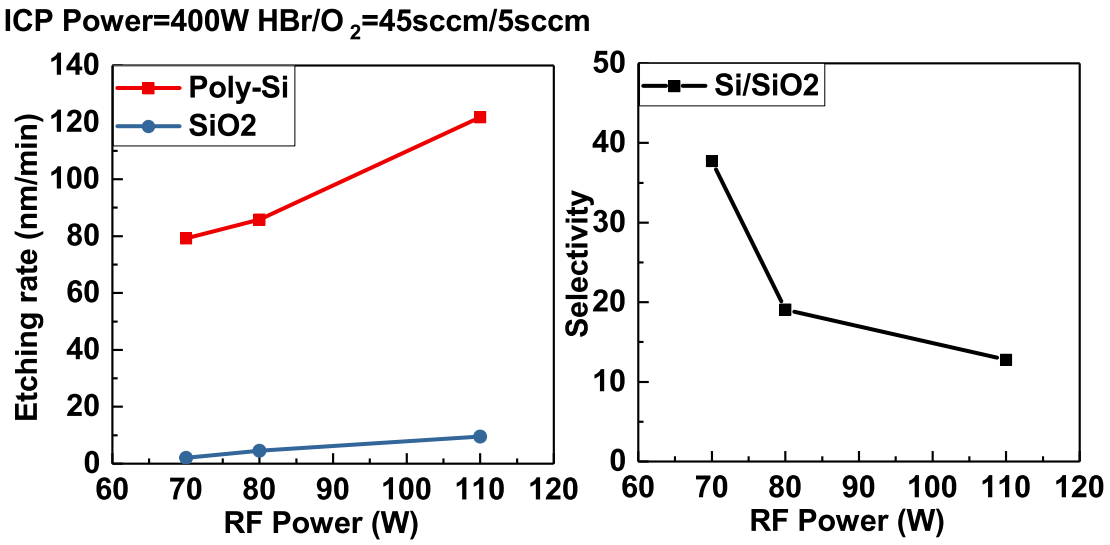

FIGURE A.1: Dependence of the dry etching rate and selectivity on the RF power for HBr/O_2 recipe.

From Fig. A.1, we found that the etching rate of Poly-Si and SiO_2 both decreases if we reduce the RF power. However, the selectivity significantly improves, and reach about 40:1 when the RF power is 70 W. This is because the reduction of RF power reduces the power of plasma ions. As a result, the impact from chemical reaction between ions will become stronger, while the physical 'bombing' is suppressed, which is in agreement with the experimental data.

Based on the measurement result, we decide to choose RF power to be 70 W for our Poly-Si etching. However, due to the very high selectivity, even native oxide will block the etching. The roughness of the native SiO_2 will give huge variations across the Poly-Si surface. As a result, we need to perform a low-selectivity process (6:1) with HBr only and RF power=110 W to pre-etch first, and then starts to use the main HBr/O_2 recipe. In order to check the impact of different overetching, we perform different tests to observe the SEM image of the plane view and cross-section. The etched patterns are 100 nm line-and-space patterns for cross-section and 50 nm/100 nm line/spacing for the plane view. The plane view results are shown in Fig. A.2. and the cross-sections are shown in Fig. A.3.

In Fig. A.2, we could observe that with 200% overetching, some edges of gate structures were damaged in the dry etching. This could be due to the variation of the e-beam resist HSQ thickness at the edge.

From Fig. A.3, we could observe that for 0% and 100% overetching, the recipe gives a very good vertical profile, almost 90 degree. However, we can observe some remaining of the Poly-Si layer at the edge of each Poly-Si pattern (rounded part), which means 0% overetching is not enough. In Fig. A. 3(b), the remaining part is not observed, which

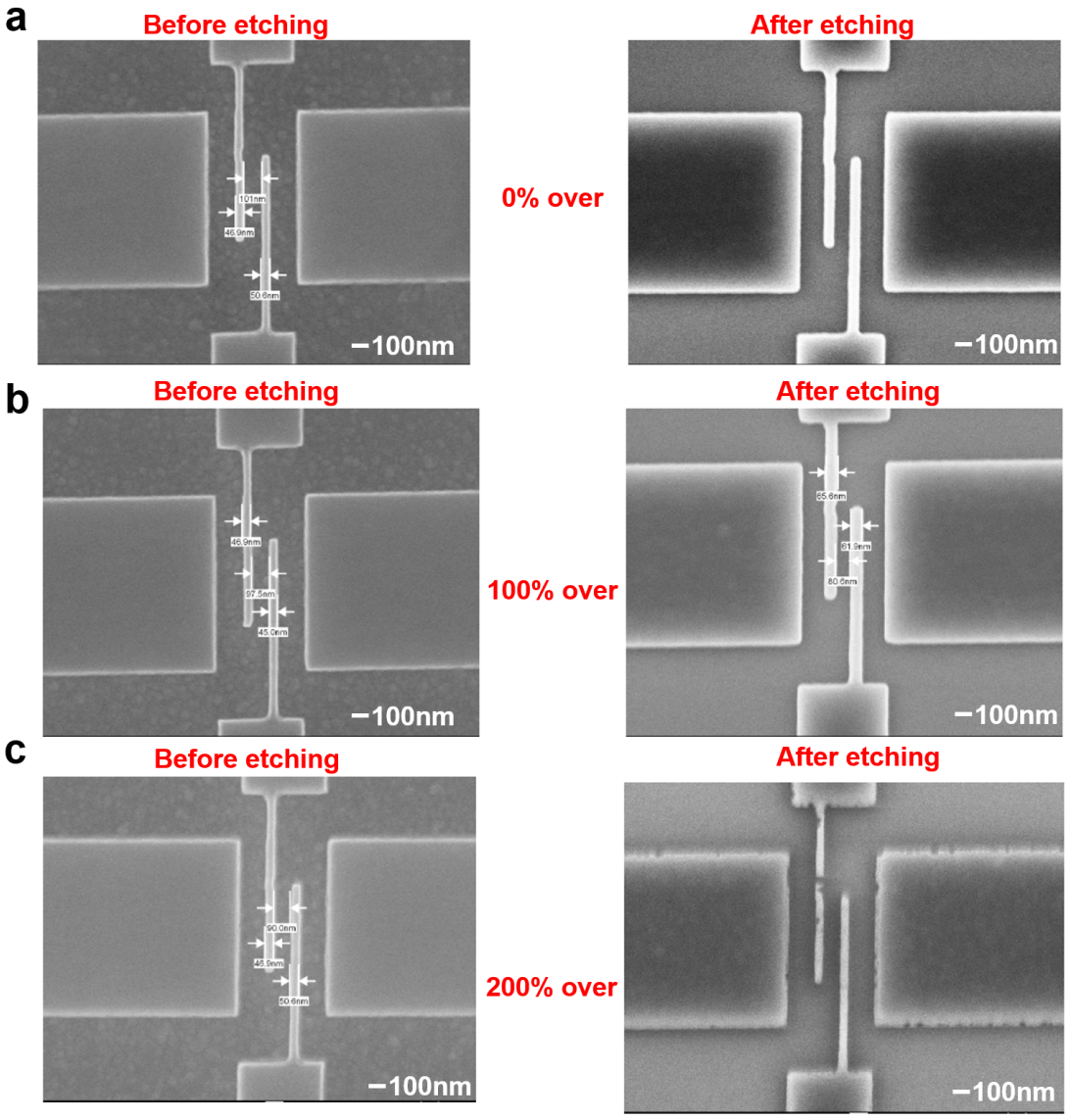

FIGURE A.2: Dependence of the dry etching rate and selectivity on the RF power for HBr/O_2 recipe.

shows a good . The rounded top of the pattern is the resist part, which is consistent with the fact that the edges of HSQ layer are easy to be damaged.

From these experiments, I successfully establish an ICP anisotropic etching, with the selectivity of 40:1, and vertical (almost 90 degree) etching profile. The relationship between the etching rate, selectivity and RF power has been successfully established.

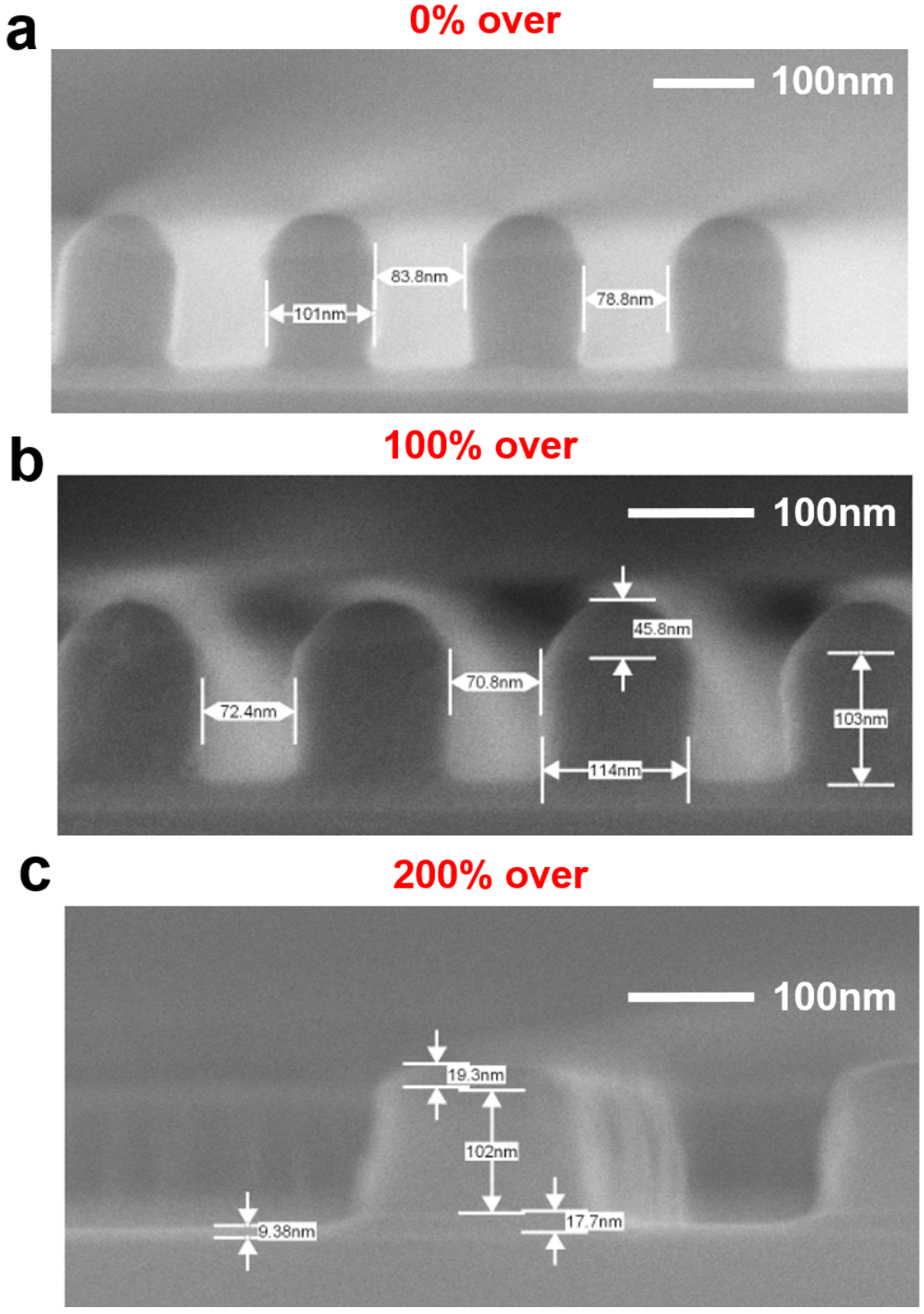

FIGURE A.3: Dependence of the dry etching rate and selectivity on the RF power for HBr/O_2 recipe.

Appendix B

Dopant diffusion test

In our fabrication process, the dopants in Poly-Si gate, raised source and drain will be annealed for a long time. If the annealing time is too short, the dopant concentration is not enough to form the dopant band. Under that circumstance, the Poly-Si gate, raised source and drain will become insulator at cryogenic temperatures, and we could not achieve proper device operation. If the annealing time is too long, the dopant will penetrate into the SiO_2 layer significantly, and may even go further into the substrate. Therefore, the total annealing time must be carefully chosen to avoid troubles.

In order to check the dopant diffusion, we make different MOS capacitors with large size to test the sheet resistance, pinhole density and dopant penetration. The schematic diagram of cross-section and mask layout are shown in Fig. B.1.:

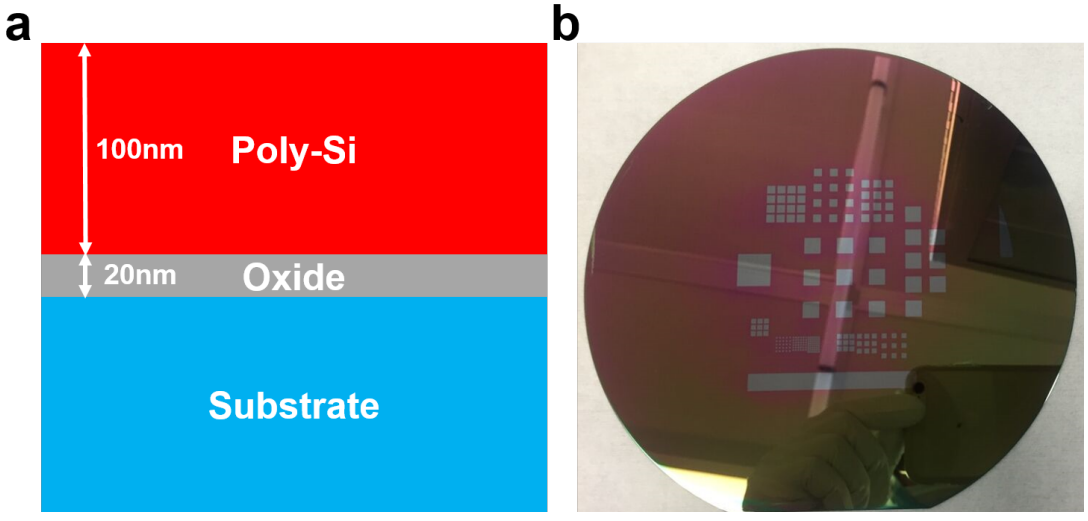

FIGURE B.1: The schematic diagram of cross-section and mask layout of the capacitors. (a) shows the cross-section while (b) shows the mask layout.

The capacitors were fabricated on bulk-Si substrate. The Poly-Si thickness was 100nm and the gate oxide thickness was 20 nm, which was the same as our main fabrication lot.

We deposited LPCVD Poly-Si everywhere, and use optical lithography, with AZ2070 as the resist. After that, we use the same ICP etching recipe with HBr/O_2 to etch all the Poly-Si dielectric. After cleaning and annealing process, the capacitors have been successfully fabricated, and we will measure the devices. Due to the requirement to measure sheet-resistance and extra complexity in fabrication, the metallisation step is not included, and we will measure the characteristics directly by probing onto the Poly-Si layer.

First, we checked the sheet resistance of the device, and extracted the doping concentration in Si. We tested the results when the device is annealed for 20 s, 40 s, 60 s, 120 s, 300 s and 600 s, respectively. The measurement result are shown in Fig. B.2.

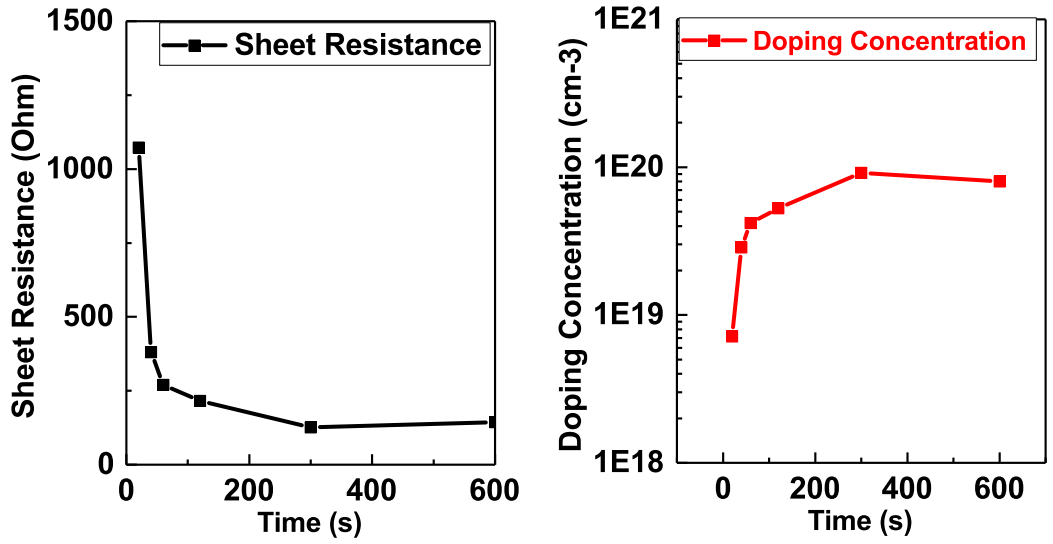

FIGURE B.2: Sheet resistance and doping concentration versus time. (a) shows the measured sheet resistance while (b) shows the extracted doping concentration.

In order to achieve degenerately doping, the donor level must be broadened into bands. Therefore, the impurity concentration must be higher than 10^{19} cm^{-3}. As a result, the total diffusion time must be larger than 20 s to achieve metallised Poly-Si. We can notice that the impurity concentration drops when the Poly-Si is annealed for 10min. This probably has originated from the penetration into the oxide. We can roughly estimate the penetrated dopants to be 10^{14} cm^{-2}.

In order to check further, we test the gate leakage of the devices. We found no leakage for the capacitors with the size 0.5 mm×0.5 mm, while leakages were observed for the some of the capacitors with the size 1.5 mm×1.5 mm, and all leakage for capacitors with the size 5 mm×5 mm. We could roughly estimate the pinhole density to be ~ 1 $/mm^{-2}$. Considering our TG size, it means 1.5 pinholes in TG layer for every 1000 devices, and 1 pinhole in FG layer for every 100 million devices, which are both acceptable. This shows our LPCVD poly-Si has good quality.

In order to confirm the characteristics in detail, we measured the CV characteristics of the device annealed for 120 s(2 min), 300 s(5 min) and 600 s(10 min). Since there were significant leakage for all 5 mm×5 mm devices, we just investigate on the 0.5 mm×0.5 mm and 1.5 mm×1.5 mm devices without any leakage current. The C-V characteristics were measured with B1500A, under an RF signal of 100 kHz. The results were shown in Fig. B.3.:

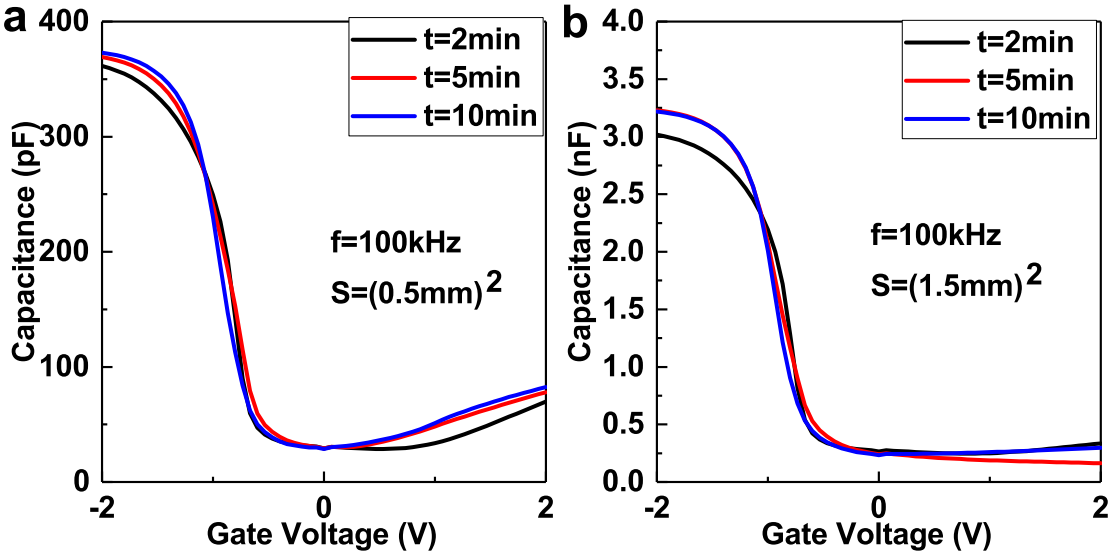

FIGURE B.3: Sheet resistance and doping concentration versus time. (a) shows the measured sheet resistance while (b) shows the extracted doping concentration.

The thickness of oxide layer is slightly different between wafers. However, all the devices show the same minimum capacitances, which implies the same substrate doping concentration for all the three wafers. As a result, no dopants have been able to penetrate through the whole oxide layer into the substrate, even with the annealing time of 10 minutes.

However, dopants in the oxide layer will already give variations on the threshold voltage, and may also result in RTN in the devices. As a result, a total annealing time of 10 minutes is unacceptable. Therefore, we decide to choose 5 minutes as the maximum tolerance.

Poly-FG will be the gate that anneal for the longest time. The Poly-FG layer will be annealed for 3 times, once for FG layer annealing, once for FG layer oxidation to form the FG-TG insulating oxide, and another once for TG layer annealing. If we assume the single annealing time to be t_{anneal} and the oxidation time to be $t_{\text{oxidation}}$, the total annealing time for FG will be $2t_{\text{anneal}} + t_{\text{oxidation}}$. Since $t_{\text{oxidation}}$ must be at least 3 minutes to form 5 nm RTA thermal oxide, the maximum value for t_{anneal} is 1 minute. As shown in Fig. B.2, in 1 minute, the doping concentration is 4.2×10^{19} cm^{-3}, which is enough for the impurity band formation, so TG layer can be metallised.

Based on all the tests carried, we choose the annealing time to be 1 minute for both FG and TG.

Appendix C

L-Edit Layout for the device design

C.1 Mask Layout Design

In order to show the design with more detail, the colour codes for different layers are shown in Fig. C.1.

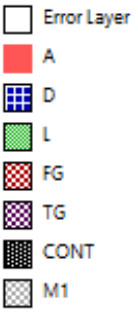

FIGURE C.1: Colours of different layers in the mask design layout.

C.1.1 Main Design (a): 2 First Gates

In this design, the size of metal layer is relatively large. Only one device will be fabricated in a single chip.

The plane view of the Source/Drain area is shown in Fig. C.3. In the S/D contact Region, the SOI part (L layer) is the largest regime, with the width of 7 μm. The poly-Si region (FG layer) is the second largest, with the width of 6 μm. The doping window region (D layer) is 5 μm wide, the metal region (M1 layer) is 4 μm wide, and the contact region (CONT layer) is 3 μm wide. The plane view of the active device region is shown in Fig. C.4, with two first gates. All the key variables are marked in Fig. C.4.

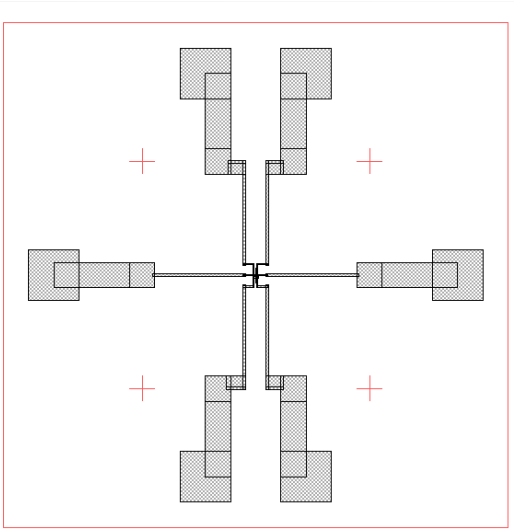

FIGURE C.2: Brief View of Design (a). This shows the metal-layer layout of the design.

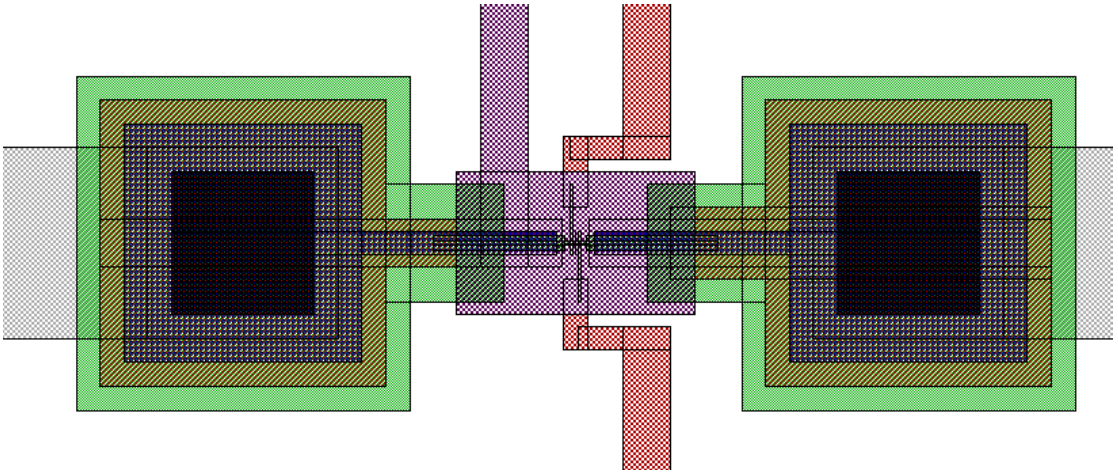

FIGURE C.3: Detailed View of Design (a). This shows the source/drain layout of the design.

In this design, the two first gates (parameters controlled by variables) and a top gate (5 μm×3 μm for all designs) define the quantum dot in th silicon nanowire regime. Two first gate are mainly used to control the tunnelling barriers of the quantum dot while the top gate is used to control the depth of potential well and carrier concentration in the nanowire regime. In this design, the dog-bone structure is used to minimise the impact of the proximity effect in the e-beam lithography process. However, the dog-bone structure will also increase the Source/Drain coupling resistance. Besides, the distance between the edge of dopant diffusion window (D layer) and left gate is kept at a constant value. Since it is very hard to estimate the diffusion length accurately, this may also be a drawback of this design.

The value of the design variables for this design are summarised below in a table (Unit: nm):

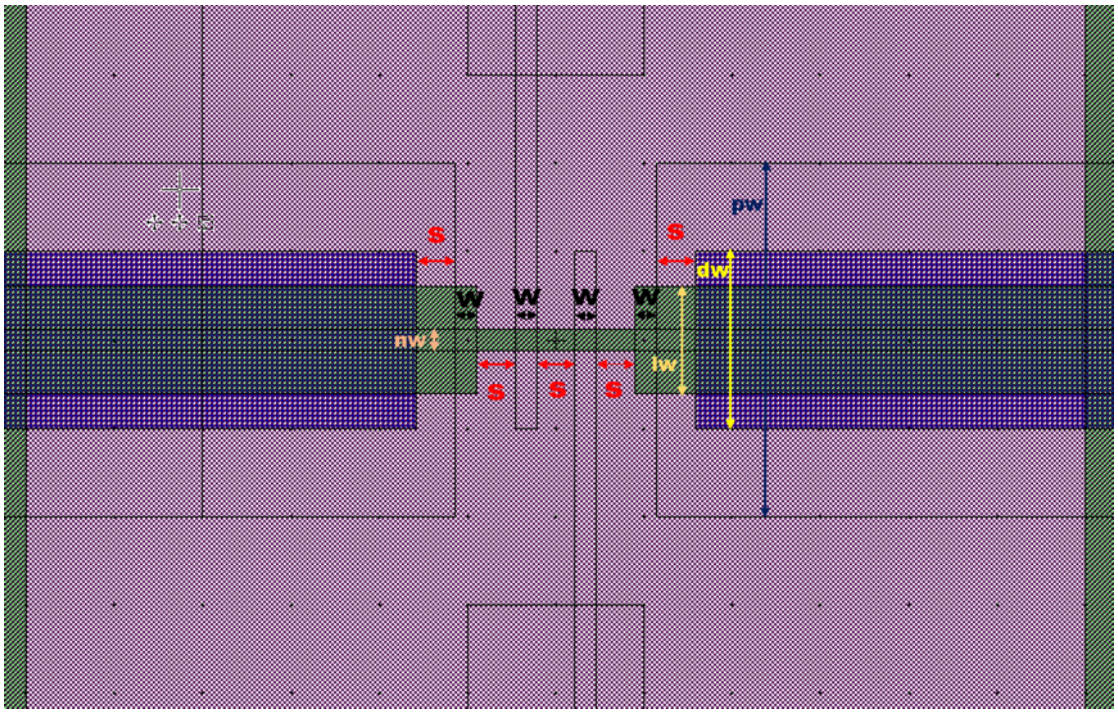

FIGURE C.4: Focusing View of Design (a). This shows the layout near the quantum dot region of the design.

TABLE C.1: Design parameter variables for the design style (a)

Name	w	s	nw	lw	dw	pw
X03Y01	25	75	25	300	500	1000
X03Y02	40	90	40	300	500	1000
X03Y03	50	100	50	300	500	1000
X03Y04	60	110	60	300	500	1000
X03Y05	75	125	75	300	500	1000
X03Y06	100	150	100	300	500	1000
X03Y07	200	250	200	300	500	1000
X03Y08	500	550	500	300	500	1000
X04Y01	25	100	25	300	500	1000
X04Y02	40	100	40	300	500	1000
X04Y03	50	100	50	300	500	1000
X04Y04	60	100	60	300	500	1000
X04Y05	75	100	75	300	500	1000
X04Y06	100	100	100	300	500	1000
X04Y07	200	100	200	300	500	1000
X04Y08	500	100	500	300	500	1000

C.1.2 Main Design (b): 3 First Gates

The design of metal layer is the same as design (a) and only one device will be fabricated in a single chip.

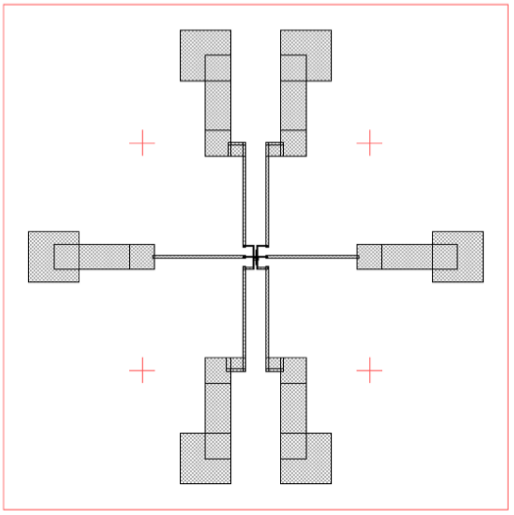

FIGURE C.5: Brief View of Design (b). This shows the metal-layer layout of the design.

The S/D regime design is the same as main design (a). The plane view of the active device region is shown in Fig. C.7, with three first gates:

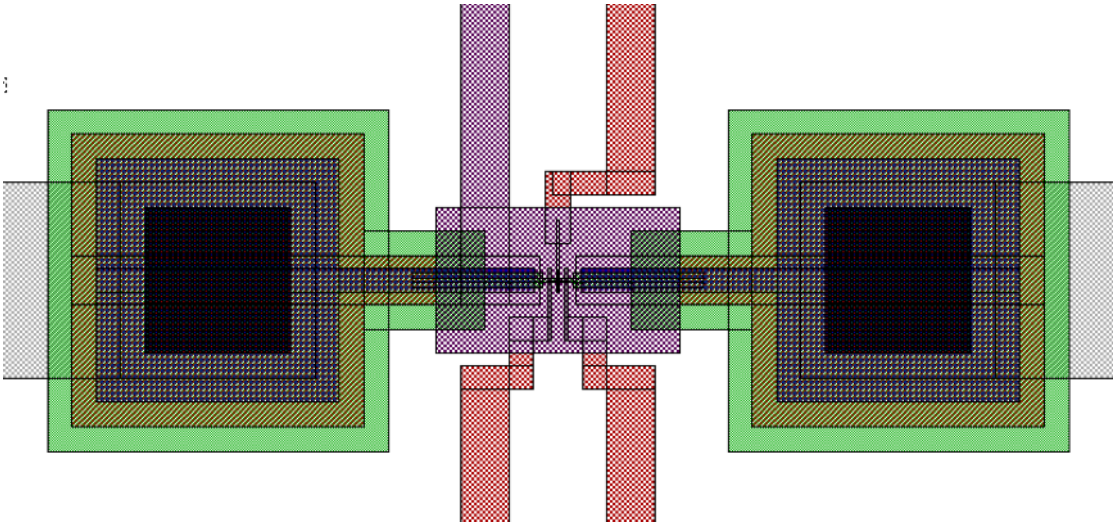

FIGURE C.6: Detailed View of Design (b). This shows the source/drain layout of the design.

The style is the same as design (a), except for the number of gates used to create potential barriers or form quantum dots. The extra gate gives more flexibility of the design, and is able to detect the energy of the single electron ejected from the quantum dot. This will help understand the operation of single electron pump.

The value of the design variables for this design are summarised below in table 3.2 (Unit: nm):

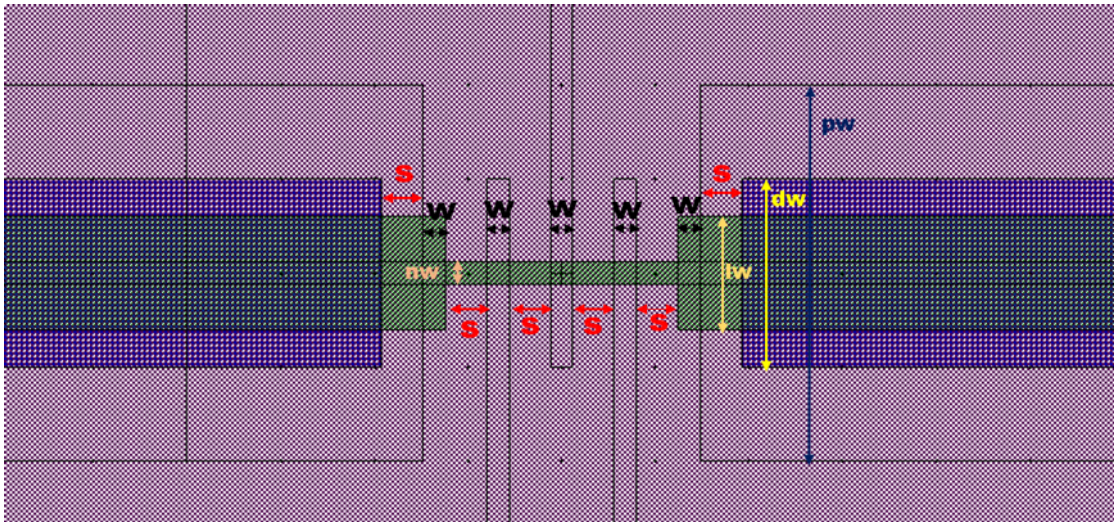

FIGURE C.7: Focusing View of Design (b). This shows the layout near the quantum dot region of the design.

TABLE C.2: Design parameter variables for the design style (b)

Name	w	s	nw	lw	dw	pw
X05Y01	25	75	25	300	500	1000
X05Y02	40	90	40	300	500	1000
X05Y03	50	100	50	300	500	1000
X05Y04	60	110	60	300	500	1000
X05Y05	75	125	75	300	500	1000
X05Y06	100	150	100	300	500	1000
X05Y07	200	250	200	300	500	1000
X05Y08	500	550	500	300	500	1000
X06Y01	25	100	25	300	500	1000
X06Y02	40	100	40	300	500	1000
X06Y03	50	100	50	300	500	1000
X06Y04	60	100	60	300	500	1000
X06Y05	75	100	75	300	500	1000
X06Y06	100	100	100	300	500	1000
X06Y07	200	100	200	300	500	1000
X06Y08	500	100	500	300	500	1000
X07Y01	50	40	50	300	500	1000
X07Y02	50	50	50	300	500	1000
X07Y03	50	60	50	300	500	1000
X07Y04	50	75	50	300	500	1000
X07Y05	50	100	50	300	500	1000
X07Y06	50	125	50	300	500	1000
X07Y07	50	150	50	300	500	1000
X07Y08	50	200	50	300	500	1000
X08Y01	50	100	50	300	500	1000
X08Y02	50	100	50	300	500	1000
X08Y03	50	100	50	300	500	1000
X08Y04	50	100	50	300	500	1000
X08Y05	50	100	50	300	500	1000
X08Y06	50	100	50	300	500	1000
X08Y07	50	100	50	300	500	1000
X08Y08	50	100	50	300	500	1000

C.1.3 Main Design (c): 2 First Gates+ 1QD

The design of metal layer is the same as design (a) and only one device will be fabricated in a single chip.

The S/D regime design is the same as main design (a). The plane view of the active device region is shown in Fig. C.10.

The difference between design (a) and design (c) is the hole inside the nanowire. This hole will form an extra quantum dot in the 2-DEG region in the channel, and we are

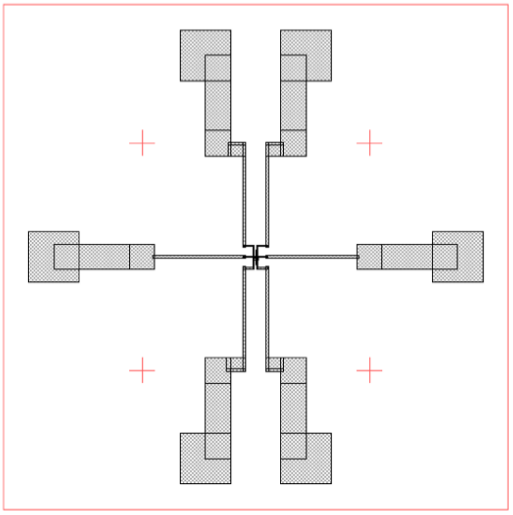

FIGURE C.8: Brief View of Design (c). This shows the metal-layer layout of the design.

interested to see the characteristics of the quantum dot and the performance of single electron pump with this type of design.

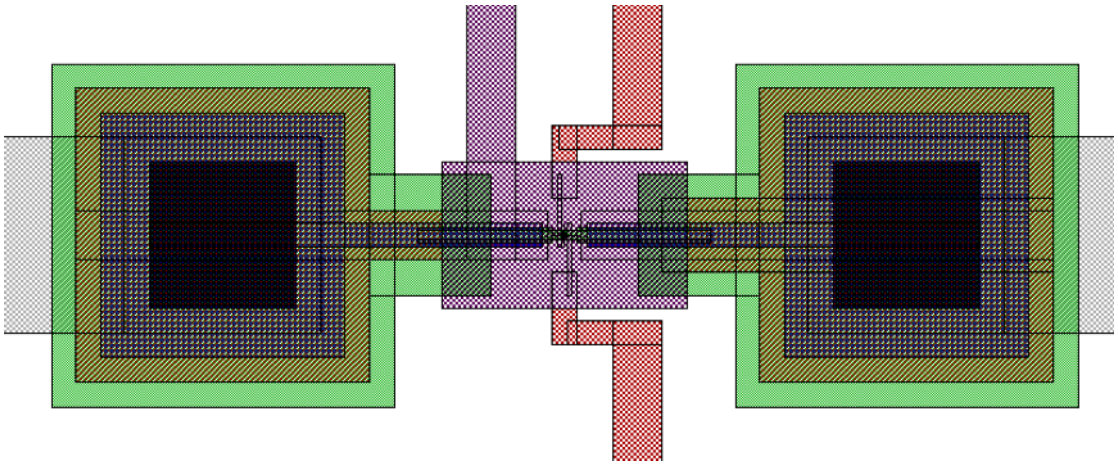

FIGURE C.9: Detailed View of Design (c). This shows the source/drain layout of the design.

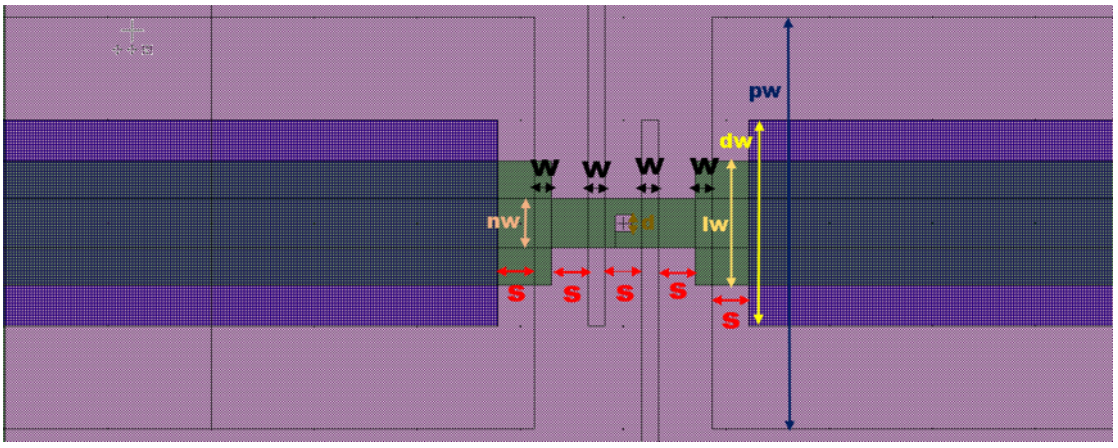

FIGURE C.10: Focusing View of Design (c). This shows the layout near the quantum dot region of the design.

The value of the design variables for this design are summarised below in a table (Unit: nm):

TABLE C.3: Design parameter variables for the design style (c)

Name	w	s	nw	lw	dw	pw	d
X09Y01	25	75	25	300	500	1000	25
X09Y02	40	90	40	300	500	1000	40
X09Y03	50	100	50	300	500	1000	50
X09Y04	60	110	60	300	500	1000	60
X09Y05	75	125	75	300	500	1000	75
X09Y06	100	150	100	300	500	1000	100
X09Y07	200	250	200	300	500	1000	200
X09Y08	500	550	500	300	500	1000	500

C.1.4 Main Design (d): 3 First Gates+ 1QD

The design of metal layer is the same as design (a) and only one device will be fabricated in a single chip.

The S/D regime design is the same as main design (a). The plane view of the active device region is shown in Fig. C.13.

The design is the same as design (c), except for the number of gates used to create potential barriers or form quantum dots.

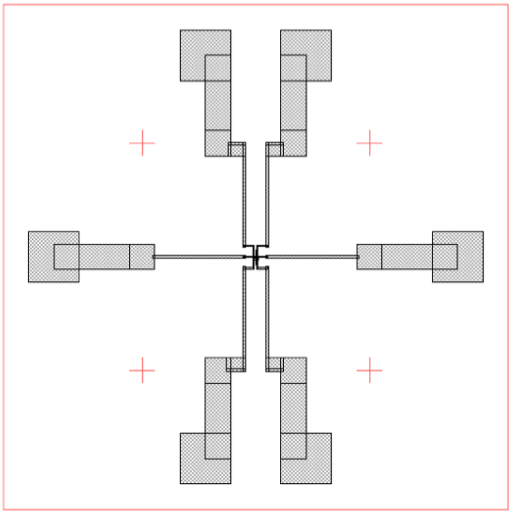

FIGURE C.11: Brief View of Design (d). This shows the metal-layer layout of the design.

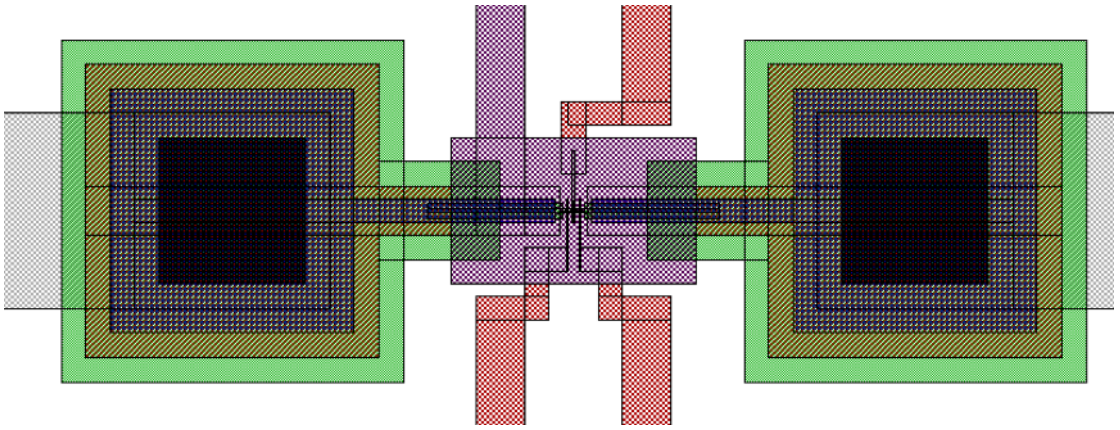

FIGURE C.12: Detailed View of Design (d). This shows the source/drain layout of the design.

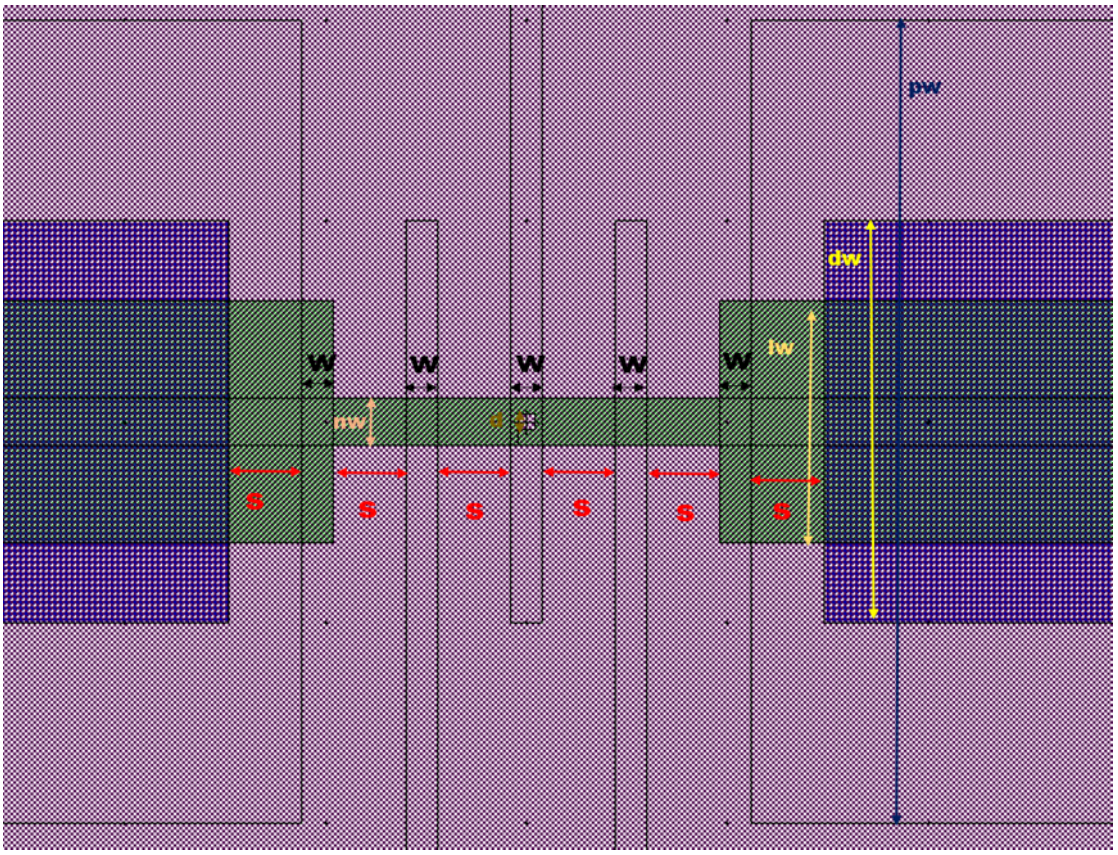

FIGURE C.13: Focusing View of Design (d). This shows the layout near the quantum dot region of the design.

The value of the design variables for this design are summarized below in a table (Unit: nm):

TABLE C.4: Design parameter variables for the design style (d)

Name	w	s	nw	lw	dw	pw	d
X09Y01	25	75	25	300	500	1000	12
X09Y02	40	90	40	300	500	1000	20
X09Y03	50	100	50	300	500	1000	25
X09Y04	60	110	60	300	500	1000	30
X09Y05	75	125	75	300	500	1000	38
X09Y06	100	150	100	300	500	1000	50
X09Y07	200	250	200	300	500	1000	100
X09Y08	500	550	500	300	500	1000	250

C.1.5 Secondary Design (e): 2 First Gates

Unlike the design for style (a), (b), (c) and (d), we reduce the size of metal layer in order to achieve the high integration density. 16 devices will be fabricated in a single chip.

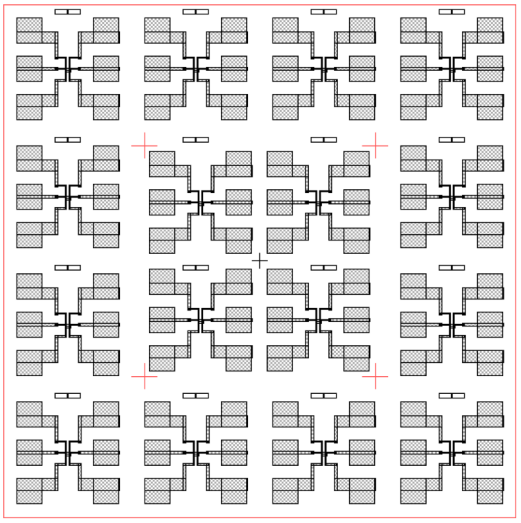

FIGURE C.14: Brief View of Design (e). This shows the metal-layer layout of the design.

The plane view of the Source/Drain area is shown in Fig. C.15, and the plane view of the active device region is shown in Fig. C.16. Except for the metal part, the design (e) is the same as design (a).

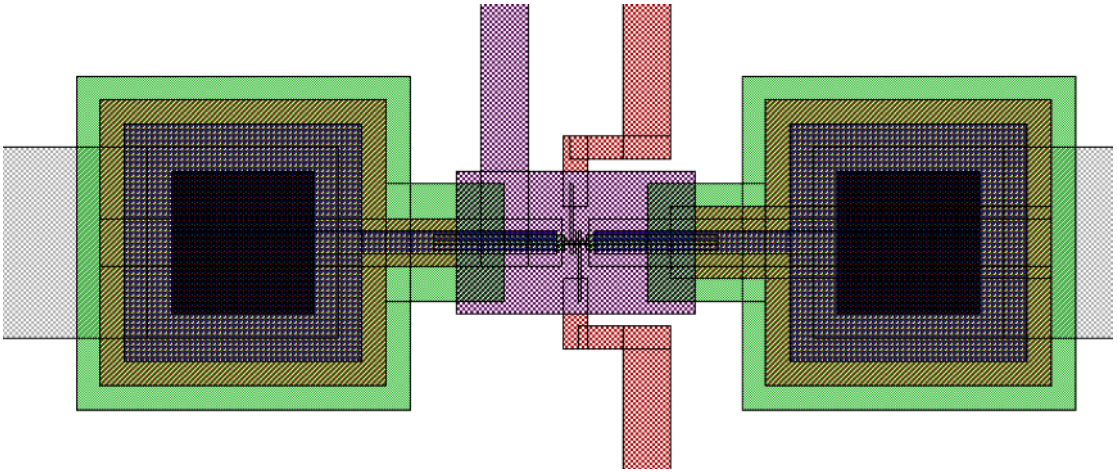

FIGURE C.15: Detailed View of Design (e). This shows the source/drain layout of the design.

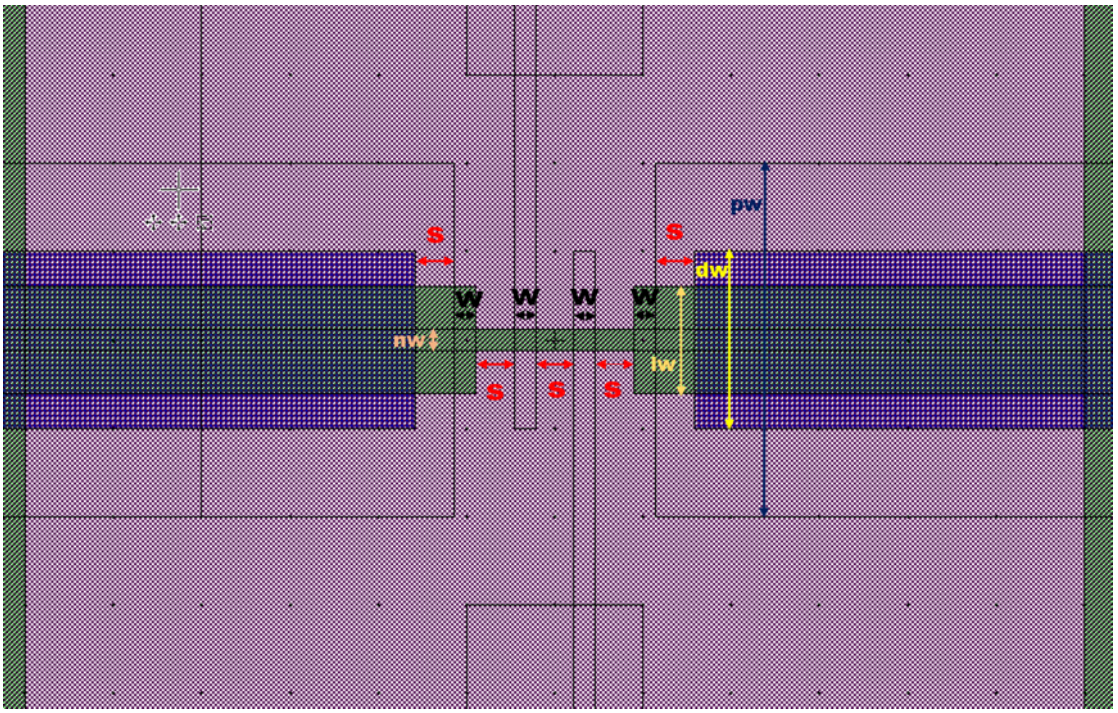

FIGURE C.16: Focusing View of Design (e). This shows the layout near the quantum dot region of the design.

The value of the design variables for this design are summarised below in a table (Unit: nm):

For X01Y01, X11Y01 and X11Y05, the variables are shown below:

TABLE C.5: Design parameter variables for the design style (e)

Name	w	s	nw	lw	dw	pw
XX01YY01	50	50	10	300	500	1000
XX02YY01	50	50	20	300	500	1000
XX03YY01	50	50	30	300	500	1000
XX04YY01	50	50	40	300	500	1000
XX01YY02	50	50	50	300	500	1000
XX02YY02	50	50	100	300	500	1000
XX03YY02	100	100	20	300	500	1000
XX04YY02	100	100	30	300	500	1000
XX01YY03	100	100	40	300	500	1000
XX02YY03	100	100	50	300	500	1000
XX03YY03	100	100	100	300	500	1000
XX04YY03	150	150	20	300	500	1000
XX01YY04	150	150	30	300	500	1000
XX02YY04	150	150	40	300	500	1000
XX03YY04	150	150	50	300	500	1000
XX04YY04	150	150	100	300	500	1000

For X02Y01, X12Y01 and X12Y05, the variables are shown below:

TABLE C.6: Design parameter variables for the design style (e)

Name	w	s	nw	lw	dw	pw
XX01YY01	25	75	25	300	500	1000
XX01YY02	40	90	40	300	500	1000
XX01YY03	50	100	50	300	500	1000
XX01YY04	60	110	60	300	500	1000
XX02YY01	75	125	75	300	500	1000
XX02YY02	100	150	100	300	500	1000
XX02YY03	200	250	200	300	500	1000
XX02YY04	500	550	500	300	500	1000
XX03YY01	25	100	25	300	500	1000
XX03YY02	40	100	40	300	500	1000
XX03YY03	50	100	50	300	500	1000
XX03YY04	60	100	60	300	500	1000
XX04YY01	75	100	75	300	500	1000
XX04YY02	100	100	100	300	500	1000
XX04YY03	200	100	200	300	500	1000
XX04YY04	500	100	500	300	500	1000

C.1.6 Secondary Design (f): 2 First Gates

The design of metal layer is the same as design (e) and 16 devices will be fabricated in a single chip.

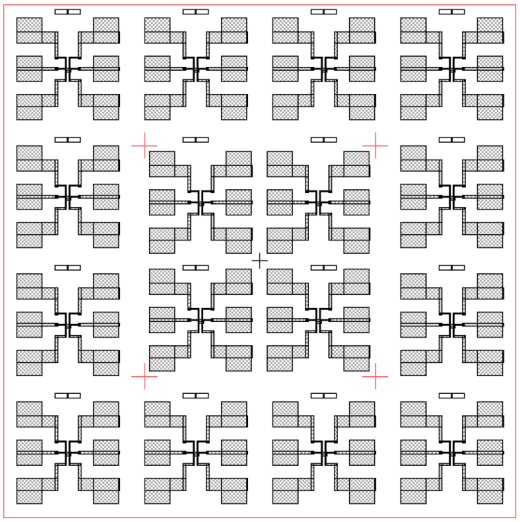

FIGURE C.17: Brief View of Design (f). This shows the metal-layer layout of the design.

The plane view of the Source/Drain area is shown in Fig. C.18, and the plane view of the active device region is shown in Fig. C.19.

The difference between design (f) and design (e) is the size of the dog-bone structure. In design (f), the width of the dog bone becomes 2 μm and dopant diffusion window is

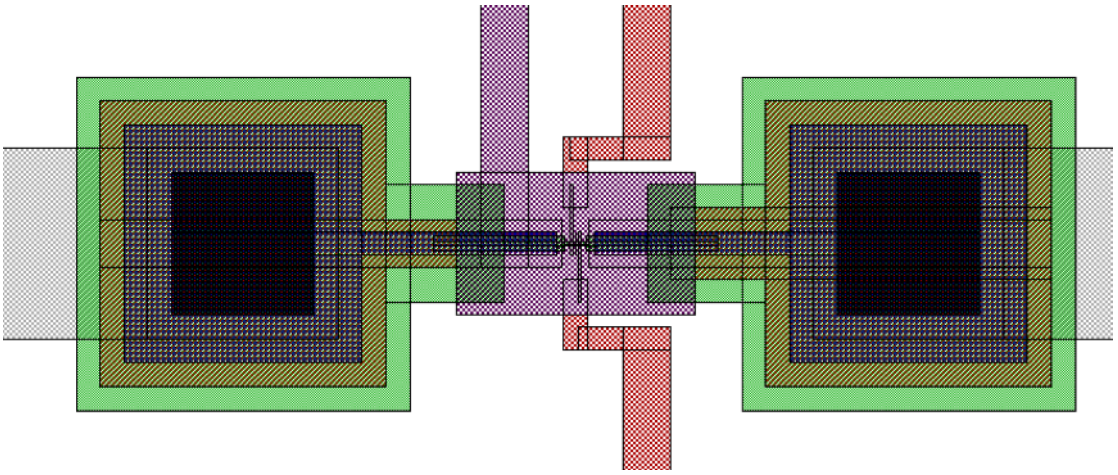

FIGURE C.18: Detailed View of Design (f). This shows the source/drain layout of the design.

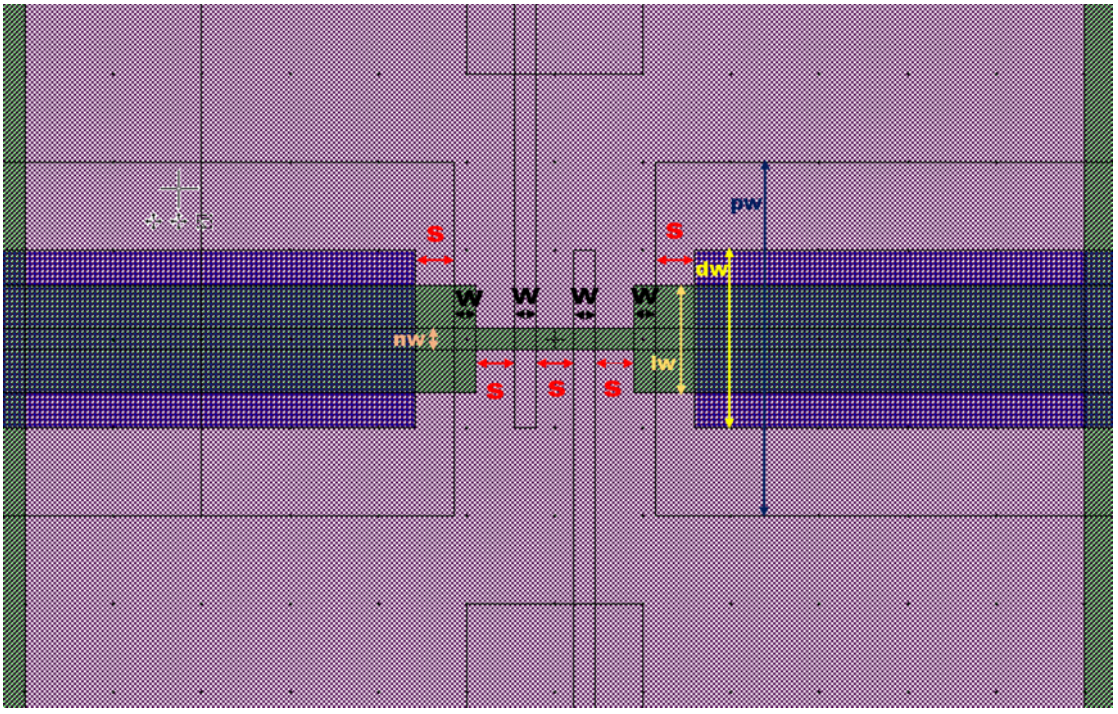

FIGURE C.19: Focusing View of Design (f). This shows the layout near the quantum dot region of the design.

also increased to 1 μm. The advantage is that the larger window is easier to be achieved by wet etching, and the source/drain series resistance will be reduced. The drawback of this design is coming from the proximity effect in e-beam lithography process.

The value of the design variables for this design are summarised below in a table (Unit: nm):

For X01Y02, X11Y02 and X11Y06, the variables are shown below:

TABLE C.7: Design parameter variables for the design style (f)

Name	w	s	nw	lw	dw	pw
XX01YY01	50	50	10	2000	1000	1500
XX02YY01	50	50	20	2000	1000	1500
XX03YY01	50	50	30	2000	1000	1500
XX04YY01	50	50	40	2000	1000	1500
XX01YY02	50	50	50	2000	1000	1500
XX02YY02	50	50	100	2000	1000	1500
XX03YY02	100	100	20	2000	1000	1500
XX04YY02	100	100	30	2000	1000	1500
XX01YY03	100	100	40	2000	1000	1500
XX02YY03	100	100	50	2000	1000	1500
XX03YY03	100	100	100	2000	1000	1500
XX04YY03	150	150	20	2000	1000	1500
XX01YY04	150	150	30	2000	1000	1500
XX02YY04	150	150	40	2000	1000	1500
XX03YY04	150	150	50	2000	1000	1500
XX04YY04	150	150	100	2000	1000	1500

For X02Y02, X12Y02 and X12Y06, the variables are shown below:

TABLE C.8: Design parameter variables for the design style (f)

Name	w	s	nw	lw	dw	pw
XX01YY01	25	75	25	2000	1000	1500
XX01YY02	40	90	40	2000	1000	1500
XX01YY03	50	100	50	2000	1000	1500
XX01YY04	60	110	60	2000	1000	1500
XX02YY01	75	125	75	2000	1000	1500
XX02YY02	100	150	100	2000	1000	1500
XX02YY03	200	250	200	2000	1000	1500
XX02YY04	500	550	500	2000	1000	1500
XX03YY01	25	100	25	2000	1000	1500
XX03YY02	40	100	40	2000	1000	1500
XX03YY03	50	100	50	2000	1000	1500
XX03YY04	60	100	60	2000	1000	1500
XX04YY01	75	100	75	2000	1000	1500
XX04YY02	100	100	100	2000	1000	1500
XX04YY03	200	100	200	2000	1000	1500
XX04YY04	500	100	500	2000	1000	1500

C.1.7 Secondary Design (g): 2 First Gates

The design of metal layer is the same as design (e) and 16 devices will be fabricated in a single chip.

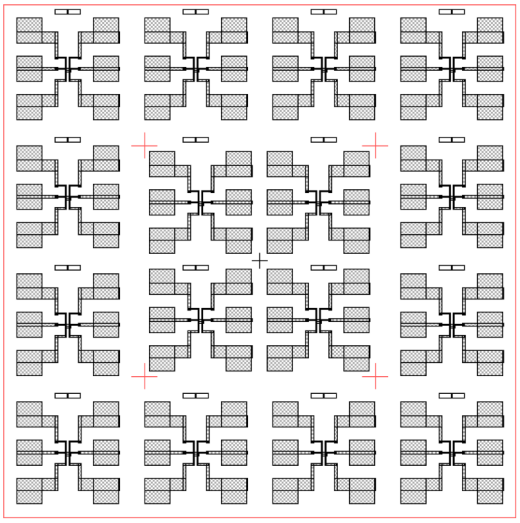

FIGURE C.20: Brief View of Design (g). This shows the metal-layer layout of the design.

The plane view of the Source/Drain area is shown in Fig. C.21, and the plane view of the active device region is shown in Fig. C.22.

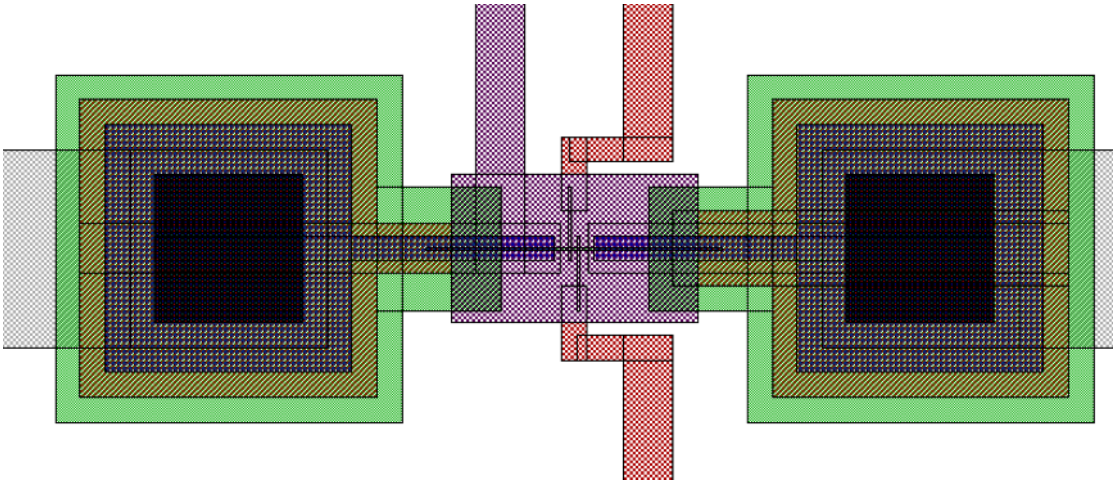

FIGURE C.21: Detailed View of Design (g). This shows the source/drain layout of the design.

The difference between design (g) and design (e) is the size of the dog-bone structure. In design (g), the dog-bone is fully removed. The advantage is that the proximity effect will be eliminated. However, long and narrow nanowire is fragile and easy to break during the fabrication process, and the series resistance will be significant for this type of design.

The value of the design variables for this design are summarised below in a table (Unit: nm):

For X01Y03, X11Y03 and X11Y07, the variables are shown below:

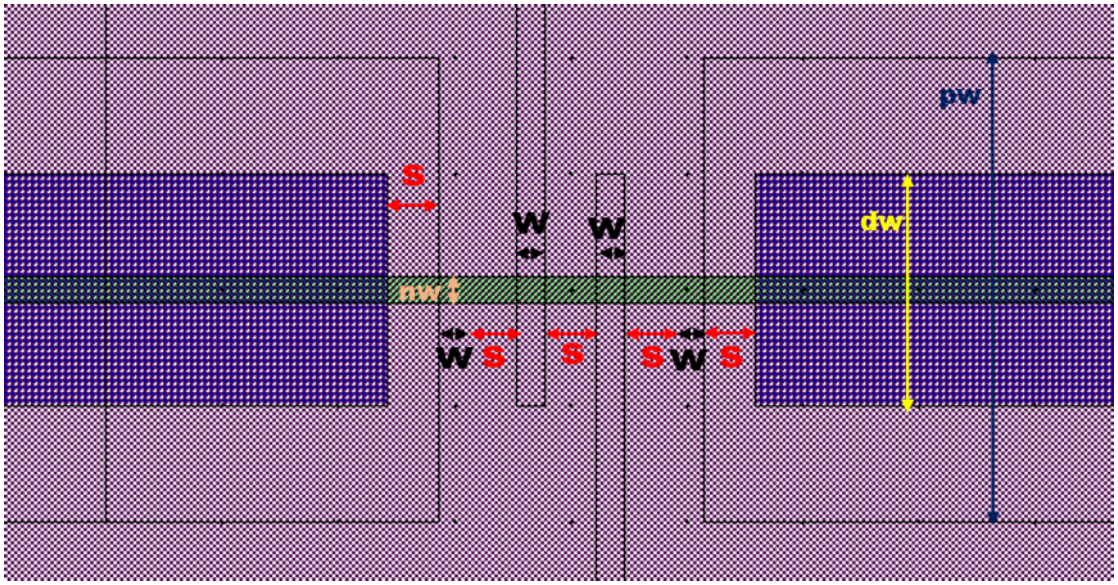

FIGURE C.22: Focusing View of Design (g). This shows the layout near the quantum dot region of the design.

TABLE C.9: Design parameter variables for the design style (g)

Name	w	s	nw	dw	pw
XX01YY01	50	50	10	500	1000
XX02YY01	50	50	20	500	1000
XX03YY01	50	50	30	500	1000
XX04YY01	50	50	40	500	1000
XX01YY02	50	50	50	500	1000
XX02YY02	50	50	100	500	1000
XX03YY02	100	100	20	500	1000
XX04YY02	100	100	30	500	1000
XX01YY03	100	100	40	500	1000
XX02YY03	100	100	50	500	1000
XX03YY03	100	100	100	500	1000
XX04YY03	150	150	20	500	1000
XX01YY04	150	150	30	500	1000
XX02YY04	150	150	40	500	1000
XX03YY04	150	150	50	500	1000
XX04YY04	150	150	100	500	1000

For X02Y03, X12Y03 and X12Y07, the variables are shown below:

TABLE C.10: Design parameter variables for the design style (g)

Name	w	s	nw	dw	pw
XX01YY01	25	75	25	500	1000
XX01YY02	40	90	40	500	1000
XX01YY03	50	100	50	500	1000
XX01YY04	60	110	60	500	1000
XX02YY01	75	125	75	500	1000
XX02YY02	100	150	100	500	1000
XX02YY03	200	250	200	500	1000
XX02YY04	500	550	500	500	1000
XX03YY01	25	100	25	500	1000
XX03YY02	40	100	40	500	1000
XX03YY03	50	100	50	500	1000
XX03YY04	60	100	60	500	1000
XX04YY01	75	100	75	500	1000
XX04YY02	100	100	100	500	1000
XX04YY03	200	100	200	500	1000
XX04YY04	500	100	500	500	1000

C.1.8 Secondary Design (h): 2 First Gates

The design of metal layer is the same as design (e) and 16 devices will be fabricated in a single chip.

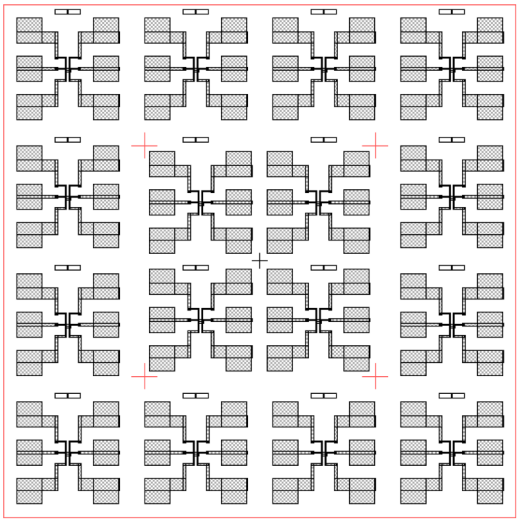

FIGURE C.23: Brief View of Design (h). This shows the metal-layer layout of the design.

The plane view of the Source/Drain area is shown in Fig. C.24, and the plane view of the active device region is shown in Fig. C.25.

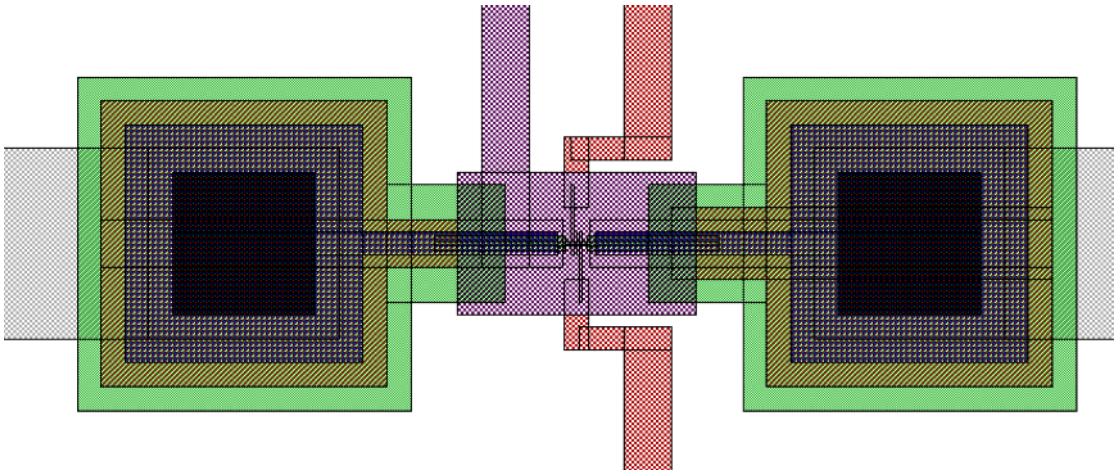

FIGURE C.24: Detailed View of Design (h). This shows the source/drain layout of the design.

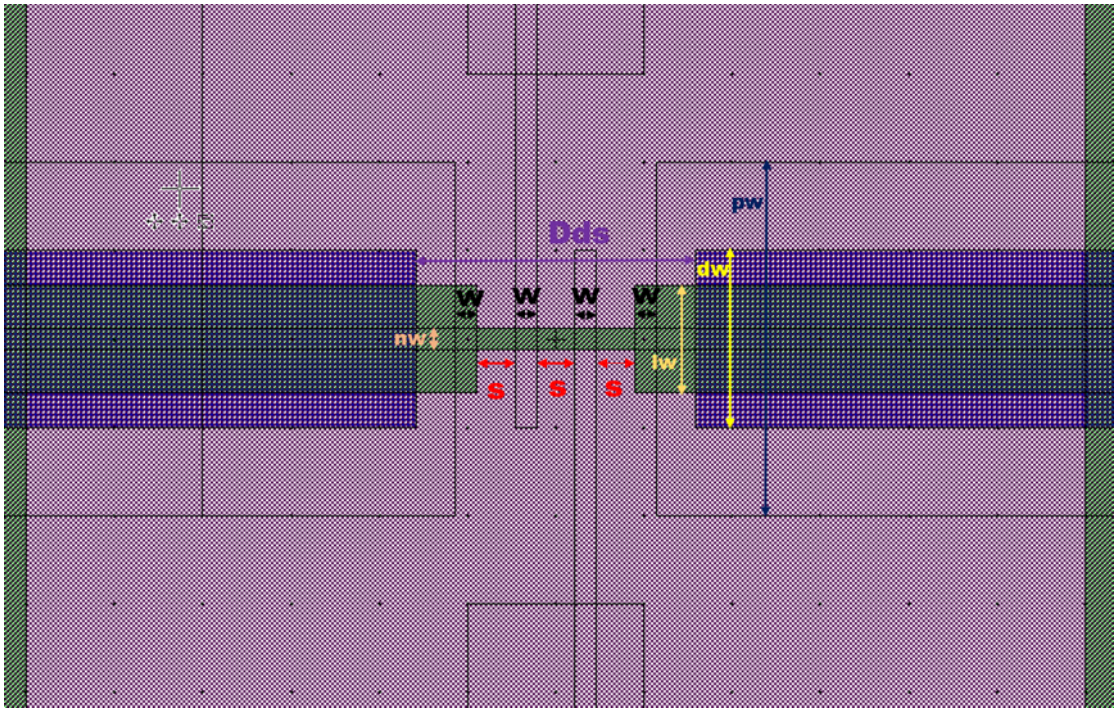

FIGURE C.25: Focusing View of Design (h). This shows the layout near the quantum dot region of the design.

In this design, the distance between the dopant diffusion layer in left and right part is kept at a fixed value. As a result, for the device with small scale, the lateral distance between the doping area and the gate area, which gives more margin of thermal budget. For the device with larger dimension, the dopant layer would be closer to the gate region. The purpose of this design is to estimate the actual dopant diffusion length.

The value of the design variables for this design are summarised below in a table (Unit: nm):

For X01Y04, X11Y04 and X11Y08, the variables are shown below:

TABLE C.11: Design parameter variables for the design style (h)

Name	w	s	nw	lw	dw	pw	Dds
XX01YY01	50	50	10	300	500	1000	1000
XX02YY01	50	50	20	300	500	1000	1000
XX03YY01	50	50	30	300	500	1000	1000
XX04YY01	50	50	40	300	500	1000	1000
XX01YY02	50	50	50	300	500	1000	1000
XX02YY02	50	50	100	300	500	1000	1000
XX03YY02	100	100	20	300	500	1000	1000
XX04YY02	100	100	30	300	500	1000	1000
XX01YY03	100	100	40	300	500	1000	1000
XX02YY03	100	100	50	300	500	1000	1000
XX03YY03	100	100	100	300	500	1000	1000
XX04YY03	150	150	20	300	500	1000	1000
XX01YY04	150	150	30	300	500	1000	1000
XX02YY04	150	150	40	300	500	1000	1000
XX03YY04	150	150	50	300	500	1000	1000
XX04YY04	150	150	100	300	500	1000	1000

For X02Y04, X12Y04 and X12Y08, the variables are shown below:

TABLE C.12: Design parameter variables for the design style (h)

Name	w	s	nw	lw	dw	pw	Dds
XX01YY01	25	75	25	300	500	1000	1000
XX01YY02	40	90	40	300	500	1000	1000
XX01YY03	50	100	50	300	500	1000	1000
XX01YY04	60	110	60	300	500	1000	1000
XX02YY01	75	125	75	300	500	1000	1000
XX02YY02	100	150	100	300	500	1000	1000
XX02YY03	200	250	200	300	500	1000	1000
XX02YY04	500	550	500	300	500	1000	1000
XX03YY01	25	100	25	300	500	1000	1000
XX03YY02	40	100	40	300	500	1000	1000
XX03YY03	50	100	50	300	500	1000	1000
XX03YY04	60	100	60	300	500	1000	1000
XX04YY01	75	100	75	300	500	1000	1000
XX04YY02	100	100	100	300	500	1000	1000
XX04YY03	200	100	200	300	500	1000	1000
XX04YY04	500	100	500	300	500	1000	1000

Appendix D

Publication List

D.1 Journal Publication: As first author

Li, Z., Husain, M.K., Yoshimoto, H., Tani, K., Sasago, Y., Hisamoto, D., Fletcher, J.D., Kataoka, M., Tsuchiya, Y. and Saito, S., 2017. Single carrier trapping and de-trapping in scaled silicon complementary metal-oxide-semiconductor field-effect transistors at low temperatures. Semiconductor Science and Technology, 32(7), p.075001.

Li, Z., Sotto, M., Liu, F., Husain, M.K., Yoshimoto, H., Sasago, Y., Hisamoto, D., Tomita, I., Tsuchiya, Y. and Saito, S., 2018. Random telegraph noise from resonant tunnelling at low temperatures. Scientific reports, 8(1), p.250.

D.2 International Conference Publication: As first author

Li, Z., Sotto, M., Liu, F., Husain, M.K., Zeimpekis, I., Yoshimoto, H., Tani, K., Sasago, Y., Hisamoto, D., Fletcher, J.D. and Kataoka, M., 2017, February. Random-telegraph-noise by resonant tunnelling at low temperatures. In Electron Devices Technology and Manufacturing Conference (EDTM), 2017 IEEE (pp. 172-174). IEEE.

D.3 Journal Publication: As other authors

Burt, D., Al-Attili, A., Li, Z., Gards, F., Sotto, M., Higashitarumizu, N., Ishikawa, Y., Oda, K., Querin, O.M., Saito, S. and Kelsall, R., 2017. Enhanced light emission from improved homogeneity in biaxially suspended Germanium membranes from curvature optimization. Optics express, 25(19), pp.22911-22922.

D.4 International Conference Publication: As other authors

Burt, D., Al-Attili, A.Z., Li, Z., Liu, F., Oda, K., Higashitarumizu, N., Ishikawa, Y., Querin, O.M., Gardes, F., Kelsall, R.W. and Saito, S., 2017, February. Strain-engineering in Germanium membranes towards light sources on Silicon. In Electron Devices Technology and Manufacturing Conference (EDTM), 2017 IEEE (pp. 92-94). IEEE.

Liu, F., Husain, M.K., Li, Z., Sotto, M.S.H., Burt, D., Fletcher, J.D., Kataoka, M., Tsuchiya, Y. and Saito, S., 2017, February. Transport properties in silicon nanowire transistors with atomically flat interfaces. In Electron Devices Technology and Manufacturing Conference (EDTM), 2017 IEEE (pp. 193-195). IEEE.

Sotto, M., Henri, S., Debnath, K., Husain, M., Li, Z., Liu, F., Khokhar, A. and Saito, S., 2017. Transversal symmetry breaking in novel photonic crystal waveguide: innovative manner to master defect band dispersion relation. SSDM 2017.

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