Cost-Effective 3D Integration using Inductive Coupling Links

Can we make stacking silicon as easy as stacking Lego?

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MOTIVATION & BACKGROUND

The Internet of Things requires a new breed of heterogenous integrated circuits that incorporate a range of disparate elements from MEMS and analogue communications to low power digital processing and non-volatile memories [1]. Each of these devices operate in different voltage domains, and require disparate fabrication materials, flows, and techniques. Additionally, Internet of Things devices must be manufacturable with extremely **low costs** providing a significant challenge from a system integration perspective.

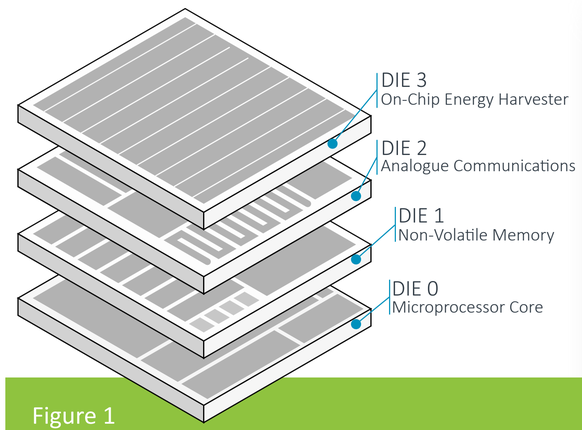


Figure 1
Illustration of a heterogeneous 3D-IC for IoT applications.

The Internet of Things requires devices that:

- Incorporate technological heterogeneity
- Consume little power
- Have small form-factors
- Are low cost
- Are easy to fabricate and assemble
- Are quick to develop (short time to market)

CHALLENGES WITH EXISTING APPROACHES

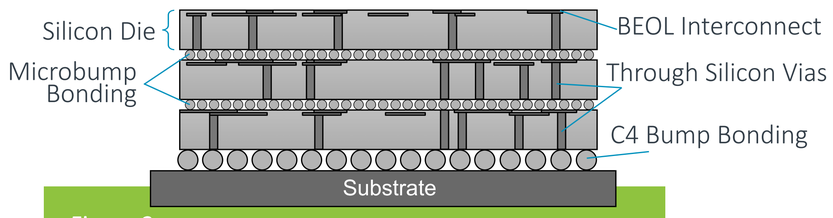


Figure 2
Illustration of 3D integration using TSVs.

To achieve 3D integration, the research community typically looks to the use of through silicon vias (TSVs). These are metallic pathways that are etched entirely through the silicon substrate to allow face-to-back die stacking.

Through silicon vias allow high density vertical connectivity between tiers, however typically demand high fabrication costs, and suffer from low reliability [2]. In addition to this, the number of CAD tools supporting 3D design using TSVs is, presently, very limited and hence 3D-ICs (particularly heterogenous stacks) have long development cycles.

TSVs allow fabrication of 3D-ICs that:

- ✓ Incorporate technological heterogeneity
- ✓ Consume little power
- ✓ Have small form-factors
- ✗ Are low cost
  ...they require specialised fabrication processes
- ✗ Are easy to fabricate and assemble
  ...they need precise (sub-micron) die stacking alignment
- ✗ Are quick to develop (short time to market)
  ...they are unsupported by many CAD tools

COIL-3D

A CAD tool for the Optimisation of Inductive Links in 3D-ICs
coil3d.ecs.soton.ac.uk

In the IoT domain, short design cycles are important and so this research aims to establish a simple design flow for realising standardised ICL interfaces between stacked dies. For high power-efficiency, optimisation of the physical inductors is essential, however typically requires the use of finite element analysis (FEA) in a process that can take several hours. As a result, the generation of optimised inductor designs poses a significant challenge.

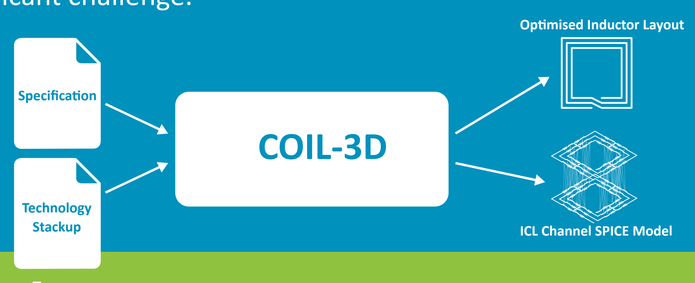


Figure 5
Top-level view of the ooperation of the COIL-3D CAD tool.

To address this challenge, we have developed a CAD tool, COIL-3D [3] that uses a rapid solver to quickly and accurately optimise a given link. The proposed solver achieves an average accuracy within 9.1% of commercial FEA software tools, and the COIL-3D optimisation flow reduces the search time by 26 orders of magnitude.

3D INTEGRATION USING INDUCTIVE COUPLING

This research explores using **Inductive Coupling Links (ICLs)** as a cost-effective alternative to TSVs for 3D integration.

ICLs address many of these challenges:

- ✓ Incorporate technological heterogeneity
- ✓ Consume little power
- ✓ Have small form-factors
- ✓ Are low cost
  ...existing processes can be used without alteration
- ✓ Are easy to fabricate and assemble
  ...their wireless nature means that 'precise' stacking is not required
- ✓ Are quick to develop (short time to market)
  ...they can be designed in a standardised way using existing CAD tools

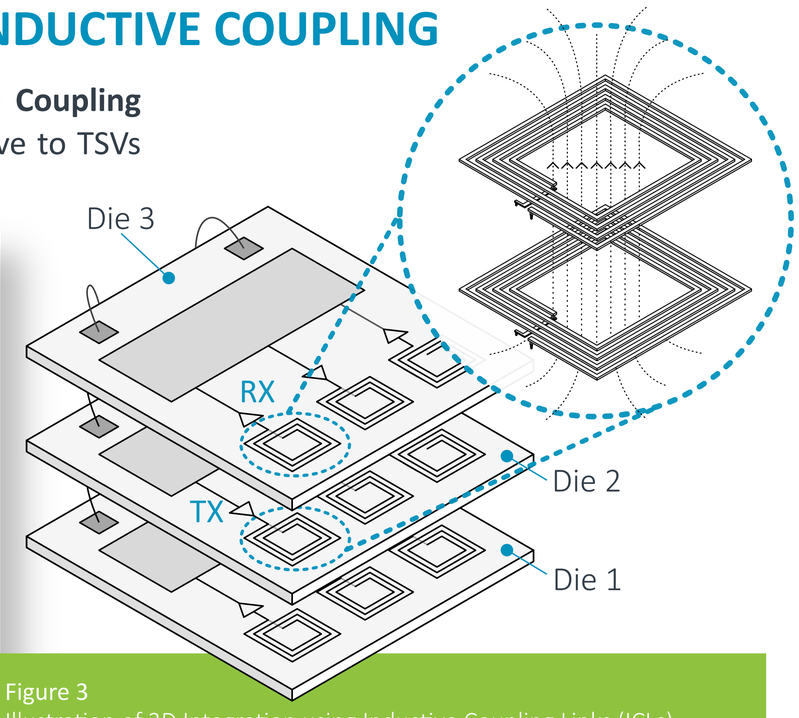


Figure 3
Illustration of 3D Integration using Inductive Coupling Links (ICLs).

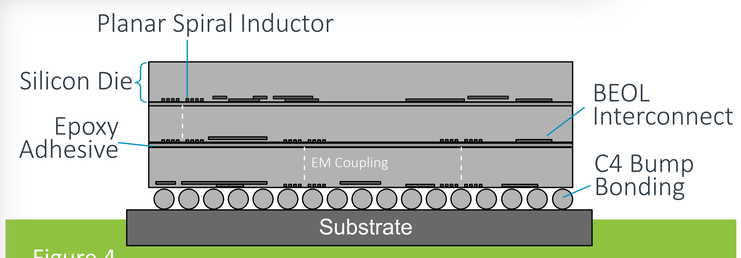
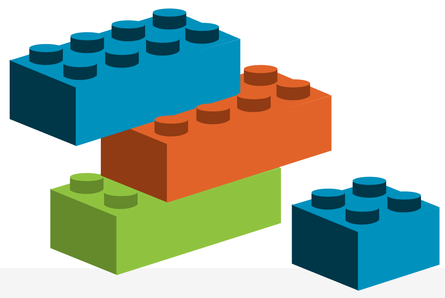


Figure 4
Illustration of 3D Integration using Inductive Coupling Links (ICLs).

In ICLs, data is encoded in a series of current pulses that are fed through planar inductors in the BEOL interconnect layers of each die. These pulses form a magnetic field, which is intersected in adjacent dies. This induces a corresponding current that can be used to recover the transmitted data.

ICLs allow **easy stacking**, **low-cost fabrication** and **short development cycles** (as they can be designed using existing CAD tools and flows). They also boast **broad compatibility**; as inductive links do not require any physical modifications to the stacked tiers, there are no challenges regarding inter-tier compatibility (unlike via-last TSVs which can only be fabricated in technologies agreeable to their formation temperatures). When incorporated into a standardised interface, ICLs offer 3D integration with no post-fabrication processing, making stacking silicon as easy as stacking Lego.



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