Silicon slot fin waveguide on bonded double-SOI for low-power accumulation modulator fabricated by anisotropic wet etching technique

JAMES BYERS,[1] KAPIL DEBNATH,[2] HIDEO ARIMOTO,[1] M. KHALED HUSAIN,[1] MOISE SOTTO,[1] ZUO LI,[1] FAYONG LIU,[1] KOUTA IBUKURO,[1] ALI KHOKHAR,[3] KIAN KIANG,[1] STUART A. BODEN,[1] DAVID J. THOMSON,[3] GRAHAM T. REED[3] AND SHINICHI SAITO[1,*]

[1]*Department of Electronics and Computer Science, University of Southampton, Southampton, SO 17 1BJ, UK*
[2]*Electronics & Electrical Communication Engineering, Indian Institute of Technology, Kharagpur, West Bengal 721302, India*
[3]*Optoelectronics Research Centre, University of Southampton, Southampton SO17 1JB, UK*
[*]*S.Saito@soton.ac.uk*

Abstract: We propose a new low $V_\pi L$, fully-crystalline, accumulation modulator design based on a thin horizontal gate oxide slot fin waveguide, on bonded double Silicon-on-Insulator (SOI). A combination of anisotropic wet etching and the mirrored crystal alignment of the top and bottom SOI layers allows us for the first time to selectively pattern the bottom layer from above. Simulations presented herein show a $V_\pi L = 0.17$Vcm. Fin-waveguides and passive Mach-Zehnder Interferometer (MZI) devices with fin-waveguide phase shifters have been fabricated, with the fin-waveguides having a transmission loss of 5.8dB/mm and a 13.5nm thick internal gate oxide slot.

1. Introduction

Silicon photonics technology [1] provides one of the most promising solutions to the problem of what is to replace short-range metal interconnects as the requirements of chip-to-chip and board-to-board communication increase [2–4]. Some of the best silicon photonic optoelectronic (OE) modulators [5] reported in academia and industry are plasma dispersion effect (PDE) accumulation modulators [6–9] fabricated on an SOI substrate. Waveguides fabricated on SOI [10–12] benefit from the high refractive index difference (Δn=2.1) [13] between crystalline-Si (c-Si) and the buried oxide (BOX, SiO_2), which facilitates very high mode confinement in sub-micron waveguides [14], maximizing the light-matter interaction between the guided mode and free carriers for PDE phase change modulation. However, this high refractive index difference leads to high scattering induced optical loss as a consequence of fabrication induced sidewall roughness (and the associated refractive index variation), as loss scales proportionally to $(\Delta n)^3$ [13, 15]. Waveguide sidewall roughness is therefore a major source of optical loss [16]. A proposed solution to reduce sidewall roughness is to use local-oxidation-of-silicon (LOCOS) and tetramethylammonium hydroxide (TMAH) anisotropic wet etching of waveguides aligned to the (111) crystal plane of Si to produce atomically flat waveguide sidewalls [8, 17, 18].

Horizontal gate oxide accumulation modulators usually rely on either partially amorphous-Si (a-Si) [19] or polycrystalline-Si (poly-Si) [7] waveguides, which suffer from grain boundary induced optical loss, as well as non-optimal electrical characteristics compared to c-Si. A vertical gate-oxide accumulation modulator with fully c-Si slot waveguides has been demonstrated [9], although this requires a complex fabrication process to recover the crystal structure of deposited

a-Si [20, 21]. A high-speed, fully-crystalline, bonded double-SOI accumulation modulator has been presented [22], however the authors state that the device speed can be increased by a factor of 2.4, and the power consumption decreased by a factor of 2, by eliminating the parasitic capacitance between the top and bottom SOI in the non-active region.

Several results have been presented of high-speed (up to 56Gb/s [23]) reverse biased pin-diode injection modulators which utilize doped periodic fin electrical contacts perpendicular to the central strip waveguide [23–27]. One major benefit of using periodic fin electrical contacts as opposed to a thin SOI planar contact (common in conventional strip/rib waveguides) is the ability to dry etch completely to the stopping BOX layer instead of relying on partial etching through the SOI layer with no well defined stopping layer, which leads to local and macro-scale fabrication variations and reduces overall yield. Fin parameters can be optimized as per the device requirements, with narrow fins exhibiting lower optical loss at the cost of higher resistance (therefore higher $V_\pi L$), and vice versa for wide fins.

The key challenge associated with developing a fully-crystalline, horizontal slot, low $V_\pi L$ accumulation modulator is the problem of how to pattern the bottom SOI of a double-SOI substrate post-bonding (patterning cannot be done pre-bonding, as this would lead to intolerable surface contaminations/defects/imperfections which would seriously degrade the horizontal gate oxide bonding quality), to achieve a fully-crystalline version of the a-Si horizontal slot accumulation modulator. If the bottom SOI is not removed, this leads to parasitic capacitance (increasing power consumption) and restricts the device architecture to microdisk or microring resonators, as the active region cannot accommodate a waveguide required for MZI phase shifters. In this work we propose and demonstrate a new fabrication technique which involves anisotropic wet etching of mirror aligned top and bottom SOI planes which for the first time successfully overcomes this key challenge. We demonstrate the feasibility of this technique by fabricating and characterizing fully passive, undoped, fin waveguide devices and fin waveguide MZI devices. The paper is organized as follows. In Section 2, we introduce and discuss the new device design and the figures of merit achievable according to simulation. In Section 3.1, we outline the new fabrication process required to realize the new device design, and outline the fabrication plan. In Section 3.2, we detail the fabrication of bonded metal-oxide-semiconductor (MOS) capacitor devices (to characterise bonding quality) and in section 3.3 we detail the successful fabrication of anisotropically wet etched passive fin-waveguides on bonded double-SOI. In Section 4 we present and discuss the characterisation results of the devices (MOS capacitor, strip/fin-waveguides, passive MZIs) outlined in Section 3.

2. Design & simulation

The horizontal gate oxide slot, fin-waveguide MZI accumulation modulator was designed on a double-SOI platform. A schematic of the phase shifter section of the device is presented in Fig. 1. The entire substrate consists of two (110) 100nm SOI layers, separated by a 10nm SiO_2 oxide layer. The orientation of the stable (111) planes of the upper and lower SOIs are mirrored (Fig. 1(A)). The central strip-waveguide is defined so the sidewalls align parallel to the stable (111) plane of both the upper and lower SOIs. The sidewalls of the upper fins (left in Fig. 1(A) schematic) are defined parallel to the stable (11-1) plane of the upper SOI. The sidewalls of the lower fins (right in Fig. 1(A) schematic) are defined parallel to the stable (11-1) plane of the lower SOI.

The MZI is a conventional design, with a 1-dimensional grating coupler input to a strip (with 10nm slot) waveguide. The strip waveguide enters a 2x1 multimode interferometer (MMI), and each output strip waveguide then undergoes two 90° bends (radius = 20μm) before coupling into the active phase shifter fin-waveguide region. On the other side of the phase shifter region the structure is exactly symmetrical. The arm length difference, ΔL_{arm}, allows the device to operate at a sub-π phase shift.

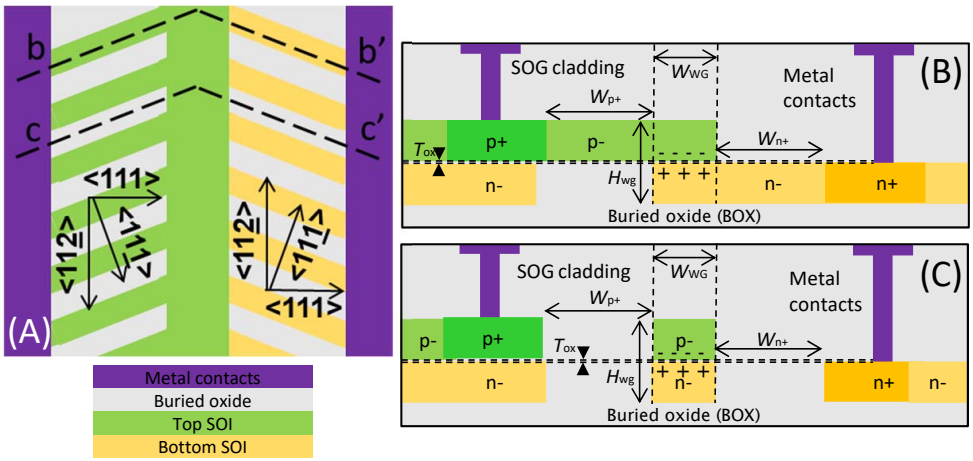

Fig. 1. (A) Top view schematic of the active phase shifter fin-waveguide region. Relevant stable (111) planes of the upper SOI and lower SOI layers are overlaid over the left (green) and right (yellow) fins respectively. (B) cross-section b–b' depicting alternating 3D section of the structure; (C) cross-section c–c' depicting conventional strip waveguide.

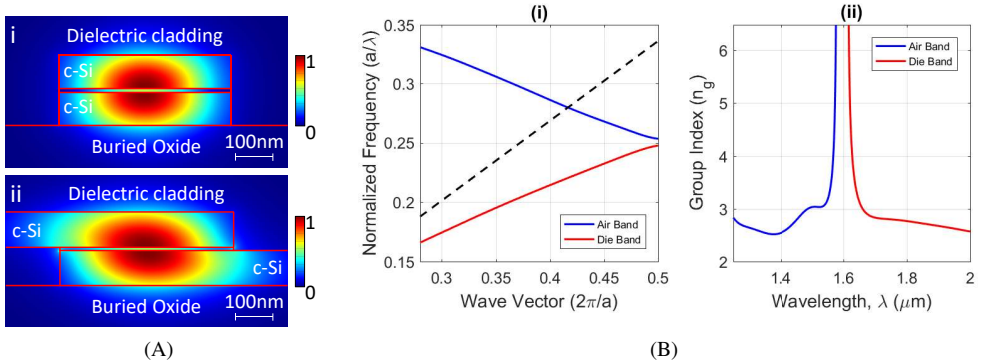

Fig. 2. Fin simulation results.(A) Normalized fundamental TE mode profile (energy density) for (i) double-SOI strip waveguide and (ii) double-SOI fin-waveguide. Waveguide thickness (T_{wg}) is 210nm, gate oxide layer is 10nm, waveguide width (w_{wg}) is 450nm. Fin thickness (T_{fin}) is 100nm, fin length is (1μm). Mode profile in fins is negligible above 200nm away from the central WG. (B) LUMERICAL simulations for fin waveguide design #4 showing (i) the normalized frequency (a/λ) bandgap diagram and (ii) the group index (n_g) (which tends to infinity at the bandgap) as a function of wavelength.

Mode profile simulations (Fig. 2) performed using commercial software LUMERICAL demonstrate that a single TE mode exists for both the strip-waveguide (Fig. 2(A)i) and the fin-waveguide (Fig. 2(A)ii). The mode for both structures is concentrated around the central region of the gate oxide, where the change in free carrier concentration would be greatest in an active modulator utilizing this design, with the mode profile concentration negligible at over 200nm into the fins.

The fins act primarily as electrical contacts either side of the gate oxide in an active modulator device, but since their placement along the strip-waveguide is periodic, they can also be designed to act as a pseudo 1-dimensional photonic crystal if desired. We have included several fin parameter designs (varying fin period (P_{fin}) and fin width (W_{fin}), shown in Table 1, one of which

exhibits a 42nm photonic bandgap between wavelengths 1576nm-1618nm. FDTD simulations performed using LUMERICAL show the normalized frequency bandgap diagram as a function of the wave vector ($2\pi/a$) for the air band and the die band (Fig. 2(B)i) and that the group index (n_g) of guided light tends to infinity at the band edge (Fig. 2(B)ii), again demonstrating the bandgap. This fin design (or an optimized version) could be used to operate the device in the slow light regime, however, if maximizing optical bandwidth and reducing optical loss was desired, a fin design that does not exhibit a photonic bandgap near the operational wavelength would be chosen. The latter category (no photonic bandgap) is the category that this work is primarily targeting.

Table 1. Fin Design Parameters

Design #	Fin width (nm)	Fin period (nm)
1	100	300
2	125	250
3	150	300
4	200	400

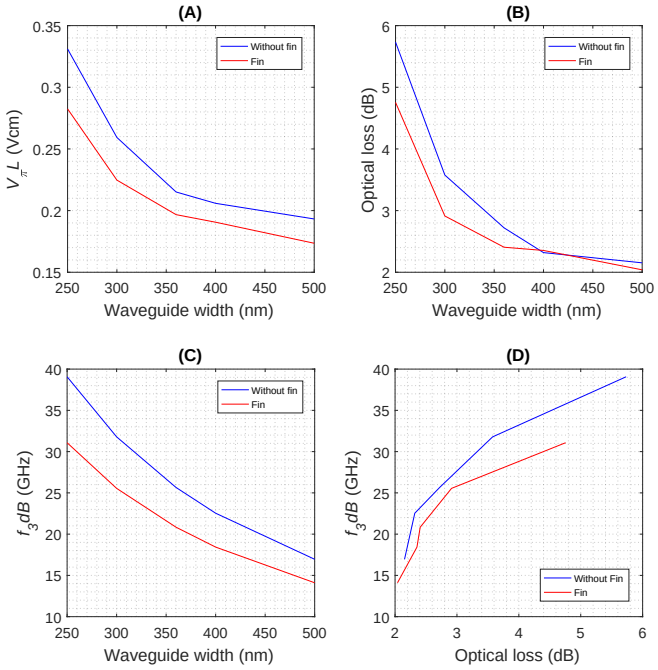

Fig. 3. Simulation results for MZI accumulation modulator (described in text) with an without fin structure. (A) $V_\pi L$ as a function of waveguide width. Fin structure showing 17.4% improvement over the non-fin structure at 250nm waveguide width and a 11.4% improvement at 500nm waveguide width. (B) Optical loss as a function of waveguide width, showing lower fin loss at narrower waveguide widths. (C) f_{3dB} as a function of waveguide width showing lower f_{3dB} for the fin waveguide design. (D) f_{3dB} as a function of optical loss.

LUMERICAL (DEVICE) simulations (results presented in Fig. 3) have been carried out

which show this modulator design is capable of achieving a lower figure of merit, $V_\pi L$, or higher 3dB bandwidth (f_{3dB}) than conventional horizontal slot accumulation modulators [28]. Figure 3 shows the results for fin-waveguide MZI accumulation modulators with fin width 160nm, fin period 214nm, as well as non-fin horizontal-slot waveguide MZI accumulation modulators for reference. The simulations were performed assuming a small AC signal of 0.001V with frequency 1000Hz, and bias voltage = 0 - +4V, at wavelength = 1310nm (although proposed device could be operated at wavelength = 1550nm if desired). The assumed length of the MZI arms is 500μm, with n-/p- doping concentration = $1.5\text{x}10^{18}$ and n+/p+ contact doping = $2\text{x}10^{20}$. The simulations take into account free carrier absorption optical loss but not surface roughness induced optical loss or coupling losses, which can be optimized separately. The "Without fin" simulations refer to simulations where the top crystalline SOI layer used as a contact was an unetched slab (similar to the already demonstrated a-Si SISCAP modulator [28]). This device is obviously impossible to fabricate using our proposed method (or any method that the authors are aware of) and is only included as a reference. Where optical confinement is highest, and loss lowest, at waveguide width 500nm, $V_\pi L$ is improved by 11.7% and optical loss improved by 5% (0.4dB). The slight decrease in f_{3dB} is due to the increased resistance caused by the fins. Depending on the required application, design parameters can be turned to achieve either $V_\pi L$=0.28Vcm, loss = 4.8dB, f_{3dB}=32GHz or $V_\pi L$=0.17Vcm, loss = 2dB, f_{3dB}=15GHz. The improved $V_\pi L$ can be attributed to the increased optical confinement in the active region of the waveguide caused by the fins as opposed to a slab structure. These simulations also show that the introduction of a fin contact structure (required to underetch the top-SOI) does not limit the modulator performance compared to using a top-SOI slab.

3. Fabrication

3.1. Fabrication outline

Here we address the problem of how to under and over-etch the top and bottom fins respectively, to realise the design presented.The double-SOI must be bonded prior to patterning, to maintain pristine SiO_2/SiO_2 interface bonding quality. The solution proposed and demonstrated herein (detail provided in section 3.3), is to use (110) SOI wafers, which, once directly bonded with a thin intermediate gate oxide layer, exhibit mirrored (111) crystal alignment between the top and bottom SOI layers (as shown in Fig. 4(E)). For structures with sidewalls aligned to the top SOI (111) crystal plane, the top half of the structure will be protected from TMAH etching by this (111) crystal plane, whereas the bottom half of the structure (separated by the thin bonding oxide layer) will not be protected by the (111) crystal plane, and will be etched, and vice versa for structures with sidewalls aligned to the bottom SOI (111) crystal plane.

Section 3.2 details the MOS-capacitor fabrication to demonstrate the oxide bonding quality. Section 3.3 then details the fin-waveguide fabrication, including the anisotropic wet etch step required to realise the over/underetching simultaneously.

3.2. MOS-capacitor fabrication

MOS capacitor devices were fabricated on directly bonded bulk (100) Si wafers (whose surface chemistry is the same as that of (110) Si wafers in regards to direct oxide bonding, as the actual bonding occurs between SiO_2-SiO_2) with a 10nm bonding SiO_2 layer to establish bonding quality. This bonding process follows a similar process to the one outlined by H. Moradinejad [29] and M. Sodagar [22]. First, p- and n- doped bulk Si wafers were thermally oxidized with 8.5nm SiO_2. Then, they underwent pre-bonding activation by immersion in 1:200 buffered HF and were then rinsed with deionized water. This served the double purpose of saturating the surface with dangling –OH bonds [30], increasing surface adhesion upon SiO_2/SiO_2 contact, and thinning the SiO_2, targeting 10nm final bonding oxide. The wafers were then immediately placed in direct

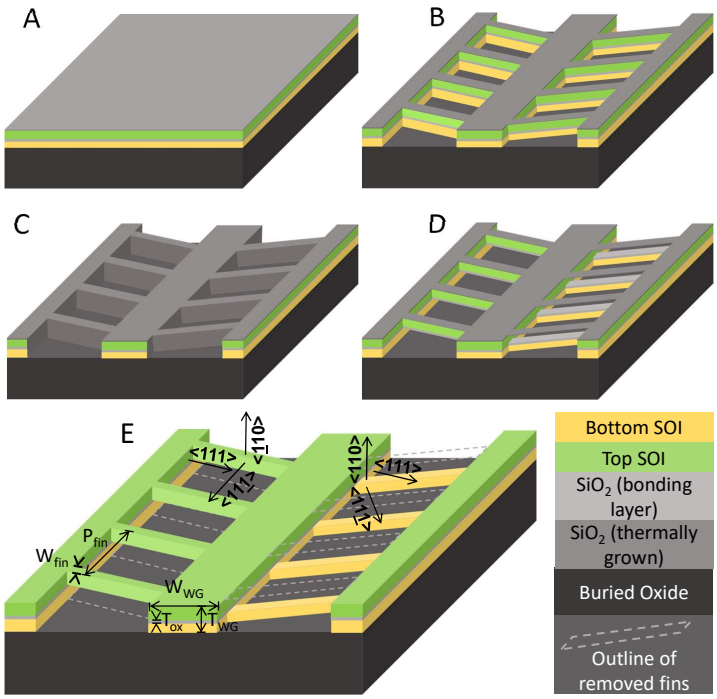

Fig. 4. Fin waveguide simplified fabrication process flow: (A) Bonded double-SOI substrate (with thin 10nm gate oxide intermediate layer), with thermally grown oxide (22nm) on top. Top and bottom (110) SOI layers have mirrored crystal orientation; (B) Fin and strip waveguides patterned using electron beam lithography and dry etched; (C) Thermal oxide (7.5nm on (111) sidewalls) grown to reduce sidewall roughness; (D) Sidewall oxide removed using HF and TMAH applied for 105minutes to etch non-(111) plane Si. Left bottom fins etched whilst left top fins protected by the (111) sidewall, vice versa with the right fins; (E) Exposed oxide removed using HF. Dielectric protective layer (PMMA) applied.

contact and manually bonded by applying minimal force to the top wafer, and annealed at 1000°C for 3 hours. The bonded wafers were then immersed in HF to remove the native oxide from the back of both wafers, and a 100nm Al layer was deposited on both sides. The wafer was then cleaved into chips and measured.

3.3. 3D fin waveguide fabrication

Similarly, we have fabricated fin and strip waveguides with an internal horizontal gate oxide layer (10nm) on bonded double-SOI. Two undoped (110) SOI (330nm SOI, 2µm BOX) wafers were thinned down using thermal oxidation and HF wet etching to SOI = 114.6nm, 98.6nm (the top SOI layer would be thinned down through several thermal oxidation steps to 100nm during waveguide fabrication). Undoped wafers were chosen for two reasons. Firstly, it is desirable to limit pre-bonding processing steps as much as possible, to maintain the highest wafer surface quality possible for bonding. Secondly, doped wafers would lead to unnecessary optical loss via free carrier absorption in non-active areas of an active device (e.g. tapers, MMIs, bends etc.).An additional loss of 4dB would be expected if we consider a device with a total waveguide length of 1mm (excluding phase shifter sections) and a dopant concentration of 1.5^{18}. The SOI wafers were then bonded using a similar process to that outlined above for the MOS capacitor devices. 8nm SiO_2 was grown using thermal oxidation, thinning the SOIs to 110nm, 95nm. The wafers were immersed in 1:200 HF, thinning SiO_2 to 5nm, then rinsed in deionized water, dried

using N_2 and immediately placed in direct contact. Due to the later anisotropic wet etch step, it is crucial to maintain the greatest wafer to wafer alignment possible. The two wafers were aligned flat to flat without the use of any high-precision tool. Our estimate for the wafer to wafer angular misalignment is between 0-1° (the effect of this misalignment is discussed below in relation to completed wet etched structures). The bonded wafer was annealed at low temperature (450°C) under applied force of 5kN in vacuum for 2 hours using an EVG520 Wafer-Bonding machine, followed by a high temperature (1000°C) anneal in atmospheric conditions for 3 hours. The back 2µm BOX was removed using HF. Inductively coupled plasma (ICP) dry etching was used to thin the 675µm handle layer to 120µm over 120 min etch time (4.6µm/min Si etch rate). At this point the wafer had to be cleaved into 3x4cm chips for the sake of the ICP tool. The wafer was diced (protective resist was applied, the wafer was diced and the resist was stripped and the wafer cleaned using N-Methyl-2-pyrrolidone (NMP), isopropanol (IPA) and fuming nitric acid (FNA)) and a further 25 min ICP etching was applied until the entire Si handle layer was removed. After the sample was cleaned using acetone (ACE) and IPA, the top BOX was removed using HF 7:1, realizing the bonded double-SOI wafer with a substrate stack: BOX(2 µm)/Si(100nm)/SiO_2(10nm)/Si(110nm).

The fin waveguide fabrication process is outlined schematically in Fig. 4. A protective 22nm SiO_2 was grown using thermal oxidation (Fig. 4(A)). Positive resist (ZEP) was applied and all sections of the device (fin waveguides, strip waveguides, passive MZI device etc.) except grating couplers were patterned using electron-beam lithography and dry etched using ICP (CHF_3 and SF_6 chemistry). The bottom BOX layer was used as an etch stopping layer. Strip waveguides were designed to align parallel to the (111) crystal plane orientation. The sample was then stripped of resist, cleaned, ZEP was reapplied and the grating couplers were patterned using electron-beam lithography. The grating couplers were ICP etched, using the 10nm bonding oxide layer as an etch stopping layer. The sample was cleaned again and then thermally oxidised, growing 7.5nm SiO_2 on the (111) fin and strip waveguide sidewalls. Positive resist (PMMA) was applied. Etching windows around the fin waveguide section of the waveguides were patterned and developed, revealing rectangular windows around the fin waveguide sections of the device unprotected by PMMA.

The sample was immersed in 20:1 HF removing the sidewalls SiO_2. This was immediately followed by a DI rinse and immersion in TMAH for 20 minutes, to reduce the sidewall roughness and selectively under-etch and over-etch the fins simultaneously. TMAH etching exploits the mirrored alignment of the (111) planes of the upper and lower c-Si sections of the platform. The upper and lower sidewalls of the central strip-waveguide align to the (111) plane, which acts as a TMAH etch stop. The fins are patterned at a 20° angle to the central strip-waveguide, therefore the sidewalls of the upper SOI fins (left of the strip-waveguide in Fig. 4 schematic) align to the upper SOI (11-1) crystal plane and the sidewalls of the lower SOI fins (right of the strip-waveguide in Fig. 4 schematic) align to the lower SOI (11-1) crystal plane.The (111) c-Si planes which define the sides of the fins act as a stopping layer for TMAH etching, protecting fins and the central strip waveguide from being etching while the non-(111) planes of the other wafer either above or below the fins are completely etched. Using scanning electron microscopy (SEM), the fins were observed not to have fully over and under etched after 20 minutes of immersion in TMAH. For this reason, the previous few steps were repeated. Sidewall native oxide was removed using 20:1 HF and TMAH etching was applied for 85 minutes (105 minutes total TMAH etch time). The sample was cleaned and imaged again using SEM (Fig. 5), confirming the full under and over etching as expected, with the top fins appearing to have been fully suspended successfully. SEM images can also be used to estimate the angular misalignment of the <111> plane of the top and bottom wafers relative to the electron-beam lithography defined dry etched waveguide and fins, by measuring the difference between the expected <111> plane etch and measured <111> plane etch. The defined waveguide width = 450nm, but the measured post-wet

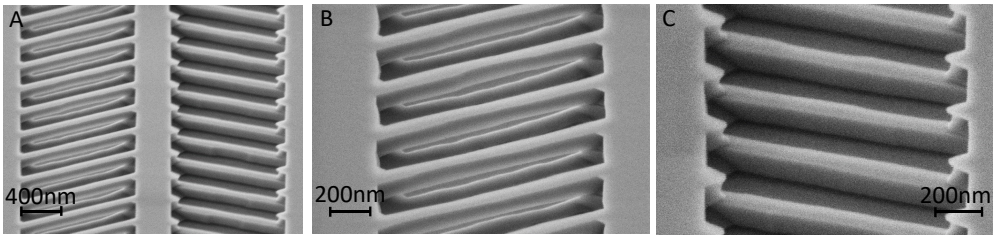

Fig. 5. SEM images of TMAH anisotropically wet etched bonded double-SOI fin waveguides, taken after SiO_2 removal, at 54° tilt to show the three dimensional nature of the over and under etched fins. (A) Overview of entire ≈ 2μm width of the waveguide; (B) Increased magnification SEM image of left (under-etched) fins, taken using "line average image stabilization", which gives the misleading impression that the waveguide is "wobbling". This is clearly not the case from the other images, however, this technique does give higher resolution and is locally accurate. This clearly shows how the left upper fins defined by the (111) crystal plane have remained un-etched, whilst the SOI beneath these fins (not protected by the (111) crystal plane barrier) has been completely etched. (C) Increased magnification SEM image of right (over-etched) fins showing that the top SOI has been completely etched.

etch width =350nm. 36nm <111> crystal plane etching per sidewall is expected based on a pre-established 0.35nm/min <111> etch rate. The remaining 14nm Si etching per sidewall can be attributed to angular misalignment. The Si <111> etch rate increases linearly as a function on angular misalignment, at approximately 0.11/1°/min). The 14nm Si etching therefore translates to 1.2° angular misalignment. Our designs are tolerant to this slight misalignment induced over-etch, however, for designs that require more precise alignment, self-aligning pre-etched alignment mark patterns could be used [31]. A 1.8μm dielectric cladding layer (PMMA was used, n=1.48) was applied and the devices were measured.

4. Characterization

4.1. Bonding oxide quality

Capacitance-Voltage (C–V) measurements (operating parameters: 30Mv AC, 10kHz) were taken for the bulk Si MOS capacitor device (Fig. 6), showing typical, expected C–V behavior (confirming bonding gate oxide quality sufficient for electronic components) and confirming the effective oxide thickness, t_{ox} = 13.5nm.

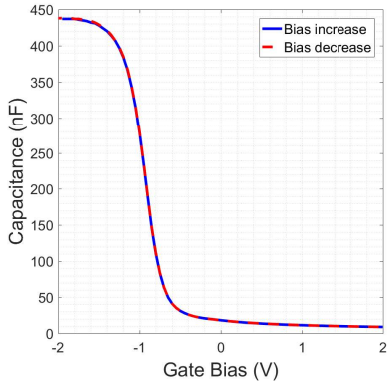

Fig. 6. C–V curve of bonded MOS capacitor device demonstrating ideal MOS capacitor behavior and capacitance relating to t_{ox}= 13.5nm. This demonstrates the high quality of the bonding oxide layer.

4.2. *Fin and strip waveguide quality*

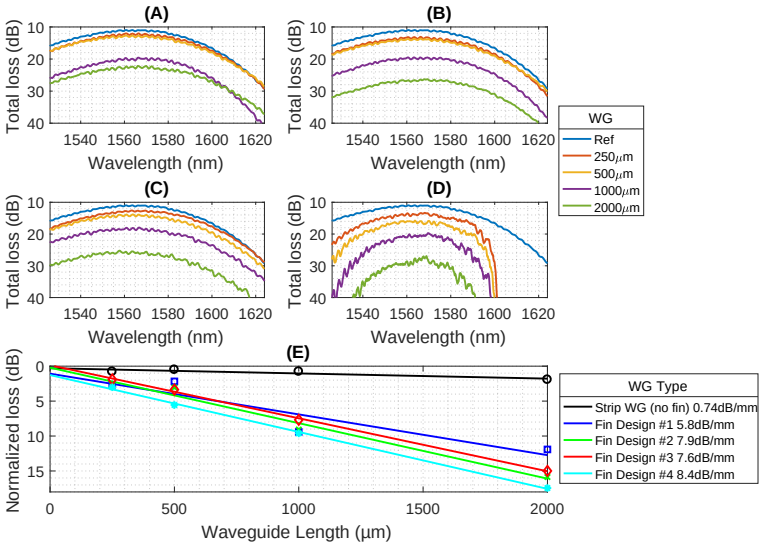

Fig. 7. A-D: Total transmission loss as a function of wavelength (nm) for each fin design #1, #2, #3, #4 respectively, and for each L_{wg}. Each presented result is an average of three identical devices, after the transmission loss of each device has individually been corrected to remove Fabry-Perot resonance caused by the grating couplers. The "Ref" result is the expected transmission loss for a 0µm long waveguide (input grating coupler input and output taper, and output grating coupler), extrapolated from 12 strip waveguides of L_{wg}=250µm–2000µm. This represents grating coupler and intrinsic set-up loss.(E) Summary of normalized transmission loss at wavelength 1565nm (peak grating coupler transmission) for all four fin waveguide design and reference strip waveguide at L_{wg}=250µm, 500µm, 1000µm, 2000µm.

Waveguide transmission loss for fin and strip waveguides was measured using a TE polarized continuous-wave (CW) light source. A tuneable (1525nm-1625nm) laser source (input power 10mW (10dBm)) was TE polarized using a fiber polarization controller. Input and output grating couplers were used to couple light from a single mode fiber (SMF) into and out of the waveguide and transmission power was measured using a photodetector connected to the output SMF. Waveguides of lengths L_{wg}=250µm, 500µm, 1000µm, 2000µm were measured. Three devices were measured per L_{wg}. Transmission loss across the wavelength spectrum from each device was corrected for Fabry-Perot (FP) resonance caused by the grating couplers and then averaged across the three devices. Figure 7(A) – 7(D) shows the non-normalized transmission spectrum (after FP resonance correction and averaging) for each fin design and each waveguide length. The reference "Ref" result is extrapolated from 12 strip waveguide devices (three per L_{wg}), and represents a 0µm waveguide (set-up, coupling and taper loss only contributing to transmission loss). The normalized transmission loss at wavelength 1565nm (the wavelength for which the grating coupler was optimised) for the strip waveguide and four fin waveguide designs is shown in Fig. 7(E). The measured transmission loss at this wavelength for the dry etched strip waveguide without fins was 0.74dB/mm, lower than the 1.5dB/mm loss measurement reported for comparable double-SOI structures incorporating a 25nm horizontal SiO_2 slot [32]. This can be improved by utilizing the same wet etching step as used for the fin waveguides, to reduce waveguide sidewall roughness (others have shown that strip waveguide optical loss can be reduced down to 0.85dB/cm [8], as a result of the wet etching process outlined herein). We later realized that we could have opened etching windows around these strip waveguide sections as well as the fin waveguide sections. Fin waveguide transmission loss was as low as 5.8dB/mm (fin

design #1), which we believe can be improved by process optimization and more importantly, design optimization. The fin waveguide transmission loss (if unoptimized) within the 500µm phase shifter will increase the total active device optical loss (simulated to be between 2-5dB depending on design parameters (Fig. 3)) by 2.4dB, which is tolerable. This would not be expected to negatively affect performance metrics such as $V_\pi L$ or f_{3dB}. Grating coupler loss as low as 4.0dB per grating has also been observed.

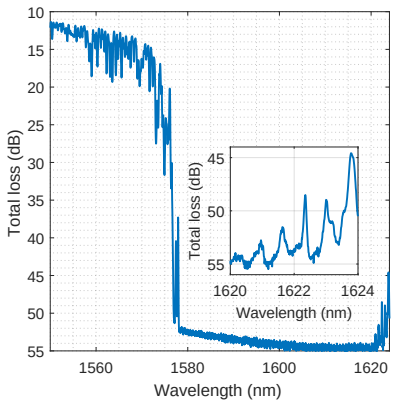

Fig. 8. Transmission loss of single fin waveguide device (fin design # 4), L_{wg} = 250µm. Wavelength spectrum spans photonic bandgap (1578nm-1620nm). Insert shows transmission at upper stopband, magnified.

Fin design #4 exhibits a photonic bandgap as predicted by FDTD simulations (Fig. 2) between 1578nm-1620nm. This is shown by the non-normalized transmission spectrum of a single fin waveguide device (L_{wg} = 250µm) in Fig. 8.

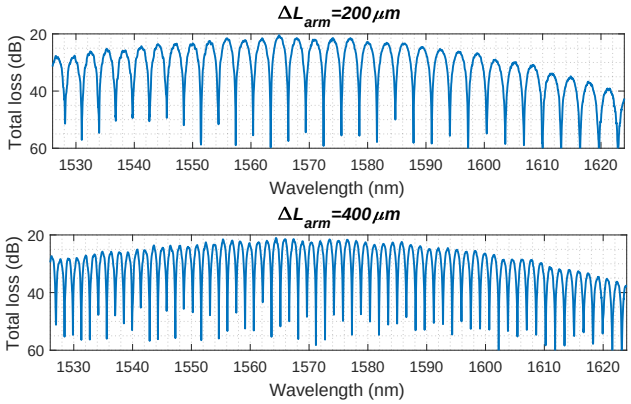

Fig. 9. Absolute transmission loss of single MZI devices (passive) with different ΔL_{arm}. The phase shifter sections of the MZI are fin-waveguide design # 3.

The passive MZI devices were characterized using the same method as that used to characterize transmission loss for the strip and fin waveguides. The conventionally designed MZI device consists of an input grating coupler and input taper, a 1X2 Multi Mode Interferometer (MMI), two strip waveguides (four waveguide bends with radius=20µm per waveguide) with an intermediate 500µm fin waveguide section (fin design #2), a 2x1 MMI, an output taper and an output

grating coupler. The transmission spectrum's of two devices, one with arm length difference, ΔL_{arm}=200μm, the other with ΔL_{arm}=400μm are shown in Fig. 9. Both devices show periodic constructive and destructive interference as a function of wavelength as expected. This result suggests that the fin waveguide quality is sufficient for use in an active accumulation modulator utilizing this design.

5. Conclusion

A new design and fabrication process has been presented and demonstrated, to extend 2 dimensional planar Si photonics vertically into 3 dimensions. The mirrored alignment of the top and bottom SOI (111) crystal planes allows the bottom layer to be etched separately from the top layer, from above. Three dimensional fin waveguides with fully suspended top fins and fully over-etched bottom fins were fabricated on bonded double-SOI with the narrowest bonding oxide thickness (13.5nm) currently recorded in literature for any strip waveguide with intermediate slot. We argue that the successful selective etching of the bottom SOI layer independently from the top SOI layer using anisotropic wet etching solves the main challenge associated with fully crystalline horizontal gate oxide MOScap modulators, and the utilization of this technique will pave the way for future development of active modulator devices with 0 parasitic capacitance, leading to higher speed or lower power consumption. C–V measurement of a MOS capacitor device demonstrated the sufficient electrical quality of the 13.5nm bonding gate oxide layer for use in active components (e.g. MZI accumulation modulator). Transmission loss of strip waveguides fabricated on this platform are lower than that previously reported in literature for similar devices, and transmission loss of fin waveguides is sufficient for use in a MZI accumulation modulator. These results demonstrate the feasibility of this platform and fabrication process on which to develop both active and passive three dimensional Si photonics devices.

Funding

EPSRC Standard Grant (EP/M009416/1); EPSRC Manufacturing Fellowship (EP/M008975/1); EPSRC Platform Grant (EP/N013247/1); The University of Southampton Zepler Institute Research Collaboration Stimulus Fund.

Acknowledgments

The data from this paper can be obtained from The University of Southampton e-Print repository: https://doi.org/10.5258/SOTON/D0667

References

1. R. A. Soref, "Silicon-based optoelectronics," Proc. IEEE **81**, 1687–1706 (1993).
2. D. A. Miller, "Rationale and challenges for optical interconnects to electronic chips," Proc. IEEE **88**, 728–749 (2000).
3. D. A. Miller, "Device requirements for optical interconnects to silicon chips," Proc. IEEE **97**, 1166–1185 (2009).
4. I. A. Young, E. Mohammed, J. T. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, and P. L. Chang, "Optical I/O technology for tera-scale computing," IEEE J. Solid-State Circuits **45**, 235–248 (2010).
5. R. K. Montgomery, M. Ghiron, P. Gothoskar, V. Patel, K. Shastri, S. Pathak, and K. A. Yanushefski, "High-speed silicon-based electro-optic modulator," (2005). US Patent 6,845,198.
6. A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal–oxide–semiconductor capacitor," Nature **427**, 615–618 (2004).
7. J. Fujikata, S. Takahashi, M. Takahashi, and T. Horikawa, "High speed and highly efficient Si optical modulator with MOS junction for 1.55 μm and 1.3 μm wavelengths," in *2013 IEEE 10th International Conference on Group IV Photonics (GFP),* (IEEE, 2013), pp. 65–66.
8. K. Debnath, H. Arimoto, M. K. Husain, A. Prasmusinto, A. Al-Attili, R. Petra, H. M. Chong, G. T. Reed, and S. Saito, "Low-loss silicon waveguides and grating couplers fabricated using anisotropic wet etching technique," Front. Mater. **3**, 10 (2016).
9. K. Debnath, D. J. Thomson, W. Zhang, A. Z. Khokhar, C. Littlejohns, J. Byers, L. Mastronardi, M. K. Husain, K. Ibukuro, F. Y. Gardes, and S. Saito, "All-silicon carrier accumulation modulator based on a lateral metal-oxide-semiconductor capacitor," Photonics Res. **6**, 373–379 (2018).

10. R. A. Soref and B. R. Bennett, "Kramers-kronig analysis of electro-optical switching in silicon," in *Integrated Optical Circuit Engineering IV,* vol. 704 (International Society for Optics and Photonics, 1987), pp. 32–38.
11. A. Auberton-Herve, "SOI materials to systems," in *Electron Devices Meeting, 1996. IEDM'96., International,* (IEEE, 1996), pp. 3–10.
12. U. Fischer, T. Zinke, J.-R. Kropp, F. Arndt, and K. Petermann, "0.1 db/cm waveguide losses in single-mode SOI rib waveguides," IEEE Photonics Technol. Lett. **8**, 647–648 (1996).
13. S. Suzuki, M. Yanagisawa, Y. Hibino, and K. Oda, "High-density integrated planar lightwave circuits using SiO_2-GeO_2 waveguides with a high refractive index difference," J. Light. Technol. **12**, 790–796 (1994).
14. P. A. Anderson, B. S. Schmidt, and M. Lipson, "High confinement in silicon slot waveguides with sharp bends," Opt. Express **14**, 9197–9202 (2006).
15. H. Arimoto, M. K. Husain, A. Prasmusinto, K. Debnath, A. Al-Attili, R. Petra, H. M. Chong, G. T. Reed, and S. Saito, "Low-loss silicon rectangular waveguides fabricated by anisotoropic wet etching for roughness reduction," in *2015 IEEE 12th International Conference on Group IV Photonics (GFP),* (IEEE, 2015), pp. 90–91.
16. C. G. Poulton, C. Koos, M. Fujii, A. Pfrang, T. Schimmel, J. Leuthold, and W. Freude, "Radiation modes and roughness loss in high index-contrast waveguides," IEEE J. Sel. Top. Quantum Electron. **12**, 1306–1321 (2006).
17. K. K. Lee, D. R. Lim, L. C. Kimerling, J. Shin, and F. Cerrina, "Fabrication of ultralow-loss Si/SiO_2 waveguides by roughness reduction," Opt. Lett. **26**, 1888–1890 (2001).
18. Y. Liu, T. Hayashida, T. Matsukawa, K. Endo, S. O'uchi, K. Sakamoto, M. Masahara, K. Ishii, J. Tsukada, Y. Ishikawa, H. Yamauchi, A. Ogura, and E. Suzuki, "An experimental study of TiN gate finFET SRAM with (111)-oriented sidewall channels," in *2008 Silicon Nanoelectronics Workshop,* (IEEE, 2008), pp. 1–2.
19. X. Wu, B. Dama, P. Gothoskar, P. Metz, K. Shastri, S. Sunder, J. Van der Spiegel, Y. Wang, M. Webster, and W. Wilson, "A 20Gb/s NRZ/PAM-4 1V transmitter in 40nm CMOS driving a Si-photonic modulator in 0.13 μm CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC),* (IEEE, 2013), pp. 128–129.
20. K. Debnath, A. Z. Khokhar, G. T. Reed, and S. Saito, "Fabrication of arbitrarily narrow vertical dielectric slots in silicon waveguides," IEEE Photonics Technol. Lett. **29**, 1269–1272 (2017).
21. K. Debnath, A. Z. Khokhar, G. T. Reed, and S. Saito, "Fabrication of silicon slot waveguides with 10nm wide oxide slot," in *2017 IEEE 14th International Conference on Group IV Photonics (GFP),* (IEEE, 2017), pp. 37–38.
22. M. Sodagar, A. H. Hosseinnia, P. Isautier, H. Moradinejad, S. Ralph, A. A. Eftekhar, and A. Adibi, "Compact, 15 Gb/s electro-optic modulator through carrier accumulation in a hybrid $Si/SiO_2/Si$ microdisk," Opt. Express **23**, 28306–28315 (2015).
23. S. Akiyama and T. Usuki, "High-speed and efficient silicon modulator based on forward-biased pin diodes," Front. Phys. **2**, 65 (2014).
24. Y. Urino, Y. Noguchi, M. Noguchi, M. Imai, M. Yamagishi, S. Saitou, N. Hirayama, M. Takahashi, H. Takahashi, E. Saito, M. Okano, T. Shimizu, N. Hatori, M. Ishizaka, T. Yamamoto, T. Baba, T. Akagawa, S. Akiyama, T. Usuki, D. Okamoto, M. Miura, J. Fujikata, D. Shimura, H. Okayama, H. Yaegashi, T. Tsuchizawa, K. Yamada, M. Mori, T. Horikawa, T. Nakamura, and Y. Arakawa, "Demonstration of 12.5-Gbps optical interconnects integrated with lasers, optical splitters, optical modulators and photodetectors on a single silicon substrate," Opt. Express **20**, B256–B263 (2012).
25. S. Akiyama, T. Baba, M. Imai, T. Akagawa, M. Takahashi, N. Hirayama, H. Takahashi, Y. Noguchi, H. Okayama, T. Horikawa, and T. Usuki, "12.5-Gb/s operation with 0.29-Vcm VπL using silicon Mach-Zehnder modulator based-on forward-biased pin diode," Opt. Express **20**, 2911–2923 (2012).
26. T. Baba, S. Akiyama, M. Imai, T. Akagawa, M. Takahashi, N. Hirayama, H. Takahashi, Y. Noguchi, H. Okayama, T. Horikawa, and T. Usuki, "25-Gbps operation of silicon pin mach-zehnder optical modulator with 100-μm-long phase shifter," in *CLEO: Science and Innovations,* (Optical Society of America, 2012), pp. CF2L–3.
27. T. Baba, S. Akiyama, M. Imai, N. Hirayama, H. Takahashi, Y. Noguchi, T. Horikawa, and T. Usuki, "50-Gb/s ring-resonator-based silicon modulator," Opt. Express **21**, 11869–11876 (2013).
28. M. Webster, P. Gothoskar, V. Patel, D. Piede, S. Anderson, R. Tummidi, D. Adams, C. Appel, P. Metz, S. Sunder, B. Dama, and K. Shastri, "An efficient MOS-capacitor based silicon modulator and cmos drivers for optical transmitters," in *2014 IEEE 11th International Conference on Group IV Photonics (GFP),* (IEEE, 2014), pp. 1–2.
29. H. Moradinejad, A. H. Atabaki, A. H. Hosseinia, A. A. Eftekhar, and A. Adibi, "High-Q resonators on double-layer SOI platform," in *2013 Photonics Conference (IPC),* (IEEE, 2013), pp. 430–431.
30. K. Ljungberg, A. Söderbärg, and U. Jansson, "Improved direct bonding of Si and SiO_2 surfaces by cleaning in H_2SO_4: H_2O_2: HF," Appl. Phys. Lett. **67**, 650–652 (1995).
31. A. V. N. Rao, V. Swarnalatha, A. K. Pandey, and P. Pal, "Determination of precise crystallographic directions on si {111} wafers using self-aligning pre-etched pattern," Micro Nano Syst. Lett. **6**, 4 (2018).
32. R. M. Briggs, M. Shearn, A. Scherer, and H. A. Atwater, "Wafer-bonded single-crystal silicon slot waveguides and ring resonators," Appl. Phys. Lett. **94**, 021106 (2009).