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FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Electronic and Computer Science

Nano Research Group

Design, Fabrication and Characterization of High Performance Zinc Oxide Nanowire Field-Effect Transistors

by

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ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

SCHOOL OF ELECTRONICS AND COMPUTER SCIENCES

Doctor of Philosophy

DESIGN, FABRICATION AND CHARACTERIZATION OF HIGH PERFORMANCE ZINC OXIDE NANOWIRE FIELD-EFFECT TRANSISTORS

Nor Azlin Ghazali

This research project is focused on the optimization and electrical enhancement of zinc oxide (ZnO) nanowire field-effect transistors by remote plasma atomic layer deposition. Three device configurations have been fabricated based on a top-down fabrication method with channel lengths in the range of 18.6 μm to 1.3 μm. These devices were produced in well-defined locations on a 150 mm diameter silicon wafer. Controllable nanowire FET dimensions and locations are seen as fundamental to wafer-scale nanowire integrated circuit fabrication. Measured electrical results show n-type depletion behaviour with good electrical characteristics for all device configurations.

The first device configuration was fabricated with optimization of a top-down process based on a spacer method, aiming to reduce the sidewall roughness of the nanowire. The approach included the top-down nanowire process with reduced sidewall roughness during pattern transfer and the improvement of the electrical characteristics. The process involved a photoresist reflow technique and dry oxidation of the etched silicon sidewalls. The optimized top-down fabrication and sidewall resist smoothing were shown to produce ZnO nanowire FETs with good electrical characteristics for channel length devices of 1.3 μm, 8.6 μm, and 18.6 μm. The optimized device is able to produce a high output drain current by a factor of three, steep subthreshold slope of 800 mV/decade and a transconductance value of 5.9 nS, which is two times higher than the device from an un-optimized fabrication process.

In the second device configuration, the aim was to improve the contact resistance between the ZnO nanowire channel and source/drain contact as well as the mobility of the ZnO nanowire FET. Enhanced performance of the ZnO nanowire FET is demonstrated by depositing an Al-doped ZnO (AZO) thin film between the ZnO nanowires and the source/drain aluminium contact. This highly conductive AZO thin film is deposited via a thermal atomic layer deposition (ALD) at 200 ^{o}C and forms a bi-layer source/drain contact. The contact resistance was reduced from 194.1 Ω with aluminium contact to only 9.6 Ω using AZO. The field-effect mobility of ZnO nanowire FETs with AZO increases from 3.5 cm^2/Vs to 85.7 cm^2/Vs in dual nanowires. The AZO layer is seen as a promising source/drain contact material for the fabrication of high performance ZnO nanowire FETs. The ZnO nanowire FET with AZO thin film as the source/drain contact is further investigated by measuring the temperature-dependant electrical characteristics. The transfer curves shows a parallel shift toward negative voltage as the temperature increased from 200 K to 300 K.

In the third device configuration, the new fabrication method using direct photolithography and lateral wet etching was used to simplify the fabrication of top-down ZnO nanowire FETs and to avoid the disadvantage of the spacer method. This particular method is a preliminary attempt towards achieving high electrical performance in ZnO nanowire FETs for RF and logic circuit applications. This novel technique allows for the formation of nanowire FET with minimal impact from ions and chemical radicals during the anisotropic dry etching process. Except for the low field-effect mobility, this experiment demonstrated desirable electrical characteristics. Bottom-gate ZnO nanowire FETs with different gate lengths show a threshold voltage between -0.7 V to 1.5 V, on/off current ratio up to 10^7 and a subthreshold swing between 200 mV/decade to 300 mV/decade. This top-down fabrication method with low temperature film deposition encourages further research regarding the RF characterization of ZnO nanowire FETs and the adaptability of a RF device using ZnO nanowire FETs.

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DECLARATION OF AUTHORSHIP

I,Nor Azlin Ghazali, declare that this thesis entitles Design, Fabrication, and characterization of High Performance Zinc Oxide Nanowire Field-Effect Transistors, and the work presented in it are my own and has been generated by me as the result of my own original research.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
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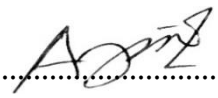
Signed: 

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Multichannel ZnO nanowire field effect transistors by lift-off process (accepted for publication)

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Effect of AZO ohmic layer on ZnO nanowire field-effect transistors (in preparation)

N. A. B. Ghazali, M. Ebert, K.Kalna, M. R. R. De Planque, and H. M. H. Chong, *Applied Surface Science.*

Conferences

ZnO nanowire-FET for charge-based sensing of protein biomolecules

N.M.J. Ditshego, N.A.B. Ghazali, M. Ebert, K. Sun, I. Zeimpekis, P. Ashburn, M.R.R. de Planque, H.M.H. Chong. IEEE NANO 2015, 15th International Conference on Nanotechnology (accepted for publication), 27 – 30 July 2015, Rome (Italy).

Top- down fabrication optimisation of ZnO nanowire-FET by sidewall smoothing

N. A.B. Ghazali, M. Ebert, N. M. J. Ditshego, M. R. R. de Planque, and H. M. H. Chong, *41st International Conference on Micro and Nano Engineering (MNE2015),* The Hague, 21st-24th September 2015.

Novel top-down fabrication of ZnO nanowires by atomic layer deposition and anisotropic dry etch process

Ebert M., Ghazali N. A.B., Kiang K.S., de Planque M.R.R., and Chong H. M. H., *29th International Microprocesses and Nanotechnology Conference (MNC 2016)*, Kyoto, 8th-11th November 2016.

Novel top-down bilayer photoresist fabrication of ZnO nanowire Field effect transistors

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Definitions and Abbreviations

AFM	Atomic Force Microscope
Al_2O_3	Aluminium Oxide
ALD	Atomic Layer Deposition
AZO	Aluminium-Doped Zinc Oxide
CHF_3	Fluoroform
CTLM	Circular Transmission Line Measurement
CO_2	Carbon Dioxide
CVD	Chemical Vapour Deposition
DC	Direct Current
DEZ	diethyl zinc
FEGSEM	Field Emission Scanning Electron Microscopy
FET	Field-Effect Transistor
FIB	Focused Ion Beam
HCl	Hydrochloric Acid
HF	Hydrofluoric Acid
IBE	Ion Beam Etcher
ICP	Inductively Coupled Plasma
IPA	Isopropyl Alcohol
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMP	1-Methyl-2-pyrrolidon
NW	Nanowire

NWFET	Nanowire Field-Effect Transistor
O_2	Oxygen
PEALD	Plasma Enhance Atomic Layer Deposition
PECVD	Plasma Enhanced Chemical Vapour Deposition
PMMA	Poly(methyl methacrylate)
RF	Radio Frequency
RIE	Reactive Ion Etch
RMS	Root-Mean-Square
RPALD	Remote Plasma Atomic Layer Deposition
SEM	Scanning Electron Microscopy
SS	Subthreshold Slope
TLM	Transmission Line Measurement
TMA	Trimethylaluminum
TMAH	Tetramethylammonium Hydroxide
VLS	Vapour-Liquid-Solid
ZnO	Zinc Oxide

Chapter 1:
Introduction

This chapter provides an introduction to the research work presented in this report. It describes the motivation and objectives of the research work and finally, it introduces the structure of the report.

1.1 Overview

It is undeniable that semiconductors changed the world beyond anything that could have been imagined since the first transistor was invented at Bell Laboratories, United States of America in 1947 [1]. Further development of the transistors has lead to devices using different type of semiconducting materials. Transistor technology developments have sustained the research of new semiconductor material and new structures of modern nanostructured semiconductor devices such as nanowires. Nanowires (NWs) made from different semiconductor material systems (gallium arsenic, zinc oxide) have been studied extensively over the past two decades and developments in this field continue. This is due to their novel electronic, photonic and sensing properties.

Zinc oxide (ZnO) as a semiconductor has attracted considerable research effort due to its unique properties such as its high electron mobility and its high crystalline quality as well as its versatile applications in fabricating electronic devices and sensors of nanoscale dimensions [2]. ZnO is an II-VI compound which crystallizes in the wurtize phase and has a wide direct bandgap of 3.4 eV at room temperature with a high breakdown voltage and large saturation velocity [2]. It also has several advantage over the GaN including larger exciton binding energy (60 meV versus 25 meV for GaN), low temperature epitaxial growth and the possibility of a wet etching process leading to potential low cost ZnO based devices. It is also a promising semiconductor material with several exciting applications and a robust tendency to grow in nanostructured form.

Generally, there are two methods to manufacture ZnO nanowires. The most common method is by a bottom-up process such as chemical vapour deposition (CVD), vapour-liquid-solid (VLS) or a wet chemical synthesis [3]–[5]. Based on these methods, high quality nanowires with excellent mobility can be fabricated but because the nanowire is scattered on the substrate, there is a need for a good pick and place method to align the

nanowire. Furthermore, many variables such as the different sizes of the grown nanowires as well as alignment issues and the issues of the alignment attest to how difficult it is to make nanowire-based devices.

The top-down process is conventional scaling, it is a straightforward process to pattern and etch the nanowires' structure. The top-down process is seen as the best candidate to overcome the drawbacks of the bottom-up process [6]. The top-down process offers nanowires a well-defined location on substrates and allows nanowires with various length to be fabricated on the same wafer. Although ZnO-based nanowires fabricated by top-down methods do not exhibit excellent mobility compared to nanowires fabricated by the bottom-up process, in Ref. [6] shows a potential of top-down methods fabricating a device with field-effect mobility > 10 cm^2/Vs with excellent crystallinity.

The nanowires are the best candidates for the realization of field-effect transistors (FETs) owing opportunity to construct a wrapping gate that offers an improvement of electrostatic control of the channel, with in parallel good on/off current ratio which are necessary for various applications [7]. The ZnO nanowires are also suitable to create high performance FETs in large-area electronics and active-matrix display or sensor arrays, which involve less complex circuitry and smaller FET densities [8].

In general, research on high performance ZnO nanowires FETs is ongoing, and there are still a number of gaps to be filled. The aim of this research work is the development of high performance FETs with high mobility based on ZnO nanowires that can be fabricated at low temperature and can therefore be implemented on silicon or polymer-based substrates.

1.2 Motivation

ZnO has been widely used in sunscreen lotions, paints, ceramics, and food supplements for quite a long time. Aside from its common uses, it also a very promising material for semiconductor devices such as transistors and diodes. The main advantages of ZnO are abundance, low price and it is non-toxic in small amounts. In recent years, ZnO has been considered a favourable candidates as metal oxide materials because of its low-cost fabrication, ideal conductivity and efficient visible transmittance [9].

Stoichiometric ZnO is a semicondcutor that crystallizes with a wurtzite structure [9]. The ZnO crystal is naturally n-type due to the native defect such as zinc interstitials and

oxygen vacancies. The research of the p-type ZnO is still an ongoing research area and the lack of p-type material has hindered the development of transistors based on ZnO. Although there are several reports on p-type measurements in ZnO [10], there is still ongoing research seeking to discover a good quality p-type ZnO. While the p-type is still mysterious, the advantages of the n-type ZnO are being utilized by using it as an active layer on p-type materials and by utilizing heteroepitaxy structures [11].

The typical Hall mobility of single crystals of ZnO at room temperature are about 100 cm^2/Vs –200 cm^2/Vs [12]. These properties make ZnO attractive for nanowires, which have been produced by a various methods that generally produce single-crystal material [13]. However, improving the quality of the crystal growth and device fabrication process may increase the mobility of ZnO nanowires to thousands of cm^2/Vs [14]. Additionally, nanowires have been found to have superior electrical and mechanical properties compared to bulk ZnO, because of their confined dimensions.

Initial studies of top-down ZnO nanowire field-effect transistors (NWFETs) showed a significant variation of electrical characteristics, such as output drain current, threshold voltage and field-effect mobility [6]. One of the possible causes is the nanowire surface roughness from the fabrication process, which can induce a high trap charge density and influence the device characteristics [15]. The other possible reason for the variation, especially the mobility, is due the existence of contact resistance. Contact resistance might decrease the voltage drop across the channel and limit the injected current [16]. In semiconductor devices, high contact resistance could lead to the deterioration of device performance caused by thermal stress, likely resulting in device failures. In addition, the ZnO nanowire FET also exhibits a relatively large operating voltage, which makes it unsuitable for low power device application. This problem can be avoided by modulating the gate insulator and carrier concentration of the ZnO channel layer [17]. In order to drive a high output current at low voltage, the capacitive coupling between the active channel and the gate electrode must be increase by reducing the gate insulator thickness or using a high dielectric constant material [18][19]. On the other hand, carrier concentration of the ZnO nanowire also related to its resistance. The large number of free carriers in the ZnO nanowire can decrease the resistance of the ZnO channel, triggering a high flow of electrons to pass through the source and drain.

In this work, the ZnO nanowire FETs will be fabricated by optimising process steps based on [6] with a focus on improving the surface roughness of the nanowire and reduce

the contact resistance between the contact pad and the active channels. Moreover, in order to increase the speed of the transistor, it is necessary to reduce the gate length specifically top-gate configuration. These strategies have the potential to produce high performance ZnO nanowire FETs in terms of low subthreshold swing, large on/off current ratio, high carrier mobility and threshold voltage stability.

The main focus of this research is the n-type ZnO nanowire based FET fabricated using a top-down fabrication method, which can demonstrate high performance transistor characteristic for radio frequency (RF) and logic circuit applications. Based on Franklin's high performance transistor review by, high performance transistors should have a low operating voltage of <1 V, high drive current of > 1 mA/μm and the channel length of < 20 nm [20]. Although mobility is one of the most widely used metrics for describing carrier transport through a semiconductor, mobility in no longer meaningful for high performance transistors with short channel variety [20]. This is because if the channel length is falls below the average length between scattering events or the channel is ballistic, the carrier transport is no longer limited by scattering in the channel [20]. Mobility remains a useful parameter for a high performance devices with long channel variety. Thus, the aim of this research work to fabricate a high performance FET based on the n-type ZnO nanowire with aforementioned high performance characteristics. So, this work aims to achieve on/off current ratio of ~ 10^6 because it is an acceptable on/off current ratio for RF applications [21], low threshold voltage between -5 V to 5 V, subthreshold swing of 200 mV/decade and mobility of ~ 100 cm^2/Vs. Instead of focussing on a channel length criteria specified by Franklin, to achieved high performance ZnO nanowire FETs, this study will focus on fabrication of a high performance transistor with gate lengths varying from 2 μm to 4 μm. In order to achieve small gate length of up to 20 nm, the electron beam (e-beam) lithography need to be used and the etching selectivity becomes critical since the most commonly used etching mask material in e-beam lithography is a thin layer of a poly(methyl methacrylate) (PMMA) [22]. Since, the deposited ZnO thin film has a grain issue, the wet etching of the nanowire could not be accurately achieved and the dry etching also not possible because the PMMA is not compatible with ZnO etching process.

1.3 Objectives

This work aims to address the following research objectives:

- To fabricate the ZnO nanowire FETs with an optimized process step to improve the surface roughness of the ZnO nanowires. Surface roughness is shown to have

significant effects in electrical properties. Therefore, improving the surface roughness, could improve the electrical characteristics of the device.

- To further optimize the device by investigating different SiO_2 thickness and using Al_2O_3 as the gate oxide to reduce the leakage current.
- To fabricate the ZnO nanowire FETs with an optimized process step of improving contact between ZnO nanowires and Al source drain pads by using the AZO.
- To fabricate a new structure of ZnO nanowire FETs using photolithography and lateral wet etch for RF applications. This experiment aim to simplify the top-down fabrication process using a wet etch method for nanowire FETs.

1.4 Thesis Outline

This thesis is structured and divided into several background and experimental chapters. This section summarises and cover the necessary scientific theory required to understand the aim and the scope of the study as well as the experimental evidence needed to justify the approach.

Chapter 2 provides an introduction and discusses the fundamental theory of the research in detail. The chapters start by discussing the operation of a metal-oxide semiconductor field-effect transistor (MOSFET). The discussion is based on the n-type definitions and the expression of the electrical parameters of the devices. It also presents a summary of existing ZnO-based field-effect transistor technologies, as well as the current research. Firstly, ZnO material will be discussed and this will be followed by a comparison ZnO nanowire FETs in terms of their fabrication processes and electrical characteristics.

Chapter 3 explains the capacitance model used for the fabricated ZnO nanowire FETs. It also discussed about the extraction method of the electrical characteristics of the ZnO nanowire FET such as threshold voltage, subthreshold slope, and field-effect mobility and verify these measured values with calculation based on analytical model and simulation model.

Chapter 4 describes the deposition of the ZnO thin film, design, and fabrication method in ZnO nanowire FET fabrication, together with the potential advantages of each technique.

Chapter 5 presents a characterization of a top-down ZnO nanowire FET made using the sidewall smoothing technique from Chapter 4. In the first phase, the effect of gate

dielectric thickness has been discussed. After the optimum gate dielectric thickness has been identified, the effect of nanowire surface roughness is explained. The sidewall smoothing technique reduced the nanowire roughness and improved the electrical characteristics of ZnO nanowire FET. The electrical characteristics of the ZnO nanowire FETs from the non-reflow and reflow resist processes were then compared to give an insight of the effect of surface roughness.

Chapter 6 explains the enhanced performance of ZnO nanowire FETs by depositing AZO thin film between the ZnO nanowire FET and the source/drain Al contact. The properties of AZO film, field-effect mobility, on/off current ratio, threshold voltage and subthreshold slope of the ZnO nanowire FETs with and without the AZO layer were systematically investigated. The electrical characteristics measured at various temperatures ranging from 200 K-300 K was then discussed.

Chapter 7. The preliminary electrical characteristics of the ZnO nanowire FET for RF applications is discussed in this chapter as well as the results based on the prototype device for RF characterization with ground-signal-ground contact pads.

Chapter 8 concludes this study with an overview of what have been achieved, and a discussion of the important contribution of this work. It suggest how to characterize this device for RF performance evaluation as future extension to this work. Further optimization processes are also described.

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Chapter 2:
Literature Review

This chapter presents the quantitative details of depletion-mode n-type ZnO nanowire FET with bottom gate structure and theory of field effect transistor (FET) upon the standard MOSFET approach. This chapter also discusses the literature on zinc oxide (ZnO) material, various ZnO nanowire deposition techniques and respective electrical properties. Its aim is to grasp the best method to fabricate high performance ZnO nanowire field-effect transistors (FETs) with excellent electrical characteristics.

2.1 Introduction

The electrical characteristics of nanowire-based FETs will be discussed in this chapter. FETs are a fundamental component in modern electronics, and are used in a wide variety of applications. The term FET indicates a three-terminal device where the current flow between source and drain is monitored by the electric field from the gate electrode. Nanowire FET have can be fabricated based on top-gate [1][2], bottom-gate [3][4] and surround-gate [5][6] geometries and all types of geometries show a promising FET characteristics. Mostly, nanowire FET are operated in an accumulation or depletion mode. The specific theory discussed in this chapter is based on depletion-mode n-channel field-effect transistors. The semiconductor employed in this study is ZnO and usually shows n-type conductivity. Thus the following discussion on FET mode of operation will focus on the FET structure with an n-type channel. Figure 2.1 shows the cross-sectional view of an n-type nanowire FET channel with a bottom-gate structure. It is assumed that the cross-section of the nanowire used in this section is a square shape rather than a circular, hexagonal or triangular nanowire shape to simplify the analytical calculation method based on thin film transistor (TFT) operation principles. This is because the fabricated ZnO nanowire FETs is technically a TFT and the conduction through ZnO nanowires is surface-centred rather than bulk-centred. The nanowire is a semiconductor with n-type impurities and the metals are used for ohmic contacts of the source and drain. Here, L and d, represent the length and thickness of the nanowire, respectively.

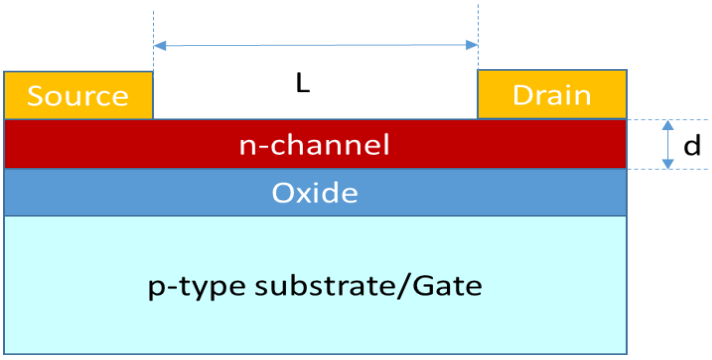


Figure 2.1 Cross-section of an n-type nanowire FET with bottom-gate structure.

Typically, nanowire FET is treated using metal-oxide-semiconductor (MOSFET) equations. However, it is important to note that the nanowire FET structure owns some dissimilarities as compared to the widely studied. In a nanowire FET, the source and drain is made from metal electrode and it contact with the channel. In contrast, the source and drain regions of the MOSFET are made up of degenerately doped semiconductor. An additional property of nanowire FETs to consider is that usually the nanowire is uniformly doped along its axial length. In MOSFET, the channel have varies dopant profiles along its axial length in order to improve the performance.

Depletion-mode FETs are normally-on-state devices. Unlike a normally-off-state FET (enhancement-mode FET), a depletion mode FET have a conductive channel and current flow strongly between the drain and source when applying zero voltage gate. When a voltage gate is applied to the gate, the bands of the semiconductor bend and electron are either depleted or accumulated underneath the gate depending on the bias this concept is the basis for the operation of the nanowire FET.

2.1.1 Depletion

In the n-channel device, when the negative voltage V_{GS} is applied to the gate, the current from drain to source, I_{DS}, is turned off because the electric field created underneath the gate repels electrons and a depletion region form at the gate-insulator surface. Therefore, the bands near the ZnO surface are bend upward. As the negative bias increases, the depletion region expand because more electrons are withdrawn. The device is said to be in off-state since no conducting channel is present. Figure 2.2 shows a diagram of how a ZnO nanowire FET operates in depletion.

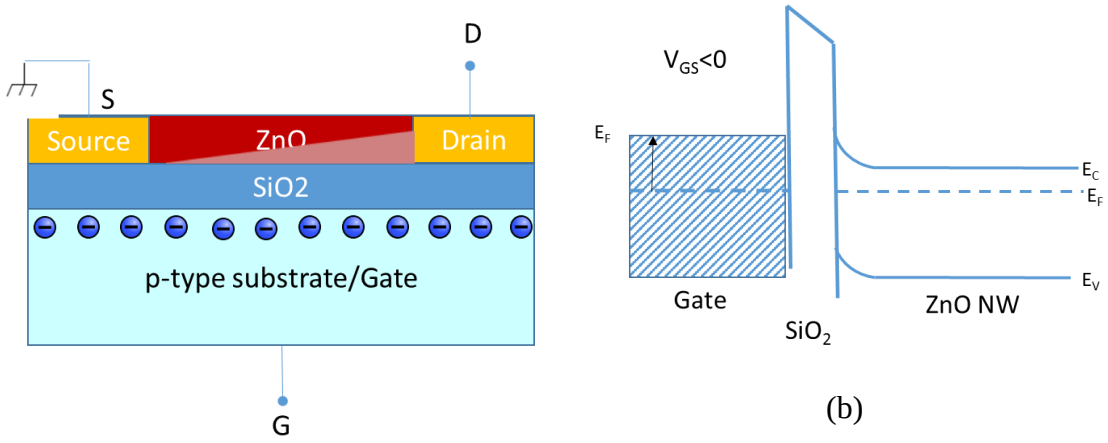
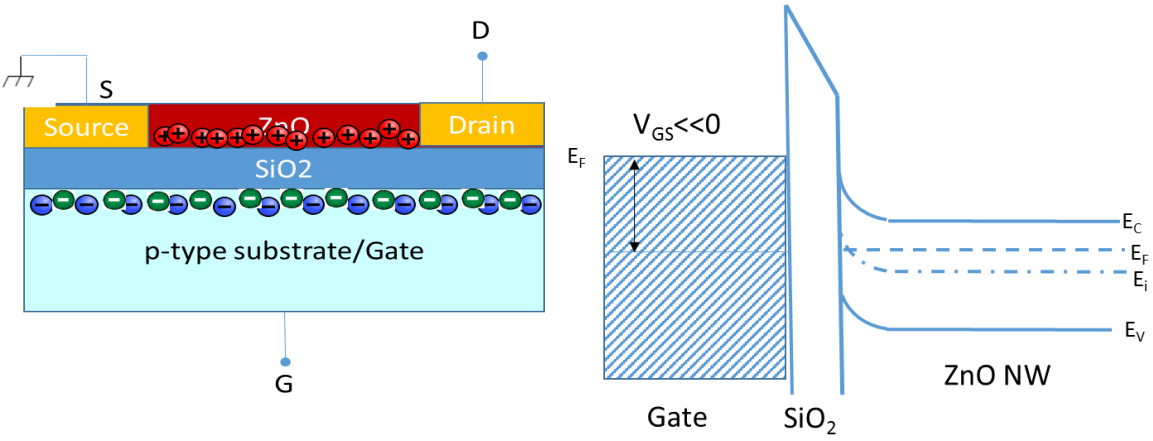


Figure 2.2 (a) Schematic of ZnO nanowire FET when negative voltage is applied (b) Energy band diagram of n-type ZnO nanowire FET in depletion conditions.

2.1.2 Inversion

When the negative voltage applied is further increased, a large number of holes were induced at SiO_2/ZnO interface. Accordingly, the bands bend upwards even more so that the intrinsic level at the surface crosses over the Fermi level as shown in Figure 2.3. There is an additional electron at the SiO_2/ZnO interface due to the minority carriers from the gate. In accordance with the charge in character observation, the condition where the number of minority carrier exceeds the number of majority carriers is referred to as inversion. However, in the case of a ZnO nanowire FET with the background n-type doping present in the material system, the inversion condition is difficult to realize under practical conditions because the ZnO based material is a wide band gap semiconductor [7].

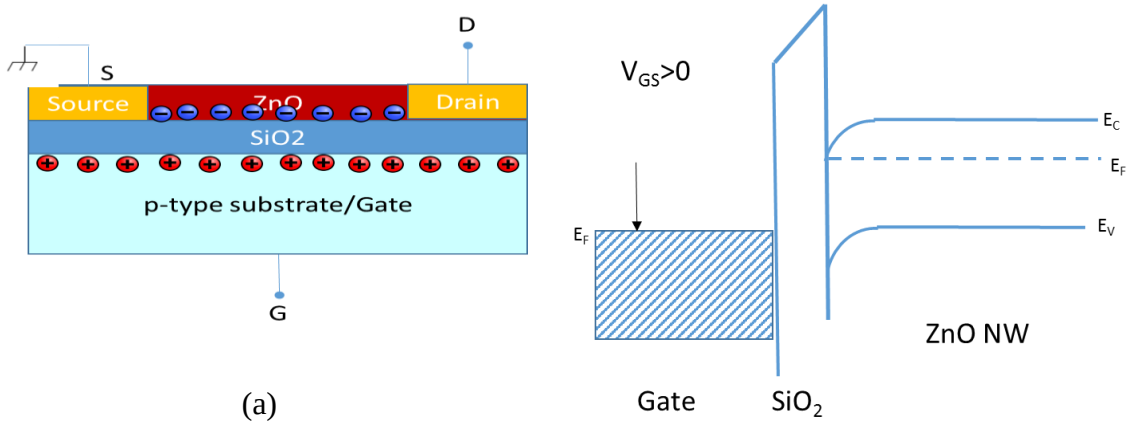


(a) (b)

Figure 2.3 (a) Schematic of ZnO nanowire FET when negative voltage is applied (b) Energy band diagram of ZnO nanowire FET in inversion.

2.1.3 Accumulation

The unique features of depletion-mode FETs is that they can also be made to operate in the enhancement-mode. This mode can be achieved by applying a positive bias to the gate. When the gate voltage is increased above the threshold voltage, V_{TH}, ($V_{GS} > V_{TH}$), the free electron is accumulated at the SiO_2/ZnO interface. Therefore, the bands near the ZnO surface are bent downwards and the conduction band edge becomes closer to the Fermi level. The schematic band diagram is shown in Figure 2.4.



(a) (b)

Figure 2.4 (a) Schematic of ZnO nanowire FET when positive voltage is applied (b) Energy band diagram of ZnO nanowire FET in accumulation.

If the gate voltage is keep on increased, the voltage drop across the ZnO channel and the corresponding potential difference leads to an expansion of the depletion layer at the drain side of the ZnO channel. When the drain bias equal to the gate bias ($V_{DS} = V_{GS}$), the width of the depletion layer equals to the thickness of the ZnO channel resulting in the onset of pinch-off and the drain current start to saturates. An excessive increase of the gate voltage lead to the increase of the V_{DS} result in the breakdown of the channel.

2.2 Electrical Characterization of Nanowire FET

The term FET indicates a three terminal device where the transverse electric-field imparted by the gate electrode controls the resistance of a ZnO channel between the source and drain terminals. In the fabrication of high performance FETs, feedback between device fabrication and characterization is important for the device optimization. Hence, accurate parameter extraction is essential in the high performance FETs. Based on the operation principle discussed previously, electrical characteristics of nanowire FETs will be discussed in this section.

2.2.1 Flat Band Voltage

The transfer from accumulation to depletion regions occurs at a finite voltage, V_{FB} called flat band voltage. It is the voltage at which the bands in the semiconductor are flat, which implies that no charge exists in the semiconductor. The flat band voltage basically equals the difference between the gate metal work function, $q\emptyset_m$, and the semiconductor work function, $q\emptyset_s$. This is the condition when there is no charge is present in the oxide or at the oxide-semiconductor interface and is referred to as the ideal flat band condition.

$$V_{FB} = q\emptyset_{ms} = q\emptyset_m - q\emptyset_s \quad (1)$$

The work function is the energy difference between the vacuum level and the Fermi level, which varies with the doping concentration.

2.2.2 Current-Voltage Relationship Concepts

In the linear region, the drain current (I_D) is dependent on both V_{GS} and V_{DS}. The I_D is a mixture of drift and diffusion currents. In the linear region operation the drift current becomes prominent and diffusion is negligible due to uniformity of the channel charge

from source to drain. Considering a differential drain voltage for an elemental section *dy* of conducting channel given by [8].

$$dV = I_D dR = \frac{I_D dy}{\mu_{FE} W |Q_{acc}(y)|} \tag{2}$$

Where μ_{FE} is the field-effect mobility and $Q_{acc}(y)$ is the total accumulation charge per unit area induced at position y within the channel given by:

$$Q_{acc}(y) = C_{ox}|V_G - V_{TH} - V(y)| \tag{3}$$

Separating the current from the voltage in Eq.3 gives:

$$I_D dy = \mu_{FE} W |Q_{acc}(y)| dV \tag{4}$$

Substituting Eq. 3 into Eq.4 and integrating from the source ($y = 0$, $V = 0$) to the drain ($y = L$, $V = V_D$) gives

$$I_D \int_0^L dy = \mu_{FE} W \int_0^{V_D} [C_{ox}(V_G - V_{TH} - V(y))] dV \tag{5}$$

Then Eq.5 yields

$$I_D = \frac{W}{L} C_{ox} \mu_{FE} \left\{ (V_G - V_{TH}) V_D - \frac{1}{2} {V_D}^2 \right\} \tag{6}$$

Since $V_D << V_G - V_{TH}$, Eq.6 is normally simplified into

$$\boxed{I_D = \frac{W}{L} C_{ox} \mu_{FE} (V_G - V_{TH}) V_D} \tag{7}$$

When $V_D \geq (V_G - V_{TH})$ channel pinches off. The channel actually ends before the drain edge. The drain current will saturate once the channel pinches off and become constant irrespective of any further increase in V_D. The resulting equation for I_D is as follows:

$$\boxed{I_{Dsat} = \frac{W}{2L} C_{ox} \mu_{sat} (V_G - V_{TH})^2} \tag{8}$$

2.2.3 Threshold Voltage, V_{TH}

Threshold voltage, V_{TH} is defined as the minimum applied gate bias which can conduct a channel between the source and drain that is needed to turn the device on for linear and saturation regions of operation. The discussion in this section will focus mainly

the derivation of the threshold voltage for depletion mode n-type ZnO nanowire FET. In this type of device, a negative gate bias will induce a space charge region under the oxide, reducing the thickness of the n-channel. A positive gate bias will create an electron accumulation layer, which increases the drain current. At threshold, it can be defined that the gate voltage, $V_G = V_{TH}$ where V_{TH} is the threshold voltage. The threshold voltage equals the sum of the flatband voltage, twice the bulk potential and the voltage across the oxide due to the depletion layer charge. The threshold voltage for the depletion mode n-type ZnO nanowire FET can be written as [9]:

$$V_{TH} = V_{FB} + 2\Psi_B + V_{DEP} \tag{9}$$

The potential due to the uncovered depletion layer charge is given by:

$$V_{DEP} = \frac{Q_{DEP}}{C_o} \tag{10}$$

The uncovered charge per unit area in the depletion region is simply

$$Q_{DEP} = -qN_D W \tag{11}$$

In the n-channel depletion mode nanowire FET, the bulk potential is negative (the band diagram bends upwards). By tying all the equation above it gives:

$$V_{TH} = V_{FB} - \frac{qN_D W}{C_0} - 2\Psi_B \tag{12}$$

2.2.4 The Subthreshold Region

When V_G is significantly larger than V_{TH}, the channel has plenty of mobile electrons and the current has limited drift due to V_D. However, when V_G is around V_{TH} or less than V_{TH}, the current is mainly due to diffusion current. The drain current in this region, is called the subthreshold current, and it is a critical characteristic for transistors operating at low voltage for low power applications. The subthreshold region reflects how fast the device can switch. The subthreshold current is given by:

$$I_D = I_{DI}\left(e^{\frac{q(V_G - V_{TH})}{nkT}}\right)\left(1 - e^{\frac{qV_D}{kT}}\right) \tag{13}$$

where I_{DI} is a dependent on temperature, device dimensions and channel doping. The term *n* in the equation is given by:

$$n = 1 + \frac{C_{DEP}}{C_{ox}} \tag{14}$$

C_{DEP} is the depletion capacitance per unit area and it is defined as:

$$C_{DEP} = \frac{\varepsilon_{ZnO}}{W_{DEP}} \tag{15}$$

The depletion width W_{DEP} may be derived to be:

$$W_{DEP} = W_m = \sqrt{\frac{\varepsilon_{ZnO}\varepsilon_o kT ln\frac{N_A}{n_i}}{qN_A}} \tag{16}$$

Subthreshold swing is another important device characteristic in the subthreshold region. The subthreshold swing, SS is defined as the change in the gate voltage required to reduce subthreshold current by one decade [5]. The subthreshold swing of a device is a measure of how fast the FET switches from the off state to the on state. This happens over the subthreshold regime of the transfer characteristics, which happens at gate voltages slightly below the threshold voltage. The logarithm is taken off the transfer characteristics, and the subthreshold swing is then the inverse of the gradient of the subthreshold regime. It is usually given in mV/decade, where the decade refers to an order of magnitude of source-drain current.

$$SS = \frac{dV_G}{d(logI_D)} \tag{17}$$

When V_D is larger than kT/q, the last term in Eq.13 can be ignored. Hence, the subthreshold swing varies exponentially with gate voltage. Thus, a curve of log (I_D) versus V_G is linear in the subthreshold region as shown in Figure 2.5, such a plot has a subthreshold swing of [10],

$$SS = n\frac{kT}{q} ln10\ V/decade \tag{18}$$

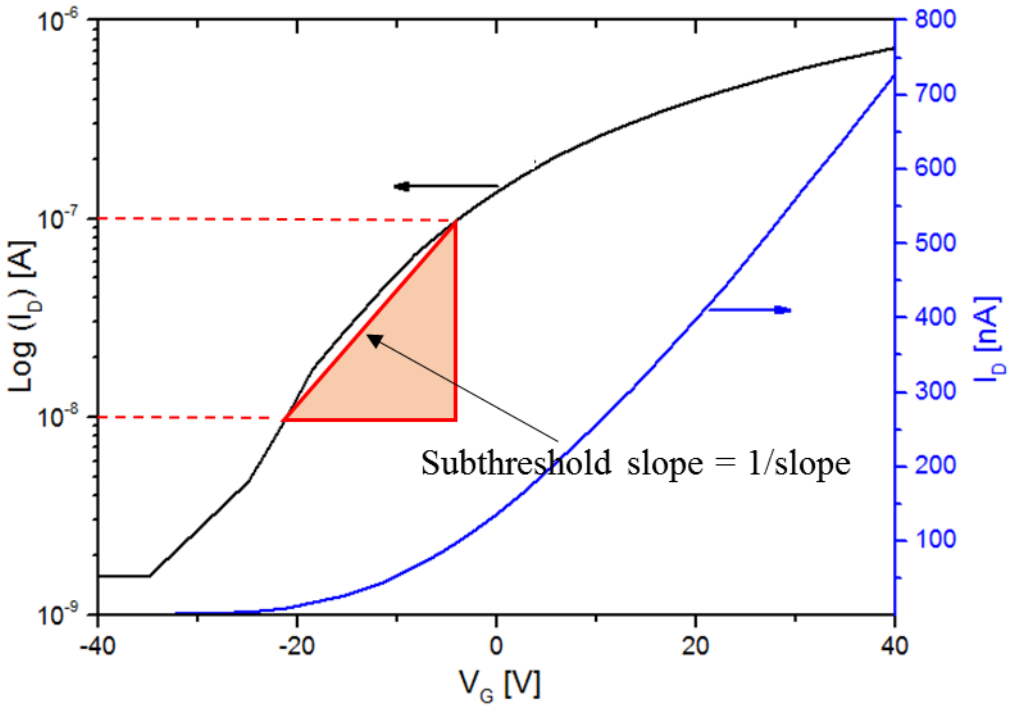


Figure 2.5 I_{DS}-V_{GS} curve in linear (blue) and semi-logarithmic scale of I_{DS}.

Theoretically, the subthreshold swing of 60 mV/decade is considered to be the lowest subthreshold swing achievable by a typical FETs [11]. A good device should have a steeper subthreshold swing in order for the device to be turned on using lower voltage.

2.3 Zinc oxide material system

Zinc oxide (ZnO) is an inorganic binary compound belonging to the II-VI semiconductor material group whose ionicity resides at the borderlines between the ionic and covalent semiconductor [12]. Research on ZnO has been being conducted since the early 1930 s [13][14]. In the last few years, we have seen the overwhelming interest in the material system possibilities of growing high quality ZnO single crystal and ZnO nanostructures. The ZnO is an excellent candidate for application in several different areas because it has a number of superior attributes when compared to other material such as GaN.

ZnO is an environmentally friendly material, wide band gap semiconductor with a direct gap of E_g ~ 3.4eV at 300 K which has been the focus of intense materials research and device development. The ZnO has fairly high quality bulk single crystal and a large exciton binding energy (~ 60meV) [13]. The electron Hall mobility of single crystalline ZnO using Monte Carlo simulation is estimated to be around 300 cm^2/Vs at room temperature [15] and its density is 5.6 gcm^{-3} [16] Moreover, ZnO can easily be etched in

acidic or alkaline solution at low temperatures. Another beneficial factor of ZnO in an electronic device is the possibility of patterning by wet etching [16].

ZnO can crystallize in three different crystals; wurtize (B4), zinc blende (B3) or rarely observed rocksalt (B1) as shown in Figure 2.6. However, ZnO preferentially crystallizes in the hexagonal wurtize-type, which is the stable phase of ZnO at 300 K and is most common form [12]. The zinc blend form can be stabilized by growing ZnO on substrate with cubic lattice structure. In both wurtize and zinc blends, the zinc and oxide centres are tetrahedral. The rocksalt (NaCl-type) structure is only observed at relatively high pressures of about 10 GPa [12]. The ZnO crystal is a hexagonal wurtize structure and exhibits partial polar characteristics with lattice parameters a = 0.3296, and c = 0.52065 nm, where the O^{2-} and the Zn^{2+} create alternating planes of tetrahedral coordinated units [13].

Most of the II-VI material show largely ionic bonding, which explains its strong piezoelectricity. Owing to the polar Zn-O bonds, zinc and oxygen planes bear positive and negative charges. In most similar materials, in order to keep electrical neutrality, those planes restructure at the atomic level. However in ZnO, its surfaces are atomically flat, stable and exhibit no reconstruction. This irregularity of ZnO has not yet been fully explained [3].

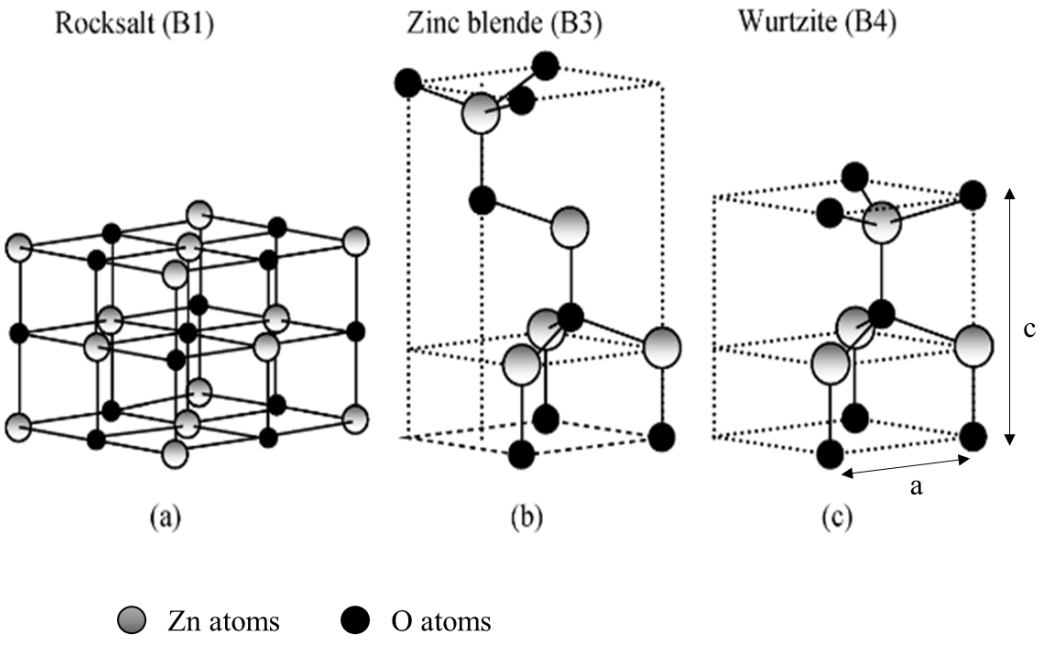


Figure 2.6 Stick and ball representation of ZnO crystal structures: (a) cubic rocksalt (B1), (b) cubic zinc blende (B3), and (c) hexagonal wurtzite (B4). The shaded gray and black spheres denote Zn and O atoms, respectively. Figure reproduced from Ref. [12].

Research interest in ZnO includes a diverse set of fields and each of them is inspired with respect to different applications. ZnO is used at the cutting edge of research in transparent electronics, optoelectronics, photovoltaics, diluted ferromagnets, sensors and solar cells [13][14][16]–[18].

2.4 Electrical properties of Zinc Oxide

It is important to understand the electrical behaviour of ZnO, prior to utilizing in the fabrication of electronic devices. The electrical properties of bulk and nanostructured ZnO have been investigated in detail over several decades, although variability across different reported samples has made definite measurement challenging [15]. Therefore, the electrical properties of ZnO are still not well understood.

ZnO is a naturally n-type doped material even in the absence of intentional doping [16]. It has been reported in the literature that this is due to the presence of some intrinsic defects. These defect include oxygen vacancies, (V_O) interstitial zinc atoms (Zn_I) and hydrogen impurities introduced during the growth of a ZnO nanowire. V_O related issues are particular interest for ZnO because it plays a central role in determining the physical and chemical properties of metal oxides [19]. However, the exact origin of the unintentional doping is still unclear and still being researched [20]. Recently, Liu et al. [21] found that V_O as the dominant donor like native point defects in ZnO and well explains the unintentional n-type conductivity. They report on a study of oxygen self-diffusion by conceiving and growing oxygen-isotope ZnO heterostructures with delicately controlled chemical potential and Fermi level and found that the diffusion process predominantly mediated by V_O [21].

The electron mobility of intrinsic ZnO have been reported several times for bulk and nanostructures ZnO, although reported values can vary considerably. The transport properties in the literature are mostly based on Hall-effect measurements, assuming a unity scattering factor at room temperature and are in the range of 200 cm^2/Vs [12] for low fields. Initial Monte Carlo simulation reported by Albrecht et al. [22] predicted that the electron mobility of intrinsic ZnO at room temperature should be around 300 cm^2/Vs, which has been verified by further theoretical calculations yielding values around 285 cm^2/Vs - 300 cm^2/Vs [23][24]. It has also been reported that the electron mobility of undoped bulk and thin film ZnO at room temperature is between 120 cm^2/Vs - 440 cm^2/Vs with different fabrication methods used [12]. In contrast to bulk values, reported mobilities

for ZnO nanostructured are normally lower than 100 cm^2/Vs, although particularly high-quality samples can sometimes show mobilities in the range of 1000+ cm^2/Vs at room temperature [25]–[28]. Nevertheless, these are usually regarded as irregular, and some authors have challenged these results [29].

The typical background carrier concentration of high quality undoped ZnO is about 10^{16} cm^{-3} in the best case [30]. However, the number varies due to the quality of the fabricated ZnO bulk or the quality of the thin film. The highest reported carrier concentration for n-type doping ZnO is estimated to be 10^{20} cm^{-3} [17]. There have been reports of lower carrier concentration in ZnO thin film on the order of 10^{15} cm^{-3} in (0001) ZnO orientation [18] and 10^{14} cm^{-3} in $(10\bar{1}0)$ ZnO orientation [31]. Generally, carrier concentration increases as the growth temperature increases. High carrier concentrations mean the donor-like defects such as oxygen vacancies (V_O), zinc interstitials (Zn_I) and/or hydrogen are highly incorporated in the ZnO bulk/thin film [16]. It is widely accepted that the fabrication method of ZnO thin films is a main factor for determining the electrical properties of ZnO.

Table 2-1 shows the compilation of carrier concentration, electron mobility and resistivity obtained in nominally undoped bulk and thin film ZnO deposited on different substrates by various growth methods. It is observed in Table 2-1 that the ZnO growth method can significantly affect the electrical properties of the bulk/film. Based on the tabulated results, ALD is a particularly attractive technique due to its capability of depositing ZnO film at low temperature with considerably good electrical characteristics. Furthermore, ALD offers a good growth control of the thickness and the composition of the thin films. ZnO is expected to have a variety of applications in electronics due to its direct and wide band gap material. Benefits of a wide band gap include higher breakdown voltage, the capacity to tolerate a large electric field, high power operation and lower noise generation [12].

Table 2-1: Electrical characteristics of ZnO bulk and thin film from various literature [18], [33]–[41].

Reference	Growth Method	Carrier Concentration, cm^{-3}	Electron Mobility, cm^2/Vs	Resistivity, Ω cm
Guziewicz, E et al (2012)	ZnO thin film grown by ALD at low temp (100 °C -240 °C)	$4x10^{16}$ (100 °C) $1.5x10^{17}$(120 °C) $4X10^{18}$ (130 °C) $3x10^{19}$ (150 °C) $1x10^{20}$ (240 °C)	10	n/a
Nunes, P et al (2002)	ZnO thin film deposited by RF sputtering and annealed at 400 °C	$2x10^{18}$ -$1.6x10^{19}$	0.3-0.53	2 $x10^{-2}$
Wei, Xuecheng et al (2007)	Bulk ZnO grown by CVT	$1.135x10^{18}$ (1010 °C) $5.535x10^{17}$ (1020 °C) $1.47x10^{17}$ (1030 °C)	97 133 162	n/a
Maeda, Katsumi et al (2005)	Bulk ZnO single crystal by the hydrothermal method with Pt inner container at 300 °C - 400 °C	$8x10^{13}$	200	380
Zhaochun, Zhang et al (2001)	ZnO thin films deposited by MOVPE at 400 °C	1.73 $x10^{19}$	52.8	6.88 $x10^{-3}$
Fortunato, E.M.C et al (2005)	ZnO thin-film at room temperature by RF magnetron sputtering	3 $x10^{16}$	2.0	$<10^2$
Kwon, Semyung et al (2013)	ZnO thin film deposited by ALD	$1.7x10^{14}$(70 °C) $3.15x10^{15}$ (90 °C) $1.56X10^{17}$ (110 °C) $4.81x10^{19}$ (130 °C)	6.4 16.1 6.4 152.5	$5.52x10^3$ $1.23x10^2$ $7.1X10^{-1}$ $8.52x10^{-4}$
Nakahara, Ken et al (2001)	ZnO thin Films by Radical Source Molecular Beam Epitaxy	$7.6x10^{16}$	120	n/a
Nause, J and Nemeth, B (2005)	Bulk ZnO grown by pressurized melt method at 1450 °C	5.05 x 10^{17} (296K) $3.64x10^{16}$ (77K)	131 298	9.43 $x10^{-2}$ $5.77x10^{-1}$
Kishimoto, S et al (2006)	ZnO thin film deposited by plasma-assisted electron beam deposition at 200 °C	~ 10^{19}	5 to 35	10^{-2} to 10^6

2.5 Fabrication of ZnO nanowire field-effect transistor (FET)

One-dimensional (1D) ZnO are more fascinating since they exhibit the most diverse and rich configurations known hitherto discovered, such as nanowires, nanorods,

nanotubes, nanofibres, nanobelts and nanoribbons [42]. The aspect ratios (length to width ratio) of nanowires are typically of the order of >1000. In view of this, they are often referred to as one dimensional materials. The shift from zero dimensional particles to one 1D rods or wires leads to improved mobility and the potential for use in novel electronic and optical applications such as large area displays, transparent and invisible electronics, optical and UV sensors and solar cells etc.

A number of factors contribute to the research interest on ZnO nanowire-based FETs. One of the factors is, the nanowire structure has a higher carrier mobility as compared to other non- 1D nanostructures of similar size, due to its single crystalline structures that reduce carrier scattering [43]. Furthermore, the increasing need to make smaller device structures with enhanced functionality has attracted significant interest in ZnO nanowires-based FETs because of the high aspect ratio of nanowires [44]. Semiconductor nanowires can be prepared in high-yield with reproducible electronic properties as essential for large-scale integrated systems [45][46]. Finally, a nanowire has the ability to work both as interconnects and active devices. Hence it has the potential to offer two of the most critical functions in any integrated nanocircuitry [47].

In an attempt to utilize ZnO nanowires for electronic devices, it is crucial to develop reproducible methods to yield high quality ZnO nanowires. ZnO nanowires can be fabricated by various methods, which can be categorized as bottom-up or top-down (Figure 2.7). The bottom-up methods are the more common methods used in nanowire fabrication. Bottom-up processes gather molecules and small solid structures from atoms to produce a large variety of shapes and functions. In the top-down process, small features are “written” onto the material by a combination of different processes which are deposition, etching and lithography to form functional devices [48]. Top-down processes can provide nanowires in well-defined locations on a wafer and allows nanowires of various length to be fabricated on the same chip.

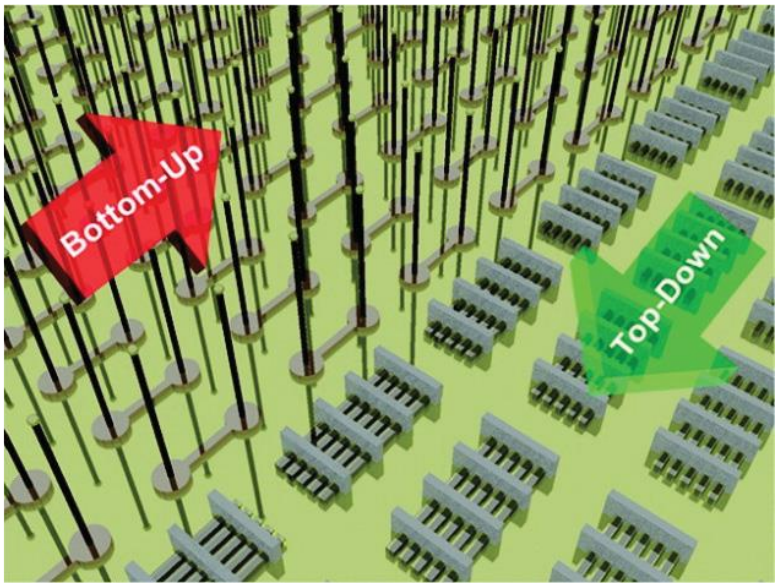


Figure 2.7 A sketch of top-down and bottom-up paradigm applied to nanowires fabrication. Figure reproduced from Ref. [49]

Well-known bottom-up processes for the synthesis of nanowires include the vapour-liquid-solid mechanism (VLS) [50][51], chemical vapour deposition (CVD) [52]–[55] or wet chemical synthesis [56]. Bottom-up grown ZnO nanowires fabricated by the methods mentioned above are typically produced as entangled meshes of nanowire. Figure 2.8 shows an SEM image of an entangled mesh of ZnO nanowire on the as-grown silicon wafer. Although bottom-up processes tend to fabricate high crystallinity, morphology and large aspect ratio of ZnO nanowires, the process can just randomly align the nanowires on the device substrate and lack the controlled synthesis to produce uniform dimensions of the nanowire. Consequently, due to these disadvantages, the bottom-up process does not provide feasible way for addressable nanowire FETs. Although some of the bottom-up techniques can produce a well-defined nanostructure, the fabrication cost of the bottom-up process is much higher than that of the top-down method [57]–[59]. The drawbacks of the bottom-up process can be solved by using top-down process [60].

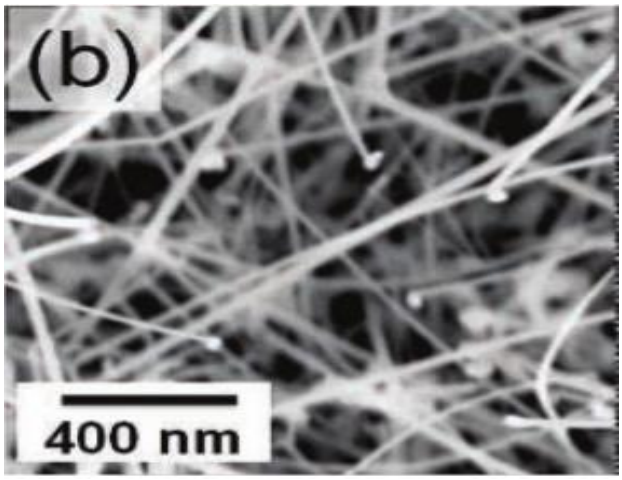


Figure 2.8 An SEM image of entangled mesh of ZnO nanowire. Figure reproduced from Ref. [50].

The lithography process is the most important process in top-down method for semiconductor device definition and placement. UV lithography is the standard industrial method in top-down methods. However, there has been a common trend toward a shorter wavelength radiation source to achieve higher image resolution [49]. Owing to the continued device scaling and increased device density, extreme ultraviolet (EUV) or X-ray lithography (XRL) may be required. Other lithography processes are also considered to extend lithography scaling beyond UV lithography capabilities, including electron beam lithography (EBL), focused ion beam (FIB), nanoimprint lithography (NIL) and deep ultra violet lithography (DUVL). EBL and FIB lithography are generally used for the fabrication of high-resolution photomasks and have the capability to pattern devices down to 5 nm, but the equipment is very expensive and the pattern writing is very slow. These methods are vulnerable and not currently amenable towards mass production.

For the low cost top-down fabrication method, optical stepper lithography seems to be the most suitable candidate. However these patterning techniques are not a direct method to pattern sub 100 nm features. Sidewall Transfer Lithography (STL) is a promising method to pattern sub-30 nm nanowire with high throughput achieved with stepper lithography [61]–[63]. In STL, lines are patterned by a combination of optical lithography and a spacer patterning process. In this technique, resist is patterned by optical lithography and etched anisotropically. A spacer is formed on the sidewall of the resist by conformal deposition and anisotropic etching. Figure 2.9 shows the SEM image of the ZnO nanowire fabricated by top-down fabrication using the spacer method. The STL method is a good alternative for shaping nanowire features using conventional and cost effective lithography. Moreover, this method is a good alternative to produce ZnO nanowires in

well-defined locations with controlled nanowire dimensions. The following section will discuss the electrical characteristics of the devices fabricated by bottom-up and top-down methods.

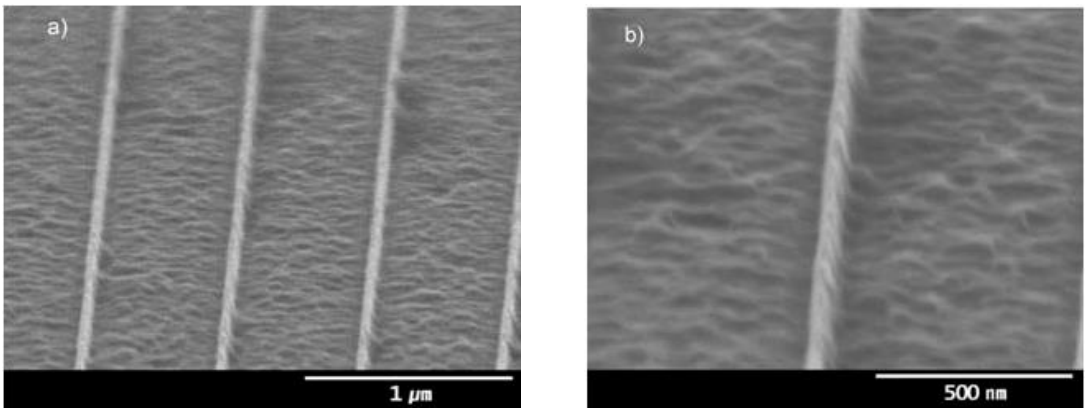


Figure 2.9 SEM image of ZnO nanowire fabricated by top-down fabrication using spacer method. Figure reproduced from Ref. [63].

2.5.1 Benchmarking the ZnO nanowire FETs

The main parameters of FETs are mobility, transconductance, subthreshold slope, on-state current, off-state current, threshold voltage, channel length etc. Higher mobility and shorter channel length will give higher on-state current and therefore higher device speed. The value of off-state current and threshold voltage describes the energy dissipation of the device. The increase of transconductance and the decrease of subthreshold slope indicate that the gate voltage has effective control on devices. There are specific target performance metrics to be considered as high performance FETs. Based on high performance transistor for CMOS reviewed by Franklin, the high performance transistor should have a low operating voltage of <1 V, high drive current of > 1 mA/ μm, and the channel length of < 20 nm [64]. However these characterisation are based on carbon nanotubes (CNTs), graphene, transition metal dichalcogenides (TMDs) and X-enes (e.g., phosphorene, silicone). In the case of ZnO based FETs, the performance could be lower as there are issues of material quality.

Figure 2.10 illustrates a comparison of 15 different ZnO nanowire FETs fabricated using various methods with difference gate configurations. The graph of field-effect mobility against subthreshold slope is plotted as both parameters are the prominent output characteristics of interest. High mobility is preferred for a high-speed device while low subthreshold slope is good for high performance device applications. Figure 2.10 shows

that the field-effect mobility is between 3 cm^2/Vs -117.34 cm^2/Vs subthreshold slope between 100 mV/decade -3000 mV/decade, I_{ON}/I_{OFF} ratio between $10^1 – 10^8$ and threshold voltage between -14.3 V – 22 V.

Due to nanowire crystallinity, bottom-up processes tend to acquire high field-effect mobility as compared to top-down process. However most of the bottom-up fabricated nanowires require additional treatment such as annealing and passivation to achieve desired electrical characteristics. Based on the survey, the highest field-effect mobility achieved by top-down process is 85.2 cm^2/Vs. Achieving a mobility of at least 80 cm^2/Vs with the top-down process is one of the inspirations for embarking on this project.

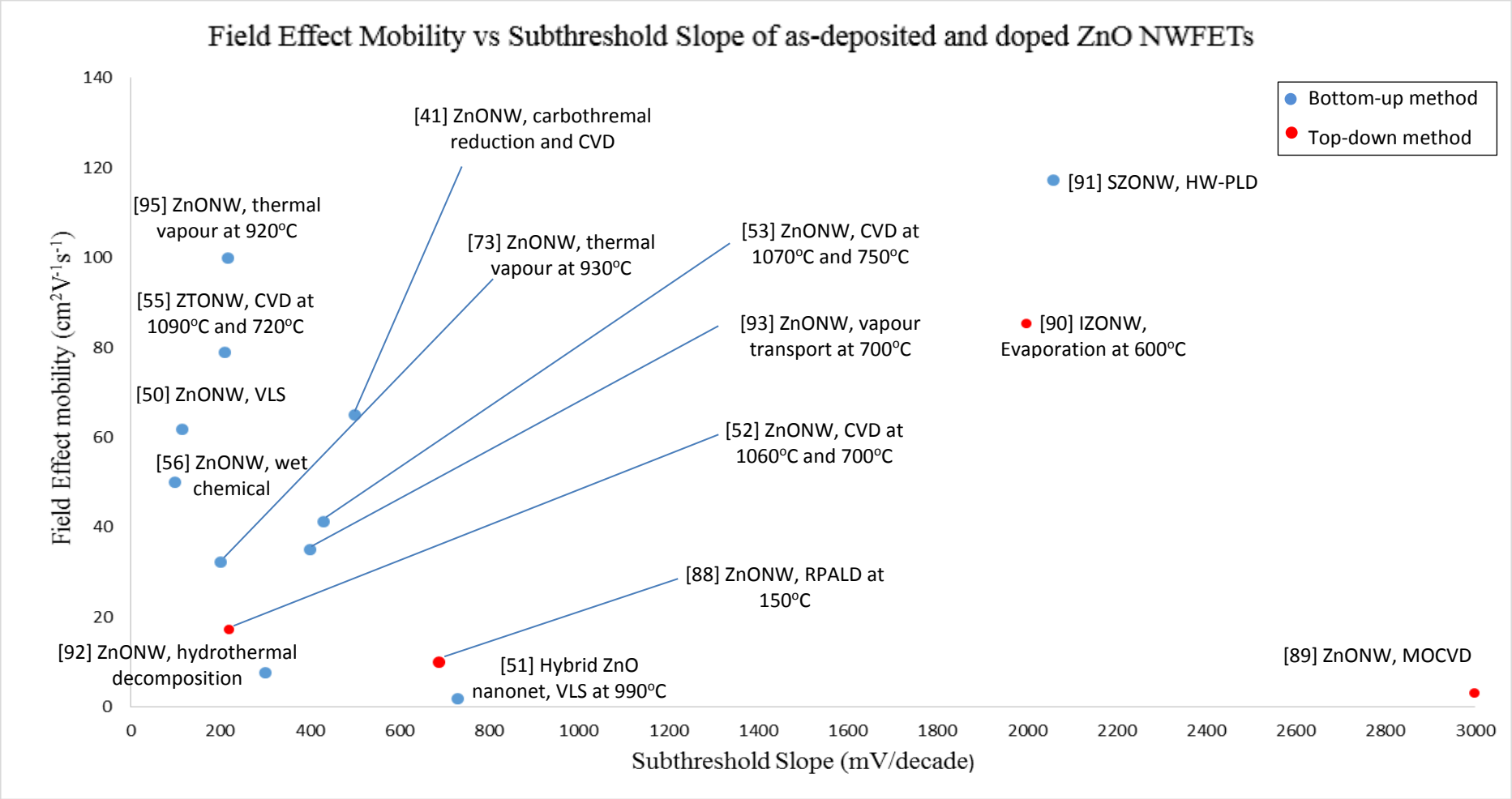


Figure 2.10 Survey on ZnO nanowires looking at field-effect mobility versus subthreshold slope.

Apart from nanowire, various ZnO structures have been used as a transistor that can produce high performance characteristics. Table 2-2 shows the characteristics of some of the published high performance ZnO transistors based on different structures.

Table 2-2 Review of high performance transistors based on various structures of ZnO.

References	ZnO Structures	Channel length [μm]	μ_{FE} [cm^2/Vs]	V_{TH} [V]	*SS* [mV/dec]	I_{ON}/I_{OFF}
Park et al. [65]	nanorod	5	1000		1040	10^4–10^5
Sanghyun et al [26]	nanowire	2	1175	0.2	150	10^6
Cheng et al.[65]	MgOZnO/ZnO heterostructures	n/a	84.2	-0.55	n/a	$2x10^6$
Burhan et al [66]	thin film	2	110	n/a	110	10^{12}
Hong et al. [67]	nanowire	3	88.2	-6.6	880	10^6
Zhang et al. [68]	nanobelt	n/a	90	0.25	360	10^5
Koike et al.[69]	$Zn_{0.7}Mg_{0.3}O$/ZnO heterostructure	50	140	-4.6	n/a	10^6

Based on the results tabulated in Table 2-2, ZnO material shows a promising potential of producing high performance FETs with high mobility, low threshold voltage of < 1 V, good subthreshold slope and high on/off current ratio. These values are significant and represent a real opportunity to realise high performance FETs based on n-type ZnO nanowires. Moreover shown a significant potential for high frequency electronics. The variation in the electrical performance is due to the different structures and post treatment of the ZnO. In addition, the ZnO have a large amount of surface defects, mainly oxygen vacancies, which absorb gas species and act as scattering and trapping centres [70]. These defects and chemical species have significant influences on the performance of ZnO devices. Park et al. have reported that a ZnO nanorod exhibited an electron mobility of 1000 cm^2/Vs after coating the nanorod with polymide [27]. Meanwhile, Ju et al. have demonstrated that the electron mobility of an ozone-treated single nanowire is up to 1175 cm^2/Vs. These results indicate the potential of ZnO nanostructure-based devices achieving a faster operation speed and improved performance after surface modification.

Table 2-3 Review of high performance transistors based on ZnO competing materials

References	Material/Structures	Channel length [μm]	μ_{FE} [cm^2/Vs]	V_{TH} [V]	*SS* [mV/dec]	I_{ON}/I_{OFF}
Tomioko et al. [71]	InGaAs nanowires	0.2	1170	0.38	75	10^8
Kang et al. [72]	Poly-Si TFTs	n/a	168	4.67	n/a	n/a
Ju et al. [73]	Mg-doped ZnO nanorods	2.2	13	-0.5	300	10^6
Wang et al. [74]	Poly-Si nanowires	0.8	346	0.35	n/a	10^9
Wong et al. [75]	a-Si nanowires	5	50	10	2500	10^5
Jiang et al. [76]	InAs/InP nanowires [76]	0.17	11500	-5	260	10^3
Crone et al. [77]	Organic TFTs	n/a	0.02	n/a	n/a	n/a

Result tabulated in Table 2-3 shows other competing materials to ZnO nanowires. Poly-silicon and amorphous-silicon are widely used in display applications [72][74][75], but their high-temperature process needed for their production or limited application to large substrate limits their utility in high performance transistor for future display and high speed logic circuit applications. In addition, emerging organic-semiconductor-based [77][78] are also limited by high process temperature or low carrier mobility. These limitations imposed by materials and/or substrates process temperatures restricting the device to operate in high performance applications such as high speed logic circuits and next generation display applications. Studies of ZnO transistors have reported high performance transistor characteristics rivalling or defeating those of amorphous-silicon and poly-silicon, especially for μ_{FE} and subthreshold slope [26][79]. The use of ZnO materials also allows low-temperature device processing, which essential for applications such as circuits fabricated on plastic substrates.

Recently, ZnO has been considered a good candidate for display electronics applications [80]. ZnO became a promising semiconductor material for transparent transistor and FETs applications because of its wide band gap of 3.4 eV and its high thin film electron mobility [12]. In addition, ZnO thin film can also easily be prepared by several deposition techniques. ZnO-based FETs have been shown to be suitable for high

performance circuit applications beyond display electronics because of their superior electronic properties [80]–[82]. Some of these applications include high-speed logic circuits, high speed control electronics and RF applications [66][80][82][83].

In order for ZnO-based FETs to be applied in RF and logic circuit applications, the device should demonstrate high subthreshold swing gradient, high on-off current ratio, output drain current at low drain bias and high mobility. Bayraktaroglu et al. [80] demonstrated high-frequency ZnO TFT with power gain cut-off frequencies of f_T = 2.45 GHz and f_{max} = 7.45 GHz, respectively. The device exhibited a subthreshold swing of 200 mV/decade, on/off current ratio of 5 x 10^{10}, threshold voltage of – 0.6 V and field-effect mobility of 68 cm^2/Vs. This demonstrated that a ZnO-based transistor could be applied in RF applications and logic circuit applications. In another publication, Cho et al. [84] presented electrical characteristics of single ZnO nanowires at high-frequency range. The device shows a subthreshold swing of 1 V/decade, field-effect mobility of 74 cm^2/Vs, and on/off current ratio in the range of 10^4-10^5. Their investigation found that the ZnO nanowire RF device transmission characteristic of S_{11} is less than 10 dB, and S_{12} ranges between -20 dB and -40 dB. They suggested that research regarding contact resistance is needed to improve transmission and improve the adaptability of RF device using ZnO nanowire [84].

Frenzel et al. [85] have demonstrated that ZnO metal-semiconductor FETs technology is suitable for creating ICs. They fabricated a ZnO-based integrated inverter consisting of normally-on metal-semiconductor FETs and Ag_xO Schottky diodes as level shifters. The inverters show high gain values up to 197 at 3 V operating voltage and low uncertainty levels in the range of 0.13 V. Park et al. [86] have demonstrated a dual gate ZnO-based TFT for NOR gate application. As characterized with the double gate and the ground plane mode, their ZnO TFTs with a double layer of Al_2O_3 are operated at a gate voltage below 5 V. The device showed a field-effect mobility of 0.38 cm^2/Vs, on/off current ratio of ~10^6, and high saturation current of 6 µA.

Although much effort has been given to fabricate a ZnO device with various device configurations and structures, the electrical performance of ZnO device still shows significant variation. This highlights the issue of material quality and fabrication techniques. Among other ZnO nanostructure, nanowires have been the most extensively studied due to their remarkable electrical performance in FETs. This work focuses on ZnO nanowires as they have obtained decent mobility values compared to other ZnO structures.

This work aimed to demonstrate top-down fabrication of ZnO nanowires as this approach will give a controlled of dimensions and alignments of nanowires. It also allows the FETs design with different channel length. Remote plasma enhanced atomic layer deposition (RPALD) is seen as the best candidate for a top-down process because it allows for a good control of carrier concentration and resistivity [87]. Based on [88], this method shows a potential of producing high performance FETs by achieving field-effect mobility >10 cm^2/Vs with excellent crystallinity. This work also will focus on improving the electrical characteristics of ZnO nanowire FET by solving the issues relating to contact resistance and surface roughness.

2.6 Conclusion

In summary, the fundamental nanowire FET parameters used to characterise ZnO nanowire FETs have been described. This chapter also discusses the regions of operation of the nanowire FETs which are depletion and accumulation. The drain current equation has been derived within the linear and saturation regions. Based on the literature review, ZnO has emerged as a promising semiconductor for a wide variety of electronic applications because of its good characteristics. It has a wide and direct bandgap of 3.4 eV, large free-exciton binding energy of 60 meV which is significantly higher than ZnSe (22 meV) and GaN (25 meV). One distinct feature of ZnO compared to other materials is the potential of producing high quality devices with low temperature processes using conventional methods making it suitable for low cost mass production. It has also shown that the ZnO nanowire FETs have superior performance such as excellent mobility and high crystalline quality. Therefore, there is great promise to produce a high performance device at low temperature based on ZnO material using a top-down process. However, the electrical performance of the ZnO nanowire FETs showed significant variation especially in field-effect mobility. Therefore, this work aimed to tackle several issues aiming to increase the electrical performance of the ZnO nanowire FETs using a top-down fabrication method, such as surface roughness and contact resistance. The top-down approach involves the use of the RPALD process to deposit a high quality ZnO layer and a spacer method to fabricate the nanowires. This work aimed to achieve depletion mode nanowire FET with field-effect mobility of at least 80 cm^2/Vs, a subthreshold swing of at least 200 mV/ decade, threshold voltage between -5 V to 5 V and an on/off current ratio of $\sim 10^6$ that is suitable for RF and logic circuit applications.

2.7 References

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Chapter 3:
Theoretical Background

This chapter discussed the extraction method of the electrical characteristics of the ZnO nanowire FET such as threshold voltage, subthreshold slope, and field-effect mobility and verify these measured values with calculation based on analytical model. The FETs fabricated in this project were characterized by electrical measurements. The interpretation of the obtained electrical data is based upon a theoretical framework that has been discussed in Chapter 2. The concept presented here relies mainly upon the standard MOSFET textbook approach [1], but has been slightly altered because ZnO nanowire FETs operate in depletion mode. This chapter also describes the modelling of ZnO thin film and simulation of the model.

3.1 ZnO Nanowire FET Electrical Characteristics

Based on the equation derived from current-voltage relationship, it is possible to extract important FET parameters. These parameters are the transconductance, the field-effect mobility and the subthreshold swing. These parameters are useful for evaluating the performance of an FET compared to other FETs fabricated with different technologies. In this section, the fabricated ZnO nanowire FET electrical characteristics such as oxide capacitance, threshold voltage and field-effect mobility will be discussed. Figure 3.1 shows the cross section view of the nanowire FET fabricated for this study. Based on the scanning electron microscope cross section, the nanowire is considered to have a triangular shape cross-section. The ZnO nanowire FET has the dimension of 100 nm in width at the base, *b*, 208 nm in height, *c* and 8.6 μm in channel length. The thickness of the SiO_2, *d* grown by thermal oxidation is 100 nm.

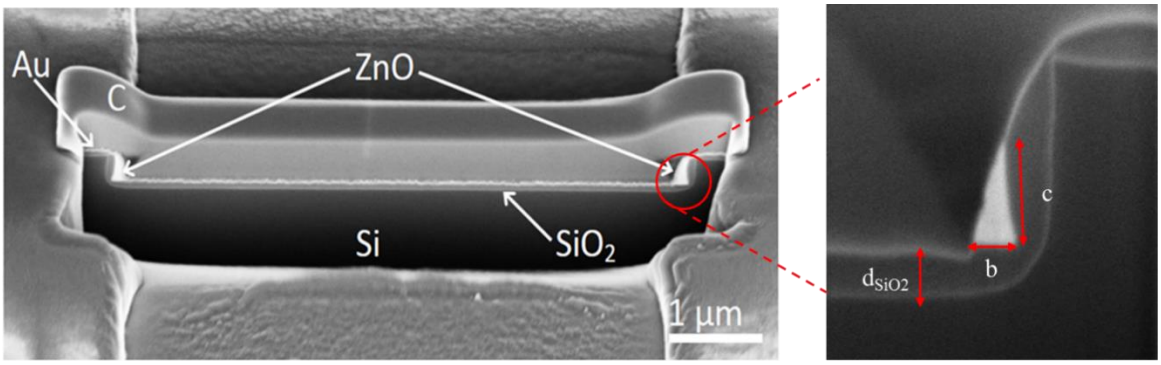

Figure 3.1 Cross-sectional view of the ZnO nanowire.

3.1.1 Oxide Capacitance

The oxide capacitance of the nanowire FET usually determines by metallic cylinder on an infinite model [2]–[4]. The cross section geometry and the equipotential lines of this model are shown in Figure 3.2. Based on this model, the nanowire is assumed to be completely embedded in the dielectric and possess a circular cross section. Wunnicke [2] was revised this assumption and it will be presented in this section based on the fabricated nanowire FETs with a triangular shape.

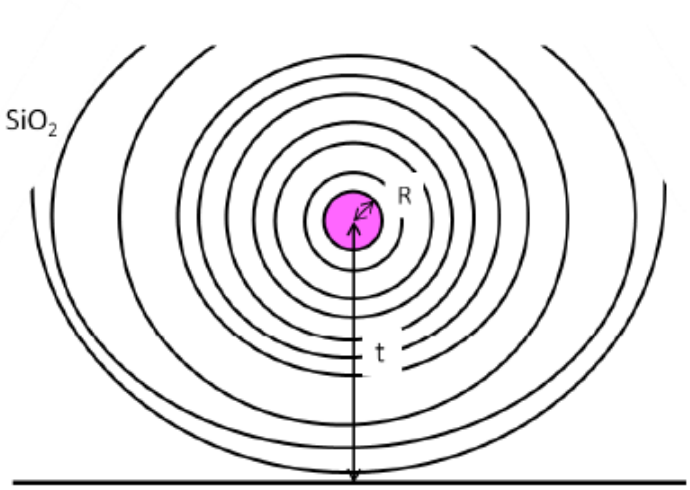

Figure 3.2 Cross section geometry of back-gated NWFETs of embedded NW with t/R =6. The lines are equally separated constant potentials obtained by finite element method (FEM) calculations. Figure reproduce from [2].

Oxide capacitance per unit area of the FET simply given by ε_o/d. The oxide capacitance of the nanowire FET per unit length based on Wunnicke [2] model can be expressed as:

$$\frac{C}{L} = \frac{2\pi\varepsilon_o\varepsilon_r}{\cosh^{-1}\left(\frac{t}{R}\right)} \tag{19}$$

Where the ε_r is the dielectric constant of the embedding dielectric, t is the distance between the metal plate and the centre of the cylinder and R is the radius of the cylinder. For x=t/R>>1, the approximation of $\cosh^{-1}(x)$ is given by $ln\left(x-\sqrt{x^2-1}\right) \approx \ln(2x)$. Therefore, from Eq. 19, the capacitance can be written as:

$$\boxed{C = \frac{2\pi\varepsilon_o\varepsilon_r L}{ln\left(2\frac{t}{R}\right)}} \tag{20}$$

Based on the nanowire structure in Figure 3.1, $t = \left(100 + \frac{c}{2}\right) nm$ where $c = 208\, nm$, so $t = 204\, nm$. If the width of the nanowire is taken as the radius, $R = \frac{W}{2} = 50\, nm$. Since $\frac{t}{R} \gg 1$ thus Eq. 20 can be used in order to calculate the gate capacitance in this study.

Eq. 20 is often used to calculate the gate capacitance in typical bottom-gate nanowire FET geometries based on the metallic cylinder on an infinite metal plate model [2]. However, if taking the case of non-embedded nanowire FETs into account, the dielectric constant for SiO_2, $\varepsilon_r = 3.9$ is inaccurate with Eq.20. Therefore, in this study uses the effective dielectric constant of $\varepsilon_{r,eff} = 2.65$ calculated for the triangular shape nanowire on SiO_2 [3]. From Eq. 20, capacitance is then calculated to be 0.59 fF.

Due to the derived nanowire FET capacitance, the drain current (Eq.15 and Eq.16) equation needs some modification. Capacitance per unit area is given by:

$$C_{ox} = \frac{C}{LW} \tag{21}$$

Substituting Eq.21 into Eq.20, yields:

$$C_{ox} = \frac{C}{LW} = \frac{2\pi\varepsilon_o\varepsilon_r}{W ln\left(2\frac{t}{R}\right)} \tag{22}$$

3.1.2 Threshold Voltage, V_{TH}

There are many different specific definitions of the threshold voltage, and several different techniques are used to extract the threshold voltage from multiple types of measurements [6]. In this study, the V_{TH} is extracted from extrapolation in the linear region of the I_{DS}-V_{GS} curve. It includes the V_{GS} axis intercept when $I_D = 0$ of the linear extrapolation of the I_{DS}-V_{GS} curve [6]. The point of intersection is then taken to be the threshold voltage. Based on Eq. 6, when $I_D = 0$,

$$I_D = (V_G - V_{TH})V_D = 0$$

$$\therefore\ V_{TH} = V_G$$

The threshold voltage is extracted from the linear curve of I_{DS}-V_{GS}. The magnitude of the threshold voltage is affected by the carrier concentration of the ZnO nanowire channel. A high carrier concertation means that the device operates in depletion mode, requiring a

negative threshold voltage to deplete the electrons. A lower threshold voltage requires switching between on and off states for higher carrier concentrations of a ZnO nanowire channel. Likewise, if the carrier concentration of the ZnO nanowire is low, and the device is off at V_G = 0 V, then the device operates in enhancement mode, with a positive threshold voltage inducing electrons into the channel through Schottky band bending. Lower carrier concentrations necessitate higher threshold voltages to fill the channel with electrons. The threshold voltage of the device is also affected by other aspects of the channel, for example the surface states at the semiconductor or dielectric interface [1].

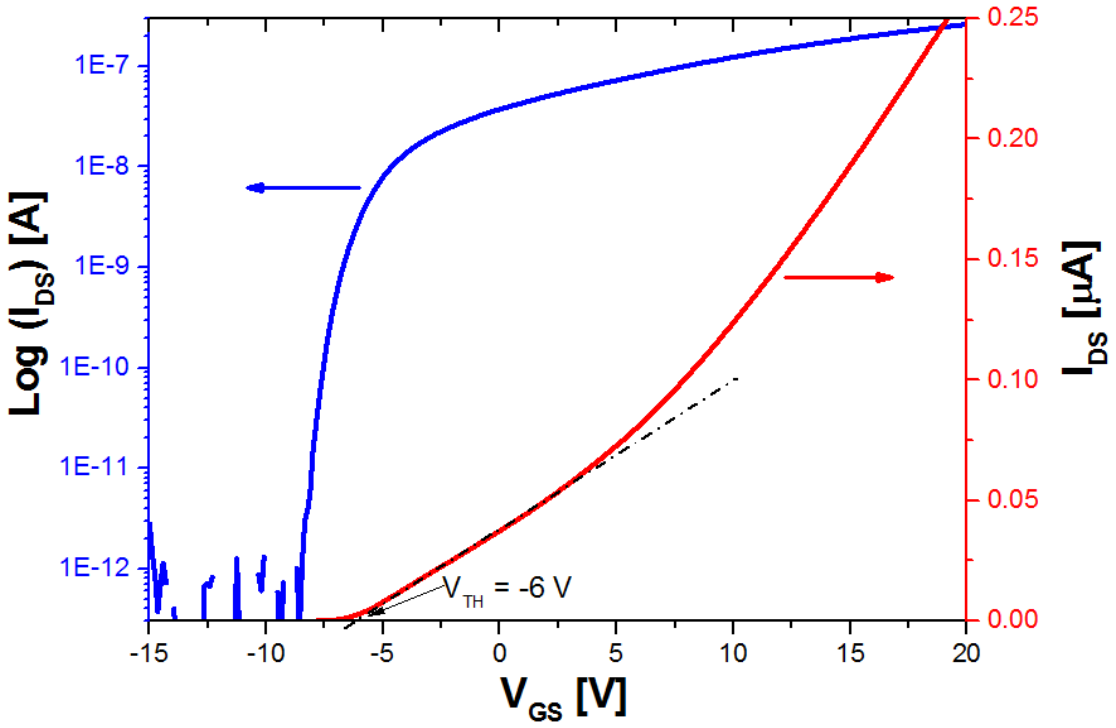

Figure 3.3 I_{DS}-V_{GS} curve at V_{DS} = 1 V of ZnO nanowire FET with channel length, L=8.6 μm. Linear curve (red) and subthreshold characteristics (blue).

Figure 3.3 shows the I_{DS}-V_{GS} curve of a fabricated ZnO nanowire FET in linear and semi-logarithmic scales at V_D = 1 V plotted on a linear scale and restricted to V_G = -15 V to 20 V. A linear line (black) is extrapolated from the linear portion of the transfer characteristics, and intersects the V_G axis at ≈ -6 V, which is taken to be the threshold voltage. This device operates in depletion mode, as it is in the on regime at V_G = 0 V.

In order to verify the measured V_{TH}, Eq. 12 in Chapter 2 is used to calculate the V_{TH}.

$$V_{TH} = V_{FB} - \frac{qN_D W_m}{C_0} - 2\Psi_B$$

where

$$\Psi_B = \frac{kT}{q}\ln\frac{N_A}{n_i}$$

The fabricated ZnO nanowire FET have the carrier concentration, N_A = 1 x 10^{18} cm^{-3} and the intrinsic concentration, n_i of ZnO is about 1 x 10^{14} cm^{-3} [4]. Therefore,

$$\Psi_{B\,(ZnO)} = 0.0026\,(\ln\frac{10^{18}}{10^{14}})$$

$$\Psi_{B\,(ZnO)} = 0.24\,V$$

The flatband voltage of the device is calculated based on Eq. 1 in Chapter 2.

$$V_{FB} = q\emptyset_{ms} = q\emptyset_{si} - q\emptyset_{ZnO}$$

$$V_{FB} = 4.85 - 4.45$$

$$V_{FB} = 0.4\,V$$

The depletion voltage can be obtained by:

$$V_{DEP} = \frac{qN_D W_m}{C_0} \tag{23}$$

Where W_m is the maximum width of the surface depletion region and it is given by:

$$W_m = 2\sqrt{\frac{\varepsilon_{ZnO}\varepsilon_o kT ln\frac{N_A}{n_i}}{qN_A}} \tag{24}$$

$$W_m = 2\sqrt{\frac{8.12\ \times 8.85\times10^{-14}\times 0.026\times ln\frac{10^{18}}{10^{14}}}{1.6\times10^{-19}\times10^{18}}}$$

$$W_m = 2.07\times10^{-6}cm$$

By substituting W_m into Eq.23

$$V_{DEP} = 4.84\,V$$

Therefore,

$$V_{TH} = 0.4 - (2\times0.24) - 4.84 = -4.92\,V$$

The calculated V_{TH} value differs from the measured value by 34% which indicates Eq.9 is valid to determine the V_{TH} for the fabricated ZnO nanowire FET device.

3.1.3 Subthreshold Swing, *SS*

From Figure 2.5 *IDS-VGS* curve in linear (blue) and semi-logarithmic scale of *IDS.SS* is measured to be 800 mV/decade. In order to verify this measured value, Eq.18 is used. By substituting Eq.14 into Eq.18 yields:

$$SS = 2.3\frac{kT}{q}\left(1 + \frac{C_{DEP}}{C}\right) V/decade \tag{25}$$

Based on Eq.25, the calculated subthreshold swing is 750 mV/decade. The calculated value differ from measured value by 7% which indicated that Eq. 25 is valid to calculate the *SS* of the device in this work.

3.1.4 Transconductance

The FET transconductance is defined as the change in drain-source current with respect to the corresponding change in gate voltage. More specifically, it is taken as the first derivative, $\frac{\partial I_D}{\partial V_G}$, of the transfer curve. The transconductance is normally taken as the maximum value of the derivative. In the linear region, Eq.7, the transconductance, g_m can be written as [8]:

$$\boxed{g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=constant} \cong \frac{W}{L}\mu_{FE}C_{ox}V_D} \tag{26}$$

In saturation region, the transconductance is a linear function of V_G and independent of V_D. The transconductance can be obtained from Eq.8:

$$\boxed{g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=constant} = \frac{W\mu_{sat}\varepsilon_{ox}}{dL}(V_G - V_{TH})} \tag{27}$$

Figure 3.4 shows the linear curve of I_{DS}-V_{GS} plotted alongside its first derivative on a linear scale, plotted from V_G = -10 V to 0 V. the maximum transconductance (g_m) is approximately 5.9 nS.

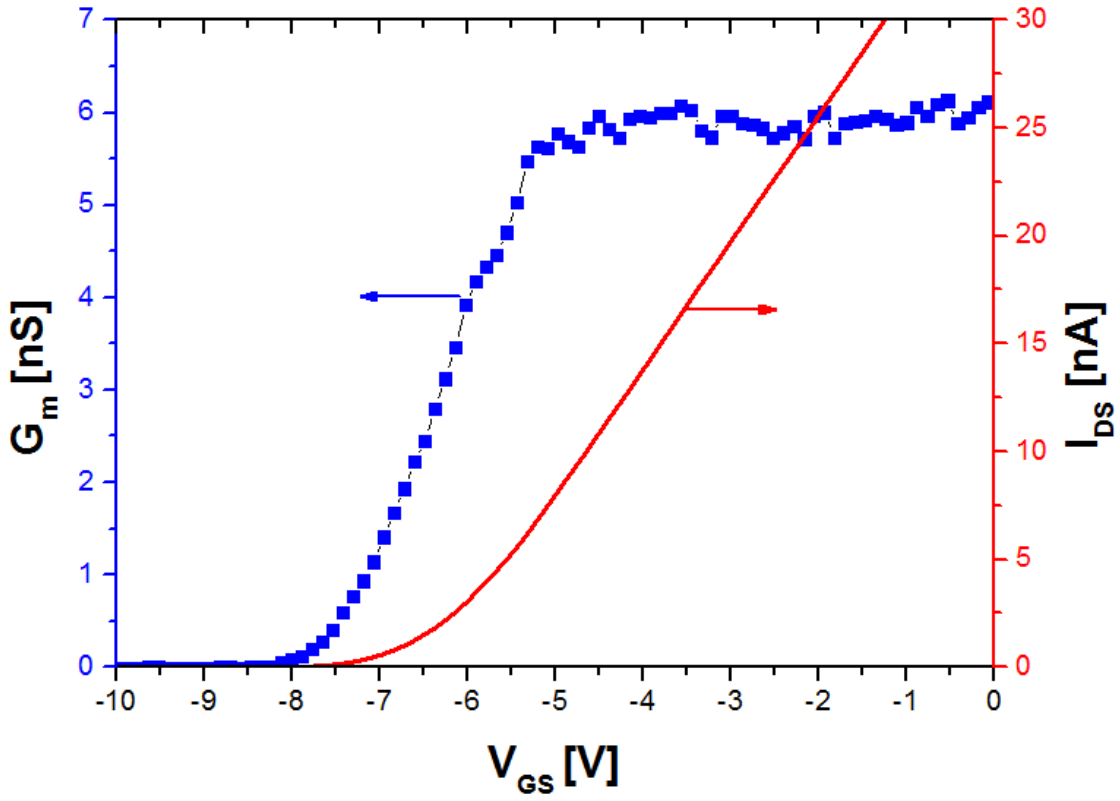

Figure 3.4 I_{DS}-V_{GS} curve (red) and resulting transconductance (blue) at V_{DS} = 1 V.

3.1.5 Field-Effect Mobility, μ_{FE}

Field-effect mobility is a measure of the mobility of the charge carriers in the semiconductor. It reflects how fast charge carriers can travel through the semiconducting material, and is adversely affected by electron scattering from various sources. Since ZnO is typically an n-type semiconductor, the mobility estimates are usually restricted to electrons. It is regularly used as a figure of merit when investigating the transistor properties. A high mobility value indicates the fast switching time of the transistor from the on-state to the off-state. Field-effect mobility, μ_{FE} is derived from the transconductance [1][9]–[11];

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=constant} \cong \frac{W}{L}\mu_{FE}C_{ox}V_D$$

From the relationship of Eq. 26, μ_{FE} can be expressed as;

$$\boxed{\mu_{FE} = \frac{Lg_m}{WC_{ox}V_D}} \quad (28)$$

Where g_m is the transconductance of the FET, L is the length of the channel, W is the width of the channel, V_D is the source-drain voltage and the C_{ox} is the capacitance of the FET.

Extraction of the field-effect mobility thus depends on accurately knowing the exact channel width and length, and calculating the capacitance of the device. For instance, the transconductance curve in Figure 3.4 shows the maximum g_m of 5.9 nS. Referring to the fabricated ZnO nanowire with the width, W = 100 nm, length, L = 8.6 µm. From Eq. 28, the μ_{FE} is calculated to be 7.41 cm^2/Vs. Nevertheless, the fabricated devices consist of dual nanowires as shown in Figure 3.1. Hence the μ_{FE} for a single nanowire device is 3.71 cm^2/Vs. The field-effect mobility is lower than bulk mobility probably because of the scattering at the surface of the channel and the existence of the contact resistance. In order to improve the field-effect mobility of the transistor, the surface roughness and interface quality between ZnO and SiO_2 need to be improved.

In order to verify the measured mobility with theory, I_{DS} is calculated based on μ_{FE} of 7.41 cm^2/Vs and Eq. 7 from Chapter 2. Figure 3.5 shows the I_{DS}-V_{GS} curve of the measured device and calculated I_D. The maximum percentage difference between measured and calculated I_D is 42%. This indicates that the field-effect mobility obtained based on modelled capacitance is valid for the ZnO nanowire FET in this study.

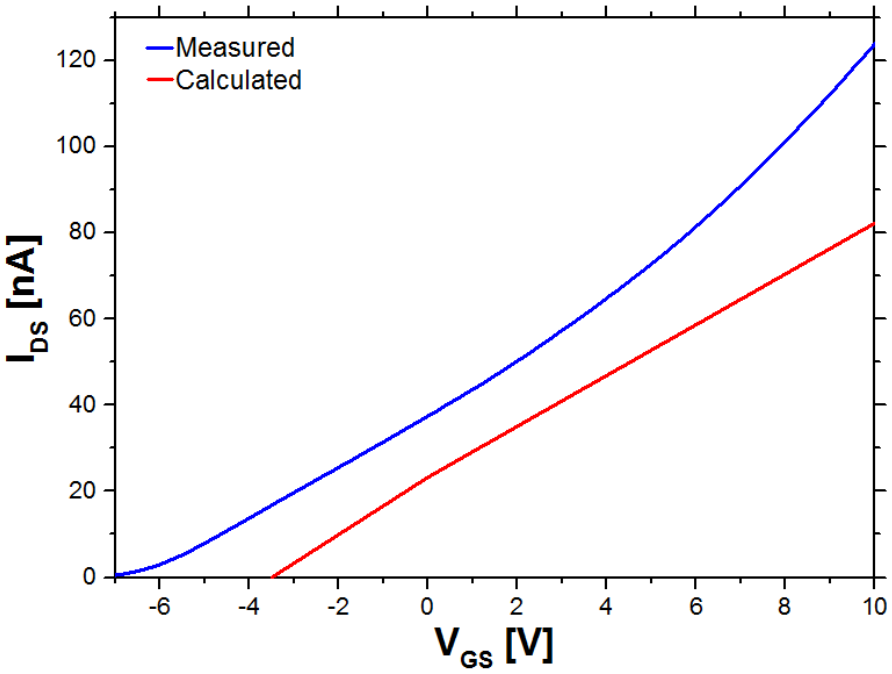

Figure 3.5 Linear I_{DS}-V_{GS} curve of measured (blue) and calculated (red) ZnO nanowire FET at V_{DS} = 1 V.

3.1.6 On/Off Current Ratio

The transfer characteristic plotted in semi-logarithmic scale as shown in Figure 3.3 also gives access to on/off current ratio. The on/off current ratio is the ratio between the maximum drain current in the on-state to the minimum drain current in the off-state. The ratio describes the ability of the device to switch the signal from 'on' to 'off'. From Figure 3.3, the on/off current ratio of the fabricated devices is approximately 10^6 at V_{DS} = 1 V.

3.2 Comparing ZnO TFT Simulation with Sultan Experiment

Device simulations are the fundamental tool for studying and forecast the device performance before fabrication process. In this study, device simulation was done using SILVACO products and tools. Simulation of the device starts by modelling the n-type depletion mode ZnO TFT. The TFT model is the best candidate to model nanowire as from the channel point of view in 2D, thin film and nanowire cross section appearance are similar. Table 3-1 shows the parameters used in modelling n-type depletion mode ZnO TFT from Ref. [12]–[14]. The simulated devices had the optimised dimensions with channel length, L=8.6 µm, channel layer thickness, t_{ZnO}=100 nm and gate insulator thickness, t_{SiO2}=100 nm.

Table 3-1: Material parameters (constants) of ZnO thin film for 2D device simulation

Material Constants for ZnO	**Values**
Bandgap, E_g (300K) (E_c-E_v)	3.4 eV
Electron affinity, χ ($E_{vac} - E_c$)	4.29 eV
Work function, ϕ_s ($E_{vac} - E_f$)	4.45 eV
Dielectric constant, ε_{ZnO}	8.12
Hall mobility, μ_H	150 cm^2/Vs
Donor level, (E_c-E_d)	30 meV

After modelling the n-type depletion mode ZnO TFT, further 2D simulation is carried out to compare the ZnO TFT simulation results with Sultan [15] ZnO nanowires experiments. All simulations carried out in Silvaco Atlas are 2D simulation to compare with the experiment result because it faster and simpler than 3D simulation. 2D simulation can generate results in faster time when device parameters are changed and varied. The field effect mobility of experimental results is 10 $cm^2/V{\cdot}s$ at a drain voltage of 1 V and threshold voltage of 24 V. The experimental device is fabricated using a top-down process

utilised remote plasma ALD and anisotropic inductively coupled plasma (ICP) etching as a method of growth at temperature of 190 ^{o}C, RF power of 100 W and a pressure of 15 mTorr. Table 3-2 shows the physical parameters that are used to define the ZnO TFT model. The simulation parameter is defined the same as the experimental device [15]. The donor concentration for the nanowire is more defined as it is measured experimentally to be between 2.0 x10^{16} cm^{-3} to 3.0 x10^{16} cm^{-3}. The silicon substrate doping is derived from the p-type Si wafer resistivity of 10 Ω.

Table 3-2 Parameter used for ZnO TFT simulation.

No.	Physical Parameter	DevEdit and Atlas Simulation Work Done	Suhana's Experiment	Units
1.	Nd=carrier concentration	2.17 x10^{16}	2.0 x10^{16} to 3.0 x10^{16}	cm^{-3}
2.	Si substrate doping	1.32 x10^{15}	1.32 x10^{15}	cm^{-3}
3.	Length of channel, L	8.6 x10^{-4}	8.6 x10^{-4}	cm
4.	Thickness of channel, t_{ZnO}	3.6 x10^{-6}	3.6 x10^{-6}	cm
5.	SiO_2 thickness, t_{SiO2}	1.0 x10^{-5}	1.0 x10^{-5}	cm
6.	Si substrate thickness	7.0 x10^{-5}	7.0 x10^{-5}	cm

Figure 3.6 shows the initial transfer characteristics of ZnO TFT using default parameters derived from literature. There are no defects introduced on oxide and channel layer at this point. Simulation results show high current and low resistivity. It also shows that the steep subthreshold slope of 65 mV/decade. However, the experimental curve shows low current, high resistivity and poor subthreshold slope (1500 mV/decade). Based on the experimental curve, the fabricated device exhibited n-type enhancement mode operation which it should be in depletion mode operation.

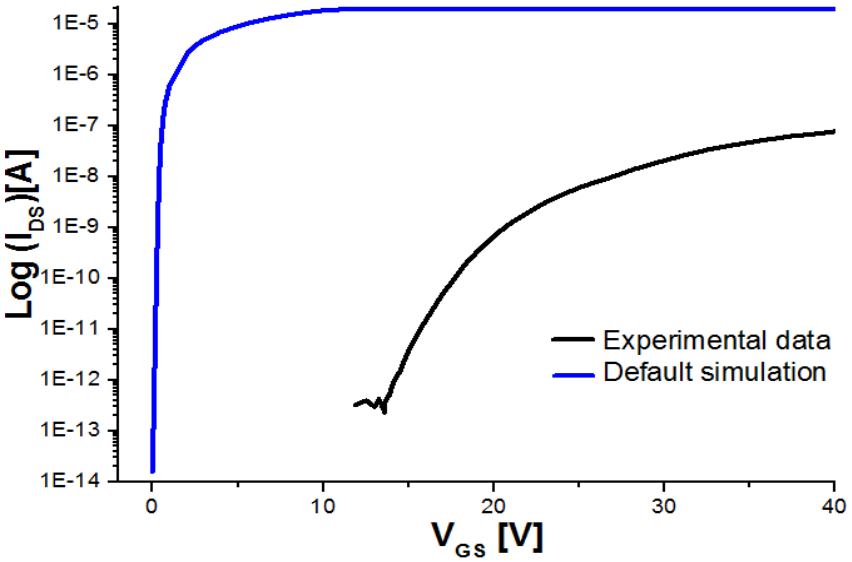

Figure 3.6 Initial simulation using default parameters derived from literature [12]-[14]

The dissimilarity in currents, resistivity and subthreshold slope in simulation and experimental device could be due to the defects. The oxide fixed trapped charge (Q_f), the interface state trapped charge (Q_{it}) and the contact resistance are suspected to contribute towards the dissimilarity of the initial simulation (default parameters) from the experimental curve.

The investigation started with the introduction of the oxide fixed trapped charge. Figure 3.7 shows the I_{DS} (log) versus the V_{GS} graph investigating the effect of oxide fixed trapped charge. In order to match the experimental graph, Q_f is varying from -3.95x10^{12} cm^{-2} to 3.0x10^{10} cm^{-2}. The Q_f mainly affect the threshold voltage by increasing the value to become more negative. The threshold voltage shift in a positive direction as Q_f become more negative. The threshold voltage matches the experimental curve at Q_f = -3.02 x10^{12} cm^{-2}.

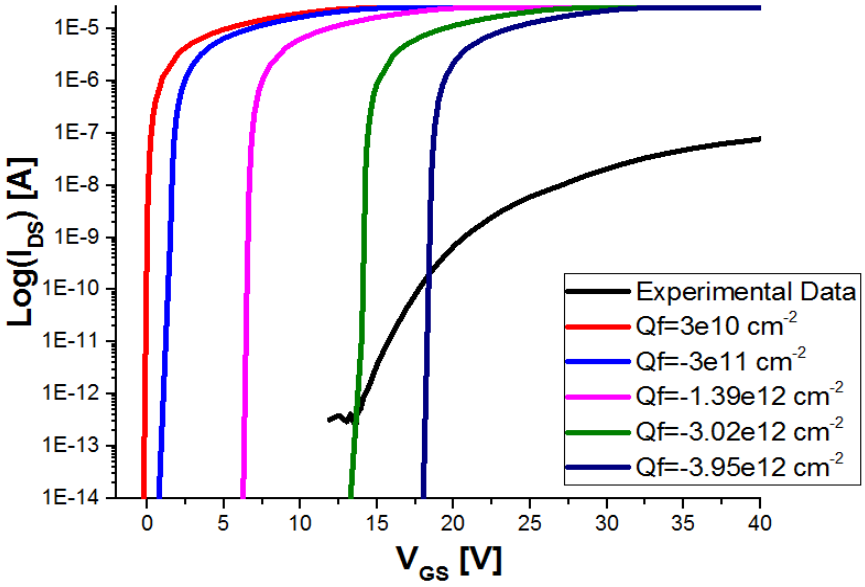

Figure 3.7 Subthreshold plot- Investigating the effect of interface charge

Next, the contact resistance is introduced in the simulation. Contact resistance has a substantial influence on the electrical characteristics of the device. It decreases the voltage across the channel, the field effect mobility as well as limits the maximum on current. The total TFT resistance is given by

$$V_{DS} = I_{DS}R_{total} = I_{DS}[R_{channel} + R_{contact}] \quad (29)$$

Where:

V_{DS} is the measured drop voltage between source and drain.

I_{DS} is the current across the drain and source.

$R_{contact}$ consist of ohmic and non-ohmic components.

$R_{channel}$ is the resistance within the ZnO channel layer.

The TFT or nanowire channel resistance exhibits purely ohmic behaviour in the linear region while the contact resistance exhibits ohmic and non ohmic behaviour. The presence of non-ideal conditions at the interface between metal and semiconductor cause the non ohmic behaviour.

The effect of the contact resistance is investigated by varying the resistance value from 10 Ω to 50 MΩ. It can be observed from the graph that the current in decreased as the resistance value increased. Figure 3.8 shows that the current of simulation curve match with the experimental data at R= 8 MΩ for ohmic contact resistance.

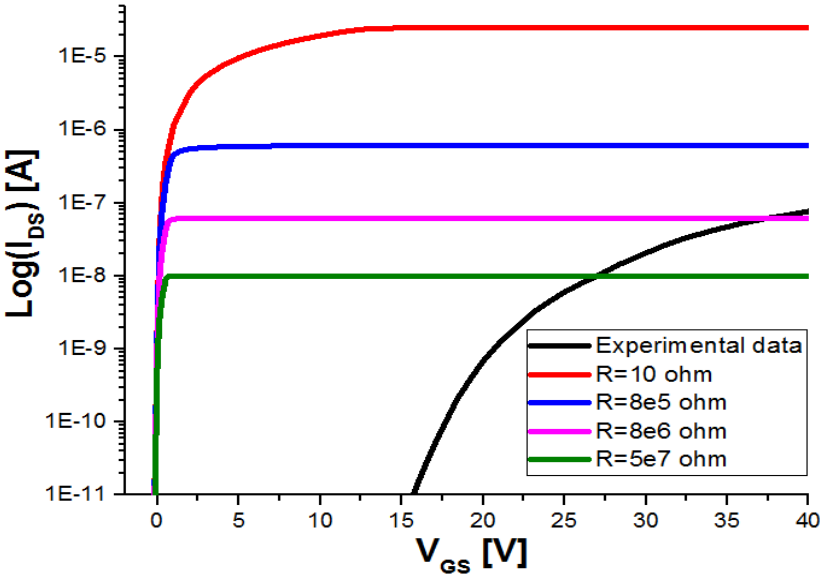

Figure 3.8 Subthreshold plot- Investigating the effect contact resistance

After introducing the Q_f and Q_{it}, the simulation model still have a steep subthreshold slope as compare to the experimental curve. There is a need to alter the simulation model in order to match the subthreshold slope. It must be noted that the experiment carried out by Sultan [15] is assumed to fabricate a single crystal ZnO channel layer. However, based on the simulation work done, the experimental device not shown a single crystal characteristic. The design of experiment (DoE) and remote plasma ALD are not optimised to produce epitaxial active channel layer. Although it can deposit single layers of material on top of another material, the single lattice is not confirmed to be matched.

To further investigate the reason of the experimental device has low current and shallow subthreshold slope, the surface charge at the ZnO channel layer are introduced. In the simulation, the surface charge between the ZnO channel and air, interface charge between ZnO channel and insulator and Q_f was included. The Q_f was set as default of $3x10^{10}$ cm^{-2} while the surface charge of the ZnO and interface charge between ZnO and the insulator I is varied from $-3.95x10^{12}$ cm^{-2} to $3.0x10^{10}$ cm^{-2}. Figure 3.9 shows the effect of surface charge in the simulation. In this simulation, contact resistance and Q_{it} is set to be zero. The surface charge causes the shift of the threshold voltage and lower the current at saturation region by a small amount of $6.3\ x10^{-5}$ A.

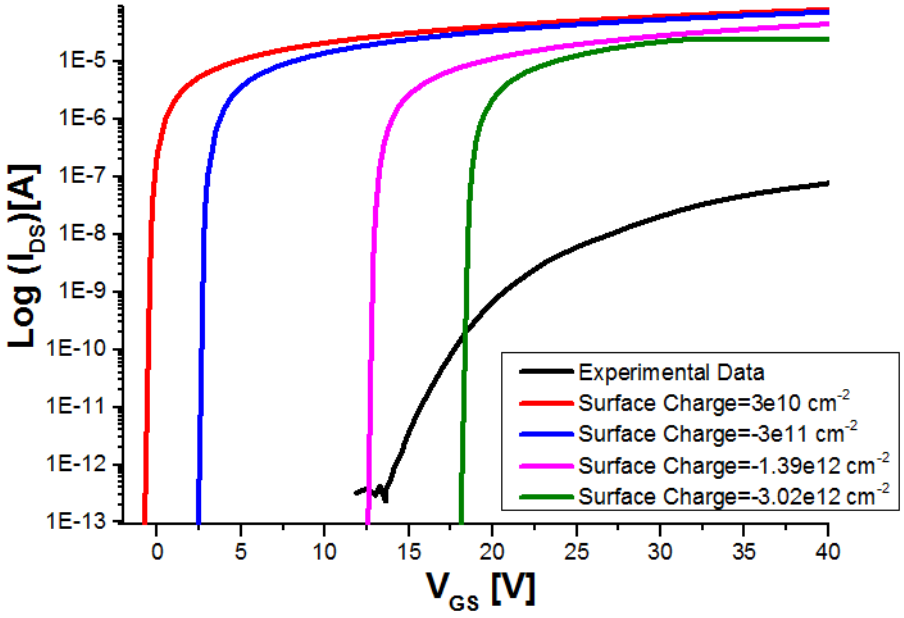

Figure 3.9 Subthreshold plot- Investigating the effect of surface charge

After all the suspected defect is introduced one by one, all the defect is combined in order to get the best fit simulation graph and experimental data. Figure 3.10 shows the subthreshold region of current/voltage characteristics of simulation curve matched to the experimental data. However, the simulation curve still has a higher subthreshold slope due the 2D simulation. This is the best matched curve that can be simulated using the 2D environment. 3D simulation allows for more precise and accurate estimation of the experimental device. The simulation work with 3D will be used in the future simulation work.

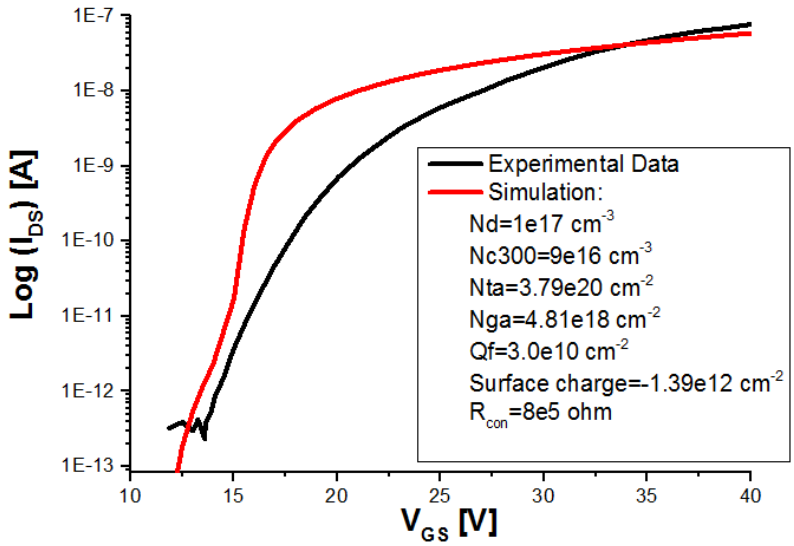

Figure 3.10 Subthreshold plot- Comparing simulation with experimental data (best fit)

Based on the graph, the contact resistance is not the only defect that contributed towards low currents but also the surface charge. After introducing the surface charge, with other defects (Q_f, Q_{it} and contact resistance) in the simulation, the steepness of the subthreshold slope decrease. By analysing the simulation curve, surface charge contributed a lot towards the low current, high resistivity and poor subthreshold slope in the experimental device. The Q_f was kept at the default value because it is been hypothesised that it has an insignificant defect for the experimental device. So it can be concluded that the main defects in the experimental device which affect the ZnO nanowire FET are interface state charge, contact resistance and surface charge. However, roughness are not properly analysed due to simulation constraints, and it is hypothesised to also limit the experimental device for achieving ideal device characteristics.

3.3 Conclusion

In this study, the ZnO nanowire is assumed to be a triangular shape. Therefore, a capacitance model based on non-embedded nanowire with an effective dielectric constant, $\varepsilon_{r,eff} = 2.65$ is used. A comparison between the measured and calculated V_{TH} yielded a difference of 34%, which demonstrated that the capacitance model used is valid for fabricated nanowire in this study. The 2D simulation also was carried out to compare with experimental result from Suhana [15]. The experimental result has field effect mobility of 10 cm^2/Vs at V_{DS} = 1 V, threshold voltage of 24 V. subthreshold slope of 1500 mV/decade. By using simulation results, it was discovered that the experimental output results are degraded due to interface state charges, contact resistance and surface charges. The simulation results gives an insight of what should be done in device fabrications.

3.4 References

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Chapter 4:
Fabrication of Top-down Zinc Oxide Nanowire FETs

This chapter explains the three techniques used to fabricate the ZnO nanowire FETs throughout this project. The chapter begins by introducing the background of fabrication methods used in this study and the device overview. The chapter continues by describing the ZnO deposition method and the details of the three device configurations fabricated in this thesis.

4.1 Introduction

The fabrication of FETs based on semiconducting nanowires required a precise patterning of the different components of the FET. These components are the source and drain contacts, the gate electrode, the insulator or gate dielectric and semiconducting nanowire channel. Generally, there are two ways of fabricating a nanowire FET; the bottom-up or the top-down process. In this study, the fabrication of the nanowire FETs based on the top-down method was used. The top-down process was chosen because it can provide nanowires on a wafer in well-defined locations and permits nanowires with various length to be fabricated on the same wafer. Although a top-down method offers various advantages, the devices fabricated based on this method normally showed significant variations of electrical characteristics, such as output drain current and field-effect mobility, even lower performance than devices fabricated using bottom-up method [1]. In order to improve device performance for devices fabricated using top-down method, a number of issues should be considered such as, surface roughness and contact resistance.

A top-down fabrication method for ZnO nanowires involves the creation of the ZnO nanowires from the large parent entity. This type of fabrication method is comprised of three main steps, which are, (i) the deposition of the semiconductor material on the SiO_2 and silicon substrate, (ii) constructing the desired pattern or shapes by photolithography and (iii) performing the pattern transfer using either etching or a lift-off process. Apart from semiconductor material deposition, photolithography plays an important role in the production of high quality ZnO nanowires. In the top-down process, the photolithography context is typically the transfer of a pattern to the substrate from the mask. One of the main issues that needs to be overcome in pattern transfer is roughness, as it can influence electrical performance and electron transport through nanowires [2]. In addition, roughness

does not scale down with the dimension of the devices. As the dimensions of the device structure get smaller roughness remain the same [3]. One of the main origins of roughness is the pattern transfer lithography process such as, mask quality, photoresist property and image projection transfer [4]. Another issue with nanowire electrical performance is the high ohmic contact resistance at source and drain region. In most nanowire FETs fabrication, an ohmic contact region is often ignored because of the challenges of introducing a highly doped region. As channel length decreases, the resistance of the source/drain contact is an important factor influencing device performance including field-effect mobility, subthreshold slope (*SS*) and on/off current ratio [5]. Hence, it is required to optimize the source/drain contact to the nanowire in order to improve the electrical characteristics of ZnO nanowire FETs.

This chapter will focus on three types of devices. The first of these is a back-gated nanowire FET fabricated based on the spacer method with the sidewall smoothing approach. These devices are an extension of the work previously done by [6][7]with the fabrication process optimized by improving the sidewall roughness. The process involves a photoresist reflow technique described in [2] to directly remove the line edge roughness in the photoresist pattern and is followed by dry oxidation to further reduce the roughness along the sidewall of the etched silicon [8]. The result of the optimized process is compared with the result achieved, using the spacer method in Chapter 5.

The second type of device is a back-gated nanowire FET fabricated with bi-layer source/drain contacts. These devices are an extension of the nanowire FETs with a sidewall smoothing approach. The optimization includes the insertion of a highly conductive aluminium-doped ZnO (AZO) deposited by atomic layer deposition (ALD) between the ZnO nanowire and the source/drain contact. The properties of the AZO film and the electrical characteristics of the ZnO nanowire FETs with bi-layer source/drain contact were systematically investigated in Chapter 6.

The third type of device is also a top-down back-gated nanowire FET but is not based on the spacer method. The new fabrication approach using lateral wet etching was investigated to avoid the drawbacks of the spacer method. The spacer method on oxide insulator is irreversible after the pattern transfer. Thus, ions and chemical radicals from the plasma source are implanted into the nanowires and change their top surface chemistry and electrical properties [9]. In this novel fabrication approach, the nanowire was directly patterned using photolithography and the lateral wet etching method to fabricate the ZnO

nanowires. By using this new method of fabrication, two process steps that use anisotropic dry etching are eliminated. The new fabrication method allows the nanowire to be fabricate on a planar back gate dielectric thin film, which enables better back gate control. The preliminary electrical performance of the device with this fabrication method was then discussed in Chapter 7.

4.2 Deposition of ZnO Film by remote plasma ALD

ALD was introduced as an atomic layer epitaxy (ALE) in 1970s by Suntola and Antson to develop thin film electroluminescence (TFEL) displays [10]. ALD is a deposition method that is capable of producing conformal and high quality metal oxide thin films. This method allows to deposit a variety of thin film materials by taking advantage of sequential chemical processes that occurs in the ALD reactor. This technique relies on the self-limiting reactions of metallization and oxidation [11]. It is a cyclical technique based on four sequence steps: precursor exposure, purging of precursors, reactant exposure and purging of the reactants [11]–[13]. During ALD process, the metal precursor molecules are absorbed onto the substrate surface until self-saturation. Then, the absorbed metals reacted with an oxidant in the oxidation step. In between an argon gas purge is applied to remove the excess precursor and the reaction by-products. The required film thickness is adjusted based on the number of cycles.

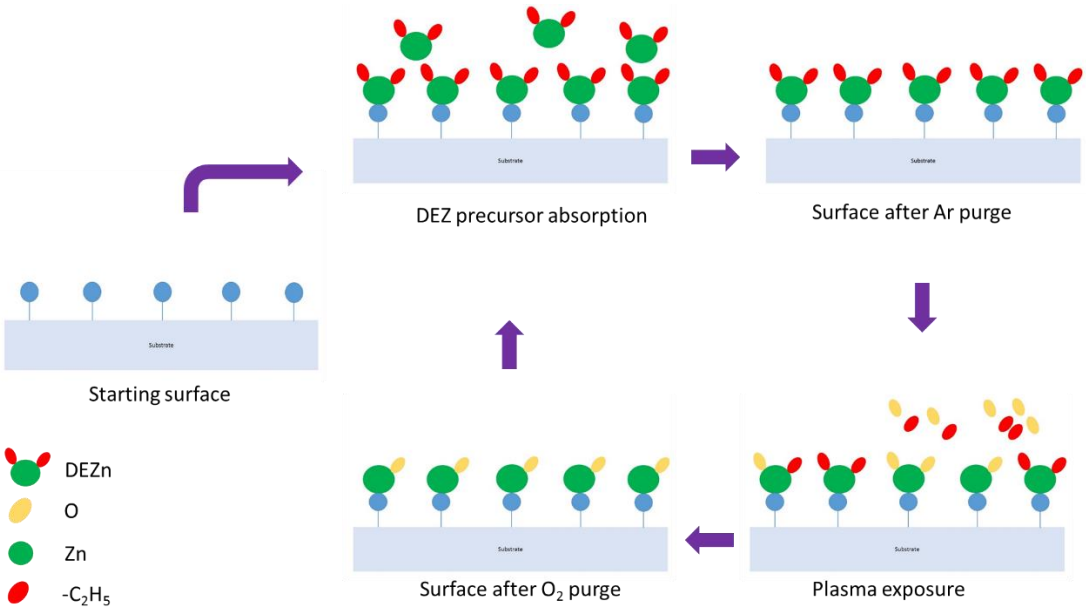


Figure 4.1 Illustration of ALD ZnO film reaction showing the DEZ – zinc monolayer deposition followed by argon purge and oxidation step of the zinc with the oxygen plasma. Adapted from [14].

There are mainly two types of ALD; thermal ALD and plasma enhanced ALD (PEALD). The main different between these two ALD processes is that in PEALD, the plasma species is used as a reactant. In thermal ALD, the chemistry of the process is thermally activated due to the deposition temperature [15]. The temperature window of thermal ALD for most of the metal oxide process is commonly between 150 ^{o}C and 400 ^{o}C [16]. The use of plasma significantly reduced the OH impurity, which affected the conductivity of the semiconductor film and induced defects in dielectric materials [12][17][14]. It also reduced the deposition temperature, offered a higher growth rate and more process versatility [14]. There are three types of PEALD equipment configuration for assisting ALD process by means of a plasma step, they are, radical-enhanced ALD, direct plasma ALD and remote plasma ALD [14][15]. In this study, remote plasma ALD was used to deposit ZnO film.

The deposition of ZnO film was carried out in a FlexAl Atomic Layer Deposition Tool made by Oxford Instruments. ZnO films were deposited on SiO_2 layer using diethyl zinc (DEZ, $Zn(C_2H_5)_2$) as the Zn precursor and O_2 plasma as reactant gas. The SiO_2 layer was thermally grown on the silicon substrate prior to ZnO deposition using dry thermal oxidation at 1000 ^{o}C. At the beginning of a remote plasma ALD cycle, a fixed amount of DEZ is introduced into the reactor for 100 ms and a layer of DEZ absorbs into the substrate surface as a saturated monolayer. After reaching saturation, excess DEZ and the reaction product will be purged from the chamber by Ar for 4 s. At this step, there is no reaction between DEZ and Ar, and Ar only works as a purge gas. The - C_2H_5 ligands of the chemisorbed Zn $(C_2H_5)_2$ species were then removed by a reaction with oxidant in the oxidation step. The oxygen radical species was produced by a remotely placed inductively coupled plasma (ICP) source operating at a pressure of 10 mTorr. The flow of O_2 was kept constant at 60 sccm during this cycle. Excess O_2 was then purged for 4s using Ar to ensure that only one reactant was present in the ALD chamber before the next step of the process was taken. One cycle produced one monolayer of ZnO on the substrate. The ZnO film deposition temperature was kept at 190 ^{o}C throughout the process. Figure 4.1 shows one cycle of the remote plasma ALD process. The process is repeated until a desired thickness has been achieved. A very conformal ZnO deposition was observed using scanning electron microscopy after the deposition of ZnO film on top of 250 nm SiO_2 layer (Figure 4.2).

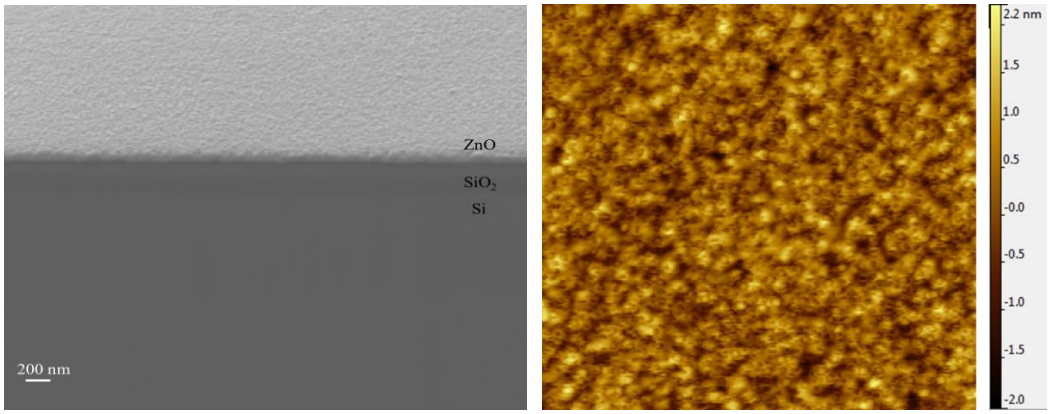


Figure 4.2 Cross-sectional SEM (right) and top-view of AFM image of as-deposited remote plasma ALD ZnO film (left).

4.3 ZnO nanowire FETs fabrication

4.3.1 Fabrication of ZnO nanowire-FET by sidewall smoothing

The top-down fabrication method based on the spacer method has been reported in [6][7]. However this fabrication work does not include the sidewall smoothing approach. The fabrication process starts with a p-type Si sample and a layer of SiO_2 thermally grown on the substrate. The SiO_2 was then etched anisotropically by photolithography pattern transfer and reactive ion etching (RIE) to form a SiO_2 pillar with an etched depth of 150 nm and 10 µm wide. The remote plasma ALD of 100 nm ZnO film was then deposited at 190 °C. For ease of discussion in this chapter, the previous top-down fabrication method will be referred to as the non-reflow photoresist spacer method. The new optimized top-down fabrication method is called the reflow photoresist spacer method and the fabrication process starts with the formation of 250 nm Si pillars by photolithography pattern transfer with a photoresist reflow process and anisotropic inductively coupled plasma (ICP) etching. The photoresist reflow process involves melting a photoresist structure to generate a smoother photoresist pattern using a heating effect. A 100 nm thick SiO_2 thin film was then grown by dry thermal oxidation at 950 °C and followed by remote plasma ALD of 100 nm thick ZnO film at 190 °C. In both non-reflow and reflow photoresist fabrication methods, after the ZnO film deposition the film was then anisotropically dry etched by ICP based on CHF_3 gas chemistry to form nanowires at the side of the SiO_2 trench. Finally 500 nm thick Al film is lifted off to form the metal contacts at the source drain region. Figure 4.3 and Figure 4.4 shows the schematic process flow of the non-reflow and reflow photoresist spacer methods respectively.

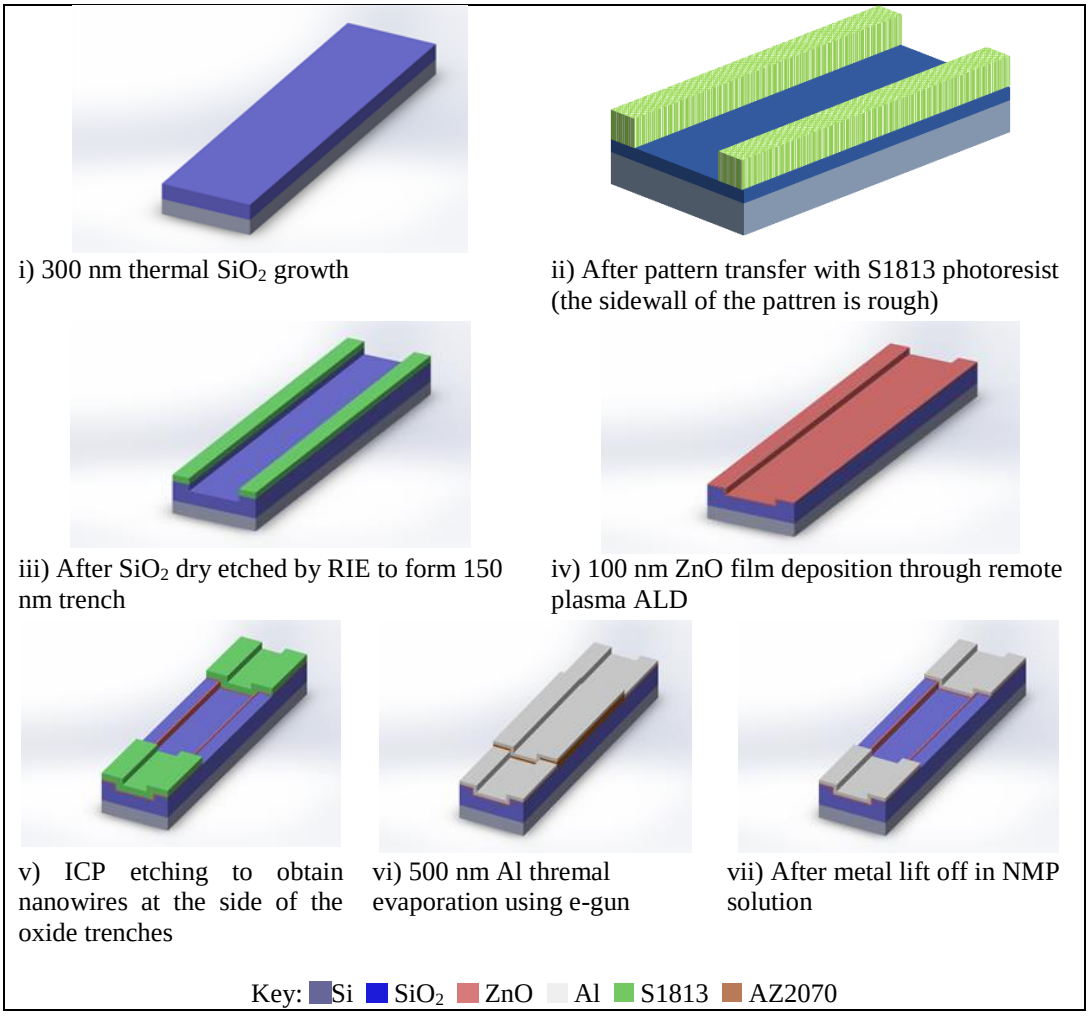


Figure 4.3 Schematic of the fabrication process for non-reflow photoresist spacer method.

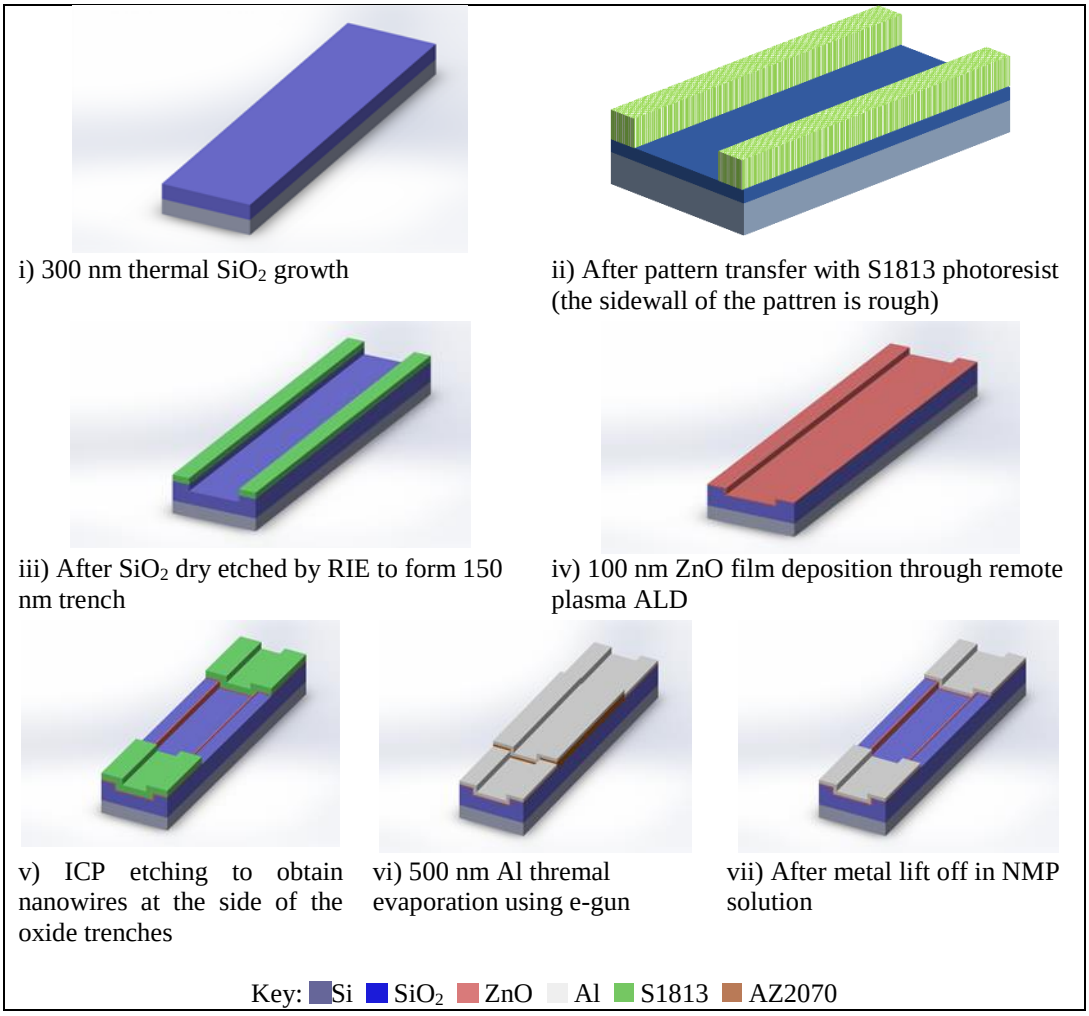


Figure 4.4 Schematic of the fabrication process reflow photoresist spacer method.

The differences between the non-reflow and reflow photoresist methods are illustrated in step (i) and (ii) of Figure 4.3. In the non-reflow photoresist method, the process starts with thermal oxidation and then followed by pattern the spacer structure on the SiO_2. However, in the reflow photoresist spacer method, instead of dry etching the thermal SiO_2 layer from the optical mask lithography layer, I first patterned the spacer structures on the silicon and applied the photoresist reflow process as shown in step (i) and (ii) of Figure 4.4. Yu et al. [2] investigated a technique to improve the quality of their nanoscale gratings line roughness by reflowing the developed photoresist. Most of the positive photo photoresists, which do not crosslink during the development, demonstrate a certain softening point between 100 °C to 130 °C for 1 min to 4 min, which can be used for reflow. In this study, the experiment of the photoresist reflow was conducted at a temperature between 100 °C to 130 C for 1 min using a hotplate to find out the suitable temperature for the S1813 photoresist reflow process. The samples of the reflow photoresist were observed under optical microscopy and scanning electron microscopy (SEM). The images were compared and the reflow point was carried out at 130 °C for 1

min was chosen to be used in the reflow photoresist method because it gives the best photoresist sidewall condition.

The image of the non-reflow and reflow photoresist were taken using scanning electron microscopy (SEM) to observe the top surface and the cross-section of the developed photoresist as shown in Figure 4.5 and Figure 4.6 respectively. From the non-reflow photoresist method (Figure 4.5), the developed photoresist exhibited a very rough sidewall. The sidewall roughness originated from the optical mask used to fabricate the ZnO devices. The edge roughness was then transferred to the SiO_2 pillar sidewall by the RIE process. In contrast, it was evident that the reflow photoresist method has smoothed off the pattern's sidewall roughness created by the initial optical mask transfer as shown in Figure 4.6.

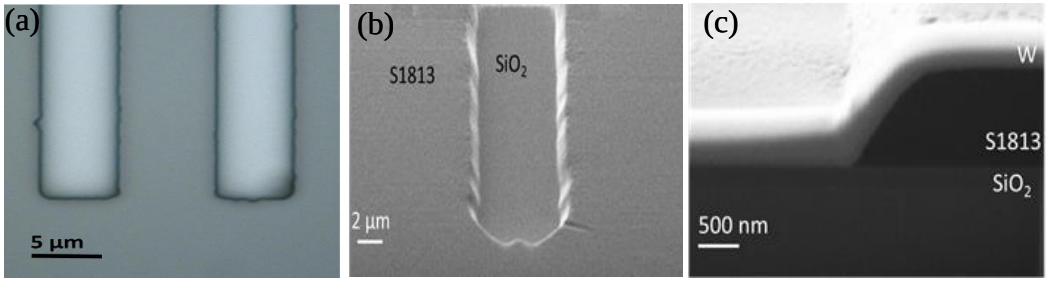


Figure 4.5 (a) Optical microscope image (b) Scanning electron micrograph of the trench top surface and (c) cross section of the of the pattern from non-reflow photoresist spacer method process.

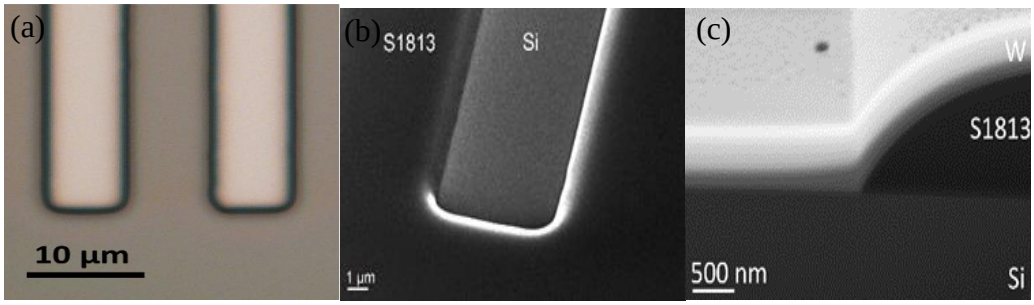


Figure 4.6 (a) Optical microscope image (b) Scanning electron micrograph of the trench top surface and (c) cross section of the of the pattern from reflow photoresist spacer method process.

Figure 4.7 shows the SEM image of a trench cross section after the thermal oxidation of non-reflow and reflow photoresist processes. In the reflow photoresist spacer method, a uniform layer and smooth surface of SiO_2 was obtained as shown in Figure 4.7 after a dry thermal oxidation of silicon. Compared to the non-reflow photoresist process, the SiO_2

layer thickness was not uniform because the dry etching process was performed after the oxidation of silicon and the surface was rough due to the effect of dry etching. Figure 4.8 shows a cross-section of conformal ZnO after the remote plasma ALD and the ZnO nanowire with the dimension of 100 nm in width, 208 nm in height and 8.6 μm in channel length from the reflow-photoresist spacer method fabrication process. The electrical performance of the ZnO nanowire FETs based on non-reflow and reflow photoresist methods will be discussed in Chapter 5.

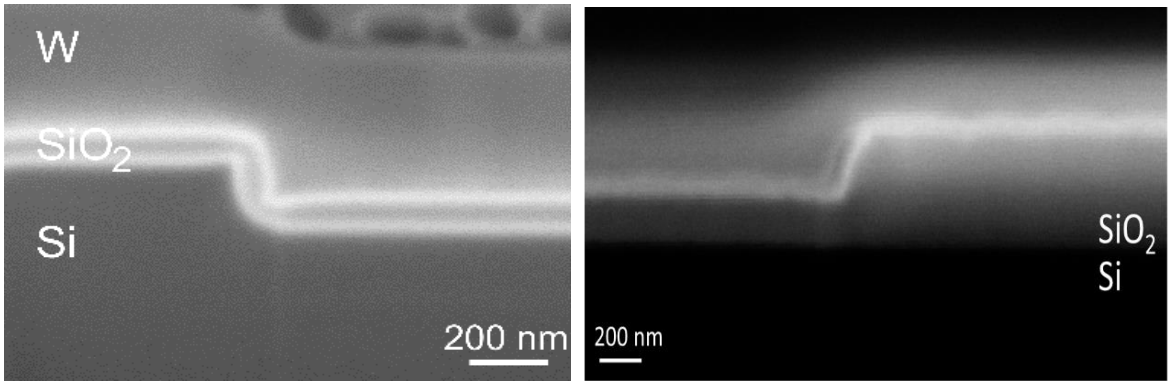


Figure 4.7 Scanning electron micrograph of the trench cross section after thermal oxidation of reflow (left) and non-reflow process (right). The tungsten (W) layer is to protect the SiO_2 layer during focused ion beam cross-sectioning and provide contrast to the SEM image.

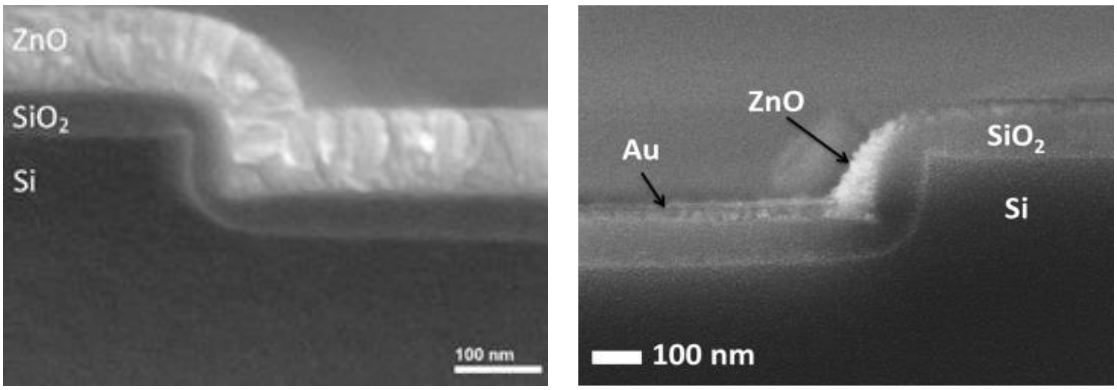


Figure 4.8 SEM cross-section of ZnO layer after remote plasma ALD deposition (left) and ZnO nanowire on the sidewall with sputtered Au for imaging (right).

4.3.1.1 Gate dielectric layer

Apart from the improving the sidewall roughness of the nanowires, the gate dielectric thickness also has been taken into consideration in the new reflow photoresist spacer method process. In using the thin gate thickness, there is a trade-off between obtaining good insulator behaviour, reasonable electrical properties, and a sufficient passivation

effect at the same time [18]. In this experiment, the ZnO nanowire FETs based on the photoresist reflow process were fabricated with four different gate dielectric thicknesses. The temperature of SiO_2 grown by dry thermal oxidation was fixed at 950 ^oC. The thickness of the SiO_2 varied between 25 nm, 50 nm, 75 nm and 100 nm. The electrical characteristics of the ZnO nanowire FET based on different gate dielectric thickness was then measured and compared. The characterization of these devices will be discussed in Chapter 5.

4.3.2 Fabrication of ZnO nanowire FET with AZO and Al heterojunction source/drain contacts

Other than optimized fabrication of ZnO nanowire FETs using the sidewall smoothing technique previously described in section 4.3.1, device fabrication is further improved by introducing bi-layer source/drain contacts. In this experiment, to avoid semiconductor damage induced by plasma and high temperature post thermal annealing and to enhance the electrical properties of the ZnO nanowire FETs, a highly conductive layer of AZO deposited using the ALD technique was inserted between the ZnO nanowire and the source/drain contact. A Savannah 100 ALD system made by Cambridge NanoTech Inc. was used for AZO deposition as bi-layer source and drain contacts.

Three different types of ZnO nanowire FETs were fabricated based on the spacer method [6][7] for the purpose of comparison and characterization. The first sample consisted of a bi-layer gate dielectric stack of SiO_2 and Al_2O_3 with a deposited Al source/drain contact electrode. The second device was fabricated with the same gate dielectric stack, but used with an intermediate layer of AZO at the source/drain contact pad. The third device was fabricated with thermal grown SiO_2 as a gate dielectric. On this sample, only Al was deposited as a source/drain contact. All of the ZnO nanowire FETs configurations are bottom gate top-down type FETs. For ease of discussion, the first, second, and third fabricated devices will be identified as sample 1, sample 2, and sample 3 respectively.

Figure 4.9 shows a schematic diagram of sample 1, sample 2 and sample 3. All samples were fabricated on a *p*-type Si wafers. The fabrication process starts by patterning the spacer structure on the silicon surface and applying the photoresist re-flow process to reduce the line edge roughness. Further fabrication process details are described in section 4.3.1 and Ref [19]. The silicon wafer was then anisotropic inductively coupled plasma (ICP) etched to form a 250 nm trench. The silicon etch was done in SF_6 and O_2 mixture at

a pressure of 30 mTorr and RF power of 100 Watt. A 100 nm thick SiO_2 layer was then thermally grown by dry oxidation at 1000 ^oC. For sample 1 (Figure 4.9(a)), another layer of Al_2O_3 film was deposited by thermal ALD at 200 ^oC as the gate dielectric stack on top of the SiO_2 film. Next, ZnO film with a thickness of 100 nm was deposited at 190 ^oC by remote plasma ALD using DEZ as described in section 4.2. The 100 nm ZnO thickness was achieved using 650 ALD cycles. After deposition, the ZnO film was etched in anisotropic ICP Ar etch to form nanowires along the edges of the $Si/SiO_2/Al_2O_3$ trenches. Finally, a 500 nm thick Al film was evaporated onto patterned AZ2070 photoresist and then lifted off in NMP solution to form Al source/drain contact. These ZnO nanowire FETs have a channel length of 2 µm and a channel width of 100 nm.

For sample 2, the device has a bilayer source/drain contact of Al/AZO. Figure 4.9(b) shows a schematic diagram of the ZnO nanowire FETs with a stack of SiO_2 and Al_2O_3 as a gate insulator and a bilayer Al/AZO source/drain contact. After the formation of ZnO nanowires along the edges of $Si/SiO_2/Al_2O_3$ trenches, the nanowire was passivated with a 20 nm Al_2O_3 thin film. Al_2O_3 thin film is used as a passivation layer and to protect ZnO nanowires during the formation of the Al/AZO source/drain contact. The source/drain contact region was opened by pH-controlled wet etching Al_2O_3 in tetramethylammonium hydroxide (TMAH) solution as described in Ref [20]. The TMAH was diluted in H_2O with the ratio of 1:300 (TMAH: H_2O). In this etching technique, the etch rate of Al_2O_3 depends on the pH of the etchant. An etchant with a pH of 11 at 40 ^oC was used because it gives a convenient and controllable etching time for the passivation layer. The etchant temperature must be kept between 39 ^oC and 43 ^oC to maintain the etchant pH 11 and etch rate of 5 nm/min. A 30 nm AZO layer was then deposited via thermal ALD on the un-passivated ZnO region. Al:ZnO (1:20) film was grown via alternate deposition of DEZ of ALD cycles, H_2O and ALD cycle of TMA at temperature of 200 °C. During the ALD process DEZ and TMA sources were not intentionally heated, and the precursor delivery lines were kept at 150 °C. Nitrogen was used as a carrier and inert gas for purging the chamber with a flow rate of 20 sccm. One cycle of ZnO consist of 15 ms DEZ pulse time, 5 s nitrogen purge, 15 ms H_2O pulse time, and 5 s nitrogen purge. The ZnO cycle was repeated 20 times before introducing one pulse of TMA for 100 ms. A total of 210 ALD cycles were required for AZO thickness of 30 nm. The target Al contents was 3% due to its metallic to semiconductor behaviour [21]. To form the top bilayer source/drain contact, the AZO film was patterned using wet etching with a solution of HCl: H_2O 1:1000 for 30 seconds. The wet etching technique was used to etch the AZO layer due to its ease of processing with

few controlling parameters and due to it being a low cost process [22][23] A 500 nm thick Al film was evaporated onto AZO and then lifted off in an NMP solution to form Al/AZO contact. These ZnO nanowire FETs have a channel length of 2 µm and channel width of 100 nm.

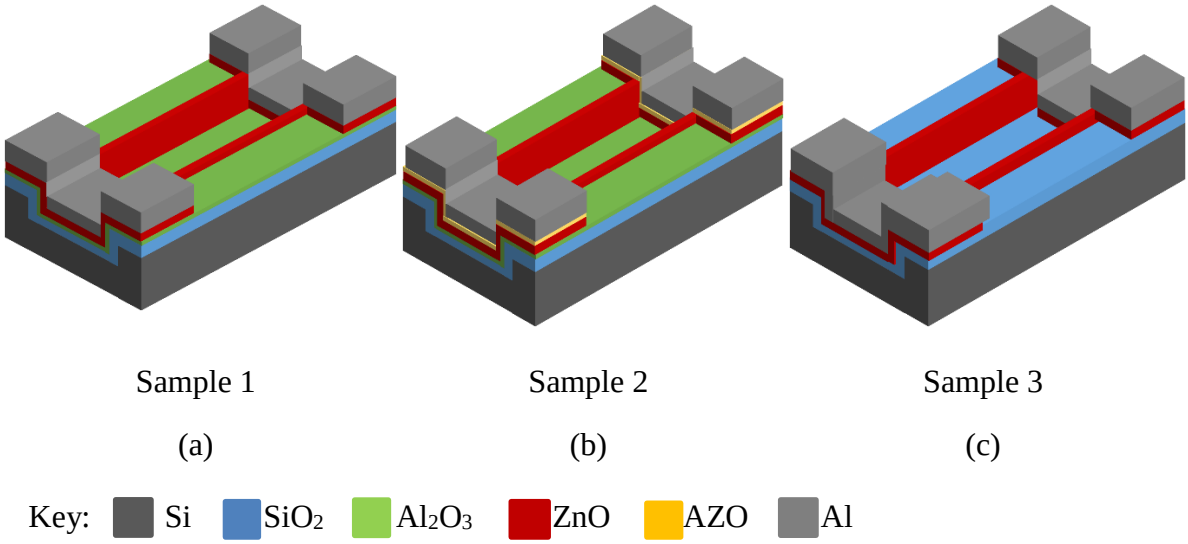


Figure 4.9 Cross-sectional schematic diagram of the ZnO nanowire FET using ZnO nanowire as channel layer: (a) with bilayer gate insulator and Al source/drain contact, (b) with bilayer gate insulator and Al/AZO source/drain contact, and (c) with SiO_2 as gate insulator and Al source/drain contact.

Figure 4.9(c) show the schematic cross sectional view of the third ZnO nanowire FETs configuration. This device configuration was fabricated for comparison purposes as our previous work used this type of device configuration. A 100 nm SiO_2 was grown by thermal oxidation of the silicon trenches and was followed by the deposition of 100 nm thick ZnO by remote plasma ALD at 190 ^{o}C. The ZnO film was then anisotropically etched by an ICP based on Ar etch to form nanowires along the edges of the previous etch trenches. The ZnO nanowire has a 2 µm channel length and a channel width of 100 nm. Finally, 500 nm Al was evaporated onto the ZnO nanowire pad and lifted off in NMP to form the source/drain contact. Figure 4.10 shows a cross-section and top-view scanning electron micrograph image of ZnO nanowires.

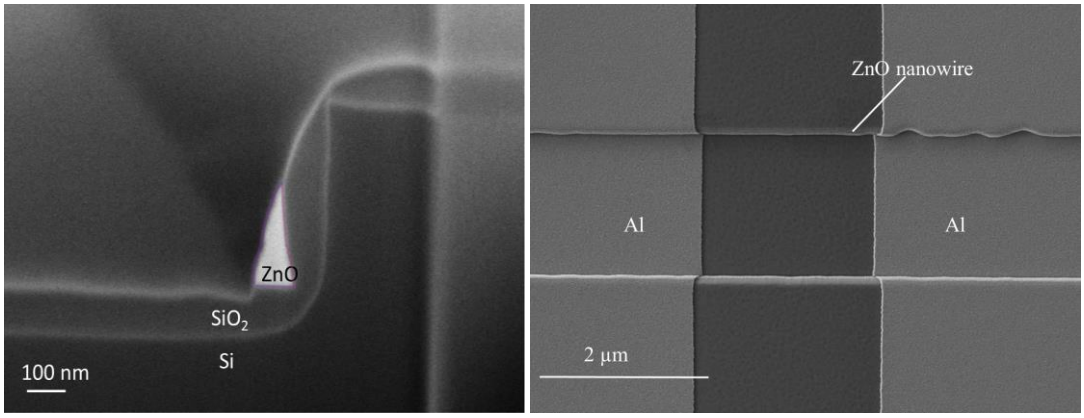


Figure 4.10. Cross-section and top view scanning electron micrograph of sample 3 with the ZnO nanowire at the edge of SiO_2 trench after ICP etching.

4.3.3 The fabrication of top-down ZnO nanowire FET by lateral wet etching

In this experiment, the new fabrication method using direct photolithography and lateral wet etching was investigated to avoid the disadvantage of the spacer method. This experiment also is a preliminary work attempt towards achieving high electrical performance in ZnO nanowire FETs. Apart from fabricating ZnO nanowire FETs for dc characterization, the fabrication in this experiment also includes a formation of ground-signal-ground contact pads for RF performance evaluation. The new fabrication method allows the formation of nanowire FETs with minimal impact from ions and chemical radicals during the anisotropic dry etching process. Bottom-gate configuration FETs using ZnO as the channel layer were realized using photolithography followed by a wet chemical etching process. A schematic cross-section view of bottom-gate ZnO nanowire FETs structure is shown in Figure 4.11.

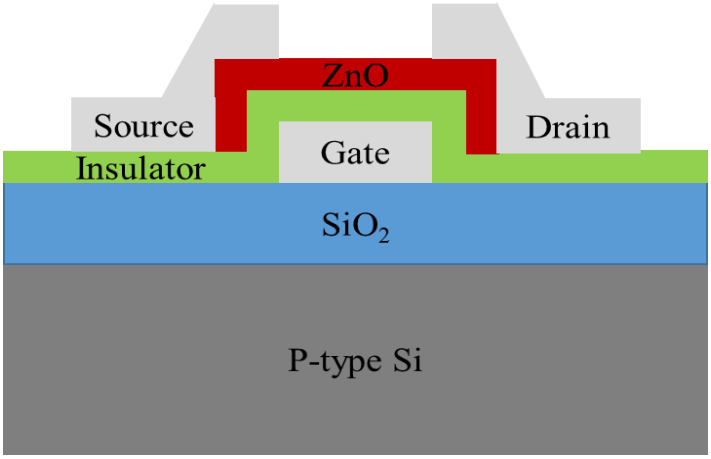
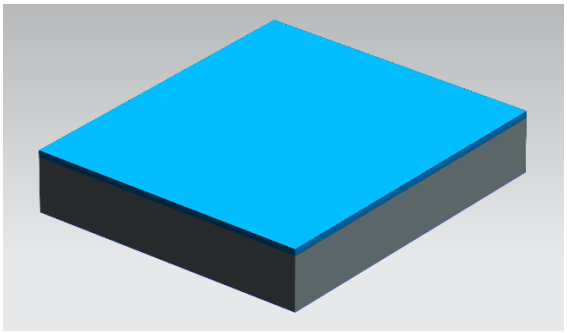
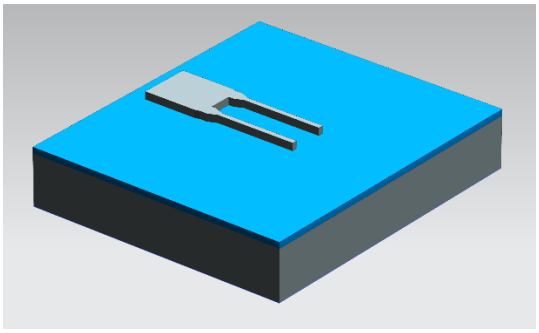


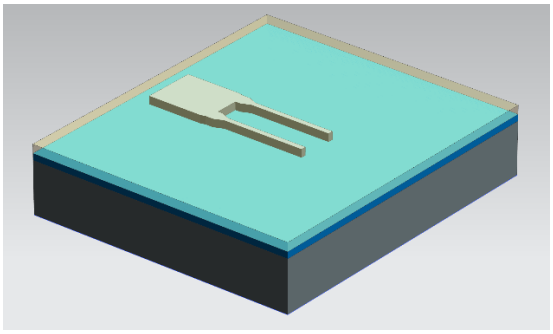
Figure 4.11 Schematic cross-section view of bottom-gate ZnO nanowire FETs.



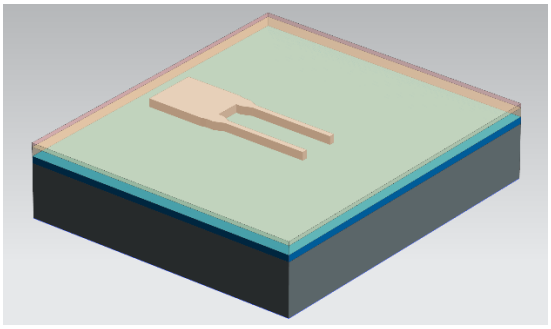
i) 250 nm 300 nm dry thermal SiO_2 growth.



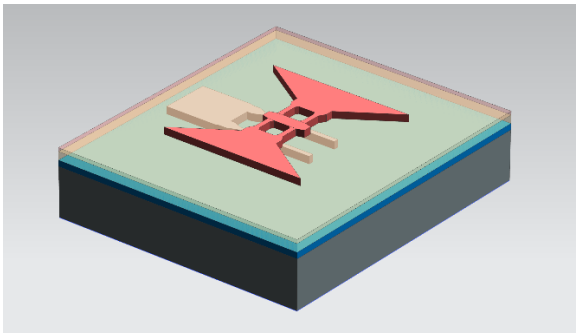
ii) After metal lift-off in NMP to pattern back gate.



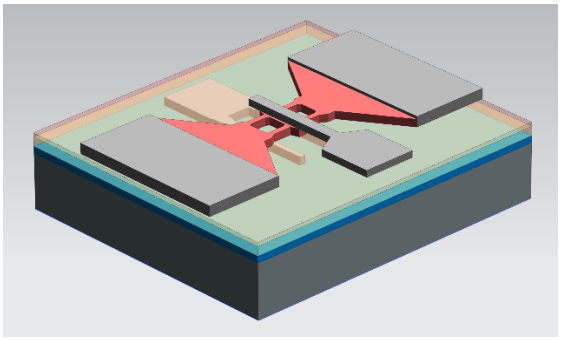
iii) After deposition of 35 nm Al_2O_3 via thermal ALD.



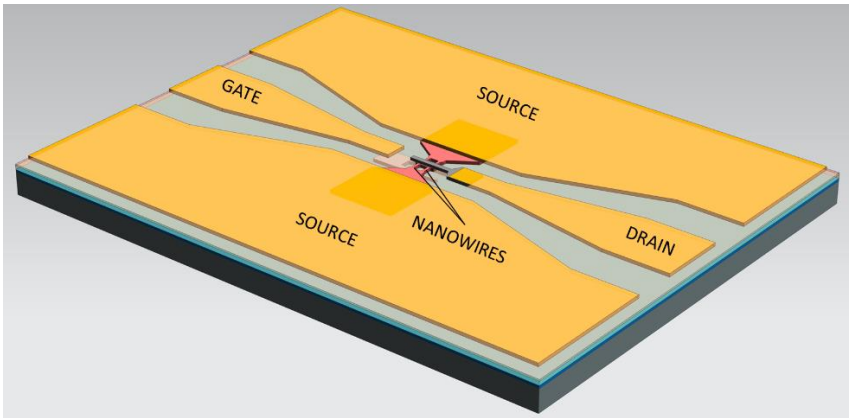
iv) 50 nm ZnO film deposition via remote plasma ALD



v) Lateral wet etching to obtain nanowires and ZnO pad areas.



vi) After metal lift off in NMP to pattern source/drain contact pads.



vii) After metal lift off in NMP to pattern ground-signal-ground contact pad for RF characterization.

Key: Si SiO_2 Al_2O_3 …. Al…. ZnO…..Au

Figure 4.12 Schematic of the fabrication process for ZnO nanowire FETs with direct photolithography and lateral wet etch.

Figure 4.12 shows the fabrication steps of structured bottom-gate ZnO nanowire FETs. In the first step, a buffer layer (thermal SiO_2) was thermally grown on p-Si (100). A 300 nm Al was evaporated over a patterned AZ2070 negative photoresist and a lift-off technique was used to form a gate contact on top of the SiO_2 buffer layer. After the lift-off process, the samples were transferred to a Savannah 100 ALD system from Cambridge NanoTech Inc. where a conformal layer of Al_2O_3 acting as a gate dielectric was deposited. The gate dielectric was deposited in 365 cycles at 200 ^oC (35 nm Al_2O_3) with TMA and H_2O as precursors, starting with an H_2O pulse.

In the next step, 40 nm ZnO layer was deposited by a remote plasma ALD process as described in section 4.2. A ZnO thickness of 40 nm was achieved using 218 ALD cycles at a temperature of 190 ^oC. After the ZnO deposition, positive photoresist (S1813) was coated on the ZnO surface and then the microscale lines of 2 µm, 2.5 µm, 3 µm, 3.5 µm and 4 µm wide were then patterned to protect the beneath ZnO nanowire during the latter etching process. A solution of HCl: H_2O 1:1000 was used to etch the ZnO nanowire for 40 s. The etching procedure was carried out at room temperature. A low concentration of HCl was used for ease of controlling the shape of the ZnO film [21]. After etching, the sample was immediately taken out and washed respectively in NMP to strip the photoresist, and was dried using the nitrogen gun.

Then, 300 nm Al was evaporated over a patterned AZ2070 photoresist and lift-off to form metal contact at the source and drain regions of ZnO nanowire FET. The top view of scanning electron micrograph is shown in Figure 4.13. Al gate contact area was opened by another pattern and Al_2O_3 was etched in the Ar ion beam etcher (IBE) with 300 mA beam current, 500 V beam voltage with an etch rate of 4 nm/s. For the device with the features for microwave performance evaluation, the bond pad design was patterned with AZ2070 negative photoresist and 200 nm Au was evaporated and lifted off to form a ground-signal-ground contact pad as shown in Figure 4.14.

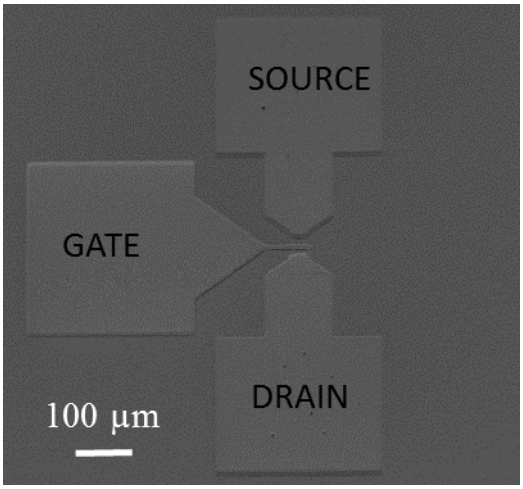


Figure 4.13 A top view of ZnO nanowire FET with patterned Al metal pads.

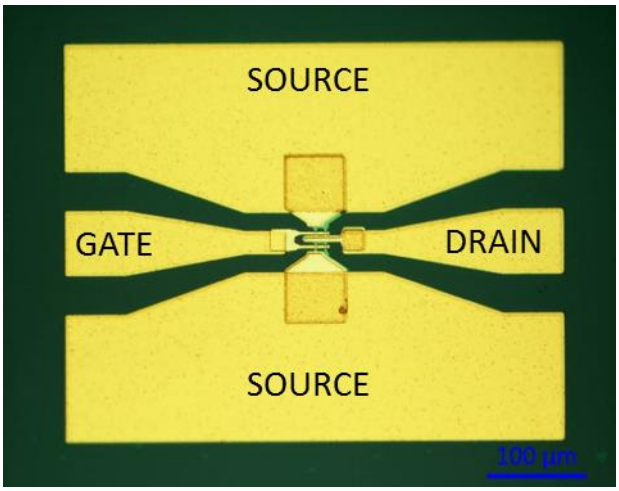


Figure 4.14 A top view of ZnO nanowire FET with Au bond pads.

4.4 Conclusion

Top-down ZnO nanowire FETs were successfully fabricated with three different experiments. The first experiment included a sidewall smoothing technique to reduce the surface roughness of the ZnO nanowire. The sidewall smoothing techniques was performed by applying the photoresist reflow process. The photoresist reflow process was shown to reduce sidewall roughness originating from the optical mask used to fabricate the ZnO devices. The second experiment is a continuation of sidewall smoothing techniques, where the AZO thin film layer was added as a source/drain contact. A bi-layer source/drain contact of Al/AZO was used with a gate dielectric stack. The aim of this technique is to improve the field-effect mobility of the ZnO nanowire FETs by reducing the contact resistance. The Al_2O_3 pH-controlled wet etching technique using TMAH was developed when the second experiment was performed. The pH controlled etching allowed a contact

window to be opened for contact after passivation without attacking ZnO nanowires. In the third experiment, a new design of ZnO nanowire FETs was introduced with the aim of achieving RF performance of ZnO nanowire FETs. This preliminary work used direct photolithography and a lateral wet etching technique to fabricate ZnO nanowire FETs. The electrical characterization of all the devices will be discussed in the next chapter.

4.5 References

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Chapter 5:
Characterization of ZnO Nanowire FETs by Sidewall smoothing

In this chapter, the sidewall roughness of ZnO nanowire FETs and effect of gate dielectric thickness are discussed. The electrical characteristics of the ZnO nanowire FETs with different gate dielectric thickness was compared and the optimum gate dielectric thickness was then being used in fabrication process of non-reflow and reflow photoresist. The ZnO nanowire FETs from non-reflow and reflow photoresist process were also being compared and discussed to give an insight of the surface roughness effect towards electrical performances.

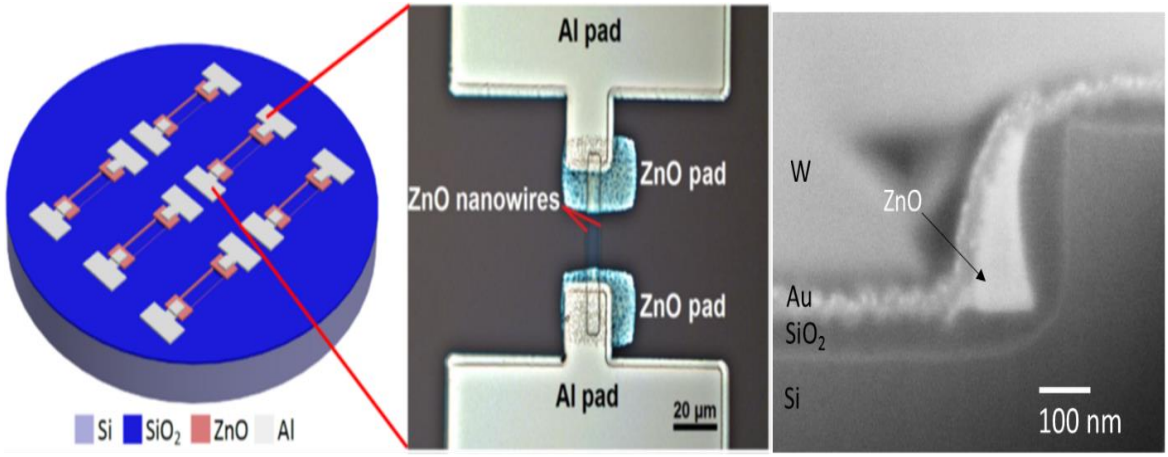
5.1 Introduction

Photolithography is one of the major steps in top-down fabrication method used to realize a pattern from the mask to the substrate. It plays an important role in producing high quality devices. The roughness associated with the surface and the edge of the photoresist could severely impact the electrical performance of the transistors [1][2]. In this work, three different chrome photomasks have been used to pattern a substrate for different layers using a photolithography process. As described in Chapter 4, roughness could originate from the quality of the mask used in photolithography, photoresist performance and image projection transfer. The roughness in this work is believed to come from the quality of the chrome photomask that have been used so many times. It was then transferred to the photoresist during the pattern transfer process. Therefore, the focus is to optimize the top-down spacer method with reduced sidewall roughness originating from the photoresist edge after the pattern transfer. This optimization could prolong the use of the chrome photomasks. The device from non-reflow photoresist with SiO_2 pillar spacer method [3][4] and device with reflow photoresist with oxidised silicon pillar spacer method have been fabricated based on the process described in Chapter 4.

The optimization of the fabrication of the device by sidewall smoothing also includes the study of suitable gate dielectric thickness. The right gate dielectric thickness is one of the important parameters in obtaining good electrical characteristics of the devices. The right thickness of gate dielectric may help to suppress the leakage current, increase

breakdown and enable the FET to operate successfully [5]. In this work, SiO_2 was used as a gate dielectric with thickness of 25 nm, 50 nm, 75 nm and 100 nm.

The finished ZnO nanowire FETs device fabricated using the reflow photoresist spacer method structure with Al source and drain pads is shown in the schematic overview and optical microscopy image in Figure 5.1(a) and Figure 5.1(b). The cross section of the ZnO nanowire is shown in Figure 5.1(c). It shows that the photolithography produced well aligned device. The ZnO nanowires were fabricated with different channel lengths between 1.3 µm to 20 µm with 100 nm in width and 208 nm in height and each device has two nanowires in parallel. The width and height of the ZnO nanowires can be controlled by altering the thickness of the ZnO layer during deposition and the height of the silicon trench.



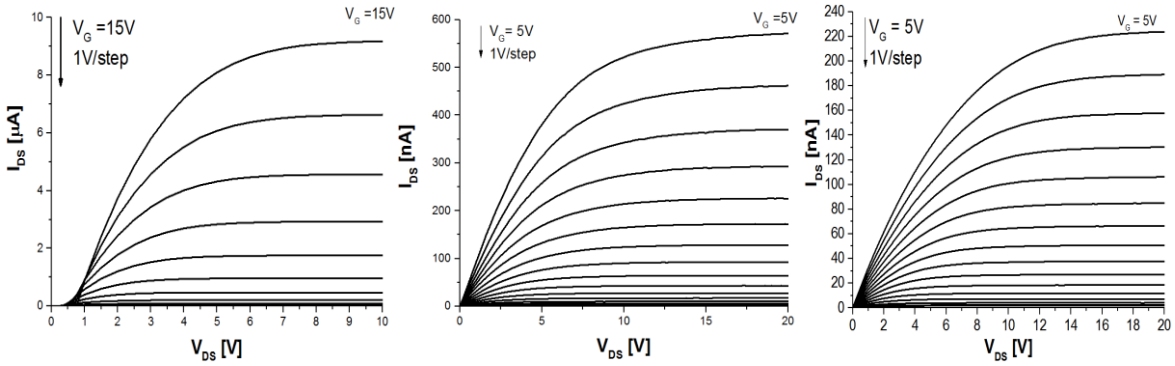
(a) (b) (c)

Figure 5.1 (a) Schematic drawing of the processed nanowire FET array (b) optical microscope image of dual nanowires (c) scanning electron micrograph of the trench section of the fabricated nanowire FETs (Au= gold coating, W= tungsten coating for focused ion beam cross-sectioning).

5.2 Effect of gate dielectric thickness

ZnO nanowire FETs with four different gate dielectric thickness were fabricated based on the fabrication process described in Chapter 4 and the electrical properties were measured. Figure 5.2 shows the I_{DS}-V_{DS} curve of the ZnO nanowire FETs with different thickness SiO_2 gate dielectrics. Note that the I_{DS}-V_{DS} curve for 25 nm SiO_2 is not included as the device is not working as a transistor. The I_{DS}-V_{DS} curve shows a linear graph with no saturation. This device could be suffering from high leakage current due to insufficient

thickness of the gate dielectric to isolate the active layer and the gate electrode. It is shown that the devices with 50 nm, 75 nm and 100 nm SiO_2 thicknesses have n-channel properties, since electrons are generated by the positive V_{GS} and this is because of the presence of some intrinsic defects [6] in ZnO nanowires. The FET with 50 nm gate dielectric exhibits a higher leakage current and also low output current as compared to FETs with 75 and 100 nm gate dielectric. This could be due to the insulating properties of the SiO_2 layer being degraded by depositing ZnO on the SiO_2 layer. Based on [7], the degradation of insulating properties is because of the diffusion of Zn into the SiO_2 layer. The acceptor types a Zn atom at the SiO_2/Si interface can induce positive space charge in silicon [8]. Zn behaves as a negative space charge in SiO_2, which can neutralize a positive sodium in SiO2 or at the SiO_2/Si interface. The Zn diffusion might be caused by the interaction of Zn and oxygen atoms near the SiO_2/Si interface [8]. Francois-Saint-Cyr et al. [9] also observed the Zn diffusion in thermally grown SiO_2 at low temperature. These results suggest that the leakage current in the 50 nm SiO_2 is initiated by the diffusion of Zn from the deposited ZnO layer on a SiO_2. Thus, the insulating properties can be improve by increasing the thickness of gate dielectric or introducing a multilayer gate dielectric.



(a) (b) (c)

Figure 5.2 I_{DS}-V_{DS} characteristics of different thickness of SiO_2 gate dielectric ZnO nanowire FETs (a) 50 nm (b) 75 nm (c) 100nm.

Figure 5.3 shows the corresponding transfer characteristics of I_{DS}-V_{GS} for the ZnO nanowire FETs at V_{DS} = 1.0 V. The off state current (I_{OFF}) for FETs with gate dielectric of 50 nm, 75 nm and 100 nm are about 2.3 x 10^{-11} A, 1.2 x 10^{-12} A and 2.4 x 10^{-13} A respectively. As the oxide thickness increased, I_{OFF} decreased by one order of magnitude at each step of oxide thickness. This suggest that the leakage current decreased as the oxide thickness increased. The results have also been observed by [10] in their works on tunnel FET. The low I_{OFF} is important in low-power, high speed communication circuit applications in order to lowing the power consumption of the circuits and thus can extend

the battery life and support the system operation with comparatively weaker power sources such as the RF power [11]. The I_{OFF} is also an important parameter in logic circuit applications and dynamic random access memory (DRAM) technology [12][13].

The subthreshold slope is defined as the voltage required increasing the drain current by a factor of 10. The subthreshold slope is one of the most important parameters in analog circuits and low-voltage applications and flat-panel display such as light-emitting-diode displays (OLEDs) and liquid crystal displays (LCDs) [14][15]. The steep subthreshold slope also becoming an important feature for the energy-efficient logic device in future VLSI technology and digital-logic applications [16]. The subthreshold slope, *SS* can be determine from the transfer characteristics through the relation $= dV_{GS}/d\ (logI_{DS})$. Here the subthreshold slope extracted value of 720 mV/decade, 2012 mV/decade and 750 mV/decade for device with gate dielectric of 50 nm, 75 nm and 100 nm respectively. Based on the electrical characteristic shown by FETs with different SiO_2 thickness, the device with gate dielectric of 100 nm exhibited superior performance as compared to other devices. The ZnO nanowire FET with 100 nm gate dielectric demonstrated lowest $I_{OFF,}$ with steep subthreshold slope. Although the device with 75 nm gate dielectric exhibited higher output current as compared to the device with 100 nm gate dielectric, the subthreshold slope and I_{OFF} for 100 nm oxide device is better.

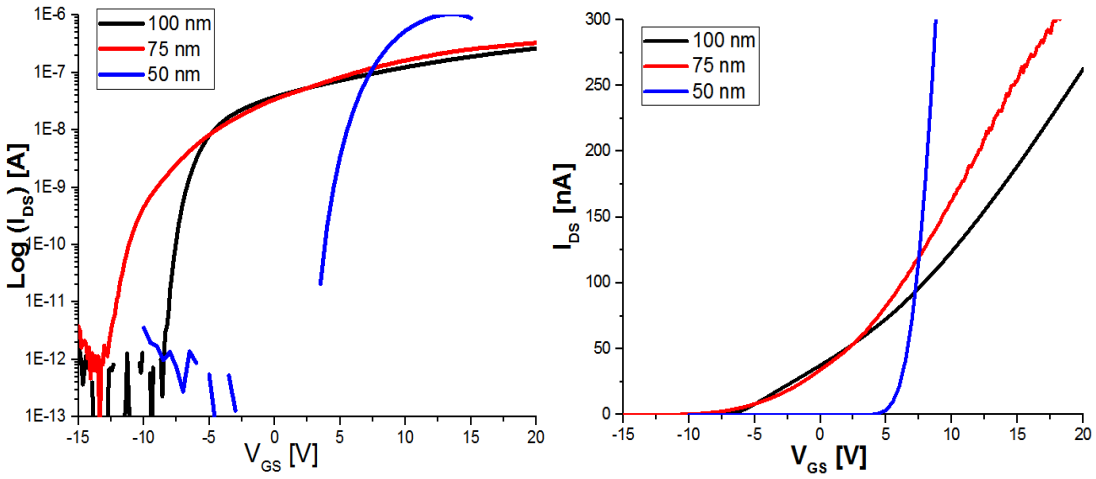
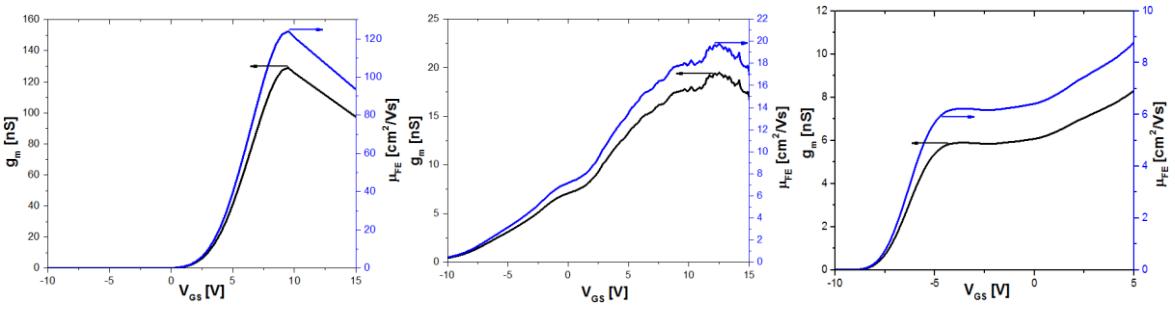


Figure 5.3 Semi-logarithmic (left) and linear (right) I_{DS}-V_{GS} characteristic of the ZnO nanowire FETs with different thickness of SiO_2 at V_{DS} = 1.0 V.

Figure 5.4 shows the plot of the transconductance, g_m and the calculated mobility as a function of gate voltage for ZnO nanowire FETs with different gate dielectric thickness. The transconductance was obtained by first derivation of transfer characteristics, I_{DS}-V_{GS}.

The field effect mobility for FETs with gate dielectric of 50 nm, 75 nm and 100 nm are estimated to be 123.8 cm^2/Vs, 19.8 cm^2/Vs and 7.5 cm^2/Vs respectively. The field effect mobility increased as the thickness of the gate dielectric decreased from 100 nm to 50 nm. These results indicate that the field effect mobility in the top-down ZnO nanowire FETs has correspond on the gate dielectric thickness. The dependence of the field effect mobility and the output current on the gate dielectric thickness can be due to charge carrier injection from source/drain contacts and charge carrier induction by the gate bias in semiconductor channel [17]. The field effect mobility is inversely proportional to the capacitance in Eq. 27, discussed in Chapter 3. It can be inferred that the source-drain current and the mobility increased with the decreased insulating thickness due to an increase in the capacitance induce more charge carriers by the same gate voltage [17]. Furthermore, upon application of the same gate voltage, the vertical electric field increased at a lower dielectric thickness, resulting in more electron injected from the source contact. Consequently, the output current and the field effect mobility increased by reducing gate dielectric thickness [17].



(a) (b) (c)

Figure 5.4 Transconductance (g_m) and field effect mobility (μ_{FE}) as a function of gate bias at V_{DS} = 1.0 V for ZnO nanowire FETs with SiO_2 thickness of (a) 50 nm (b) 75 nm and (c) 100 nm.

The SiO_2 layer cannot be too thin in order to maintain its insulating ability to act as the gate dielectric layer in ZnO nanowire FETs, although the mobility increased as the gate dielectric thickness decreases. In this study, the device with 100 nm SiO_2 layer was chosen to be used in the next experiments.

5.3 Sidewall roughness measurement

One of the main aims of this work is to compare the sidewall roughness between non-reflow and new reflow fabrication methods. ZnO nanowire FETs based on non-reflow and reflow photoresist spacer methods have been fabricated. Figure 5.7 shows a spacer structure used to fabricate ZnO nanowire FETs with the position of the AFM tip and the scan direction when the measurement was done. The wafer was cleaved along the 10 µm wide spacer structure and the segment was placed on the sample stand for AFM measurement. The patterns allowed the cleavage of the sample to result in at least one segment of the spacer structure very close to the cleaved edges so that AFM tip can easily reach the sidewall of the spacer structure in the direction perpendicular to the sidewall. With the AFM tip normal to the etched sidewall, the feedback loop of the z-directional movement of the AFM tip is still effective. This AFM setup is also being used by [18][19] for AFM sidewall scanning. Both sidewall roughness of ZnO nanowires based on non-reflow and reflow process have been measured using atomic force microscopy (AFM) under ambient condition in intermittent non-contact mode. The AFM sidewall roughness measurement for the resist, trench and nanowire was carried out under ambient conditions in intermittent non-contact mode with a high aspect ratio (HAR) AFM tip from Bruker (previously known as Veeco). The tip radius is 10 nm and shaped like a polygon based pyramid with a half cone angle of the high aspect ratio portion typically less than 5° and a height of 10 µm. Image processing and analysis are performed using Gwydion software, where the images are flattened with a plane fit procedure and rms sidewall surface roughness value is extracted from the software.

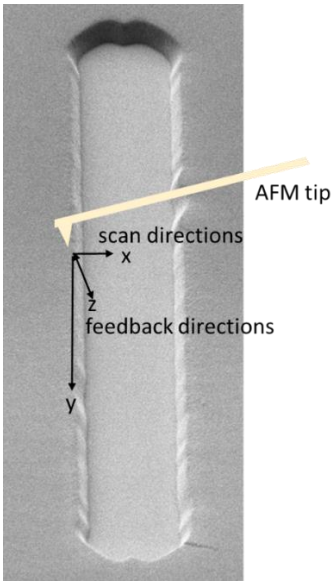


Figure 5.5 Position of the AFM tip and scan directions.

Figure 5.6 shows the AFM images of patterns at selected process steps based on non-reflow and reflow photoresist spacer method. The root-mean-square (rms) roughness of photoresist after lithography based on the non-reflow spacer method was 23.2 nm as shown in Figure 5.6(a). In the non-reflow process, the photoresist was applied on the SiO_2 layer to form the spacer templates. After the dry etching of the SiO_2 to form the nanowire spacer template, the surface rms roughness decreased to 13.1 nm (Figure 5.6(b)) with striations created by ion bombardment during the dry etch. The striations on the sidewall begin at the top of spacer structure and are transferred down to the bottom of the scanned sidewall. This type of striations was also observed by Jang et al. on the waveguides sidewall [19]. The inset in Figure 5.6 (b) illustrated the cross-section of striations that cause the trench features in the AFM at the top of the SiO_2 sidewall. During the subsequent ZnO ICP etching, these striation transfer into the nanowire sidewall but the striation features have been reduced as shown in Figure 5.6(c) with rms roughness of 11.2 nm. Although, the surface roughness value reduced as the non-reflow spacer method process proceed through the steps, sidewall roughness of the photoresist transferred throughout the fabrication process was significant [20]. As a result, ZnO nanowires still suffer from the surface roughness that contribute to degradation of its electrical performance.

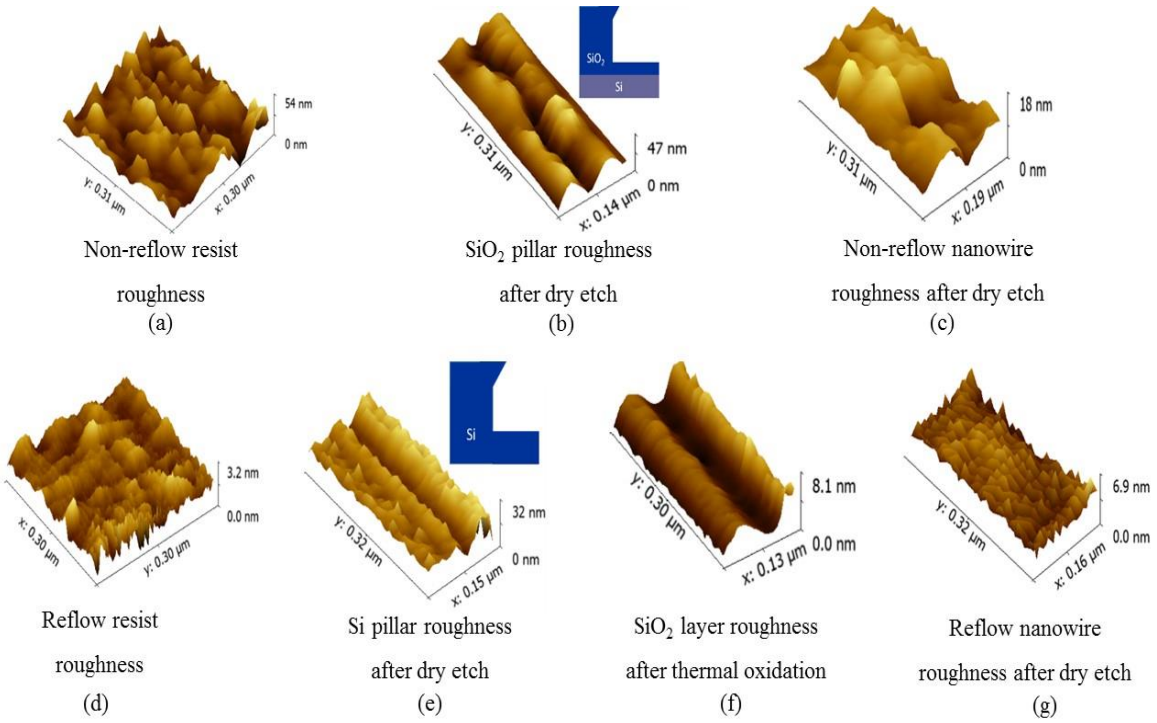


Figure 5.6 AFM image of surface sidewall profile of the device fabrication based on (a) non-reflow process (b) reflow process.

Figure 5.6 (d) shows the AFM image of the photoresist after lithography and photoresist reflow being applied. The rms roughness based on the photoresist reflow spacer method was 3.6 nm which is 6 times lower than for the non-reflow photoresist fabrication method. In the reflow photoresist spacer method the spacer structures was patterned on the silicon instead of SiO_2. The silicon sidewall has an rms roughness of 5.9 nm after the dry etch as shown in Figure 5.6 (e) with striations features as illustrated in the inset of Figure 5.6(e). Similar striations are also observed in the non-reflow process, as shown in Figure 5.6 (b). After dry thermal oxidation of the silicon, the striations from silicon dry etch was transferred to the SiO_2 sidewall but with smoother surface of rms roughness 5.4 nm as compared to the SiO_2 trench sidewall from non-reflow photoresist process. The oxidation of silicon trenches to grow the SiO_2 has smoothed the trenches' surface. The ZnO was then deposited on the SiO_2 spacer template and etched by ICP etching. The rms roughness of the ZnO nanowire based on the reflow photoresist spacer method after the ICP etching was measured to be 5.5 nm which is two times lower than to the sidewall roughness of the nanowire from non-reflow photoresist process. Throughout the fabrication based on reflow photoresist process, the rms roughness only varies between 3.6 nm to 5.9 nm. A summary of the AFM measured surface roughness based on the non-reflow and reflow process is shown in Figure 5.7.

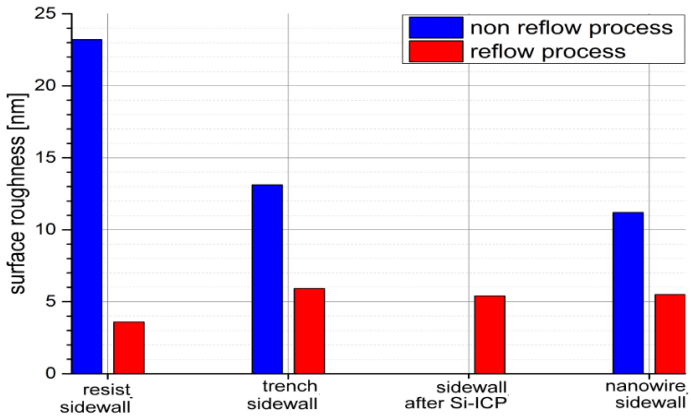
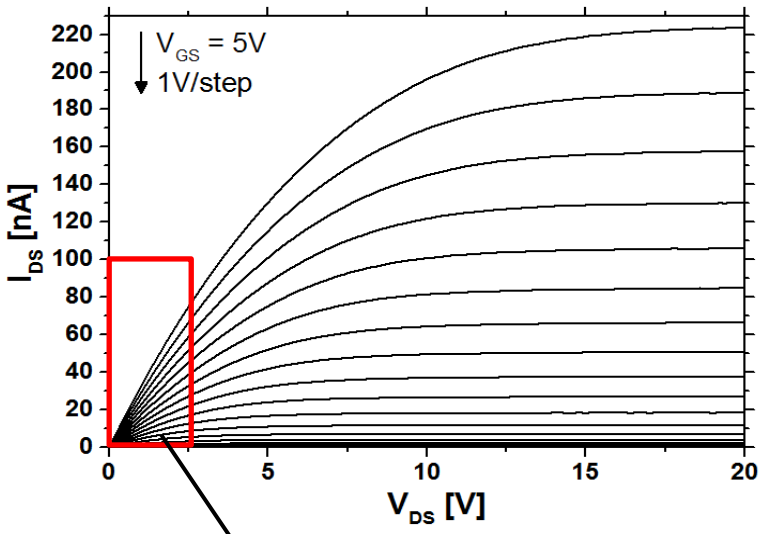


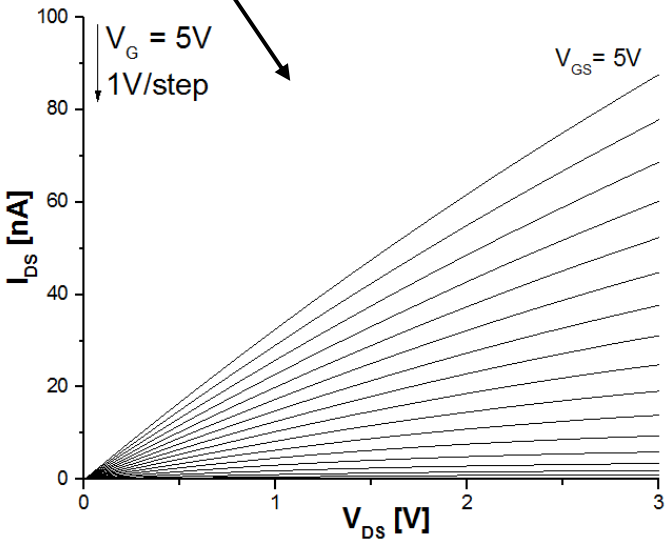
Figure 5.7 Comparison of the nanowire surface roughness between the non-reflow process and the new reflow fabrication design measured by AFM.

5.4 Electrical Characteristics of ZnO nanowire FET by sidewall smoothing

The electrical characterization was performed using a semiconductor device parameter analyser (Agilent B1500A) in the dark at room temperature. Figure 5.8 shows the output source-drain current-voltage (I_{DS}-V_{DS}) characteristics of the ZnO nanowire FET with two parallel nanowires and a channel length of 8.6 µm fabricated based on the new reflow photoresist process. The transistor operated in the n-type depletion mode and the output characteristics shows a clearly defined linear and saturation region, which indicate that the carrier modulation in the channel can be controlled by the gate-voltage. The drain bias of the ZnO device provides good field-effect transistor characteristics [21]. The device is driven by a back gate V_{GS} sweep from –10.0 V to 5.0 V at 1.0 V step. A saturation current of 220 nA for V_{GS} = 5.0 V and V_{DS} = 20.0 V could be observed. From the I_{DS}-V_{DS} characteristics, current crowding can be seen at low drain voltage and from V_{GS} = -2.0 V to -10.0 V indicating the presence of the contact resistance between the source/drain electrodes and the ZnO nanowire channel layer. This is also observed by Barquinha et.al and Huang et.al in their thin film transistor with Al source and drain contact [22][23].



(a)



(b)

Figure 5.8 (a) I_{DS}-V_{DS} characteristics with a V_{GS} drive from -10 V to 5 V with steps of 1.0 V and (b) Zoomed area of I_{DS}-V_{DS} characteristics from V_{DS} 0 V to 3 V.

In order to assess the scalability of the ZnO nanowire process, the measurement was conducted for channel lengths of 1.3 µm, 8.6 µm and 18.6 µm. Well behaved output characteristics were also found at all channel lengths, with clearly defined linear and saturation regions as shown in Figure 5.9. The largest drain current is obtained for the FET with 1.3 µm ZnO channel length which corresponds to the shortest channel length. This is in a good agreement with the characteristic of ZnO TFT fabricated by Madzik et al. [24]. It is also seen in Figure 5.9 that the drain current exhibited increased in slope near saturation region as the channel length decreased. The poor saturation seen in Figure 5.9 for nanowire

FET with 1.3 µm channel length suggest the presence of short-channel effects, which have also been observed in ZnO-based TFTs [25][26].

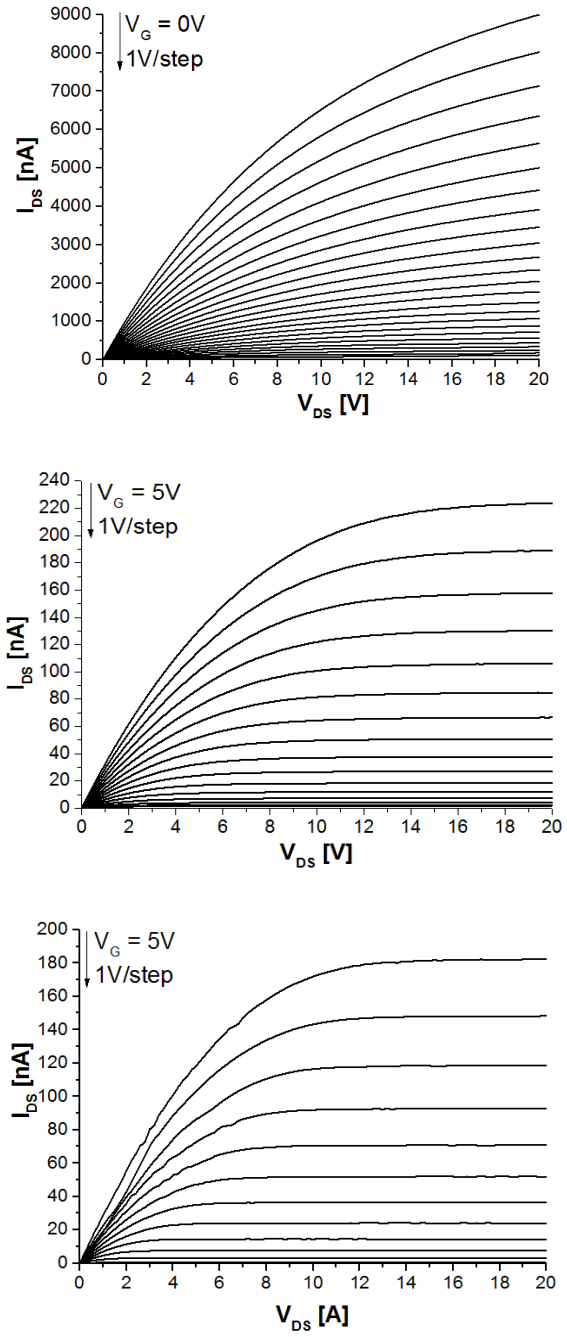


Figure 5.9 Output characteristics of ZnO nanowire FET comprising two parallel nanowires with channel lengths, L of (a) 1.3 µm (b) 8.6 µm (c) 18.6 µm.

Figure 5.10 shows subthreshold characteristics for ZnO nanowire FETs with different channel length at V_{DS} = 1.0 V. Subthreshold slope of 1600 mV/decade, 700 mV/decade, and 1800 mV/decade are obtained for the nanowire FETs with channel lengths of 1.3 µm, 8.6 µm, and 18.6 µm respectively. In conventional MOSFETs, the subthreshold slope is subject to the ratio of the gate capacitance to other capacitance such as interface

trap state capacitance and has a theoretical limit of ~ 60mV/decade [27]. Normally, a small subthreshold slope is require for low-threshold voltage, low-power operation. The relatively large subthreshold slope in his work can be due to the geometric effect of the ZnO nanowire and existence of surface trapping charge [28]. The subthreshold slope can be improved by using a top-gate configuration, using high-k dielectric material and/or passivating the surface of the nanowires [28]. In addition, the poor value of subthreshold slope observed for the 1.3 µm device can be explained by short-channel effect due to poor control of the channel by the gate as a result of the thick gate oxide [26].

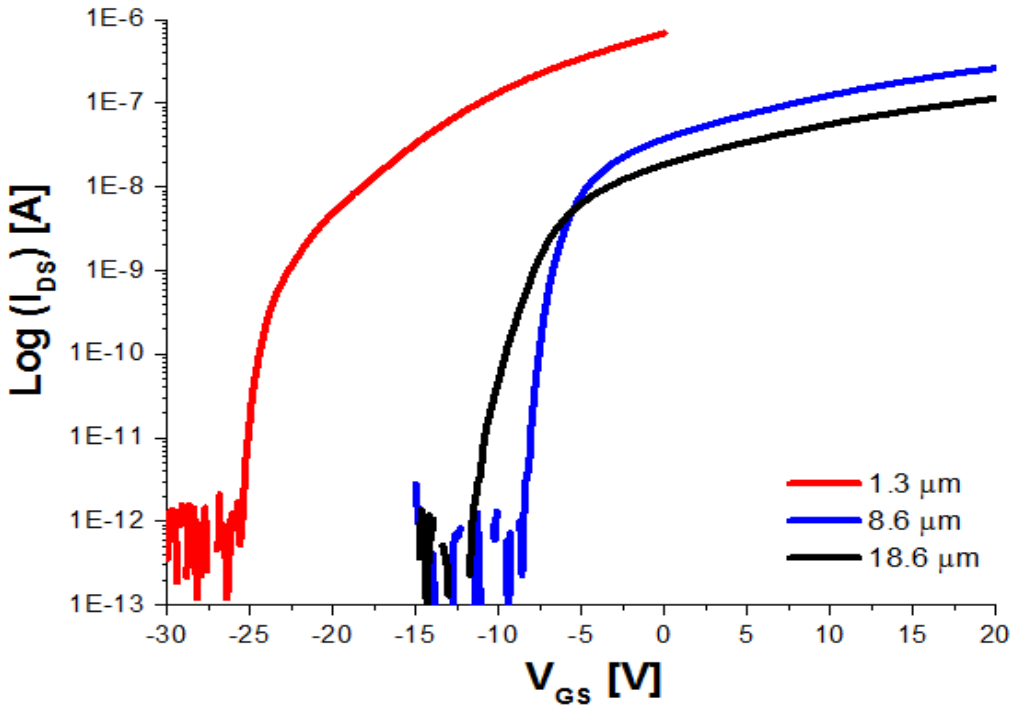


Figure 5.10 Transfer characteristics for devices with different channel lengths at V_{DS} = 1.0 V.

The electrical characteristics of reflow photoresist spacer method devices was also compared with the non-reflow photoresist spacer method devices. The comparison was based on the device with 8.6 µm length nanowires. Figure 5.11 show the source-drain current versus gate voltage (I_{DS}-V_{GS}) characteristics for both non-reflow and reflow ZnO nanowire FET. The measured subthreshold slope of 750 mV/decade given by the maximum slope in transfer curve in log scale and on-off current ratio of 10^6 at V_{DS} = 1.0 V was achieved from reflow device. The subthreshold slope of non-reflow device is 1030 mV/dec and current ratio is 10^3. Both non-reflow and reflow ZnO nanowires show typical n-type semiconductor behaviour, which is due to presence of some intrinsic defects [6]. The I_{DS}-V_{GS} curve show that the FET devices fabricated using non-reflow process exhibit a threshold voltage of 11.0 V indicating n-channel enhancement-mode operation. On the

contrary, ZnO nanowire FET fabricated from reflow process suggested an n-channel depletion mode operation with a threshold voltage of -6.0 V.

This result shows that the surface roughness can have a significant influence on the operation mode of ZnO nanowire-based FETs and associates with the presence of surface trap states or interface trap states [29]. The positive threshold voltage in non-reflow device is due to the deep traps in the nanowire channel or at the interface where the negative voltage from reflow device is attribute to delocalized electrons from shallow donors in the channel [30]. Note that from the Figure 5.11, ZnO nanowire FET from reflow process poses higher current, I_{DS}. The difference in electrical properties of both fabrication process is due to the scattering or trapping of the conduction electrons at the interfaces or close to the surface of the ZnO nanowire [29].

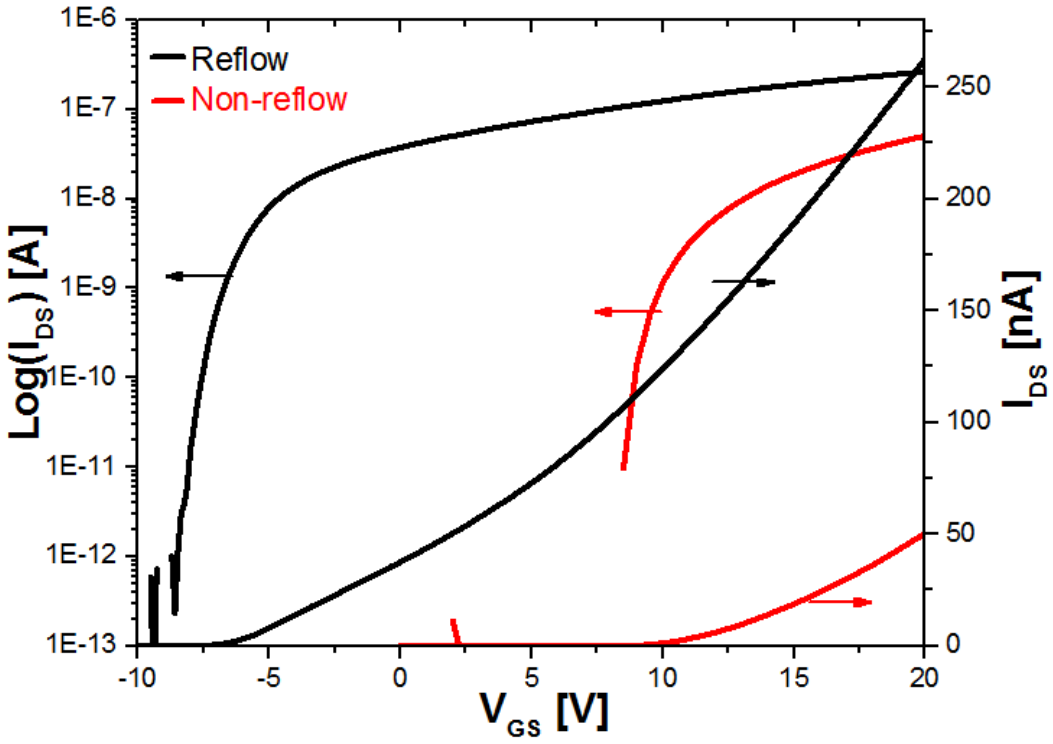
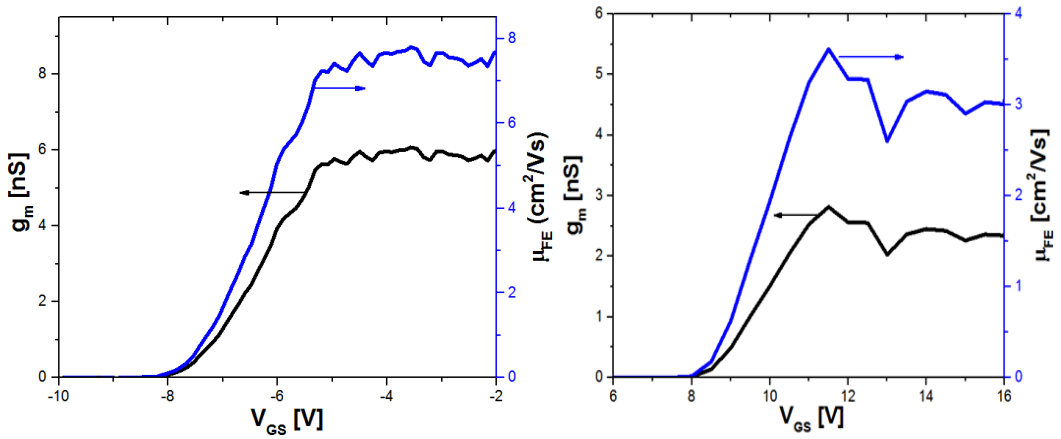


Figure 5.11 Semi-logarithmic and linear I_{DS}-V_{GS} characteristic of the reflow (black) and non-reflow (red) fabricated nanowire FET at V_{DS}= 1.0 V.

Figure 5.12 (a) and (b) shows the plot of the corresponding transconductance, $g_m = dI_{DS}/dV_{GS}$ curve obtained from transfer characteristics I_{DS}-V_{GS} and the calculated mobility as a function of gate voltage for n-channel depletion (reflow) and enhancement-mode (non-reflow) ZnO nanowire FETs. The field-effect mobility of FET based on reflow and non-reflow process are estimated to be 7.7 cm^2/Vs and 3.6 cm^2/Vs respectively. These results indicate that the field-effect mobility in the top-down ZnO nanowire FETs has correspond

not only on the surface roughness and will require further investigation. The field-effect mobility is calculated from the transconductance peak (Figure 5.12) at 5.9 nS and 2.8 nS following the method in [20]. Although the transconductance peak of the device from reflow process showed an improvement as compared to the device from non-reflow process, the capacitance of the two devices is different due to their respective back-gate oxide profiles. This characteristics is also reported by Hong et.al [29] based on the characteristic of their back-gate ZnO nanowire FET grown using bottom-up process. The next experiment discussed in Chapter 6 will include the optimization of the contact resistance in order to further improve the field-effect mobility of the devices.



(a) (b)

Figure 5.12 Transconductance (*gm*) and field-effect mobility (μ_{FE}) as a function of gate bias at V_{DS} =1.0 V for ZnO nanowire FET of (a) reflow and (b) non-reflow.

5.5 Conclusion

In summary, ZnO nanowire FET with SiO_2 gate dielectric of various thickness ranging from 25 nm to 100 nm were fabricated. The FETs with 100 nm thick gate dielectric layer exhibited lower I_{OFF} and steeper subthreshold slope than other FETs with thinner dielectrics. The FETs with 25 nm and 50 nm gate dielectric suffer from higher leakage current. It is because thinner gate dielectric suffer from diffusion of Zn into SiO_2 when depositing ZnO on a SiO_2. Therefore the insulation properties of SiO_2 layer is degrading. The SiO_2 layer of more than 50 nm is required under the ZnO layer to minimize the effect of the Zn diffusion on SiO_2. The optimized top-down fabrication process and sidewall photoresist smoothing have been shown to produce ZnO nanowire FET with good output electrical characteristics. This device is able to provide a high output drain current, low threshold voltage and steeper subthreshold slope than devices without smoothed

sidewalls. Electrical characteristic of the devices were strongly influenced by the surface morphology of ZnO nanowires. The electrical measurements of the device shows a strong depletion mode transistor, which starts to switch at -6.0 V gate voltage. The transconductance exhibits a value of 5.9 nS. In conclusion, the photoresist smoothing process has shown a significant improvement of the ZnO nanowire rms roughness by six times lower than the non-reflow process.

5.6 References

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Chapter 6:
Improving Performance of Top-down Zinc Oxide Nanowire FETs with AZO and Al bi-layer source/drain contacts

This chapter explains the enhanced performance of ZnO nanowire FETs by inserting a layer of Al-doped ZnO (AZO) between the ZnO nanowires and the Al source/drain contacts.

6.1 Introduction

In the previous chapter, a method to enhance the electrical performance of the ZnO nanowire FETs by reducing the surface roughness of the nanowires was discussed. However, the surface roughness is not the only issue that contributed to the variation of the electrical performance. Further enhancement of the ZnO nanowire FETs performance should be achieved by reducing the contact resistance, as the degradation of driving capability commonly results from the presence of high resistivity of the metal-semiconductor contact [1]. Contact resistance could decrease the voltage drop across the channel and limit the injected current [2]. High contact resistance in ZnO nanowire devices could lead to the deterioration of the device performance by thermal stress which probably cause device failures [3]. In addition, the bond between electrodes and ZnO nanowires could also cause variations in ZnO nanowire FETs electrical performance [4]. Formation of reliable and proper ohmic contacts for ZnO nanowire FETs with a low contact resistance is one of the important requirements to realize high performance ZnO nanowire FETs that have high field-effect mobility, high on/off current ratio, steep subthreshold slope and threshold voltage close to 0.0 V [4].

As channel length decreases, the resistance of the source/drain contact plays an important factor influencing the device performance including field-effect mobility, subthreshold slope (*SS*) and on/off current ratio [5]. Hence, it is required to optimize the source/drain contact to the nanowire in order to improve the electrical characteristics of ZnO nanowire FETs. A large research effort has been devoted to enhance the electrical properties of electrode materials by introducing new metal for electrodes such as Au, Ag, Mo and Ti to tailor the interface between the metal and the semiconductor channel [6]–[8].

The other popular method has been used to reduce the contact resistivity by thermal annealing [9][10] and Ar or H_2 plasma treatment [11][12].

Bang et al. [9] used a post-annealing method in ambient air at 250 ^oC for two hours to reduce the contact resistivity of their ZnO TFT with Ti/Au source/drain electrodes. Goldberger et al. [10] anneal their ZnO nanowire transistors at between 220 ^oC and 400 ^oC in O_2 to further lower the contact resistance of Ti/Au source/drain contacts to ZnO nanowires and even lower contact resistance of 6 x 10^{-4} Ωcm^2 have been reported in the literature using multilayer metal contact structures (Ti/Al/Pt/Au) on top of the annealing process [13][14]. Park et al. [11] proposed the use of Ar plasma treatment on amorphous indium gallium zinc oxide (a-IGZO) TFTs to reduce the contact resistance between the Pt/Ti source/drain electrode and a-IGZO. Even though the thermal annealing and Ar plasma treatment demonstrate an improved contact resistivity, the thermal annealing process could not be suitable to apply to the device that required a low temperature process [15]. Moreover, Ar plasma treatment is well-known in inducing surface damage on the semiconductor once inappropriate power of plasma treatment are involved [16]. Recently, conductive oxides from group III element (Al, Ga, and In) - doped ZnO have been suggested as transparent source/drain electrode due to its low resistivity on order of 10^{-4} Ωcm, good electrical conductivity and non-toxicity [1]. The most common conductive oxide materials used as transparent source/drain electrode are ZnO:Al (AZO) [1][17][18], ZnO:Ga (GZO) [19] and ZnO:In_2O_3 (IZO) [20]. There have been many works on conductive oxide source/drain electrodes on ZnO based thin film transistors for display applications and the most common method of deposition for those materials are based on radio-frequency magnetron sputtering [1][19][20].

In this work, a highly conductive layer of AZO deposited by atomic layer deposition (ALD) method was inserted between the ZnO nanowire and the source/drain contact as described in Chapter 4. Three different types of ZnO nanowire FETs were fabricated in order to investigate the viability of ZnO nanowire FETs using AZO as part of the source/drain contacts. The variation of the ZnO nanowire FETs include the device with and without the AZO layer and the integration of high-k dielectric material (Al_2O_3) into ZnO nanowire FETs. The ALD based Al_2O_3 will be combined with thermally grown SiO_2 to function as a gate-stack dielectric. The effect of the Al_2O_3/SiO_2 gate dielectric will be investigated with the aim to improve the electrical performance of ZnO nanowire FETs. In addition, the contact resistance values between Al/ZnO and Al/AZO interfaces were characterized by circular transmission line measurement (CTLM).

Annular ring and centre disc-structure contacts were used to measure the contact resistance at the Al/ZnO and Al/AZO interfaces. The properties of AZO film, field-effect mobility, on/off current ratio, threshold voltage, and subthreshold slope of the ZnO nanowire FETs with and without the AZO layer were systematically investigated. It was demonstrated that the ZnO nanowire FETs with the AZO layer shows the improved field-effect mobility and the subthreshold slope compared to the devices without the AZO layer.

6.2 Contact Resistance, R_C

The interface between Al contacts and both ZnO and AZO constitute contact resistances. It is a challenging task to model the contact resistance theoretically [21]. Therefore, it is usually measured experimentally by using transmission line model (TLM) or circular transmission line model (CTLM) structures [21]. In this work CTLM was used to extract the contact resistance at the Al/ZnO and Al/AZO interfaces. The advantage of using CTLM structures as compare to the linear TLM structure, is that there is no need for a physical (electrical) separation of the structure because the current can only flow between the two co-centric metals contacts [21]. A top-view schematic of the CTLM structures used to extract contact resistance is shown in Figure 6.1. The radial separation between the contacts were 20 µm, 40 µm, 60 µm, 80 µm and 100 µm. A 30 nm AZO thin film was deposited on 1 cm x 1 cm of 100 nm SiO_2/Si substrate. Then, 500 nm Al was evaporated to form the four contact points. Hall Effect measurement method was used to measure sheet resistance and verified by CTLM.

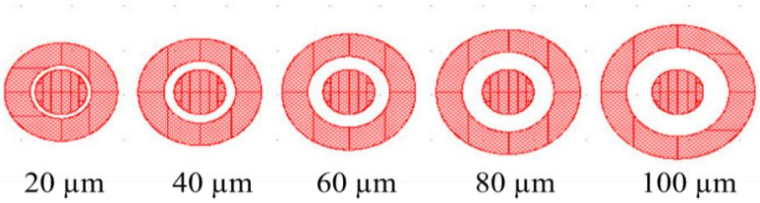


Figure 6.1. Mask layout of the CTLM structures used to determine the contact resistance.

The contact resistance, R_C is estimated by CTLM method [21]. The contact resistance of Al/ZnO and Al/AZO interface was determined using fabricated CTLM structure with a different spacing between the aluminum pad of 20 µm, 40 µm, 60 µm, 80 µm and 100 µm. The total resistance, R_T, between the contacts for the circular configuration is given by:

$$R_T = \frac{R_{sh}}{2\pi\,(r)}[s + 2L_T] \tag{6.1}$$

where R_{sh} is the sheet resistance of the semiconductor material on which the contact is made, r is the radius of the inner circular contact, s is the gap between inner and outer circular and L_T is the transfer length. L_T is the average distance that an electron or hole travels in the semiconductor beneath the contact before it flows up into the contact. Figure 6.2 illustrated r and s of the CTLM structures. The total resistance for different spacing of the aluminum pad is plotted in Figure 6.3. A linear fit is performed to these five points and then R_C, R_{sh} and L_T are obtained as described in Ref. [21]. The R_C and L_T are obtained from the intercept of a linear graph with y-axis and x-axis. The intercept with the y-axis yields $2R_C$ and the intercept with the x-axis yields $2L_T$. The value of specific contact resistance (ρ_c) can be then obtained by:

$$\rho_c = (L_T)^2 \times R_{sh} \tag{6.2}$$

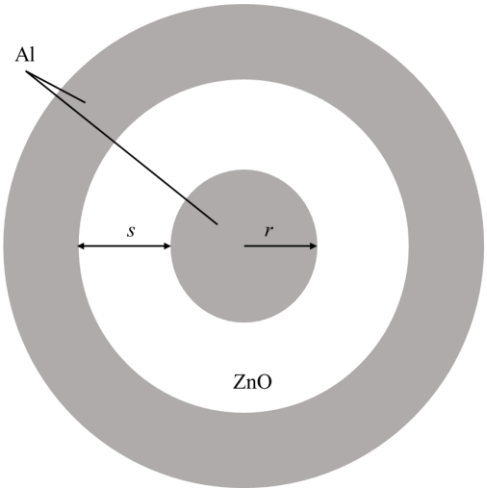


Figure 6.2 The schematic of top view of the CTLM which indicate the radius radius of the inner circular contact, r and the gap between inner and outer circular, s.

The specific contact resistance value of the Al/AZO and Al/ZnO are 1.4×10^{-3} $\Omega.cm^2$ and 8.8×10^{-3} $\Omega.cm^2$ and R_{sh} value were 1.04×10^{-3} Ω/sq and 6.4×10^{-2} Ω/sq respectively. Notably, ρ_c and R_{sh} values of the Al/AZO layer are lower than those with Al/ZnO layer. It shows that the device with the AZO layer has a better Ohmic contact than the device with the AZO layer. The low contact resistance of 9.6 Ω was achieved for the sample with the Al/AZO layer and the resistance of 191.4 Ω for the sample with the Al/ZnO layer. The use of the AZO layer as a bi-layer source/drain could realize a lower contact resistance in the ZnO nanowire FETs.

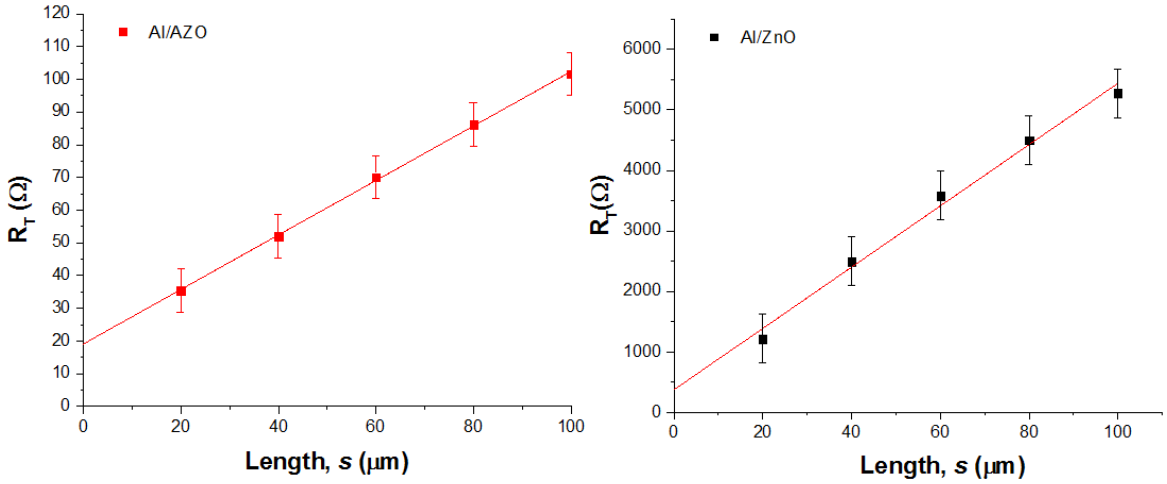


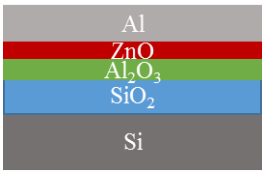
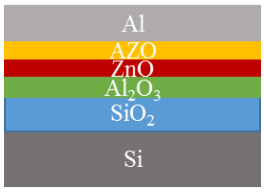
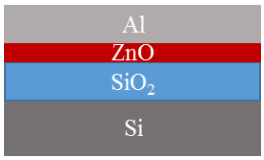
Figure 6.3 Resistance as a function of the distance between aluminum contact on AZO and ZnO.

6.3 Characterization of ZnO nanowire FETs with AZO and Al source/drain contacts

The electrical characterization was performed using a semiconductor device parameter analyzer (Agilent B1500A) in the dark at room temperature without annealing. Figure 6.4 shows the transfer characteristics of ZnO nanowire FETs with and without the AZO. The plotted graph is based on the ZnO nanowire with 2 µm length at V_{DS} = 1 V. The electrical characterization was performed using semiconductor device parameter analyser (Agilent B1500A) in the dark at room temperature without annealing. Figure 6.4 shows the transfer characteristics of ZnO nanowire FETs with and without the AZO. The plotted graph is based on the ZnO nanowire with 2 µm length at V_{DS} = 1 V. The extracted device electrical parameters are listed in Table 6-1. It can be seen that ZnO nanowire FETs with the Al/AZO bi-layer (sample 2) show the best electrical performance. The threshold voltage was obtained by extrapolating the linear region of the I_{DS} – V_{GS} curve from the point of maximum slope to a zero drain current, I_{DS}. Sample 3 shows a threshold voltage, V_{TH} of -16.0 V. After the Al_2O_3 was introduced in sample 1 as additional gate oxide layer, the V_{TH} shifts to 6.5 V. The V_{TH} shift could be attributed to higher density, smaller surface roughness, lower leakage current, and fewer interface defects. Kim et al. [6] also reported that the ZnO film deposited on the Al_2O_3 layer appear to have larger crystalline size corresponding to the full width at half maximum (FWHM) values than the ZnO film deposited on SiO_2. Thus, the ZnO film on Al_2O_3 has a larger grain size than a ZnO film deposited on SiO_2 [22][23]. The improvement in ZnO crystalline structure could cause the threshold shift after the Al_2O_3 layer was introduced. For sample 2, the V_{TH} is -11.0 V. The

fabrication of the device with bilayer source/drain electrode includes the passivation of the ZnO nanowires using Al_2O_3. The shift of the V_{TH} from 6.5 to -11.0 V is due to the effect of passivation. The un-passivated device experiences depletion from the adsorption of the oxygen ions that are negatively charged in the atmosphere. This causes the ZnO nanowire FETs to operate in an enhancement mode although it is expected for them to operate in a depletion mode [24]. The results demonstrate that the source/drain electrode have remarkable influence on V_{TH} and I_{ON}/I_{OFF} of ZnO nanowire FETs. The device with the Al/AZO source/drain electrode shows a higher I_{ON}/I_{OFF} ratio are attributed to the difference in the source/drain contacts.

Table 6-1 Comparison of device performance characteristics of ZnO nanowire FETs with and without AZO and the device without the gate insulator stack.

	V_{TH} (V)	SS (mV/dec)	μ_{FE} (cm^2/Vs)	I_{ON}/I_{OFF}
Sample 1 (Figure 4.9 (a))				
	6.5	480	3.5	1 x10^5
Sample 2 (Figure 4.9 (b))				
	**-11.0**	**170**	**85.7**	**1 x10^7**
Sample 3 (Figure 4.9 (c))				
	-16.0	670	1.2	1 x10^5

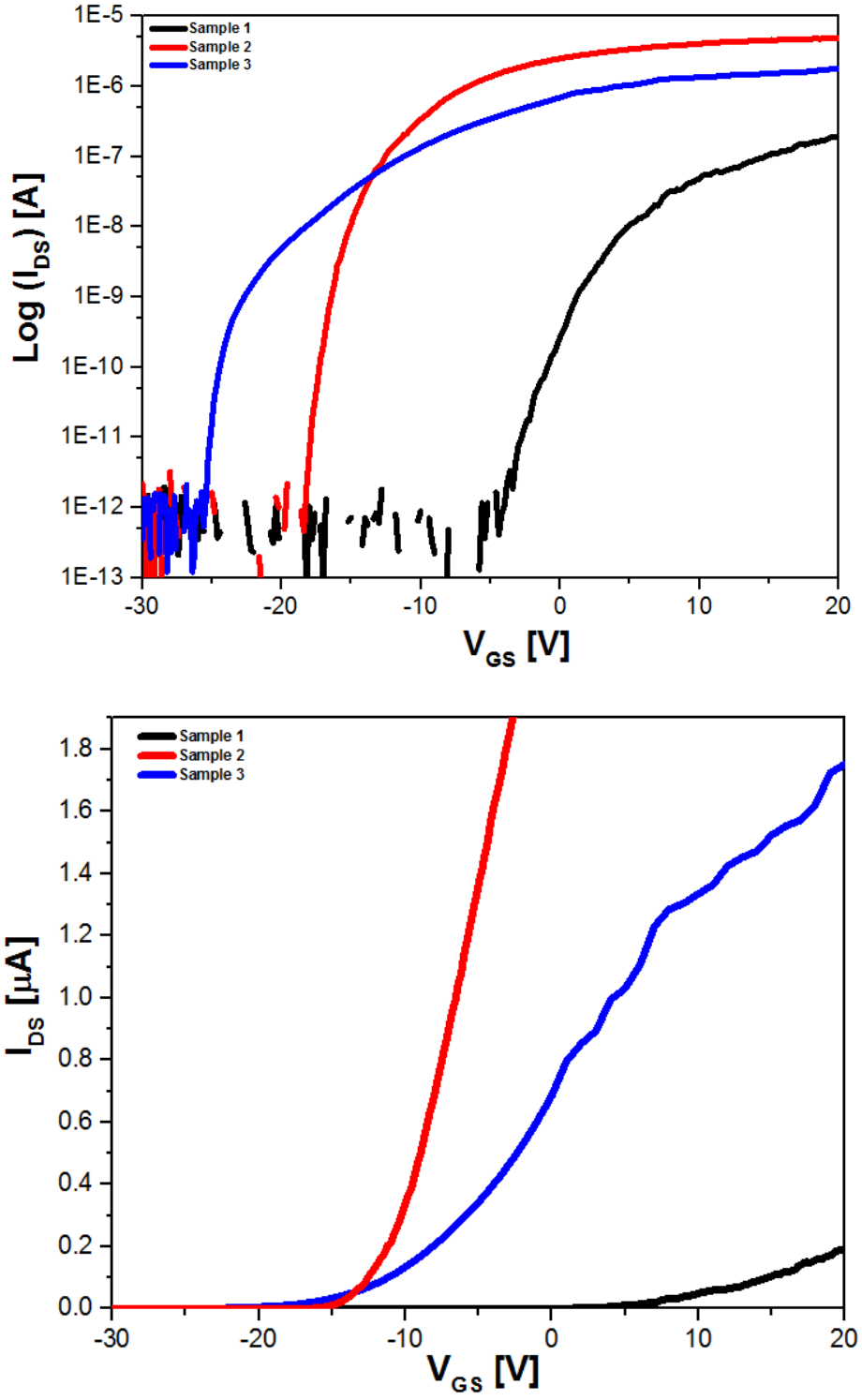


Figure 6.4 Semi-logarithmic (top) and linear (bottom) transfer characteristics of the ZnO NWFETs with and without AZO and with and without gate oxide stack at V_{DS} = 1.0 V.

The device with the Al/AZO source/drain electrodes (sample 2) exhibits a very steep subthreshold slope (*SS*) of 170 mV/decade and a high field-effect mobility, (μ_{FE}) of 85.7 cm^2/Vs at low operating voltage of 1.0 V, whereas the device without the AZO layer (Sample 1) exhibit value of SS = 480 mV/decade and μ_{FE} of 3.5 cm^2/Vs. These results

indicate that the insertion of AZO layer between source/drain contact and the ZnO nanowires reduces the contact resistance, (R_C) significantly, thus leading to the very steep subthreshold slope. Sample 3 with only SiO_2 and Al contact, exhibits the *SS* = 670 mV/decade and μ_{FE} of 1.2 cm^2/Vs. The ZnO nanowire FETs with the gate oxide stack of SiO_2/Al_2O_3 has exhibited a better performance than the device with only SiO_2. Kim et al., [22] has also observed an improvement of current-voltage characteristics of their ZnO TFTs with Al_2O_3 interlayer and performed X-ray diffractometer (XRD) analysis of the ZnO films. Based on their XRD analysis, the ZnO films on the Al_2O_3 substrates shows the higher intensity of the (002) peak and larger crystalline size corresponding to the full width at half maximum (FWHM) values than the ZnO films deposited on SiO_2 [22]. The ZnO film deposited on Al_2O_3 has a larger crystalline than the ZnO films deposited on the SiO_2, thus, reducing the defects such as oxygen vacancy, interstitial and dislocation [22]. As a result, the improved electrical characteristics could be due to the crystalline improvement where the ZnO film deposited on the Al_2O_3 layer has a larger crystalline structure than the ZnO film deposited on SiO2 thus, reducing the defects such as oxygen vacancy, interstitial and dislocation [22]. Kim et al. also witnessed a ZnO film with high crystalline quality could have been grown on Al_2O_3 based on their XRD analysis [23]. The improvement of the *SS* could also be attributed to the lower interfacial trap density at the interface of gate oxide/ZnO [25]. This result could be verified by TEM in future work.

The μ_{FE} was determined by the maximum transconductance at a constant drain voltage and calculated from the following equation;

$$\mu_{FE} = \frac{\partial I_{DS}}{\partial V_{GS}} . \frac{L}{W . C_{ox} . V_{DS}} \tag{6.3}$$

where C_{ox} denotes the effective capacitance of the gate insulator per unit area; L and W represent the channel length and the width, respectively. I_{DS}, V_{GS} and V_{DS} correspond to the drain current, the gate voltage, and the drain voltage, respectively. The C_{ox} was calculated as a series capacitance of SiO_2 and Al_2O_3 for the device with gate oxide stack. The capacitance is calculated as described in Ref. [26].

Figure 6.5 shows the plot of the transconductance, $g_m = dI_{DS}/dV_{GS}$ obtained from transfer characteristics (I_{DS} – V_{GS}) and the calculated mobility as a function of gate voltage for ZnO nanowire FETs with and without AZO layer. The improvement in the field-effect

mobility indicates that the Al/AZO bi-layer contact has lower traps and interface charges at the interface between the ZnO layer and the source/drain electrode [27]. Insertion of a layer with a high carrier concentration between the ZnO nanowire channel and the source/drain electrodes reduces the contact resistance, consequently leading to the improvement of μ_{FE} [28]. This was also observed by Masuda et al. in their transparent ZnO TFTs [28].

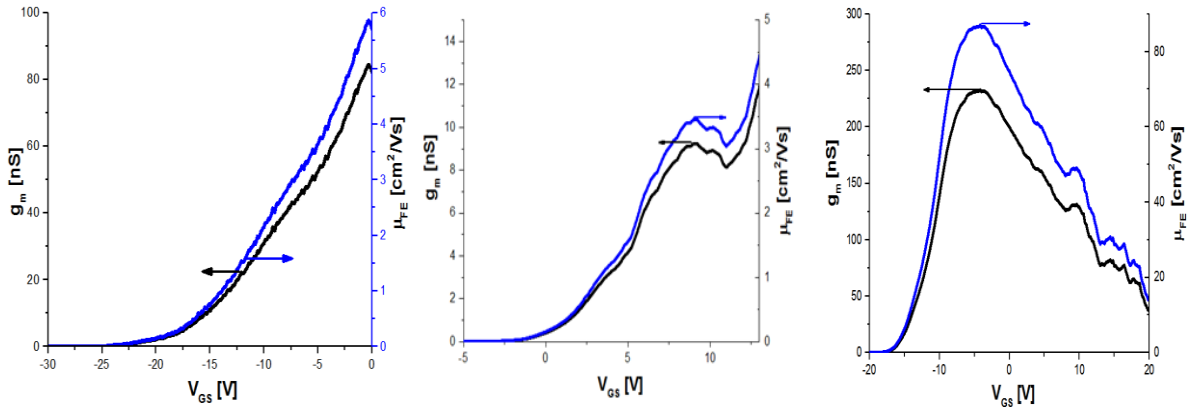
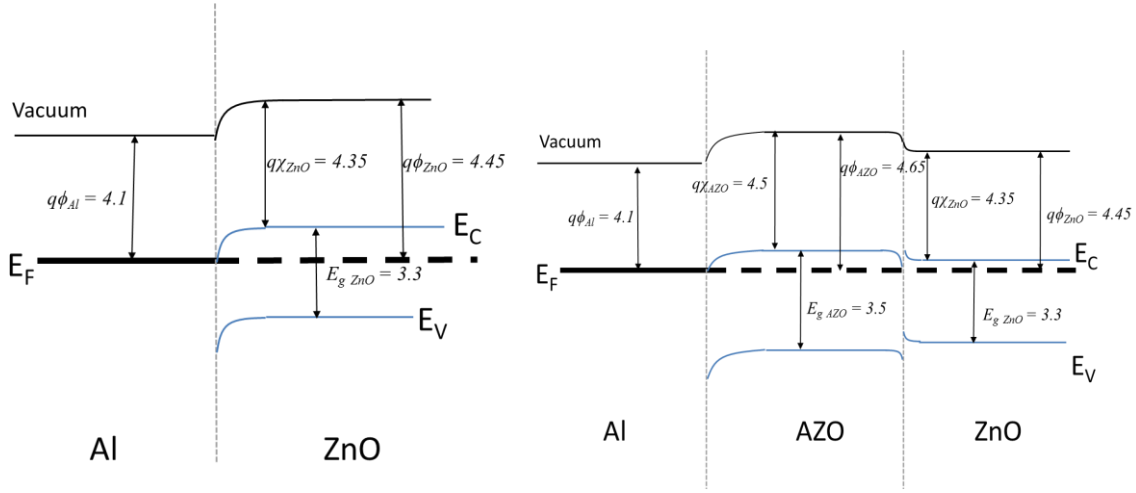


Figure 6.5 Transconductance (g_m) and field-effect mobility (μ_{FE}) as a function of gate bias at V_{DS} = 1.0 V for ZnO nanowire FETs (a) with Al electrodes and SiO_2 gate oxide (b) with Al electrodes and Al_2O_3/SiO_2 gate oxide (c) with Al/AZO electrodes and Al_2O_3/SiO_2 gate oxide.

The AZO layer between the Al contact and ZnO nanowires shrinks the depletion region significantly and makes carrier tunnelling possible through the Al contact structure [3]. Energy band diagram of a metal-semiconductor interface without the AZO layer is shown in Figure 6.6(a). In this diagram, the energy band gap, E_g for ZnO and AZO is taken as 3.3 eV [29] and 3.5 eV [30] respectively, and electron affinity, qχ is 4.35 eV [31] and 4.5 eV [32] for ZnO and AZO respectively. Furthermore, the ZnO work function, $q\phi_{ZnO}$ is 4.45 eV [33] and for AZO, $q\phi_{AZO}$ is 4.65 eV [30]. Since the ZnO has a lower electron concentration of around 10^{17} cm^{-3} as compared to the AZO around 10^{20} cm^{-3} based on Hall measurements, the relatively large depletion width underneath the Al metal leads to a high barrier height, ϕ_{Bn}, and causes the high contact resistance which could also be associated with a high density of interface states at the surface of ZnO nanowires [2]. When the AZO layer was inserted between the Al metal and the ZnO nanowires, the depletion layer below the Al metal decreases significantly. The barrier height of the Al/AZO is lower than at the Al/ZnO interface as shown in the possible energy band diagram of the Al/AZO/ZnO system in Figure 6.6(b). A tunnelling-field emission at the Al/AZO interface and

thermionic-field emission at the AZO/ZnO interface are also indicated. Hence, Al/AZO/ZnO interface deliver a more efficient electron transport as compare to the Al/ZnO interface.



(a) (b)

Figure 6.6 Energy band diagram of contact system in the case of the ZnO nanowire FETs with and without AZO.

6.4 Temperature-Dependent Electrical Characterization of ZnO Nanowire FETs with AZO and Al Source/Drain Contacts

The device with AZO and Al source/drain contact were further investigated by measuring the temperature dependence of their electrical characteristics. The purpose of this measurement is to understand the carrier transport mechanism in ZnO nanowires. Temperature reduction in the device allows a significant increase of carrier mobility, lower power consumption, decrease of leakage current, reduces thermal noise and increased thermal conductivity [34]. As an example, if the device can work properly in the temperature range below 300 K, this device can be used to build active matrix displays on plastic substrates. The temperature dependence of electrical properties was evaluated by measuring the transfer characteristics of the ZnO nanowire FETs in the dark at different temperatures and under vacuum condition. The linear transfer curve and the output characteristics of devices were measured in the temperature range between 200 K and 300 K. Subsequent measurement cycles were done in order to guarantee that the variation of drain current was due to the temperature difference and not to instability effects. The measured device is based on the ZnO nanowire with 2 µm length. The lowest temperature for measurement was 200 K, which could be due to the back-gate carrier freeze-out.

Carrier freeze-out occurs in the temperature where the thermal energy within the semiconductor is not enough to fully ionize the impurity atoms [35].

Figure 6.7 shows the semi-logarithmic of the linear transfer characteristics measured in the range from 200 K to 300 K at fixed V_{DS} of 1.0 V. As seen in this figure, the drain current in the entire V_{GS} region increases with increasing temperature. The transfer curves show a parallel shift to more negative voltages indicating a reduction of the flat-band voltage [36].

The threshold voltage and subthreshold slope as a function of temperature are shown in Figure 6.8. From Figure 6.8, it reveals that as the temperature increase from 200 K to 300 K, the V_{TH} decreased from 7.0 V to -2.0 V. At higher temperature, more electrons can escape from localized states and contribute to the free carrier, which causes a decrease of V_{TH} [37][38]. The V_{TH} and *SS* trend exhibit a slight increase at certain temperature. The V_{TH} is related to the slope of the drain current in linear region, small changes in drain current caused the non-linear changes in V_{TH}. This may have happened due to the trap density or the defect states existed during the fabrication process. The same trends have also been observed by Heo et al. [37] in their amorphous indium-zinc-oxide (*a*-IZO) TFTs. The other possible reason is due to the surface roughness [39]. However, since ZnO is a temperature dependent semiconductor, the surface roughness decreased as the temperature increased. As compared to the device measured at room temperature in ambient air, the V_{TH} is shifted towards more positive voltage. These is due to reduction of oxygen trapping effects on the nanowire surface. This results also suggest that the charge transport characteristics of the ZnO transistor is sensitive to the environmental conditions. The obtained result agree with those presented elsewhere [40][41].

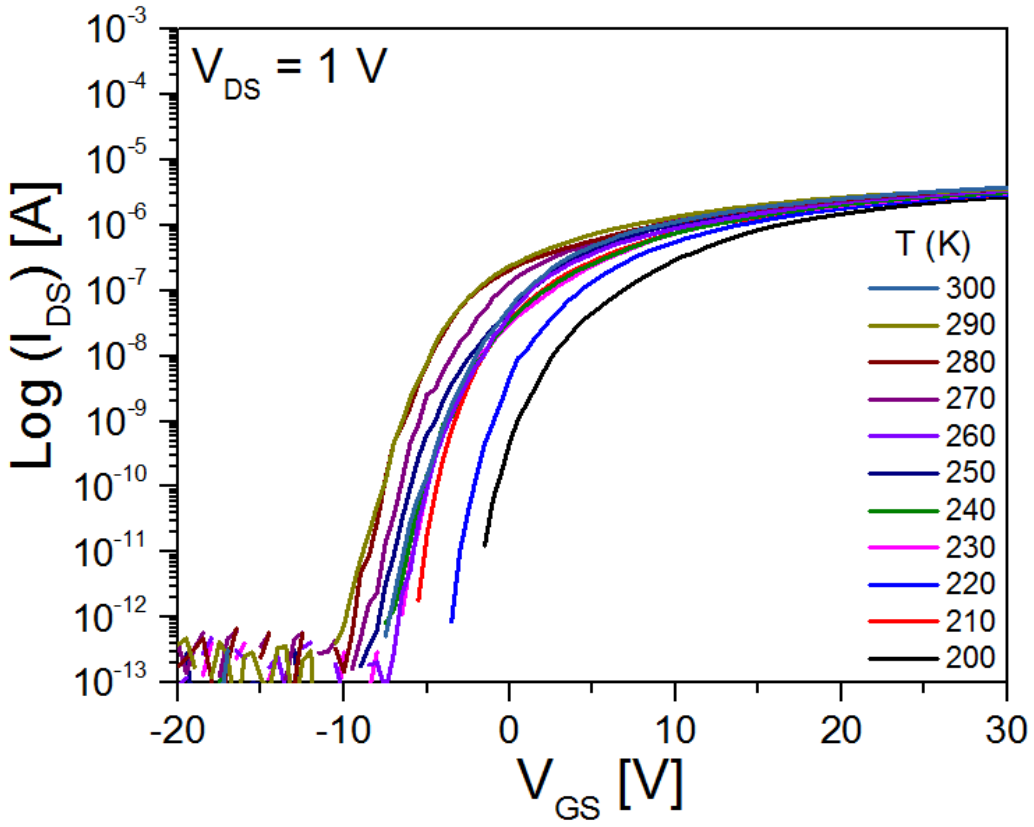
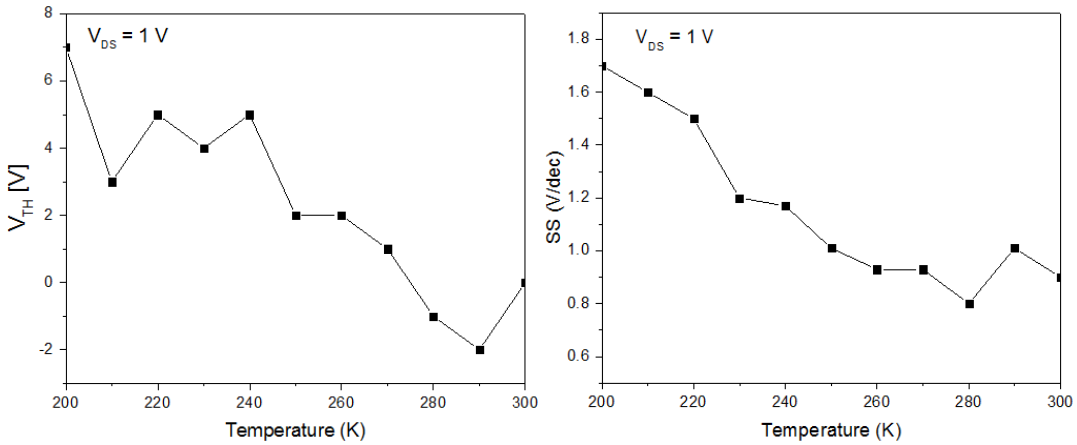


Figure 6.7 Transfer characteristics of ZnO nanowire FET in the temperature range from 200 K to 300 K measured at V_{DS} = 1.0 V.

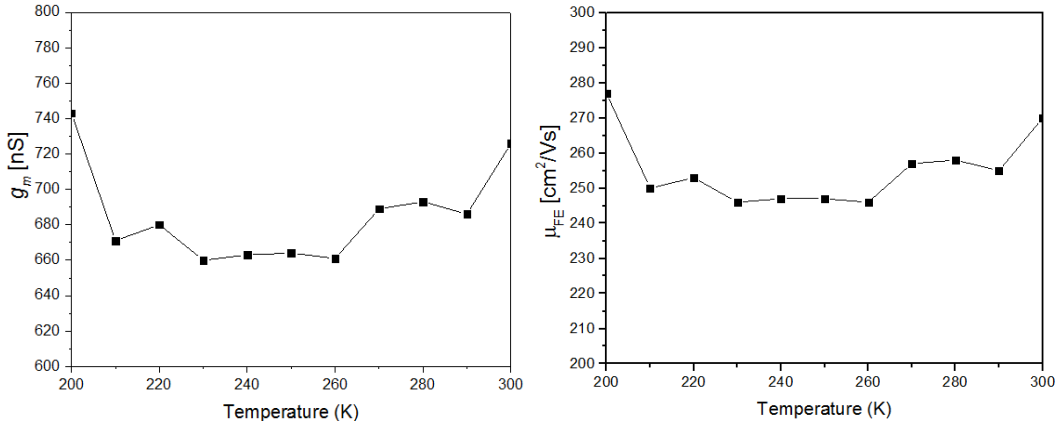


(a) (b)

Figure 6.8 Temperature dependence of a) threshold voltage and b) subthreshold slope V_{DS} = 1.0 V.

Figure 6.9 shows the plot of extracted transconductance peak and field-effect mobility against temperature. The graph (Figure 6.9 (a)) shows the g_m values range between 743 nS to 660 nS. The highest trasnconductance peak was observed at temperature 200 K. Then the transconductance peak started to decreased at temperature of

210 K and maintain at slightly the same value until at 290 K. At 300 K, the transconductance peak increased to 726 nS. The plot in Figure 6.9 (b) shows the correlation between field-effect mobility and temperature. The device measured at 200 K exhibits highest μ_{FE} of 277 cm^2/Vs for dual nanowires and lowest value of 246 cm^2/Vs for dual nanowires was measured at 230 K. These μ_{FE} values shows an excellent improvement as compared to the μ_{FE} extracted from the transistors measured at room temperature in ambient air. Wang et al [40] suggested that one possible justification is that the traps limit the charge transport when the ZnO nanowire exposed to ambient air. The improvement of the μ_{FE} when measured in specific temperature under vacuum condition is due to reduction of oxygen trapping effects on the nanowire surface. This results also suggest that the charge transport characteristics of the ZnO transistor is sensitive to the environmental conditions. The obtained result agree with those presented elsewhere [40][41]. The improvement of the μ_{FE} could also be attributed to reduction of contact resistance and increased thermionic emission due to low temperature [42].



(a) (b)

Figure 6.9 (a) Transconductance peak vs. temperature and b) extracted field-effect mobility vs. temperature at V_{DS} = 5.0 V.

In Figure 6.10, a similar behaviour of transfer curves parallel shifting for the transfer curve near to saturation region. The similar V_{TH} shift is also been observed in the plot, although the shift to the left is slightly smaller than the shift in the linear region.

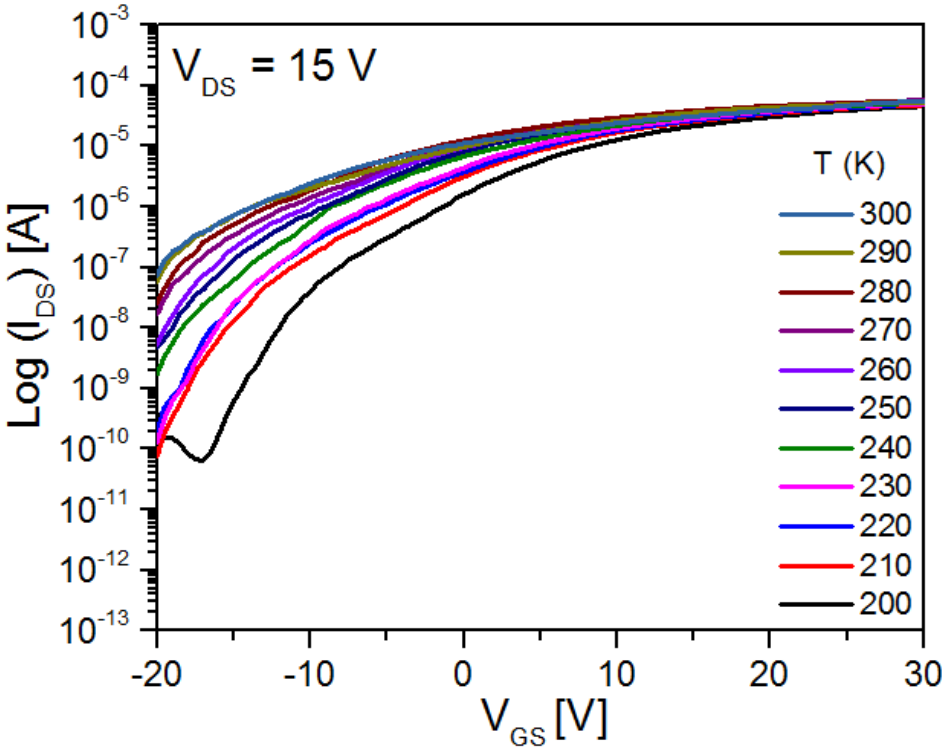


Figure 6.10 Transfer characteristic at V_{DS} = 15.0 V in the temperature range from 200 K to 300 K in semi-logarithmic plot.

Typical behaviour of the output characteristics with different temperature is shown in Figure 6.11. For gate voltage, V_{GS}. = -5 V to 25 V, it is observed that the drain current increased with the temperature due to the reduction of the $V_{TH,}$ that has been observed earlier from the transfer characteristics in Figure 6.7. However, an interesting effect is observed in output characteristics at temperature 280 K and 300 K for V_{GS}. = 15 V and 25 V. The drain current at temperature 280 K is slightly higher than the drain current at temperature 300 K for V_{GS}. = 15 V and 25 V. They did not increase linearly as the temperature increased. This may have happened due to the effect of increasing V_{TH} at temperature of 300 K. Estrada et al. [38] also observed slight non-linearity in their output characteristics at higher V_{GS}. The non-linearity is due to increasing R_S with temperature and reduction of V_{TH} [38].

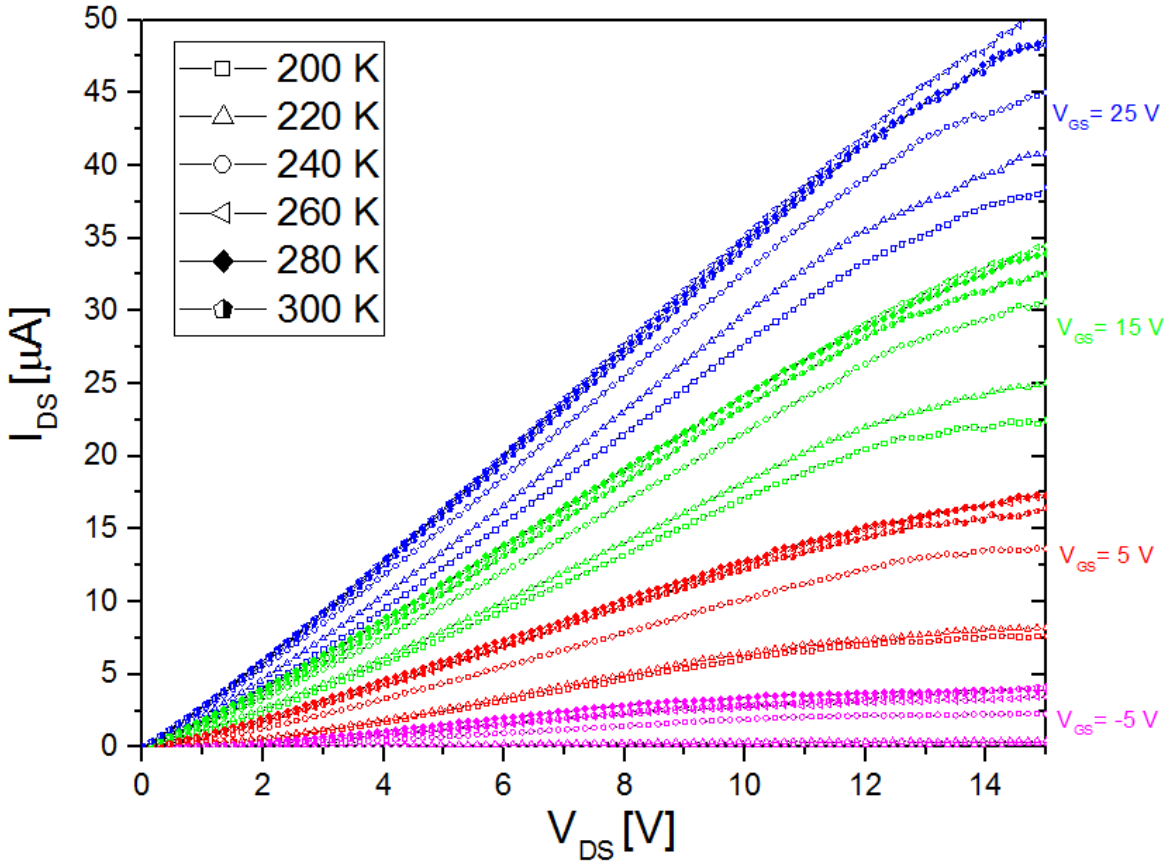


Figure 6.11 Output characteristics in the temperature range from 200 K to 300 K at different V_{GS}.

6.5 Conclusions

A bi-layer source/drain contact was applied to further improve the performance of the ZnO nanowire FETs. The source/drain region has been overlaid with a highly conductive AZO layer prior to the deposition of Al contact. The CTLM method was used to estimate the source/drain contact resistance. The measured results shown that the contact resistance of Al/AZO decreased to 9.6 Ω thus indicating a better ohmic contact in the bi-layer source/drain structure. The ZnO nanowire FETs with the AZO layer as the source/drain contact have thus exhibited enhanced performance when compared to the ZnO nanowire FETs without AZO layer. Their field-effect mobility has increased above 96% and the subthreshold slope reduces more than one third. These results have demonstrated that the AZO thin film is an excellent choice for the source/drain contacts to fabricate high performance ZnO nanowire FETs. The behaviour with temperature of the electrical characteristics of ZnO nanowire FETs with AZO thin film is measured. It is seen that up to 300 K, the transfer curves show a parallel shift toward more negative gate

voltages. The V_{TH} decreased due to the temperature increments which is characteristic of ZnO nanowire FETs.

6.6 References

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Chapter 7:

Towards RF Characteristics of ZnO Nanowire FETs

This chapter discusses the electrical characteristics of the ZnO nanowire FET fabricated with different gate length. It was also fabricated with micrometre size ground-signal-ground for RF properties evaluation of ZnO nanowire FETs. This chapter only presents the DC characteristics of the ZnO nanowire FETs.

7.1 Introduction

A lot of study regarding ZnO TFT for display applications has been demonstrated due to its attractive characteristics, such as high mobility, high on/off current ratio and low process temperature[1]–[3]. However, as high resolution and fast response displays that operate at high speed are being introduced, higher mobility transistor are required to provide the necessary switching speed. High mobility transistor is shown to be feasible using ZnO [4], gallium indium zinx oxide (GIZO) [5], zinc tin oxide [6] and $InGaO_3$ [7] thin film, which led to the fabrication of TFT-based high speed logic circuits [8]–[10]. As higher speed needed for fast switching, nanowire-based transistor seem to be promising candidates because of its small size and tend to have higher mobility [11]. The dc characteristics of the ZnO-based nanowire transistor is well-known. The RF characterization of the ZnO transistor has been reported before, but all reports are based on ZnO-based thin film transistors However, the RF characterization of the ZnO-based nanowire transistor has rarely been revealed.

In this work, the prototype ZnO nanowire FETs for RF characterization were fabricated based on the novel top-down fabrication process. The fabrication process involve the direct photolithography and lateral wet etching technique to fabricate the nanowires. The details of the fabrication process is discussed previously in Chapter 4. The electrical characteristics of the transistors with gate length of 2 µm, 2.5 µm, 3 µm, 3.5 µm and 4 µm will be discussed to further understand the fabrication issues towards achieving ZnO nanowire FET with RF characterization.

7.2 Electrical Characterization

The fabrication process of the ZnO nanowire FETs for RF characterization have been discussed previously in Chapter 4. The devices were DC characterized using semiconductor device analyser (Keysight B1500A) in the dark at room temperature. The ZnO nanowire FETs have been fabricated with different gate length from 2.5 µm to 4 µm. All the device have been electrical characterized, where they showed excellent field-effect transistor behaviour. I_{DS}-V_{GS} measurements were performed for the extraction of threshold voltage, subthreshold swing, transconductance and field-effect mobility. Hereby, transfer characteristic measurements have been performed for ZnO nanowire FETs with gate lengths of 2 µm, 2.5 µm, 3 µm, 3.5 µm and 4 µm. Figure 7.1 illustrated the definition of gate length = 2 µm for ZnO nanowire FETs.

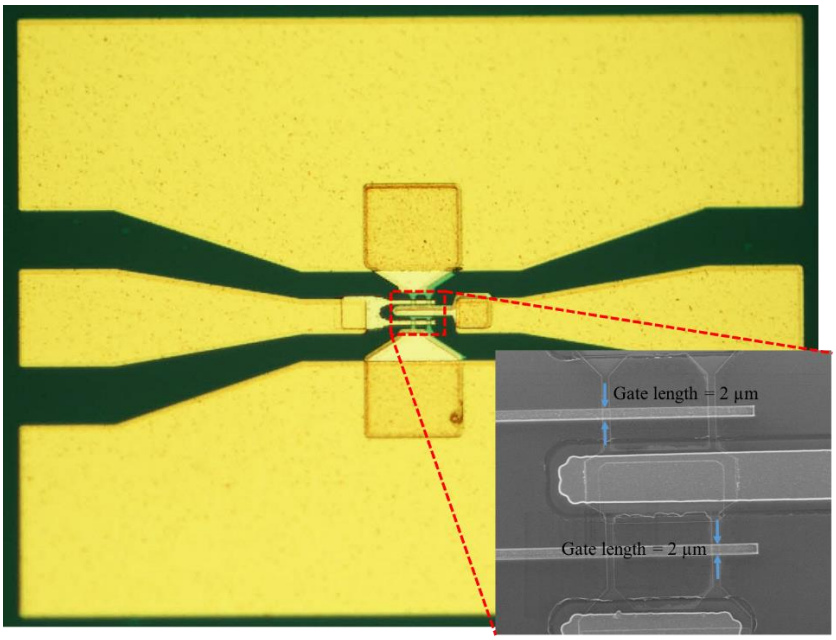


Figure 7.1 Top-view image of the ZnO nanowire FET with gate length = 2 µm.

Figure 7.2 shows the transfer characteristics for ZnO nanowire FETs with gate lengths between 2.5 µm to 4 µm at V_{DS} = 1.0 V. All curves show a threshold voltage close to 0 V. All devices show a saturation at V_{GS} = 5.0 V. Based on transfer curves, the ZnO nanowire FETs in this experiment does not show a good scaling behaviour. The output drain current for the device with good scaling behaviour will increase linearly with the reduction of the gate lengths. Furthermore, the threshold voltage will shift to more negative as the gate lengths decreased. This behaviour could be due to the variations or imperfections introduced during fabrication process. In addition, when the gate length of

the transistor is below 5 µm, the contact effect may seriously affect the transistor performance [12].

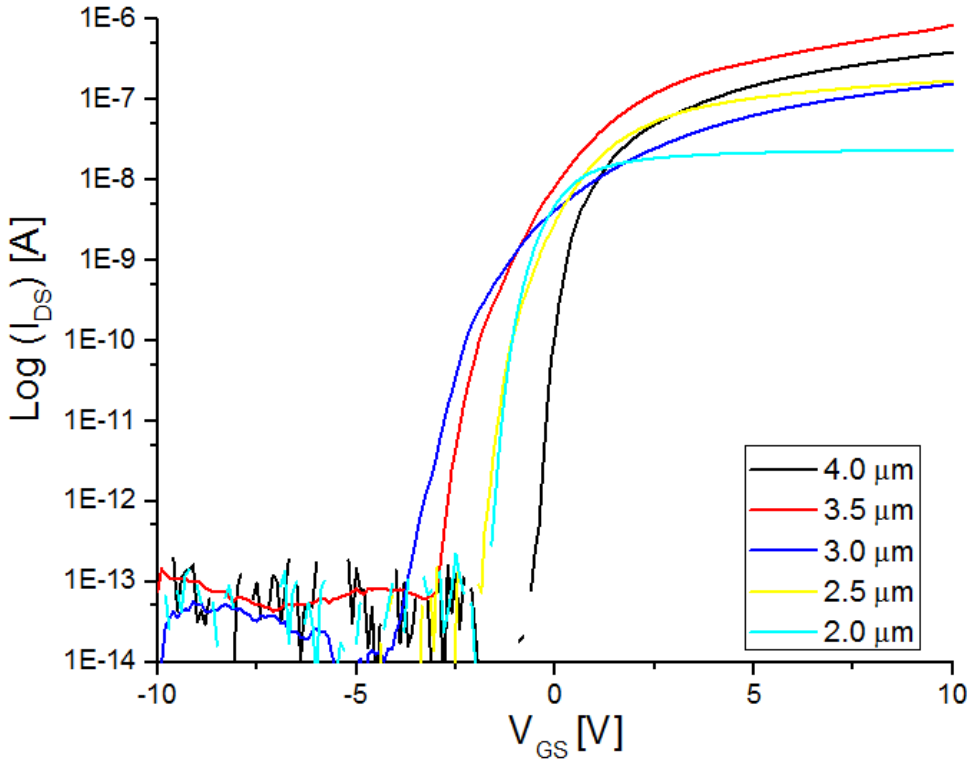


Figure 7.2 Transfer characteristics of ZnO nanowire FETs with gate lengths between 2.5 µm to 4 µm at V_{DS} = 1.0 V in semi-logarithmic plot.

The extracted device electrical parameters with applied drain voltage of 1.0 V are listed in Table 7-1. The fabricated devices exhibits good electrical characteristics except for the low field-effect mobility. From Table 7-1, it can be seen the ZnO nanowire FET with gate length of 3 µm and 4 µm exhibits excellent on/off current ratio of $1x10^7$. It can be seen that μ_{FE} values increase with enlarging the gate length. The highest μ_{FE} was observed with 0.48 cm^2/Vs with 3.5 µm gate length. The V_{TH} of the ZnO nanowire FETs shift slightly towards positive voltage as the gate length dimension increased. Only the device with 2 µm gate length shows a depletion mode operation. The other ZnO nanowire FETs show an enhancement mode operation. The subthreshold slope is measured between the output current of 10 pA and 100 pA at V_{DS} = 1.0 V. The variation of the subthreshold slope is very little. The ZnO nanowire FET with 4 µm exhibits steepest subthreshold slope of 210 mV/decade.

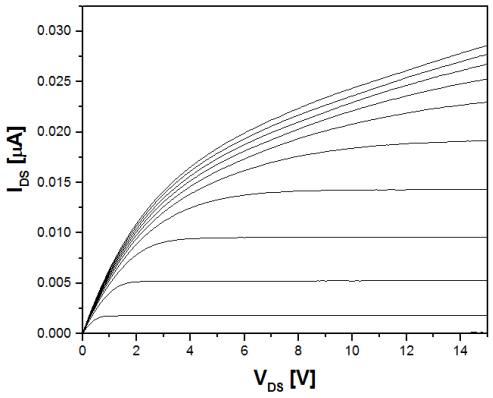
Table 7-1 Electrical characteristics of ZnO nanowire FETs with gate lengths varies from 2.5 µm to 4 µm at V_{DS} = 1.0 V.

Gate length (µm)	V_{TH} **(V)**	***SS*** **(mV/dec)**	μ_{FE} **(cm^2/Vs)**	I_{ON}/I_{OFF}
2.0	-0.7	300	0.04	$1x10^5$
2.5	0.4	250	0.13	$1x10^6$
3.0	0.5	280	0.10	$1x10^7$
3.5	0.8	290	0.48	$1x10^6$
4.0	1.5	210	0.24	$1x10^7$

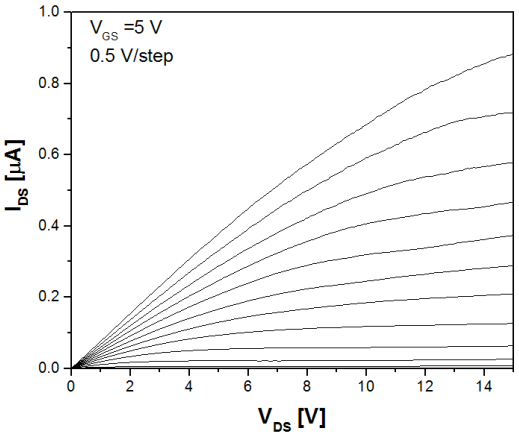
The cause of the enhancement mode could be due to the grain boundaries and trapped interface charges between the ZnO and the Al_2O_3. Study on ZnO thin film structures have revealed a solid relation between atomic structures and electrical characteristics [13]. Blatter and Geuter [14] assumed that double Schottky barriers form at every grain boundary, which affects the dynamic and static properties of the carrier transfer. Acceptor and donor states, known as deep traps contribute to the charge at the interface of the channel. Acceptor states show a neutral electrical behaviour when empty and become negatively charged when trapping electrons. In contrast, donor states become positive charge by emitting an electron [14]. As a result of trapping the numbers of carriers and electrical performance of the transistor degrades. The electrical field generated by charged interface cause the band bending at the adjacent grain to rise up [14]. In other work, Hossain et al. [15] demonstrated a simulation model, which exhibits the relation of the number of grain boundaries to the electrical performance of ZnO TFTs. When the number of the grain boundaries increased, the distance between them reduced until the depletion region overlap to each other. Consequently, the minimum conduction band edge becomes lifted up to form the equilibrium Fermi level, which leads to a reduced concentration of thermally activated carries. This effect causes a lower field-effect mobility of the transistor and effects the resistance of the nanowire channel [16][17]. As a result, the transistor operation mode will shift from a depletion mode to an enhancement mode operation.

Figure 7.3 shows output characteristics for ZnO nanowire FETs with gate length varying from 2 µm to 4 µm. The output curve measured at V_{DS} from 0 V to 10 V exhibits clear pinch-off and saturation, indicating that the device follows the standard field-effect transistor theory and that the Fermi level in the channel is controlled by the gate voltage

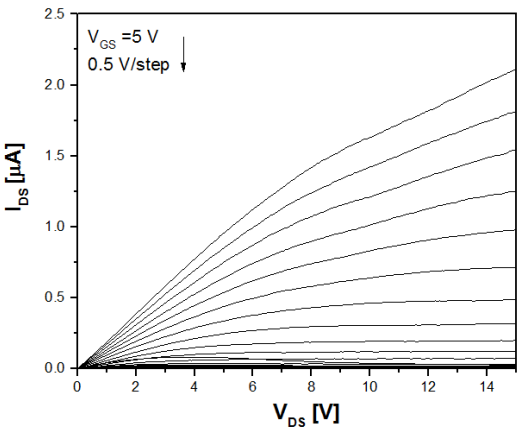
and the drain bias [5]. It can be seen that the largest drain current is obtained for the transistor with 3.5 µm gate length, which correspond with the highest field-effect mobility obtained by this device. At drain bias of 15 V and a gate bias of 5 V, excellent drain current of 0.03 µA, 0.9 µA, 2.1 µA, 6.8 µA, and 2.6 µA are obtained for gate length of 2 µm, 2.5 µm, 3 µm, 3.5 µm, and 4 µm respectively. From the output characteristics, current crowding can be observed at high gate voltage for transistor with 2 µm gate length, indicating the present of high contact resistance.



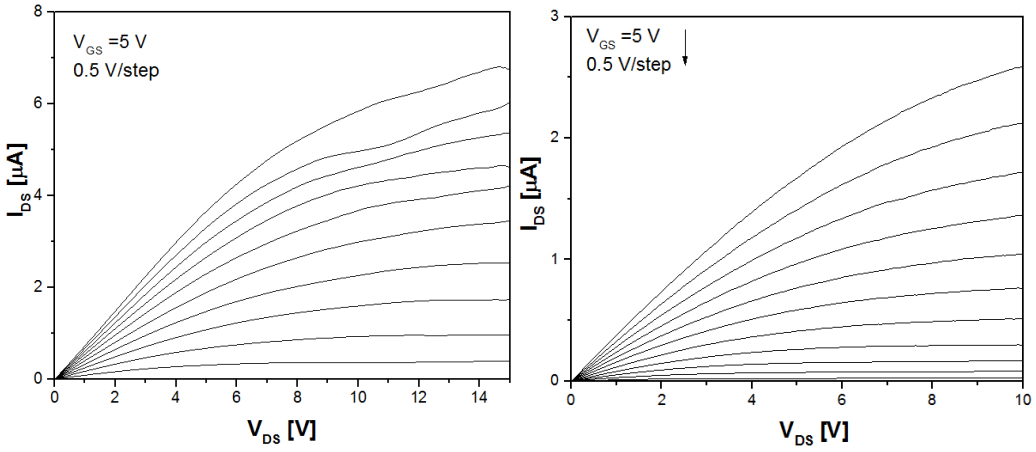
(a)



(b)



(c)



(d) (e)

Figure 7.3 Output characteristics of nanowire transistor with gate length of a) 2 µm, b) 2.5 µm, c) 3 µm, d) 3.5 µm, and e) 4 µm.

Table 7-2 summarises the parameters obtained from electrical measurement on the transistor fabricated with AZO and Al source/drain contacts described previously in Chapter 6 and transistors fabricated by lateral wet etching technique. The comparison is based on ZnO nanowires with 2 µm gate length. The threshold voltage of the AZO/Al source drain contacts nanowire transistor is -11 V, compared with -0.7 V for the nanowire transistor fabricated by lateral wet etching and field effect mobility is 85.7 cm^2/Vs compared with 0.04 cm^2/Vs respectively. The subthreshold slope of the nanowire transistors with AZO and Al source/drain contacts exhibit more than 1.5 times steeper than the subthreshold slope for the transistors fabricated by lateral wet etching. The on/off current ratio for nanowire transistors with AZO and Al source/drain contact is $1x10^7$ which is two magnate higher than the on/off ratio for nanowire transistor fabricated by lateral wet etching.

Table 7-2 Comparison of electrical characteristics of ZnO nanowire FETs by lateral wet etching and device with AZO/Al source drain contacts

	ZnO nanowire FET with AZO and Al source/drain contacts (2 µm gate length)	**ZnO nanowire FET by lateral wet etching (2 µm gate length)**
V_{TH} **(V)**	-11.0	-0.7
SS **(mV/dec)**	170	300
μ_{FE} **(cm^2/Vs)**	85.7	0.04
I_{ON}/I_{OFF}	$1x10^7$	$1x10^5$

The insertion of AZO and Al source/drain contact gives a significant improvement in field effect mobility than the transistor fabricated by lateral wet etching technique, which correlates with lower traps and interface charges at the interface between the ZnO layer and the source/drain contacts [19]. This correlation suggests that the field effect mobility in nanowire transistors is limited by interface traps and charges between ZnO nanowire and source/drain contacts, particularly in the device fabricated by lateral wet etching where only Al used as the source/drain contacts. These results have a good agreement with the transistors fabricated in Chapter 6 (Sample 1 and Sample 3), where these transistors only used Al as source/drain contact and exhibited low field effect mobility of 3.5 cm^2/Vs and 1.2 cm^2/Vs respectively. The steeper subthreshold slope in the transistor with AZO and Al source/drain contact also could be due to the reduction of the contact resistance.

The electrical characteristics of the ZnO nanowire FETs fabricated by the spacer method with AZO and Al source/drain contact shows a superior value especially the field effect mobility than the ZnO nanowire FETs by lateral wet etching. Other electrical characteristics are comparable with nanowire transistors with AZO and Al source/drain contacts. The fabrication of the ZnO nanowire FETs by lateral etching seem to be more suitable for achieving RF performance characterization. The nanowires structures fabricated by the lateral wet etching method allow an ease formation of ground-signal-ground pad on the nanowire transistors and has a minimal impact from ions and chemical radicals during the dry etching process. An integration of the AZO as a source/drain contacts in nanowire transistors by lateral wet etching could lower the traps and interface charges between Al and ZnO nanowires. Hence, the field effect mobility and the subthreshold slope for this device will increase significantly.

7.3 Conclusions

ZnO nanowire FETs with varying the gate lengths of transistor were successfully fabricated by new fabrication process based on direct photolithography and a lateral wet etch. The fabricated transistor with gate length ranging from 2 µm to 4 µm has shown excellent electrical characteristics except for the low field-effect mobility. The ZnO nanowire FETs exhibit on/off current ratios of 10^7, a subthreshold swing between 210 mV/decade to 300 mV/decade and threshold voltage ranging between -0.7 V to 1.5 V. The highest field-effect mobility is 0.48 cm^2/Vs. The devices show enhancement mode transistor behaviour, which is assumed to be correlated to grain boundary deep level trapped charges and interface charges as well as the imperfections introduced during the

fabrication process. Future work on the device fabrication should improve the ZnO deposition and wet etching of ZnO thin film.

7.4 References

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Chapter 8:
Conclusions and Future Outlook

8.1 Conclusions

This thesis built upon foundations laid by the very successful work of a previous graduate student. In seeking to carry the ball torch, we have tried to improve upon each piece of the ZnO nanowire FETs. We started by improving the device performance, reliability and, repeatability by optimising the fabrication process and redesigning the device. We continued to improve the device by developing new methods where necessary.

Back-gate ZnO nanowire field-effect transistors fabricated by the top-down spacer method were investigated in this study. Before the fabrication process started, an n-type depletion ZnO thin film transistor device simulation was carried out and compared to experimental results by Sultan, et al. The experiment results had a mobility of 10 cm^2/Vs at drain voltage of 1 V, subthreshold slope of 1500 mV/decade and threshold voltage of 24 V. The on/off current ratio of experiment result is 10^6 with the oxide thickness of 100 nm and nanowire dimensions of 40 nm width, 36 nm thickness and 10 μm length. Based on the simulation, it was discovered that the experimental results are degraded because of three main factors which are the interface charge, contact resistance and defects within the channel. The other defects contributing to poor experimental results were the roughness and surface charge. However, these two parameters were not simulated due to the limitation of the simulation software.

Top-down ZnO nanowire FETs were then fabricated with and without an optimization of top-down fabrication process by sidewall smoothing. The aim was to address the issues highlighted in Chapter 1. The problem of surface roughness was addressed by optimizing the top-down fabrication process of ZnO nanowire with a reduced sidewall roughness during the pattern transfer. The optimized method was shown to produce ZnO nanowire FETs with good electrical characteristics. The device is able to produce a higher output drain current by a factor of three, a lower threshold voltage and a steeper subthreshold slope of 800 mV/decade compared to devices from the non-reflow resist method. The device with a smoothed sidewall shows a strong depletion mode transistor, which starts to switch at -6 V gate voltage. The transconductance exhibits a value of 5.9 nS which is two times higher than transconductance of devices from the non-

reflow resist method. The electrical characteristics of the devices are significantly influenced by the sidewall surface roughness of ZnO nanowires.

Electrical charateristics of a bi-layer source/drain metal contact stack made of AZO and Al on ZnO nanowire FET was reported for the first time. This method is developed to further improve the performance of the top-down ZnO nanowire FETs especially the mobility of the device. The source/drain region has been covered with a highly conductive AZO layer prior to the deposition of Al contact. The measured results of the contact resistance based on the CTLM method decreased from 191.4 Ω to 9.6 Ω by 95% upon insertion of AZO thin-film thus showing better Ohmic contact in the bi-layer source/drain structure. The field-effect mobility of the ZnO nanowire FETs with Al/AZO source/drain contact increased by more than 96% from 3.5 cm^2/Vs to 85.7 cm^2/Vs in dual nanowires and the sub-threshold slope decreased from 470 mV/decade to 170 mV/decade. These results are indications that the AZO thin film is an excellent choice for source/drain contacts to fabricate high performance ZnO nanowire FETs. Since the ZnO nanowire FETs with AZO thin film source/drain contact exhibit excellent electrical characteristics at room temperature, the device was further investigated by performing temperature-dependent measurement in the range of 200 K to 300 K. The transistors show typical behaviour of the electrical characteristics with different temperatures. It shows the stability of this transistor operates at low temperature. These characteristics are also an indication of the measurement accuracy, thus consequently implies that these nanowire FETs are more reliable and stable which provides a promising platform for low temperature fabrication process and choice of better ohmic contact for various electronic applications. However, according to the temperature specifications of commercial displays, the transistors have to work in the temperature range between 243 K and 360 K [1]. For this purpose, the variation with temperature of electrical characteristics in the temperature range above 300 K is also an important piece of information need to be considered in the future works.

ZnO nanowire FETs with a ground-signal-ground contact pad were successfully fabricated. At first, the device fabrication was performed using e-beam lithography in order to pattern a small gate length of up to 20 nm. However, due to grain issues in deposited ZnO thin film, the wet etching of the nanowires could not be properly performed. In addition, the photoresist used for the e-beam lithography was not compatible with the ZnO etching process. Inspired by the unsuccessful fabrication using e-beam lithography, which indirectly simplify the top-down ZnO nanowire FETs fabrication process. The ultimate aim of this device fabrication is for RF characterization, however, due to some problems during

fabrication and equipment unavailability to perform the RF characterization, it could not be done on time. The electrical characterization of the transistor with different gate lengths varying from 2 µm to 4 µm was successfully completed. The transistor exhibits excellent threshold voltage between -1 V to 2 V, a steep subthreshold slope ranging from 210 mV/decade to 300 mV/decade, and high on/off current ratio up to 10^7. Despite these excellent numbers, the field-effect mobility for this transistor is quite low. It is assumed that contact resistance contributes to these low field-effect mobility values. The highest field-effect mobility for this transistor was 0.48 cm^2/Vs. These fascinating advancements of ZnO fabrication using direct photolithography and lateral etch encourages more research efforts to address technical challenges and to tackle the technical challenges of using the ZnO nanowire FET for RF applications.

In summary, the nanowire transistors fabricated in this work have achieved a number of advancements and a comparable result in the field of ZnO nanowire FETs research as compared to the previous literature, discussed in Chapter 2. The fabricated nanowire transistors have a steep subthreshold slope of 170 mV/decade which is among the steepest subthreshold slope as compare to other ZnO nanowire FETs fabricated by previous researchers. In this work, a comparable field effect mobility achieved with the best value of 85.7 cm^2/Vs and the on/off current ratio of 10^7.

8.2 Future Outlook

Significant progress has been made in both understanding ZnO nanowire FETs fabrication and their characterization. The top-down ZnO nanowire FETs in this work provide a good starting point and foundation for future study of ZnO nanowire FET for logic circuits and RF applications. Further investigation is needed to explore the true potential of ZnO nanowire FETs to be applied in logic circuit and RF applications.

Transmission electron microscopy (TEM) analysis and X-ray diffraction (XRD) are two major techniques which may be used for structure characterization. TEM observation can provide direct imaging of nanocrystalline structures, from which the grain size distribution and shape can be obtained [1]. The grain size of the ZnO nanowire/thin film should be properly analysed in order to fully understand the ZnO nanowire FETs' properties. The TEM study will determine the grain size of the ZnO nanowire and the defect in the ZnO. The improvement of the ZnO thin film deposition could be made if needed when the grain size information is known. Kim et al. [2] have performed the XRD

and TEM analysis on their ZnO film grown by RF magnetron sputtering, to understand the grain size effect on the photoluminescence.

Fast switching is an important requirement of the FETs regarding its implementation in practical applications. The desirable electrical characteristic of ZnO nanowire FETs have been proven, yet the high speed potential has not yet been demonstrated. In the next stage from the work presented here, it would beneficial to perform RF characterization in order to foresee the potential of the ZnO nanowire FETs in RF applications. A transistor suitable for RF applications should display a high f_T and a high f_{max}. These features will allows circuit operation at high frequencies and support low noise performance. The main key issue is field-effect mobility in the ZnO transistor. Reaching a low field-effect mobility in early work, optimizing the source/drain contact using AZO thin film and ZnO thin film deposition could be one of the solution to enhance the field-effect mobility.

There is room for improvements of ZnO nanowire FET fabrication based on direct photolithography and lateral wet etch (as discussed in Chapter 4). The electrical performance of the device, especially the field-effect mobility, can be improved by inserting AZO thin film as a bi-layer source/drain contact electrodes. The insertion of AZO film has been proven to enhance the electrical performance of the ZnO FETs' fabrication based on the spacer method (as discussed in Chapter 6). It is believed that AZO thin film can improve the Ohmic contact between the source/drain contact [3] and ZnO nanowire channel.

In addition, the dimension of the gate length also should be reduced. Gate length scaling improves transistor performance by reducing the intrinsic gate capacitance and increasing the transconductance as well as control of the reduction of parasitic capacitances and resistances [4]. The improvement should consider the dimension of gate length up to 10 nm with a ZnO nanowire length of 50 nm to 5000 nm using e-beam lithography.

8.3 References

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