UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND THE ENVIRONMENT

Engineering Materials Research Group

PhD thesis

Electrical and material characterisation of Silicon Carbide based resistive memories

by

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Thesis for the degree of Doctor of Philosophy

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ABSTRACT

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ELECTRICAL AND MATERIAL CHARACTERISATION OF SILICON CARBIDE BASED RESISTIVE MEMORIES

Junqing Fan

Resistive memory is widely considered as a promising non-volatile memory to address the demands for high-density data storage, low power consumption, augment the performance of current transistor-based memories or even replace current transistor-based memories. Main advantages of resistive memory include simple Metal/Insulator/Metal device structure, low switching voltage, fast switching speed, and long data retention. Material properties of the insulating layer play important roles in the overall performance of resistive memory. Among a range of insulator materials of resistive memories that have been reported in the literature thus far, Silicon Carbide (SiC) has shown great promise as the insulating layer which leads to resistive memories with desirable performance including large ON/OFF ratios, excellent data retention, and CMOS compatibility in device fabrication. However, there are still many challenges to be solved in the resistive memories using SiC, especially amorphous (a)-SiC as the insulating layer to be superior to other resistive memories. One of these challenges is to reduce the forming voltage which could affect the power consumption and complexity of the peripheral power-supply circuit. Another challenge is to achieving device structure exclusively using native CMOS back-end-of-line materials which would enable low fabrication cost and low development time to embed a-SiC based resistive memories in the CMOS back-end-of-line layer. Moreover, the existing Electrochemical metallisation (ECM) mechanism cannot precisely predict the switching voltage nor resistance state of resistive memories, and there is a lack of knowledge on how the material properties of the insulating layer affect resistive-switching performance and mechanisms. Further exploration of the resistive-switching characteristics to improve the understanding of switching mechanism and influence of material and electrical properties of the insulating layer on resistive-switching characteristics are needed from a scientific point of view.

This thesis focuses on addressing all the challenges above, highlights the influence of insulator material choice on the performance of resistive memories using SiC as the insulating layer. Amorphous silicon carbide (a-SiC), Cu embedded a-SiC (a-SiC:Cu), CMOS back-end-of-line dielectrics (a-Si(O)C:H), and crystalline SiC (c-SiC) are used as the insulating layer of resistive memories in this thesis. The material and electrical properties of these insulator materials are characterised. Metal/Insulator/Metal resistive memories using these insulator materials as the insulating layer are fabricated and the resistive-switching characteristics of these resistive memories are studied. Ultra-high ON/OFF ratios up to 10^9 which enables fast and reliable detection of the states, are achieved. Forming voltage and SET voltage are reduced and endurance is improved by embedding Cu nanoparticles in the a-SiC insulating layer. Non-volatile resistive-switching is observed on resistive memories using exclusively native CMOS back-end-of-line materials including Cu, W, a-SiC:H, a-SiOC:H, and a-SiCO:H. The influence of material and electrical properties of the insulating layer on resistive-switching characteristics of resistive memories made exclusively using CMOS back-end-of-line materials is discussed.

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Declaration of authorship

I, **Junqing Fan** declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

Electrical and material characterisation of Silicon Carbide based resistive memories

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
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3. Where I have consulted the published work of others, this is always clearly attributed;
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   J. Fan, L. Jiang, S. Wang, R. Huang, K.A. Morgan, L. Zhong, and C.H. de Groot, Amorphous SiC resistive memory with embedded Cu nanoparticles, Microelectronic Engineering, 174 (2017), pp.1-5.

   J. Fan, L. Jiang, L. Zhong, R.P. Gowers, K.A. Morgan, and C.H. de Groot., Microstructure and electrical properties of co-sputtered Cu embedded amorphous SiC, Materials Letters, 178 (2016), pp.60-63.

   K.A. Morgan, J. Fan, R. Huang, L. Zhong, R.P. Gowers, J.Y. Ou, L. Jiang, and C.H. de Groot, Active counter electrode in a-SiC electrochemical metallization memory, Journal of Physics D: Applied Physics, (2017)

   K.A. Morgan, J. Fan, R. Huang, L. Zhong, R.P. Gowers, L. Jiang, and C.H. de Groot, Switching kinetics of SiC resistive memory for harsh environments, AIP Advances 5, (2015) 077121.

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Chapter 1: Introduction

1.1 Motivations

Non-volatile memory such as NAND Flash memory can maintain stored data when power is off and is widely applied in persistent data storage. The demands on persistent data storage with high capacity, high speed, low power consumption, and low cost, are increasing in the portable electronics market and high-performance computer market [1]. For example, the maximum capacity of NAND Flash memory for persistent data storage in high-end smartphones has increased from 16 GB in 2007, to 256 GB in 2017. Another example is that more and more personal computers and servers are using the solid-state hard drive (SSD) which is usually made by NAND Flash memory because SSD has higher write/read speed, e.g. approximately 500 MB/s, than that of the traditional hard disk drive. The increasing of persistent data storage capacity is expected to continue in the next few years due to the successful development and commercialising of 3D NAND Flash memory [2]. While, there are challenges that the 3D NAND Flash memories need to overcome, include slow fabrication process, low poly-Si channel mobility [2], high programming voltage, and low body erase speed [3]. Hence there is a large chance for alternative non-volatile memories to catch up with 3D NAND Flash memory. Moreover, persistent data storage using NAND Flash memory has different data management interfaces with main memory [4, 5]. This multi-interface configuration is inefficient as significant among of work and energy are wasted in data transmission between data management interfaces [5]. The solution is to build persistent data storage use the same data management interface as the main memory. One major challenge to achieve this by current NAND Flash memory is that NAND Flash memory is not byte-addressable (operate individual memory cells) [4, 5]. Hence, alternative non-volatile memory with byte-addressable feature needs to be developed.

In the meantime, further down-scaling of volatile memory such as Static random access memory (SRAM) and dynamic random access memory (DRAM) is facing challenges to restrict the leakage current [4, 6]. More energy would be consumed by SRAM and DRAM to maintain the data stored when the leakage current increased. Hence, it is challenging to maintain the power consumption of volatile memories as their density is approaching an unprecedented high level. For example, the energy consumed to maintain the data stored, among the total energy consumption is expected to increase from 15% for a 4 GB DRAM to 47% for a 64 GB DRAM [4]. One potential solution is to use non-volatile memory along with volatile memory to complement power consumption performance because non-volatile memory consumes much lower power to maintain the data stored [4]. This can be achieved by integrate non-volatile memories with volatile memories on the same chip or

eventually embed non-volatile memories on top of Complementary Metal Oxide Semiconductor (CMOS) circuit which could save the valuable cell area and reduce interconnect latency [1, 7]. However, these goals are very challenging to achieve by Flash memory due to the limitations including complex fabrication processes, high switching voltage, and slow switching speed [1]. As a result, alternative non-volatile memory free from these limitations needs to be developed.

1.2 Aims and Objectives

Electrochemical metallisation (ECM) resistive memory is a type of advanced non-volatile memory, which has presented desirable performance including low switching voltage, high programming speed, promising down-scalability to nanometer scale, and potential for high-density data storage that difficult to achieve by alternative non-volatile memories [1, 8]. If not specified, all resistive memory in this thesis refers to ECM resistive memory. Prior to this PhD project, a few studies in the literature have reported that resistive memory using amorphous SiC (a-SiC) as the middle device layer, i.e. the insulating layer, can lead to promising performance including ultra-high ON/OFF ratios [9] and excellent retention [10, 11]. There are still many challenges to be solved in these resistive memories using a-SiC as the insulating layer to be superior to other resistive memories. One of these challenges is to reduce the forming voltage which could affect the power consumption and complexity of peripheral power-supply circuit [12]. Another challenge is to achieving device structure exclusively using native CMOS back-end-of-line materials which would enable low fabrication cost and low development time to embed a-SiC based resistive memories in the CMOS back-end-of-line layer [7]. Both the two challenges mentioned can be overcome based on the up to date knowledge of resistive-switching theory and existing technologies. Moreover, the existing ECM mechanism cannot precisely predict the switching voltage and resistance state of resistive memories, and there is a lack of knowledge on how the material properties of the insulating layer affect resistive-switching performance and mechanisms. It is the focus of this thesis to address these challenges.

1.3 Organisation of report

The thesis is organised as follows. Chapter 2 provides a literature review of the relevant topics. Firstly, a review of the most advanced non-volatile memories in the market and their challenges is provided. Next, a review of resistive memory device structure, the resistive-switching characteristics, and common resistive-switching mechanisms including ECM and others, is provided. Then, an in-depth review of the electrochemical metallisation (ECM) switching mechanisms and the conduction mechanism of ECM resistive memories are given. Afterward, the

influence of material properties of the insulating layer on the resistive-switching performance is reviewed. At the end of this chapter, insulator materials which are used as the insulating layer of resistive memories in this thesis are reviewed. These insulator materials including amorphous silicon carbide (a-SiC), Cu embedded a-SiC, CMOS back-end-of-line dielectrics, and crystalline SiC.

Chapter 3 reports design and fabrication methods of resistive memories in this thesis, methods to measure material and electrical properties of insulator materials, and methods to measure the resistive-switching characteristics of resistive memories in this thesis.

Chapter 4 reports the influence of sputter target power and Argon gas flow of the sputtering process on the material and electrical properties of amorphous SiC (a-SiC) films. Also, resistive-switching characteristics of Cu/a-SiC/Au and Cu/a-SiC/W resistive memories were presented, which exhibit high ON/OFF ratios.

Chapter 5 reports material and electrical properties of co-sputtered Cu nanoparticles embedded amorphous SiC (a-SiC:Cu) films, and resistive-switching characteristics of Cu/a-SiC:Cu/Au resistive memories, which exhibit reduced forming and SET voltages, improved endurance, and high ON/OFF ratios.

Chapter 6 reports the material and electrical properties of CMOS back-end-of-line dielectrics (a-Si(O)C:H). Also, resistive-switching characteristics of W/a-Si(O)C:H/Cu resistive memories were presented, which exhibit high ON/OFF ratios. Moreover, the influence of material and electrical properties of the a-Si(O)C:H insulating layer on resistive-switching characteristics is discussed.

Chapter 7 reports the material and electrical properties of Vapor phase epitaxy (VPE) crystalline SiC (c-SiC), and current conduction and resistive-switching characteristics of Cu/c-SiC/Si devices.

Chapter 2: Operation of resistive memory (RM)

This chapter presents a comprehensive review relevant to the development of resistive memories using SiC as the insulating layer. Section 2.1 reviews the current non-volatile memories on the market and their challenges. Highlights the demands on non-volatile memories with high density, high speed, low power consumption, and low cost, and pointed out the development of electrochemical metallisation (ECM) resistive memory could potentially solve these demands. All the resistive memories studied in this thesis are classified as ECM resistive memory. Section 2.2 reviews the fundamentals of ECM resistive memory and other resistive memories. Highlights the Metal/Insulator/Metal of resistive memories, the resistive-switching characteristics, and basic concepts of ECM and other switching mechanisms. Section 2.3 provides an in-depth review of the physics of ECM resistive memory. The three main switching processes Electroforming/SET and RESET and the current conduction mechanisms in the low and high resistance state were reviewed. Section 2.4 reviews the influence of material properties of the insulating layer to the resistive-switching characteristics. The effect of embedding metal particles in the insulating layer and thickness of the insulating layer on resistive-switching characteristics were reviewed. Also, the design of resistive memory using CMOS back-end-of-line (BEOL) dielectrics as the insulating layer was reviewed. Finally, section 2.5 reviews material properties and device application materials including crystalline SiC, amorphous SiC, and BEOL dielectrics, which are studied as the insulating layer of the resistive memories in this thesis. Also, resistive memories that have amorphous SiC insulating layer appeared before this thesis started was reviewed.

2.1 Current non-volatile memories and their challenges

2.1.1 Flash memory

Flash memory is currently the most successful non-volatile memory and is widely applied in portable and high-speed persistent data storage. There are two main types of Flash memories, which are NAND and NOR Flash memories. Both NAND and NOR Flash memories all have floating-gate metal-oxide-semiconductor (MOS) transistor as the memory cell. In NAND Flash memories, multiple floating-gate MOS transistors are serial connected. The NAND Flash memories have a higher program/erase speed, e.g. 200 μs/500 μs, than that of the NOR Flash memories, hence are widely used in data storage applications [13]. In NOR Flash memories, multiple floating-gate MOS transistors are parallel connected. The NOR Flash memories have higher random access speed of individual memory cell, e.g. 0.075 μs, hence are widely used as code storage in embedded applications. Different from conventional MOS transistor, floating-gate MOS transistor has a

floating gate below the control gate to storage charges, as shown in Figure 2-1. The threshold voltage of a floating-gate MOS transistor can be manipulated by charging and discharging the floating gate. Data could be stored non-volatile in a floating-gate transistor in terms of the different threshold voltage. The writing process of NAND and NOR Flash memories usually uses Fowler-Nordheim (FN) tunnelling and hot carrier injection, respectively, to charge the floating gate [14]. Figure 2-1a shows the writing process of a floating-gate MOS transistor using FN tunnelling, where a large voltage, e.g. 20 V, is applied on the control gate, and 0 V is applied on the source, drain, and p-type Si (p-Si) channel. The high voltage potential on the control causes electrons in the p-Si channel to tunnel through the tunnel oxide to the floating gate. Electrons tunnelled to the floating gate will be trapped there, and will not go further to the control gate due to the existing of the blocking layer, as shown in Figure 2-1a. The erase process of NAND and NOR Flash memories is usually using FN tunnelling to discharge the floating gate. Figure 2-1b shows the erase process of a floating-gate MOS transistor using FN tunnelling where a large voltage, e.g. 20 V, is applied to the source, drain, and p-Si channel, and 0 V is applied to the control gate. The high voltage potential on the p-Si channel causing electrons trapped in the floating gate to tunnel through the tunnel oxide to the p-Si channel.

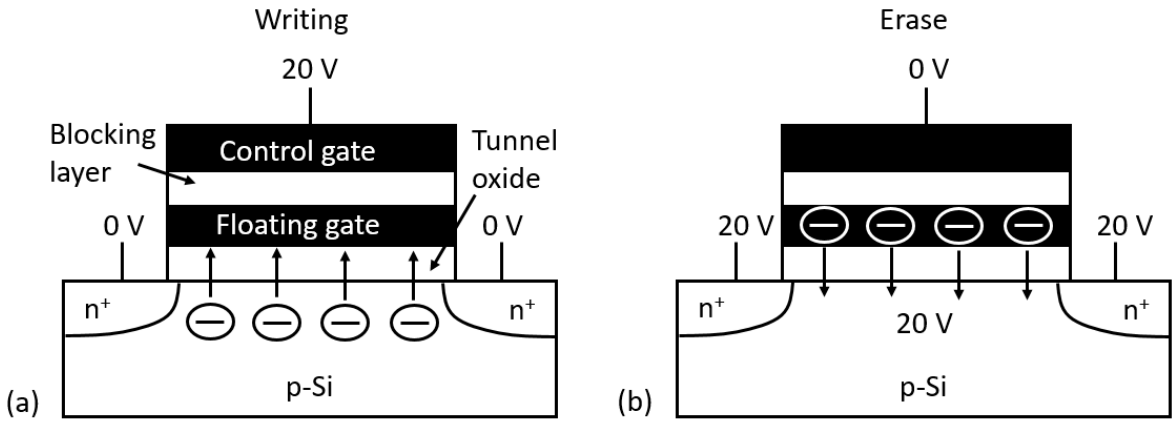


Figure 2-1. Floating-gate MOS transistor. (a) Writing process. (b) Erase process.

Same as other memory and logic devices composed of transistors, Flash memory has achieved increasing bit density and reducing bit cost by aggressive scaling of the device dimension in the X and Y dimension (2D). Although the demands on keeping a trend of increasing bit density and reducing bit cost are still strong [15], further development of Flash memories is facing tremendous challenges beyond 32 nm node in the traditional 2D way [16]. Cross-talk between neighbouring floating gates increase with the down-scaling of the gate length [17], which significantly depredate device reliability. Moreover, lithography cost increase with the down-scaling of gate length and has become intolerable at 1x nm node [2]. The ultimate solution to further development of Flash memory became building stacked Flash memory vertically to increase the density of Flash memory.

Figure 2-2a shows the equivalent circuit of a 3D NAND memory cell array. There are eight columns of vertically arranged memory cells in the equivalent circuit. In each column, there are six floating gate transistors serial connected. The transistors on the top of each column are the string select transistors. The control gate and drain of the string-select transistors connect the String select line (SSL) and the Bit line (BL), respectively. The transistors at the bottom of each column are the ground-select transistors. The control gate and source of the ground select transistors connect the Ground select line (GSL) and the Common source line (CSL), respectively. The transistors in the middle of each column are the NAND memory cells and their control gate connects the Word line (WL). Figure 2-2b shows the cross-section schematic of four columns of 3D NAND memory cells in the XZ-plane view. The small rectangles in dark green represent the control gates of the transistors, and the long rectangles in light green represent poly-Si channels of the vertically arranged transistors. Top and bottom of the Poly-Si channels connect to the BL and the p-Si substrate which is connected to the n^+ source, respectively. The Poly-Si channel of two adjacent columns of transistors is separated by a hole, as shown in Figure 2-2b. Figure 2-2c shows the zoom-in schematic of a single memory cell in the 3D NAND memory cell array. The Poly-Si channel is on the left, the tunnel oxide is on the right of the Poly-Si channel, the Trap SiN is on the right of the tunnel oxide, the blocking layer is on the right of the trap SiN, and the W gate is on the right of the blocking layer. The top and bottom of the tunnel oxide/SiN/blocking layer/W gate structure are insulated with silicon dioxide or other interlayer dielectrics [3]. Very high storage density has been achieved with much lower bit cost using this vertical structure [15]. In 2014 and 2016, Samsung introduced the 24 layer [18] and 48 layers [19] commercial 3D Flash memories, respectively and gained great success.

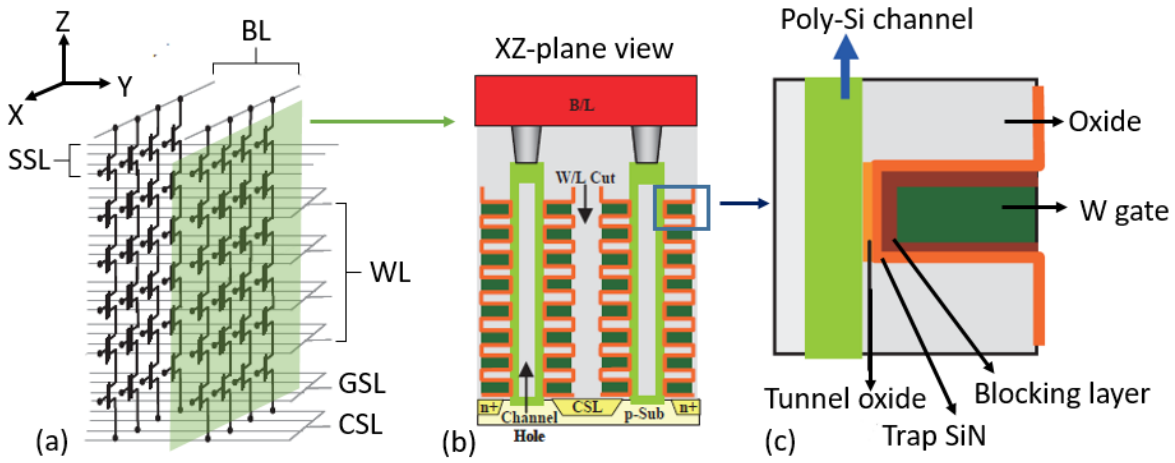


Figure 2-2. (a) An equivalent circuit of 3D NAND memory cell array. (b) Cross-section schematic of 3D NAND memory cell array in the XZ-plane view. (c) Schematic of a 3D NAND memory cell. [20]

However, there are also many emerging non-volatile memories such as electrochemical metallisation (ECM) resistive memory, have advanced features compare to 3D NAND Flash memory

and other Flash memories. For example, ECM resistive memory has simpler device structure, lower switching voltage, and higher switching speed compare with Flash memory [7]. In the meantime, many of these emerging non-volatile memories show comparable performance to 3D NAND Flash memory and other Flash memories in features dominated by Flash memory, including non-volatile data storage and high density. Moreover, 3D NAND Flash memory needs to overcome challenges including slow stack deposition, slow high-stack etching, low poly-Si channel mobility [2], to achieve higher performance and higher density. All these facts leave great development space and high chance to catch up with 3D NAND Flash memory for the emerging non-volatile memories like the ECM resistive memory.

2.1.2 Spin transfer torque magnetic RAM

Spin transfer torque (STT) magnetic RAM (MRAM) is one advanced type of MRAM. It stores data by the magnetisation of a nanoscale magnet. Different from hard disk drive which uses the same method to store data, the selection of storage address is done electronically without the need of a mechanical part [21]. The advantage of traditional MRAM is that the write/erase speed of 1 ns is fast and the data storage is non-volatile [21]. The major problem of traditional MRAM is that it needs a magnetic field in the write/erase processes while it is difficult to reduce the dispersion of magnetic field in small MRAM device. The dispersion of magnetic field causes an unwanted half program to the non-selected devices adjacent the device being programmed. Hence the down-scaling of MRAM is very challenging. STT-MRAM uses a polarised current to change the magnetic polarity. As a result, no magnetic field is required in the write/erase processes of STT-MRAM hence the down-scaling problem is solved [22]. The employing of polarised current in STT-MRAM also lowered the power consumption in the write/erase process because the polarised current has higher efficiency in changing the magnetic polarisation. The polarised current in STT-MRAM is generated by driving the non-polarised current through a thick magnetic layer [22]. The first MRAM memory commercial product was introduced in 2006 by Freescale, now Everspin [23]. However, the large-scale commercialisation of STT-MRAM did not happen due to the rapid down-scaling of its opponents, i.e. SRAM, DRAM, and NAND Flash memory, in the past decade [23]. With the pace of down-scaling of SRAM and DRAM slowing down, there is a change for the large-scale commercialisation of STT-MRAM to happen in the next five years [23]. In 2017, Everspin launched a commercial 256 Mbit DDR3 STT-MRAM chip based on 40 nm process. Besides, a 1 Gbit DDR4 STT-MRAM chip using GlobalFoundries 28 nm process is coming soon [24]. On the other side, the possibility for STT-MRAM to be applied in persistent data storage as a replacement to the 3D Flash memory is not high. This is because the fabrication maturity of 3D Flash memory is way advance than STT-MRAM. Moreover, other emerging non-volatile memories such as ECM resistive memory

has smaller and simpler device structure than STT-MRAM hence are easier to achieve high density and low cost than STT-MRAM. However, higher computing performance could be obtained by using STT-MRAM and ECM resistive memory together to combine the high speed and low power consumption feature of STT-MRAM with the high density and low-cost feature of ECM resistive memory.

2.1.3 Phase change memory

Phase change memory (PCM) stores data by switched the phase change material in the middle of the device into a crystalline and amorphous state to change its resistance. Although PCM also uses the change of resistance to store data, the structure of PCM is very different from resistive memories. A PCM usually has a top electrode, a phase change layer, a heater, and a bottom electrode, as shown in Figure 2-3a [25]. The SET process of a PCM is achieved by heating the phase change layer to a temperature slightly higher than the crystallisation temperature T_{crys} of the phase change layer and last for a relatively long period to change the phase change layer into a crystalline state, as shown in Figure 2-3b [25]. The RESET process of a PCM is achieved by heating the phase change layer to a temperature higher than the melting temperature T_{melt} of the phase change layer and last for a relatively short period to change the phase change layer into an amorphous state, as shown in Figure 2-3b [25]. The major advantages of PCM are the phase change mechanism is well understood and the technology is mature. Similar technology has been applied on optical disk storage for over three decades. In the meantime, PCM has fast programming speed close to DRAM [26], and high endurance [26, 27]. The downside of it is the relatively high energy cost per bit, which is about 10 to 40 times higher than DRAM [26, 28]. The Intel Optane™ memory using the so-called 3D XPoint technology is available on the market since 2017. Although Intel and its co-operator Micron did not reveal what type of memory the 3D XPoint technology is, it is very likely the 3D XPoint technology is PCM. The Optane™ memory is working as an accelerator between the main memory, i.e. DRAM, and the hard disk drive (HDD). Intel claims that using the Optane™ memory along with a hard disk drive can deliver an overall performance close to a solid-state drive made by Flash memory but at a much lower price. Moreover, the solid state drive (SSD) version of Optane™ memory using 3D Xpoint technology is also available on the market. The capacity of Optane™ solid state drive (SSD) is from 280 GB to 480 GB and has more or less 1.5 to 5 times faster write speed than SSD made of Flash memory depending on the tasks. While the price is nearly twice as the SSD made of Flash memory with similar capacity.

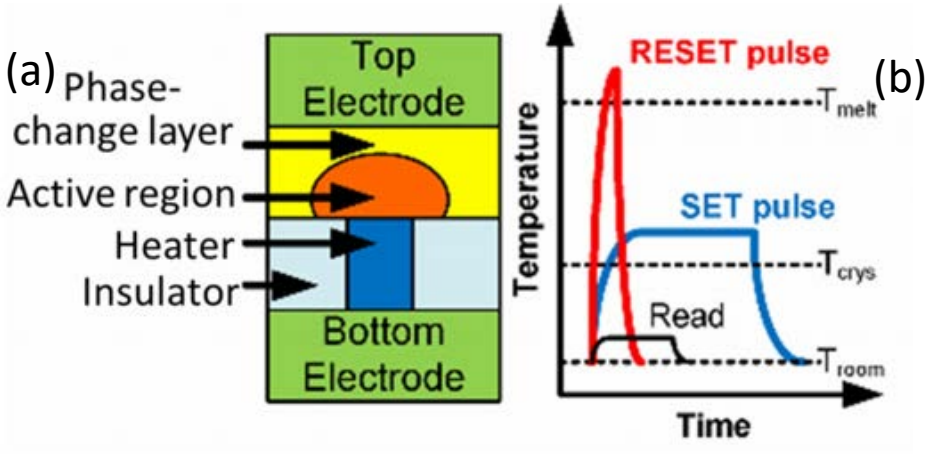


Figure 2-3. (a) Schematic cross-section of a PCM. (b) Temperature-time characteristics of the SET, RESET, and READ processes of a PCM. [25].

2.1.4 Commercialised and prototype RMs

Resistive memory has been considered as a promising candidate in a wide variety of applications including persistent data storage as a replacement for Flash memory, accelerator between DRAM and Flash memory, and low-power embedded memory. Commercial products of resistive memory are still limited. In 2012, Panasonic introduced a microcontroller with 64 KB resistive memory embedded [29]. In 2016, Panasonic with Fujitsu Semiconductor Limited launched a stand-alone resistive memory product MB85AS4MT with 4 Mbit capacity. Although the capacity of commercial resistive memories is quite limited, the situation may be changed by the fast development of electrochemical metallisation (ECM) resistive memory. ECM resistive memory is an advanced type of resistive memory. Many chip level ECM resistive memory prototypes have been demonstrated, which provide bright hopes for the mass production of ECM resistive memory products. In 2010, Adesto Technologies demonstrated the integration of 1 Mbit ECM resistive memories in 130 nm CMOS Cu back-end-of-line [30]. In 2014, Sony and Micron demonstrated 16 Gbit ECM resistive memories using CuTe as the active electrode [31]. In 2017, Sony announced 3D stackable ECM resistive memories cell which could be used to realise 100 Gbit persistent data storage [32]. Also, the resistive memories studied in this thesis are all classified as ECM resistive memory. In the following sections, fundamentals of ECM resistive memories and other resistive memories are reviewed. The ECM switching mechanisms and current-conduction mechanisms of ECM resistive memories are reviewed afterwards.

2.2 Fundamentals of electrochemical metallisation (ECM) and other RMs

2.2.1 Structure of RMs

Resistive memories usually have a Metal/Insulator/Metal (MIM) device structure [33, 34], as shown in Figure 2-4. The MIM device structure connects external circuit through the two "metal" layers. This configuration makes a resistive memory a two terminal device. Data storage in resistive memories is achieved by applying a switching voltage to change the resistance of the MIM device structure. Both the "Metal" and "insulator" materials in the MIM device structure play important roles in achieving the resistive-switching function. So far, resistive memories composited by a wide range of "metal" and "insulator" materials have been demonstrated.

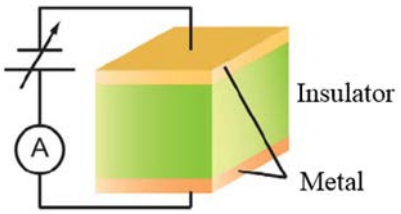


Figure 2-4. Metal/insulator/Metal (MIM) device structure of a resistive memory [33].

A wide variety of materials include oxides (e.g. Al_2O_3 [35], SiO_2 [36], HfO_2 [37], TiO_2 [38], ZnO [39]), and semiconductors (e.g. a-Si [40], a-SiC [10, 11]), have been demonstrated as the middle device layer, i.e. the insulating layer in resistive memories. But, it is not guaranteed any insulator or semiconductor can provide resistive switching function when used as the insulating layer in a MIM device structure. It is believed that the combination of "metal" and "insulator" materials used in the MIM device structure, has a profound influence on the resistive-switching behaviour.

The "Metal" layers, i.e. electrodes in most resistive memories are metals including Pt [11], Au [10], Ag [41], Cu [11], W [42]. Other conductor materials, such as TiN [35], TaN [43], heavily doped Si (Si^+) [40], ITO [44], have also been used as the electrode in many resistive memories. Resistive memories could be divided into two groups depending on the combination of electrode materials used in the MIM device structure. One group of resistive memories employ inert conductor materials such as Pt, TiN, TaN, W, in both electrodes. The other group of resistive memories employ one active conductor material such as Cu, CuTeGe [45], Ag, in one of the electrodes and use an inert conductor material for the other electrode. MIM device structure with and without an electrode using active conductor material usually leads to resistive switching behaviours with completely different mechanisms. Different resistive switching mechanisms are reviewed in the following section.

Before that, the common operation behaviour of resistive memories will be introduced in the following.

2.2.2 Resistive-switching characteristics of RMs

Resistive memory stores data by changing its resistance using a switching voltage. A high resistance represents data “0”, and a low resistance represents data “1”. Most resistive memories have two resistance states, the high resistance state (HRS) and the low resistance state (LRS). The switching process between resistance states triggered by applying switching voltage is known as the resistive-switching process. When a resistive memory is not subject to a switching voltage, its resistance state remains over time, i.e. non-volatile. The length of time when resistance state shows no significant degradation after switching is known as the retention. A resistive memory can be switched between HRS and LRS repeatedly over multiple cycles from few tens of cycles up to billions of cycles. Also, the difference between HRS and LRS during the repeated resistive-switching has to be highly distinguishable. The number of cycles the resistive-switching could repeat before the difference between HRS and LRS became indistinguishable is defined as the endurance.

Figure 2-5 shows the current-voltage (I-V) characteristics of a full switching cycle of typical resistive memory. For many resistive memories, the pristine state of the device has very high resistance and a high forming voltage V_{FORM} which is usually higher than SET voltage V_{SET} of the subsequent resistive-switching cycles as shown in Figure 2-5, to switch the device from HRS to LRS for the first time. The resistive-switching cycles in Figure 2-5 begin with step 1 and 2 where +V was applied to the resistive memory, and the current passing through the resistive memory increased abruptly to the 0.01 A current compliance when the +V increased to V_{FORM}. Current compliance is usually applied in the forming and SET processes of resistive memories, to prevent large current passing through the device which may cause permanent breakdown of the insulating layer. The resistive memory was switched from HRS to LRS, and was maintained in the LRS in step 3. Next, -V was applied to the resistive memory in step 4. The current passing through firstly increased with the increasing -V, then abruptly reduced over orders of magnitudes when –V increased to the RESET voltage V_{RESET}. The resistive memory was switched from LRS back to HRS, and was maintained in the HRS in step 5. Up to now, a full cycle of resistive-switching is completed.

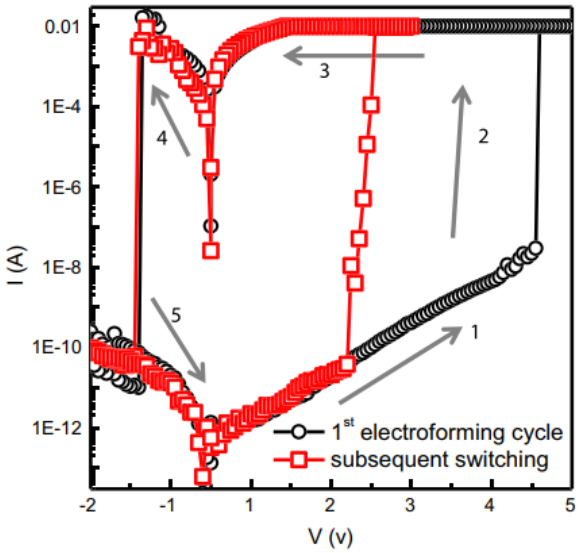


Figure 2-5. Typical resistive-switching I-V characteristics of our Cu/a-SiC/Au resistive memory [46].

Figure 2-6a shows the endurance characteristics of resistive memory. LRS current and HRS current of the resistive memory read out at 0.1 V in between repeated resistive-switching, were plotted in red and black, respectively in Figure 2-6a. Read voltage V_{READ} is usually much smaller than V_{SET} and V_{RESET} to avoid disturbing the programmed resistance states. Neither LRS current nor HRS current show significant degradation through the 100 resistive-switching cycles as shown in Figure 2-6a.

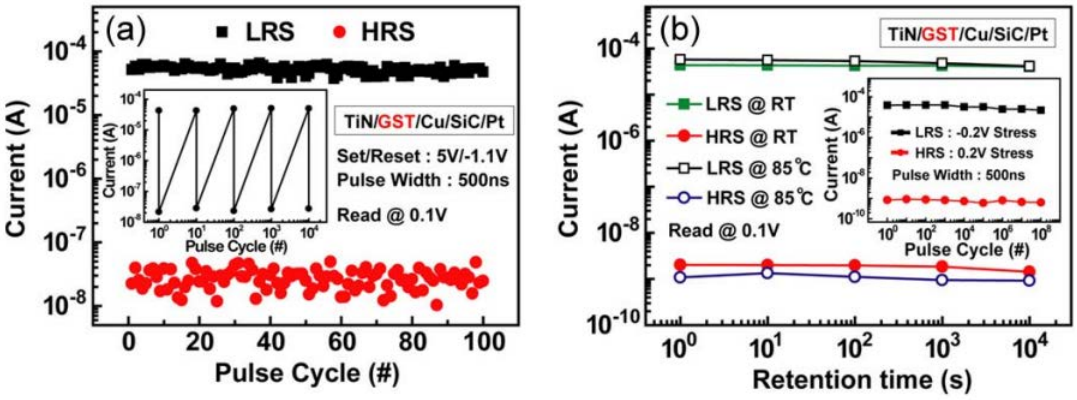


Figure 2-6. (a) Endurance of a resistive memory over repeated resistive-switching. (b) Retention characteristics of TiN/GeSbTe/Cu/SiC/Pt resistive memories. [47]

Figure 2-6b shows the retention characteristics of resistive memory. The LRS and HRS retention characteristics of resistive memory are usually measured individually from two identical resistive memories because it is a time-consuming measurement. The current of the resistive memory in LRS and the resistive memory in HRS was read out at 0.1 V over a prolonged period, as shown in Figure 2-6b. Same as in the endurance measurement, V_{READ} used for the retention measurements is usually much smaller than V_{SET} and V_{RESET} to avoid disturbing the programmed resistance states. Neither LRS current nor HRS current show significant degradation over 10^4 seconds.

There are four resistive-switching modes depending on voltage polarity combination of V_{SET} and V_{RESET}. Positive-unipolar mode is achieved by $+V_{SET}$ followed by $+V_{RESET}$, as shown in Figure 2-7a. Positive-bipolar mode is achieved by positive $+V_{SET}$ followed by $-V_{RESET}$, as shown in Figure 2-7b. Negative-bipolar mode is achieved by $-V_{SET}$ followed by $+V_{RESET}$, as shown in Figure 2-7c. Negative-unipolar mode is achieved by $-V_{SET}$ followed by $-V_{RESET}$, as shown in Figure 2-7d. Most resistive memories present either bipolar resistive-switching mode or unipolar resistive-switching mode [9]. Resistive memories that shown all the four resistive-switching modes are called nonpolar resistive memories [10].

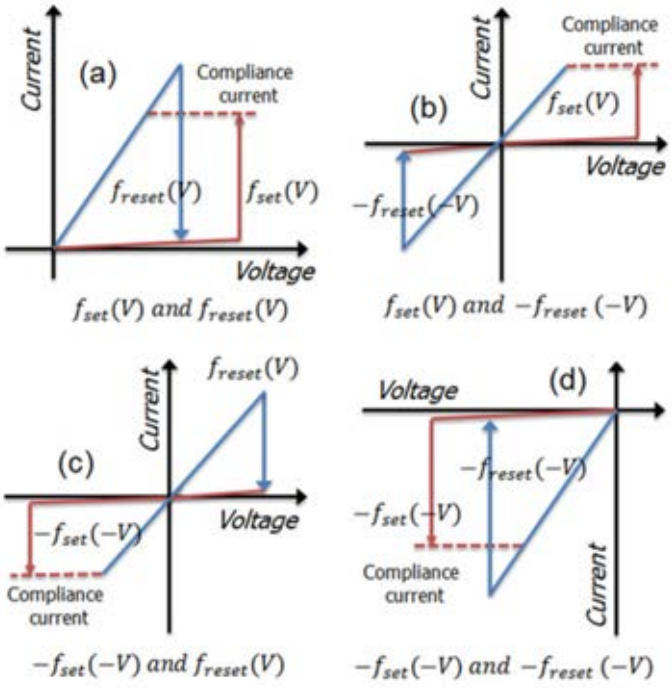


Figure 2-7. I-V characteristics of four resistive-switching modes. (a) Positive-unipolar, (b) positive-bipolar, (c) negative-bipolar, and (d) negative-unipolar. [48]

It is possible to predict the polarity of the V_{FORM}/V_{SET} and V_{RESET} in some resistive memory by applying this knowledge of resistive-switching mechanisms. However, it is difficult to precisely predict the resistance values of a resistive memory in LRS and HRS. Hence further analysis of resistive-switching mechanism is required to gain an in-depth understanding of the resistive-switching behaviour. Common resistive-switching mechanisms are reviewed in the following.

2.2.3 Resistive-switching mechanisms

Although resistive memories have the MIM device structure, the switching mechanisms can be very different. Many resistive-switching models including electrochemical metallisation (ECM), valence change memory (VCM), thermochemical memory (TCM), and interface-type resistive switching, have been developed to explain the switching mechanisms. ECM and VCM resistive memories are

most commonly studied in the literature. All the a-SiC based resistive memories in this thesis are classified as ECM resistive memory. Characteristics of ECM and VCM switching mechanisms are briefly compared in the following to help distinguish the two most common switching mechanisms. In-depth review of ECM switching mechanism is given in the following section.

The concept of ECM switching mechanism and VCM switching mechanism are very similar. Essentially, it is believed that the change of resistance by both ECM switching and VCM switching, is due to forming and dissolving a conductive filament in the insulating layer. The difference is the conductive filament in ECM switching is formed by metal materials injected from the active electrode such as Cu, Ag, while the conductive filament in VCM switching is composed of oxygen vacancies in the insulating layer. The metal conductive filament in the insulating layer of ECM resistive memories has been observed using Transmission Electron Microscope (TEM) [49] and Conductive atomic force microscope (C-AFM) [35]. Figure 2-8a shows a TEM cross-section image of an ECM resistive memory which has a Cu conductive filament in its Al_2O_3 insulating layer. A bright filament shape in the gap between two large electrodes can be clearly observed in Figure 2-8a, which is the Cu conductive filament [49]. The metal materials compose the conductive filament in ECM resistive memories such as Cu and Ag are very conductive hence large resistance change can be achieved. The oxygen vacancy filament in VCM resistive memories has been observed using TEM and Energy-Dispersive X-ray spectrometer (EDX) [50]. Figure 2-8b shows the TEM cross-section image of a VCM resistive memory and the EDX oxygen map in its Ta_2O_5 insulating layer. The region depicted by the dashed line in Figure 2-8b where has very low oxygen concentration in the Ta_2O_5 insulating layer is the oxygen vacancy conductive filament. The depletion of oxygen in the oxygen vacancy filament changes the valence state of the insulating layer hence the resistance of the MIM device structure was changed [51]. VCM resistive memories usually have an insulating layer made of metal oxides [50] such as HfO_2 [52], Ta_2O_5 [53], $SrTiO_3$ [54], TiO_2 [55], and ZnO [12]. However, metal oxides have also been used as the insulating layer of ECM resistive memories, apart from many other insulator and semiconductor materials. What makes the difference is all the ECM resistive memories have one of the electrodes made of active conductor materials such as Cu and Ag, which is the reservoir of the conductive filament, while VCM resistive memories usually have both of its electrodes made of inert conductor materials such as Pt [52], TiN [12, 52]. Table 2-1 lists some typical ECM and VCM resistive memories.

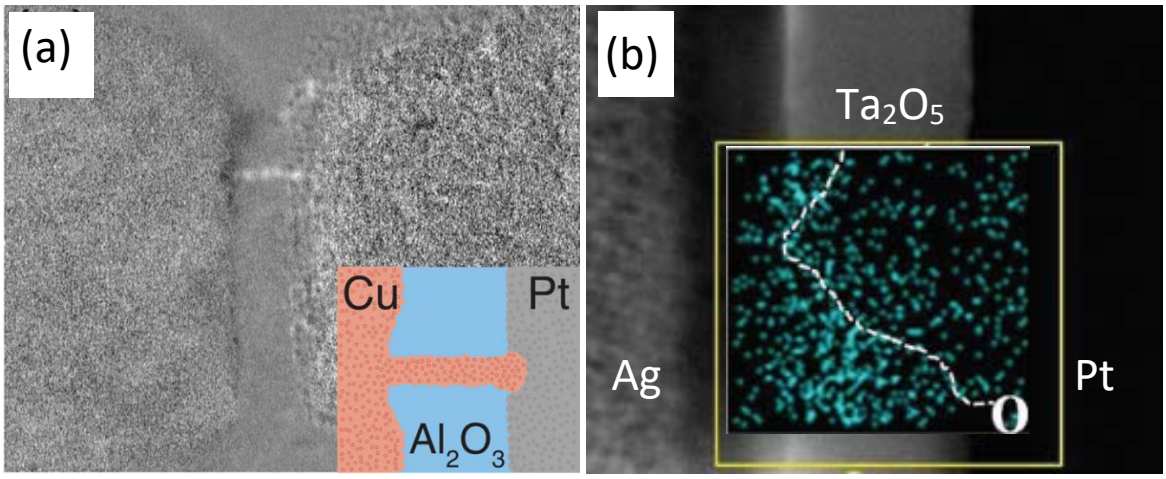


Figure 2-8. (a) TEM image of a Cu filament in the Al_2O_3 insulating layer of a Cu/Al_2O_3/Pt resistive memory in LRS [49]. (b) TEM image of an Ag/Ta_2O_5/Pt resistive memory. An EDX map of O is overlapped over the TEM image, which shows an O vacancy region with a filament shape [50].

Table 2-1. Parameters of typical ECM and VCM resistive memories.

Type	Structure	Switching mode	$\|V_{SET}\|$ (V)	$\|V_{RESET}\|$ (V)	SET time	RESET time	ON/OFF ratio	Retention	Endurance
ECM	Cu/a-SiC/Au [10]	Unipolar, bipolar	2-3	1-2	N.A.	N.A.	10^6-10^8	10 years	N.A.
ECM	Cu/a-SiC/Pt [11, 47]	Bipolar	5	1.1	500 ns	500 ns	10^3	10 years	10^4
ECM	Cu/AlO_x/W [42]	Bipolar	1.3-1.6	1.5	N.A.	N.A.	5×10^2	1000 s	>20
ECM	Cu/TaOx/Pt [56]	Unipolar, Bipolar	1.1-1.7	0.3-0.8	N.A.	N.A.	10^4-10^5	N.A.	N.A.
ECM	Cu/Ta/SiCN/ Al_2O_3/TiN [57]	Bipolar	2	2	N.A.	N.A.	10^4	>10^4 s	>1.6×10^4
VCM	Ti/TiO_2/$SrTiO_3$ [58]	Bipolar	1.1	0.15	N.A.	N.A.	10^7	N.A.	>100
VCM	Pt/Ta_2O_{5-x} /TaO_{2-x}/Pt [59]	Bipolar	4.5	6	10 ns	10 ns	10	10 years	10^{11}
VCM	Ta/Ta_2O_5:Ag/ Ru [60]	Bipolar	1.5	1.5	100 ns	100 ns	10	>5×10^4 s	5×10^7
VCM	Pt/SiO_2:Pt/Ta [61]	Bipolar	3-5	4.5-5	100 ps	100 ps	10-1000	>10^7 s	3×10^7
VCM	Pt/GdO_x/TaN_x [62]	Bipolar	2-5	3-4	30 ns	10 µs	10^6	>10^4 s	>10^4

2.3 Physics of ECM RM

2.3.1 Electroforming and SET mechanisms

The electroforming and SET mechanisms of ECM resistive memories involve the formation of metal conductive filament inside the insulating layer. The difference is the electroforming process refer to the first time the filament is formed in a pristine resistive memory while the SET process usually refers to the formation of the conductive filament in subsequent switching cycles. There are four steps in the formation of the conductive filament. Firstly, the neutral atoms M in the active electrode (anode) oxidise into cations as described by Equation 2.1,

$$M \rightarrow M^{z+} + ze^{-}, \tag{2.1}$$

where M^{z+} represents the metal cation, z is the number of electrons lost by the metal cation, and e is the charge of one electron. Secondly, the metal cations migrate from the active electrode towards the inert electrode (cathode) under the influence of the external electric field. Thirdly the metal cations reduce back to neutral atoms M either at the inert electrode or inside the insulating layer as described by Equation 2.2,

$$M^{z+} + ze^{-} \rightarrow M \tag{2.2}$$

In the last step, the Cu atoms inside the insulating layer gradually accumulate into a conductive filament connecting the two electrodes. The position where the reduction of cations happens is still in debate and is believed to depend on the properties of the insulating layer. If the metal cations only reduce to neutral metal atoms after they arrive the inert electrode or the front end of the conductive filament, then it is likely that the conductive filament is accumulating from the inert electrode back to the active electrode [63], as shown in Figure 2-9. While if the metal cations reduce to neutral metal atoms inside the insulating layer before they arrive the inert electrode, then it is likely that the conductive filament is accumulating from the active electrode towards the inert electrode [35], as shown in Figure 2-10.

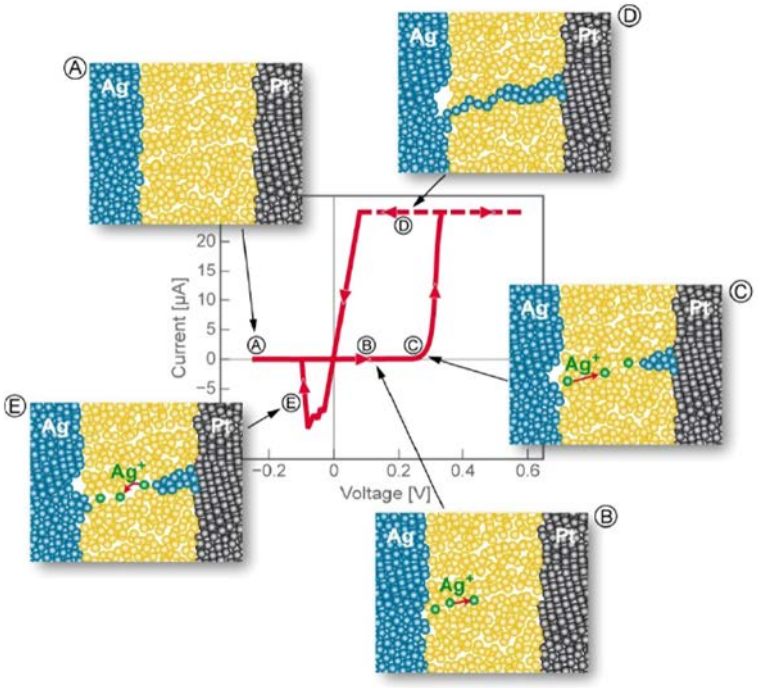


Figure 2-9. Schematic of the formation of the conductive filament where the conductive filament is accumulating from the inert electrode back to the active electrode. [63]

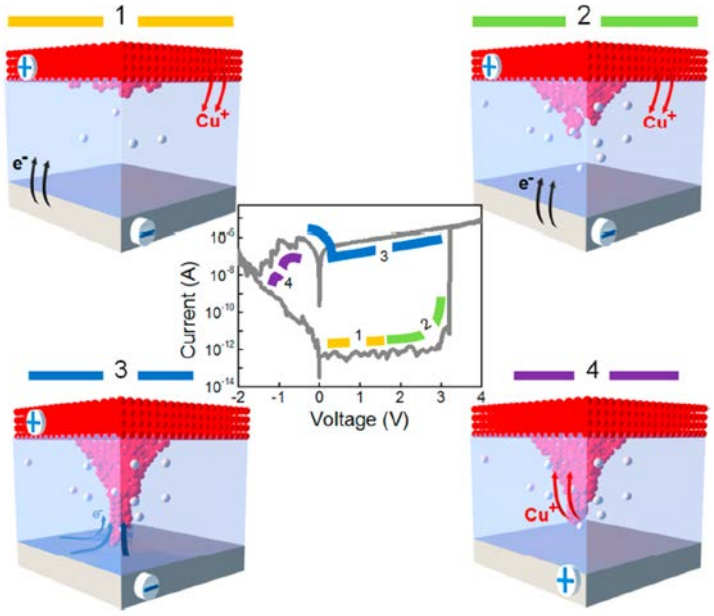


Figure 2-10. Schematic of formation of the conductive filament where the conductive filament is accumulating from the active electrode towards the inert electrode. [35]

2.3.2 LRS conductive mechanism

In ECM resistive memories, current conduction in the LRS is usually dominated by current conduction through the metal conductive filaments. Hence, most ECM resistive memories in LRS have an Ohmic I-V characteristic similar to a metal conductor, where the current is proportional to

the voltage. Ohmic I-V characteristics of an ECM resistive memory is illustrated in Figure 2-11a [10], where the slope of the straight line fits the I-V characteristics is approximately 1. Also, metal-like temperature dependence on of resistance, where the resistance increase with increasing temperature has been observed from ECM resistive memories in LRS, as shown in Figure 2-11b [10].

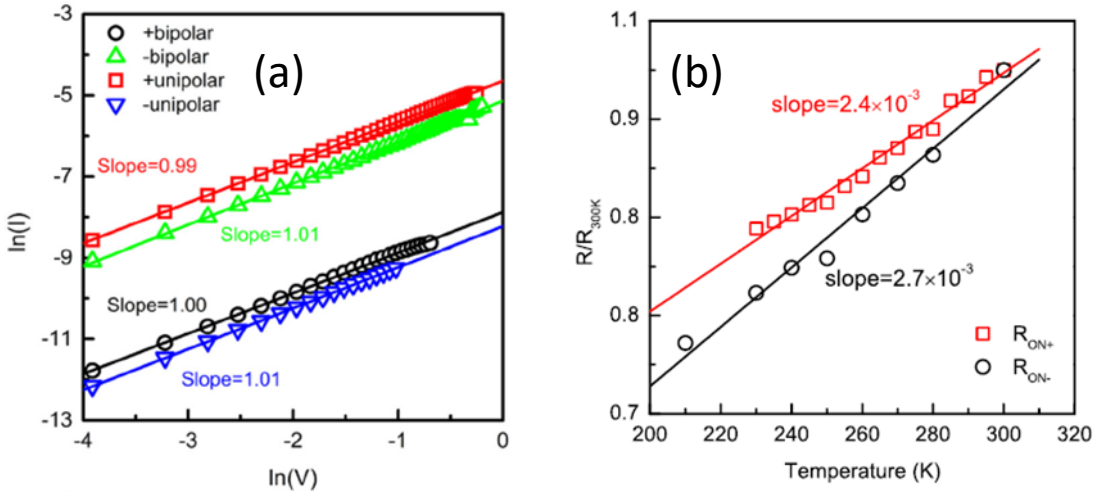


Figure 2-11. (a) LRS I-V characteristics in the double logarithmic plot, (b) temperature dependence of resistance in LRS for our a-SiC resistive memories. [10]

Figure 2-12 shows the typical relation between LRS resistance and device area of ECM resistive memories. The LRS resistance has no dependence on the device area indicating the current conduction in LRS is only occurs in a particular position in the device instead of throughout the entire area of the device. The position in the device where the current density is concentrating is likely to be where the metal conductive filament is [35].

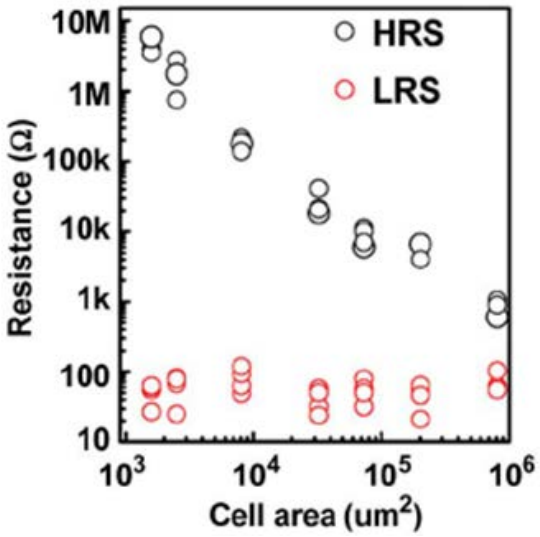


Figure 2-12. Area dependence of resistance in LRS and HRS of Al/Cu_xO/Cu ECM resistive memories. [64]

2.3.3 RESET mechanism

The RESET switching of ECM resistive memory is explained as the disruption of the conductive filament [35, 63, 65]. The disruption of the conductive filament could either be induced by the electrochemical dissolution of the conductive filament or by Joule heating dissolution. In the electrochemical dissolution of the conductive filament, a V_{RESET} that has a polarity opposite to the V_{SET} is applied on the device, and the metal atoms in the conductive filament would move back to the active electrode through a reversed electrochemical metallisation process, as shown in Figure 2-13a [10]. In Joule heating enhanced lateral diffusion of the conductive filament, high temperature near the conductive filament increases to a critical temperature due to Joule heating and dissolves the conductive filament, as shown in Figure 2-13b [10].

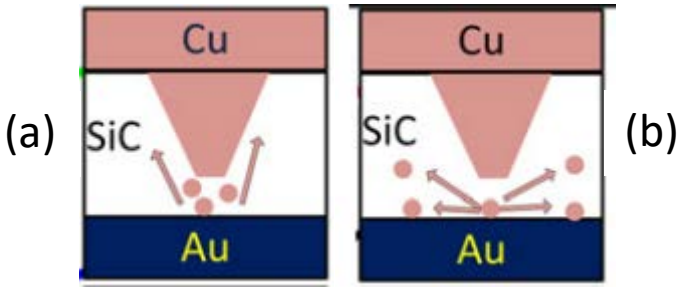


Figure 2-13. Schematic of dissolution process of the metal conductive filament of ECM resistive memory. (a) Electrochemical dissolution. (b) Joule heating enhanced lateral diffusion. [10]

2.3.4 HRS conductive mechanism

Current conduction mechanisms including reverse bias Schottky emission [10] and Poole-Frenkel (PF) emission [11] are most commonly found in the literature to describe the current conduction characteristics of ECM resistive memories in HRS. In reverse bias Schottky emission, the electron (e.g. n-type Schottky contact) with higher thermal energy would be emitted from the metal side into the semiconductor side, over the Schottky barrier with a Schottky barrier height (Φ_B), as shown in Figure 2-14a [66]. The Schottky barrier height in the reverse bias Schottky emission reduces with increasing electric field due to an image-force lowering effect. The I-V characteristics of the reverse bias Schottky emission are described by Equation 2.3 [66],

$$I = AJ = AA^*T^2\exp\left(\frac{-q\Phi_B}{kT} + \frac{q}{kT}\sqrt{\frac{qE}{4\pi\varepsilon}}\right), \quad (2.3)$$

where A is the area of the Schottky contact, J is the current density, A^* is the Richardson constant, T is temperature, q is the charge of one electron, k is the Boltzmann constant, E is the electric field, and ε is the permittivity of the semiconductor.

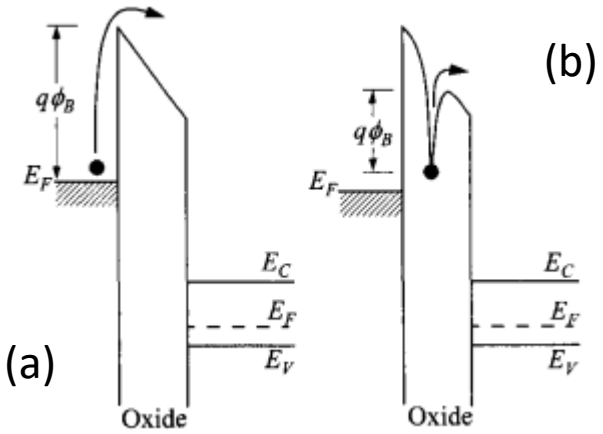


Figure 2-14. Schematics of (a) Schottky emission under reverse bias, and (b) Poole-Frenkel emission. [66]

The PF emission is also known as the internal Schottky emission [67]. Current conduction in the PF emission is due to the emission of trapped electrons in the insulating layer, as shown in Figure 2-14b [66]. The current conduction in PF emission is bulk limited instead of contact limited as in reverse bias Schottky emission [67]. The I-V characteristics of the PF emission are described by Equation 2.4 [66],

$$I \propto E\exp\left(\frac{-q\phi_B}{kT} + \frac{q}{kT}\sqrt{\frac{qE}{\pi\varepsilon}}\right) \tag{2.4}$$

2.4 Influence of the insulating material on the performance of RM

2.4.1 Insulating layer embedded with metal particles

Recently, insulating layer embedded with metal particles have attracted significant interest in non-volatile resistive memory applications [68, 69]. It was found that embedding metal NPs in the insulating layer can improve stability in, e.g. SiO_2 [68] and TiO_2 [70] based resistive memories. Well-dispersed metal NPs enhanced local electrical field [71] within the insulating layer which subsequently lowers operating voltages, and enhanced switching stability [70].

Figure 2-15 shows a study of the electric field distribution in Au nanoparticles embedded SiO_2 [72]. Au nanoparticles with 6 nm diameter were embedded in 36 nm thermal oxide (SiO_2:Au) [72], as shown in Figure 2-15a and 2-15b. The simulated electric field inside the SiO_2:Au composite shows an local intensification of the electric field in the direction from the top electrode to the bottom electrode [72]. The electric field enhancement is mainly produced by the repulsion of potential contours inside the metal nanoparticles [72]. The shape of the metal nanoparticles, whether it is

spherical or not, does not have a huge influence on the electric field enhancement effect while the overall size of the metal nanoparticle has to be noticeably smaller than the insulating layer [72].

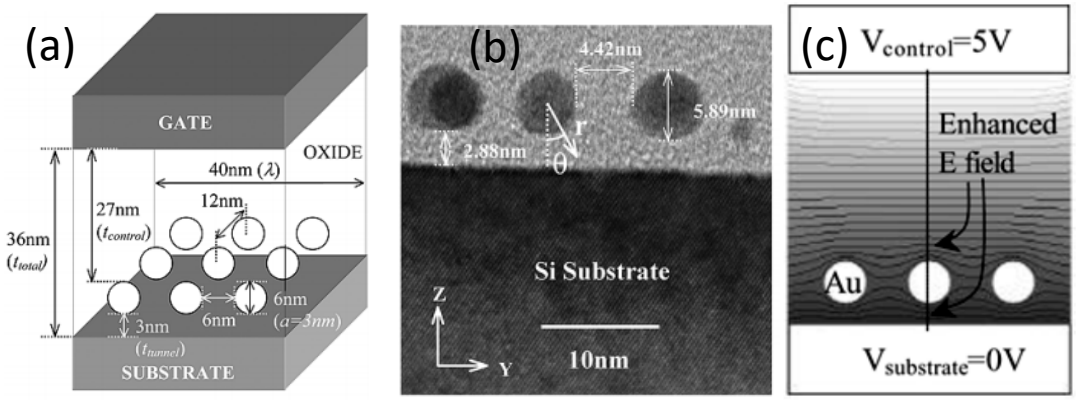


Figure 2-15. (a) Schematic of Gate/SiO_2:Au/Substrate structure. (b) TEM cross section image of Au nanoparticles in SiO_2. (c) Simulated local electric field. [72]

2.4.2 Thickness of the insulating layer

The thickness of the insulating layer of ECM resistive memories are usually in the range of 4 nm to 100 nm [63, 73]. The insulating thickness, in theory, has a large effect on the formation of the conductive filament. The length of the conductive filament is usually equal to the thickness of the insulating layer as shown in Figure 2-9. Hence the thicker the insulating layer, the longer distance the metal clusters need to migrate during the formation of the conductive filament. An increase of metal migration distance can potentially increase the electroforming time or forming voltage in the resistive memories when the metal ion mobility in the insulating layer is the dominating factor in the switching kinetic. Also, the electric field inside the insulating layer is proportional to the thickness of the insulating layer. The decrease of the electric field with the increasing insulating layer thickness could provide a noticeable effect on the resistive-switching [71]. An increase of forming voltage with increasing insulating layer thickness has been observed in ECM resistive memories, as shown in Figure 2-16 [74].

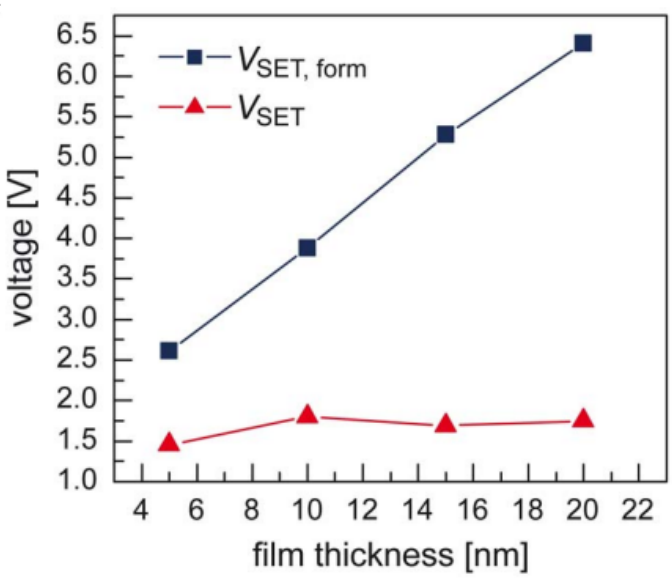


Figure 2-16. Forming voltage and SET voltage of Cu/SiO_2/Pt resistive memories with different SiO_2 thickness [74].

2.4.3 Using Back-end-of-line dielectric as the insulating layer

Back-end-of-line (BEOL) is the top part of an integrated circuit fabrication where the individual devices, such as transistors, capacitors, resistors, are interconnected with multiple layers of metallization layers. Modern integrated circuit is dominated by CMOS technology. All the BEOL in this thesis refers to CMOS BEOL. The metal-interconnect layers together with their associated interlayer dielectric in BEOL have a Metal/Insulator/Metal (MIM) structure similar to a resistive memory. The similarity in structure between BEOL layers and resistive memory opens up the opportunity to use this structure to incorporate embedded resistive memory in the BEOL without additional fabrication [7]. The resistive memory made use exclusively BEOL materials can be easily stacked on top of the CMOS control circuit. This 3D stacked configuration could effectively avoid the interconnect latency between the memory cells and the CMOS control circuit [7]. Also, it can achieve high-density memory integration with $4F^2/n$ effective area, where F is the feature size and n is the number of stacking layers. Moreover, lower fabrication cost and development time are expected if resistive memory is made exclusively by BEOL materials.

Many resistive memories have shown good compatibility with BEOL metal materials such as Cu and W. Cu has been widely accepted as the active electrode [10], and W demonstrated as the inert electrode [7]. Hence the main challenge to fabricate resistive memory using exclusively BEOL materials is to find suitable BEOL dielectrics as the insulating layer.

Many studies have demonstrated resistive memory that have an insulating layer made by BEOL compatible dielectrics such as TiO_2 [38], Al_2O_3 [35]. While these dielectrics are not currently in use

in the BEOL. Hence, extra fabrication cost and development time are expected to integrate the non-native dielectrics in the BEOL. Also, many studies have reported resistive memories using SiO_2 as the insulating layer [75], while SiO_2 has long been replaced by low dielectric constant (k) dielectrics such as a-SiOC:H in the BEOL [76]. Very few studies in the literature have reported resistive memories using BEOL dielectrics as the insulating layer [7]. Only a few resistive memories in these studies shown full switching cycles and the typical ON/OFF ratios were in the range of 10^3. Further exploration of using BEOL dielectrics as the insulating layer is required. A review of state-of-the-art BEOL dielectrics is given in the following.

Low-k dielectrics were introduced to BEOL to reduce Resistance-Capacitance (RC) delay of interconnect layers. The length of metal line increases and width of interlayer dielectric (IDL) reduces with the rapidly increasing CMOS integrated circuit sizes and lead to an increase in resistance and capacitance, respectively. Both the increase of resistance and capacitance contribute to the overall increase of RC delay in the BEOL layers [77]. A popular figure about the interconnect delay problem of CMOS interconnect published in the 1997 International technology roadmap for semiconductor (ITRS) [78], is shown in Figure 2-17. It was predicted that the interconnect delay will exceed the transistor delay (Gate delay) and dominate the overall delay after 250 nm node. This prediction has come true. As a result, low-k dielectrics are studied as a solution to reduce the capacitance of the BEOL layers and reduce the RC delay. The Silicon oxycarbide a-SiOC:H with k value in the range 2.5-4.2 [79] are introduced to replace Silicon oxyfluoride (SiOF, k=3.3-4 [80, 81]), as the ILD in BEOL. Besides, the diffusion barrier (DB), etch stop (ES), and Cu capping layer (CCL) which are required for the Cu damascene fabrication processes and usually would remain in the BEOL layers, also need to use materials with lower k to reduce their impact on the interconnect RC delay. A-SiOC:H with k value in the range 3.7-4.8 [82, 83] and hydrogenated SiC a-SiC:H with k value in the range 2.8-7.2 [84] are found promising in the DB, CCL, ES applications as replacements to amorphous hydrogenated Silicon nitride (a-SiN:H, k=6.8-7.5) [85]. In this thesis, one type of a-SiC:H and two types of a-SiOC:H were investigated as the insulating layer of resistive memories. The main difference between the two a-SiOC:H films are their C and O atomic%. For simplicity, the a-SiOC:H films with higher C at% are referred as a-SiCO:H. Also, a-Si(O)C:H are used to refer to all the a-SiC:H, a-SiCO:H, and a-SiOC:H films.

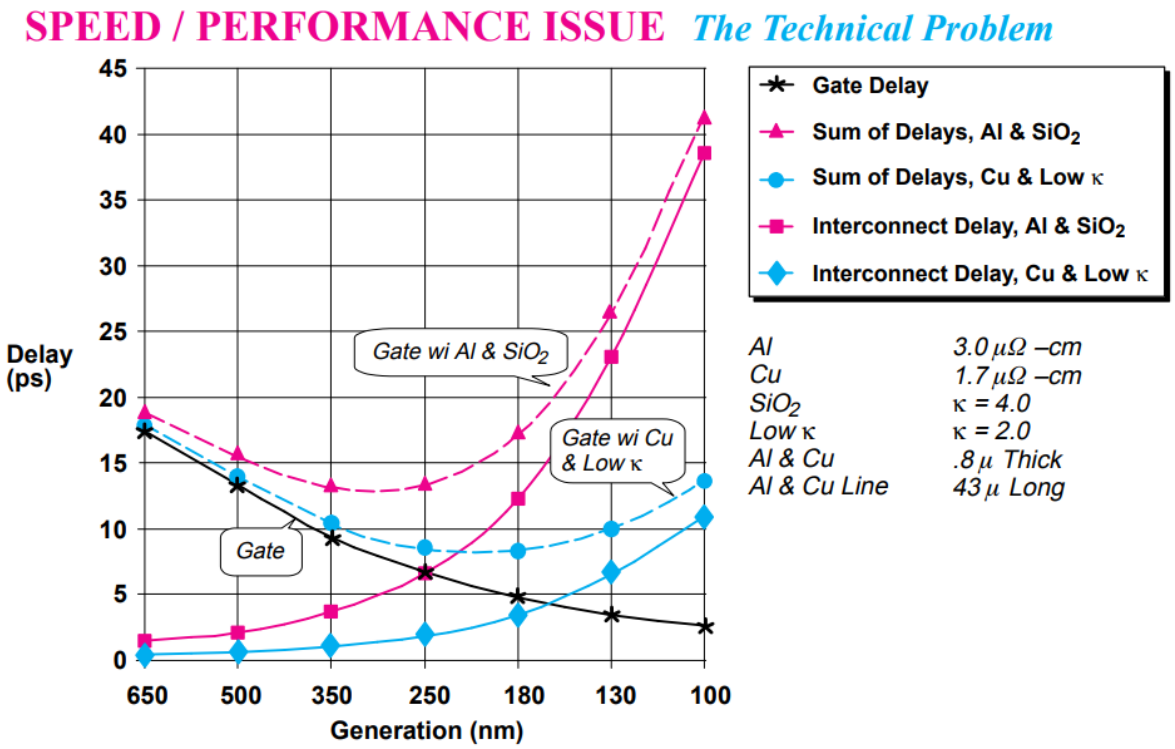


Figure 2-17. Gate and interconnect delay versus feature size [78].

2.5 Material properties and device applications of SiC

2.5.1 History and Application of SiC

SiC is a wide-band gap (E_g=2.0-7.0 eV) semiconductor with an indirect band structure [86, 87]. It was first discovered by Edward G. Acheson in 1890s. Naturally formed SiC which is known as the Moissanite is very rare hence the Acheson's discovery of SiC is very significant. The first large-scale application of SiC was for use as an abrasive. Later, the application SiC extended into photoelectronics. SiC has been widely applied in the early stage of blue light emission diode (LED) applications, mainly because it is possible to deposit SiC with Eg > 2.6 eV needed for blue light emission and the techniques to dope both n-type and p-type SiC with controlled resistivity were available [88].

In the last few decades, much attention has been given to crystalline SiC (c-SiC) electronic devices in high power, high temperature and in harsh environments due to its advanced material and chemical stability, high breakdown voltage, and high thermal conductivity [89, 90]. For example, c-SiC power MOS Field effect transistors (MOSFETs) have achieved performance figures-of-merit 70 times higher than Si power MOSFET [91]. Also, c-SiC Junction FET has shown stable operation up to 500°C [92] which is desirable for use in applications such turbine engine combustion monitor, geothermal wells [87]. Moreover, c-SiC Schottky diodes can resist 1.4 × 10^{16}/cm^2 24 GeV portion

and 7 × 10^{15}/ cm^2 1 MeV neuron irradiation [93]. The radiation hardness is required in harsh environment applications such as nuclear power instrument, or aerospace.

A-SiC:H and a-SiOC:H with k values in the range 3.7-4.8 [82, 83] are found interesting in BEOL Cu damascene process [94]. Both materials are considered as the Cu diffusion layers in BEOL to replace amorphous SiN [83, 95, 96] because their dielectric constant is lower than amorphous SiN. Low dielectric constant which can reduce the interconnect RC delay, is considered as an important standard for choose BEOL dielectrics [76]. In addition, the a-SiC:H has also found interesting in etch stop layer application because it has good chemical stability and can be selectively removed after oxidation [97]. Moreover, a-SiOC:H with k value in the range 2.5-4.2 [79] has been used as the ILD in BEOL [79]. Both a-SiCO:H and a-SiOC:H are refered as silicon-oxycarbide in the literature. The name silicon-oxycarbide is not used in this thesis to avoid confusion.

Recently amorphous SiC (a-SiC) has been demonstrated as the insulating layer in resistive memories. Advanced resistive-switching characteristics have been observed from these resistive memories, including high ON/OFF ratios [9, 46] and excellent retention [10, 11]. However, these resistive memories are facing challenges such as high V_{FORM}, not have used native BEOL materials. Also, the influence of the material properties of the a-SiC insulating layer on switching characteristics is not well understood and require further investigation. A wide variety of SiC materials including a-SiC, a-Si(O)C:H, and c-SiC have been applied as the insulating layer in this thesis to investigate the solution of the challenges that existing a-SiC resistive memories were facing and investigate the material properties of these materials from a general material point of view. Reviews over these SiC materials are given in the following.

2.5.2 Crystalline SiC

SiC has a large number of polytypes. About 200 polytypes of SiC have already been discovered [98] and can be classified into three lattice systems including Cubic (C), Hexagonal (H), and Rhombohedral (R). The crystal structure of SiC has an large influence on its material properties [89]. The crystal structure of SiC is composed of tetrahedral bonded Si-C bilayers. The wide variety of SiC polytypes is formed by Si-C bilayers stacked in different sequence. The stacking sequence of the Si-C bilayer is alike in the close-packed planes and different in the dimension perpendicular to these planes [99]. For example, Figure 2-18a-c show the crystal structure of three common SiC polytypes which are 4H-SiC, 3C-SiC, and 6H-SiC, respectively [100]. Every Si-C bilayer can be situated in one of the three possible positions in both lateral and vertical directions. The three positions are arbitrarily assigned the notation A, B, and C. The stacking sequence of the Si-C bilayer in the lateral direction in all the three SiC polytypes all follows the ABC-ABC stacking order. While the stacking sequence

of the Si-C bilayer in the vertical direction in the 4H-SiC, 3C-SiC, and 6H-SiC follows ABCB-ABCB, ABC-ABC, and ABCACB-ABCACB stacking orders, respectively. The number 4 in 4H-SiC means there are four Si-C bilayers in a stacking sequence, and the letter H means the crystal structure is a Hexagonal lattice system.

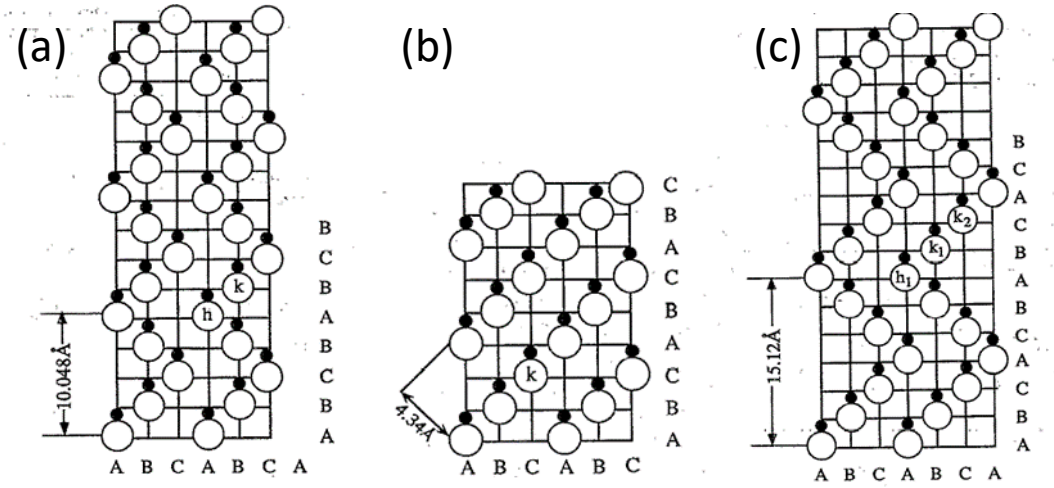


Figure 2-18. Crystal structure of SiC polytypes. (a) 4H-SiC, (b) 3C-SiC, and (c) 6H-SiC [100]. White and black circles represent Si and C, respectively.

Generally, SiC has high hardness around 2000 to 2800 Kg per mm^3 [101]. The density of SiC with low defects is around 3.2 g/cm^3. SiC can form good Schottky contacts with many metals and have Schottky barrier heights over 1 eV [99]. Schottky barrier height of SiC Schottky contacts shows weak dependence on metal work function, which is known as the Fermi-level pinning effect [99, 102]. Ohmic contact is difficult to achieve on SiC [89]. High doping concentration and high annealing temperature such as 800°C to 1300°C are required to obtain Ohmic contact on SiC with low contact resistance [99]. Common shallow dopants for SiC include Nitrogen (n-type), and Aluminum, Boron, Beryllium, Gallium, Oxygen, and Scandium (p-type) [87]. SiC sublimes at around 2100 °C at an ambient pressure of roughly 5 Torr [100]. Undoped SiC has a resistivity in the range 10^2 to 10^3 Ohm-cm [103].

The sublimation growth is the most investigated and successful technique for the growth of bulk SiC [104]. High-quality 6H-SiC and 4H-SiC wafers are available commercially [87]. Also, high-quality crystalline SiC could be grown on Si and SiC substrates. SiC epitaxy on Si substrate usually produces 3C-SiC [105]. Heteroepitaxial growth of 3C-SiC on 6H-SiC substrate [106] and homoepitaxy of 6H-SiC [107] and 4H-SiC [108] have also been demonstrated. The advantage of epitaxy of 3C-SiC on Si substrate is large area SiC can be obtained at low cost [109]. 3C-SiC grown on Si substrate using Vapor phase epitaxy (VPE) was used as the insulating layer in this thesis. Material properties of 3C-SiC and other semiconductors are listed in Table 2-2.

Table 2-2. Comparison of important semiconductor properties. [89]

Property	Si	GaAs	3C-SiC	6H-SiC	Diamond	GaN
Band gap (eV) at 300 K	1.1	1.4	2.2	2.9	5.5	3.4
Maximum operating temperature (K)	600	760	1200	1580	1400	N.A.
Electron mobility (cm^2/Vs)	1400	8500	1000	600	2200	900
Hole mobility (cm^2/Vs)	600	400	40	101	1600	150
Saturation velocity of electron (cm/s)	1×10^7	2×10^7	2×10^7	2×10^7	2.7×10^7	2.7×10^7
Breakdown voltage (V/cm)	3×10^5	4×10^5	2.1×10^6 to 4×10^6	2.5×10^6	10^7	5×10^6
Thermal conductivity (W/cm)	1.5	0.5	3.2 to 5	4.9	20	2.7
Refractive index (400 nm to 2400 nm)	3.9 [110]	3.4 to 3.6 [111]	2.7 [112]	2.5 to 2.8 [113]	2.4 [114]	2.3 to 2.6 [115]
Dielectric constant	11.8	12.8	9.7	9.7	5.5	9

2.5.3 Amorphous, hydrogenated, and oxidised SiC

Amorphous SiC thin films have attracted large research interests because they retain some of the advanced material properties of c-SiC and can be deposited using relatively inexpensive techniques and at relatively low deposition temperature [116]. Also, it is well known the material properties of amorphous SiC thin films could be tuned over a wide range by changing its composition and deposition method. For example, refractive index, dielectric constant, band gap, and density of amorphous SiC thin films can be tuned by adjusting Hydrogen, Carbon, and Oxygen concentration.

A-SiC thin film is usually deposited using Radio frequency (RF) sputtering. In RF sputtering of a-SiC, pure SiC target is used as the source of SiC, inert gas such as Ar gas is used as the sputtering gas, and materials including Si and metals can be used as substrates. Also, good film quality can be obtained by sputtering conducted at room temperature [117, 118]. The band gap and refractive index of a-SiC are around 2.1 eV [119] and 3.3 [120], respectively.

A-SiC:H thin film can be deposited using a wide variety of techniques including reactive sputtering and Plasma enhanced chemical vapor deposition (PECVD). Reactive sputtering of a-SiC:H is usually conducted by sputtering SiC target in Ar/H_2 gas mixture [121] or sputtering Si target in Ar/CH_4 gas mixture [116], at substrate temperature 100 °C to 300 °C. PECVD of a-SiC:H is usually conducted at deposition temperature 250 °C to 400 °C and uses trimethylsilane and other organosilicon gas as

the precursor gases. Also, these precursor gases are diluted in gases such as H_2 or He [84, 95] during the deposition. It is reported in the literature that both the dielectric constant and mass density of a-SiC:H decrease with the increasing H concentration [84]. Dielectric constant and mass density of a-SiC:H are in the range 2.8 to 7.2 and 1.0 g/cm^3 to 2.5 g/cm^3, respectively. Refractive index of a-SiC:H is in the range 1.6-2.6 [122]. Band gap of a-SiC:H has been determined to be 2.6 eV using Reflection electron energy loss spectroscopy (REELS) and Spectroscopic ellipsometry (SE) [123]. Resistivity of a-SiC:H films has been determined in the range 10^{10} Ohm-cm to 10^{17} Ohm-cm using two-point resistance measurement [84].

A-SiOC:H thin film is usually deposited by PECVD. PECVD of a-SiOC:H is usually conducted at deposition temperature 250 ^{o}C to 400 ^{o}C and uses various silane and methlysilane as precursor gases. Also, these precursor gases were diluted in N_2O, and other oxidising gases [82] during the deposition. Very low dielectric constant can be achieved by increasing C concentration in a-SiOC:H or increasing O concentration in the a-SiOC:H, respectively [79, 124, 125]. Dielectric constant of a-SiOC:H is around 3.1-4.8 [76]. Refractive index of a-SiOC:H is in the range 1.4-1.7 [79, 125]. Mass density of a-SiOC:H is in the range 1.6-3 g/cm^3 [79]. Band gap of a-SiOC:H is around 2.6-3.6 eV [82].

A wide variety of techniques have been applied to characterise the material properties of SiC thin films. Some of the commonly used techniques including X-ray diffraction (XRD) spectroscopy, X-ray photoelectron (XPS) spectroscopy, and Fourier-transform infrared (FTIR) spectroscopy have been applied in this thesis and will be introduced in Chapter 3.

2.5.4 Existing RMs using a-SiC as the insulating layer

Resistive memories with a-SiC insulating layer have been studied in a number of cases [9-11, 46, 47] before this PhD project started. These works are mainly conducted by W. Lee et al. from Gwangju Institute of Science and Technology and L. Zhong et al. from our research group. The a-SiC insulating layers in these resistive memories are all deposited using RF sputtering at room temperature. Cu is used as the active electrode in all these a-SiC resistive memories. Pt [11] and Au [10] are used as the inert electrode in Cu/a-SiC/Pt and Cu/a-SiC/Au resistive memories, respectively.

W. Lee et al. investigated the resistive-switching of Cu/a-SiC/Pt resistive memories [11, 47]. Figure 2-19 shows the bipolar switching characteristics of Cu/a-SiC/Pt resistive memories with and without a $Ge_2Sb_2Te_5$ (GST) thermal barrier on top of Cu. The ON/OFF ratio is found increased from 10^2 to 10^4 due to the addition GST thermal barrier on top of Cu is reported, which is attributed to the thermally assisted electrochemical reduction of the Cu filament induced by the GST thermal barrier. The Cu conductive filament in LRS leads to the Ohmic conduction mechanism which is shown in Figure 2-20a, and metallic temperature dependence of current which is shown in Figure 2-20b. The

current conduction in HRS is determined to be Poole-Frenkel emission. The Cu/a-SiC/Pt resistive memories show excellent retention over 10^4 s at 150 °C, as shown in Figure 2-6b. Also, an accelerated test of mean time to failure has been conducted, as shown in Figure 2-21a. The mean time to failure at 85 °C is estimated to be 10 years, as shown in Figure 2-21b. W. Lee et al. ascribed the long retention time of Cu/a-SiC/Pt resistive memories to the high chemical stability of SiC and the ability to act as a Cu diffusion barrier. In addition, large endurance around 10^4 and fast switching speed approximately 500 ns have been measured from Cu/a-SiC/Pt resistive memories, as shown in Figure 2-6a.

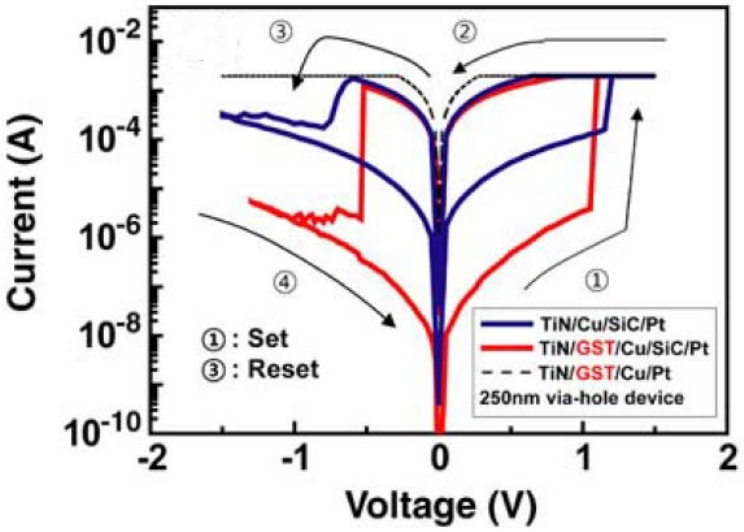


Figure 2-19. Typical resistive-switching I-V characteristics of Cu/a-SiC/Pt resistive memories with (red curves) and without (blue curves) a GST thermal barrier. [47]

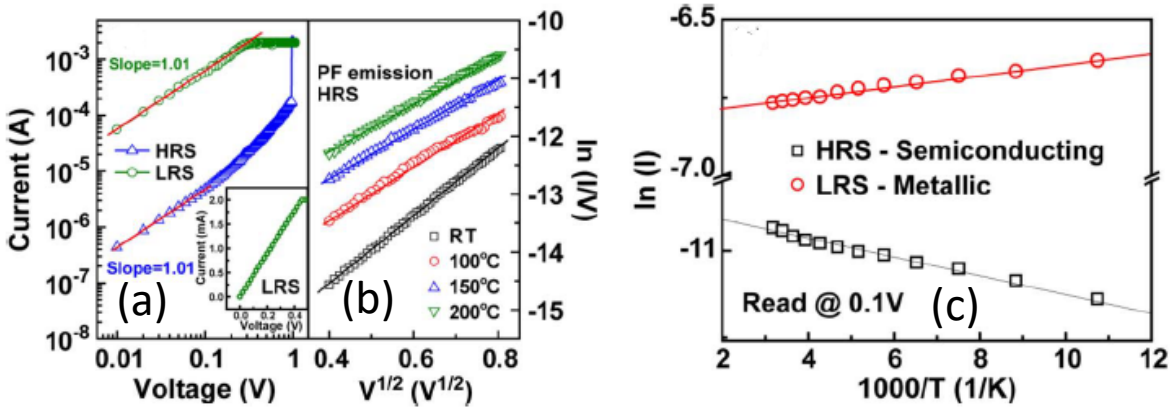


Figure 2-20. I-V characteristics of Cu/a-SiC/Pt resistive memories in (a) Log(I)-Log(V) and (b) Ln(I/V)-√V plots. (c) HRS and LRS current vs temperature for Cu/a-SiC/Pt resistive memories. [11]

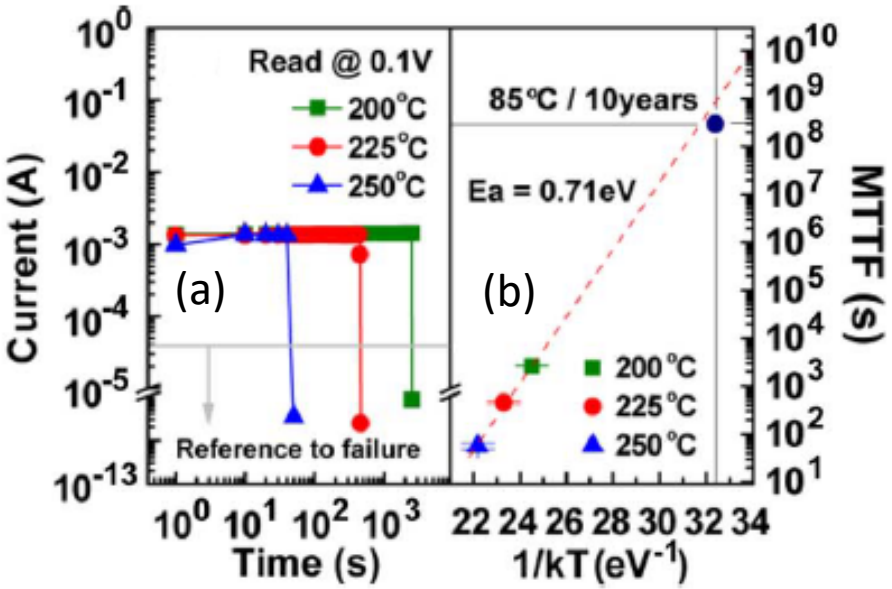


Figure 2-21. Retention test of Cu/a-SiC/Pt resistive memories. (a) Acceleration test at 200 °C, 225 °C, and 250 °C and (b) mean time to failure vs the reciprocal temperatures. [11]

L. Zhong et al. investigated the resistive-switching of Cu/a-SiC/Au resistive memories [9, 10, 46]. Nonpolar resistive-switching consists of four possible modes: +bipolar, +unipolar, -bipolar, and –unipolar, has been observed from the Cu/a-SiC/Au resistive memories [10]. Figure 2-22 shows the switching I-V characteristics of all the four modes. A higher V_{FORM} in the electroforming cycle in contrast to subsequent V_{SET} has been observed frequently in all the four modes. The higher V_{FORM} is attributed to the requirement to induce the conductive paths in the pristine device. Ultrahigh ON/OFF ratio up to 10^9 and excellent retention over 10^3 s at 85 °C has been observed. Ohmic conduction and metal-like temperature dependence of the resistance have been observed from the LRS of Cu/a-SiC/Au resistive memories switched by both $+V_{SET}$ and $-V_{SET}$, as shown in Figure 2-11. The SET process using $+V_{SET}$ is attributed to the formation of Cu filament. The SET process using $-V_{SET}$ is attributed the formation of Au filament. Current conduction in the HRS of Cu/a-SiC/Au resistive memories switched in all the four possible modes has been found being dominated by the Schottky emission under reverse bias, as shown in Figure 2-23. The insets of Figure 2-23 show the schematics of RESET process of the four possible modes. The first inset on the top shows the rupture of the Cu filament due to Joule heating enhanced lateral diffusion in the RESET of +unipolar mode. The second inset on the top shows the rupture of the Cu filament due to electrochemical dissolution in the RESET of +bipolar mode. The third inset shows the rupture of the Au filament due to electrochemical dissolution in the RESET of –bipolar mode. The last inset shows the rupture of the Au filament due to Joule heating enhanced lateral diffusion in the RESET of –unipolar mode.

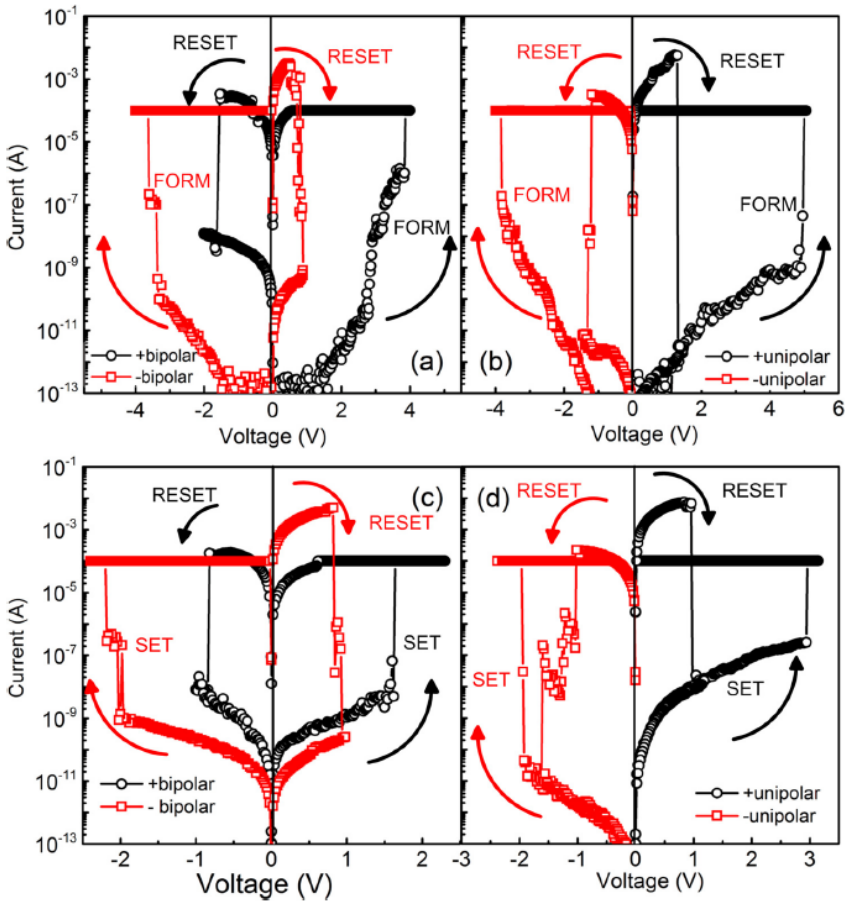


Figure 2-22. Switching I-V characteristics of Cu/a-SiC/Au resistive memories. Electroforming cycles of (a) +bipolar and -bipolar modes, and (b) +unipolar and -unipolar modes. Typical switching cycles of (c) +bipolar and -bipolar modes, and (d) +unipolar and -unipolar modes. The arrows indicate the respective voltage sweeping directions. [10]

Although many advanced switching characteristics have been measured from the Cu/a-SiC/Pt and Cu/a-SiC/Au resistive memories, there are still many challenges to be solved in these resistive memories using a-SiC as the insulating layer to be superior to other resistive memories. One of these challenges is to reduce the V_{FORM} which could affect the power consumption and complexity of peripheral power-supply circuit [12]. Reduce of V_{FORM} by embedding Cu in the a-SiC films is discussed in Chapter 5. Another challenge is to achieving device structure entirely using native BEOL materials which would enable low fabrication cost to embed a-SiC based resistive memories in the CMOS BEOL [7]. A replacement of the Au electrode by W electrode which is a native BEOL metal, in Cu/a-SiC/W resistive memories is discussed in Chapter 4. Also, resistive-switching of Cu/a-Si(O)C:H/W resistive memories which are fabricated entirely using standard BEOL materials, is discussed in Chapter 6. Moreover, the existing ECM mechanism cannot precisely predict the switching voltage and resistance state of resistive memories, and there is a lack of knowledge on how the material properties of the insulating layer affect resistive-switching performance and mechanisms. The influence of material properties of the a-SiC:Cu film, a-Si(O)C:H film, c-SiC film, on

switching characteristics of corresponding resistive memories, is discussed in Chapter 5, Chapter 6, and Chapter 7, respectively.

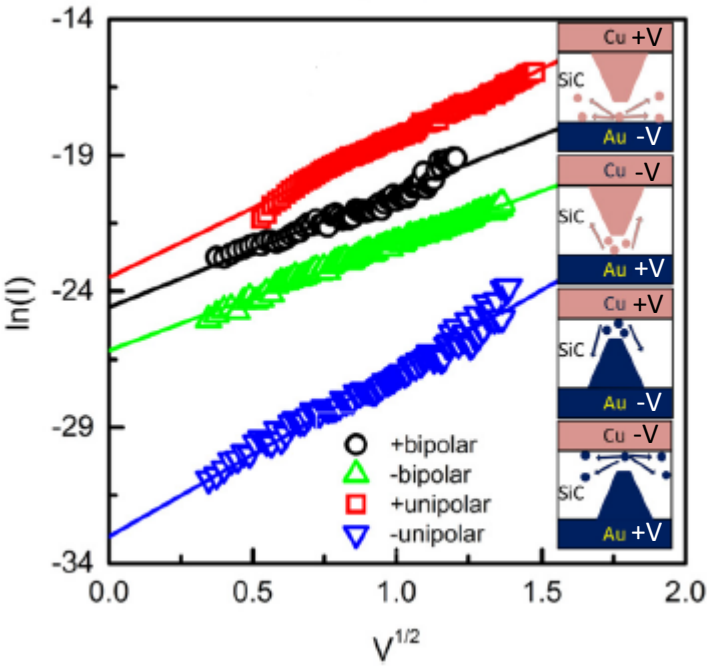


Figure 2-23. HRS I-V characteristics in Ln(I)-√V plots, with linear fits to the Schottky emission under reverse bias. The insets illustrate the possible RESET mechanisms for each switching mode: +unipolar, +bipolar, -bipolar, and –unipolar in the top-down sequence. [10]

2.6 Summary

This Chapter reviewed a wide range of topics relevant to the electrical and material characterisation of a-SiC resistive memories. Firstly, the challenges which inhabit the existing non-volatile memories to fully resolve the demands on higher capacity, lower cost, and lower power consumption were reviewed. Also, the fast development of ECM resistive memories was reviewed. Next, fundamentals of resistive memory including structure, resistive-switching characteristics, and common switching mechanisms were reviewed. All the a-SiC resistive memories in this thesis are classified as ECM resistive memories. In-depth review of the physics of ECM resistive memories was given, which covers the electroforming, SET, and RESET switching mechanisms, and current conduction mechanisms in LRS and HRS. The influence of material properties of the insulating layer on ECM resistive memory performance was reviewed afterwards. The improvement of switching stability attributable to the embedding of metal particles in the insulating layer and the decrease of V_{FORM} with the decreasing of insulating layer thickness were reviewed. In addition, an overview of BEOL dielectrics that are expected to be used as the insulating layer is given. At the end of this chapter, an overview of a variety of SiC materials which were used as the insulating layer in this thesis was

provided. Material properties of a-SiC, a-Si(O)C:H, and c-SiC thin films deposited using RF sputtering, PECVD, and VPE, respectively, were reviewed. Also, material characteristics of these thin films including XRD, XPS, and FTIR were reviewed. In addition, existing a-SiC resistive memories were reviewed, including Cu/a-SiC/Au resistive memories which shown ultra-high ON/OFF ratios and nonpolar switching and Cu/a-SiC/Pt resistive memories which shown excellent retention and high switching speed were reviewed. The challenges of existing a-SiC were discussed, and the works in the following Chapters related to these challenges were introduced.

Chapter 3: Experimental Methodologies

This Chapter reports the experimental methodologies used in this thesis. Firstly, the design and fabrication of resistive memories which have amorphous and crystalline SiC as the insulating layer were reported. Next, the methods used to characterise the material and electrical properties of these amorphous and crystalline SiC thin films were introduced. At the end of this Chapter, the methods used to characterise the resistive-switching functionalities were introduced.

3.1 Design and fabrication of SiC thin films and devices

3.1.1 RMs that have a-SiC and a-SiC:Cu insulating layer

Resistive memories that have a-SiC and a-SiC:Cu insulating layer in this thesis include Cu/a-SiC/Au, Cu/a-SiC/W, and Cu/a-SiC:Cu/Au resistive memories. Cu/a-SiC/Au, Cu/a-SiC/W resistive memories are referred as a-SiC resistive memories and Cu/a-SiC:Cu/Au are referred as a-SiC:Cu resistive memories in this thesis for simplicity. All these resistive memories have the same device structure as shown in Figure 3-1. 300 nm Au or W inert electrode is on top of the Si substrate covered with 1 µm thermal SiO_2. A SiO_2 barrier which has 250 nm thickness and 100 µm × 100 µm surface area is on top of the Au or W inert electrode. In the centre of the SiO_2 barrier is an open hole which has an area of 2 µm × 2 µm to 100 µm × 100 µm. The area of the hole is also active device area of the resistive memory. The extra Cu/SiC area surrounding the active device area was designed to provide enough space to place the testing probe in the current-voltage measurements. 40 nm a-SiC or a-SiC:Cu insulating layer and 300 nm Cu active electrode is on top of the SiO_2 barrier. The surface area of this SiC/Cu layers is 100 µm × 100 µm. The SiC/Cu layers contact the inert electrode directly in the centre hole of the SiO_2 barrier and form the Cu/SiC/metal resistive memory structure.

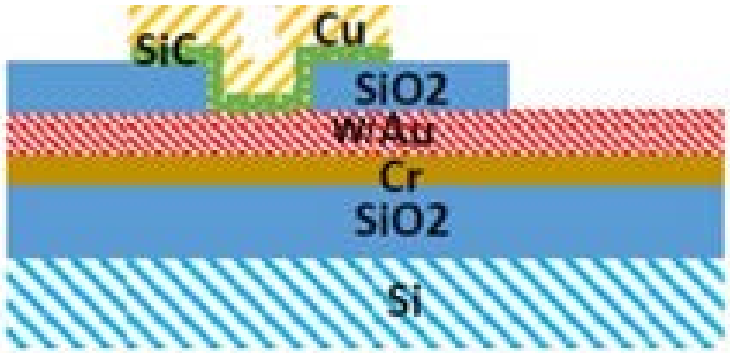


Figure 3-1. Cross-section schematic of a-SiC and a-SiC:Cu resistive memories.

The fabrication of all the a-SiC and a-SiC:Cu resistive memories were done by Dr. Le Zhong and Dr. Ruomeng Huang. Fabrication process flow of these resistive memories is shown in Figure 3-2. In step 1, a thin Cr adhesion layer and 300 nm Au or W were sputtered on the Si substrate coated with 1 µm thermal SiO_2. In step 2, 250 nm SiO_2 was reactive sputtered on the Au or W. Photolithography was then applied to pattern a layer of photoresist (PR) on the SiO_2. In step 3, SiO_2 was etched using Reactive ion etching (RIE). The areas where the SiO_2 was etched away are the active device area and the Au or W contact. In step 4, another photolithography was applied to pattern a layer of PR on the SiO_2. In step 5, 40 nm a-SiC or a-SiC:Cu, and 300 nm Cu active electrode were sputtered without breaking the chamber vacuum. In step 6, a lift-off process was performed to form the final device structure, by bathing the device chip in Acetone.

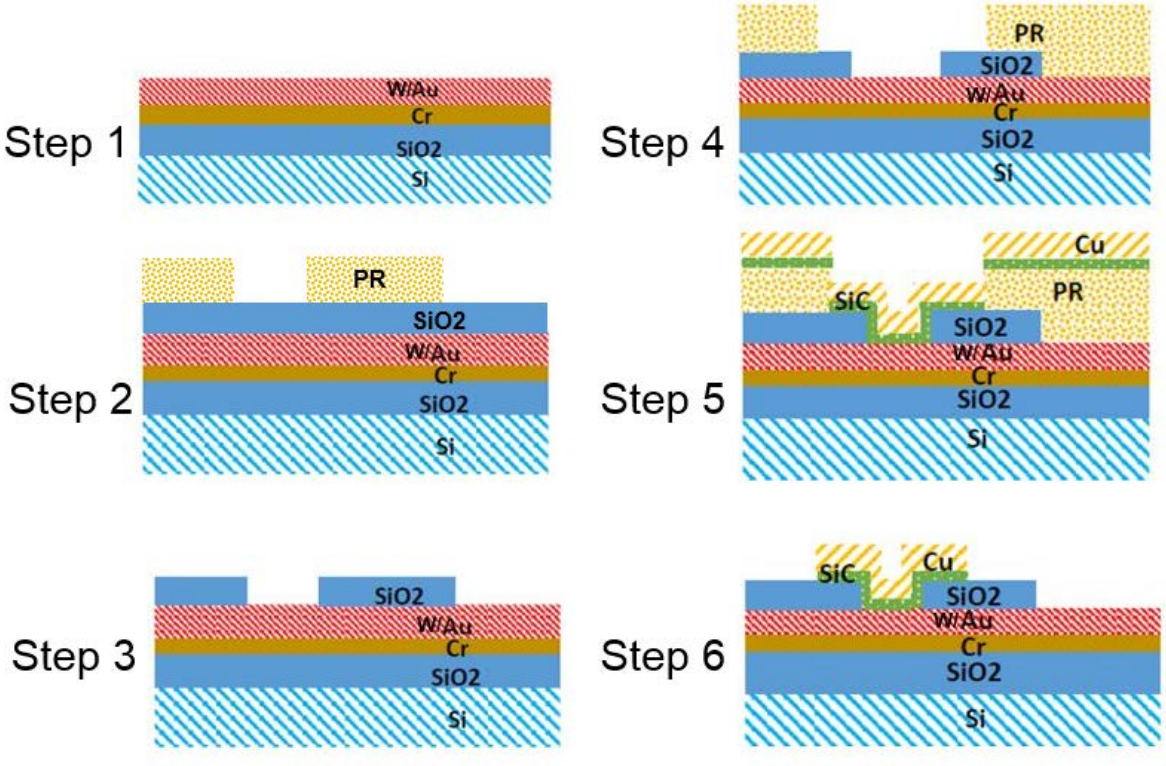


Figure 3-2. Fabrication process flow of a-SiC and a-SiC:Cu resistive memories.

3.1.2 RMs that have Back-end-of-line dielectrics as the insulating layer

Resistive memories that have BEOL dielectrics (a-Si(O)C:H) as the insulating layer in this thesis include W/a-SiC:H/Cu, W/a-SiCO:H/Cu, and W/a-SiOC:H/Cu resistive memories. All these W/a-Si(O)C:H/Cu resistive memories are referred as a-Si(O)C resistive memories in this thesis for simplicity. All the a-Si(O)C:H resistive memories have the W/a-Si(O)C:H/Cu structure as shown in Figure 3-3. In this device structure, 300 nm Cu active electrode is on top of the Si substrate coated with 100 nm SiO_2, 100 nm SiN, 10 nm TaN, and 8 nm Ta. 20 nm or 40 nm a-Si(O)C:H is on top of the Cu. W electrodes with about 280 nm thickness and surface area of 2 µm × 2 µm to 100 µm × 100

µm, is on top of the a-Si(O)C:H insulating layer. Also, there are a few Cu contact windows on the side of each substrate.

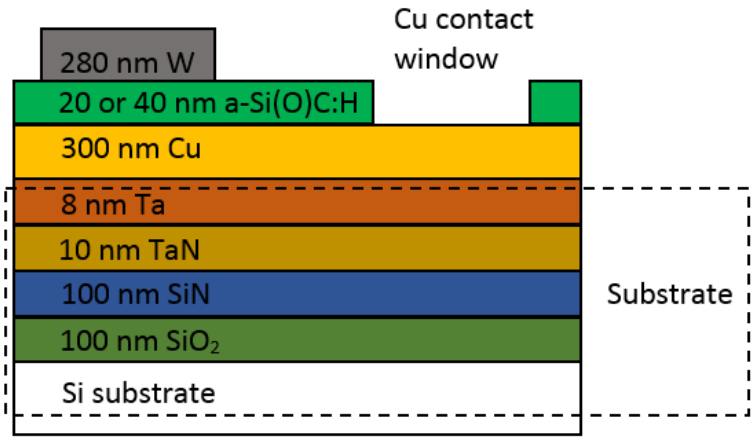


Figure 3-3. Cross-section schematic of a-Si(O)C:H resistive memory.

All the Si substrates coated with a-Si(O)C:H were fabricated by Intel®. The a-Si(O)C:H thin films on top of these substrates were deposited using Plasma enhanced chemical vapor deposition (PECVD). Chemical composition and mass density of the a-SiC:H, a-SiOC:H, and a-SiCO:H films were provided by Intel, as shown in Table 3-1.

Table 3-1. Chemical composition and mass density of a-SiC:H, a-SiOC:H, and a-SiCO:H films.

Dielectric	at% Si	at% C	at% O	at% H	Mass density ($g \cdot cm^{-3}$)
a-SiC:H	31.5	33.2	0.1	35.1	2
a-SiOC:H	36.1	10	45.2	8.7	2.4
a-SiCO:H	24.5	22.7	23.7	29	2

Deposition and patterning of the W electrodes on the a-Si(O)C:H thin films were conducted at the University of Southampton. Firstly, a photolithography process was applied to patterned a layer of PR on the a-Si(O)C:H. Next, W thin film about 280 nm thick was DC sputtered. Then, a lift-off was conducted by bathing the device chip in Acetone for about 3 min, to realise the W electrode pattern. In addition, Cu contact windows were created on the side of the device chip by scratching-off the a-Si(O)C:H on top of the Cu using a razor blade.

3.1.3 RMs that has crystalline SiC insulating layer

c-SiC has been used as the insulating layer in Cu/c-SiC/Si resistive memory. Figure 3-4 shows the cross-section schematic of Cu/c-SiC/Si resistive memory. Cu electrodes with 300 nm thickness and

100 µm × 100 µm surface area are on top of the Si substrate coated with c-SiC. The Si substrate which has low resistivity was used as the inert electrode of c-SiC resistive memory.

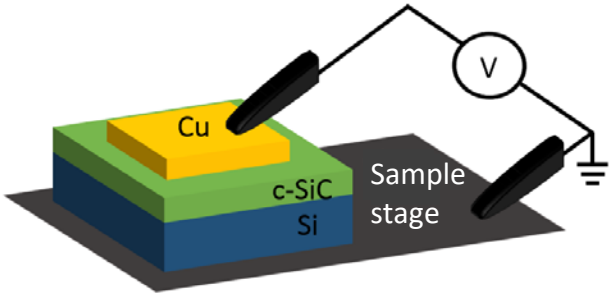


Figure 3-4. Cross-section schematic of c-SiC resistive memories.

The c-SiC/Si substrate was provided by Dr. Matteo Bosi from Institute of Materials for Electronics and Magnetism, Parma, Italy. The Si substrate is p-type doped, and has 0.01-0.02 Ohm-cm resistivity, a size of 2 cm × 8 cm, and (100) orientation. c-SiC was grown on the Si substrate using Vapor phase epitaxy (VPE). The VPE of c-SiC was conducted in the way as the schematic in Figure 3-5 shows [109]. The VPE of c-SiC started with a carbonization step where C_3H_8 gas was injected into the growth chamber and the growth temperature was raised to 1125 °C. Then, a heating ramp step began where SiH_4 and C_3H_8 gases were injected into the growth chamber and the growth temperature was raised to 1380 °C. The growth continued for another 1 min after the growth temperature reached 1380 °C and then the VPE of c-SiC was completed. Deposition and patterning of Cu electrodes on the c-SiC/Si substrate were conducted at the University of Southampton. Firstly, a photolithography process was applied to patterned a layer of PR on the c-SiC. Next, Cu thin film about 300 nm thick was DC sputtered. Then, a lift-off was conducted by bathing the chip in Acetone for about 3 min, to realise the Cu electrode pattern.

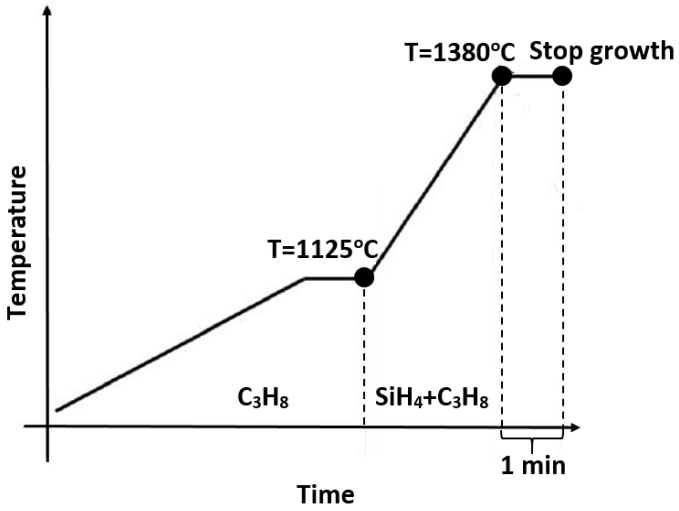


Figure 3-5. Schematic of c-SiC VPE [109]. Time and temperature are not in scale in the plot.

3.1.4 Sputtering of a-SiC, a-SiC:Cu, Cu, and W thin films

Sputtering of the a-SiC, a-SiC:Cu, Cu, and W thin films has been conducted using a K.J. Lesker® sputtering system as shown in Figure 3-6a. For the record, sputtering of the a-SiC:Cu thin films were done by Dr. Le Zhong. The rest sputtering was completed by the author himself. The sputtering system has two Radio frequency (RF) target holders with individual RF power supplies, and two Direct current (DC) target holders with individual DC power supplies. In the sputtering process, sputtering gas such as Argon gas was injected into the vacuum sputtering chamber. A high voltage bias was applied to the target holder to form an Ar plasma near the target. Ar ions (Ar^+) from the plasma strike the negatively biased target and sputter out target particles from the target. The sputtered target particles would fly towards the substrate and form a film, as shown in Figure 3-6b. In DC sputtering, the target was negatively biased all the time, while in RF sputtering, the field w oscillated between negative and positive at usually 13.56 MHz, to prevent charging of the target [126].

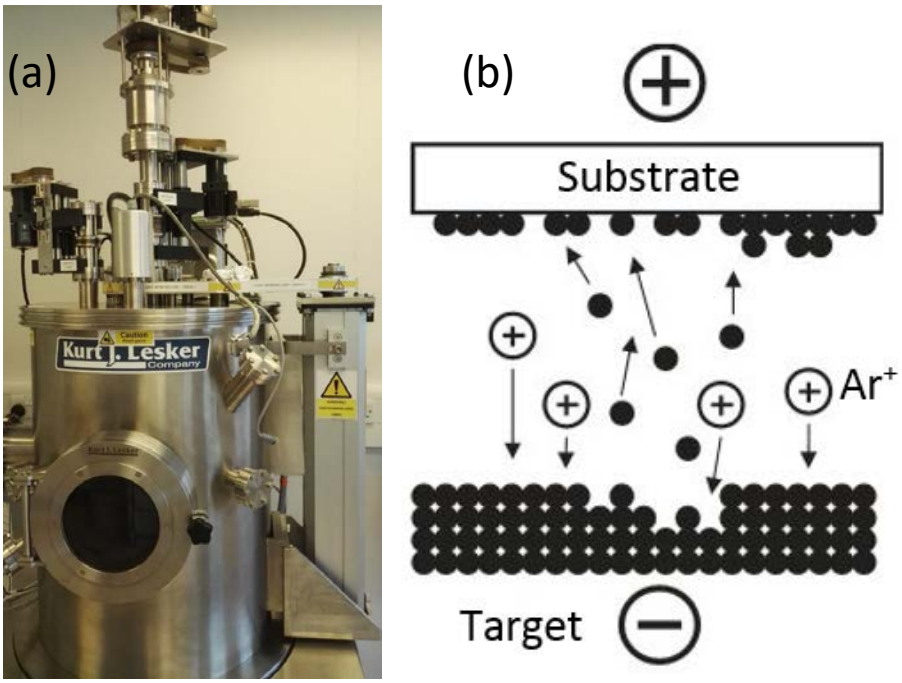


Figure 3-6. (a) K.J.Lesker® sputtering system. (b) Schematic of the sputtering process [126].

For all the sputtering processes conducted in the K.J.Lesker® sputtering system, SiC target that have 99.9% was sputtered using an RF target holder. Cu and W targets that have 99.99% and 99.95% purities, respectively were sputtered using a DC power supply. Substrates were ultrasonically cleaned in Acetone and IPA, subsequently, to minimize contamination on the substrates. After loading the substrate, the sputtering chamber was pumped to high vacuum $<10^{-6}$ mBar to minimize possible impurity in the sputtering chamber. Then the Ar gas was injected into the sputtering chamber, and the sputtering process started. The substrate temperature was at room temperature

during the sputtering. Parameters including target power, Ar gas flow, and Ar gas pressure used in the sputtering of a-SiC and a-SiC:Cu thin films are listed in Table 3-1 and 3-2, respectively. Sputtering condition used in the sputtering of a-SiC and a-SiC:Cu insulating layers are highlighted in Table 3-2 and 3-3, respectively. Sputtering condition of Cu and W electrodes are listed in Table 3-4.

Table 3-2. Sputtering condition of a-SiC thin films. Sputtering of a-SiC insulating layer of a-SiC resistive memories used the same condition as a-SiC sample A.

Sample name	Sputtering process	Substrate	SiC target power (W)	Ar gas flow (sccm)	Ar pressure (mBar)	Sputtering time (min)
A	No.1	SiO_2/Si	250	3	5x10-3	70
B	No.1	Si	250	3	5x10-3	70
C	No.2	SiO_2/Si	250	3	5x10-3	70
D	No.2	Si	250	3	5x10-3	70
E	No.3	SiO_2/Si	300	3	5x10-3	50
F	No.3	Si	300	3	5x10-3	50
G	No.4	SiO_2/Si	150	3	5x10-3	115
H	No.4	Si	150	3	5x10-3	115
I	No.5	SiO_2/Si	250	5	8x10-3	90
J	No.5	Si	250	5	8x10-3	90
K	No.6	SiO_2/Si	250	10	2x10-2	105
L	No.6	Si	250	10	2x10-2	105
M	No.7	SiO_2/Si	150	3	5x10-3	120
N	No.7	Si	150	3	5x10-3	120
Q	No.8	Si	250	3	5x10-3	70
S	No.8	SiO_2/Si	250	3	5x10-3	70

Table 3-3. Sputtering condition of a-SiC:Cu thin films. Sputtering condition of a-SiC:Cu thin films with 20 Cu% and 30 Cu% was used in the sputtering of a-SiC:Cu insulating layer of a-SiC:Cu resistive memories.

a-SiC:Cu thin film	SiC target power (W)	Cu target power (W)	Ar gas flow (sccm)	Ar pressure (mBar)
0 Cu%	250	0	3	5×10^{-3}
30 Cu%	250	15	3	5×10^{-3}
46 Cu%	250	25	3	5×10^{-3}
57 Cu%	250	35	3	5×10^{-3}
20 Cu%	340+300	10	3	5×10^{-3}
22 Cu%	300+300	10	3	5×10^{-3}
23 Cu%	250+250	10	3	5×10^{-3}
28 Cu%	200+200	10	3	5×10^{-3}
41 Cu%	150+150	10	3	5×10^{-3}

Table 3-4. Sputtering condition of Cu and W thin films.

Metal	SiC target power (W)	Ar gas flow (sccm)	Ar pressure (mBar)
Cu	110	3	5×10^{-3}
W	210	3	5×10^{-3}

3.1.5 Patterning of device structure using photolithography

The device structure of resistive memory was patterned on the device chip using photolithography. An EVG® 620T mask aligner as shown in Figure 3-7 was used to transfer the designed patterns on the photomask to the PR. Positive PR S1813® and negative PR AZ2070® were used in the patterning of device structures. In the photolithography process, firstly the PR was spin coated on the substrate. Then the substrate coated with PR was baked on a hotplate. Next, the patterns on the photomask were transferred to the PR using the mask aligner. During the exposure, Ultra-violet (UV) light went through the transparent area of the photomask and projected on the PR. The patterns were realised on the PR afterwards, by bath the device chip in developer solvent of the PR. For positive PR S1813®, the area that was exposed to the UV light (broadband) was removed in the developer, as shown in Figure 3-8a. For negative PR AZ2070®, the area that was not exposed to the UV light (365 nm i-line) was removed in the developer, as shown in Figure 3-8b.

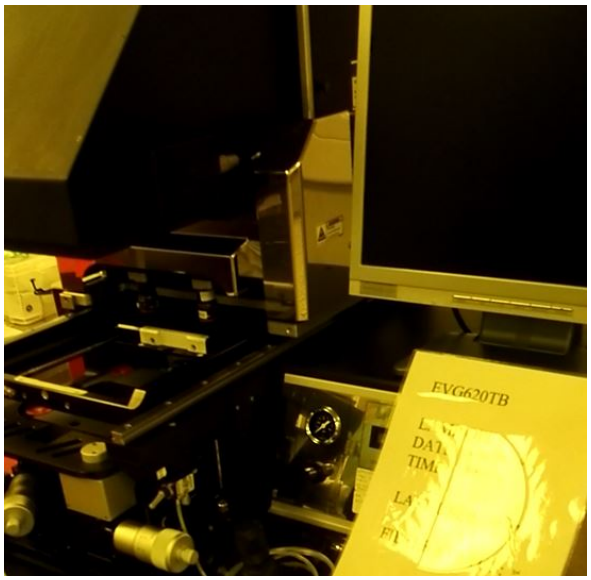


Figure 3-7. EVG 620T® mask aligner.

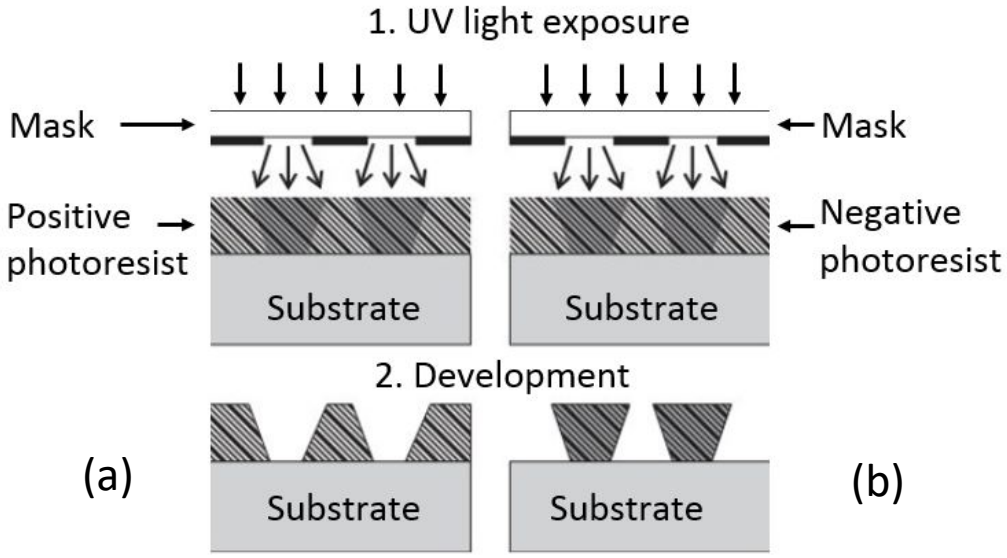


Figure 3-8. Schematics of photolithography processes of (a) positive PR and (b) negative PR [126].

3.2 Methods for material characterisation

3.2.1 Energy dispersive X-ray spectroscopy

Energy-Dispersive X-ray Spectroscopy (EDX) measurements have been conducted on a-SiC:Cu thin films sputtered on Al substrates using a Jeol JSM 6500F Field emission scanning electron microscope (FESEM). The use of Al substrates eliminates any possible Si EDX spectra from the SiO_2/Si substrates and thus ensure all Si spectra can be attributed to the deposited a-SiC:Cu films. For the record, the EDX measurement was done by Dr. Le Zhong. Figure 3-9 shows the basic working principle of EDX. Firstly, an electron beam with high kinetic energy is projected on the sample. Some of the electrons

will collide with the atoms in the sample as shown in Figure 3-9a. The core-level electron can be knocked-off from the atom through inelastic scattering as shown in Figure 3-9b. An electron on outer shell will decay spontaneously to the inner shell electron vacancy and emit a photon as shown in Figure 3-9c. The energy of the emitted photon equal to the energy difference between inner shell and outer shell. This energy is different for each element due to the different atomic structure. Hence the energy of the emitted photon can be used to identify the chemical composition of the sample in EDX analysis. The EDX system which is usually installed in an SEM or Transmission electron microscope (TEM), uses a photodetector to measure the number of photons emitted in an energy spectrum such as 0.1 eV to 10 eV which is mainly in the X-ray range. Chemical composition of the sample can be identified by the peak position in the EDX spectrum apart from H and He which cannot be detected by EDX. Also, the intensity ratio of peaks in the EDX spectrum can be used to calculate the atomic concentration of each element in this sample.

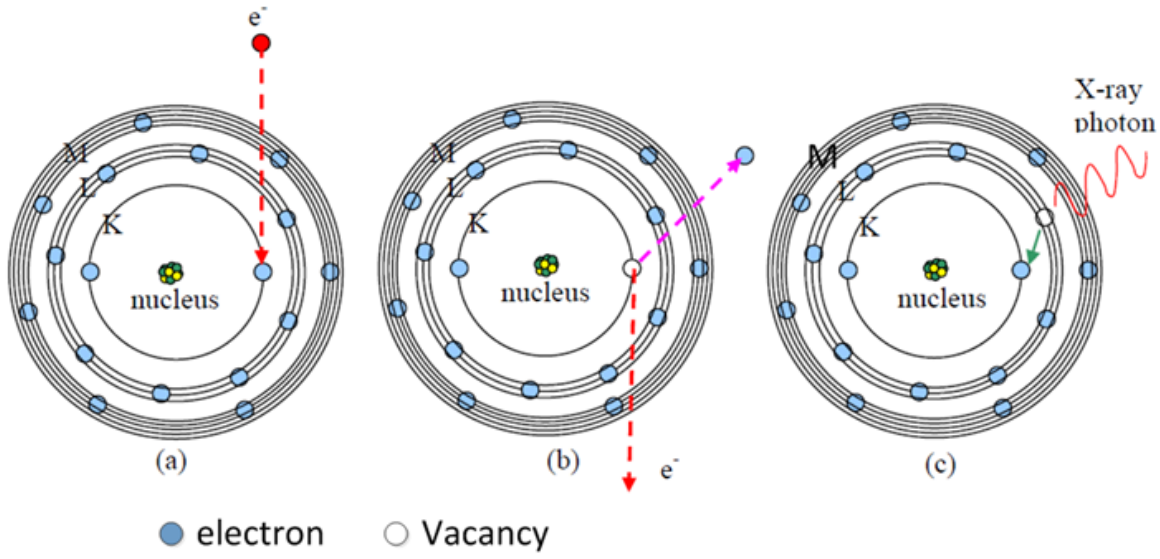


Figure 3-9. Working principle of Energy Dispersive X-ray Spectroscopy. (a) Bombard specimen atom with high-energy electron, (b) generation of electron vacancy, (c) electron transition and emission of X-ray photon [127].

3.2.2 X-ray diffraction

X-ray Diffraction (XRD) measurement has been conducted on a-SiC:Cu and c-SiC thin films using a Rigaku Smartlab® XRD system. For the record, the part of XRD measurement conducted on a-SiC:Cu thin films was done by Dr. Le Zhong. The XRD measurement conducted on c-SiC thin films was done by the author himself. Figure 3-10a shows the Rigaku Smartlab® XRD system. The basic operation principle of XRD measurement is introduced as follows.

A Cu Kα (0.1541 nm) X-ray source is used in the Smartlab® XRD system. Diffraction spectrum of the crystalline sample measured to study the microstructure of the sample. Figure 3-10b shows the Schematic of X-ray diffraction from parallel crystal lattice plane. Two coherent X-rays (X-ray 1 and X-ray 2) were projected on to the parallel crystal lattice plane with an incidence angle θ. The difference of pass length between X-ray 1 and X-ray 2 reflected from the lattice planes equals AB+BC. Constructive interference of these X-rays happens when AB+BC equal to an integer multiple of half wavelength of these X-rays. This relation between constructive interference angle and wavelength is known as Bragg's law and is described by Equation 3.1,

$$n\lambda = 2d_{hkl}sin\theta, \tag{3.1}$$

where n is an integer, λ is the wavelength of the incidence X-ray, d_{hkl} is the distance between lattice planes. Usually, only the primary diffraction maximum when n=1, is considered in XRD analysis. Hence Equation 3.1 is simplified as Equation 3.2,

$$\lambda = 2d_{hkl}sin\theta \tag{3.2}$$

Constructive interference angle is different in different crystal orientation and in different crystal system because d_{hkl} is different. Hence, the microstructure of the sample could be revealed by observation incident angles where constructive interference happens.

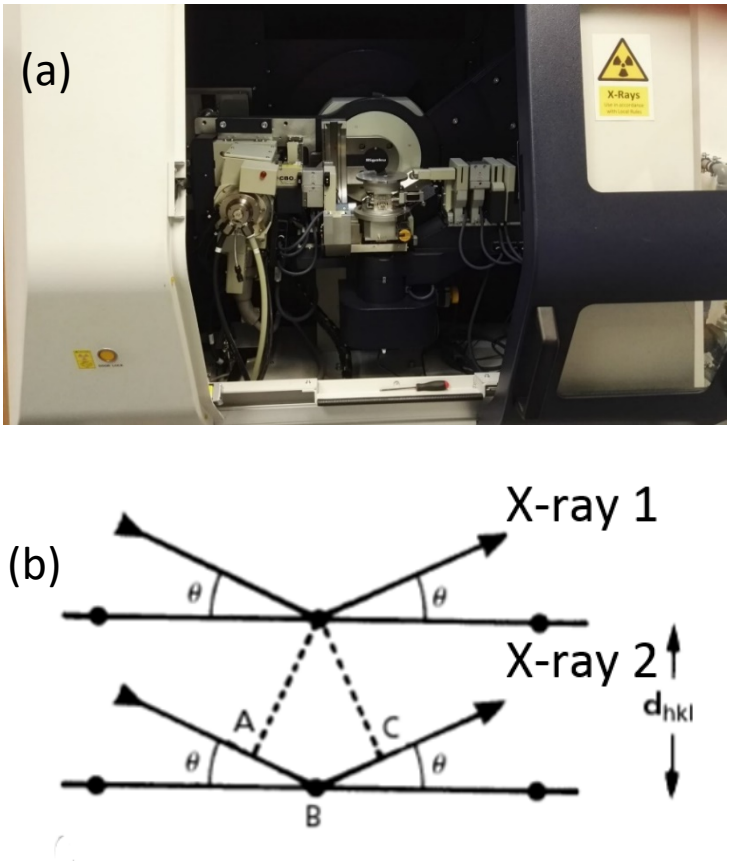


Figure 3-10. (a) Rigaku Smartlab® XRD system. (b) Schematic of X-ray diffraction. [128].

The measured XRD spectrum of a-SiC:Cu and c-SiC thin films were compared with the XRD spectrum of SiC thin films in the literature. XRD peaks near 35.7^{o} and 41.5^{o} correspond to SiC (111) [129] and SiC (200) [109, 130], respectively, are usually observed from the XRD spectrum of crystalline SiC in the literature. XRD spectrum of a-SiC in the literature usually shows no such diffraction peak corresponding to SiC crystal plane [10].

3.2.3 Transmission electron microscopy

Transmission electron microscope (TEM) has been used to observe the microstructure of a-SiC:Cu thin films. Figure 3-11 shows the Jeol JEM 3010 transmission electron microscope (TEM) which was used in the observation. The TEM observation was done together with Dr. Shuncai Wang. The electron gun on the top of the TEM emits electrons with high kinetic energy downwards to the sample. The condenser lens below the electron gun condense the electrons into a radially symmetrical electron bean using an electromagnetic field. The condenser aperture between the condenser lenses controls the size of the electron beam which is projected downwards to the sample. The smaller the size of the beam the higher the resolution of the TEM image but the lower the signal intensity hence low signal to noise ratio. The electron beam gets scattered when passing through the sample which is on the sample holder below the condenser lens. The scattering of the electrons by the atoms in the sample forms the TEM image and the diffraction of the electrons from the crystal lattice planes in the sample forms the diffraction image. The objective aperture below the sample holder allows electrons that have been diffracted to a specific angle to pass to adjust the contrast of the image. The objective lens focuses the image using an electromagnetic field and also initially magnify the image. Selected area aperture below the objective lens is used to choose to project either TEM image or diffraction image on the screen. Projector lens below the selected area aperture magnifies the image. Finally, the magnified image is either projected on to a fluorescent screen which can be viewed by eyes directly.

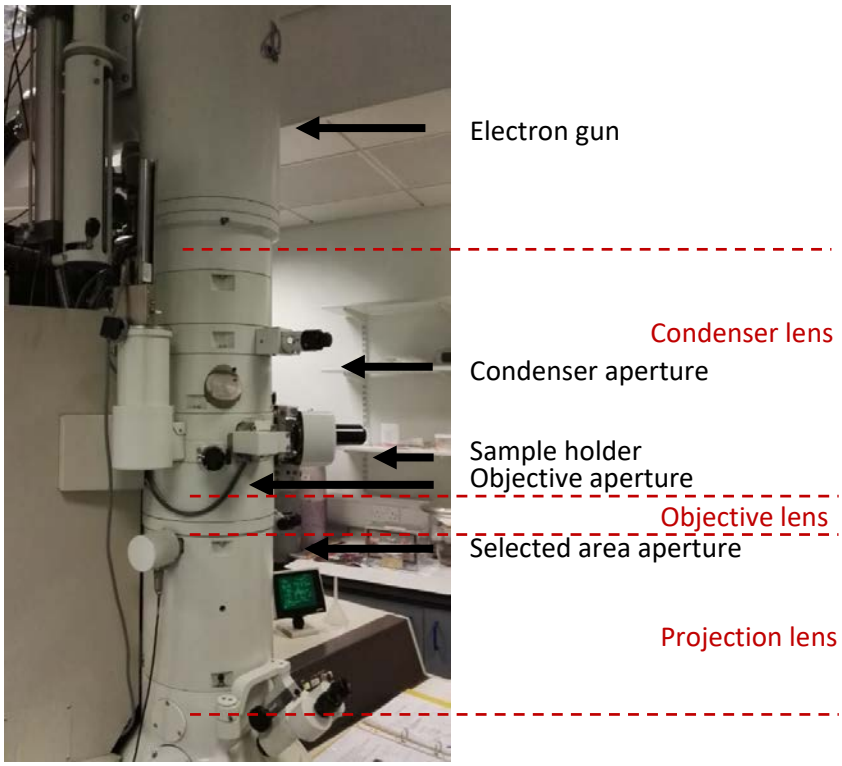


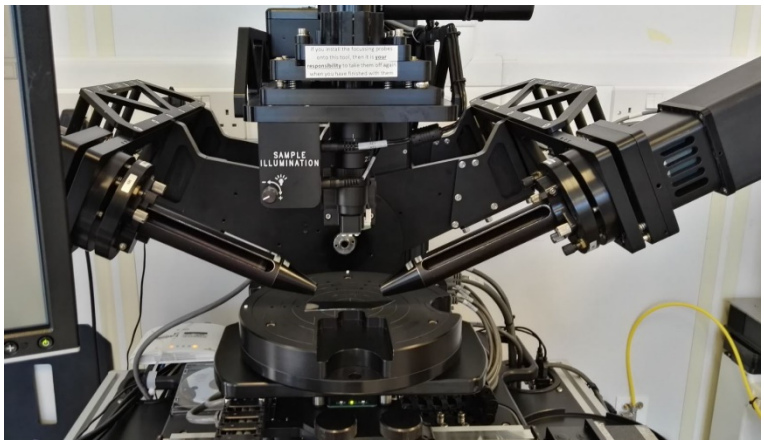
Figure 3-11. Jeol JEM 3010 TEM in the University of Southampton.

The TEM samples were prepared by scratching a-SiC:Cu thin films using a razor blade. The a-SiC:Cu powders scratched off from the a-SiC:Cu thin films were caught on the Cu grids. Bright-field images of a-SiC:Cu samples were taken at 300K to 400K magnification. Also, Selected area electron diffraction (SEAD) images and EDX spectrum of the a-SiC:Cu samples were measured.

3.2.4 Variable angle spectroscopic ellipsometry

Variable angle spectroscopic ellipsometry (VASE) measurements have been conducted on a-SiC, a-Si(O)C:H, and c-SiC thin films using a J.A. Woollam® M-2000® spectroscopic ellipsometer. Two incident angles 65° and 75° were used. Figure 3-12a shows a photo of the J.A. Woollam® M-2000® spectroscopic ellipsometer. In the VASE measurement, a linearly polarised light was projected onto the sample from the left side, as shown in Figure 3-12b. The light goes into the top of the sample for depth from a fraction of nanometres to a few tens of micrometres, depends on the wavelength of the light and the absorption coefficient of the film on the top. A detector on the right side measures the light reflected from the sample. The interactive with sample changes the polarisation of the reflected light. Refractive index n, extinction coefficient k, and thickness of materials on top of the sample can be estimated from the change of polarisation using suitable model.

(a)



(b)

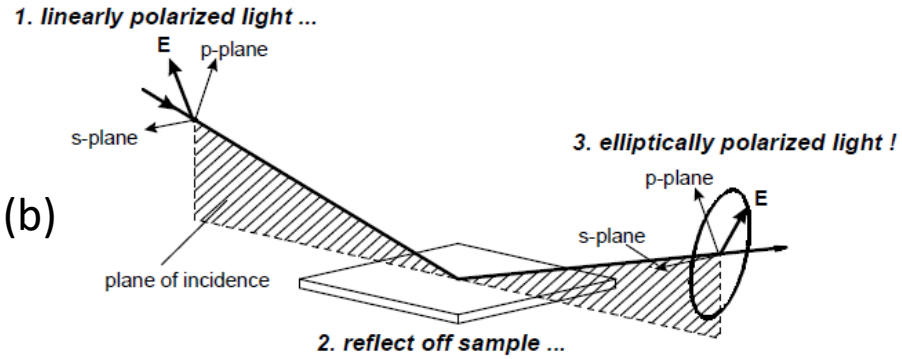


Figure 3-12. (a) J.A. Woollam® M-2000® spectroscopic ellipsometer. (b) Schematic of ellipsometry measurement [131].

In addition, the absorption coefficient α as a function of the energy E the incident light can be extracted from the modelling of VASE spectrum. The extracted α is also a function of the band gap E_g of the sample in the Tauc plot. For semiconductors that have an indirect band gap, the Tauc plot is described by Equation 3.3 [132],

$$\alpha hc/\lambda = \alpha E = B(E - E_g)^2, \tag{3.3}$$

where α is the absorption coefficient, h is Planck's constant, λ is the wavelength, c is the speed of light, and B is a constant. For semiconductors that have a direct band gap, the Tauc plot is described by Equation 3.4 [133],

$$\alpha E = A(E - E_g)^{1/2}, \tag{3.4}$$

where A is a constant. The band gap of the sample can be determined from the Tauc plot.

A variety of modelling schemes have been applied on the VASE spectra of a-SiC, a-Si(O)C:H, and c-SiC films to obtain the optimised modelling quality. A Cauchy model and a Tauc-Lorentz model have been applied to analyse the spectra of a-SiC films in the transparent (600 to 1200 nm) wavelength region and the entire wavelength spectrum (200 to 1600 nm), respectively. Thickness and refractive

index of a-SiC films was extracted using the Cauchy model, and the absorption coefficient was extracted using the Tauc-Lorentz model. Figure 3-13a and 3-13b show the simulated spectra of an a-SiC film using the Cauchy model and Tauc-Lorentz model, respectively. All the simulated spectra generally fit the measured spectra. Similarly, the VASE spectra of a-Si(O)C:H films and the c-SiC film were analysed using a Tauc-Lorentz model and a Cauchy model, respectively to achieve optimised modelling quality. Refractive index and absorption coefficient of the a-Si(O)C:H films were extracted using the Tauc-Lorentz model. Thickness and refractive index of the c-SiC film were extracted using the Cauchy model.

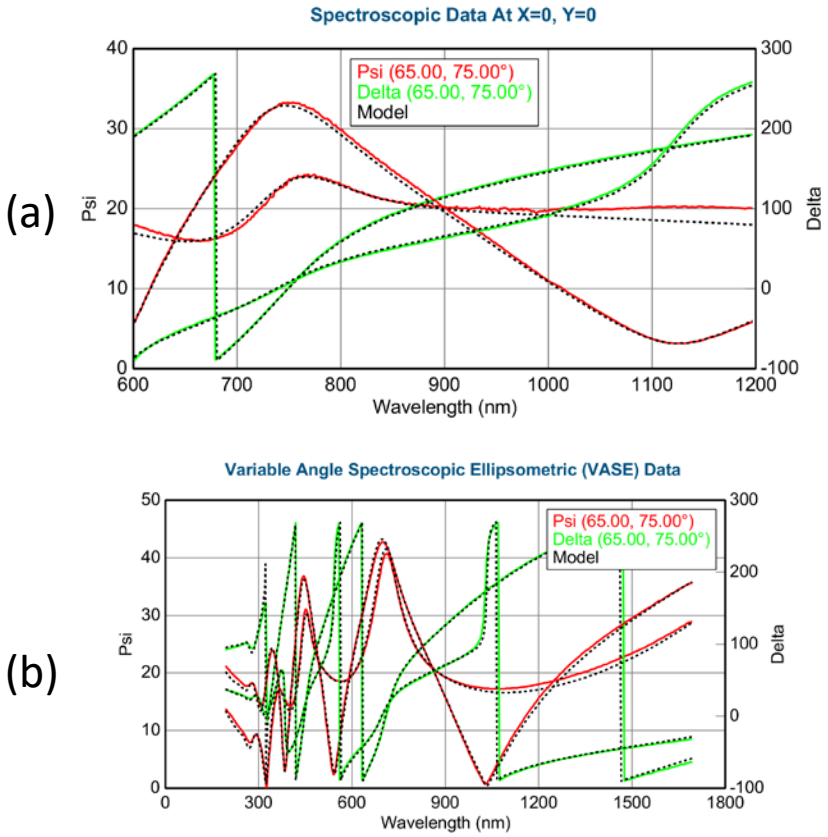


Figure 3-13. Measured VASE spectra of an a-SiC film on Si substrate, and the simulated spectra using (a) a Cauchy model and (b) a Tauc-Lorentz model.

3.2.5 X-ray Photo-electron spectroscopy

X-ray photoelectron spectroscopy (XPS) measurement was conducted on the a-SiC:H, a-SiCO:H, and a-SiOC:H thin films using a Theta probe XPS spectrometer, to investigate the chemical composition of these a-Si(O)C:H films. Figure 3-14a shows the measurement chamber of the Theta probe XPS spectrometer. The XPS measurement was done together with Dr. Ruomeng Huang. The basic operation principle of XPS measurement is introduced as follows.

In the XPS measurement, a monochromatic X-ray beam was projected onto the sample. Electrons were ejected from the core-level of the atoms in the sample near the surface due to X-ray bombarding. The electron ejected from an atom by interaction with a photon is known as a photoelectron. Figure 3-14b shows the schematic of the ejecting process of the photoelectron. Some of the photoelectrons were collected by the photoelectron analyser. The photoelectron analyser only allows photoelectrons with specific kinetic energy to be detected at a time and counts the number of electrons detected. Over time, the photoelectron analyser will scan the number of photoelectrons detected over a kinetic energy E_K spectrum. Binding energy E_B required to eject the photoelectron can be calculated using Equation 3.5,

$$E_B = h\nu - E_K - W, \tag{3.5}$$

where $h\nu$ is the energy of the X-ray, h is the Planck constant, ν is the frequency of the X-ray, and W is the work function of the XPS spectrometer. The obtained E_K spectrum is calculated into an E_B spectrum as shown in Figure 3-14c. The E_B spectrum is referred as the XPS spectrum in this thesis for simplicity. The value of E_B of a photoelectron is determined by the atomic structure of the element and the chemical bond. Hence, the position of peaks in XPS spectrum can be used to identify the chemical composition of the sample. Also, the concentration of the composition element in the sample can be calculated from the area of a peak correlate to the core-level of the composition element.

In the measurement of a non-conductive sample, electrons lost from the surface due to photoemission took a long time to be charged which makes the surface of the sample biased and shifts the XPS spectrum. To solve this problem, an electron flood gun was used in the measurement which continuously projects electron flood to the sample to compensate the emitted electrons and keep the charge neutrality of the sample. Also, an Ar ion gun can be used before the XPS scan starts, to sputter away the contamination on the sample surface or sputter away the sample surface for a depth profile measurement.

In the XPS measurement of a-Si(O)C:H thin films, the surface was first sputtered for 40 s to remove any contamination. The sputtering rate is approximately in the range 5 to 10 nm/min. Then, a survey XPS spectrum in -10 to 1350 eV was measured using a 0.5 eV resolution. Subsequently, the narrow scan in the range 90 to 115 eV, 274 to 303 eV, and 520 to 550 eV which corresponding to Si 2p, C 1s, and O 1s, respectively, were measured using a 0.1 eV resolution.

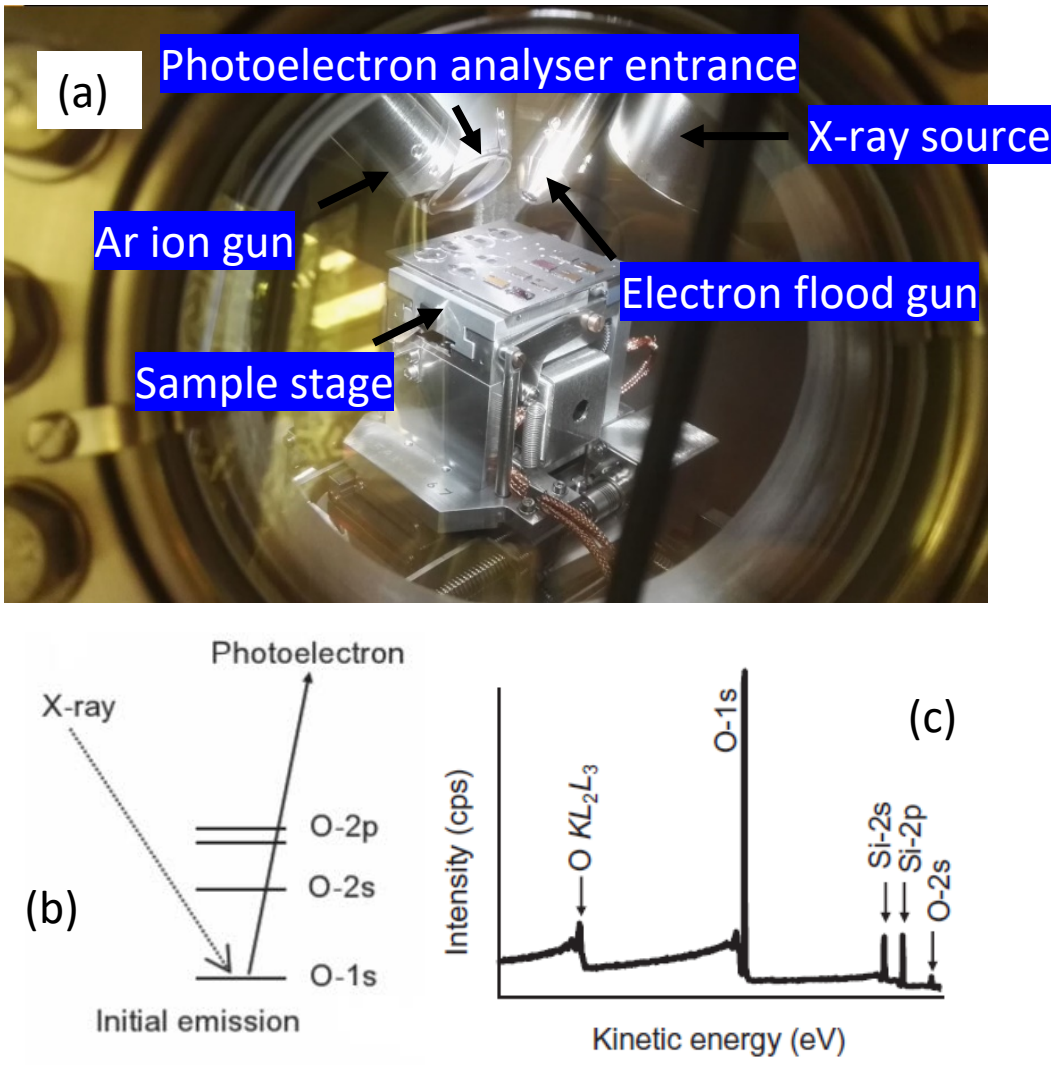


Figure 3-14. (a) Measurement chamber of the Theta Probe XPS spectrometer in the Southampton nanofabrication centre. (b) Photoelectron process and (c) XPS spectrum of a Silicon oxide thin film on Si wafer [134].

The measured XPS spectra of a-Si(O)C:H thin films were compared with the XPS spectra of SiC and a-Si(O)C:H reported in the literature. Three core-level spectra are important in the XPS analysis of SiC and a-Si(O)C:H thin films including Si 2p, C 1s, and O 1s. Figure 3-15a shows the Si 2p and C 1s spectra of an a-SiC:H film. In the Si 2p spectrum of crystalline SiC, a-SiC, and a-SiC:H, there is one main peak that is close to 100.2 eV corresponding to the Si-C bond [117, 135, 136]. Also, subpeaks near 99.5 eV correspond to Si-Si bond and near 102.8 eV corresponds to the presence of SiO_x contamination have been observed in the Si 2p spectra of SiC films in the literature. The O 1s peak near 532.2 eV corresponds to the SiO_x contamination on the SiC surface has been reported in the XPS spectra of these SiC films. The C 1s peak of crystalline SiC and a-SiC is usually composed by a peak near 283.0 eV corresponds to C-Si bond and another near 284.6 eV corresponds to C-C bond.

The structure of core-level peaks of a-SiCO:H and a-SiOC:H films is more complex. Figure 3-15b shows the Si 2p and C 1s spectra of an a-SiCO:H film. The Si 2p spectrum of a-SiCO:H and a-SiOC:H films is usually composed by multiple-peaks including Si-Si (99.2-99.5 eV), Si-C (100.3-100.7 eV), Si-O-C (101.8 eV), and Si-O (102.6-103 eV) [136]. The C 1s spectrum is usually composed by multiple-peaks including C-Si (283.2-283.6 eV) and C-C (284.6 eV). The O 1s spectrum is usually composed by multiple-peaks including O-Si (532.4 eV) and Si-O-Si (533.1 eV) [137].

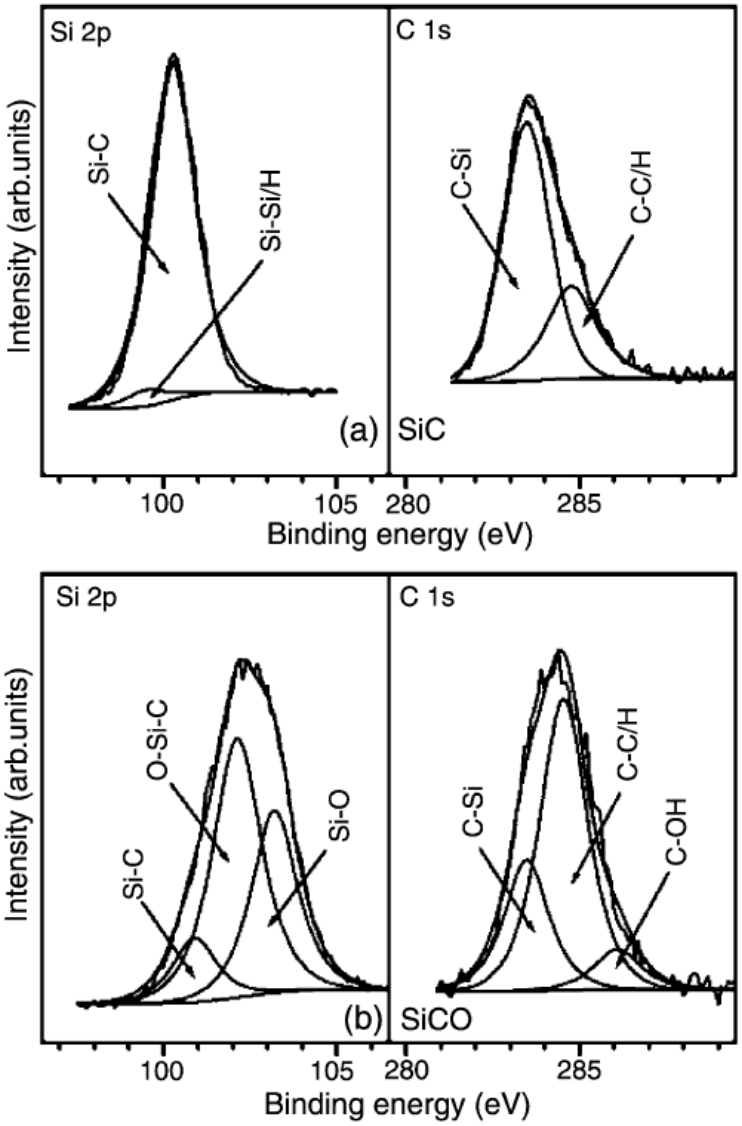


Figure 3-15. Narrow scans of Si 2p and C 1s XPS spectra for the (a) a-SiC:H and (b) a-SiCO:H films [136].

3.2.6 Schottky barrier assessment based on XPS measurement

Schottky barrier height (SBH) of a-Si(O)C:H/Cu Schottky contacts were estimated using XPS analysis [82, 123, 138]. Figure 3-16a shows the band alignment of an a-Si(O)C:H/Cu Schottky contact. In the equilibrium condition where the net current flow is zero, the Fermi level is flat at both the bulk of

a-Si(O)C:H and the a-Si(O)C:H/Cu interface. The energy difference between Fermi level and the valence band maximum E_v and the core-level E_{CL}, e.g. Si 2p, in the bulk of a-Si(O)C:H are $(E_v)_{bulk}$ and $(E_{CL})_{bulk}$, respectively. Both $(E_v)_{bulk}$ and $(E_{CL})_{bulk}$ can be measured from thick a-Si(O)C:H films using XPS measurement, as shown in Figure 3-16b. The thickness of the thick a-Si(O)C:H films should be >10 nm which makes the Schottky contact beneath the thick a-Si(O)C:H films out of the measurement depth of XPS, and <25 nm to avoid surface charge become significant [123]. The energy difference between Fermi level and the core-level at the a-Si(O)C:H/Cu interface is $(E_{CL})_{int}$ which can be measured from thin a-Si(O)C:H films on Cu substrate using XPS, as shown in Figure 3-16c. The thickness of the thin a-Si(O)C:H films should be less than the measurement depth of XPS, i.e. <10 nm, to enable the measurement of $(E_{CL})_{int}$ at the a-Si(O)C:H/Cu Schottky contact [123, 134], and >3 nm to let XPS measurement produce a stable output [123, 139]. The Φ_B for electron is the energy difference between the Fermi level and the conduction band minimum at the a-Si(O)C:H/Cu interface. The Φ_B for hole is the energy difference between the Fermi level and the valence band maximum at the a-Si(O)C:H/Cu interface. The Φ_B for electron and hole can be calculated using Equation 3.6 and 3.7, respectively [82],

$$\text{Electron } \Phi_B = E_g - (E_{CL})_{int} + (E_{CL} - E_v)_{bulk}, \tag{3.6}$$

$$\text{Hole } \Phi_B = (E_{CL})_{int} - (E_{CL} - E_v)_{bulk}, \tag{3.7}$$

where E_g is the band gap of the a-Si(O)C:H.

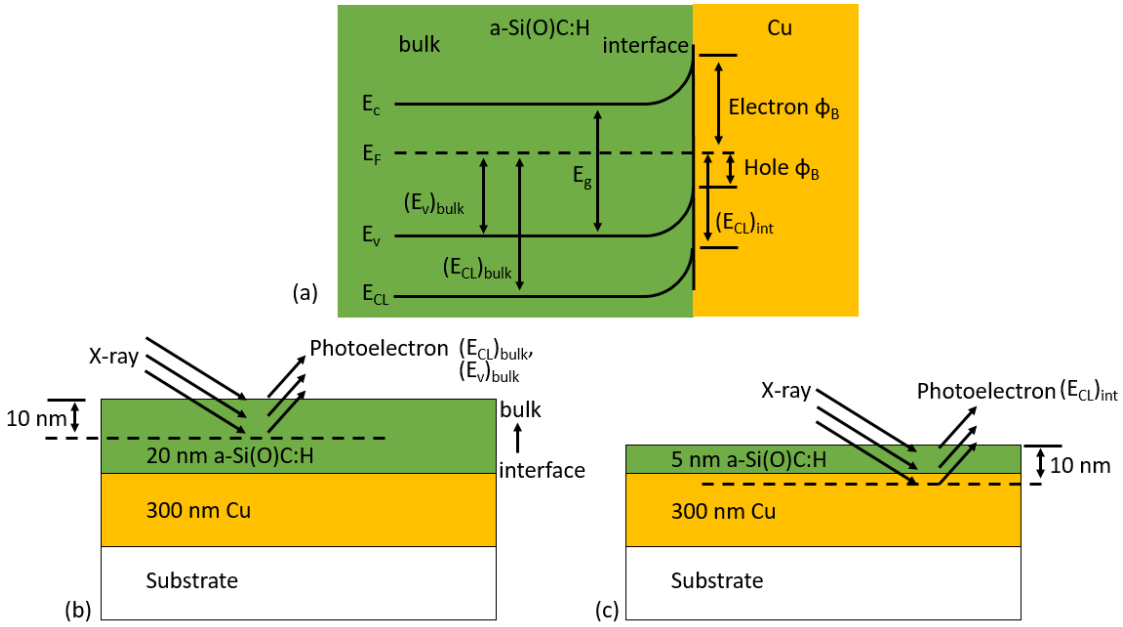


Figure 3-16. (a) Schematic of band alignment at a-Si(O)C:H/Cu interface. Schematics of (b) $(E_{CL})_{bulk}$ and $(E_v)_{bulk}$ measurements on 20 nm a-Si(O)C:H film and (c) $(E_{CL})_{int}$ measurement on 5 nm a-Si(O)C:H film.

E_g of a-Si(O)C:H films were obtained from the ellipsometry analysis of our a-Si(O)C:H films, as described in Chapter 3.2.4. $(E_v)_{bulk}$ and $(E_{CL})_{bulk}$ of a-Si(O)C:H films were extracted from the XPS survey spectrum of our a-Si(O)C:H films with 20 nm thickness. The XPS measurement was described in Chapter 3.2.5. $(E_v)_{bulk}$ was extracted from position where the photoemission reduced to zero in the XPS survey spectrum (0-20 eV). The Si 2p peak position was extracted from the XPS survey spectrum using a single Gaussian function, and was used as the $(E_{CL})_{bulk}$ in the calculation of SBHs. Si 2p position measured from a-Si(O)C:H films similar to our a-Si(O)C:H films, with 5 nm thickness on Cu coated substrates in the literature was used as the $(E_{CL})_{int}$ in the calculation of SBHs.

3.2.7 Fourier transform infrared spectroscopy

Fourier transform infrared (FTIR) spectroscopy measurement has been conducted on a-SiC thin films to investigate the bonding structure of the a-SiC films. The basic principle of FTIR measurement is introduced as follows. Figure 3-17 shows the schematic of transmission mode measurement in an FTIR spectrometer. An infrared (IR) source emits broadband IR light toward the Michelson interferometer in the FTIR spectrometer. The IR light passes through the Michelson interferometer is "encoded" with an interferogram signal which is a function of time and can be used later to calculate the IR spectrum. Then, the IR light contains the interferogram signal passes through the sample. Part of the IR light was absorbed by the sample, and the rest IR light that passes through the sample carries the IR absorption information. Next, the detector measures the intensity of this IR light passes through the sample to obtain the interferogram. In the end, the computer calculated the interferogram into an IR spectrum using Fourier transform. The advantages of FTIR spectrometer compare with the monochromatic spectrometer include higher measurement speed because the spectrum was measured simultaneously, and higher signal-noise ratio because the optical throughput is high. Figure 3-18 shows an FTIR spectrum of an a-SiC:H in the literature [122]. The absorbance of IR with a certain wavelength is noticeably higher because molecules absorb IR with a certain frequency (c/wavelength, c is the speed of light) matches their vibrational frequency. The absorption peaks in the FTIR spectrum correspond to a specific vibration mode of a particular molecule. For example, IR absorption peaks at 790 cm^{-1} and 1330 cm^{-1} correspond to the stretching vibration of Si-C and scissoring vibration of Si-CH_2-Si, respectively [122]. Hence, it is possible to exploit the FTIR spectrum to study the bonding structure of a-SiC:H films.

The a-SiC thin films on Si substrates were sent to Intel® for the FTIR measurement. FTIR spectra of a-SiC thin films on Si substrate were measured in the transmission mode. Also, a background subtraction process has been performed by Intel to the raw spectra.

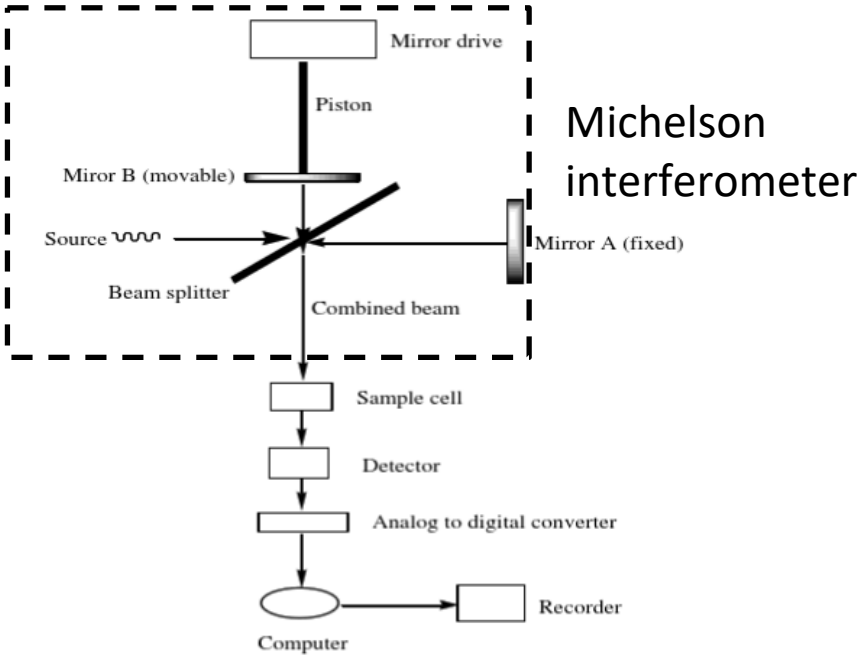


Figure 3-17. Schematic of transmission mode measurement in an FTIR spectrometer. [140]

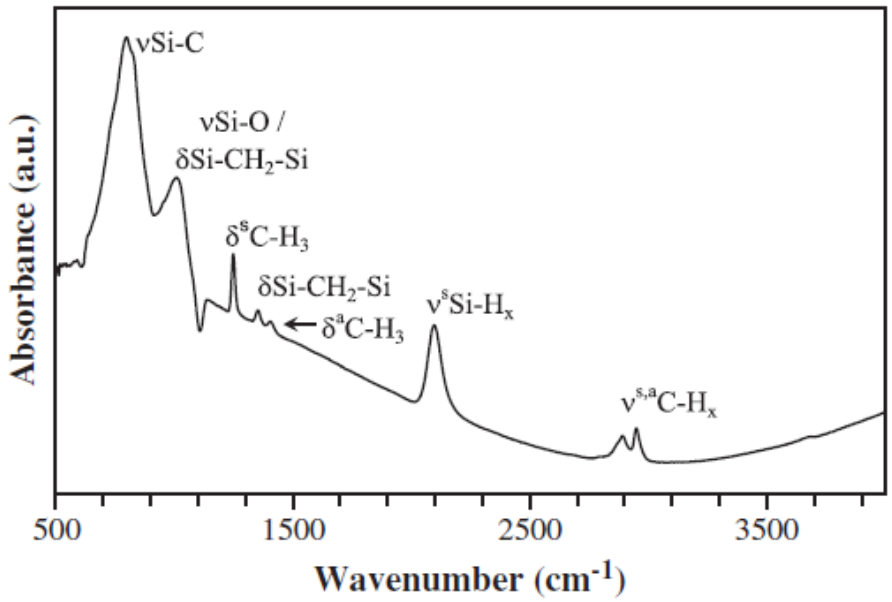


Figure 3-18. FTIR spectrum of an a-SiC:H thin film [122].

3.2.8 Nuclear reaction analysis and Rutherford backscattering

Nuclear reaction analysis (NRA) and Rutherford backscattering (RBS) measurements have been conducted on the a-SiC thin films the measure their chemical composition. The a-SiC thin films were sent to the University of Albany for the NRA and RBS measurements. The concentration of the H, C, and O contents in the a-SiC thin films was determined using NRA. The concentration of the Si content in the a-SiC thin films was determined using RBS.

3.2.9 Van der Pauw measurement

Van der Pauw measurement has been conducted on a-SiC and a-SiC:Cu thin films using an HL5500PC® Hall effect system was used in the measurements, as shown in Figure 3-19. The system can measure sheet resistance up to 10^{11} Ohm/□, in theory. The measurement of a-SiC:Cu thin films was done by Dr. Le Zhong. Figure 3-20 shows the schematics of Van der Pauw measurement. Four probes were positioned on the four corners of the sample in the measurement, which were named as contact A, B, C, and D. Current-voltage characteristics of the sample were measured twice using two contact configurations. In the first measurement, a current I_{CD} was applied between contacts C and D, and the voltage V_{AB} between contacts A and B was measured, as shown in Figure 3-20a. In the second measurement, a current I_{DA} was applied between contacts D and A, and the voltage V_{BC} between contacts B and C was measured, as shown in Figure 3-20b. The resistivity of the sample could be calculated using Equation 3.8 [141],

$$\rho = 2.2662 d_{surface} (\frac{V_{AB}}{I_{CD}} + \frac{V_{BC}}{I_{DA}}) F(Q), \tag{3.8}$$

where $d_{surface}$ is the depth of the sample surface where the current went through, F is a correction factor and is a function of Q. Q is the symmetry factor and can be calculated using Equation 3.9,

$$Q = \frac{V_{AB} I_{DA}}{I_{CD} V_{BC}}, \tag{3.9}$$

or using the reciprocal of Equation 3.9, whichever has the result greater than 1. When 1<Q<10, F could be estimated using Equation 3.10 [141],

$$F = 1 - 0.34657 \left[\frac{Q-1}{Q+1}\right]^2 - 0.09236 [\frac{Q-1}{Q+1}]^4 \tag{3.10}$$

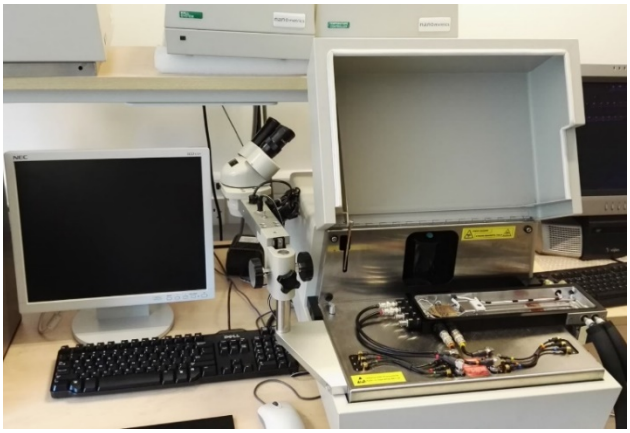


Figure 3-19. HL5500PC® Hall effect system.

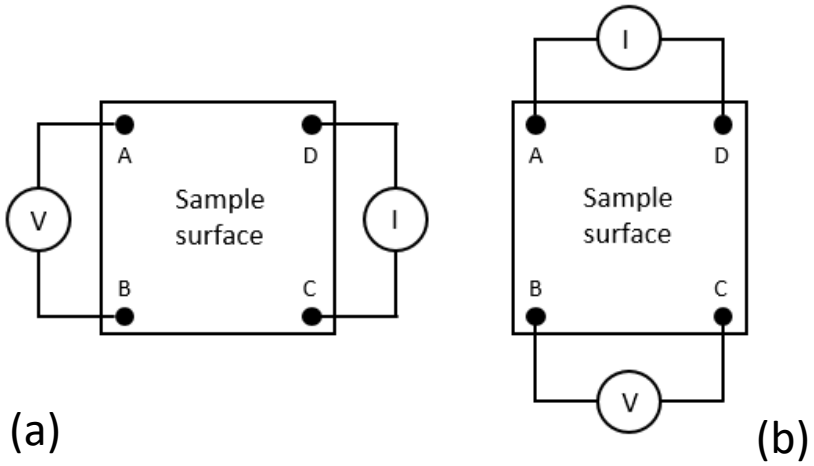


Figure 3-20. Van der Pauw measurements. (a) I_{DC}-V_{AB}. (b) I_{AD}-V_{BC}.

3.2.10 Resistance measurement at low temperature

The resistance of a-SiC:Cu films at 140 K to 300 K, was measured using a LakeShore® EMTTP4 cryogenic probe station. The measurement was done by Dr. Le Zhong. In the measurement, two probe was applied on the surface of a-SiC:Cu films. A 3 V voltage V was applied on the a-SiC:Cu film between the two probe and the current I pass through was measured. Resistance R=V/I was normalised with the resistance at 300 K R_{300K}, to make the comparison between a-SiC:Cu films easier.

3.2.11 Four-point-probe measurement

Four-point-probe measurement has been conducted on a-SiC and a-Si(O)C:H films using a Janel RM3® four-point-probe system as shown in Figure 3-21a. The system can measure sheet resistance <6.34×10^7 Ohm/□, in theory. In the measurement, four probes in a line were placed on the surface of the sample, as shown in Figure 3-21b. The space (S) between probes is the same. A current I was applied between the two probes on the side, and the voltage V between the two probes in the centre was measured. When the diameter of the sample is much larger than S, the sheet resistance R_{sheet} of the sample surface can be calculated using Equation 3.11,

$$R_{sheet} = 4.53V/I, \tag{3.11}$$

The resistivity ρ of the sample surface can be calculated using Equation 3.12,

$$\rho = R_{sheet} d_{surface}, \tag{3.12}$$

In order get an accurate measurement, the substrate should have much higher resistivity than the thin film on top.

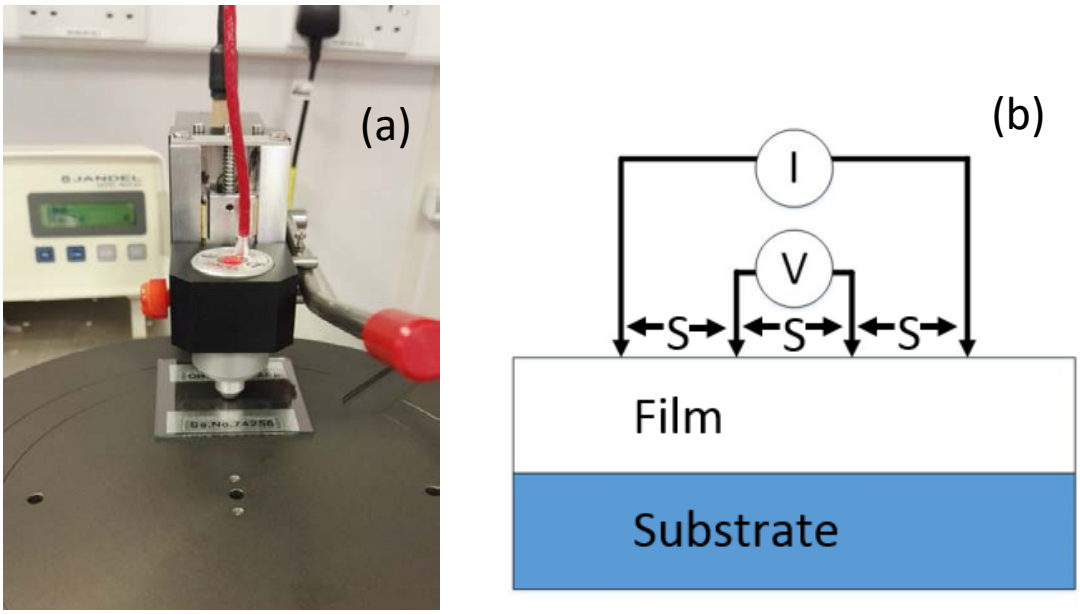


Figure 3-21. (a) Janel RM3® four-point-probe system. (b) Schematic of four-point-probe measurement.

3.3 Methods for electrical measurements

3.3.1 Capacitance-voltage measurement

Capacitance-voltage (C-V) measurement has been conducted on pristine a-SiC, a-SiC:Cu, and a-Si(O)C:H resistive memories using an HP 4279 1 MHz C-V meter. Figure 3-22a shows the 4279 C-V meter. For the record, C-V measurement of the a-SiC:Cu resistive memories was done by Dr. Le Zhong. The rest C-V measurements were done by the author himself. Schematic of the C-V measurement is shown in Figure 3-22b. All the pristine a-SiC, a-SiC:Cu, and a-Si(O)C:H resistive memories have a Metal/Insulator/Metal (MIM) device structure the same as a parallel plate capacitor. The device chip of resistive memory was placed on the sample stage in a probe station. The probe station has an optical microscope which can be used to precisely positioning the probes on the resistive memory. High current (HCUR) and High potential (HPOT) terminals were connected to one metal electrode the low current (LCUR) and low potential (LPOT) terminals were connected to the other metal electrode. An alternating current (AC) voltage signal at 1 MHz was supplied by the HCUR. The current I_{MIN} went through the MIM device structure was measured by the LCUR, and the voltage V_{MIM} across the MIM was measured by the HPOT and LPOT. Amplitude and phase angle of I_{MIN} and V_{MIM} were obtained in the measurement and capacitance of the MIM device structure can be calculated [142].

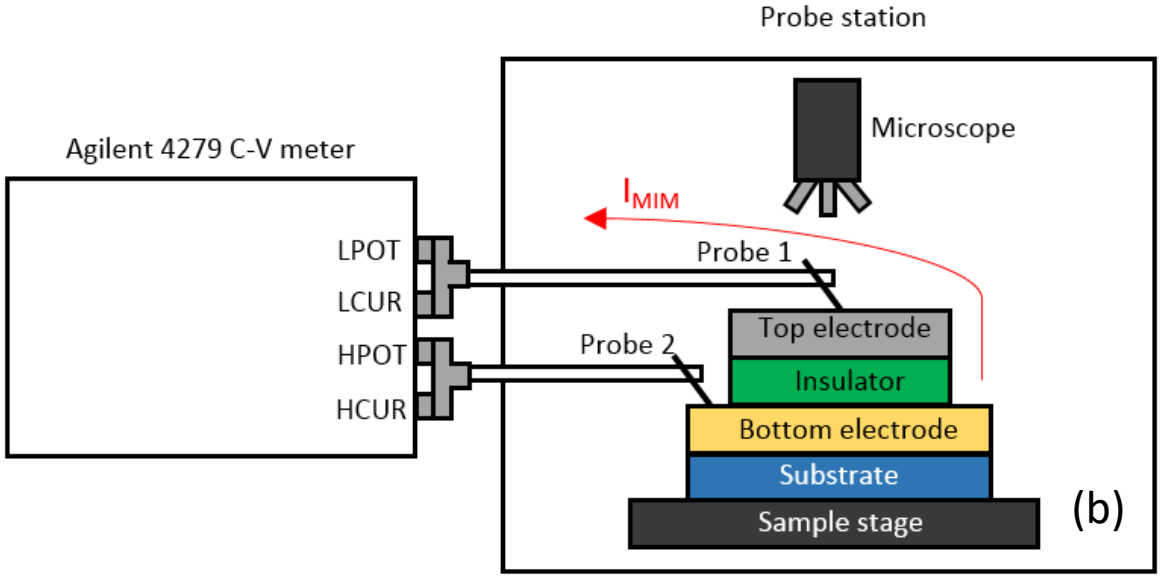


Figure 3-22. (a) HP 4279 C-V meter. (b) Schematic of C-V measurement.

3.3.2 Current-voltage measurement

Current-voltage (I-V) measurement has been conducted on a-SiC, a-SiC:Cu, a-Si(O)C:H, and c-SiC resistive memories, using semiconductor parameter analysers including Agilent B1500A, Keithley 4200SCS, and Agilent 4155C. I-V measurements were conducted in DC and Pulse modes. Agilent B1500A, Keithley 4200SCS, and Agilent 4155 all have four SMUs which can perform both DC and pulsed measurements. Figure 3-23 shows the schematic of I-V measurements. A pair of Source and measurement units (SMUs) of a parameter analyser were used in the I-V measurement. A voltage signal was applied by the SMU1 to the top electrode of the resistive memory, and the bottom electrode was grounded (GND) by the SMU2. The current went through the resistive memory was measured from the top electrode as it has the same polarity as the voltage applied.

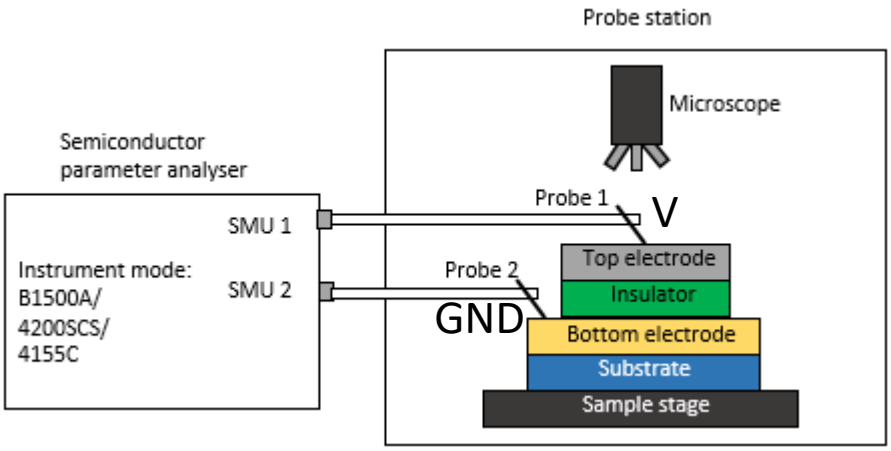


Figure 3-23. Schematic of I-V measurement.

In the DC mode, a voltage was continuously applied to the device under test, as shown in Figure 3-24a. The amplitude of the voltage increased step by step. In each step, the voltage increases V_{step} and the SMU starts to measure the current after a delay in which the I-V characteristics became stable. The DC mode is very useful in the study of resistive-switching characteristics because it provides the "real-time" monitoring of the resistive-switching I-V characteristics. However, investigating of resistive-switching characteristics in pulse mode is required because pulse signal instead of DC signal is used in the operation of commercial memory products.

In pulse mode, a set of voltage pulse was applied to the device under test, as shown in Figure 3-24b. A very short pulse width is usually required for the pulsed measurement to test the maximum switching speed. For example, 500 nm pulse has been applied to switch Cu/a-SiC/Pt resistive memories [47]. Hence it is impossible to monitor the "real-time" resistive-switching characteristics in pulse mode. Also, the current measurement resolution in pulse mode is usually much worse than DC mode due to the short pulse width.

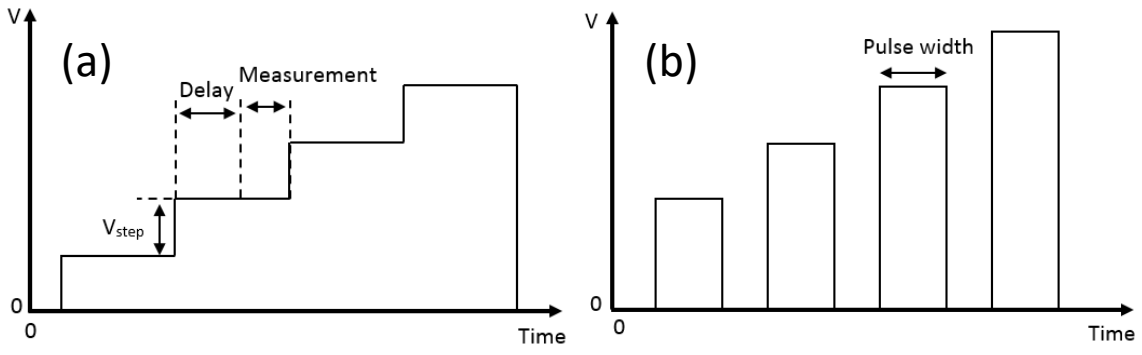


Figure 3-24. Schematics of I-V measurement in (a) DC and (b) pulse modes.

Figure 3-25a shows the Agilent B1500A which has been used to measure resistive-switching characteristics of a-SiC resistive memories in DC and pulse modes. It has also been used to measure the pristine state I-V of a-SiC:Cu resistive memories. The B1500A has high current measurement

resolution near 1 pA which is suitable for measurement of a device with ultra-high resistance such as a-SiC resistive memories. Figure 3-25b shows the Keighley 4200SCS which has been used to measure resistive-switching characteristics of a-SiC and a-SiC:Cu resistive memories in DC and pulse modes. Also a preliminary test on a-SiC:H resistive memory has been conducted using the pulse module of the 4200SCS. The 4200SCS is a versatile equipment which has both SMUs and a high-speed pulse module. Also, it has powerful programming ability which allows the user to arrange a set of measurements in a sequence which was found very helpful in the measurement of a-SiC:Cu resistive memories. Figure 3-25c shows the Agilent 4155C which has been used to measure the pristine state I-V characteristics and resistive-switching characteristics of a-Si(O)C:H and c-SiC resistive memories in DC mode. The 4155C is also very good at current measurement resolution same as B1500A, which is needed for the measurement of a-Si(O)C:H resistive memories. In the meantime, 4155C is attached to the 4279 C-V meter which makes the performing of C-V and I-V measurements in sequence on a-Si(O)C:H resistive memories very convenient. For the record, the DC I-V measurement of Cu/a-SiC/W resistive memories were done by Mr. Robert Gowers and Dr. Katrina Morgan. The pulsed I-V measurement of Cu/a-SiC/Au resistive memories were done by Dr. Katrina Morgan.

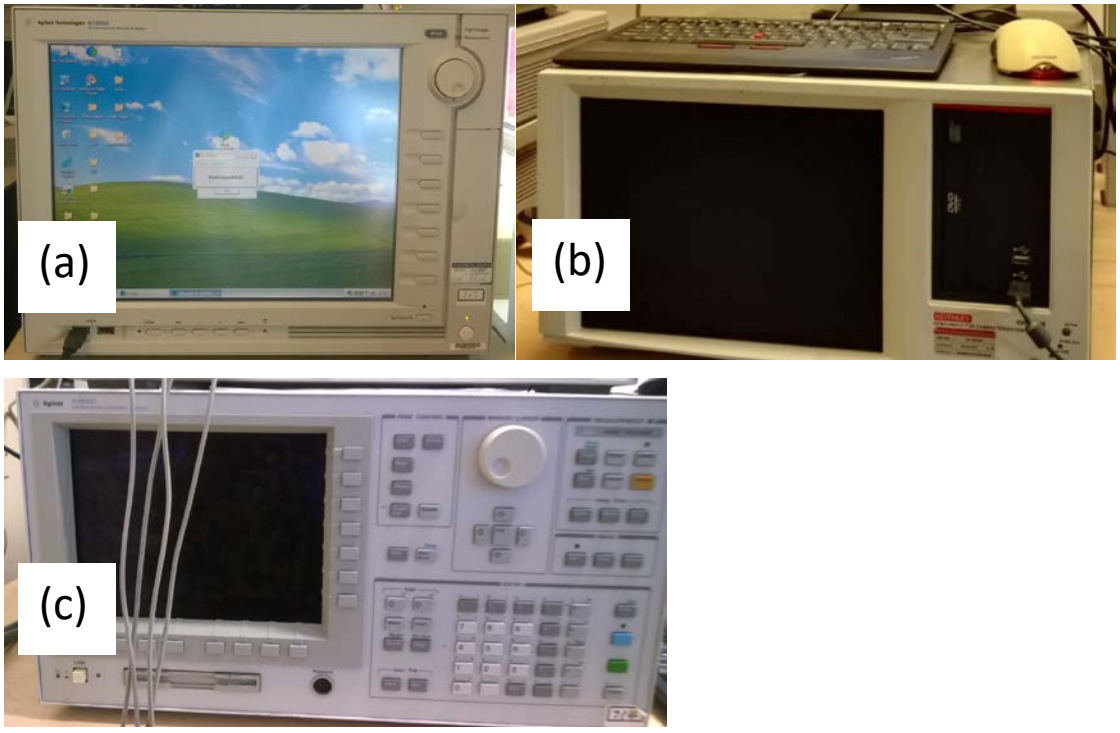


Figure 3-25. (a) B1500A, (b) 4200SCS, and (c) 4155C.

Chapter 4: Amorphous SiC films and RMs

Amorphous SiC has shown significant application potentials in ECM resistive memories. The ECM resistive memories that have amorphous SiC (a-SiC) as the insulator layer, have shown excellent retention and stabilities [11, 47], ultra-high ON/OFF ratio in the range 10^8 to 10^9 [9]. In ECM, the resistive-switching behaviour is governed by the formation and dissolution of metal filaments inside the insulator layer [46, 63]. Hence the properties of the materials used as the insulator layer play an important role in determining the resistive-switching behaviour of the resistive memories. Although basic studies on the material properties of RF sputtered a-SiC, including chemical composition, amorphous microstructure, dielectric constant has been conducted [9-11, 46], properties such as refractive index, band gap, mass density, and bonding structure remaining missing.

Integrating memories in CMOS BEOL is considered as a desired architecture to reduce interconnect latency [7] and achieve high storage density [143]. Considering the fabrication cost resistive memories that can be fabricated using standard materials and processes of CMOS BEOL fabrication, would intuitively become extremely attractive. Although most a-SiC resistive memories reported use Cu as the active electrode which is commonly used in the BEOL, Pt [11, 47], and Au [9, 10, 46, 144] which are not commonly used in the BEOL was used as the inert electrode.

In this chapter, the material properties of a-SiC films sputtered using different sputtering conduction were measured to investigate the effect of the sputtering condition of material properties of the a-SiC films. Knowing the influence of sputtering condition on the material properties of a-SiC films can enable the controlled deposition of a-SiC films with optimised material properties for resistive memory and other applications. In addition, resistive-switching of Cu/a-SiC/W resistive memories that replaced Au which is not a native BEOL metal to a native BEOL metal, i.e. W. The compatibility of the a-SiC insulating layer with Cu and W which are native BEOL metals simultaneously shows great embedding potential of Cu/a-SiC/W resistive memory in the BEOL layer.

4.1 Thickness, refractive index, and band gap of amorphous SiC films

Variable angle spectroscopic ellipsometry (VASE) measurement was conducted on the RF sputtered a-SiC films on Si substrates and Si substrates coated with 2 µm SiO_2 (SiO_2/Si). Thickness and refractive index of a-SiC films were extracted from the modelling of VASE spectra using a Cauchy model to investigate the influence of sputtering condition on the material properties of the a-SiC

films. The deposition rate can be used to control the deposition of a-SiC with a designed thickness in the fabrication of a-SiC resistive memory. The refractive index can be used to estimate the microstructure and dielectric constant of the a-SiC films. Thickness, deposition rate, and refractive index at the wavelength of 673 nm of RF sputtered a-SiC films were summarised in Table 4-1. The value of refractive index is a function of wavelength. The 673 nm wavelength selected here is commonly used in the literature. All the refractive index of a-SiC films in this thesis refer to refractive index at 673 nm.

Table 4-1. Thickness, deposition rate, and refractive index of a-SiC films.

Sample name	a-SiC thickness (nm)	a-SiC deposition rate (nm/min)	Refractive index
A	249.8 ±1.0	3.6	2.3
B	287.9 ±0.3	4.1	2.2
C	236.4 ±0.7	3.4	2.5
D	274.4 ±0.4	3.9	2.4
E	258.1 ±2.5	5.2	2.1
F	274.3 ±1.5	5.5	2.3
G	333.4 ±0.1	2.9	1.8
H	341.6 ±0.5	3.0	1.8
I	306.3 ±0.3	3.4	1.8
J	308.1 ±2.1	3.4	1.9
K	376.4 ±1.2	3.6	1.8
L	392.3 ±2.3	3.7	1.8
M	330.2 ±1.7	2.8	1.9
N	345.4 ±0.9	2.9	1.9
Q	299.8 ±0.2	4.3	2.0
S	294.5 ±1.9	4.2	2.0

Figure 4-1a shows the deposition rate of a-SiC films as a function of SiC target power. An increase of deposition rate with SiC target power was clearly observed. This is attributed to the increase of the kinetic energy of the Ar plasma, which produced a higher sputtering yield. Figure 4-1b shows the deposition rate of a-SiC films as a function of Ar gas pressure. The deposition rate of a-SiC films RF sputtered at 5×10^{-3} mBar Ar gas pressure environment is noticeably higher than a-SiC films RF sputtered at higher Ar gas pressure environment. This is attributed to the increase of collisions between the SiC particles sputtered from the SiC target, and Ar gas atoms, before arriving at the

sample surface. The mean free path of sputtered species decreases with increased Ar gas pressure [145, 146].

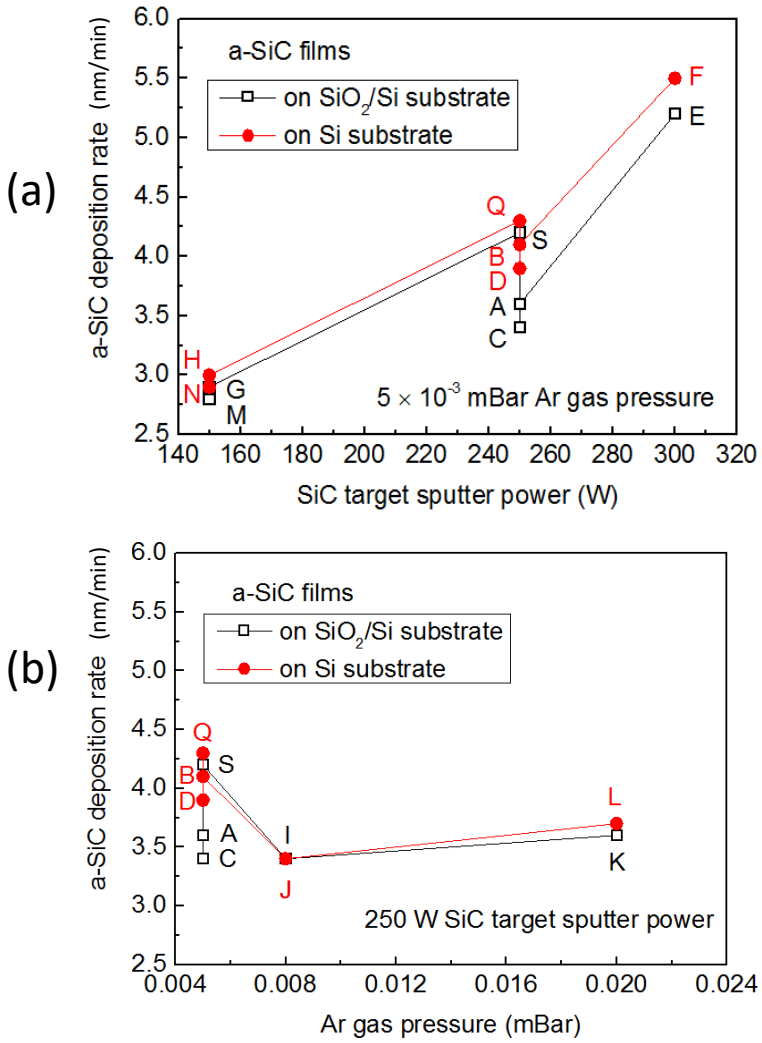


Figure 4-1. The deposition rate of a-SiC films RF sputtered using (a) 5×10^{-3} mBar Ar gas pressure and 150 to 300 W SiC target power, and using (b) 250 W SiC target power and 5×10^{-3} to 20×10^{-3} mBar Ar gas pressure.

The refractive index of the a-SiC films with their corresponding RF sputtering condition was plotted in Figure 4-2. The refractive index is higher for a-SiC films sputtered using higher 250 to 300 W SiC target power but with large variation, as shown in Figure 4-2a. The variation is likely caused by the thermal conduction of the SiC target, which varies with the consumption of the SiC target from run to run. The actual values are not far from the refractive index of cubic SiC in the literature [112].

Figure 4-2b shows the refractive as a function of Ar gas pressure. A reduction of the refractive index with increasing Ar gas pressure was observed. In lower Ar gas pressure, the sputtered SiC particles have relatively lower chance to collide with Ar gas atoms in the chamber. As a result, the sputtered SiC particles arrived at the substrate with less energy loss in collisions with Ar gas atoms, which is

known as the thermallisation [126]. The sputtered SiC particles with higher energy will knock out loosely bound atoms on the substrates, including film-forming atoms as well as unwanted impurities, improving adhesion and making the film denser [126]. It is known that refractive index depends on film density [132]. Increase of refractive index with increased mass density of films has widely been reported in the literature [147-149].

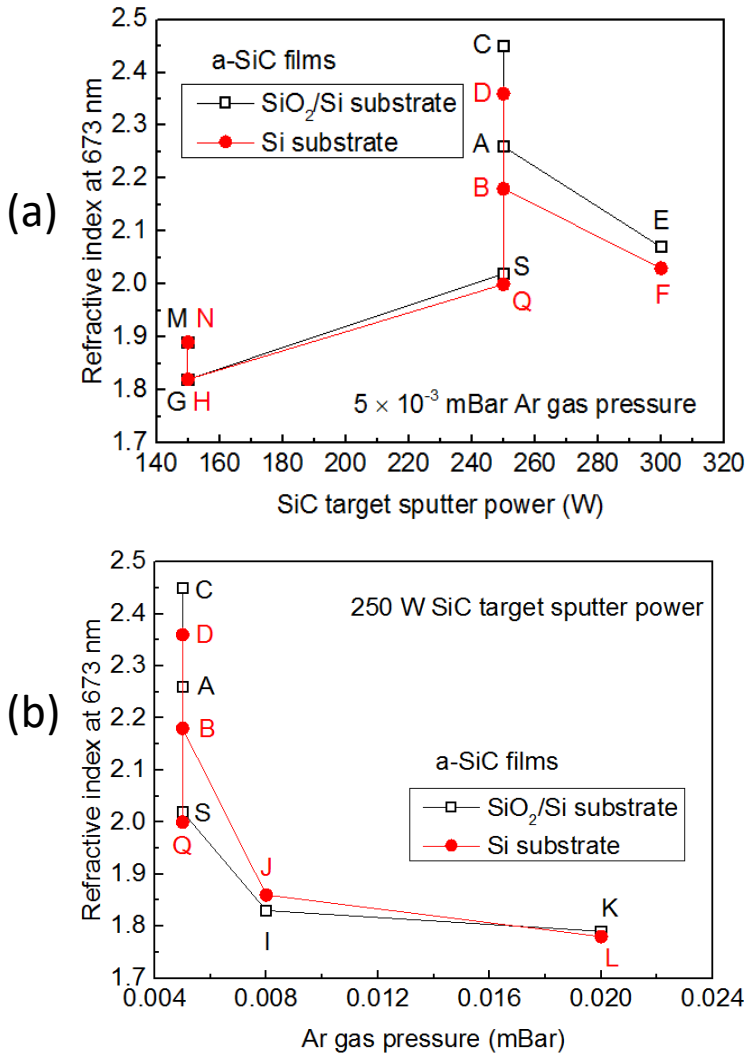


Figure 4-2. Refractive index of a-SiC films RF sputtered using (a) 5 × 10^{-3} mBar Ar gas pressure and 150 to 300 W SiC target power, and using (b) 250 W SiC target power and 5 × 10^{-3} to 20 × 10^{-3} mBar Ar gas pressure.

The absorption coefficient of a-SiC films as a function of energy was extracted from VASE spectra using a Tauc-Lorentz model, as described in Chapter 3.2.4. Figure 4-3a and 4-3b show the same set of absorption coefficient data of the a-SiC films plotted in the Tauc plots for indirect band gap and direct band gap, respectively. The band gap E_g was determined by extrapolating the linear part to αE=0 in the Tauc plots, as shown in Figure 4-3. The E_g of a-SiC film, extracted from the Tauc plot of the indirect and direct band gap is around 2.2 to 3.3 eV and 4.9 to 5.6 eV, respectively. Although

both the Tauc plots of the indirect and direct band gap show linear behaviour near the edge of absorption, the values of E_g extracted from the Tauc plots of the indirect band gap are closer to E_g 2.2 to 2.9 eV of SiC in the literature [89, 150]. This is expected because SiC was known as a typical indirect band gap semiconductor [89]. Hence, the E_g of the a-SiC films extracted from the Tauc plot of the indirect band gap is more likely to be the correct one. The extracted E_g of the a-SiC films could potentially be used to estimate the Schottky barrier height at the a-SiC/metal Schottky contacts. Higher E_g is likely to lead to higher SBH at the a-SiC/metal Schottky contacts because the metal Fermi level is usually pinned around the middle of the band gap of a-SiC due to the existing of surface states.

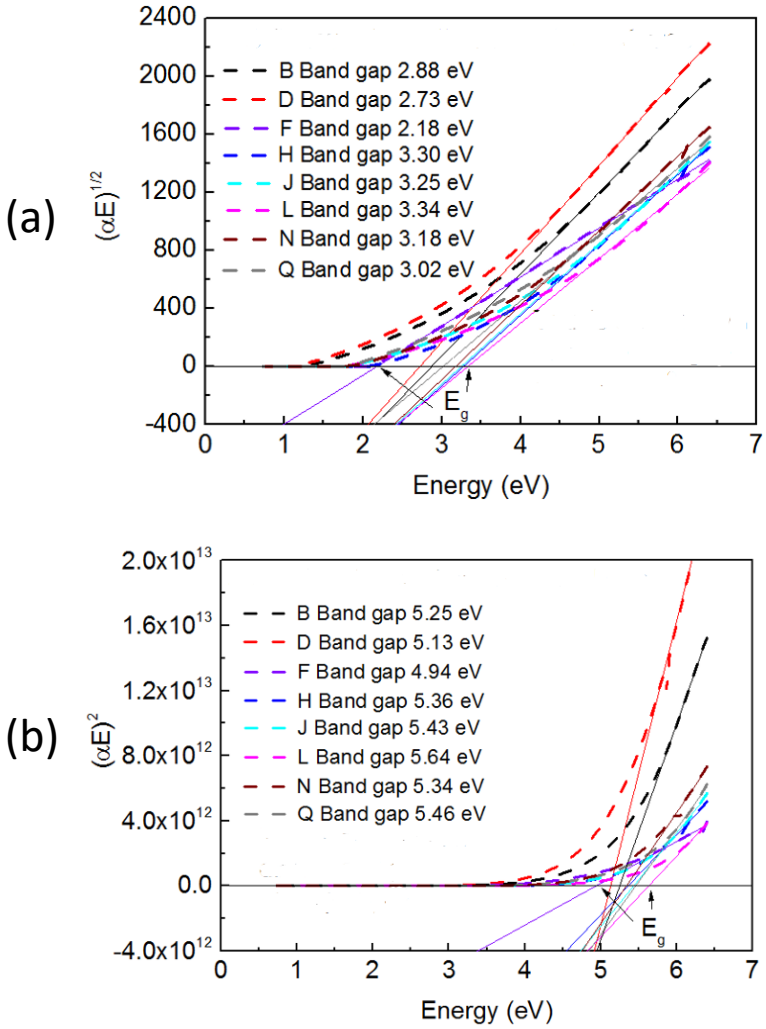


Figure 4-3. (a) Indirect band gap and (b) Direct band gap Tauc plots for RF sputtered a-SiC films on Si substrates, with respective linear fits.

The effect of RF sputtering condition on a-SiC band gap was investigated. The band gap of a-SiC films with their corresponding sputtering condition were plotted in Figure 4-4. A-SiC films sputtered using higher SiC target pressure have a noticeably lower band gap. A-SiC films sputtered using higher Ar gas pressure have a noticeably higher band gap. The origin of the dependence of a-SiC

band gap with SiC target power and Ar gas pressure used in the RF sputtering processes is not clear. It is likely that different sputtering condition leads to the different microstructure of a-SiC films which affects the band gap.

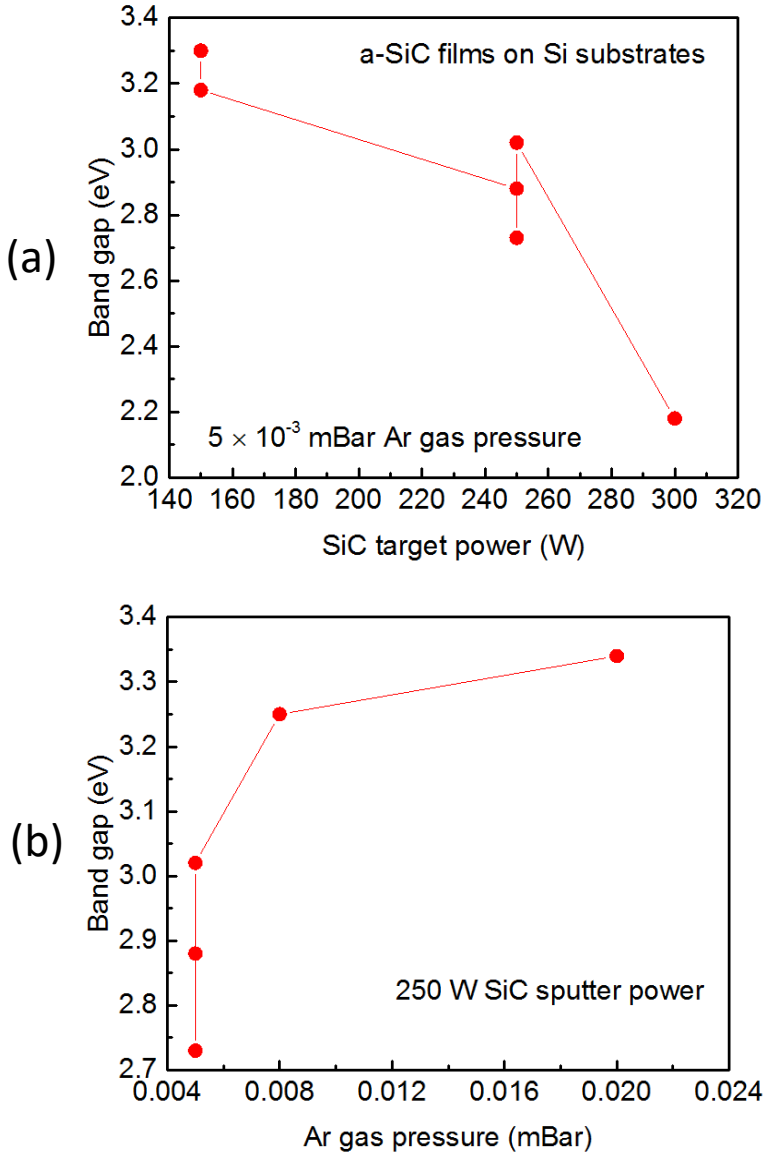


Figure 4-4. The band gap of a-SiC films RF sputtered using (a) 5×10^{-3} mBar Ar gas pressure and 150 to 300 W SiC target power, and using (b) 250 W SiC target power and 5×10^{-3} to 20×10^{-3} mBar Ar gas pressure.

4.2 Bonding structure of a-SiC films

FTIR measurement has been conducted in transmission mode, on the RF sputtered a-SiC films on Si substrates to investigate the chemical composition and bonding structure of the a-SiC films. Figure 4-5a shows the raw FTIR spectra of RF sputtered a-SiC films on Si substrates, between 400 cm^{-1} and 4000 cm^{-1}. Although the background of the raw FTIR spectra largely altered the value of absorbance,

the infrared absorption peaks are still distinguishable, as shown in Figure 4-5a. Figure 4-5b shows the processed FTIR spectra in which the background was removed using FTIR spectrum measured from a blank Si substrate. By comparing the FTIR spectra in Figure 4-5a and 4-5b, it is clear that the position of infrared absorption peaks was not altered by the background removing process.

In the fingerprint wavenumber region 500 to 1450 cm^{-1}, two absorption band were clearly observed for all the a-SiC films. The first one with absorption peak around 789 to 823 cm^{-1} could be assigned to the Si-C stretching ν [46, 122, 151, 152]. The second one with absorption peak around 997 to 1041 cm^{-1} could be assigned the Si-O stretching ν, which suggests the existence of impurity oxygen components in the a-SiC films. In addition, absorption band that has lower intensity can also be detected in some of the a-SiC films around 1259 to 1419 cm^{-1}. These peaks could be assigned to the $C\text{-}H_3$ twisting δ^s 1250 cm^{-1}, $Si{=}CH_2$ scissoring δ 1360 cm^{-1}, and $C\text{-}H_3$ wagging δ^a 1405 to 1412 cm^{-1}, and suggests the existing of hydrogen components in the a-SiC films. The appearance of the hydrogen and oxygen contents is inconsistent with the non-oxygenated and non-hydrogenated sputtering condition utilised to deposit these films and is believed due to H_2O/O_2 from the atmosphere diffused into the film after deposition [122]. The source of oxygen and hydrogen in these films is possibly from contaminations and will be further discussed in this section.

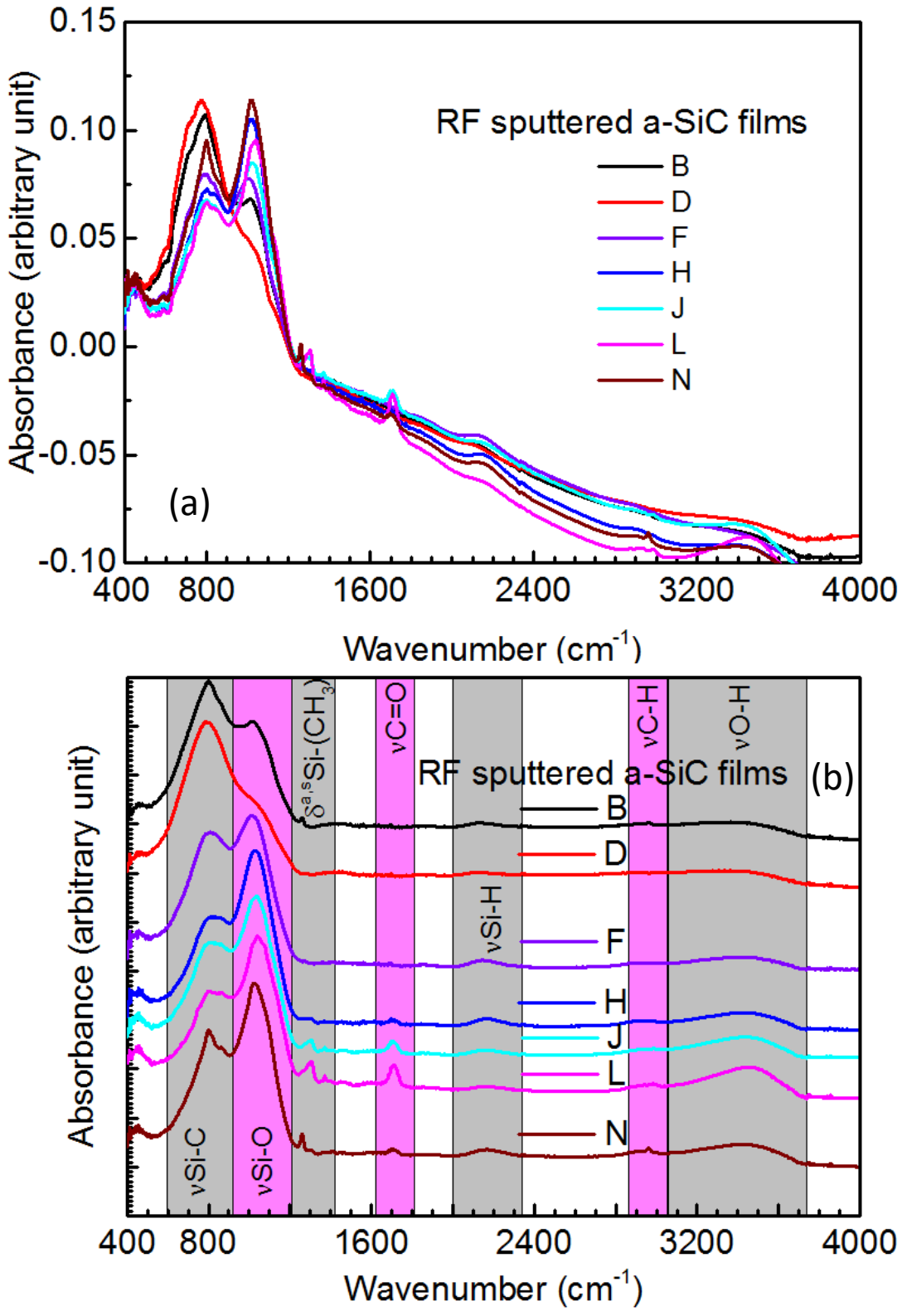


Figure 4-5. FTIR spectra of a-SiC films on Si substrates. (a) Raw spectrum. (b) Processed spectrum. Greek letters were used to represent different vibration modes: ν=stretching, δ^a= wagging, and δ^s=twisting.

In the functional group wavenumber region, 1450 to 4000 cm^{-1}, four absorption bands were observed for most of the a-SiC films, as shown in Figure 4-5. The first absorption band located

approximately at 1600 to 1800 cm^{-1}, which could be assigned to the C=O stretching ν. The C=O stretching ν absorption peak is most pronounced in the FTIR spectra of a-SiC sample H, J, L, and N, suggests higher incorporation of organic functional groups in the films. The second absorption band located approximately at 2000 to 2300 cm^{-1}, which could be assigned to the Si-H stretching ν. The Si-H stretching ν peaks were found around 2120 to 2173 cm^{-1} which is consistent with the values for hydrogenated a-SiC (a-SiC:H) in the literature [122]. The formation of the Si-H bond is attributable to the H_2O contamination diffusion into the films and passivated silicon dangling bonds [122]. The third absorption band located at approximately 2800 to 3100 cm^{-1}, which could be assigned to the C-H stretching ν. The existing of C-H stretching ν absorption peak is consistent with absorption peaks observed at approximately 1259 to 1419 cm^{-1} which were assigned to the $Si-CH_3$ wagging and twisting vibration. The last and most interesting absorption band located approximately at 3400-3600 cm^{-1}, which could be assigned to the O-H stretching ν. The existing of O-H stretching in the 3400-3600 cm^{-1} indicates the presence of silanol groups in the a-SiC films which suggests the Si-O bonds in a-SiC films was formed by H_2O contamination passivated any silicon dangling bonds after the deposition [122]. The position of all the observed absorption peaks in the FTIR spectra of the RF sputtered a-SiC films on Si substrates in Figure 4-5, is summarised in Table 4-2.

Table 4-2. Summary of observed peak positions for various chemical bonds related oscillation modes, in the a-SiC films on Si substrates.

a-SiC films	FTIR peak position (cm^{-1})						
	ν Si-C	δ^a $Si-CH_2-Si$/ ν Si-O	$\delta^{a,s}$ $Si-CH_3$	ν C=O	ν Si-H	ν C-H	ν O-H
B	800.31	1016.30	1259.29	1843.61	2119.39	2960.20	3453.88
D	788.74	997.02	1419.35	1845.54	2119.39	2873.42	3426.89
F	808.23	1016.30	1419.35	1845.54	2146.38	2890.77	3451.96
H	823.46	1031.73	1307.50	1695.12	2171.45	2910.06	3453.88
J	823.46	1039.44	1303.64	1708.62	2163.74	2981.41	3453.88
L	806.10	1041.37	1305.57	1708.62	2173.38	2981.41	3457.74
N	800.31	1024.02	1259.29	1697.05	2169.53	2962.13	3453.88

4.3 Chemical concentration of a-SiC films

The concentration of Si, C, O, and H contents in a-SiC films was obtained using nuclear reactive analysis (NRA) combined with Rutherford backscattering spectrometry (RBS) measurement and was

shown in Table 4-3. Atomic percentage (at%) of contents in the a-SiC films was calculated from using Equation 4.1:

$$at\%_E = N_E / \sum N_i, \quad (4.1)$$

where N is the concentration of composition elements. The at% of Si, C, O, and H in the a-SiC films was listed in Table 4-4. For most of the a-SiC films, at% of Si is close but slightly lower than at% of C. The Si/C is about 0.67 to 0.98 among all the a-SiC films. The extra Carbon in the a-SiC films likely comes from contamination. Also, the result shows very high at% of the O and H contents. It is possible that the O and H contents come from the diffusion of H_2O/O_2 into the films after deposition instead of from the sputtered process. No clear relation between the sputtering condition and chemical composition of the a-SiC films could be identified.

Table 4-3. Concentration of contents in the a-SiC films.

a-SiC films	Concentration N_E (10^{15} atom·cm^{-2})			
	Si	C	O	H
B	752	870	340	357
D	805	893	282	232
F	679	725	437	528
H	718	829	693	1042
J	610	768	552	716
L	684	1022	747	972
N	753	891	691	856
Q	692	704	476	649

Table 4-4. Atomic percentage of contents in the a-SiC films.

a-SiC films	Atomic percentage				Si/C ratio
	Si	C	O	H	
B	32.4%	37.5%	14.7%	15.4%	0.86
D	36.4%	40.4%	12.7%	10.5%	0.90
F	28.7%	30.6%	18.4%	22.3%	0.94
H	21.9%	25.3%	21.1%	31.7%	0.87
J	23.1%	29.0%	20.9%	27.1%	0.79
L	20.0%	29.8%	21.8%	28.4%	0.67
N	23.6%	27.9%	21.7%	26.8%	0.85
Q	27.4%	28.0%	18.9%	25.7%	0.98

4.4 Mass density of a-SiC films

Mass density ρ of the a-SiC films can be calculated when N_E of all contents and thickness d are known, using Equation 4.2:

$$\rho = \sum(N_E \times AMU_E) / dN_{av}, \quad (4.2)$$

where AMU_E is the atomic mass unit of the contents, and N_{av} is Avogadro's number (6.02×10^{23} particles per mol). The mass density of a-SiC films calculated including and excluding the O and H contents were summarised in Table 4-5. The mass density of the a-SiC films is close to the values of hydrogenated a-SiC (a-SiC:H) in the literature [84, 153] while noticeably lower than the mass density of crystalline SiC 3.2 g·cm^{-3}. Lower mass density of our a-SiC films is attributable to the increasing H content and nano pores in the films [84]. It is not clear at the moment how the mass density of a-SiC films would affect resistive-switching behaviours of a-SiC resistive memories. Hence, deposition condition of a-SiC film sample D which has mass density closet to the mass density of crystalline SiC was used in the fabrication of our a-SiC resistive memories for the simplicity of resistive-switching analysis.

Table 4-5. The mass density of the a-SiC films. Mass density has been calculated both include and exclude O and H contents.

a-SiC films	a-SiC thickness (nm)	Mass density (g·cm^{-3})	
		Include O and H	Exclude O and H
B	287.9	2.2	1.8
D	274.4	2.3	2.0
F	274.3	2.1	1.7
H	341.6	2.1	1.5
J	308.1	1.9	1.4
L	392.3	1.9	1.3
N	345.4	2.1	1.5
Q	299.8	2.0	1.5

Figure 4-6a shows the Si at% and C at% in the a-SiC films with their corresponding mass density calculated include and exclude the O and H contents. A-SiC films with higher mass density generally have higher Si at% and C at%, no matter the mass density was calculated including or excluding the O and H contents. Figure 4-6b shows the O at% and H at% in the a-SiC films with their corresponding mass density calculated include and exclude the O and H contents. A-SiC films with higher mass density generally have lower O at% and H at%, no matter the mass density was calculated including

or excluding the O and H contents. It is possible that the O and H contents are impurities diffused into the a-SiC films after deposition, and the a-SiC films with higher mass density are more resistant to the diffusion of H_2O/O_2.

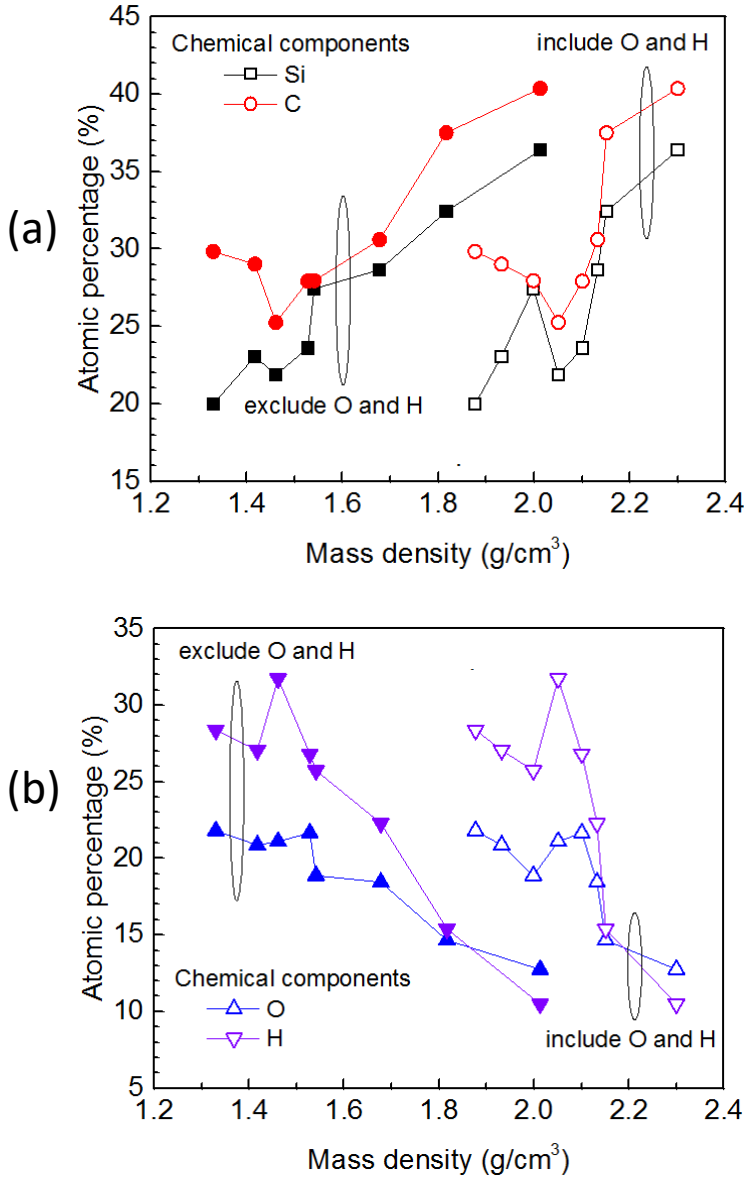


Figure 4-6. The at% of chemical contents in the a-SiC films with their mass density calculated including and excluding the O and H contents. (a) Si and C. (b) O and H.

The mass density of the a-SiC films was plotted with their SiC target power and Ar gas pressure as shown in Figure 4-7a and 4-7b, respectively to investigate the effect of sputtering condition on the mass density of the a-SiC films. The mass density of the a-SiC films does not show a clear dependence on the SiC target power. While both the mass density of the a-SiC films decreases with the increase of Ar gas pressure. This is attributable to the fact that sputtered SiC particles undergo more collisions with the Ar gas atoms in the sputtering chamber with higher Ar gas pressure, before arriving the substrate surface, which makes the a-SiC films more loosely packed and has lower mass

density [154]. Also, the increase of Ar gas pressure would also reduce the energy of neutral Ar^0 reflected from the SiC target which is the cathode. This would reduce the effect of 'hot' neutral (hot means high energy) bombardment on the substrate surface, hence less loosely bonded particles was knock-off and the film is less densified [155].

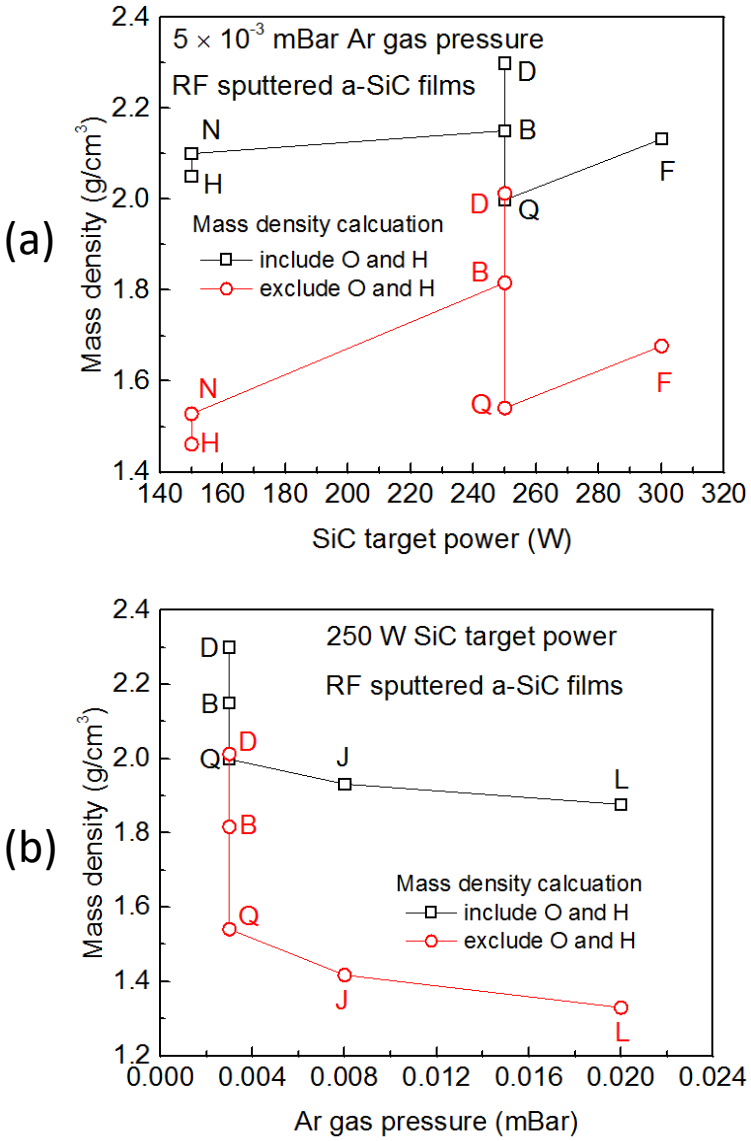


Figure 4-7. The mass density of a-SiC films RF sputtered using (a) 5 × 10^{-3} mBar Ar gas pressure and 150 to 300 W SiC target power, and using (b) 250 W SiC target power and 5 × 10^{-3} to 20 × 10^{-3} mBar Ar gas pressure.

Figure 4-8a shows the refractive index versus mass density of the a-SiC films. The refractive index n generally increases with the increase of mass density ρ which is consistent with the Lorentz-Lorenz equation, also known as the Clausius-Mossotti relation and Maxwell's equation, which is described by Equation 4.3 [147, 156-158],

$$\frac{n^2-1}{n^2+2} = \frac{4\pi N_{av}\alpha}{3M}\rho, \qquad (4.3)$$

where α is the mean molecular polarisability, and M is the molecular weight (40.11 g·mol^{-1} for SiC). It is interesting to find out the relation between refractive index and mass density of a-SiC films from a general material research point of view. The $\frac{n^2-1}{n^2+2}$ was plotted as a function of ρ which is known as the Lorentz-Lorenz plot as shown in Figure 4-8b, to better observe the Lorentz-Lorenz relation. The refractive index fits well on straight lines with the mass density as expected from Equation 4.3. The α extracted from the fits with corresponding mass density calculated including and excluding the O and H contents are 6.5×10^{-24} cm^3 and 4.3×10^{-24} cm^3 which are all in the correct order of magnitude. The straight line fits the data with mass density calculated including the O and H contents has a fit quality factor R^2 = 0.70 and an intercept=-0.35. While, the straight line fits the data with mass density calculated excluding the O and H contents has a higher R^2=0.95 and an intercept=0.05 closer to zero as Equation 4.3 required [147].

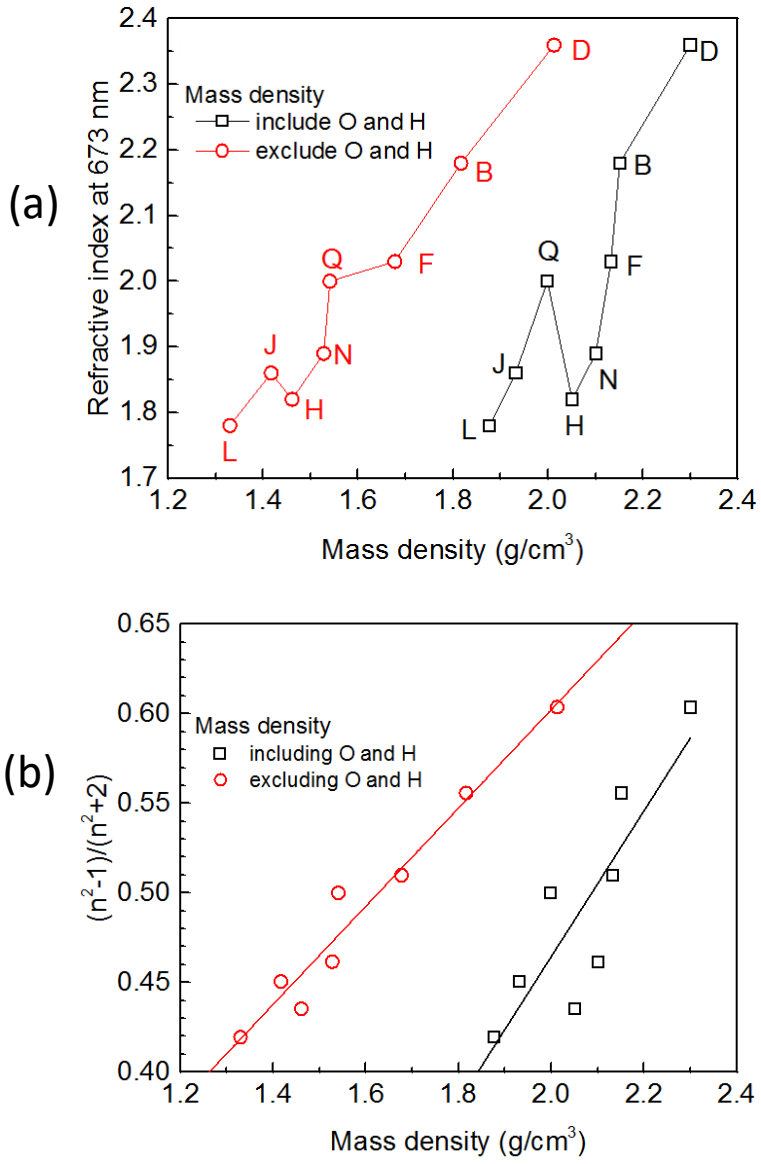


Figure 4-8. Refractive index of a-SiC films with their corresponding the mass density. (a) Linear plot. (b) Lorentz-Lorenz plot, with respective linear fits.

4.5 Electrical resistivity of a-SiC films

Four-point-probe and Van der Pauw measurements have been conducted on the a-SiC films to investigate their electrical resistivity. Both four-point-probe and Van der Pauw measurements measure the sheet resistance of the sample in the plane of the sample surface. The resistivity of the sample can be calculated when the sheet resistance and the thickness d is known, using Equation 3.12. The sheet resistance of most a-SiC films was out of the range of both four-point-probe and Van der Pauw measurements. The sheet resistance and resistivity of a-SiC films that was detected in the four-point-probe and Van der Pauw measurements were summarised in Table 4-6.

Table 4-6. Sheet resistance and resistive of a-SiC films.

a-SiC films	Substrate	a-SiC thickness (nm)	Four-point-probe		Van der Pauw	
			Sheet resistance (Ohm/□)	Resistivity (Ohm-cm)	Sheet resistance (Ohm/□)	Resistivity (Ohm-cm)
A	SiO_2/Si	249.8	N.A.	N.A.	5.7×10^8	1.4×10^4
B	Si	287.9	N.A.	N.A.	N.A.	N.A.
C	SiO_2/Si	236.4	N.A.	N.A.	1.7×10^7	4.0×10^2
D	Si	274.4	7×10^7	1.9×10^3	5.5×10^6	1.5×10^2

The maximum sheet resistance could be detected using our four-point-probe system is in theory around 6.3×10^7 Ohm/□. Hence, the a-SiC films with thickness around 300 nm need to have a resistivity lower than 2K Ohm-cm, to have their sheet resistance detected by the four-point probe system. Although our Van der Pauw system could, in theory, detect sheet resistance up to 10^{11} Ohm/□ which is higher resistivity compare to the four-point probe system, the actual maximum sheet resistance could be detected is lower due to the high requirement on low contact resistance. The measurements do indicate high resistivity for all a-SiC films but it is clear that in-plane conductivity measurements are not very suitable to detect actual values.

4.6 Capacitance of the fabricated devices

Cu/a-SiC/Au and Cu/a-SiC/W resistive memories were fabricated to investigate the resistive-switching in the a-SiC film and the effect of the inert electrodes on the switching characteristics. The deposition condition of a-SiC film sample D (same as sample A, B, C) was selected to be used in the deposition of the a-SiC insulating layer of both the Cu/a-SiC/Au and Cu/a-SiC/W resistive memories, as described in Chapter 3.1.4. The selection of sample D is because it has the highest mass density among all our a-SiC film samples and the value 2.0-2.3 g/cm^3 is closest to the mass

density of crystalline SiC 3.2 g/cm^3. The mass density closer to that of crystalline SiC indicates fewer defects/voids in the a-SiC film sample D which help simplify our analysis of switching characteristics. The effect of material properties of a-SiC layer which can be tuned in the sputtering process, on switching characteristics is worth investigating in the future, as discussed later in Chapter 8.2 Future work.

Figure 4-9 shows the cross-section SEM of an a-SiC resistive memory. A 300 nm Au or W inert electrode is at the bottom of the device structure. The 40 nm a-SiC insulating layer is on top of the inert electrode, and a 300 nm Cu electrode is on top of a-SiC. The Cu/a-SiC/Au or Cu/a-SiC/W device structure in the centre is the active device area. Also, there is a SiO_2 barrier covered with a-SiC and Cu surrounds the active device area.

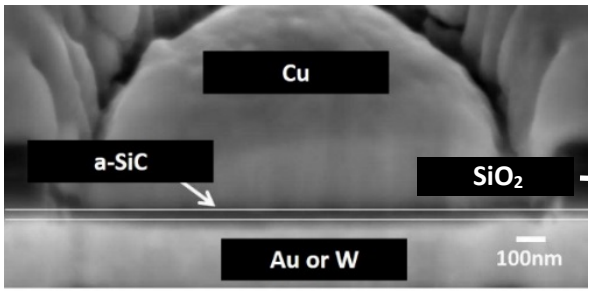


Figure 4-9. Cross-section SEM image of an a-SiC resistive memory.

Figure 4-10 shows the capacitance-voltage (C-V) characteristics of pristine Cu/a-SiC/W devices. The C-V characteristics of the Cu/a-SiC/SiO_2/W insulating structure on the same device chip were presented in Figure 4-10 for reference. The capacitance does not change with the bias voltage, as expected for Metal/Insulator/Metal capacitor. The DC voltage in C-V measurements was ramped up to a maximum ± 0.1 V to avoid switching the resistance state of the device in C-V measurement. Similar C-V characteristics have been observed on pristine Cu/a-SiC/Au devices.

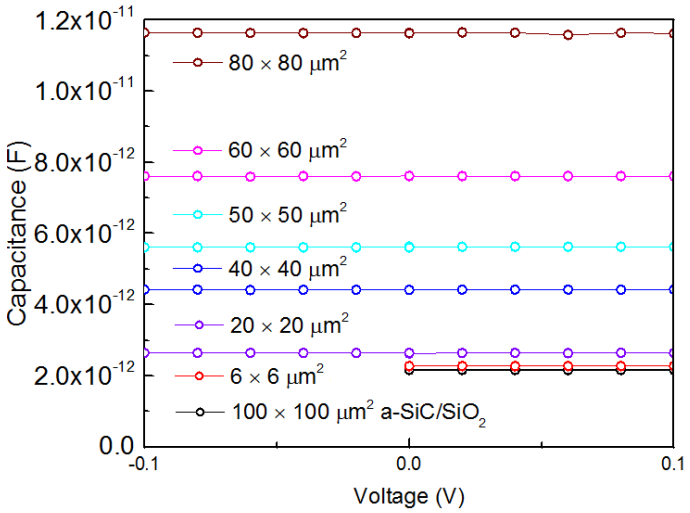


Figure 4-10. Capacitance-voltage (C-V) of pristine Cu/a-SiC/W devices.

In Figure 4-10, the capacitance of Cu/a-SiC/W devices is getting close to the capacitance of Cu/a-SiC/SiO_2/W insulating structure with the reducing of active device area. This is because the Cu/a-SiC/W devices contain a Cu/a-SiC/SiO_2/W insulating structure around the active device and the area of the insulating structure increase with the decrease of active device area. The contribution of the active device area and the insulating structure to the total capacitance is described by the Equation 4.4,

$$C_{total} = C_{SiC} + C_{insulating}\frac{A_{insulating}}{100\ \mu m \times 100\ \mu m} = \frac{\varepsilon_0 \varepsilon_{SiC} A_{SiC}}{d_{SiC}} + C_{insulating}\frac{100\ \mu m \times 100\ \mu m - A_{SiC}}{100\ \mu m \times 100\ \mu m}, \quad (4.4)$$

where C_{SiC} is the capacitance of the active device area, $C_{insulating}$ is the capacitance of an 100 µm × 100 µm full size Cu/a-SiC/SiO_2/W insulating structure, A_{SiC} is the active device area, $A_{insulating}$ is the area of the insulating structure surrounding the active device area, ε_0 is the permittivity of free space, ε_{SiC} is the dielectric constant of the a-SiC, and d_{SiC} is the thickness of a-SiC.

Figure 4-11 shows the capacitance of the active device area of Cu/a-SiC/W and Cu/a-SiC/Au devices. The capacitance is proportional to the active device area as expected. The dielectric constant of the a-SiC is extracted to be 7.5 to 7.6, from the proportionality factor of capacitance-area dependence, which is consistent with the dielectric constant of SiC in the literature [99].

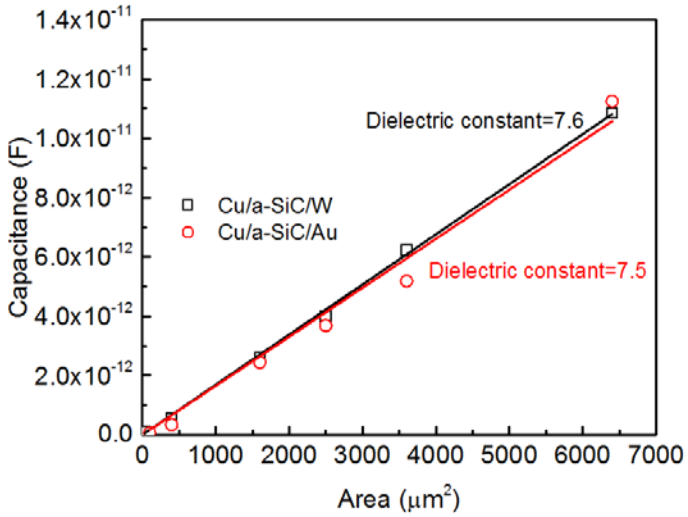


Figure 4-11. Capacitance at 0 V of the active device area of Cu/a-SiC/W and Cu/a-SiC/Au devices, with respective linear fits.

4.7 W vs Au as the inert electrode

Bipolar resistive-switching has been observed from both Cu/a-SiC/Au and Cu/a-SiC/W devices. Figure 4-12a and 4-12b show the DC current-voltage (I-V) sweep of a-SiC resistive memories with Au and W inert electrodes, respectively. Both were SET from a high resistance state (HRS) to a low

resistance state (LRS) by applying a $+V_{SET}$, and RESET from an LRS to a HRS by applying a $-V_{RESET}$, for multiple cycles. The ON/OFF ratio between LRS current I_{ON} and HRS current I_{OFF} at 0.1 V, for both a-SiC resistive memories with Au and W electrodes, is around 2×10^7 which is comparable with the values previously observed in a-SiC resistive memories [9, 10, 46] and higher than the value around 10^4 reported for the majority of resistive memories that have other materials as the insulating layer.

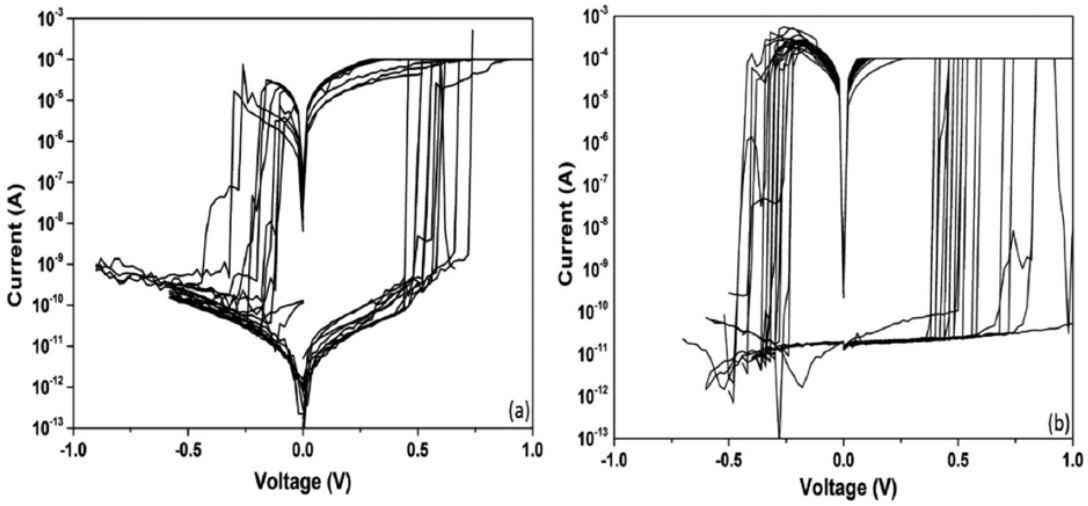


Figure 4-12. Bipolar resistive-switching of a-SiC resistive memories with (a) Au and (b) W inert electrode.

Previously, Cu/a-SiC/Au resistive memories LRS conduction has been identified as metallic Ohmic conduction [10, 46] in bipolar resistive-switching. Cu/a-SiC/W devices is compared to Cu/a-SiC/Au devices in Figure 4-13, to see if changing the inert electrode affects the LRS current conduction. LRS I-V characteristics in the Log(I)-Log(V) scale fit with straight lines with gradient around 1.00 for both a-SiC resistive memories with W and Au inert electrodes, indicating Ohmic current conduction [159].

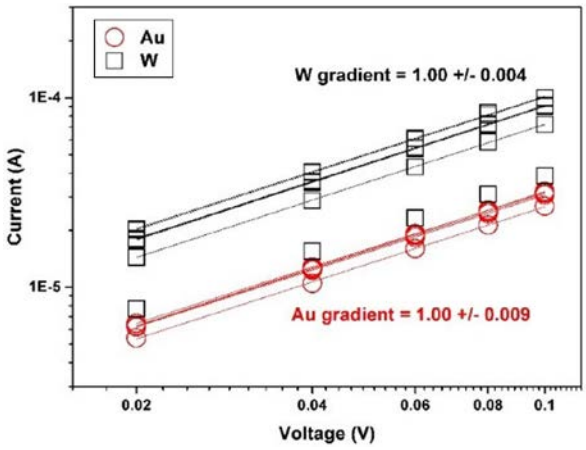


Figure 4-13. LRS I-V characteristics in the Log(I)-Log(V) scale, for a-SiC resistive memories with W and Au bottom electrodes, with respective linear fits.

The pristine state and HRS current conduction of Cu/a-SiC/Au resistive memories have been previously identified as reverse bias Schottky emission [10]. Pristine state and HRS I-V characteristics of Cu/a-SiC/W resistive memory were plotted in the Ln(I)-√V scale, as shown in Figure 4-14, to see if changing the inert electrode effects the HRS current conduction. The straight lines fit well with Ln(I)-√V for Cu/a-SiC/W, indicating the pristine state and HRS current conduction is reverse bias Schottky. The Schottky emission behaviour seen in a-SiC resistive memories with both W and Au inert electrodes, originates from Schottky barriers between the metal electrodes and the a-SiC, contributing to their ultra-high HRS resistance.

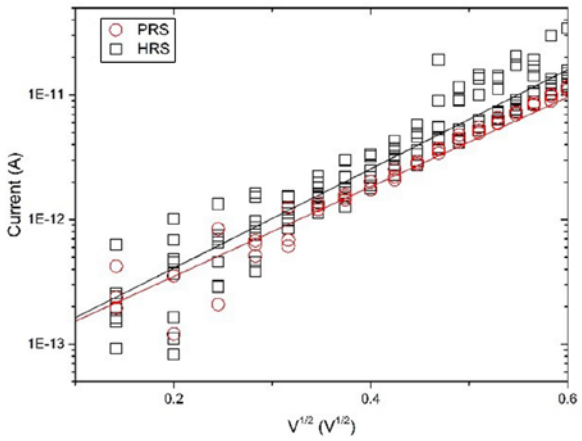


Figure 4-14. Plot of Ln(I)-√V for pristine state (PRS) and HRS of a Cu/a-SiC/W device, with respective linear fits.

Previously, Cu/a-SiC/Au resistive memory has shown repeatable pulsed switching with the highest ON/OFF ratio for any ECM resistive memory of ON/OFF ratio $\geq 10^8$ as shown in Figure 4-15a [144]. Pulsed switching for a Cu/a-SiC/W resistive memory is shown in Figure 4-15b, with LRS resistance R_{ON} and HRS resistance R_{OFF} on average 100 Ohm and 10^9 Ohm, respectively. Although the ON/OFF ratio 10^7 of the Cu/a-SiC/W resistive memory is slightly lower compared Cu/a-SiC/Au, the pulsed switching of Cu/a-SiC/W is comparable with Cu/a-SiC/Au.

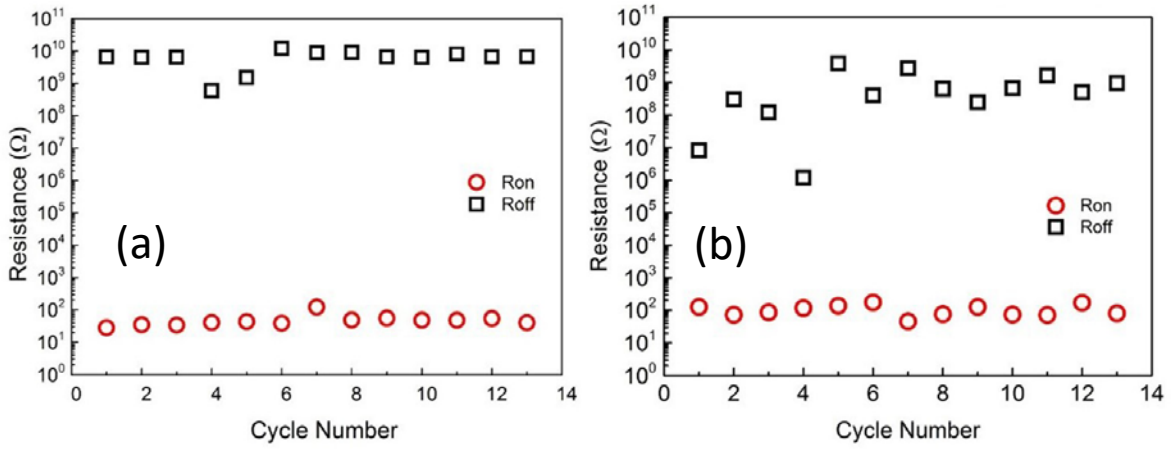


Figure 4-15. Pulsed measurements for (a) Cu/SiC/Au and (b) Cu/SiC/W resistive memories.

4.8 Summary

In conclusion, material properties of a-SiC films and resistive-switching of a-SiC resistive memories were studied. The influence of sputtering condition on the material properties of a-SiC films including refractive index, band gap, and mass density was investigated. The refractive index of a-SiC films is in the range 1.8 to 2.5 and reduces with increasing Ar gas pressure in the sputtering. The band gap of a-SiC films is in the range 2.2 to 3.3 eV. O and H contents were found in a-SiC films. The origin of O and H contents is possible from contamination. The mass density of a-SiC films calculated including and excluding the O and H contents are in the range 1.9 to 2.3 $g \cdot cm^{-3}$ and 1.3 to 2.0 $g \cdot cm^{-3}$, respectively. Also, a-SiC films with lower mass density have a higher concentration of O and H contents. It is possible that the O and H contents are impurities diffused into the a-SiC films after deposition, and the a-SiC films with higher mass density are more resistant to the diffusion of H_2O/O_2. The deposition condition of the a-SiC film sample D which has the highest mass density 2.0-2.3 g/cm^3 among our a-SiC film samples was selected to be used in the fabrication of both Cu/a-SiC/W and Cu/a-SiC/Au resistive memories. The mass density 2.0-2.3 g/cm^3 is closer to the value 3.2 g/cm^3 of single crystalline SiC hence it is likely that the a-SiC film sample D has fewer defects/voids. As a result, the analysis of switching characteristics is expected to be less complicated than using a-SiC with lower mass density.

The dielectric constant 7.5-7.6 of a-SiC was determined from the capacitance of the active device area of Cu/a-SiC/W and Cu/a-SiC/Au devices. Also, bipolar resistive switching has been observed from these a-SiC resistive memories with W and Au inert electrodes. High ON/OFF ratio around 10^7 was observed from DC I-V sweep and pulsed switching of Cu/a-SiC/W, which is comparable with the ON/OFF ratio of Cu/a-SiC/Au previously observed. Ohmic conduction in LRS and reverse bias Schottky emission in HRS were the same between a-SiC resistive memories with W and Au inert

electrodes. Generally, switching performance did not show a significant difference by changing the Au inert electrode with W which is a native BEOL material. The Cu/a-SiC/W resistive memory with BEOL compatibility is promising for future resistive memory applications.

Chapter 5: Cu embedded amorphous SiC films and RMs

In this chapter, the properties of Cu embedded amorphous SiC (a-SiC:Cu) films and Cu/a-SiC:Cu/Au resistive memories were studied. The aim is to find out if Cu embedding in the a-SiC insulating layer can improve the resistive switching and how much Cu volume% (Cu%) is needed. Firstly, the effect of Cu% on the electrical conduction of a-SiC:Cu needs to be determined because the a-SiC:Cu with an overdose of Cu could change the material into a metal which cannot be used as the insulating layer in resistive memory. The effect of the microstructure features on the electrical conduction of the a-SiC:Cu films, with Cu% between 0 % and 57 %, was analysed by temperature dependent measurements, along with an effective-medium approximation model. The insulator-metal transition of a-SiC:Cu was found at 57 Cu%. The dielectric constant of the a-SiC:Cu films was measured from pristine Cu/a-SiC:Cu/Au device structures. The electrical contacts between metal electrodes, i.e. Cu and Au, and a-SiC:Cu resulted in Schottky emission. Also, the effect of the Cu embedding on resistive switching characteristics was studied for 20 and 30 Cu%. Reduced forming and SET voltages and increased endurance were observed for devices with 30 Cu%. At the same time, all key advantageous characteristics of amorphous SiC resistive memory such as ON/OFF ratio of 10^7 and the co-existence of bipolar and unipolar modes were maintained upon Cu embedding.

5.1 Microstructure of a-SiC:Cu films

Figure 5-1 shows the EDX spectra and corresponding Cu% a set of a-SiC:Cu samples on Al substrates. A-SiC:Cu films with suitable Cu% were selected to be used in the fabrication of a-SiC:Cu resistive memories. A-SiC:Cu films with Cu% range from 0% to 57% were successfully achieved.

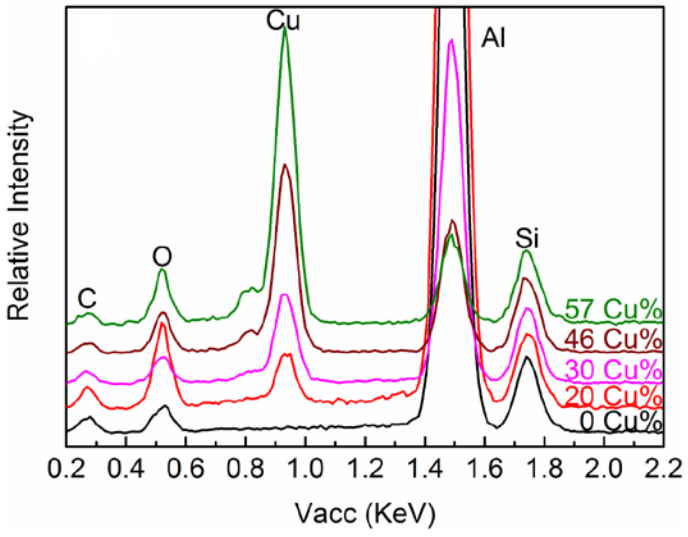


Figure 5-1. EDX spectra of co-sputtered a-SiC:Cu films on Al substrates.

Microstructure of a-SiC:Cu were studied using XRD and TEM. Knowing the size and distribution of Cu in a-SiC:Cu helps the analysis of the analysis of electrical conduction of a-SiC:Cu films. Figure 5-2 shows high-resolution XRD pattern of a-SiC:Cu films on the SiO_2/Si substrates. The absence of the characteristic crystalline SiC (111) peak at 35.7° [160] indicates the sole presence of amorphous SiC in the films. The peak observed at 43.6° corresponds to Cu Nanoparticles (NPs) [161], and its broadening reflects the Cu NPs diameter (D) according to the Scherrer equation, which is described by Equation 5.1 [162],

$$D = 0.94\lambda/[\beta cos(\theta)], \quad (5.1)$$

where λ is the X-ray wavelength of the Cu Kα radiation (0.1541 nm), β is the full width at half maximum of the peak, and θ is the diffraction angle. Cu NPs sizes of approximately 1.0 nm, 1.2 nm, 2.0 nm, and 2.5 nm were obtained for a-SiC:Cu films with 20%, 30%, 46%, and 57% Cu, respectively. The increase of the Cu NPs size with increasing Cu% indicates that higher Cu target power not only affects the Cu% but also increase the Cu NPs sizes. The increase of Cu NPs size with Cu target power aligns with reported works in relation to metal depositions using magnetron sputtering [163, 164]. Generally speaking, high target power induces sputtered species with high energy and thus high mobility on the substrate which subsequently form large particles.

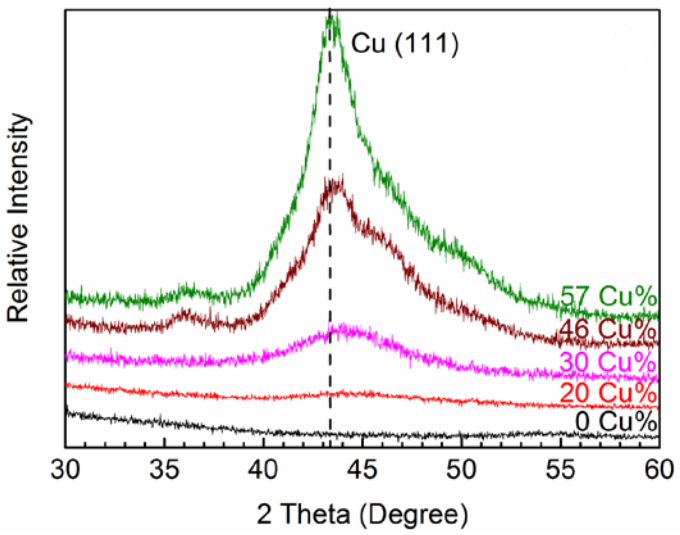
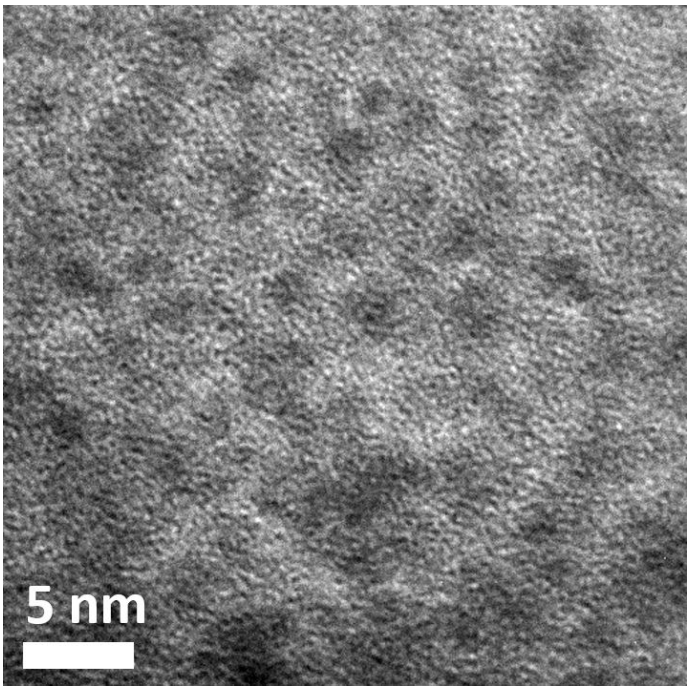


Figure 5-2. XRD patterns of co-sputtered a-SiC:Cu films on SiO_2/Si substrates.

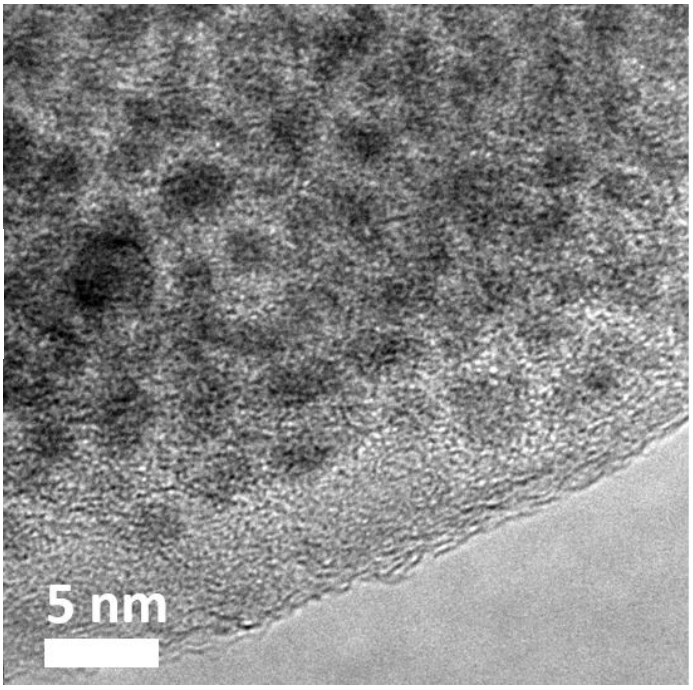
TEM bright-field images of a-SiC:Cu samples with typical Cu% including 20%, 30% and 57% are shown in Figure 5-3 a, b, and c, respectively. The dark-colour particles are attributed to the scattering of electron with Cu NPs which are heavier than the background a-SiC and scatter electrons at bigger angles. Also, the EDX spectra of a-SiC:Cu samples shown Si, C, and Cu signal as expected. Well distributed Cu NPs were clearly observed. Moreover, an increased density of Cu

particles with increasing Cu% were observed. The size of these particles is approximately 1-5 nm which roughly agree with the results from XRD analysis.

(a)



(b)



(c)

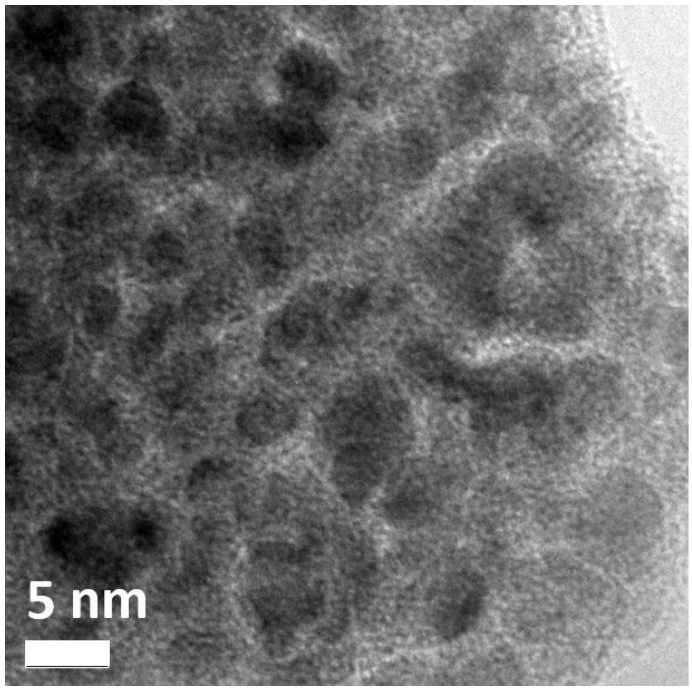
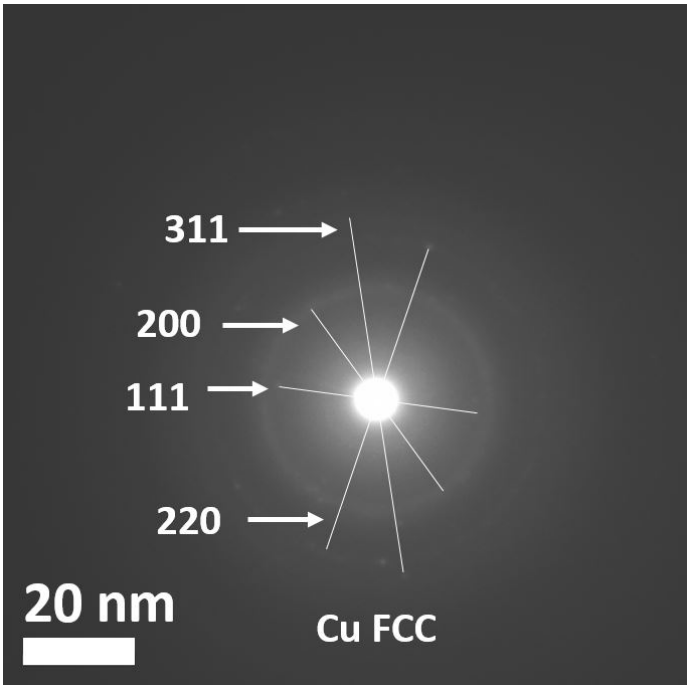


Figure 5-3. TEM images of a-SiC:Cu with (a) 20 Cu%, (b) 30 Cu%, and (c) 57 Cu%.

Selected area electron diffraction (SAED) images of of a-SiC:Cu with 20, 30, and 57 Cu% are shown in Figure 5-4 a, b, and c, respectively. Four indicated fringe patterns have radii in the ratio of √3:√4:√8:√11, which corresponds to the (111), (200), (220), and (311) planes of crystalline Cu with face-centered cubic (FCC) structure [165]. The crystalline structure of Cu observed is consistent with results of XRD analysis.

(a)



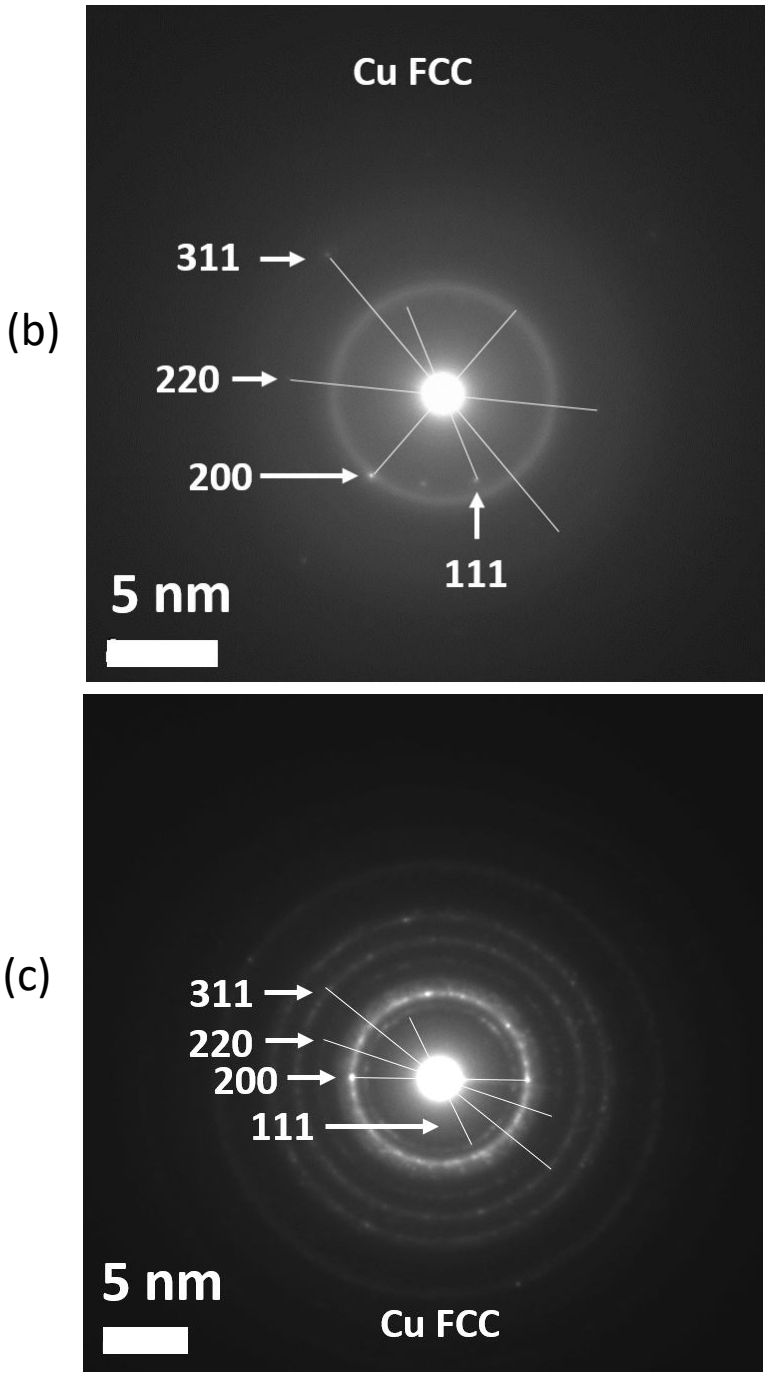


Figure 5-4. SAED images of a-SiC:Cu with (a) 20 Cu%, (b) 30 Cu%, and (c) 57 Cu%.

5.2 Electrical properties of a-SiC:Cu films

Electrical properties of a-SiC:Cu films were investigated to judge whether the a-SiC:Cu films are suitable to be used in the fabrication of a-SiC:Cu resistive memories. Figure 5-5 shows the normalised resistance R/R_{300K} of typical a-SiC:Cu films as a function of temperature obtained from two-point I-V measurements. A-SiC:Cu films with 20%, 30% and 46% Cu show semiconductor-like temperature dependence, where resistance decreases with increasing temperature, while the film

with 57% Cu starts to show sign of metal-like electrical behaviour. This suggests that the metallic percolation Cu% (X_c) is approximately at 57%, which is within the percolation thresholds estimated for metal-insulator composites in general [166]. The primary aim of this work is to investigate the electrical properties of the composite with Cu% below the percolation threshold. To further investigate the metal-insulator transition of the a-SiC:Cu composite with the increase of Cu%, resistivity measurements of a-SiC:Cu composite with 0 Cu% to 57% were conducted.

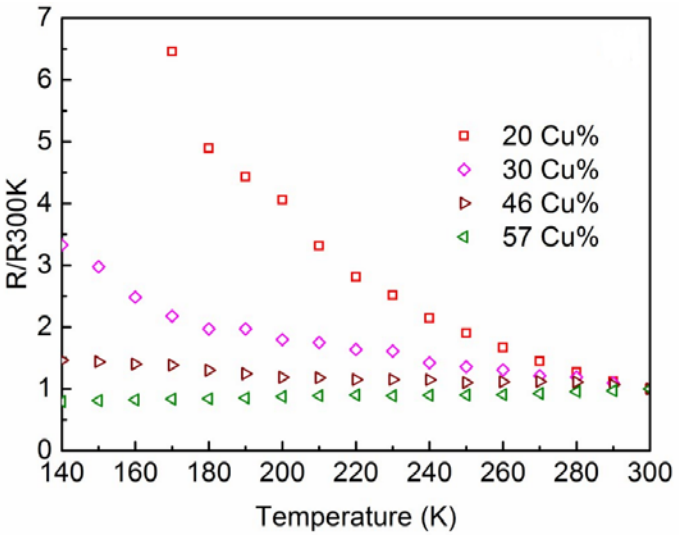


Figure 5-5. Normalised resistance of typical a-SiC:Cu films with 20 Cu% to 57 Cu%, as a function of temperature.

Figure 5-6 shows room temperature resistivity of a-SiC:Cu films as a function of Cu%. Since the Cu NPs sizes (<2.5 nm) in our films are much smaller than the film thickness (in the range between 120 nm and 580 nm), the a-SiC:Cu films can be assumed to be a three dimensional (3D) metal-insulator composites. An effective medium approximation (EMA) model has recently been reported to evaluate electrical conduction mechanism in 3D metal-insulator composites [166, 167]. In particular, when metal volume% is in the regime below percolation threshold Xc, the resistivity of the composite ρ as function of metal volume% X is dominated by tunnelling conduction mechanism which is described by Equation 5.2,

$$\frac{(X/X_c)}{\sqrt{1/\Sigma\rho}+1} + 4X\left\{\left[1+\frac{\xi}{2D}\ln(\alpha\Sigma\rho+1)\right]^3 - 1\right\} = 1, \qquad (5.2)$$

where α is a constant signifying ratio of tunnelling conductance over metallic conductance, Σ is a fitting parameter associated with conductivity of the effective medium and has a unit of S/cm, D is the diameter of metal NPs, and ξ is the tunnelling decay length which follows $\xi = \hbar/\sqrt{2mU_0}$, where m is the electron mass and U_0 is tunnelling barrier height. ξ value is estimated to be 0.2 nm by using U_0=0.94 eV for Cu/a-SiC contact [9]. Using ξ=0.2 nm, D=2.5 nm, and Xc=57% Cu in Equation 5.2, an optimal fit with R^2 value of 0.94 is achieved as shown in Figure 5-6 with $\alpha=1.7\times10^{-4}$ and Σ=2.5105

S/cm. This confirms that, for a-SiC:Cu films, when Cu is below its percolation threshold, tunnelling plays an important role in its electrical conduction performance. A-SiC:Cu films with typical Cu% below percolation threshold, including 20 and 30 Cu% were applied as the insulating layer of Cu/a-SiC:Cu/Au resistive memories.

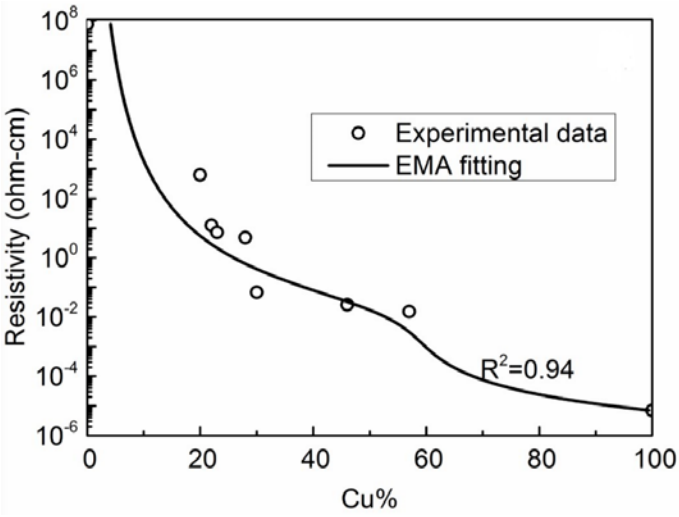


Figure 5-6. Resistivity of a-SiC:Cu films as a function of Cu% with the solid line showing fit based on EMA model.

5.3 Pristine state a-SiC:Cu RMs

The dielectric constants of a-SiC:Cu were obtained by measuring capacitance of pristine state Cu/a-SiC:Cu/Au devices, as shown in Figure 5-7. The Cu/a-SiC:Cu/Au devices have a cross-section structure as shown in the Schematic in Figure 3-1 and SEM image in Figure 4-9. Dielectric constant ε_r was extracted as 7.5, 5.4, and 4.6, for a-SiC:Cu with 0%, 20%, and 30% Cu, respectively. In particular, ε_r=7.5 for pure a-SiC aligns well with previous reported value [99].

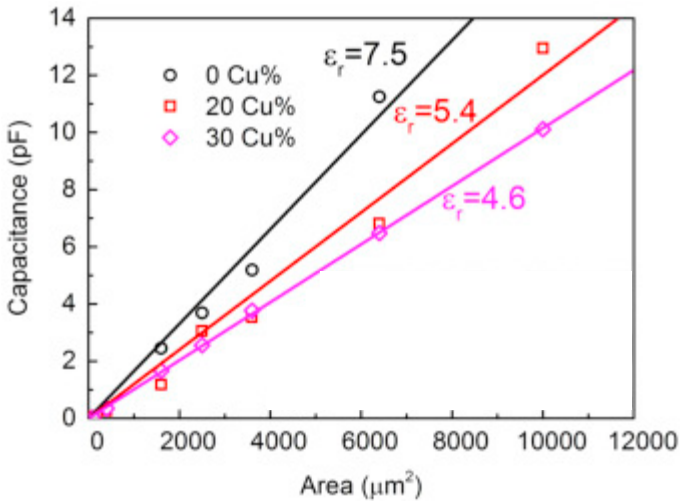


Figure 5-7. Capacitance as a function of micro-capacitor device areas, with respective linear fits.

Current density-voltage (J-V) characteristics were measured by applying a voltage to the Cu electrode while keeping Au electrode always grounded as described in Chapter 3.3.2, in order to investigate the conduction mechanism at the interface between metal electrodes and a-SiC:Cu films. It was found in our previous studies of Cu/a-SiC/Au resistive memories that the existence of a-SiC/metal Schottky contacts is the key factor for the ultra-high ON/OFF ratio of the Cu/a-SiC/Au resistive memories [9]. Therefore, it is important to understand how Cu embedding affects the a-SiC:Cu/metal Schottky contacts. Figure 5-8a and 5-8b show Ln(J)-√V when applying -V and +V to the Cu electrode, respectively. Linear fits are obtained for both voltage polarities which suggests reverse bias Schottky emission mechanism follows Equation 2.3. SBH values of 0.91 eV, 0.90 eV and 0.85 eV were extracted for 0%, 20%, and 30% Cu, respectively. The SBHs decrease with increasing Cu% is possibly related to enhanced tunnelling conduction mechanism [168] in a-SiC:Cu composites with higher Cu%. Furthermore, symmetric characteristics of Ln(J)-√V is observed in the –V and +V regions for all the devices. Despite the work function difference between Cu (4.9 eV) and Au (5.3 eV), SBH values in both voltage polarity regimes are similar. This may relate to strong Fermi level pinning effect in SiC due to the existence of defects [169] and high degree of covalency [99], which play a dominating effect in determining the SBHs.

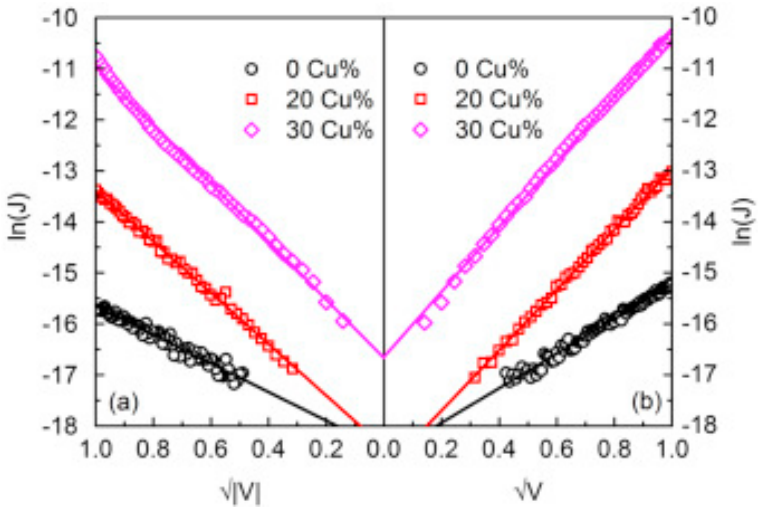


Figure 5-8. Ln(J)-√V when applying (a) -V and (b) +V to Cu electrodes, with respective linear fits.

5.4 Resistive-switching of a-SiC:Cu RMs

Figure 5-9 shows the forming I-V characteristics of multiple pristine Cu/a-SiC:Cu/Au resistive memories with 0%, 20% and 30% Cu%, respectively. In the pristine state, all the Cu/a-SiC:Cu/Au RMs with different Cu% show very high resistance, typically larger than 3 GOhm at 0.1V. When the voltage applied on the device increases to forming voltage V_{FORM}, an abrupt increase of current towards the 100 µA current compliance was observed and is attributable to the formation of Cu

conductive filament. Average values of V_{FORM} of Cu/a-SiC:Cu/Au RMs with 0 , 20 and 30 Cu% are 9.4 V, 6.8 V, and 2.8 V, respectively. It is likely that the reduction of V_{FORM} is due to the existing of embedded Cu NPs in the a-SiC:Cu insulating layers. It has been reported that the existence of metal NPs in an insulator film increases the electric field adjacent to the metal nanoparticles [72, 170, 171]. The reduction of V_{FORM} is hence attributable to the increase of electric field in the a-SiC:Cu layer, which accelerates the drift of Cu inside a-SiC:Cu from Cu electrode towards Au electrode.

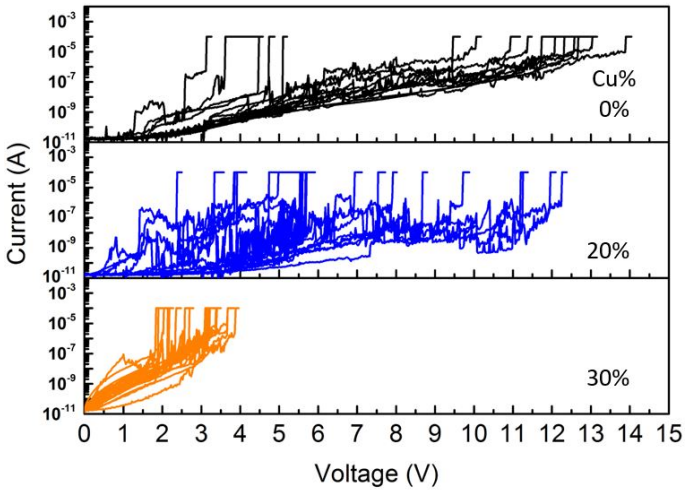


Figure 5-9. Forming I-V characteristics of multiple Cu/a-SiC:Cu/Au resistive memories with 0%, 20%, and 30% Cu%.

Figure 5-10a and 5-10b show typical I-V characteristics of the stable switching cycles of Cu/a-SiC:Cu/Au resistive memories with 50 × 50 μm^2 device area and different Cu% in bipolar and unipolar modes, respectively. The co-existence of bipolar and unipolar modes, which is a desired feature [172], was observed for all resistive memories with different Cu% and thus is not affected by Cu embedding. SET voltage (V_{SET}), RESET voltage (V_{RESET}), low resistance state resistance R_{ON} and high resistance state resistance R_{OFF} measured at 0.1 V, and ON/OFF ratio of the devices are summarised in Table 5-1. V_{SET} of Cu/a-SiC:Cu/Au resistive memories shows a reduction with increased Cu% in both bipolar and unipolar modes, which is attributable to the existence of embedded Cu NPs. Potential mechanism of V_{SET} reduction with increased Cu% are discussed in the following section. Furthermore, Cu/a-SiC:Cu/Au resistive memories with different Cu% show comparable ON/OFF ratios of approximately 10^7 in bipolar and 10^5 to 10^7 in unipolar modes. These ratios are higher than the typical ratio of $<10^4$ for the majority of resistive memories that have insulating layer made of other materials, suggesting great application potential for a-SiC:Cu.

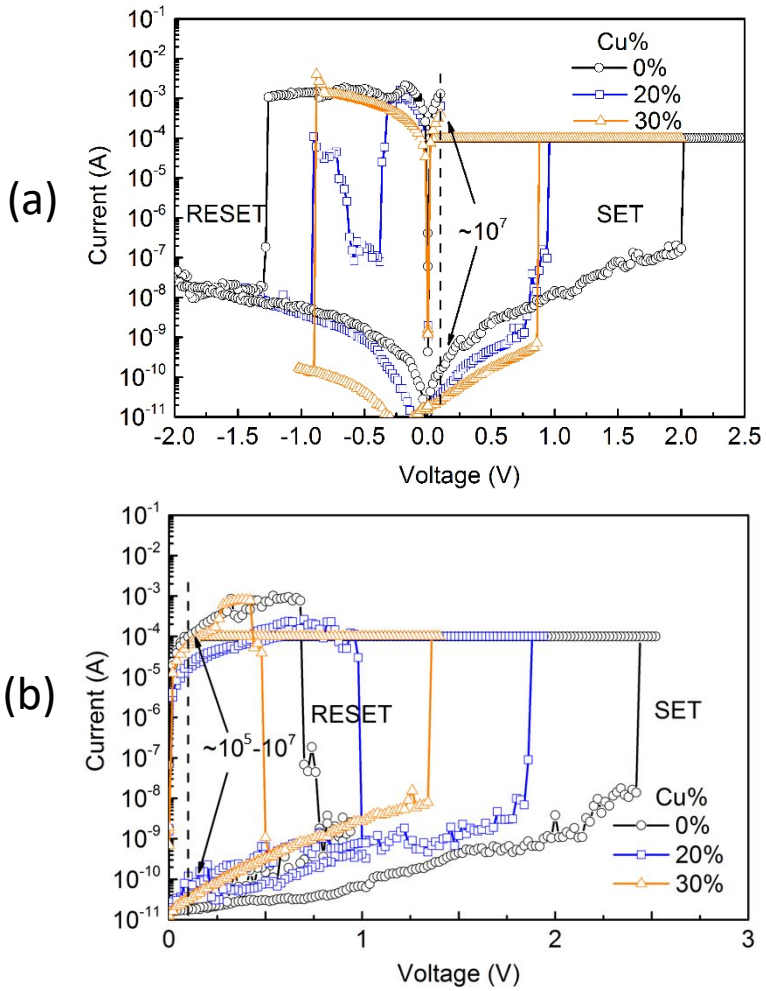


Figure 5-10. I-V characteristics of switching cycles. (a) Bipolar and (b) unipolar modes of Cu/a-SiC:Cu/Au resistive memories with different Cu%.

Table 5-1. Switching parameters of Cu/a-SiC:Cu/Au resistive memories with different Cu%.

RM with different Cu%	V_{SET} (V)	V_{RESET} (V)	R_{ON} (Ohm)	R_{OFF} (10^9 Ohm)	ON/OFF ratio (10^6)
Bipolar mode					
0%	2	-1.26	76	0.6	8.2
20%	0.94	-0.9	157	2.8	18
30%	0.86	-0.88	249	3.9	16
Unipolar mode					
0%	2.42	0.68	1030	5.2	5
20%	1.86	0.98	4910	1.7	0.4
30%	1.34	0.48	1600	2.9	1.8

5.5 Conduction mechanisms of a-SiC:Cu RMs

I-V analysis has been widely used as a method to decipher the conduction and switching mechanisms of resistive memories [9, 172]. Figure 5-11a and 5-11b show the LRS current conduction behaviour of Cu/a-SiC:Cu/Au resistive memories with different Cu% in bipolar and unipolar modes, respectively. The slope of linear fits of LRS in Log(I)-Log(V) plot are all close to 1, which indicates Ohmic conduction. We believe the Ohmic conduction in our devices with $+V_{SET}$ is attributable to the formation of Cu conductive filament [9]. The formation process of the Cu conductive filament could be described with the well-known ECM model [63]. In this model, when a positive voltage is applied on the Cu electrode, Cu atoms would be oxidised into Cu cations and drift toward the negatively charged Au electrode. Due to the low Cu drift rate, Cu cations would likely start to reduce before they reach the Au electrode and form Cu conductive filament which gradually grows towards the Au electrode. In Cu/a-SiC:Cu/Au resistive memories, the growth of Cu conductive filament might also pass a few positions where embedded Cu particles are located. Hence, for resistive memory with embedded Cu particles, the Cu atoms required to form the Cu conductive filament may be reduced as in comparison with resistive memory with 0% Cu, contributing to the reduction of V_{FORM} (Figure 5-9) and V_{SET} (Table 5-1).

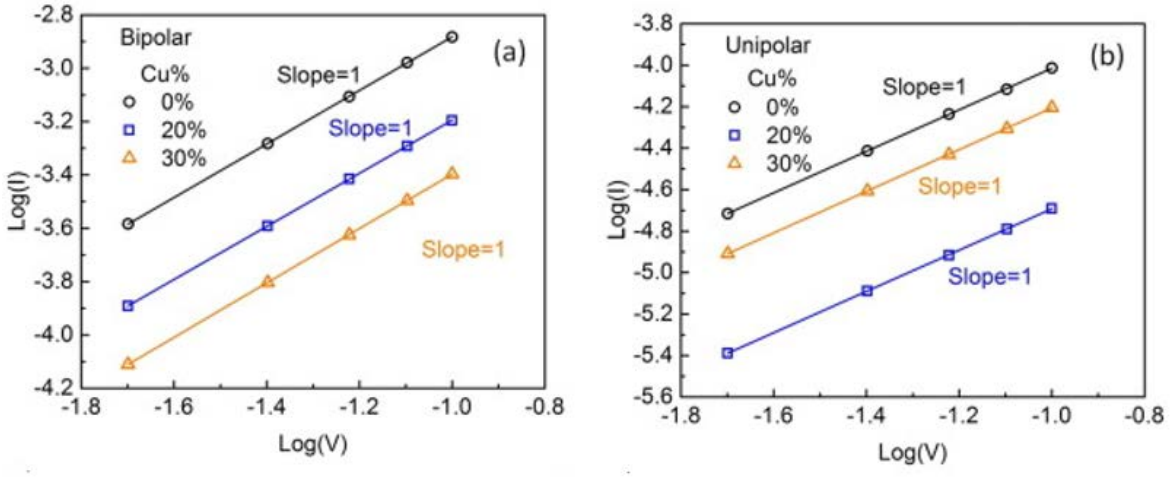


Figure 5-11. I-V characteristics of LRS of Cu/a-SiC:Cu/Au resistive memory for (a) bipolar and (b) unipolar modes, with respective linear fits.

Figure 5-12a and 5-12b show HRS characteristics of Cu/a-SiC:Cu/Au resistive memories with different Cu% in bipolar and unipolar modes, respectively. Linear fits in Ln(I)-√V plots of Cu/a-SiC:Cu/Au with all different Cu% suggests Schottky emission conduction which is described by Equation 2.3 [66]. The existence of Schottky contact is likely a contributing factor to the up to 5 Gohm R_{OFF}, and consequently high ON/OFF ratio of up to 10^7 of our Cu/a-SiC:Cu/Au resistive

memories [9]. The results suggest that Cu embedding would not change the existence of reverse bias Schottky emission conduction mechanism in HRS.

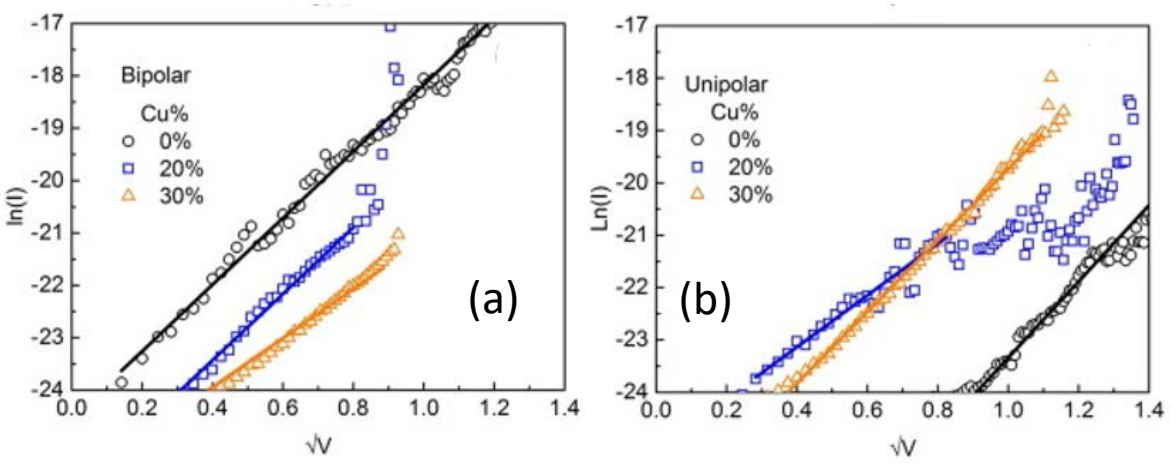


Figure 5-12. I-V characteristics of HRS of Cu/a-SiC:Cu/Au resistive memory for (a) bipolar and (b) unipolar modes, with respective linear fits.

5.6 Endurance of a-SiC:Cu RMs

Pulsed SET and RESET were used to switch the resistive memories repeatedly to test the effect of Cu embedding on the endurance of Cu/a-SiC:Cu/Au resistive memories. Resistance after each switch was read out at 0.1V to avoid large disturbance on the resistance state. Figure 5-13 show multiple cycles of Cu/a-SiC:Cu/Au resistive memories with 0%, 20%, and 30% Cu%, respectively. In Figure 5-13a to 5-13c, Cu/a-SiC:Cu/Au resistive memories with 30 Cu% shows most stable switching performance and the longest endurance. Although its ON/OFF ratio is about an order lower than devices with less Cu embedded, the remaining 10^6 ON/OFF ratio is still very high. Despite limited number of switching test cycles, our results suggest that Cu/a-SiC:Cu/Au RMs could be used in applications where different trade-offs between ON/OFF ratio, stability and endurance are required than in the consumer market, such as in harsh environment application [144].

5.7 Summary

Cu NPs embedded a-SiC with multiple Cu% in 0 to 57 Cu% range were fabricated. Cu NPs diameters approximated in the range 1 to 5 nm were extracted from high-resolution XRD spectra and TEM images. Electrical conduction of the a-SiC:Cu films was evaluated using an effective medium approximating model after knowing the diameter of the NPs is much smaller than the thickness approximately 120 to 580 nm of the a-SiC:Cu films. Electric resistance vs temperature suggests that the percolation threshold is close to 57 Cu%. Below the percolation threshold, tunnelling is

identified as the key conduction mechanism of the composites with the resistivity well described by the effective medium approximation model. Cu/a-SiC:Cu/Au resistive memories were fabricated using a-SiC:Cu with typical Cu% below percolation threshold including 20 and 30 Cu%. Measurements from pristine Cu/a-SiC:Cu/Au devices give dielectric constants of 7.5, 5.4, and 4.6 for a-SiC:Cu with 0, 20, and 30 Cu%, respectively. Reduced V_{FORM} and V_{SET} and increased endurance were observed in Cu/a-SiC:Cu/Au resistive memories, most noticeable at 30 Cu%. Furthermore, advantageous switching characteristics of a-SiC resistive memories including reverse bias Schottky emission in pristine state and HRS, high ON/OFF ratio up to 10^7, and co-existence of bipolar and unipolar modes were maintained upon Cu embedding. All above suggests that Cu embedding could be considered as a promising method to improve the overall performance of Cu/a-SiC:Cu/Au resistive memories.

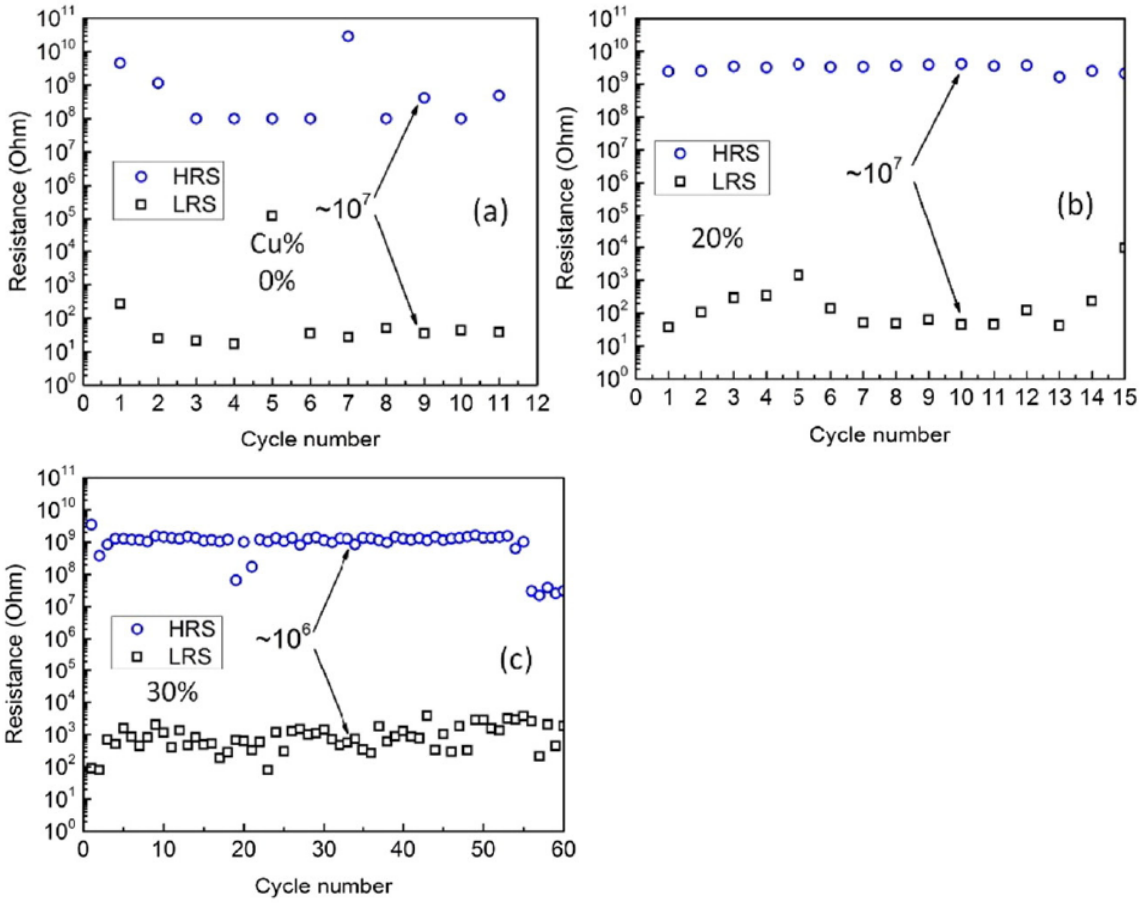


Figure 5-13. Endurance of pulsed switching of Cu/a-SiC:Cu/Au resistive memories with (a) 0%, (b) 20%, and (c) 30% Cu%. [173]

Chapter 6: Back-end-of-line a-Si(O)C:H films and RMs

Back-end-of-line (BEOL) dielectrics including a-SiC:H, a-SiOC:H, and a-SiCO:H were studied as the insulating layer of a-Si(O)C:H resistive memories in this chapter to understand the influence of material properties on switching characteristics which would be useful to develop resistive memory fabricated using exclusively native BEOL materials and have optimised performance. 20 nm and 40 nm a-Si(O)C:H films were deposited using PECVD, on Si substrates coated with 100 nm thermal oxide and 300 nm Cu by Intel®. Intel has also measured the chemical composition using Nuclear reaction analysis (NRA) and Rutherford backscatter spectroscopy (RBS). After we received the a-Si(O)C:H films, we performed XPS and VASE on the films to study the material properties of the a-Si(O)C:H films. W electrodes were patterned on the a-Si(O)C:H films to form the W/a-Si(O)C:H/Cu memory device structure. Current conduction in the pristine Cu/a-Si(O)C:H/W devices was studied using current density-voltage analysis combined with XPS analysis. Bipolar resistive-switching with ultra-high ON/OFF ratios 10^6 to 10^{11} have been observed from Cu/a-Si(O)C:H/W resistive memories. LRS and HRS current conduction mechanisms were analysed to deduce the switching mechanisms. An increase of V_{Form} with a-Si(O)C:H thickness was observed. Also, V_{FORM} of a-SiC:H devices was noticeably lower than a-SiOC:H and a-SiCO:H devices with the same thickness of a-Si(O)C:H. In addition, 20 nm a-SiOC:H devices have shown noticeable longer endurance than the other devices.

6.1 Material properties of a-Si(O)C:H films

The performance of resistive memories that have a-Si(O)C:H films as the insulating layer were studied layer in this chapter. The material properties of the insulating layer play an important role in resistive-switching characteristics. The chemical composition of the a-Si(O)C:H films were analysed using XPS. The thickness of the a-Si(O)C:H films were measured using VASE. Material properties such as refractive index and band gap that affects the dielectric properties of a-Si(O)C:H films and current conduction of a-Si(O)C:H Schottky contacts were also measured.

6.1.1 X-ray Photo-electron Spectroscopy (XPS) measurement of chemical composition

Figure 6-1 shows the survey XPS spectra of 20 nm and 40 nm a-Si(O)C:H dielectric films on Si substrates coated with 300 nm Cu. Si 2p and C 1s peaks were clearly observed from the survey XPS spectra of a-SiC:H films. No O 1s peak in the survey XPS spectra of a-SiC:H films indicates low oxygen contamination in the a-SiC:H films. Si 2p, C 1s, and O 1s peaks were clearly observed from the survey XPS spectra of a-SiOC:H and a-SiCO:H films.

The at% of Si, C, and O contents in the a-Si(O)C:H films was calculated using Equation 6.1,

$$at\%_{element} = (\frac{Area_{element}}{R.S.F_{element}}) / \sum_{i=1}^{N} (\frac{Area_i}{R.S.F_i}), \quad (6.1)$$

where Area is the area under the peak of the element, R.S.F is the relative sensitivity factor which is 0.817, 1, and 2.93 for Si 2p, C 1s, and O 1s, respectively. The at% of Si, O, and C calculated was summarised in Table 6-1. The chemical composition calculated from the XPS survey spectra is generally consistent with the values measured using NRA and RBS provided by Intel®, as shown in Table 3-1. The at% for the different film thickness of a-Si(O)C:H are consistent. The a-SiC:H films have nearly no O contents and <2 at% O measured by XPS was attributed to contaminations. Also, a-SiCO:H films have noticeably higher C contents than a-SiOC:H films, as expected.

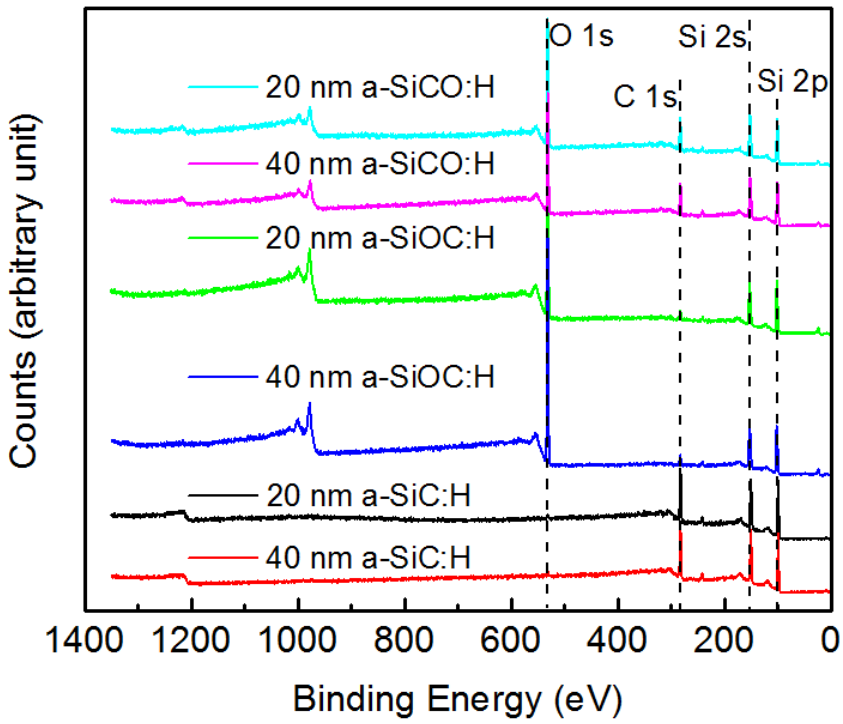


Figure 6-1. The XPS survey spectra of 20 nm and 40 nm a-SiC:H, a-SiOC:H, and a-SiCO:H films.

Table 6-1. At% of Si, C, and O contents in a-Si(O)C:H films calculated from the XPS survey spectra.

Dielectric films	Si at%	C at%	O at%
20 nm a-SiC:H	54.5	43.8	1.6
40 nm a-SiC:H	54.2	44.5	1.3
20 nm a-SiOC	46.3	7.3	46.4
40 nm a-SiOC	45.1	7.2	47.8
20 nm a-SiCO:H	46.5	24.4	29.1
40 nm a-SiCO:H	47.1	25.0	27.9

XPS narrow scan of Si 2p, C 1s, and O 1s were measured to investigate the bonding structure. The bonding structure in a-Si(O)C:H affects the dielectric constant which determines the RC delay of the logic circuit as well as the current conduction of a-Si(O)C:H Schottky contacts in the BEOL resistive memory. 20 nm films were chosen for XPS narrow scans, as surface charging is suppressed compared to the 40 nm films. Figure 6-2a and b show the Si 2p and C 1s XPS narrow scans, respectively, of a 20 nm a-SiC:H film. The Si 2p peak (96-104 eV) was deconvoluted into two peaks at 100.0 and 99.4 eV corresponding to Si-C and Si-Si/H bonds, respectively. The C 1s peak (278-288 eV) was deconvoluted into two peaks at 283.1 eV and 284.1 eV, corresponding to C-Si and C-C bond, respectively. Normalised area Area/R.S.F of deconvoluted peaks was extracted from the narrow scans, as shown in Table 6-2. Relatively high Area/R.S.F of the Si-Si/H indicates the presence of H contents in a-SiC:H which is consistent with the 35.1 at% of H measured by NRA and RBS.

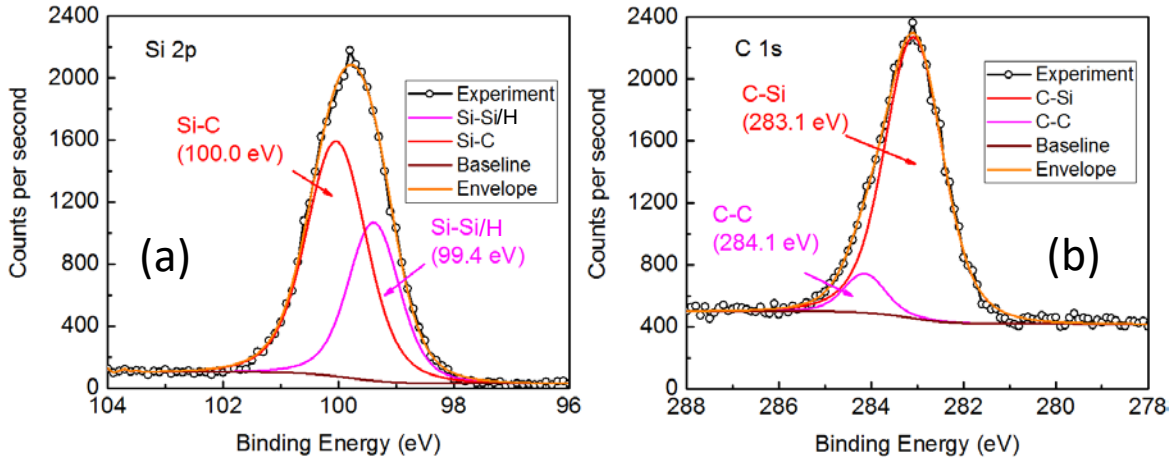


Figure 6-2. Narrow scans of Si 2p and C 1s XPS spectra for a 20 nm a-SiC:H film.

Table 6-2. Parameters of deconvoluted XPS peaks for a 20 nm a-SiC:H film.

Parameters	Si 2p		C 1s	
	Si-Si	Si-C	C-Si	C-C
B.E. (eV)	99.38	100.03	283.08	284.14
Area	1222.8	2124.0	3072.5	303.9
R.S.F	0.817	0.817	1	1
Area/R.S.F	1496.7	2599.8	3072.5	303.9

Figure 6-3a, b, and c show the Si 2p, C 1s, and O 1s XPS narrow scans, respectively of a 20 nm a-SiOC:H film. The Si 2p peak (96-106 eV) was deconvoluted into four peaks at 102.7 eV, 102.0 eV, 101.1 eV, and 100.0 eV corresponding to Si-O, O-Si-C, Si-C, and Si-Si/H bonds, respectively. The C 1s spectrum was composed mainly of a single peak at 283.5 eV which is mainly corresponding to the C-Si bond and may contain C-C and C-OH contribution. The O 1s peak (526-538 eV) was deconvoluted into two peaks at 532.3 eV and 531.7 eV, corresponding to Si-O-Si and O-Si bonds,

respectively. Normalised area Area/R.S.F of deconvoluted peaks was extracted from the narrow scans, as shown in Table 6-3. The Area/R.S.F of Si-O is noticeably higher than Si-C. Also, Area/R.S.F of the Si-Si/H is nearly negligible indicates the low concentration of H contents in a-SiOC:H which is consistent with the 8.7 at% of H measured by NRA and RBS.

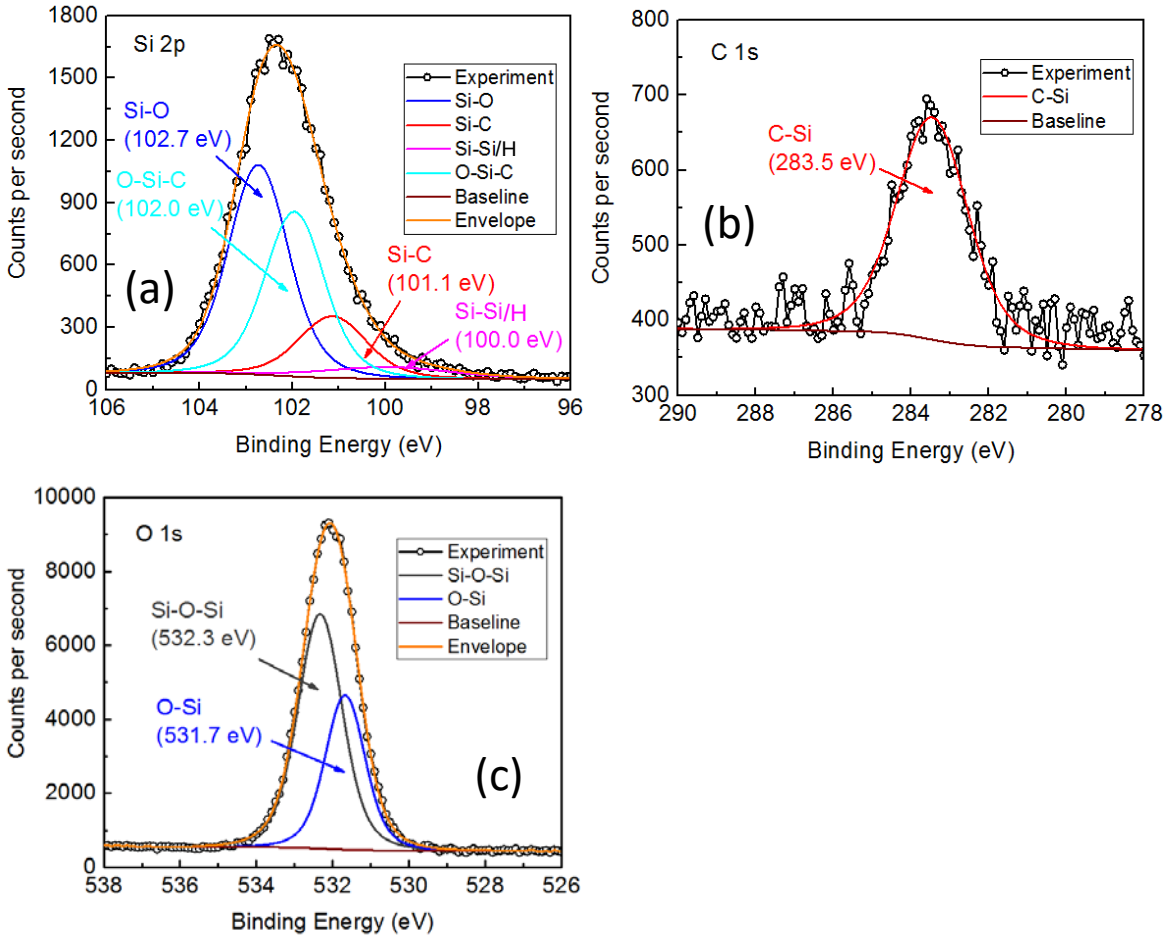


Figure 6-3. Narrow scans of (a) Si 2p, (b) C 1s, and (c) O 1s XPS spectra for a 20 nm a-SiOC:H film.

Table 6-3. Parameters of deconvoluted XPS peaks for a 20 nm a-SiOC:H film.

Parameters	Si 2p				C 1s	O 1s	
	Si-Si	Si-C	O-Si-C	Si-O	C-Si	O-Si	Si-O-Si
B.E. (eV)	99.96	101.14	101.96	102.73	283.46	531.67	532.33
Area	205.1	585.2	1372.1	1763.1	732.8	5855.5	9928.3
R.S.F	0.817	0.817	0.817	0.817	1	2.93	2.93
Area/R.S.F	251.0	716.3	1679.4	2158.0	732.8	1998.4	3388.5

Figure 6-4a, b, and cc show the Si 2p, C 1s, and O 1s XPS narrow scans, respectively of a 20 nm a-SiOC:H film. The Si 2p peak (96-106 eV) was deconvoluted into four peaks at 102.9 eV, 102.2 eV, 101.2 eV, and 100.0 eV corresponding to Si-O, O-Si-C, Si-C, and Si-Si/H bonds, respectively. The C 1s peak (278-290 eV) was deconvoluted into two peaks at 283.6 eV and 284.9 eV, corresponding to C-

Si and C-C bonds, respectively. The O 1s spectrum (526-538 eV) was composed mainly of a single peak at 538 eV which is mainly corresponding to the O-Si bond. Area/R.S.F of deconvoluted peaks was extracted from the narrow scans, as shown in Table 6-4. The Area/R.S.F of Si-C is noticeably higher than Area/R.S.F of Si-O.

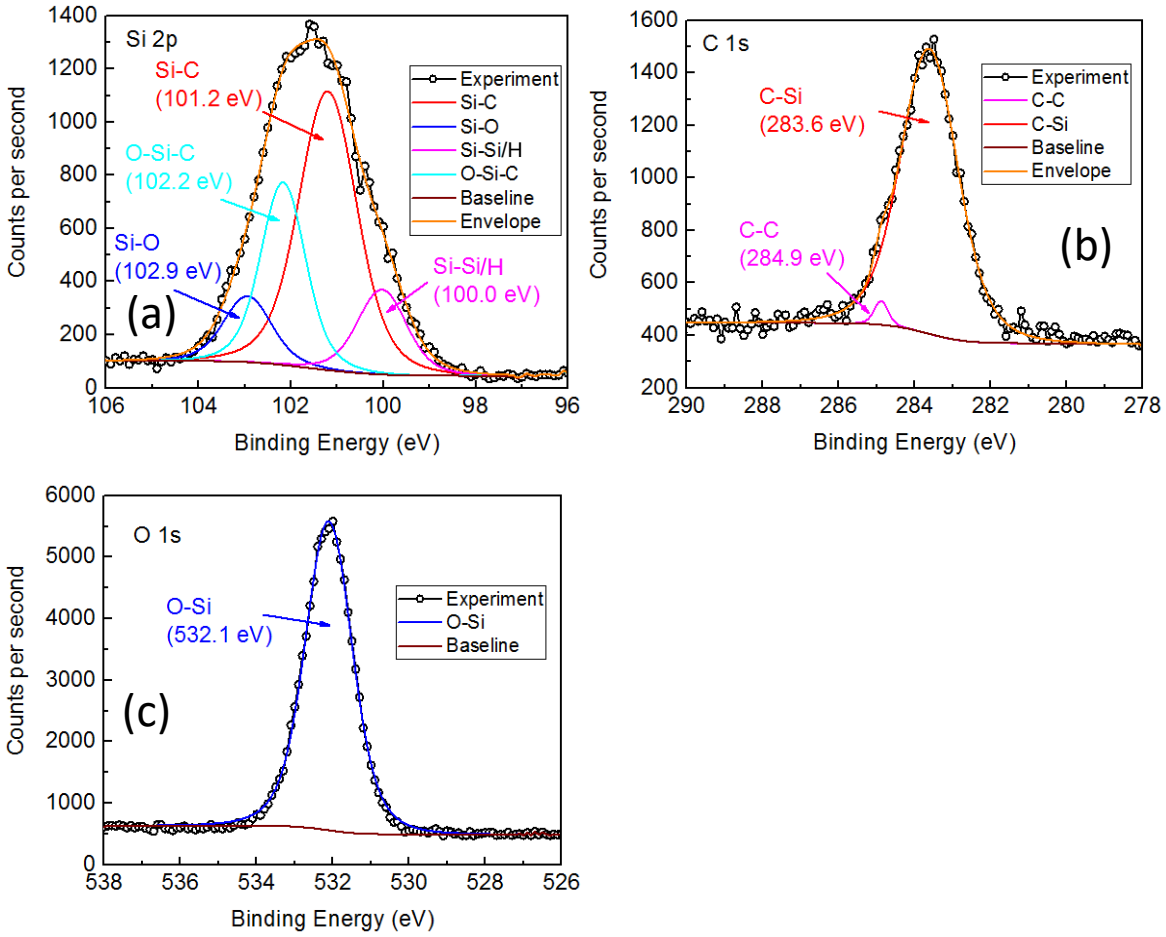


Figure 6-4. Narrow scans of (a) Si 2p, (b) C 1s, and (c) O 1s XPS spectra for a 20 nm a-SiCO:H film.

Table 6-4. Parameters of deconvoluted XPS peaks for a 20 nm a-SiCO:H film.

Parameters	Si 2p				C 1s		O 1s
	Si-Si	Si-C	O-Si-C	Si-O	C-Si	C-C	O-Si
B.E. (eV)	100.03	101.2	102.17	102.94	283.62	284.88	532.11
Area	456.8	1771.2	895.5	346.4	2215	44.901	8354.5
R.S.F	0.817	0.817	0.817	0.817	1	1	2.93
Area/R.S.F	559.1	2167.9	1096.1	424.0	2215.0	44.9	2851.4

6.1.2 Ellipsometry measurement of material properties

Variable angel spectroscopy ellipsometry (VASE) measurement was conducted on a-Si(O)C:H films on Si substrates coated with 300 nm Cu to investigate the thickness, refractive index, and band gap

of a-Si(O)C:H films. The thickness of the a-Si(O)C:H films extracted from the modelling of VASE spectra are around 21.2 to 23.6 nm and 40.0 to 45.6 nm, which are close to the respective nominal values of 20 nm and 40 nm given by Intel®. The a-Si(O)C:H films with thickness around 20 nm and 40 nm are referred as 20 nm a-Si(O)C:H films and 40 nm a-Si(O)C:H films in this thesis for simplicity. The effect of a-Si(O)C:H thickness on resistive-switching behaviour will be discussed in the following section.

In addition, the refractive index of a-Si(O)C:H films was extracted from the modelling of VASE spectra. Figure 6-5 shows the refractive index of the 20 nm and 40 nm a-Si(O)C:H films as a function of wavelength. The refractive index at 673 nm is 2.2 to 2.3, 1.6, and 1.7 to 1.9 for a-SiC:H, a-SiOC:H, and a-SiCO:H films, respectively, which agrees with the refractive index at similar wavelength of a-SiC:H [123, 136], a-SiOC:H [83], and a-SiCO:H [82, 136] films in the literature. All the refractive index of a-Si(O)C:H films in this thesis refers to refractive index at 673 nm.

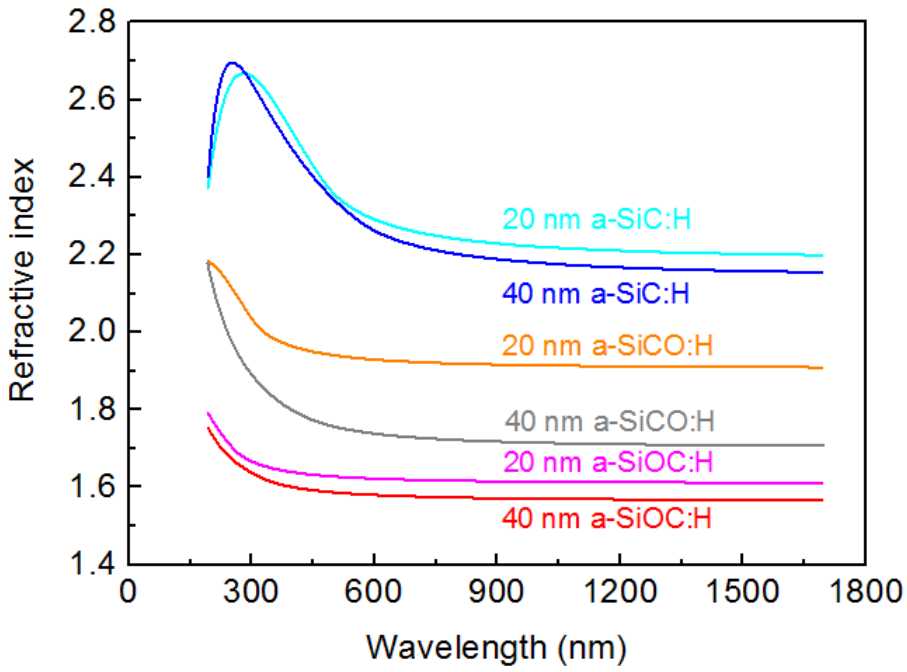


Figure 6-5. The refractive index as a function of wavelength of 20 nm and 40 nm a-Si(O)C:H films.

Moreover, the absorption coefficient α of a-Si(O)C:H films as a function of energy E was extracted from the modelling of VASE spectra. The extracted absorption coefficient was plotted in the Tauc plot for indirect band gap semiconductor which was discussed in Chapter 3.2.4. Figure 6-6 shows the Tauc plot of a-Si(O)C:H films. The band gap was determined from extrapolation of the linear part to αE=0 in the Tauc plot. The band gap E_g for a-SiC:H, a-SiOC:H, and a-SiCO:H was estimated to be 2.75 eV to 3.07 eV, 4.12 eV to 4.76 eV, and 4.00 eV to 4.03 eV, respectively, which is close to the band gap of a-SiC:H [123, 174], a-SiOC:H [82], and a-SiCO:H [82] films in the literature. Comparing the E_g of a-Si(O)C:H with their chemical composition listed in Table 3-1 and 6-1, an

increase of E_g with increasing C concentration was observed. This is attributable to extra electronic states induced by addition of carbon [82].

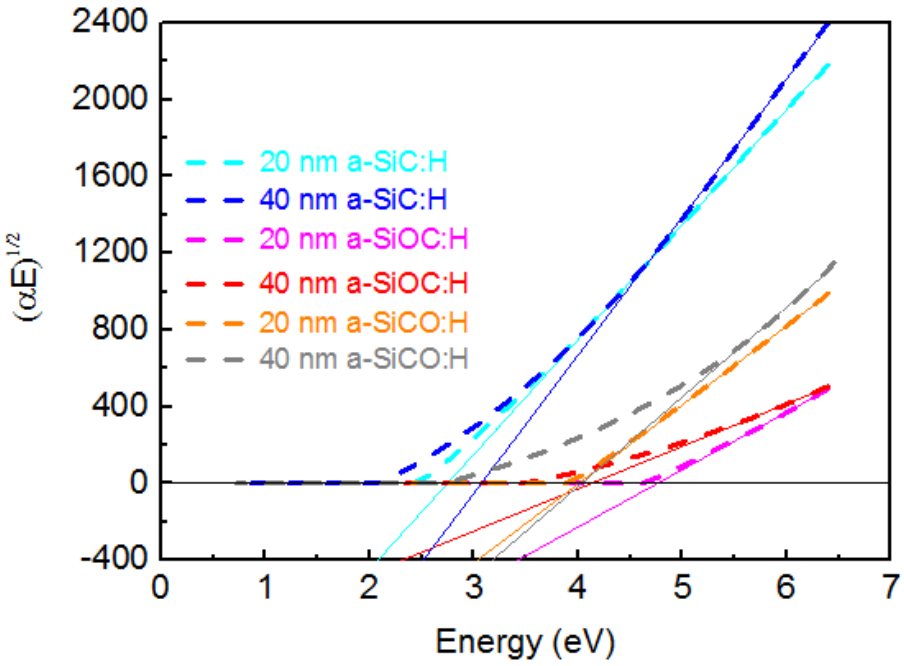


Figure 6-6. Tauc plot for a-Si(O)C:H films. α is the absorption coefficient, with respective linear fits.

6.2 Pristine W/a-Si(O)C:H/Cu device

W electrodes were patterned on 20 nm and 40 nm a-SiC:H, a-SiOC:H, and a-SiCO:H films to form the W/a-Si(O)C:H/Cu device structure of a-Si(O)C:H resistive memory. In the pristine state, the W/a-Si(O):H/Cu devices have electrical characteristics similar to a parallel plate capacitor. The fabrication quality of W electrodes on the a-Si(O)C:H insulating layer was verified by measuring the area dependence of current and capacitance of the pristine state. The current and capacitance were directly proportional to the device area indicating uniform W electrodes interface to the a-Si(O)C:H. The dielectric constant of the a-Si(O)C:H insulating layers was extracted from the capacitance of the pristine devices. An insulating layer with a lower dielectric constant is preferred for BEOL applications to reduce RC delay. Current conduction mechanism in the pristine W/a-Si(O)C:H/Cu devices were investigated using current-voltage measurement combined with XPS analysis. The understanding of current conduction mechanism of the pristine devices helps to understand the current conduction after the resistive-switching and the switching mechanisms. Also, it is interesting to investigate the current conduction of a-Si(O)C:H/Cu Schottky contacts from a material research point of view.

6.2.1 Fabricated devices

Figure 6-7a shows a device chip that contains W/a-SiC:H/Cu resistive memories. All the device chips of W/a-Si(O)C:H/Cu resistive memories are about 3 cm × 3 cm large and contain about a thousand W electrodes. The W electrodes patterned on top of the a-SiC:H insulating layer are shown in Figure 6-7b. The size of W electrodes of a-Si(O)C:H resistive memories is in the range 20 µm × 20 µm to 100 µm × 100 µm, which is also device area of the W/a-Si(O)C:H/Cu resistive memory. The W/a-Si(O)C:H/Cu device have a cross-section structure as shown in the Figure 6-7c. This device structure was described in Chapter 3.1.2.

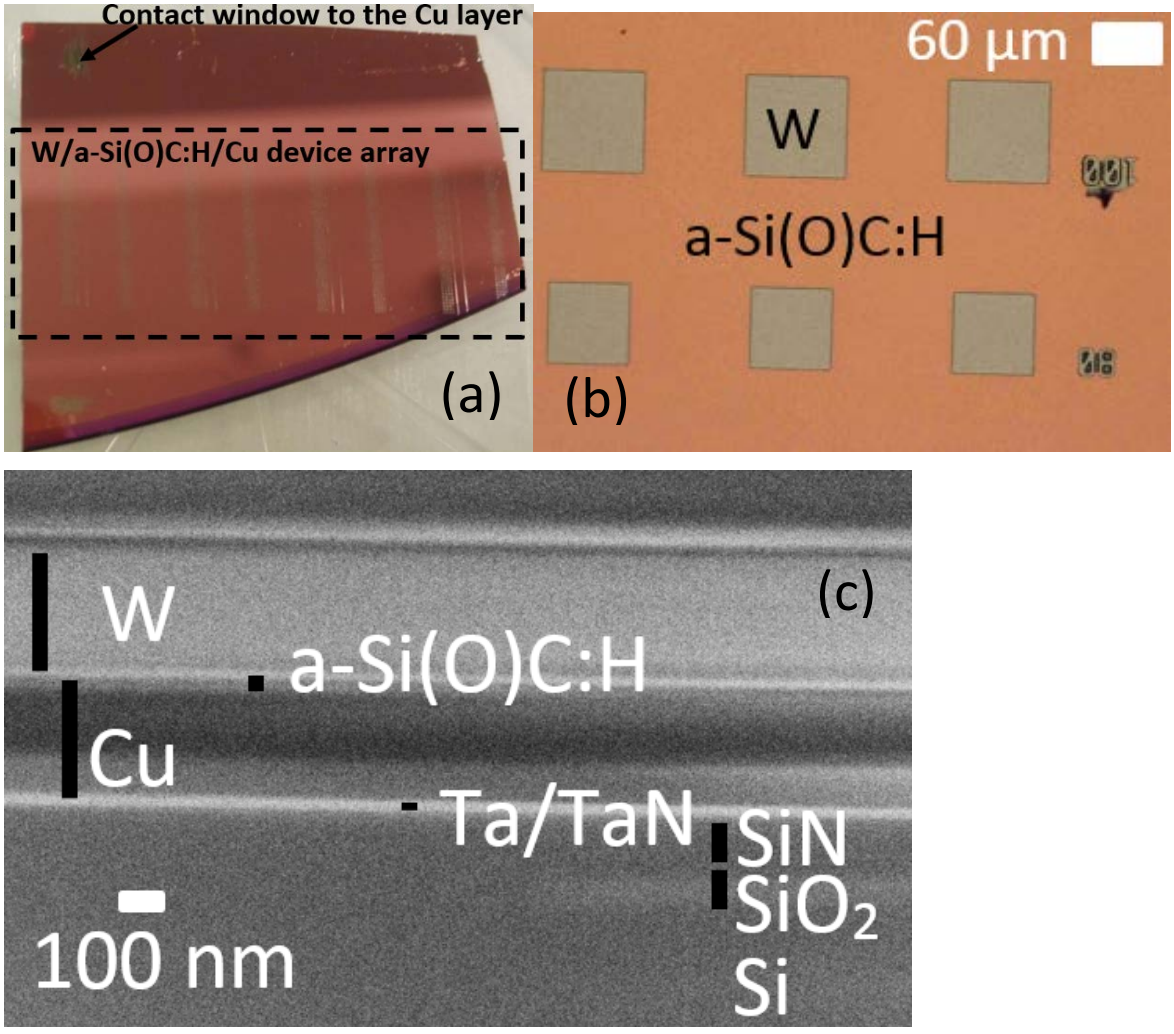
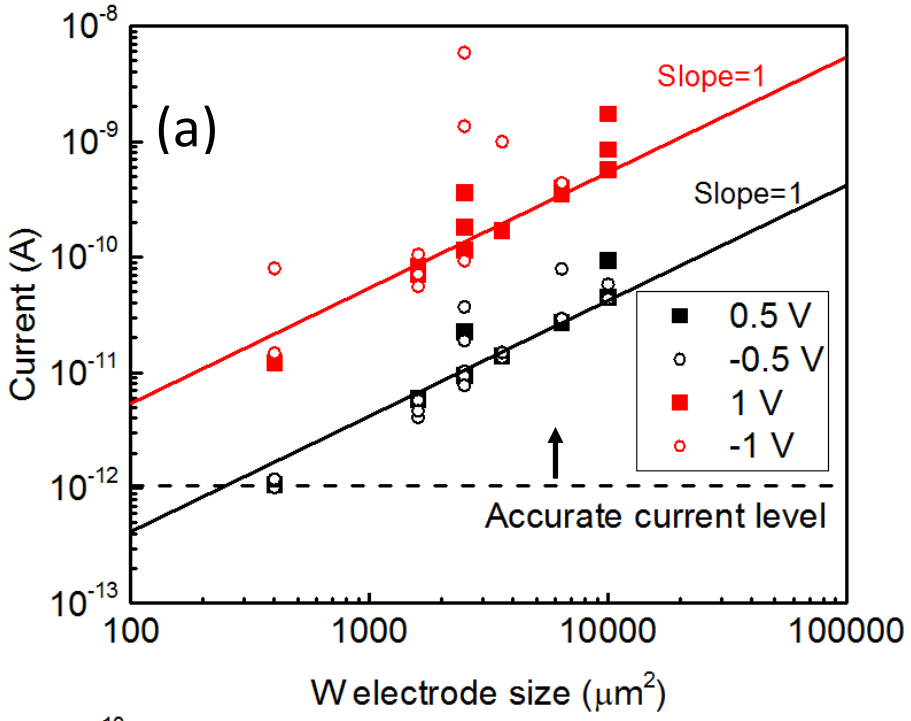


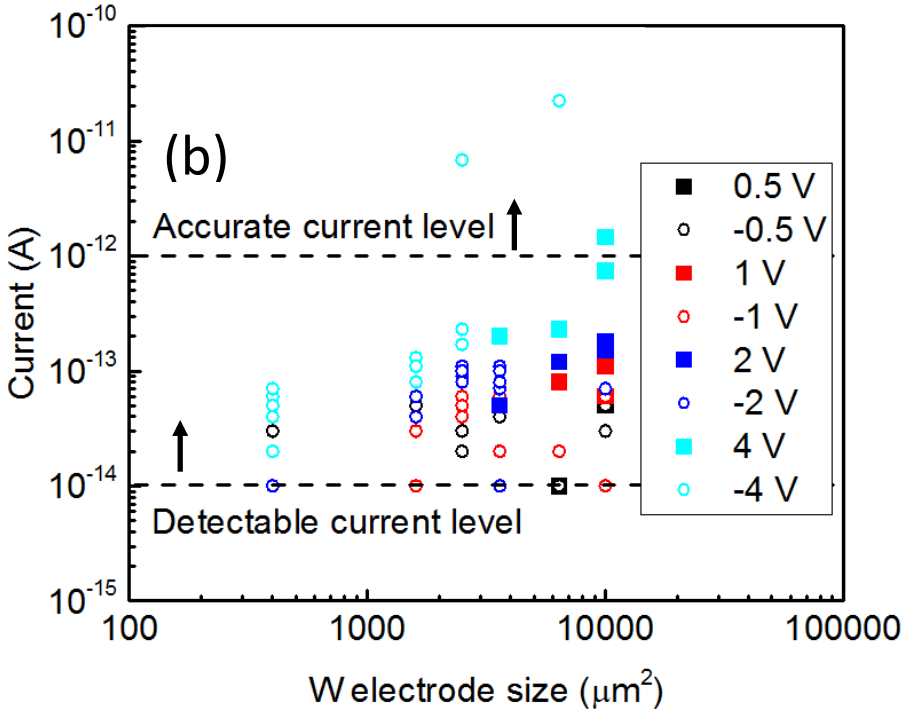
Figure 6-7. (a) Device chip of W/a-SiC:H/Cu resistive memories. (b) W electrodes on the a-SiC:H insulating layer. (c) SEM cross-section image of a W/a-SiC:H/Cu device structure.

6.2.2 Current dependence on W electrode area

Area dependence of the current of pristine W/a-Si(O)C:H/Cu devices was measured to verify the fabrication quality of the W electrodes of pristine a-Si(O)C:H resistive memories. A low voltage in the range ±0.5 to ±4 V was applied to measure the current. A higher voltage such as ±5 V cannot be

applied in this measurement because it can stimulate the resistive-switching and qualitatively alter the electrical properties of the pristine W/a-Si(O)C:H/Cu devices. Figure 6-8a, b, and c show the current vs W electrode area of pristine a-SiC:H, a-SiOC:H, and a-SiCO:H devices, respectively. Current of pristine W/a-SiC:H/Cu and W/a-SiCO:H/Cu devices fit a straight lines with slope=1 in the double logarithmic plot, indicating the current is proportional to the W electrode area. This suggests that the current distribution from the W electrodes to the a-SiC:H and a-SiCO:H films is uniform. The current of the pristine W/a-SiOC:H/Cu devices were lower than the current resolution 10^{-12} A of our equipment as mentioned in Chapter 3.3.2, because the high resistance of the pristine W/a-SiOC:H/Cu devices. Capacitance vs W electrode area of pristine W/a-Si(O)C:H/Cu devices was required to confirm uniform behaviour.


(a)
Slope=1
Slope=1
0.5 V
-0.5 V
1 V
-1 V
Accurate current level
Current (A)
W electrode size (μm²)


(b)
Accurate current level
Detectable current level
0.5 V
-0.5 V
1 V
-1 V
2 V
-2 V
4 V
-4 V
Current (A)
W electrode size (μm²)

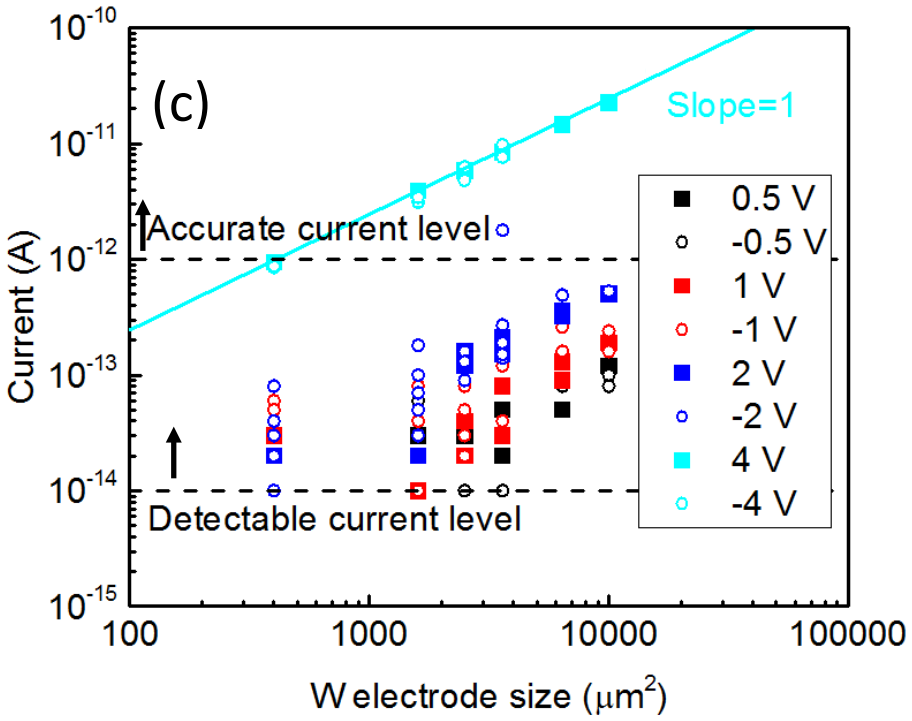


Figure 6-8. Current as function of W electrode area for pristine (a) a-SiC:H, (b) a-SiOC:H, and (c) a-SiCO:H devices, with respective linear fits.

6.2.3 Capacitance vs W electrode area

Capacitance of pristine W/a-Si(O)C:H/Cu devices were measured at 1 MHz as described in Chapter 3.3.1. Figure 6-9 shows the capacitance vs W electrode area of the pristine W/a-Si(O)C:H/Cu devices. The capacitance of all the pristine devices is proportional to the W electrode area as expected. The dielectric constant of the a-Si(O)C:H films was extracted from the proportionality factor of capacitance-area dependence. The dielectric constant of a-SiC:H, a-SiOC:H, and a-SiCO:H was 5.3 to 5.9, 4.0 to 4.3, and 4.1 to 4.2, respectively. The dielectric constant values of a-Si(O)C:H films in the range 4.0 to 5.3 distinguish them from the porous a-SiOC:H (k≈3.1-3.3) and consistent with the prior measurement of non-porous a-Si(O)C:H [175]. In low-frequency (1 MHz), the dielectric constant consists of three components being electronic, ionic, and orientation polarisation [83, 136]. The dielectric constant resulting from electronic polarisation is equal to the square of the refractive index [136], which is about 5.1, 2.5, and 3.3 for a-SiC:H, a-SiOC:H, and a-SiCO:H, respectively. The O at% of a-SiC:H, a-SiOC:H, and a-SiCO:H estimated from our XPS analysis is 1.3-1.6 at%, 46.4-47.8 at%, and 27.9-29.1 at%, respectively, as shown in Table 6-1. The electronic polarisation contributed dielectric constant decrease as the O at% increase which is attributable to more Si-C bonds are replaced with Si-O bonds [175]. Also, the difference between low-frequency dielectric and electronic polarisation contributed dielectric constant is lowest for a-SiC:H and

highest in a-SiOC:H which is attributable to the increase of O concentration which leads to higher ionic and dipolar polarisation contribution to the dielectric constant [136].

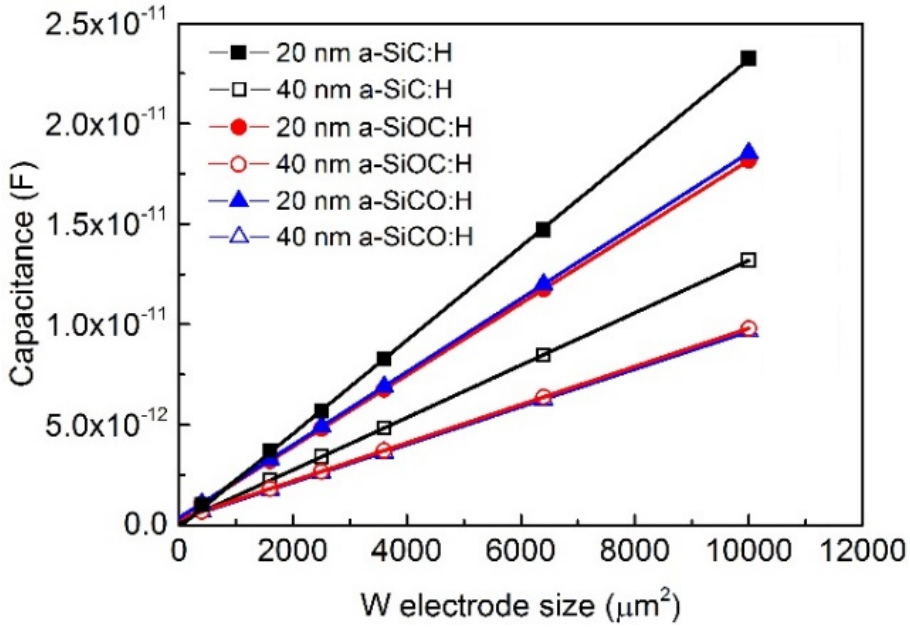


Figure 6-9. Capacitance vs W electrode area of pristine W/a-Si(O)C:H/Cu device, with respective linear fits.

6.2.4 Conduction mechanism of pristine a-SiOC:H device

Schottky emission conduction has been identified as the dominate conduction mechanisms in the HRS of a-SiC resistive memories and the origin of the ultra-high HRS resistance. The resistance of the Schottky contact is largely determined by the SBH. Usually, the resistance of resistive memories in HRS is lower than the resistance in the pristine state. Hence it is interesting to understand the pristine conduction mechanism which helps to understand the HRS conduction mechanism and switching mechanisms. Current density-voltage (J-V) characteristics of pristine W/a-Si(O)C:H/Cu devices were plotted in the Ln(J)-√V scale as shown in Figure 6-10. The Ln(J) of pristine a-SiC:H and a-SiOC:H fit with straight lines indicates reverse bias Schottky emission dominates the conduction mechanism, according to the Equation 2.3. The Schottky barrier height (SBH) of a-SiC:H, was extracted to be 0.94 V for both +V and -V. The SBH of a-SiCO:H devices was extracted to be 1.21 for both +V and -V. Despite the work function difference between Cu (4.9 eV) and W (4.5 eV), the SBH values were similar when applying +V and –V on the W electrode, for a-SiC:H and a-SiCO:H devices. This may relate to strong Fermi level pinning effect in a-Si(O)C:H due to the existence of defects [169] and strong covalent bonding [176]. The conduction mechanism and SBH of a-SiOC:H devices cannot be accurately determined as the current of pristine a-SiOC:H devices was below the 10^{-12} A. The high resistance of pristine a-SiC:H and a-SiCO:H devices was attributed to the large SBHs. The

even higher resistance of the pristine a-SiOC:H devices is attributable to an even higher SBH. XPS analysis was applied to further investigate the SBH of a-Si(O)C:H films.

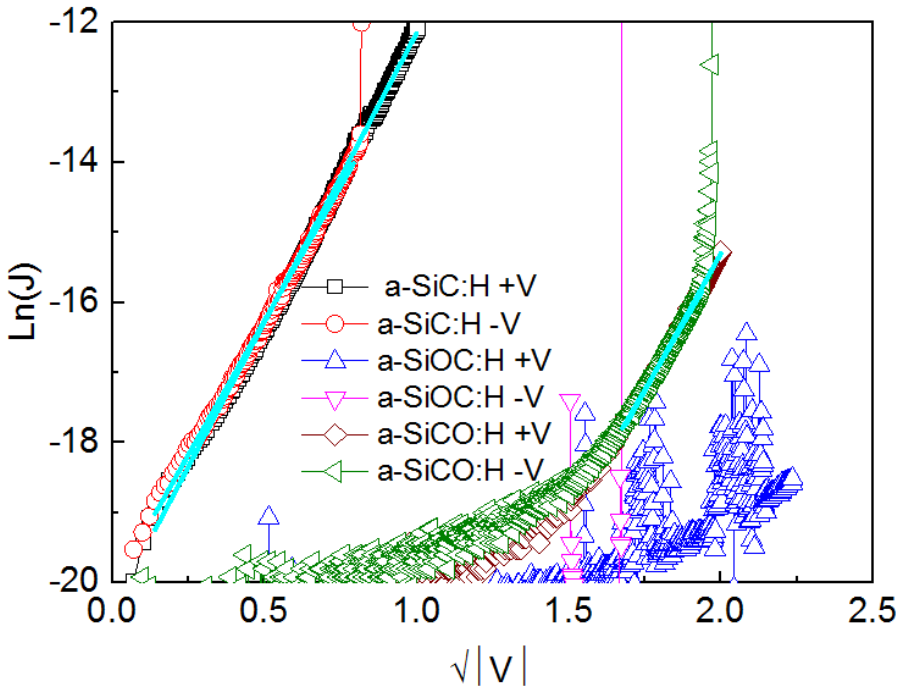


Figure 6-10. Ln(J)- √V characteristics of pristine W/a-SiC(O):H/Cu devices, when applying –V and +V were applied to the W electrode, with respective linear fits.

6.2.5 X-ray Photo-electron Spectroscopy measurement of Schottky barrier height

XPS analysis as described in Chapter 3.2.6 was applied to extract the SBH of a-Si(O)C:H/Cu Schottky contacts. E_g of 20 nm and 40 nm a-Si(O)C:H films determined from VASE analysis, VBM and Si 2p core level in the XPS spectra of 20 nm a-Si(O)C:H films on Cu, and Si 2p of 5 nm a-Si(O)C:H films on Cu in the literature were used in the calculation of SBHs. The SBHs extracted from XPS analysis and J-V analysis, were compared to further investigate the conduction mechanism of pristine a-Si(O)C:H devices.

Figure 6-11 shows the valence band spectrum in the XPS survey spectra for 20 nm a-Si(O)C:H films on 300 nm Cu coated substrates. The valence band is predominantly composed of C 2p, O 2p, and Si 3s states. The valence band spectra of a-SiC:H and a-SiCO:H films are resemblance to the valence band spectra obtained by King [82]. The valence band spectrum of the a-SiOC:H film is similar to the valence band spectra of a-SiO_2 obtained by King [82], but has lower valence band maximum (VBM) which is attributable to the adding of carbon component. The "carbon doping" in a-SiO_2 introduces into valence band additional states and lower binding energies [82]. Position of the valence band maximum (VBM) were extracted using extrapolation of the linear part to counts=0. The VBM for the a-SiC:H, a-SiOC:H, and a-SiCO:H is -0.31 eV, 0.96 eV, and 0.34 eV, respectively. The

negative VBM is clearly unphysical and is attributed to charge shift. Although the VBM values do not reflect the real difference between VBM and Fermi level of a-Si(O)C:H films due to surface charge, the Si 2p peak position would shift the same among value hence the relative position between the VBM and Si 2p peaking is not affected by the charge shift [123].

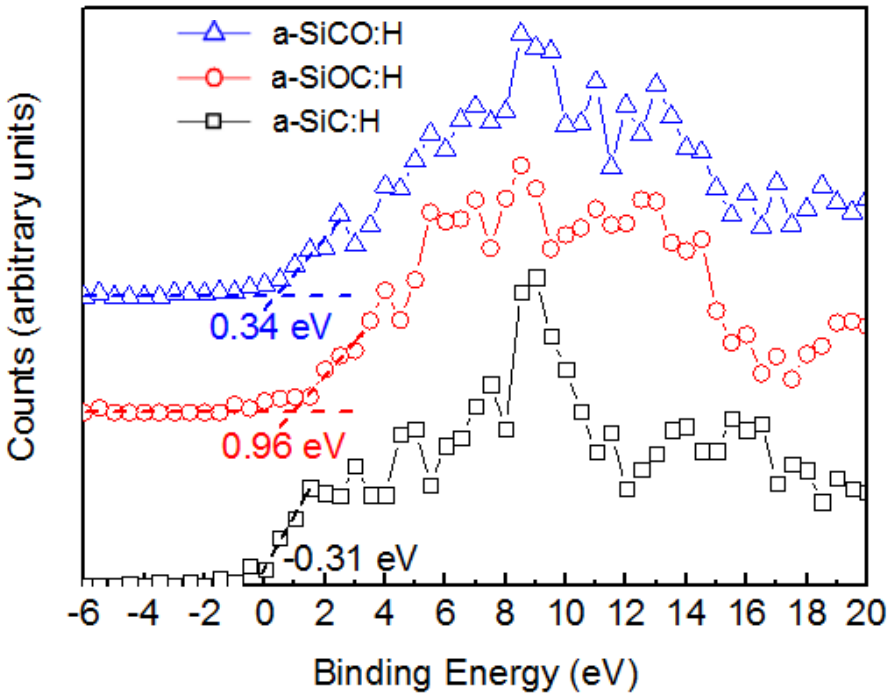


Figure 6-11. Valence Band Maximum region in the XPS survey spectra of 20 nm a-Si(O)C:H films, with respective linear fits.

Figure 6-12 shows the Si 2p peaks in the XPS survey spectra of 20 nm a-Si(O)C:H films on Cu coated substrates. The Si 2p core-level was determined to be 99.7 eV, 102.2 eV, and 101.4 eV for a-SiC:H, a-SiOC:H, and a-SiCO:H using a single Gaussian-Lorentzian function. Although using single Gaussian-Lorentzian function is not accurate, the errors of core-level position will not quantitatively affect the XPS measurement of SBH [123].

The peak position of Si 2p of 5 nm a-Si(O)C:H films on Cu in the literature was used in the XPS measurement of SBH. The Si 2p peak position at 100.9 eV of a-SiC:H [123], 102.8 eV of a-SiO_2 film [82], and 102.35 eV of a-$SiO_{0.55}C_{0.7}$ film [82] was used in the calculation of the SBHs of a-SiC:H, a-SiOC:H, and a-SiCO:H Schottky contacts, respectively. The difference between conduction band minimum (CBM) and Fermi level and the difference between VBM and Fermi level are the SBH Φ_B for electron and hole, respectively [123].

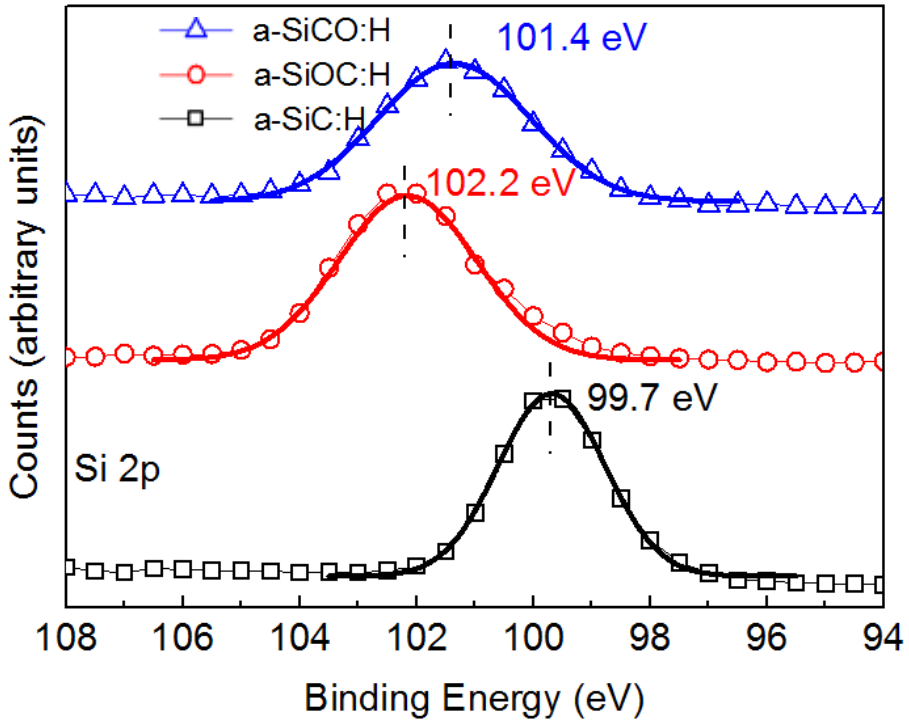


Figure 6-12. Si 2p patterns in the XPS survey spectra of 20 nm a-Si(O)C:H films.

The electron SBH and hole SBH of the a-Si(O)C:H/Cu Schottky contacts, were calculated using the values of E_g, $(Si\ 2p\text{-}VBM)_{bulk}$, and $(Si\ 2p)_{int}$ previously determined, and Equation 3.6 and 3.7. The values of E_g were determined from VASE measurements of 20 nm and 40 nm a-Si(O)C:H films. All the values used in the calculation of SBHs, and the calculated SBHs are summarised in Table 6-5. The values of SBHs extracted from Ln(J)-√V analysis of pristine a-Si(O)C:H devices was also listed in Table 6-5 for comparison. The VBM extracted from the XPS measurement is 0.8 eV to 0.9 eV and 1.1 eV to 1.3 eV for a-SiC:H and a-SiCO:H, respectively, which is close to the SBHs of extract from the Ln(J)-√V analysis. This indicates the a-SiC:H and a-SiOC:H films is possible p-type doped which is attributable to the O contents that acting as an acceptor in SiC [87]. Figure 6-13 Shows the schematic of band alignment at the a-Si(O)C:H/Cu interfaces plotted using the calculated electron SBH and hole SBH. The estimated position of CBM and VBM relative to the Fermi level at the a-Si(O)C:H/Cu interfaces is consistent with the values reported for a-Si(O)C:H/Cu Schottky contacts in the literature [82, 123]. The estimated position of CBM relative to the Fermi level is higher than the estimated position of VBM relative to the Fermi level, at the a-Si(O)C:H/Cu Schottky contacts.

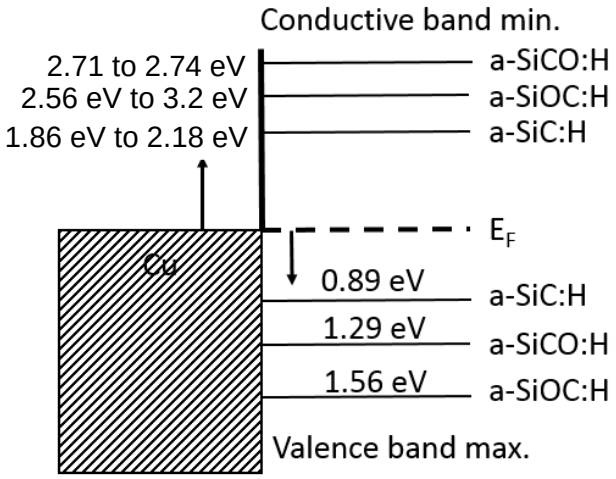


Figure 6-13. Band alignment at a-Si(O)C:H/Cu Schottky contacts.

Table 6-5. Schottky barrier height (SBH) estimated using I-V analysis and XPS measurement.

Dielectric	Si 2p at Interface (eV)	VBM in bulk (eV)	Si 2p in bulk (eV)	Band gap (eV)	Electron SBH (eV)	Hole SBH (eV)	SBH from Ln(J)- √ V (eV)
a-SiC:H	100.9 [123]	-0.31	99.7	2.75-3.07	1.86-2.18	0.89	0.93-0.94
a-SiOC:H	102.8 [82]	0.96	102.2	4.12-4.76	2.56-3.20	1.56	>1.21
a-SiCO:H	102.35 [82]	0.34	101.4	4.00-4.03	2.71-2.74	1.29	1.20-1.21

6.2.6 Modelling

The equivalent circuit model was built to further investigate the conduction mechanism of pristine W/a-Si(O)C:H/Cu devices. The knowledge on the conduction mechanism of pristine W/a-Si(O)C:H/Cu can be used in the comparison with conduction mechanisms in LRS and HRS to deduce the switching mechanism of a-Si(O)C:H resistive memories. Also, it is interesting from a general scientific point of view to investigate the conduction mechanisms of a MIM device structure i.e. pristine W/a-Si(O)C:H/Cu. Current conduction in the pristine W/a-Si(O)C:H/Cu devices is modelled in the following.

The MIM device structure of pristine W/a-Si(O)C:H/Cu devices was composed of two Schottky contacts, i.e. W/a-Si(O)C:H and a-Si(O)C:H/Cu. The current conduction of pristine W/a-Si(O)C:H/Cu devices was previously found dominated by reverse bias Schottky emission. Symmetric J-V characteristics were also observed when +V and –V were applied on the W electrode indicating that the two Schottky contacts were contacted back-to-back in the MIM device structure [177]. Figure

6-14a shows the DC equivalent circuit of a pristine W/a-Si(O)C:H/Cu device. The two Schottky diodes were connected by the bulk a-Si(O)C:H resistor. The a-Si(O)C:H Schottky contacts were modelled in the equivalent circuit as two p-type Schottky diodes because the SBH extracted from the Ln(J)-√V analysis was closer to the hole SBH measured using the XPS. The band diagram of a pristine W/a-Si(O)C:H/Cu device is plotted assuming the a-Si(O)C:H is p-type doped, as shown in Figure 6-14b. The current was dominated by the hole current because the electron SBH was found much higher than the hole SBH [178]. When +V was applied on the W electrode, and Cu was grounded, holes were injected from the W electrode into a-Si(O)C:H through reverse biased Schottky emission which forms the current through the W/a-Si(O)C:H junction $I_{Reverse}$. The current conduction of holes in the p-type bulk a-Si(O)C:H follows Ohmic conduction, which forms the current through the bulk of a-Si(O)C:H I_{Bulk}. Also, the holes were emitted from a-Si(O)C:H to Cu by forward bias Schottky emission, which forms the current pass through the a-Si(O)C:H/Cu junction $I_{Forward}$.

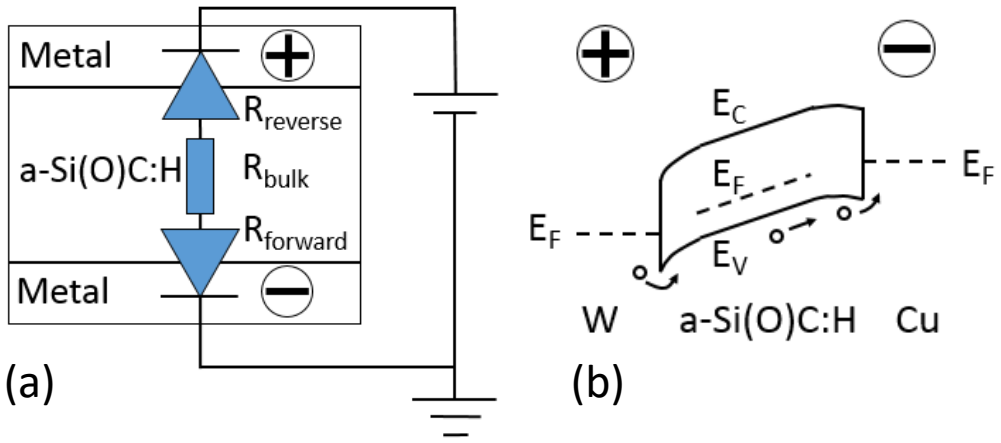


Figure 14. (a) Equivalent circuit and (b) band diagram of a pristine W/a-Si(O)C:H/Cu device.

The resistance contributed from the bulk a-Si(O)C:H resistor and Schottky contact in forward bias, is negligible compare with the resistance of the Schottky contact in reverse bias. This can be directly observed by comparing the I_{Bulk}, and $I_{Forward}$ of a-Si(O)C:H devices with the measured current of pristine a-Si(O)C:H devices which was dominated by the $I_{Reverse}$. The I_{Bulk} and $I_{Forward}$ were calculated using Equation 6.2 [179] and 6.3, respectively,

$$I = AA^{*}T^{2}\exp(\frac{-q\Phi_B}{kT})\exp(\frac{qV}{kT} - 1). \quad (6.2)$$

$$I = \frac{V}{R} = V/(\frac{\rho d}{A}), \quad (6.3)$$

where A is the area of W electrode, T is the temperature, q is the charge of single electron, k is the Boltzmann constant, R is the resistance of the bulk resistor, ρ is the resistivity of the a-Si(O)C:H film, and d is the thickness of the bulk a-Si(O)C:H. The measured SBH of a-SiC:H and a-SiC Schottky

contacts were used in the calculation. Also, the resistivity of a-SiC:H, a-SiCO:H was estimated between 7.66 10^6 Ohm-m of a-SiC [46] and 10^{12} Ohm-m of SiO_2 [66, 180]. All the parameters used in the calculation are listed in Table 6-6. The calculated I_{Bulk}, and $I_{Forward}$ were compared with the I-V characteristics of the pristine a-SiC:H and a-SiCO:H devices, as shown in Figure 6-15a and b, respectively. It is clear that $I_{Forward}$ exceeds the measured current by orders of magnitudes at voltage > 0.3 to 0.5 V. Also, the I_{Bulk} is orders of magnitudes higher than the measured current unless the estimated resistivity was increased to approximately 10^{12} Ohm-m which is the resistivity of SiO_2. According to the current continuity requirement, $I_{Reverse}=I_{Bulk}=I_{Forward}$. Hence the resistance of the bulk resistor and the Schottky contact in forward bias, is negligible compared with the resistance of the Schottky contact in reverse bias. As a result, it is valid to only consider the reverse bias Schottky emission in the current conduction analysis of pristine W/a-Si(O)C:H/Cu devices.

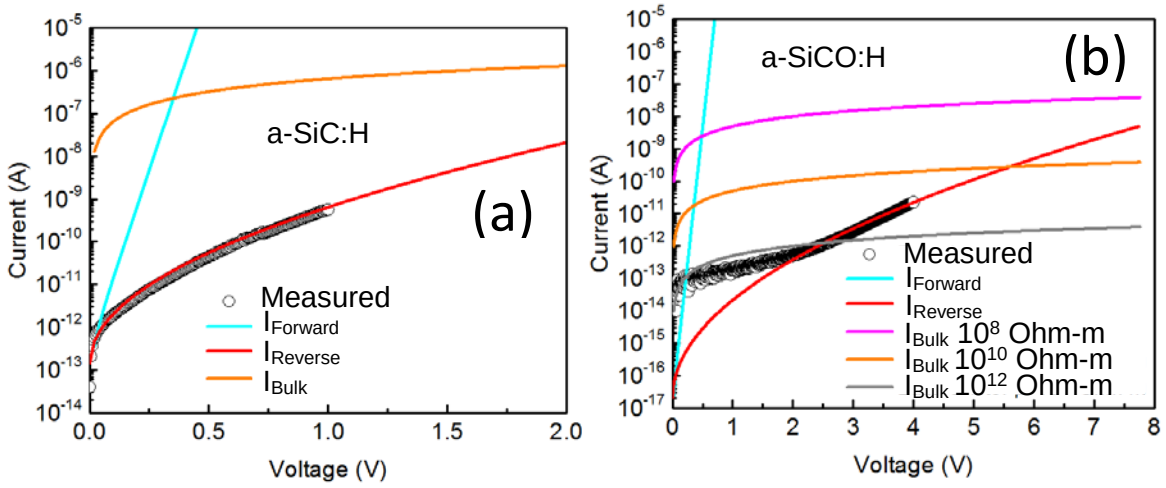


Figure 6-15. The calculated I_{Bulk} and $I_{Forward}$ of pristine (a) a-SiC:H and (b) a-SiCO:H devices.

Table 6-6. Parameters used in the I-V calculation of pristine a-SiC:H and a-SiCO:H devices.

Parameters	a-SiC:H	a-SiCO:H
Bulk thickness d	20 nm	20 nm
Reverse biased interface thickness	5.7 nm	10.8 nm
Schottky barrier height (eV)	0.95	1.18
Top electrode size A (μm^2)	10000	10000
Bulk resistivity (Ohm-m)	10^6	10^8 to 10^{12}

6.3 Resistive-switching of a-Si(O)C:H RMs

Resistive-switching in the bipolar mode has been observed from W/a-Si(O)C:H/Cu devices that have a-SiC:H, a-SiOC:H, and a-SiOC:H insulating layers. The DC I-V characteristics of the a-SiC:H, a-SiOC:H, and a-SiOC:H devices was measured to show the bipolar switching behaviour. Endurance and

retention of a-Si(O)C:H devices were measured to show the repeatable and non-volatile characteristics of the bipolar switching. Current conduction in LRS and HRS was analysed to investigate the switching mechanisms. Also, V_{FORM}, V_{SET}, and V_{RESET} of a-SiC:H, a-SiOC:H, and a-SiCO:H devices were compared to investigate the influence of the material properties of the a-Si(O)C:H insulating layer on switching characteristics.

6.3.1 Bipolar resistive-switching

Figure 6-16a and b show the first and subsequent switching cycles of a-SiC:H, a-SiOC:H, and a-SiCO:H devices. All the three devices have identical 50 µm x 50 µm device area and 40 nm thickness of a-Si(O)C:H insulating layer for comparison. The first switching cycle is recognised as the electroforming cycle for the resistive memories, because V_{FORM} in the first cycle is generally higher than the V_{SET} in the subsequent cycle. The electroforming cycle is widely observed in ECM resistive memories and is caused by the need to generate the conductive paths through the entire thickness of the insulator layer [10, 63]. Sometimes, V_{FORM} lower than V_{SET} was also observed for a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories, but this was atypical.

In Figure 6-16a, a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories were switched from the pristine state into the LRS by a -5.2, -7.2, and -7.5 V V_{FORM}, respectively. A 100 µA current compliance was applied in the electroforming process to prevent the devices from permanent breakdown. The LRS current was then measured in a low voltage range without applying the current compliance. Next, the a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories were RESET from LRS to HRS by a 1.5 V, 0.7 V, and 4.7 V V_{RESET}, respectively. A bipolar switching cycle was completed. The same procedure was repeated in the subsequent cycle to switch the a-Si(O)C:H resistive memories between HRS and LRS, as shown in Figure 6-16b. The V_{SET} in Figure 6-16b is -2.7 V, -7.1 V, and -2.4 V for a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories, respectively. The V_{RESET} in Figure 6-16b is 0.5, 1.1, 0.3 V for a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories, respectively. The voltage was applied to the W electrode instead of the Cu electrode because Cu was connected to the substrate of the device chip and common to all the devices on the same chip. Applying a large voltage on the Cu electrode could accidentally damage the insulating layer on nearby W/a-SiC(O)C:H/Cu devices. Hence the polarity of V_{FORM}, V_{SET}, and V_{RESET} is opposite to the corresponding voltage of bipolar switching in the literature, where the voltage was applied to the Cu electrode on top of the device. No difference in resistive-switching behaviour is expected to be caused by such measurements as voltage is a relative quantity.

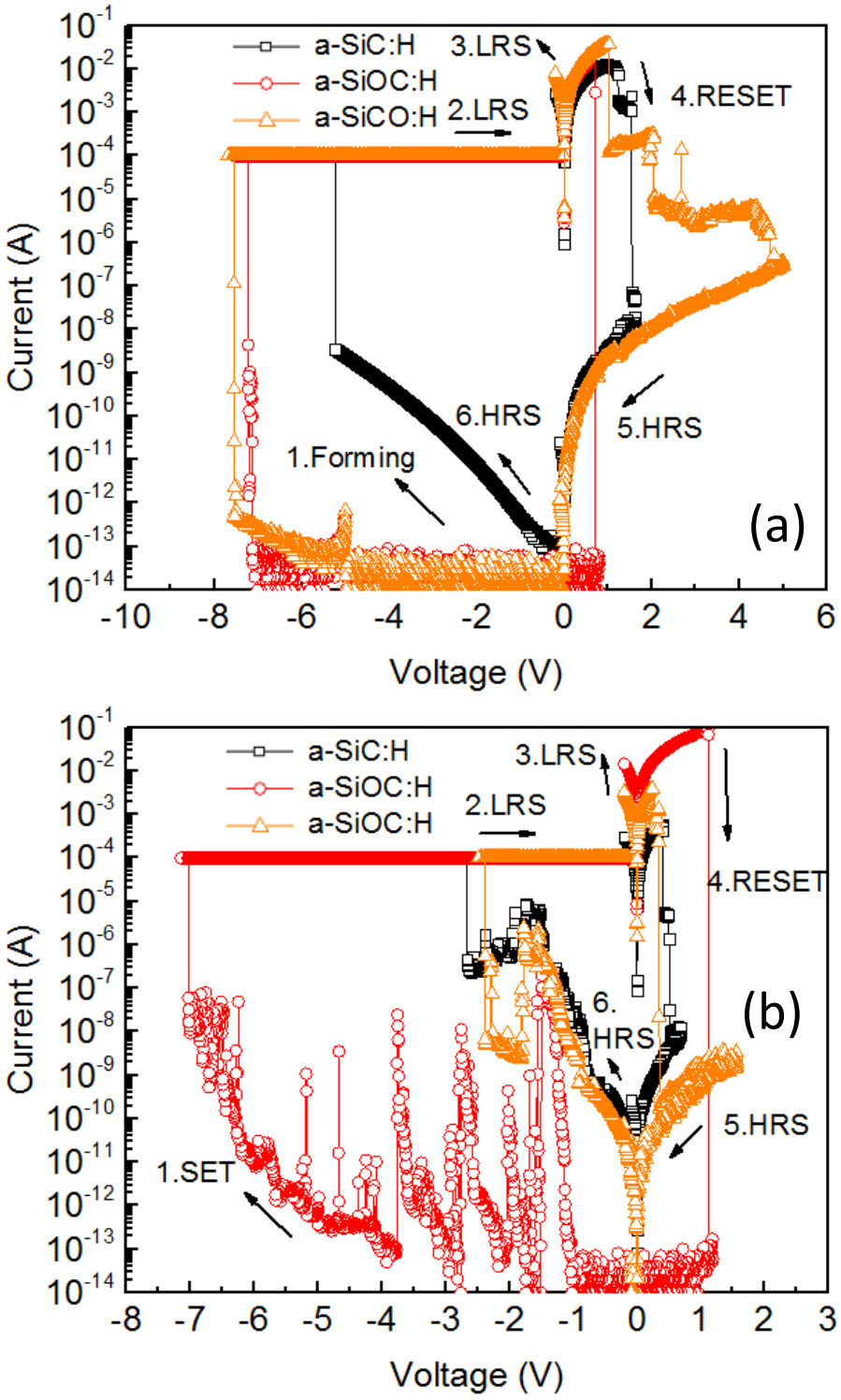


Figure 6-16. Bipolar switching, I-V characteristics of a-Si(O)C:H resistive memories. (a) Electroforming cycle and (b) subsequent cycle.

Ultra-high ON/OFF ratios were observed in the bipolar switching of a-Si(O)C:H resistive memories. The ON/OFF ratio at -0.1 V in Figure 6-16a is 5.4×10^{7}, 2.9×10^{11}, and 3.3×10^{9} for the a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories, respectively. ON/OFF ratio at -0.1 V in Figure 6-16b is 5.8×10^{5}, 3.7×10^{11}, and 2.6×10^{8}, for the a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories,

respectively. Although the ON/OFF ratios in the subsequent cycle are generally lower than the electroforming cycle, the values in the range 5.8×10^5 to 3.7×10^{11} are still higher than typical ON/OFF ratio $<10^4$ for the majority of resistive memories that have other materials as the insulating layer [173] and is comparable with other Cu/a-SiC/Au resistive memories.

Similar bipolar switching I-V characteristics were measured from resistive memories with 20 nm a-Si(O)C:H thickness. However, the number of 20 nm a-SiC:H resistive memories that shown repeated bipolar switching was very low. Most 20 nm a-SiC:H devices were only able to switching from pristine state to LRS and not able to RESET. The origin of this phenomenon will be discussed later.

Figure 6-17 shows the endurance of bipolar switching of an 20 nm a-SiOC:H resistive memory. This device was repeatly switched using the DC I-V measurement as described above for 21 cycles. This is one of the highest endurance observed so far from a-Si(O)C:H resistive memories using DC I-V measurement. ON/OFF ratios was on average 10^8 over the 21 cycles. One switching error where a LRS was close to HRS was observed among 21 cycles. While the switching cycles measured from most a-Si(O)C:H resistive memories in this thesis are in the range 1-10. Higher record for the repeating times are expected in optimised pulsed switching measurements.

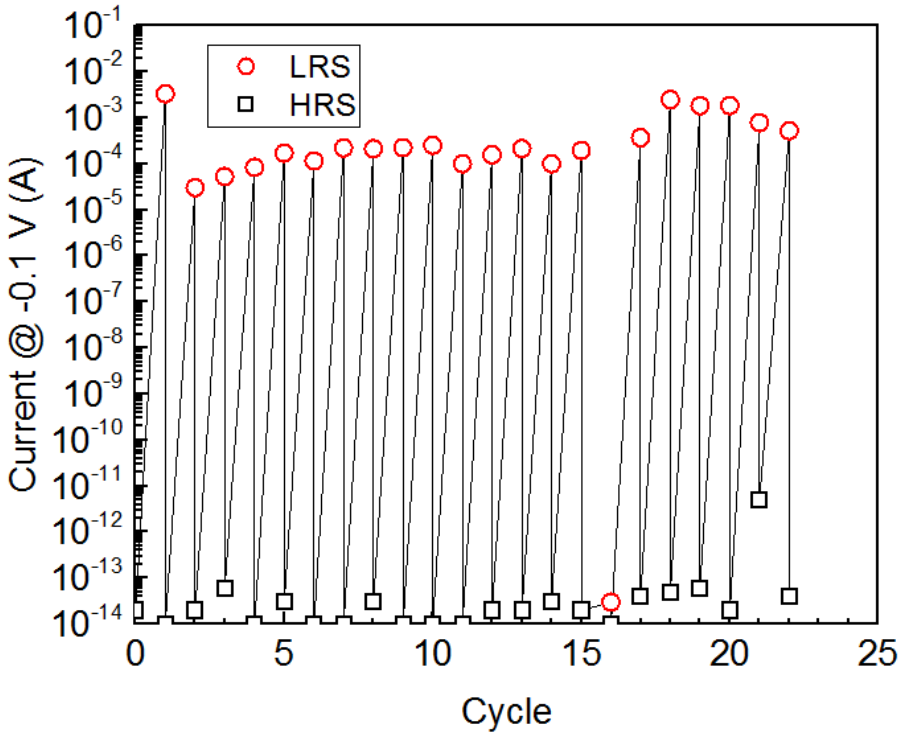


Figure 6-17. Endurance of switching of an W/20 nm a-SiOC:H/Cu resistive memory.

Non-volatile characteristics of the resistive memories were assessed by room temperature retention measurement, as shown in Figure 6-18. Two identical a-Si(O)C:H resistive memories were used in the retention measurement where with one device was SET to LRS and the other RESET to

HRS. No qualitatively variation of the LRS and HRS currents in the first 10^5 s after SET and RESET, respectively, could be observed in Figure 6-18. Large variation of LRS and HRS currents >10^5 s after SET and RESET was observed and is attributable to the damage of the devices by repeated probe positioning in the retention measurements. This indicates the a-Si(O)C:H devices possess a good retention. Long retention along with the high ON/OFF ratio in the 5.8 × 10^5 to 3.7 × 10^{11} range suggest promising application potentials of W/a-Si(O)C:H/Cu resistive memories.

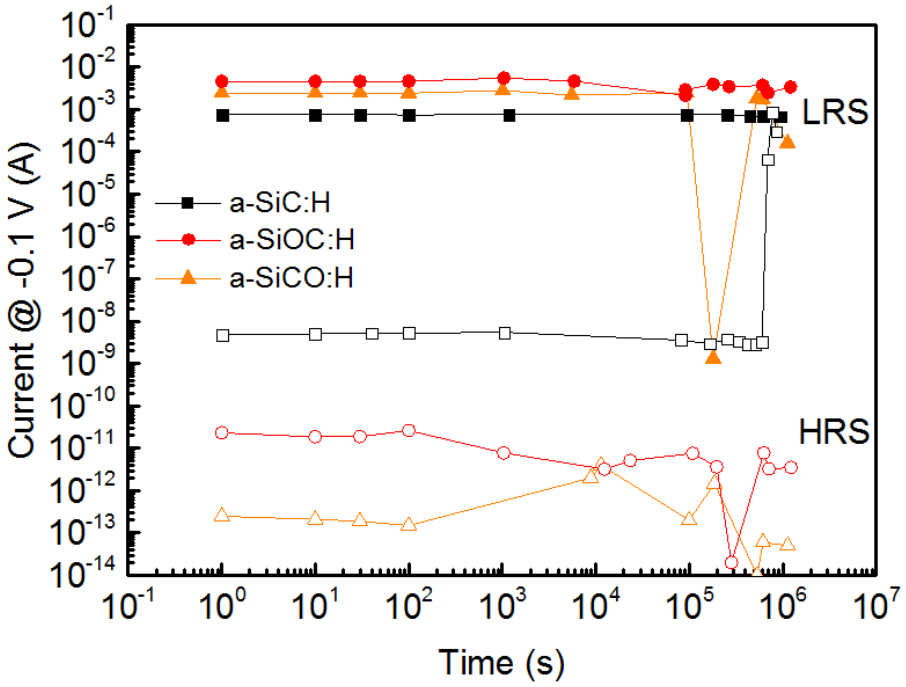


Figure 6-18. LRS and HRS retention of a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories.

6.3.2 Conduction mechanism in LRS

Detailed I-V characteristics of the a-Si(O)C:H resistive memories, in the LRS and HRS, were exploited to investigate the resistive-switching mechanism. Figure 6-19a shows the LRS I-V characteristics of the a-Si(O)C:H resistive memories. The slope of the straight lines fit the LRS I-V characteristics of the devices are all close to 1, indicating that Ohmic conduction is the main conduction mechanism in the LRS, where the current is proportional to the voltage. The Ohmic conduction in LRS is attributable to the formation of Cu conductive filament [9, 63]. Cu conductive filament in resistive memories with diameter around 10-20 nm has been reported from TEM [181, 182] and conductive-AFM [35] observations.

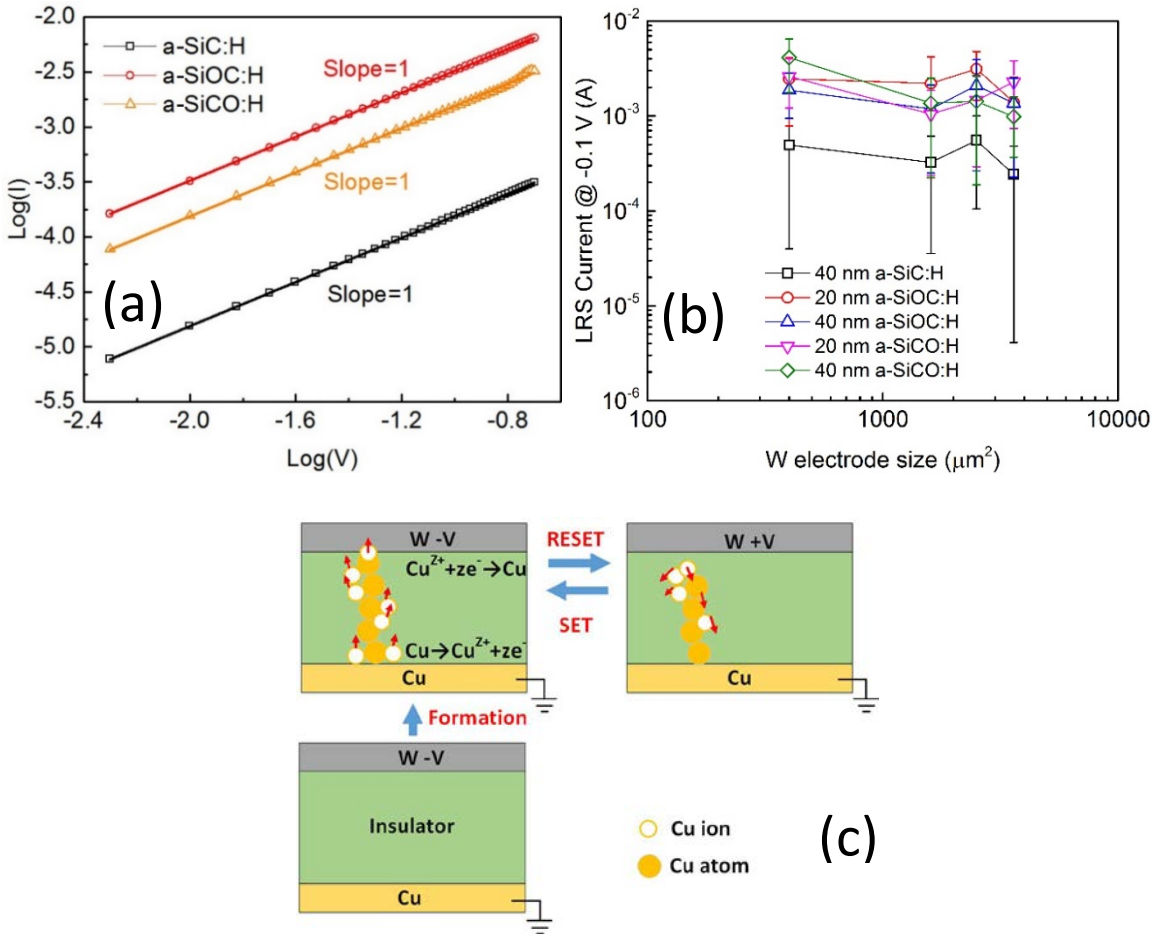


Figure 6-19. (a) Log(I-Log(V) of a-Si(O)C:H resistive memories in LRS, with respective linear fits. (b) LRS current vs W electrode area. The current was measured at -0.1 V. (c) Schematics of bipolar resistive-switching.

Figure 6-19b shows the LRS current vs W electrode area of the a-Si(O)C:H resistive memories. No noticeable area dependence could be observed from the LRS current of the a-SiC:H, a-SiOC:H, and a-SiCO:H devices, which is consistent with the Ohmic conduction contributed to a conductive filament [63, 159]. According to the well-known ECM switching mechanism, the formation of the conductive filament is attributable to the injection of active metal form the anode in the electroforming and SET processes [9, 63]. Figure 6-19c shows the schematic of bipolar switching of a-Si(O)C:H resistive memories. When the $-V_{FORM/SET}$ was applied to the W cathode, the Cu atoms at the Cu anode oxides into Cu^{Z+} cations $Cu \rightarrow Cu^{Z+}+Ze^-$. Subsequently, Cu^{Z+} cations were driven by the electric field across the Cu and W electrodes, and reduced to Cu atoms at the W cathode $Cu^{Z+}+Ze^- \rightarrow Cu$ [9, 63]. Eventually, the accumulated Cu atoms gradually grown into a Cu conductive filament, which switched the a-Si(O)C:H resistive memory to the LRS. In the bipolar switching, the RESET process was attributed the electrochemical dissolution of the Cu conduction filament. When the $+V_{RESET}$ was applied to the W cathode, the Cu atoms of the conduction filament migrated back to the Cu electrode in the way opposites to the growth of Cu conductive filament in the ECM process.

6.3.3 Conduction mechanism in HRS

Figure 6-20 shows the HRS I-V characteristics of the a-Si(O)C:H resistive memories in the √V-Ln(I) scale. The HRS I-V characteristics of the devices all fit straight lines in √V-Ln(I) scale, indicates reverse biased Schottky emission is dominating the current conduction in the HRS. The switching from Ohmic conduction in LRS to the Schottky emission conduction in the HRS suggests the rupture of the conductive filaments in the RESET process, as described in Figure 6-19c. The SBH of a-Si(O)C:H Schottky contacts in the HRS was calculated using Equation 2.3 and the intercept of the straight lines. The calculated SBH is 0.36 eV, 0.55 eV, and 0.42 eV for the a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories, respectively, assuming the Schottky contact area was 200 nm^2 which equals the area of conductive filament in the literature [35, 181]. The calculated SBH is 0.79 eV, 0.97 eV, and 0.84 eV for the a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories, respectively, assuming the Schottky contact area was 50 µm × 50 µm which equals the original area of the device. In both cases, the SBH in HRS is noticeably lower than the SBH in pristine state for a-Si(O)C:H resistive memories. This is attributable to the existence of Cu residual in the a-Si(O)C:H insulator layer [183]. Figure 6-20b shows the HRS current vs the W electrode area of a-Si(O)C:H resistive memories. The HRS current of the a-Si(O)C:H resistive memories, did not show area-dependence which is different from the current conduction of pristine a-Si(O)C:H devices which was also dominated by reverse bias Schottky emission. The change of area dependence of HRS current conduction is also attributable the existing of the residual conductive filament and indicates the residual conduction filament was not uniformly distributed in the a-Si(O)C:H insulating layer.

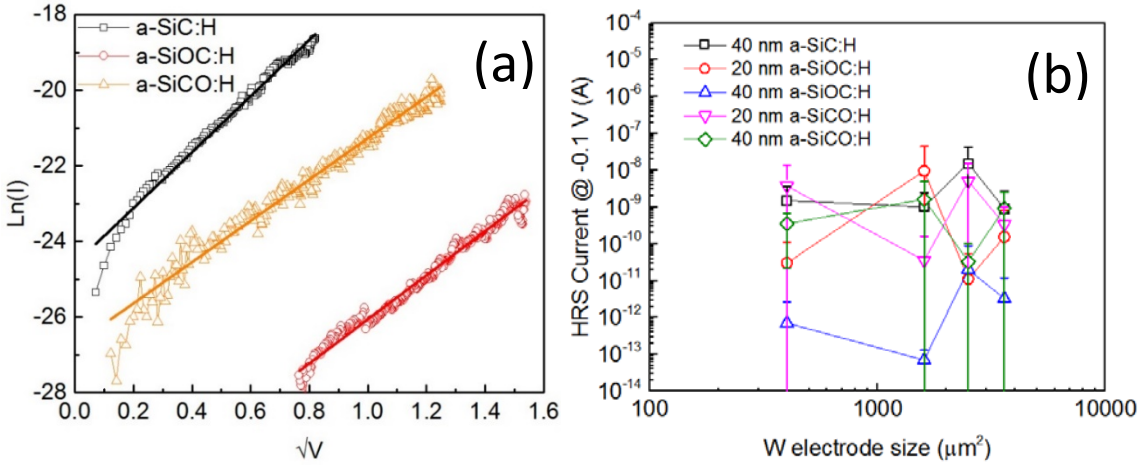


Figure 6-20. (a) HRS I-V characteristics of a-Si(O)C:H resistive memories in √V-Ln(I) scale, with respective linear fits. (b) HRS current vs W electrode area. The HRS current was measured at -0.1 V.

6.3.4 Influence of materials properties

V_{FORM}, V_{SET}, and V_{RESET} of the a-Si(O)C:H resistive memories with 20 nm and 40 nm a-Si(O)C:H thickness were compared in Figure 6-21 to investigate the influence of the material properties of the a-Si(O)C:H insulating layer on switching characteristics. An increase of V_{FORM} and V_{SET} with a-Si(O)C:H thickness could be observed in Figure 6-21a and 6-21b, respectively for a-SiOC:H and a-SiCO:H resistive memories. According to the ECM theory, there are three main rate-limiting processes in the formation of Cu conductive filament, i.e. oxidation-reduction of active metal, drift-diffusion of metal cation in the insulating layer, and nucleation of active metal into a conductive filament. The increase of V_{FORM} and V_{SET} with a-Si(O)C:H thickness suggest the ion migration process is a major rate limitation process in the electroforming and SET processes [184].

In addition, V_{FORM} of the a-SiOC:H and a-SiCO:H resistive memories, is noticeably higher than the V_{FORM} of the a-SiC:H resistive memories with the same 40 nm a-Si(O)C:H thickness. This suggests the electroforming process is dependent on the insulating material. While the difference of V_{SET} between the a-SiOC:H and a-SiCO:H resistive memories, and the a-SiC:H is less noticeable than the difference of V_{FORM}. This is attributable to the existence of residual conductive filament remained in the a-Si(O)C:H, which reduced the influence of insulating layer on the voltage require to form the Cu conductive filament.

Moreover, the material properties of the a-Si(O)C:H insulating layer also shown influence on whether an a-Si(O)C:H resistive memory can or cannot RESET, qualitatively. The a-SiC:H resistive memories were found rarely RESET when the a-SiC:H thickness was reduced from 40 nm to 20 nm, which did not happen on a-SiOC:H and a-SiCO:H resistive memories. The a-SiOC:H resistive memories with 20 nm thickness of the a-SiOC:H even presented the best endurance characteristics. It is possible that an exceeding amount of Cu atoms were injected into the thin a-SiC:H insulating layer in the electroforming process. For all the a-Si(O)C:H resistive memories that shown repeated RESET, the difference of the V_{RESET} is small, as shown in Figure 6-21a and 6-21b.

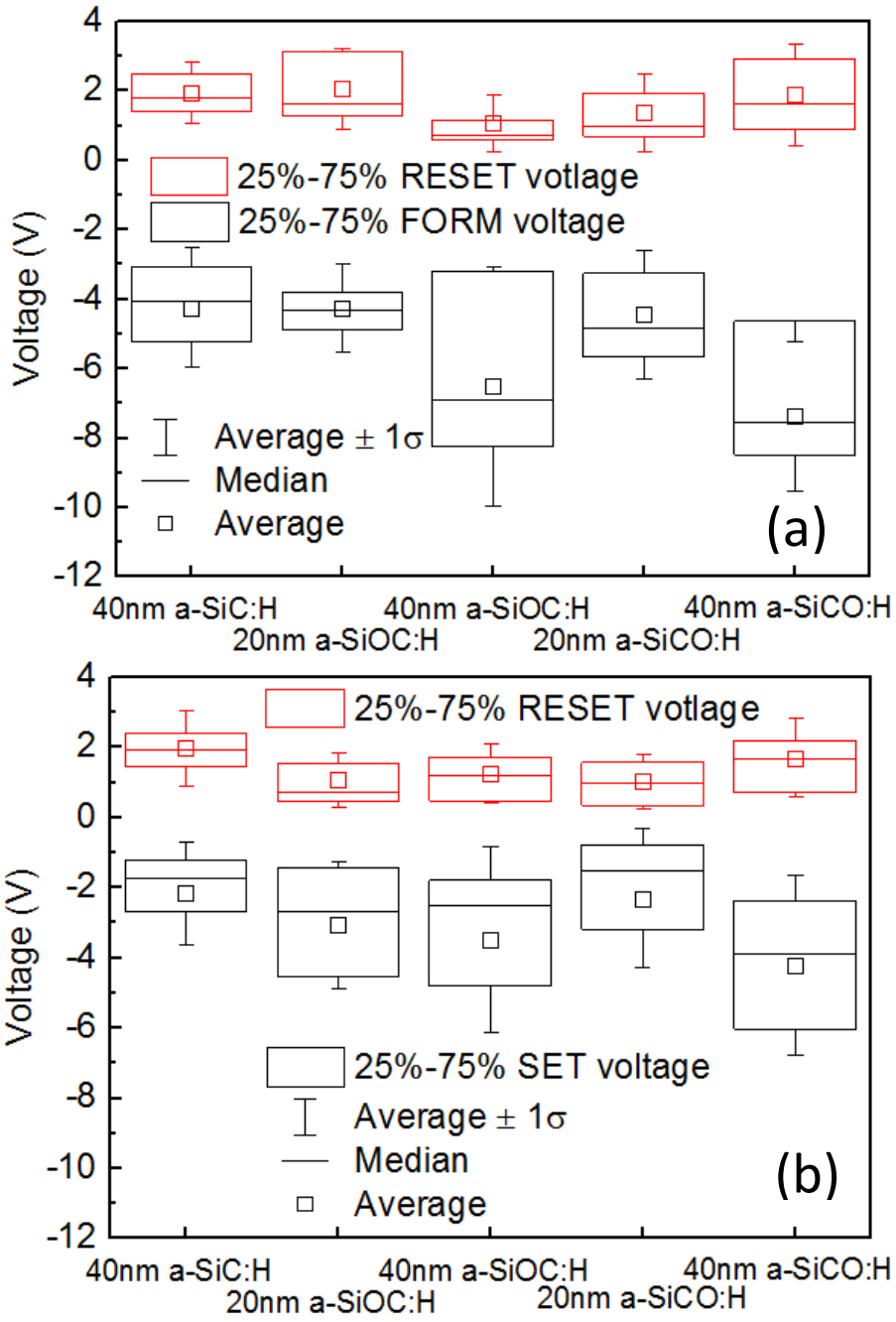


Figure 6-21. Boxplots of the (a) V_{FROM} and V_{RESET} in the electroforming switching cycles and (b) V_{SET} and V_{RESET} in the subsequent switching cycles of a-Si(O)C:H resistive memories.

6.3.5 Comparison between BEOL a-Si(O)C:H RMs and sputtered a-SiC and a-SiC:Cu RMs

The BEOL a-Si(O)C:H RMs in this Chapter, the sputtered a-SiC RMs in Chapter 4, and the sputtered a-SiC:Cu RMs in Chapter 5 all shown interesting resistive-switching behaviours. A quick comparison between BEOL a-Si(O)C:H RMs and sputtered a-SiC and a-SiC:Cu RMs are provided in the following. Table 6-7 compares fabrication and performance features of these RMs. The a-Si(O)C:H insulating layer was deposited using a high volume manufacturing PECVD tool. This makes BEOL a-Si(O)C:H RMs more advanced regarding BEOL compatibility than sputtered a-SiC and a-SiC:Cu RMs. However, this advantage is not unrivalled because the sputtering of a-SiC and a-SiC:Cu at room temperature is also BEOL compatible. While, one or two extra photolithography steps might be required in the fabrication of RMs using sputtered a-SiC or a-SiC:Cu instead of BEOL a-Si(O)C:H as the insulating layer compare to RMs using native BEOL a-Si(OC):H as the insulating layer.

The $|V_{SET}|$ and $|V_{RESET}|$ of BEOL a-Si(O)C:H RMs are in the range 2.2-4.5 V and 1.0-2.0 V, respectively, which are higher than the values 0.9-2.4 V and 0.5-1.3 V of a-SiC and a-SiC:Cu RMs. Lower V_{SET} and V_{RESET} of a-SiC and a-SiC:Cu RMs are more desired as the lower switching voltage could reduce power consumption in SET and RESET processes. Also, the lower switching voltage reduces the difference between switching voltage of RMs and supply voltage of logic devices which is normally <1 V. This can potentially reduce the complexity of peripheral circuit to supply voltage in two different voltage range in embedded systems.

The ON/OFF ratios of BEOL a-Si(O)C:H RMs is in the range 10^6-10^{11} which are higher than that 10^5-10^9 of sputtered a-SiC and a-SiC:Cu RMs. Higher ON/OFF ratio would lead to more stable read out of the stored data and require less complicated peripheral readout circuit.

Table 6-7. Comparison of fabrication and performance features of BEOL a-Si(O)C:H RMs and sputtered a-SiC and a-SiC:Cu RMs.

	BEOL a-Si(O)C:H RMs	Sputtered a-SiC and a-SiC:Cu RMs
Deposition method of the insulating layer	PECVD using a high volume manufacturing PECVD tool	Room temperature sputtering using a lab sputtering system
$\|V_{SET}\|/\|V_{RESET}\|$ (V)	2.2-4.5/1.0-2.0	0.9-2.4/0.5-1.3
ON/OFF ratio	10^6-10^{11}	10^5-10^9

Overall, both BEOL a-Si(O)C:H RMs and sputtered a-SiC and a-SiC:Cu RMs all have their strengths. While it is believed that there is still huge optimisation potential for both BEOL a-Si(O)C:H RMs and sputtered a-SiC and a-SiC:Cu RMs. Hence, it is too early to conclude whether BEOL a-Si(O)C:H RMs or sputtered a-SiC and a-SiC:Cu RMs are better. It was discussed in Chapter 4, 5, and 6 that the material properties of the sputtered a-SiC, a-SiC:Cu and the BEOL a-Si(O)C:H can be tuned in a wide range during the deposition. Resistive-switching with improved performance is expected to be obtained when a-SiC, a-SiC:Cu, or a-Si(O)C:H with optimised material properties are found in the future.

6.4 Summary

In this Chapter, material properties of the a-SiC:H, a-SiOC:H, and a-SiCO:H films were characterised and the influence of the materials properties of these a-Si(O)C:H films on the switching characteristics were analysed. The Chemical composition of the a-Si(O)C:H films were analysed using XPS. The a-SiC:H films was mainly composed of Si and C along with H shown in the NRA measurement. The a-SiCO:H films have more Si-C bonds than Si-O bonds, and the a-SiOC:H films have more Si-O bonds than Si-C bonds. Refractive index of the a-SiC:H, a-SiOC:H, and a-SiCO:H films, was measured to be 2.2, 1.6, and 1.8, respectively. The band gap E_g for a-SiC:H, a-SiOC:H, and a-SiCO:H was estimated to be 2.9 eV, 4.4 eV, and 4.0 eV, respectively.

W/a-Si(O)C:H/Cu resistive memories were fabricated. The W electrodes with area in the range 20 µm × 20 µm to 100 µm × 100 µm were patterned on the a-Si(O)C:H films. The current and capacitance of pristine a-Si(O)C:H devices were proportion to the W electrode area. The dielectric constant of a-SiC:H, a-SiOC:H, and a-SiCO:H insulating layers, was measured to be 5.6, 4.2, and 4.1, respectively. Current conduction of pristine a-Si(O)C:H devices were dominated by the reverse bias Schottky emission. The SBH of pristine a-SiC:H and a-SiOC:H devices were calculated to be 0.94 eV and 1.20 eV, respectively which is close to the SBH for holes at the a-Si(O)C:H/Cu Schottky contact estimated from XPS measurement. The pristine a-SiOC:H devices which have higher resistance than the capability of our equipment was expected to have an SBH >1.21 eV. An equivalent circuit which contains two head-to-head p-type Schottky diodes connected by a resistor was developed for pristine a-Si(O)C:H devices.

Resistive-switching in the bipolar mode has been observed from W/a-Si(O)C:H/Cu resistive memories. Long retention and high ON/OFF ratios in the 5.8×10^5 to 3.7×10^{11} range suggest promising application potentials of W/a-Si(O)C:H/Cu resistive memories. The Cu conductive filament in LRS leads to Ohmic conduction. The a-Si(O)C:H containing residual conductive filament

in HRS lead to reverse bias Schottky emission conduction mechanism and lower SBH compared to pristine state.

The material properties of the a-Si(O)C:H insulating layers have shown a variety of influence on the switching characteristics. An increase of V_{FORM} and V_{SET} with the a-Si(O)C:H thickness was observed. Also, V_{FORM} of a-SiOC:H and a-SiCO:H resistive memories was noticeably higher than the V_{FORM} of a-SiC:H resistive memories. While the difference of V_{SET} is much lower between a-SiC:H, a-SiOC:H, and a-SiCO:H resistive memories. Moreover, the material properties of the a-Si(O)C:H films have shown critical influence on whether the resistive memories can switch repeatedly or not. It is clear that material properties of the a-Si(O)C:H insulating layer have significant influence on the switching characteristics. It is promising to further optimise the switching characteristics of a-Si(O)C:H resistive memories using the material properties of the a-Si(O)C:H insulating layer as turn knob.

Chapter 7: Epitaxy crystalline SiC film and RMs

In this Chapter, material properties of crystalline SiC film were characterised and the switching behaviour of the c-SiC resistive memory were studied. The c-SiC film was grown on a Si substrate by Dr. Matteo Bosi from Institute of Materials for Electronics and Magnetism, Parma, Italy. The grown method was described in Chapter 3.1.3. After receiving the c-SiC film, thickness and refractive index of the c-SiC was measured using VASE. Cu electrodes were patterned on the c-SiC film to form the Cu/c-SiC/Si device structure, as described in Chapter 3.1.3. The I-V characteristics of the pristine Cu/c-SiC/Si devices and Cu/c-SiC/Cu devices were measured to investigate the conduction mechanism. The I-V characteristics of resistive-switching in the bipolar mode were measured from a c-SiC resistive memory. The ON/OFF ratios, and V_{FROM}, V_{SET} of the c-SiC resistive memory, were compared with a-SiC resistive memories to investigate the influence of crystallinity on the switching characteristics. Conduction mechanism in LRS and HRS of the c-SiC resistive memory were exploited to evaluate the switching mechanism.

7.1 Thickness and refractive index

VASE measurement was conducted on the c-SiC film on Si substrate to measure the film thickness and refractive index. Knowing the thickness of c-SiC films helps the analysis of switching voltage of c-SiC films because both the electric field and the length of the conductive filament in resistive memories are usually dependent on the thickness of the insulating layer. Also, knowing the refractive index helps to understand the microstructure of the c-SiC film. Figure 7-1 shows the thickness map of the c-SiC film on Si substrate. Thickness gradients on the X-axis and Y-axis direction were observed. In the Y-axis direction, the c-SiC film is thicker near the centre and thinner near the edge. In the X-axis direction, the c-SiC film is thicker on the left and thinner on the right. Also, the thickness contour matches the pattern on the c-SiC films as shown in the inset of Figure 7-1, which confirms the existence of the thickness gradients. The existing of thickness gradients is due to the depletion of silane downstream in the chamber [109].

Figure 7-2 shows refractive index map of the c-SiC film. The refractive index at 673 nm is in the range 2.6 to 2.8 for most part of the c-SiC film and is close the value reported for SiC in the literature [113]. The refractive index of c-SiC is higher than the refractive index of a-SiC up to 2.5 measured in Chapter 4.1. According to the Lorentz-Lorenz relation, the refractive index is proportional to the mass density. It is likely that the mass density of c-SiC films is higher than the 2.0 $g \cdot cm^{-3}$ mass density of a-SiC. The refractive index at the right side of the c-SiC film where the film is very thin, increased to 3.35 which is attributable to the refractive index of the Si substrate [185].

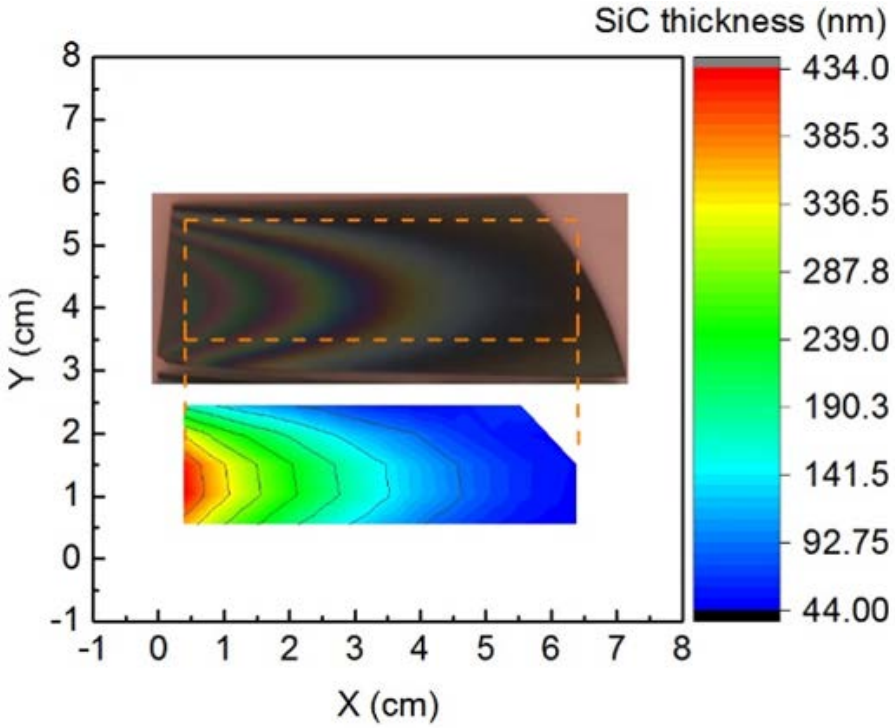


Figure 7-1. Thickness map of the c-SiC film on Si substrate. Inset is a photo of the c-SiC film.

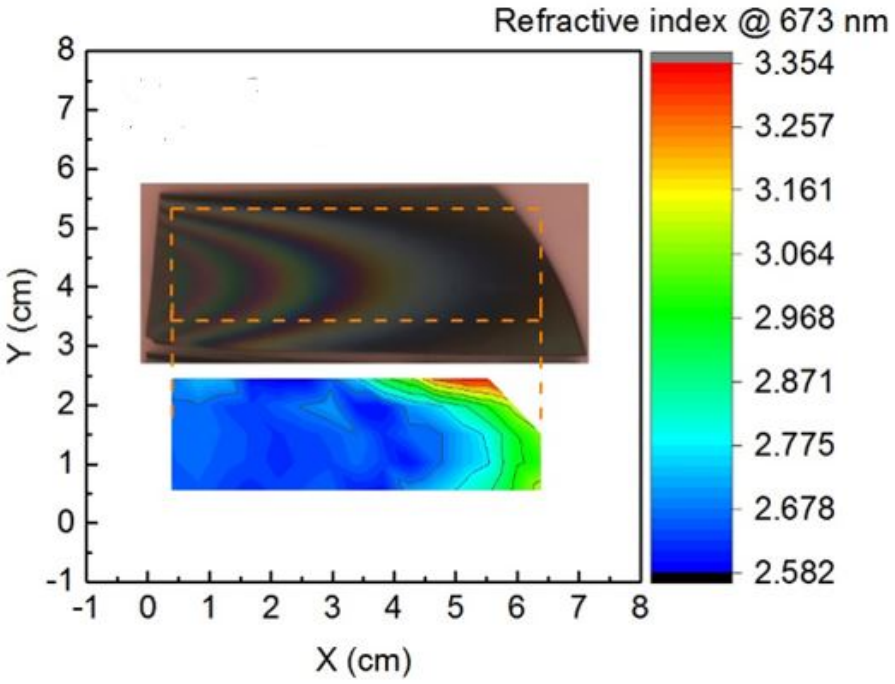


Figure 7-2. Refractive index map of the c-SiC film on Si substrate.

7.2 X-Ray Diffraction pattern

XRD spectra of the c-SiC film were measured to investigate the epitaxy quality of c-SiC on Si (001) surface. Figure 7-3a shows the XRD spectrum of a typical VPE c-SiC film on (001) Si substrate. The

peak near 33° corresponds to the forbidden Si (200) peak [186]. The peak near 35.7° corresponds to SiC (111) peak [129]. The peak near 41.5° corresponds to 3C-SiC (200) peak [109, 130], which indicates the c-SiC film is in epitaxial relation with the (001) Si substrate [130]. The peaks near 61.7° and 69.15° correspond to Cu Kβ and Kα radiation diffracted from the Si (400) planes [129]. Figure 7-3b shows the XRD patterns corresponding to SiC (200), measured at multiple points of the surface of the c-SiC films. The SiC (200) peaks is always near 41.5° which indicates the crystallinity of the c-SiC film is uniform over the Si substrate.

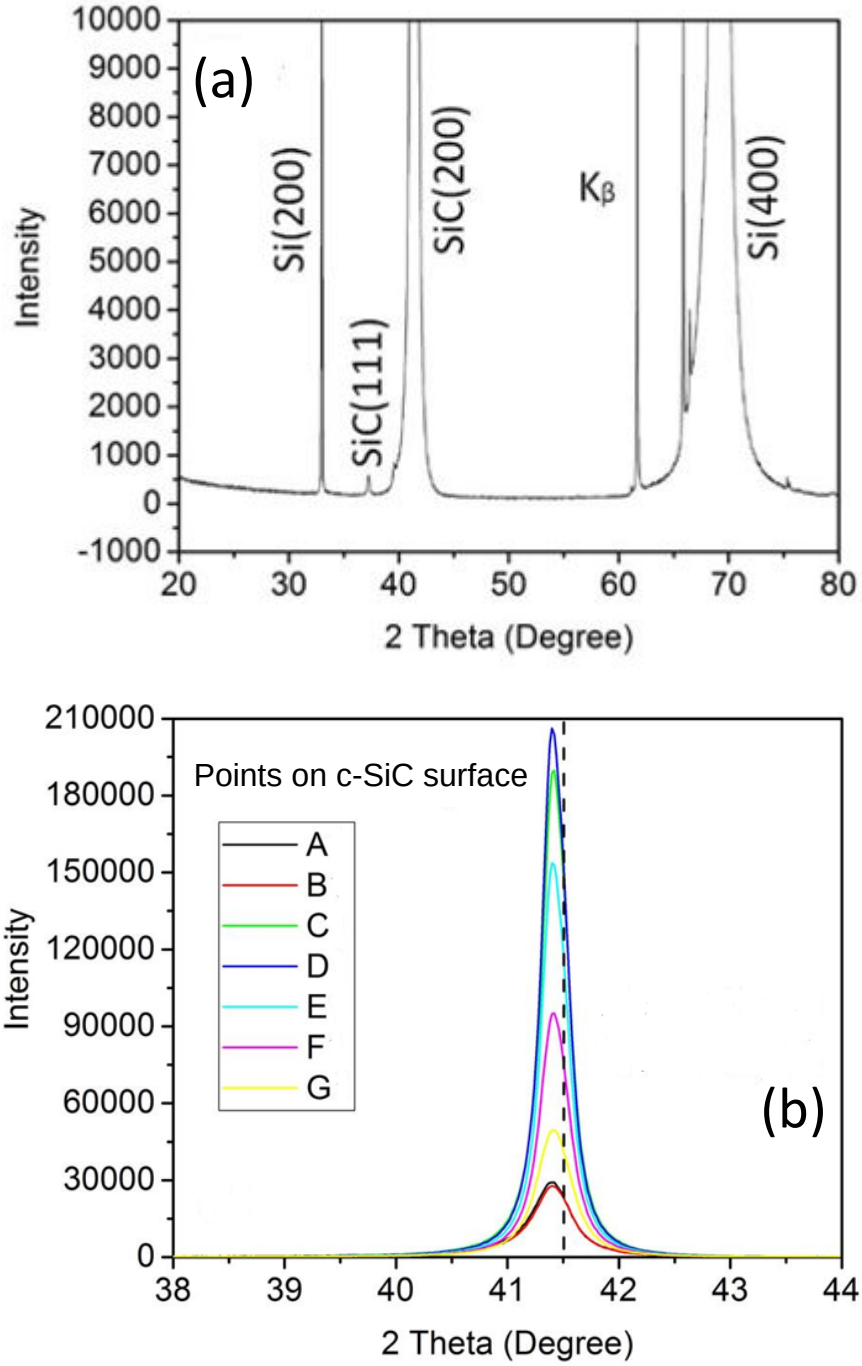


Figure 7-3. (a) XRD spectrum of the c-SiC film. (b) XRD patterns measured from multiple points over the surface of the c-SiC film.

7.3 Conduction mechanism of pristine Cu/c-SiC/Si device

The I-V characteristics of pristine Cu/c-SiC/Si devices were measured to investigate the current conduction mechanism. Knowing the current conduction mechanism of the pristine device helps to understand the conductive mechanisms after resistive-switching and the switching mechanism. Also, it is interesting to investigate the current conduction of c-SiC/Cu Schottky contact and c-SiC/Si heterojunction from a material research point of view. A voltage was applied to the Cu electrode and the Si substrate was grounded, as described in Chapter 3.1.3 and Chapter 3.3.2. Figure 7-4 shows the I-V characteristics of pristine Cu/c-SiC/Si devices with SiC thickness in the range 44 nm to 385 nm. A slightly rectifying I-V characteristic was observed with the current higher when +V was applied to the Cu electrode. The rectifying I-V characteristic could be attributed to either the c-SiC/Cu Schottky contact or the c-SiC/Si heterojunction. The I-V characteristics between two Cu electrodes on the c-SiC film was measured and compared with the I-V characteristics of the pristine Cu/c-SiC/Si devices corresponding to these two Cu electrodes, to investigate whether the rectifying current conduction was caused by the c-SiC/Cu junction or the c-SiC/Si junction.

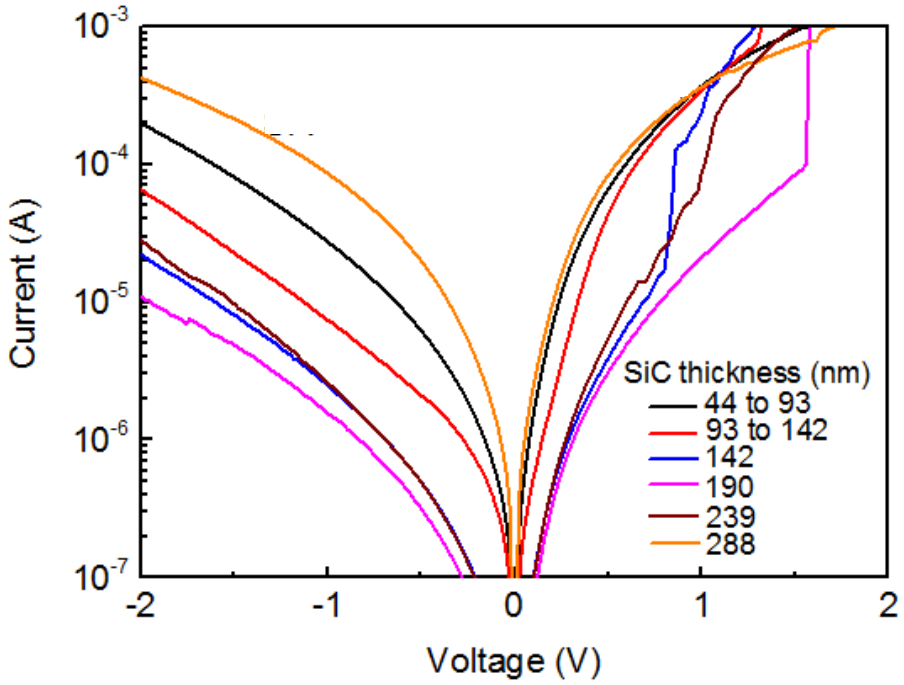


Figure 7-4. I-V characteristics of pristine Cu/c-SiC/Si devices with SiC thickness in the range 44 nm to 385 nm.

Figure 7-5a shows the I-V characteristics between two Cu electrodes, i.e. Cu(A) and Cu(B), on the c-SiC film. Schematics of the measurement is shown as in Figure 7-5b. I-V characteristics of the pristine Cu(A)/c-SiC/Si and Cu(B)/c-SiC/Si devices were also measured, as shown in Figure 7-5a. It is clear the I-V characteristics of pristine Cu(A)/c-SiC/Si and Cu(B)/c-SiC/Si devices both shows

rectifying conduction behaviour. Also, the reverse bias current of the pristine Cu(A)/c-SiC/Si and Cu(B)/c-SiC/Si devices match the I-V characteristics measured between the two Cu electrodes. This implies the rectifying conduction of pristine Cu/c-SiC/Si devices is attributed to the c-SiC/Cu Schottky contact.

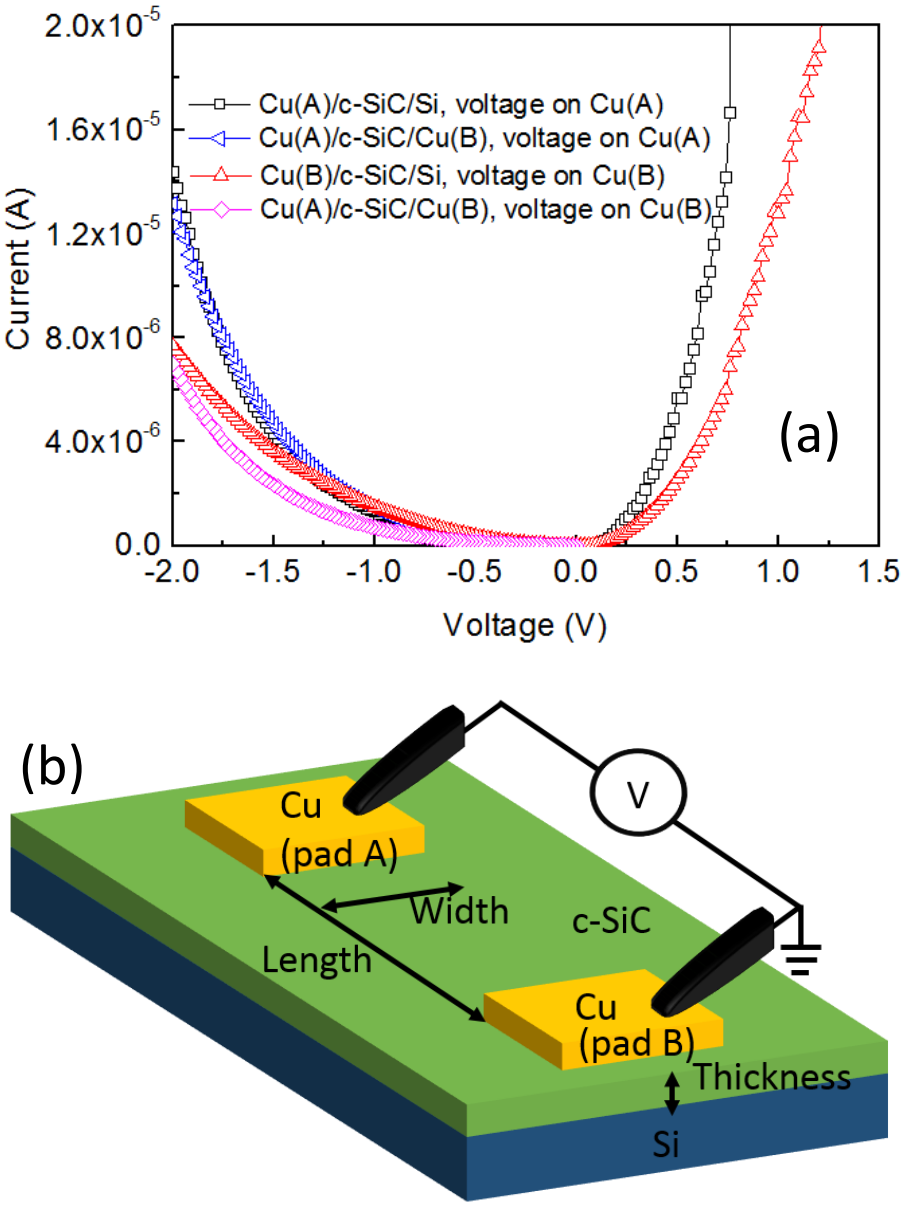


Figure 7-5. (a) I-V characteristics of pristine Cu/c-SiC/Cu and Cu/c-SiC/Si devices. (b) Schematic of the I-V measurement on a Cu/c-SiC/Cu device.

The forward bias and reverse bias I-V characteristics of pristine Cu/c-SiC/Si devices were analysed to further investigate the conduction mechanism. Figure 7-6 shows the measured and calculated forward bias I-V characteristics of pristine Cu/c-SiC/Si devices. Solid lines in Figure 7-6 were calculated using the forward bias Schottky emission equation which is described by Equation 7.1,

$$I = I_s\left(\exp\left(\frac{V}{\eta V_t}\right) - 1\right), \tag{7.1}$$

where I_s is the reverse saturation current, η is the ideality factor, and V_t is the thermal voltage which is 26 mV at 300 K. The solid lines were calculated separately in four voltage range 0.02 to 0.16 V, 0.16 to 0.32 V, 0.32 to 0.44 V, and 0.44 to 0.6 V, respectively to match the measured I-V characteristics. The ideality factor used in the calculation increased from 2.6 to 10.7 with the increasing voltage range, as shown in Table 7-1. Ideality factor higher than 1 indicates the increase of current voltage is limited by other conduction mechanism [187].

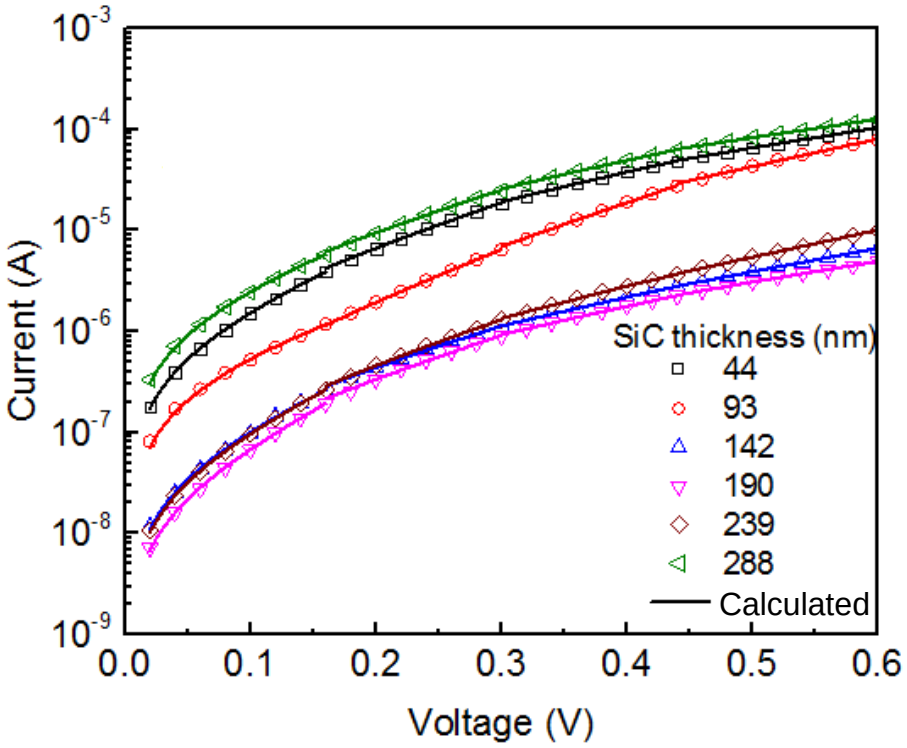


Figure 7-6. Forward bias I-V characteristics of the pristine Cu/c-SiC/Si devices.

Table 7-1. Ideality factor used in the calculation of forward-biased Schottky emission.

Voltage (V)	Ideality factor for Cu/c-SiC/Si devices with different SiC thickness					
	44 nm	93 nm	142 nm	190 nm	239 nm	288 nm
0.02 to 0.16	3.07	4.27	2.94	2.60	2.74	3.65
0.16 to 0.32	4.15	3.41	4.67	4.33	4.07	4.52
0.32 to 0.44	6.53	3.99	6.81	6.98	5.83	6.92
0.44 to 0.6	9.36	6.34	7.72	8.98	6.49	10.66

Figure 7-7 shows the reverse bias I-V characteristics of pristine Cu/c-SiC/Si devices, in the Ln(I)-√V scale. The straight lines fit indicates that reverse bias Schottky emission dominates the conduction mechanism. The SBH calculated using Equation 2.3 is in the range of 0.56 eV to 0.68 eV. Although

the calculated SBH is much lower than 0.9 eV of a-SiC, it is comparable to the values for c-SiC Schottky contacts in the literature [188].

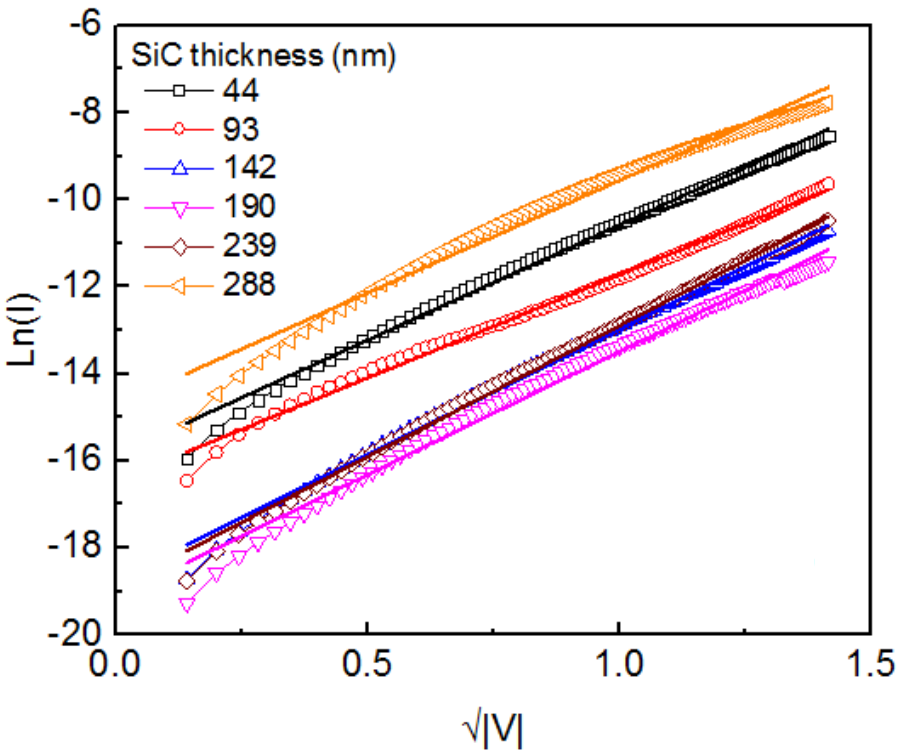


Figure 7-7. Reverse bias I-V characteristics of pristine Cu/c-SiC/Si devices, in the Ln(I)-√V scale, with respective linear fits.

7.4 Bipolar resistive-switching

Resistive-switching in the bipolar mode has been observed from a Cu/c-SiC/Si device with SiC thickness in the range 153 nm to 234 nm. Figure 7-8 shows the I-V characteristics of the bipolar resistive-switching for the Cu/c-SiC/Si device. The I-V characteristics of the first switching cycle where the device was switched from pristine state to LRS and back to HRS, was plotted in red lines. The first switching cycle is recognised as the electroforming cycle because the V_{FORM} in the first cycle was generally higher than the V_{SET} in the subsequent cycles. V_{FORM}, V_{SET}, and V_{RESET} are approximately 8.5 V, 3.2 V to 10.9 V, and -4.4 V to -8.4 V, respectively for the c-SiC resistive memory. These switching voltages are noticeably higher than the V_{FORM} approximately 4 V to 5 V, V_{SET} approximately 2 V, and V_{RESET} approximately -2 V of a-SiC resistive memories [10], which is attributable to the large thickness of the c-SiC insulating layer. The thickness of the c-SiC insulating layer is in the range 153-234 nm while the thickness of the a-SiC insulating layer is only 40 nm. It is likely that the high thickness of the c-SiC insulating layer would greatly reduce the electric field applied hence lead to higher switching voltage. The bipolar switching was repeated on the c-SiC resistive memory for 30 cycles till it is no longer able to RESET. The ON/OFF ratios measured at 1 V are in the range 20 to

2000 which is dramatically lower than the ON/OFF ratios of the a-SiC, a-SiC:Cu, and a-Si(O)C:H resistive memories. The low ON/OFF ratios of the c-SiC resistive memory is mainly attributed to the low HRS resistance. The origin of the low HRS resistance is discussed in the following paragraphs.

Detailed LRS and HRS I-V characteristics of the c-SiC resistive memory were analysed to investigate the conduction and switching mechanisms. Figure 7-9 shows the LRS I-V characteristics of the c-SiC resistive memory, in the Log(I)-Log(V) scale. The LRS I-V characteristics fit with straight lines that have a slope in the range 1.07 to 1.18, close to 1, which indicates Ohmic conduction in the LRS. The Ohmic conduction in LRS is attributable to the formation of Cu filament when $+V_{FORM}$ and $+V_{SET}$ were applied on the Cu electrode, according to the ECM switching mechanism [10, 63].

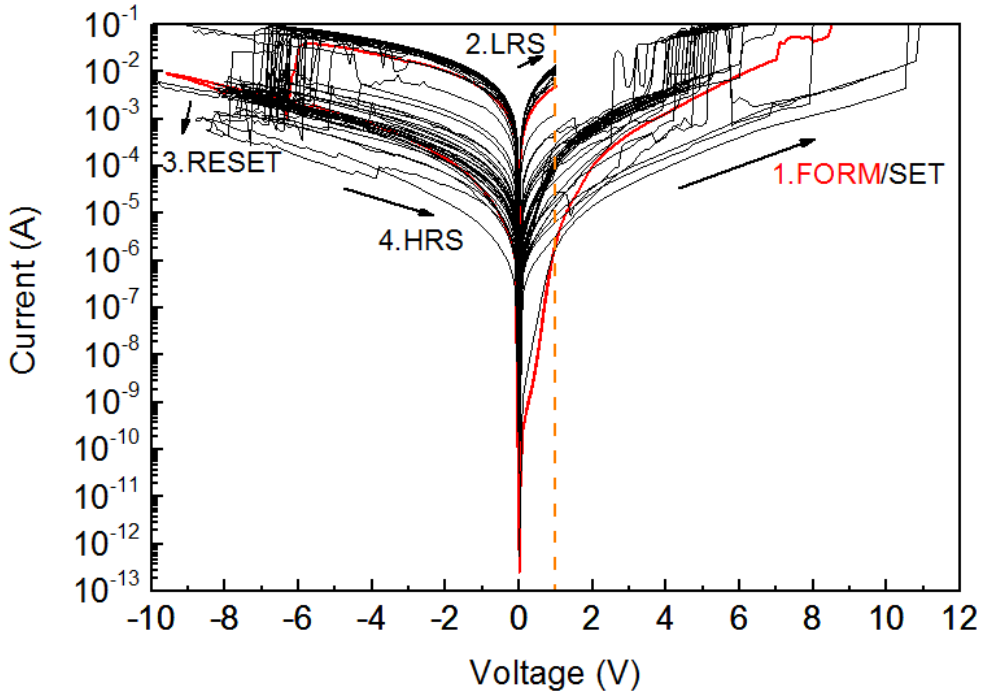


Figure 7-8. I-V characteristics of bipolar resistive-switching for a Cu/c-SiC/Si device with SiC thickness in the range 153-234 nm. The first resistive-switching cycle was plotted in red lines.

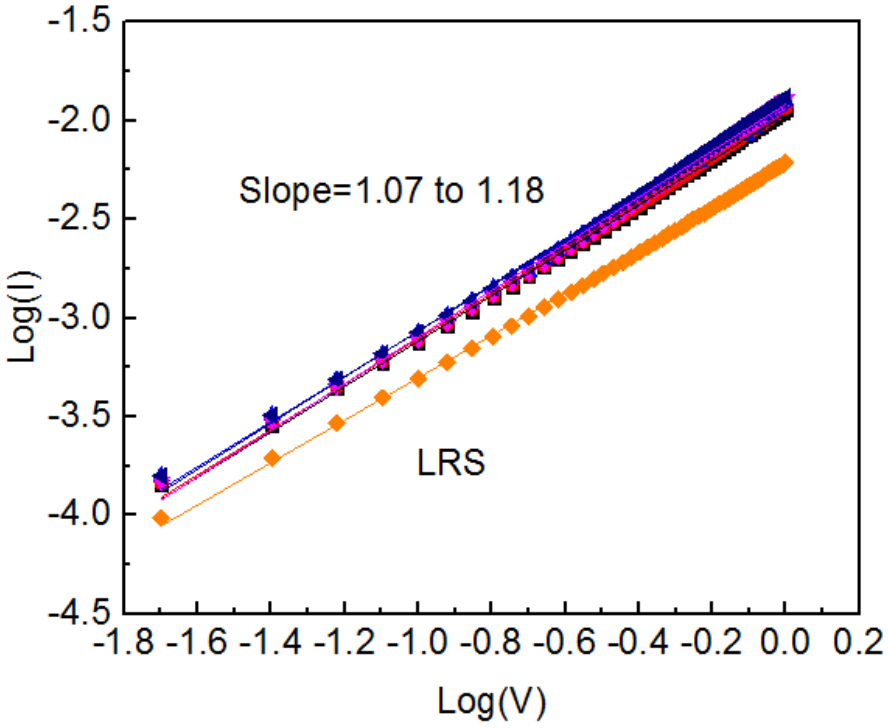


Figure 7-9. Log(I)-Log(V) of the c-SiC resistive memories in LRS, with respective linear fits.

Figure 7-10 shows the HRS I-V characteristics of the c-SiC resistive memory. Some HRS I-V characteristics fit with straight lines that have a slope closer to 2, which indicates space charge limited current conduction [66]. Other HRS I-V characteristics fit with straight lines that have a slope closer to 1, which indicates Ohmic conduction in the HRS. The space charge limiting conduction and Ohmic conduction in the HRS of c-SiC resistive memory indicates the existence of a Cu conductive network in the HRS. It is possible that the RESET process of the c-SiC resistive memory only increased the resistance of the Cu conductive filament instead of dissolving the Cu conductive filament. The absence of current conduction dominated by reverse bias Schottky emission in the HRS is responsible for the low HRS resistance and the low ON/OFF ratios of the crystalline SiC RM.

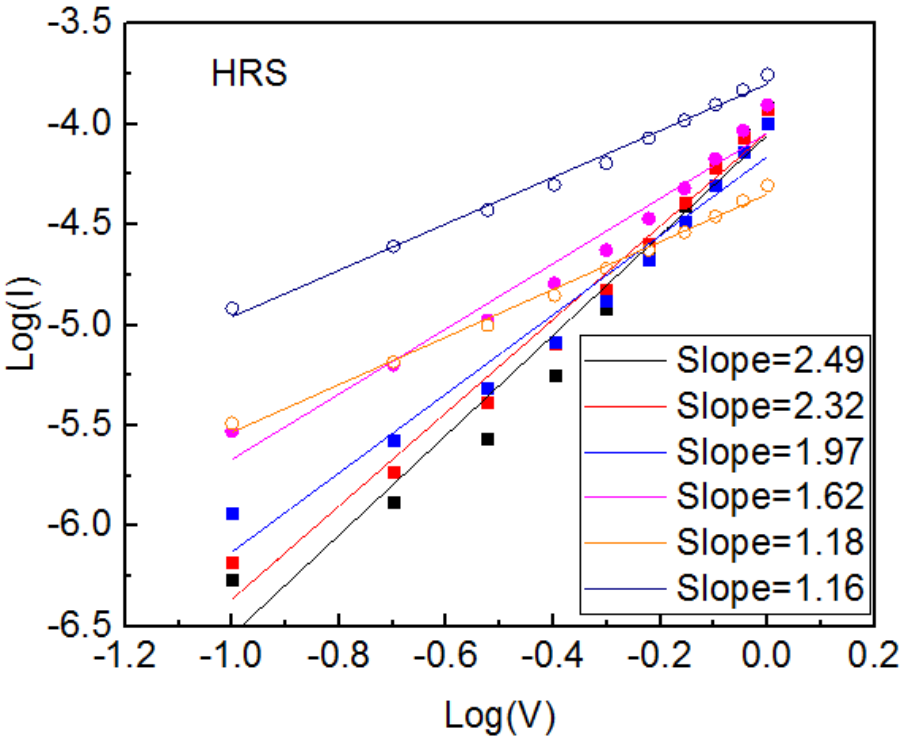


Figure 7-10. Log(I)-Log(V) of the c-SiC resistive memories in HRS, with respective linear fits.

7.5 Summary

Material properties of the c-SiC film were characterised and the switching behaviour of the Cu/c-SiC/Si resistive memory were studied. The thickness of c-SiC on the Si substrates has a gradient from 434 nm reduce to 44 nm. The refractive index of c-SiC is uniform on most part of the Si substrate and is in the range of 2.6 to 2.8. Rectifying I-V characteristics were measured from the pristine Cu/c-SiC/Si devices. The reverse bias I-V characteristics of the pristine c-SiC devices were attributed to the reverse bias Schottky emission of the c-SiC/Cu Schottky contact. The SBH of c-SIC/Cu contact was extracted to be 0.56 eV to 0.68 eV.

Bipolar resistive-switching has been observed from a c-SiC resistive memory that has c-SiC thickness in the range 153 nm to 234 nm. The switching was repeated for 30 cycles and has ON/OFF ratios in the range 20 to 2000. V_{FROM} and V_{SET} are approximately 8.5 V, and 3.2 V to 10.9 V, respectively, which are noticeably higher than the values of amorphous-SiC resistive memories. This is attributable to the high c-SiC thickness. Cu conduction filament in LRS leads to Ohmic conduction. Conduction mechanism of c-SiC resistive memory in HRS varies between Ohmic conduction and space charge limited conduction. The absence of the current conduction dominated by reverse bias Schottky emission in the HRS is responsible for the low HRS resistance and the low ON/OFF ratios of the crystalline SiC RM.

Chapter 8: Conclusions and future work

8.1 Conclusions

Material properties of amorphous (a)-SiC films and resistive-switching of a-SiC resistive memories were studied. The influence of sputtering condition on the material properties of a-SiC films was investigated. Material properties of a-SiC films can be tuned in a wide range by adjusting the SiC target power and Ar gas flow. Bipolar resistive switching has been observed from Cu/a-SiC/W resistive memories in which the inert W electrode is a native Back-end-of-line (BEOL) metal. Generally, switching performance did not show a significant difference by replacing the Au inert electrode with W. The Cu/a-SiC/W resistive memory with BEOL compatibility is hence promising for future resistive memory applications.

In addition, the material properties of the a-SiC can be tuned by embedding Cu nanoparticles. Material properties of a-SiC:Cu films co-sputtered with a controlled Cu% were investigated. Cu nanoparticles with a diameter of approximately 1 nm to 5 nm were found distributed in the a-SiC films, through XRD and TEM analysis. Tunnelling conduction was identified as the key conduction mechanism of the a-SiC:Cu films with the resistivity well described by the effective medium approximation model. Cu/a-SiC:Cu/Au resistive memories were fabricated using a-SiC:Cu with typical Cu% below percolation threshold including 20 and 30 Cu%. Resistive-switching performance of the Cu/a-SiC:Cu/Au resistive memories were studied. Reduced V_{FORM} and V_{SET} and increased endurance were observed in Cu/a-SiC:Cu/Au resistive memories, most noticeable at 30 Cu%. Furthermore, advantageous switching characteristics of a-SiC resistive memories including reverse bias Schottky emission in pristine state and HRS, high ON/OFF ratio up to 10^7, and co-existence of bipolar and unipolar modes were maintained upon Cu embedding. All the above suggests that Cu embedding should be considered as a promising method to improve the overall performance of Cu/a-SiC:Cu/Au resistive memories.

Material properties of the BEOL dielectrics a-Si(O)C:H were characterised and the influence of the materials properties of these a-Si(O)C:H films on the switching characteristics were analysed to solve the challenge to fabricate resistive memories using exclusively native BEOL materials. W/a-Si(O)C:H/Cu resistive memories were fabricated. Current conduction of pristine a-Si(O)C:H devices was dominated by the Schottky emission under reverse bias. An equivalent circuit which contains two head-to-head p-type Schottky diodes connected by a resistor was developed for pristine a-Si(O)C:H devices. Resistive-switching in the bipolar mode has been observed from W/a-Si(O)C:H/Cu resistive memories. Long retention and high ON/OFF ratios in the 5.8×10^5 to 3.7×10^{11} range suggest promising application potentials of W/a-Si(O)C:H/Cu resistive memories. The material

properties of the a-Si(O)C:H insulating layers have shown a variety of influence on the switching characteristics. It is possible to further optimise the switching characteristics of a-Si(O)C:H resistive memories using the material properties of the a-Si(O)C:H insulating layer as turn knob.

At last, material properties of the crystalline-SiC film were characterised and the switching behaviour of the Cu/c-SiC/Si resistive memory was studied. The thickness of c-SiC on the Si substrates has a gradient from 434 nm reducing to 44 nm. The refractive index of c-SiC is uniform on most part of the Si substrate and is in the range of 2.6 to 2.8. Rectifying I-V characteristics were measured from the pristine Cu/c-SiC/Si devices. Bipolar resistive-switching has been observed from a c-SiC resistive memory that has c-SiC thickness in the range of 153 nm to 234 nm. High V_{FROM} and V_{SET} were measured which is attributable to the high c-SiC thickness. Also, low ON/OFF ratios were observed which is attributable to the absence of current conduction dominated by reverse bias Schottky emission in the HRS.

8.2 Future work

8.2.1 Influence of materials properties of a-SiC insulating layer on switching characteristics

The material properties of a-SiC film RF sputtered using different SiC target power than Ar gas flow were investigate. It was found that the material properties including thickness, refractive index, band gap, and mass density of the a-SiC films can be turned by adjusting the SiC target power and Ar gas flow. It is known that the material properties of the insulating layer have large influence of the switching characteristics. However, the a-SiC insulating layer of all the a-SiC resistive memories investigated in this project, was RF sputtered using the same SiC target power and Ar gas flow. The switching characteristics of a-SiC resistive memories that have a-SiC insulating layer deposited using different SiC target power and Ar gas flow could investigated in the future to understand the influence of material properties of the a-SiC insulating layer on the switching characteristics of the a-SiC resistive memories.

8.2.2 Nonpolar switching for a-Si(O)C:H RMs

Nonpolar resistive-switching has been observed from the W/40 nm a-SiC:H/Cu resistive memories that have 40 nm a-SiC:H insulating layer. Figure 8-1a, b, c, and d show the I-V characteristics of positive bipolar, negative bipolar, positive unipolar and negative unipolar switching for W/a-SiC:H/Cu resistive memories. The measurement setup and fabrication process for W/a-SiC:H/Cu resistive memories requires further optimisation in order to improve the yield of devices switching in all the four switching modes. At the moment, only limited amount of a-SiC:H resistive memories

have shown negative unipolar switching. Also, the nonpolar resistive-switching measurement could be conducted on other a-Si(O)C:H resistive memories to investigate the optimised insulating layer for each resistive-switching modes.

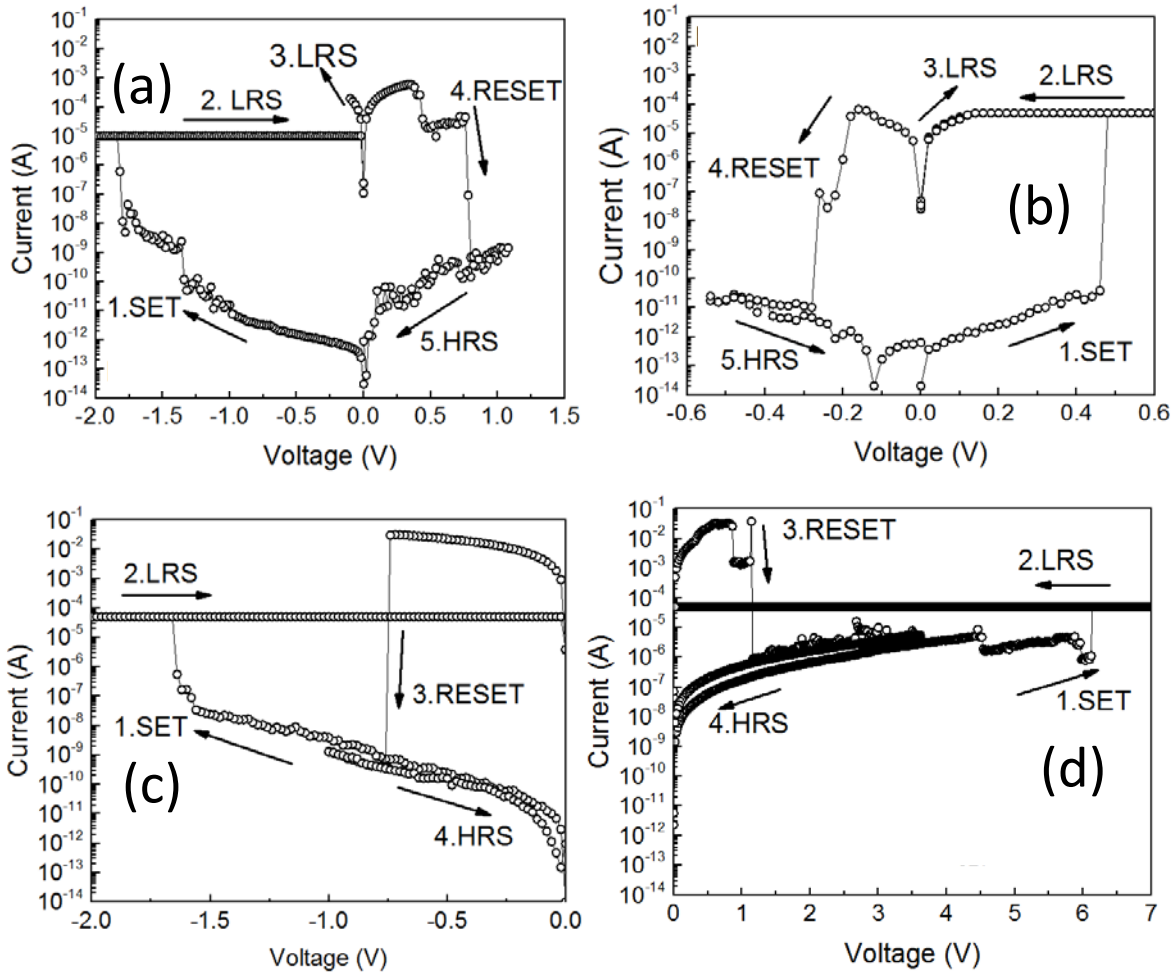


Figure 8-1. I-V characteristics of resistive-switching for W/a-SiC:H/Cu resistive memories in (a) positive bipolar, (b) negative bipolar, (c) positive unipolar, and (d) negative unipolar modes.

8.2.3 Pulsed switching for a-Si(O)C:H RMs

Preliminary test of pulsed switching was conducted on W/40 nm a-SiC:H/Cu resistive memories using the pulse module of the Keithley 4200SCS parameter analyser which is capable to perform transient pulsed measurement as short as 100 ns. The functionality of the pre-amplifiers which is used in combination with the pulse module to the Keithley 4200SCS, need to be checked. Also, the pulsed measurement programme requires to be optimised.

In the endurance measurement of a-SiC:H resistive memories, a pulsed I-V sweep was applied on the W electrode to electroform or SET the device into LRS, as shown in Figure 8-2. In the pulsed I-V sweep measurement, the resistance of the a-SiC:H resistive memory can be monitored in real-time

and a current compliance could be applied to protect the device. However, the disadvantage is the pulse width is high, of the order of 10 ms. It is required to develop an alternative method to apply the current compliance in the electroforming and SET processes in order to testing the V_{FORM} and V_{SET} at a higher speed.

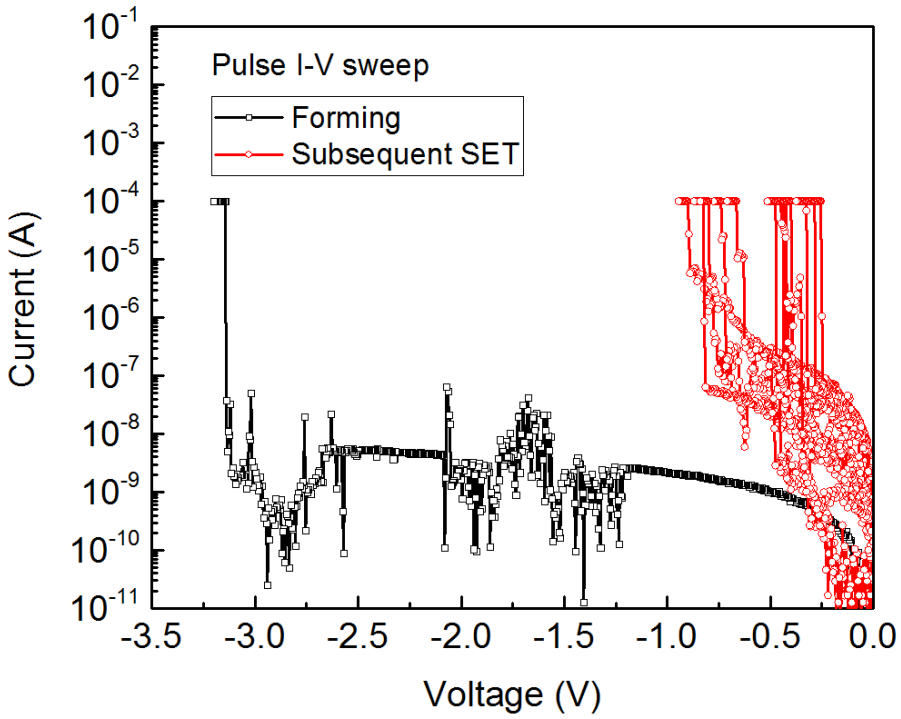


Figure 8-2. Pulsed I-V sweep of electroforming and SET processes for a W/a-SiC:H/Cu resistive memory.

In addition, a discrete voltage pulse was applied on the W electrode to RESET the device into HRS. Figure 8-3 shows the transient current measured when voltage pulses were applied to RESET a W/a-SiC:H/Cu resistive memory. The current of the W/a-SiC:H/Cu was first increased in the beginning when the voltage pulse was just applied, then abruptly decreased due the occurrence of RESET process. The RESET possesses shown in Figure 8-3 only took to about 40 µs to 80 µs to finish. This implies the a-SiC:H resistive memories is promising the operate at high speed.

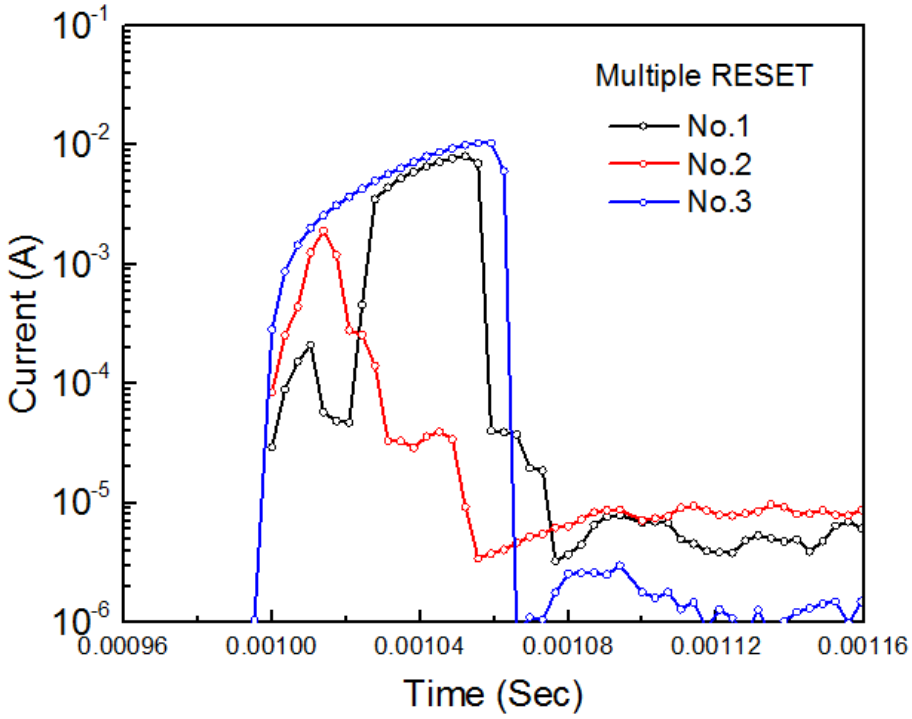


Figure 8-3. Transient current measured in three RESET processes of a W/a-SiC:H/Cu resistive memory.

Figure 8-4 shows the endurance of a W/a-SiC:H/Cu resistive memory switched using pulsed measurement. The LRS and HRS current was measured at -0.1 V in between the SET and RESET processes using DC measurement to increase measurement accuracy. The bipolar resistive-switching was repeated for 15 cycles on the W/a-SiC:H/Cu resistive memory which is higher than the endurance of the same type of device in DC I-V measurement. Hence, it is promising to obtain optimised endurance performance of a-Si(O)C:H resistive memories using pulsed measurement.

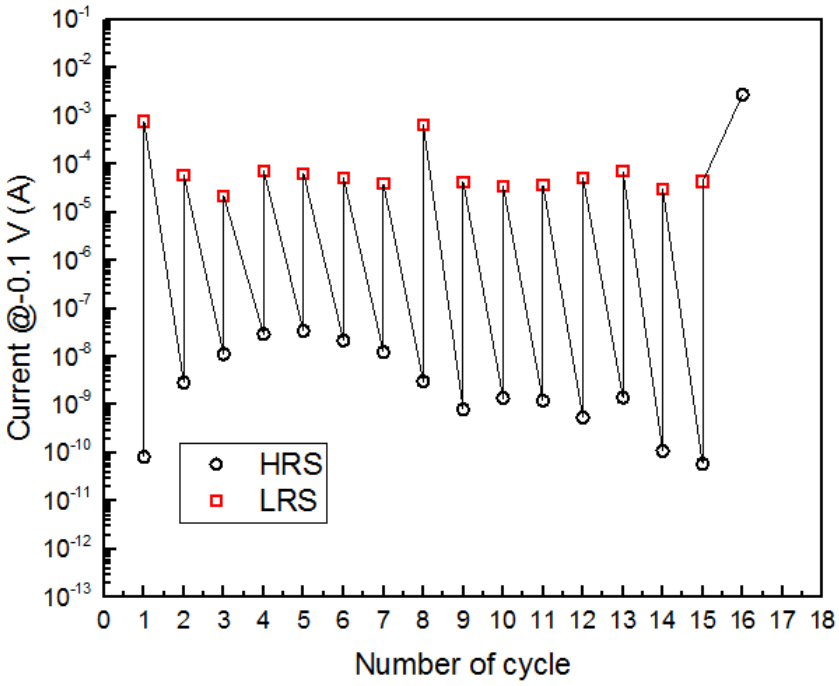


Figure 8-4. Endurance of a W/a-SIC:H/Cu resistive memory switched using pulsed measurement.

List of publications

Peer-reviewed journal publication

J. Fan, L. Jiang, S. Wang, R. Huang, K.A. Morgan, L. Zhong, and C.H. de Groot, Amorphous SiC resistive memory with embedded Cu nanoparticles, Microelectronic Engineering, 174 (2017), pp.1-5.

J. Fan, L. Jiang, L. Zhong, R.P. Gowers, K.A. Morgan, and C.H. de Groot., Microstructure and electrical properties of co-sputtered Cu embedded amorphous SiC, Materials Letters, 178 (2016), pp.60-63.

K.A. Morgan, **J. Fan**, R. Huang, L. Zhong, R.P. Gowers, J.Y. Ou, L. Jiang, and C.H. de Groot, Active counter electrode in a-SiC electrochemical metallization memory, Journal of Physics D: Applied Physics, (2017)

K.A. Morgan, **J. Fan**, R. Huang, L. Zhong, R.P. Gowers, L. Jiang, and C.H. de Groot, Switching kinetics of SiC resistive memory for harsh environments, AIP Advances 5, (2015) 077121.

Conference presentation

J. Fan, L. Jiang, L. Zhong, S. Wang, R. Huang, K.A. Morgan, C.H. de Groot, Resistive memories using Cu nanoparticles embedded amorphous SiC, Micro and Nano Engineering, Vienna, 2016. (Invited talk)

K.A. Morgan, **J. Fan**, R.P. Gowers, L. Jiang, and C.H. de Groot, Switching mechanisms of Cu/SiC resistive memories with W and Au counter electrodes, Device Research Conference Newark, Materials Research Society, 2016.

Paper in preparation

J. Fan, O. Kapur, R. Huang, S.W. King, C.H. de Groot, and L. Jiang, Back-end-of-line a-SiO_xC_y:H dielectrics for resistive memory, to be submitted to *Applied Physics Letters*.

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