Single-Phase Simplified Split-Source Inverter (S^3I) for Boost DC-AC Power Conversion

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***Abstract*— The single-phase split-source inverter is an emerging and attractive topology for boost dc-ac power conversion system. Such an inverter features high compactness, however, at the expense of high-frequency commutations across diodes. The corresponding hybrid PWM also confines the voltage harmonics to concentrate around the switching frequency and its multiples. This paper proposes a simplified split-source inverter which is realized by inserting only one power switch into an H-bridge. While generating the ac output, the newly developed PWM strategy ensures the inductor charged with constant duty-cycle. When compared to the existing split-source inverters, it offers the added benefits of reduced switch count, enhanced voltage boosting gain, reduced output filter requirement, and enhanced power efficiency. Comprehensive steady-state analysis is discussed while simulation and experimental results are subsequently presented to prove the validity of the proposed topology and the PWM strategy.**

***Index Terms*— Boost dc-ac power conversion, single-stage inverter, split-source inverter, pulse width modulation.**

I. Introduction

In many dc-ac power conversion systems, the input dc source is below the demanded peak voltage of the ac output [1], [2]. The boost dc-ac power conversion is therefore undeniably an important research topic of continuously growing importance in power electronics applications.

The main feature of the conventional dc-ac power conversion systems is usually based on two-stage topologies with the deployment of a dc-dc converter in the first stage to boost the voltage across the dc-link of an H-bridge [3]–[5]. However, these two-stage topologies experience apparent shortcoming such that they suffer from low efficiency with power loss dissipated across both the dc-dc converter and the dc-ac inverter. To this end, there are extensive efforts devoted to increase the power efficiency, with emphasis is predominantly given to the improvement of dc-dc converter in the first stage. For instance, the interleaved-type boost converter proposed in [6], [7] is one of the solution which is capable of reducing the inductor current harmonics and thereby ensure higher efficiency.

Instead of further improving the two-stage topologies, new research interest is inspired towards the development of single-stage topologies. This new trend has enabled the emergence of a variety design of single-stage topologies with significant efficiency improvement and increased compactness. For example, two back-to-back bidirectional boost dc-dc converter which share a single dc source, with the ac output acquired from the differential voltage between the outputs of converters are proposed [8], [9]. A major concern of these converters is that sinusoidal varying duty-cycle is needed for ac voltage generation, which unavoidably exerts substantial challenges in the design of appropriate control schemes. Complicated controllers such as sliding mode control [8] are often involved. Besides, special consideration must be taken into account to control the inductor current of the converter [10].

The Z-source inverter (ZSI), on the other hand, is another type of single-stage topology which can be traced back to 2003 [11]. It is established by introducing an impedance network into the dc-link. The introduction of ZSI has garnered significant interest, and since then, various impedance networks have been investigated. Comprehensive review of the different impedance networks have been summarized in [12]–[14]. All the existing impedance networks, however, exhibit a common shortcoming. The essential number of passive energy storage components such as capacitors and inductors in the impedance networks is relatively large.

Recently, an emerging type of single-stage boost dc-ac topology which features high compactness and requires only a boosting inductor and a dc-link capacitor has been reported. It is referred to as the split-source inverter (SSI). As the name implies, the input dc source is split from the dc-link and the voltage is boosted by charging a boosting inductor, as reflected by the configurations depicted in Fig.1. The first introduced SSI in Fig. 1(a) utilizes two diodes to connect a boost inductor to an H-bridge [15]–[17]. In the latter attempt,

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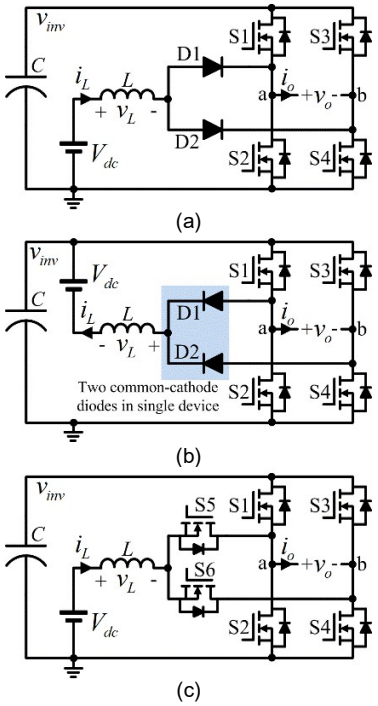

Fig. 1. Recent developments in single-phase split source inverter (SSI) topology, (a) first topology (SSI1) [15]–[17], (b) alternative topology enabling the use of two common-cathode diodes in single package (SSI2) [18], (c) improved topology (SSI3) [19].

two diodes have been conveniently replaced by a commercially available device which comprises two common-cathode diodes by reconfiguring the input dc source, as shown in Fig. 1(b) [18]. The increased compactness in this modified SSI, however, comes at the expense of the inevitable need of isolated dc source to isolate the negative terminals of both the dc source and dc-link. Alternatively, authors in [19] has recently proposed a rather different modification on the original SSI by replacing the two diodes with two power MOSFETs operating in synchronous rectification mode, as depicted in Fig. 1(c). The replacement of diodes not only contributes to bidirectional power flow, but at the same time resolves the high commutation frequency issue across the diodes.

It is important to note that the adoption of conventional sinusoidal PWM in all the aforementioned SSIs will result in variable inductor charging duty-cycle, which is complicated [19]. When the inductor is charged with variable duty cycle, the inductor current presents some undesirable low frequency harmonics, rendering an increment of its overall root-mean-square (rms), which further giving rise to high conduction loss. In this instance, a hybrid modulation of quasi-sinusoidal and constant PWM is preferably adopted [18], [19] to overcome these drawbacks. However, there is an accompanied constraint such that the harmonics in the output voltage are obliged to concentrate around the switching frequency and its multiples.

Addressing this concern, the aim of this work is to establish a simplified SSI topology which retains the attractive features of the existing SSIs with the added benefits of reduced power switch count, enhanced voltage boosting gain, reduced output power filter requirement, and enhanced power efficiency. This paper is organized as follows: Section II presents the proposed simplified SSI (S^3I) with detailed discussion on the steady-state analysis and mathematical derivations, Section III proceeds to summarize a comparison between the proposed S^3I and the recent SSI topologies. Sections IV and V present the simulation and experimental results, respectively, and finally Section VI draws the conclusion.

II. Proposed Simplified Split-Source Inverter (S^3I)

A. Topology Description and Principle of Operation

Fig. 2 illustrates the circuit diagram of the proposed single phase S^3I inverter. The existing SSI topology is reconfigured so as to incorporate only an auxiliary power switch into an H-bridge to form a three-switch leg and a half-bridge in parallel connection. The additional terminal introduced in the three-switch leg is connected to a dc source through an inductor. It is thus apparent that the dc source is split from the inverter dc-link. Compared to the SSIs in Fig.1, the proposed S^3I features a reduction in component count. While retaining the bidirectional power flow capability of SSI3, the exclusion of diodes in the proposed circuit configuration also hinders it from experiencing high commutation frequency issue incurred across the diodes, as in the SSI1 and SSI2.

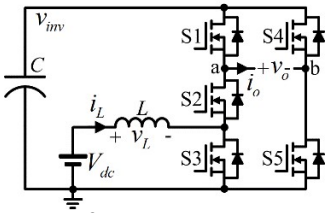

Fig. 2. The proposed simplified split-source inverter topology (S^3I).

To prevent short circuit across the dc-link, three switches in the first leg {S1,S2,S3} must never be ON concurrently. Two out of the three switches need to be turned on to avoid floating of terminals, i.e. across terminal a and the second terminal of inductor L. Similarly, the two switches in the half-bridge {S4,S5} must not be ON concurrently. In this regard, there are three permitted switching states for the three-switch leg [S1 S2 S3] = {[1 0 1], [1 1 0], [0 1 1]} and two permitted switching states for the half-bridge [S4 S5] = {[0 1], [1 0]}, constituting a total of six valid switching states. Equivalent circuit diagrams for all the corresponding switching states are illustrated in Fig. 3. Noticed that charging of inductor L is not influenced by the voltage at terminal a. This means that inductor L can be charged when $v_a = v_{inv}$ and $v_a = 0$. On the other hand, inductor L can only be discharged when $v_a = v_{inv}$. This is attributed to the fact that its discharging current is flowing through terminal a, when both S1 and S2 are ON. Therefore, the maximum inductor discharging duty-cycle (or minimum inductor charging duty-cycle) is defined by the minimum duty-cycle of $v_a = v_{inv}$.

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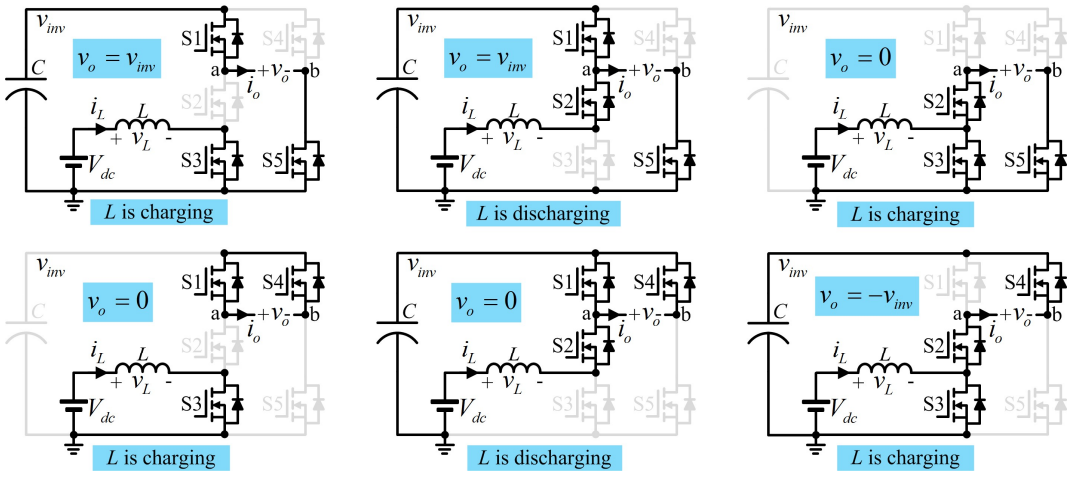

Fig. 3. Switching states of the proposed S^{3}I.

B. PWM and Inverter Gain

Fig. 4 depicts the PWM strategy developed for the proposed S^{3}I. Unlike the SSI topologies in Fig. 1, sinusoidal PWM technique can be easily implemented in the proposed S^{3}I without complicated modifications. It is hence needless to establish a dedicated hybrid modulation of quasi sinusoidal and constant PWM as in the existing SSI topologies, since the deployment of unipolar switching technique will suffice. With the hybrid modulation not taken into consideration, harmonics in the output voltage will not be obliged to center around the switching frequency and its multiples. Instead, harmonics in the output voltage concentrate around twice the switching frequency ($2f_s$) and its multiples. This is apparently an advantage since it indicates lower filter size requirement.

Assuming negligible dc-link voltage ripple, the fundamental output voltage of the proposed S^{3}I is deduced as

$$v_{o,1} = m \cdot V_{inv} \sin(\omega t) = \hat{V}_{o,1} \sin(\omega t) \tag{1}$$

where, $m = \hat{V}_{\sin} / \hat{V}_{tri}$ is the modulation index, and V_{inv} is the average dc-link voltage.

In order to achieve voltage boosting, a negative constant reference -V* is inserted between the peak of sinusoidal reference and the peak of triangular carrier to control the charging duty-cycle of inductor L,

$$D = \frac{V^*}{2\hat{V}_{tri}} + \frac{1}{2} \tag{2}$$

As inductor L is charged and discharged with constant duty cycle, voltage boosting from input to dc-link is not affected by the sinusoidal varying duty-cycle upon its ac output generation. Taking volt-second balance across inductor L with continuous current, the dc-dc gain is computed as

$$\frac{V_{inv}}{V_{dc}} = \frac{1}{1-D} \tag{3}$$

The overall gain of the proposed S^{3}I can be computed by combining (1) and (3), given as

$$\frac{\hat{V}_{o,1}}{V_{dc}} = \frac{m}{1-D} \tag{4}$$

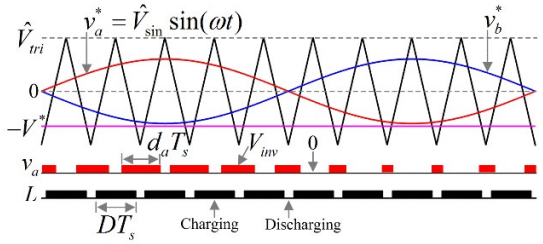

Fig. 4. PWM strategy for the proposed S^{3}I.

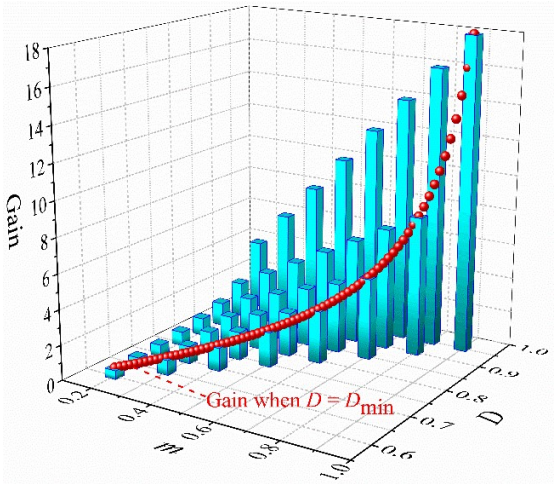

Fig. 5. The gain of the proposed S^{3}I as a function of modulation index and inductor charging duty cycle.

Both m and D allow control freedom for the proposed S^{3}I. However, minimum D is constrained by $V^* = \hat{V}_{\sin}$ since inductor L can only be discharged when terminal a is connected to dc-link. Consequently, the minimum charging duty-cycle for inductor is

$$D_{\min} = \frac{1}{2}(m+1) \tag{5}$$

If the minimum inductor charging duty-cycle is selected, the overall S^{3}I gain is given as

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$$\frac{\hat{V}_{o,1}}{V_{dc}} = 2\frac{m}{1-m} \tag{6}$$

An overview of the S^{3}I gain as a function of m and D is illustrated in Fig. 5.

C. High Frequency and Low Frequency Ripples

The volt-second balance and charge balance of inductor and capacitor, respectively are considered for the computation of high frequency ripple,

$$\Delta V_{inv,HF} = \frac{D\cdot(1-D)\cdot I_L}{C\cdot f_s} \tag{7}$$

$$\Delta I_{L,HF} = \frac{D\cdot V_{dc}}{L\cdot f_s} \tag{8}$$

where f_s is the switching frequency, L is the boost inductor, C is the dc-link capacitor, V_{dc} is the input voltage, I_L is the average (dc component) inductor current, and D is the inductor charging duty-cycle. The instantaneous output power pulsation of the inverter results in a ripple at twice the fundamental frequency. This is best illustrated by analyzing the input and output current of an H-bridge at different load angles, as shown in Fig. 6. Taking the average input current over a switching period, the low frequency input current is computed as

$$\langle i_{in}\rangle = \frac{1}{T_s}\int_t^{t+T_s} i_{in}dt = \begin{cases} d\cdot i_o, 0<\omega t<\pi \\ -d\cdot i_o, \pi<\omega t<2\pi \end{cases} \tag{9}$$

where $d = |m\sin(\omega t)|$ represents the duty cycle of $|v_o|$, i_{in} represents the instantaneous input current, and i_o represents the instantaneous output (load) current.

For unity power factor (PF = 1) shown in Fig. 6(a), the output current is proportional to the voltage with i_{in} pulsates between 0 and V_{inv}/R. Therefore, the low frequency input current for unity power factor is

$$\langle i_{in}\rangle_{PF=1} = \left|\hat{I}_{o,1}\sin(\omega t)\right| \tag{10}$$

where $\hat{I}_{o,1}$ indicates the peak of load current. The equation has clearly shown the existence of a dc component and a double fundamental frequency component which can be extracted by performing Fourier analysis. For inductive load (PF < 1) shown in Fig. 6(b), the load current is continuous and sinusoidal. Compared to the fundamental output voltage, a phase delay of θ is observed in the load current. With high switching frequency, the load current is approximately constant for each switching period, i.e. $i_o(t+T_s) = i_o(t)$. Therefore, the low frequency input current for PF < 1 can be deduced as

$$\langle i_{in}\rangle_{PF<1} = \frac{1}{2}m\cdot\hat{I}_{o,1}\cos\theta - \frac{1}{2}m\cdot\hat{I}_{o,1}\cos(2\omega t-\theta) \tag{11}$$

Noticed that the low frequency input current in this instance also consists of a dc component and a double fundamental frequency component, as similar to that of unity power factor. Assume that the dc-link capacitor is infinitely large for perfect power decoupling, the double fundamental frequency current is bypassed through the capacitor with ideally zero impedance. Therefore, the peak of the double fundamental frequency dc-link voltage can be computed by considering the reactance of dc-link such that

$$\hat{V}_{inv,2\omega} = \hat{I}_{in,2\omega}\cdot\left|Z_{c,2\omega}\right| = \frac{\zeta\cdot\hat{I}_{o,1}}{2\omega\cdot C} \tag{12}$$

where $\omega = 2\pi 50$ rad/s and $\zeta = \begin{cases} \frac{4}{3\pi}, PF=1 \\ \frac{m}{2}, PF<1 \end{cases}$

The existence of the double fundamental frequency voltage across dc-link induces a similar frequency voltage across inductor L. The double fundamental frequency inductor current is therefore

$$\hat{I}_{L,2\omega} = \frac{\zeta\cdot\hat{I}_{o,1}\cdot(1-D)}{4\omega^2\cdot C\cdot L} \tag{13}$$

Finally, the overall dc-link voltage ripple and inductor current ripple are

$$\Delta V_{inv} = \frac{\zeta\cdot\hat{I}_{o,1}}{\omega\cdot C} + \frac{D\cdot(1-D)\cdot I_L}{C\cdot f_s} \tag{14}$$

$$\Delta I_L = \frac{\zeta\cdot\hat{I}_{o,1}\cdot(1-D)}{2\omega^2\cdot C\cdot L} + \frac{D\cdot V_{dc}}{L\cdot f_s} \tag{15}$$

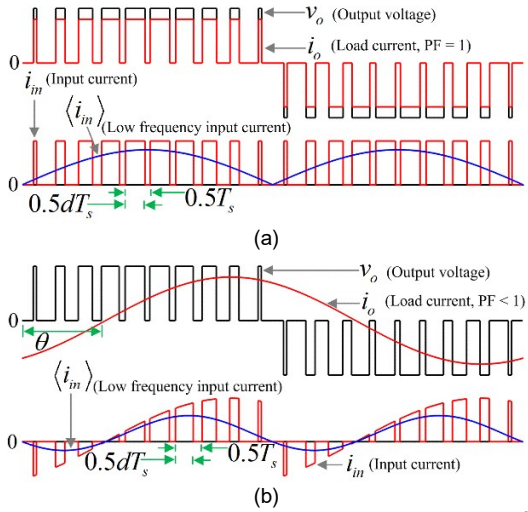

Fig. 6. The relationship between input and output current of an H-bridge inverter.

III. Comparative Study

A comparison of the recently presented SSI topologies and the proposed S^{3}I is summarized in Table 1. Note that the considered SSI topologies are essentially the same from the viewpoints of their topological structures, component count, and voltage boosting gain. Besides, their output voltage harmonics are confined at the switching frequency and multiples thereof.

SSI2 differs from SSI1 such that it utilizes diodes which are packed into smaller enclosure, gaining advantage in compactness but at the same time incurring an added disadvantage of isolated dc source requirement. Meanwhile, SSI3 differs from SSI1 and SSI2 such that it replaces the two diodes with two MOSFETs. Aside from resolving the

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complication of high commutation frequency across diodes, the replacement has made possible bidirectional power flow in the inverter.

Similar to SSI3, the proposed S^{3}I discards the employment of any diode in the inverter. The merits of SSI3 are thus inherited in the proposed S^{3}I. With some topological reconfiguration, the proposed S^{3}I manages to save one component count by needing only five power MOSFETs. Its attainable voltage gain for a given modulation index is twice that of SSI1-SSI3, which appears to be one of its advantages. In addition, the output voltage harmonics concentrate around twice the switching frequency and multiples thereof, thereby reduces the power filter requirement, i.e. smaller power filter for higher cutoff frequency.

TABLE I
COMPARISON BETWEEN SINGLE-PHASE SSI TOPOLOGIES AND THE PROPOSED S^{3}I

	SSI1 [15]-[17], SSI2 [18]	SSI3 [19]	**Proposed S^{3}I**
Switches	4	6	**5**
Diodes	2	0	**0**
Inductor	1	1	**1**
Capacitor	1	1	**1**
Bidirectional	no	yes	**yes**
Voltage gain	$m/(1-m)$	$m/(1-m)$	$\mathbf{2m/(1-m)}$
Minimum harmonic frequency	f_s	f_s	$\mathbf{2}f_s$

IV. SIMULATION RESULTS

A. Verification of the Proposed S^{3}I

Simulation was conducted in MATLAB Simulink to verify the operation of the proposed S^{3}I topology. The value of each component is selected based on the available resources for experimental implementation, i.e. C = 4700μF, L = 11mH, load resistor = 50Ω, and load inductor = 100mH. The input voltage, V_{dc} was set to 30V and the switching frequency was chosen to be 4 kHz. The minimum charging duty-cycle, D_{min} was considered such that the inverter can be controlled solely by modulation index according to (6).

The modulation index m of 0.85 was simulated first to verify the capability of the proposed topology in generating 240V rms (root mean square). As can be seen in Fig. 7, the average dc-link voltage is boosted to 395V with the fundamental peak output voltage recorded as 335.5V. High voltage boosting gain of approximately 11 is achieved. The spectrum of the output voltage shows that the harmonics are centered in the vicinity of twice the switching frequency (2*4kHz) and its multiples.

Simulation was also repeated to evaluate the output voltage, capacitor voltage ripple, and inductor current ripple under varying m. Their corresponding simulated results are recorded and plotted in Fig. 8, 9, and 10 respectively. The simulated dc-link voltage ripple and inductor current ripple are slightly higher than their calculated values. Nonetheless, good agreement between the simulations and calculations confirms the operation of the proposed S^{3}I.

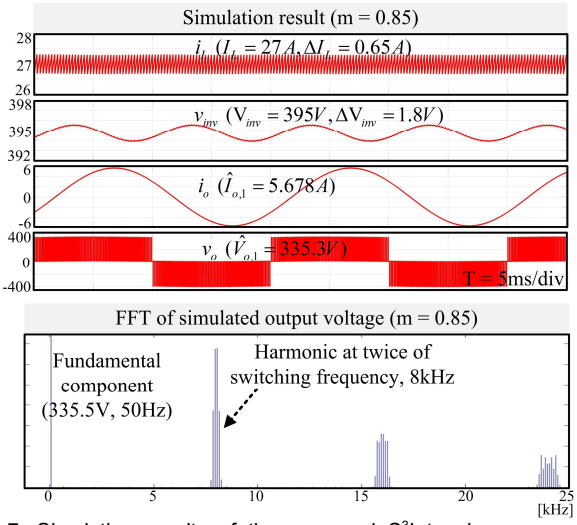

Fig. 7. Simulation results of the proposed S^{3}I topology generating approximately 240V rms (V_{dc} = 30V, m = 0.85).

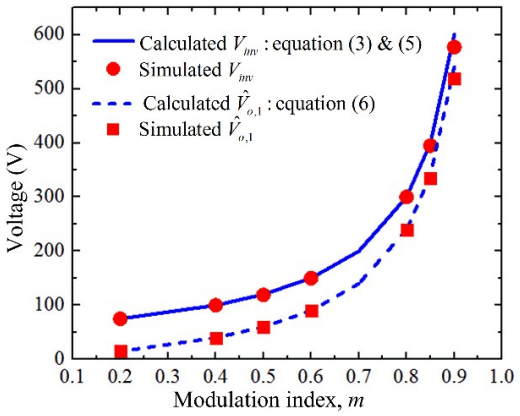

Fig. 8. Simulated output voltage as a function of modulation index and the comparison with theoretical calculation

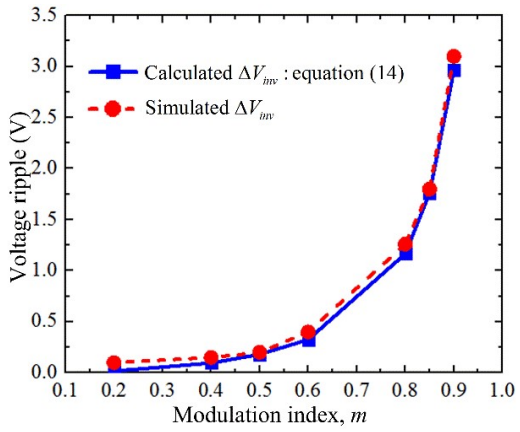

Fig. 9. Simulated capacitor voltage ripple as a function of modulation index and the comparison with theoretical calculation.

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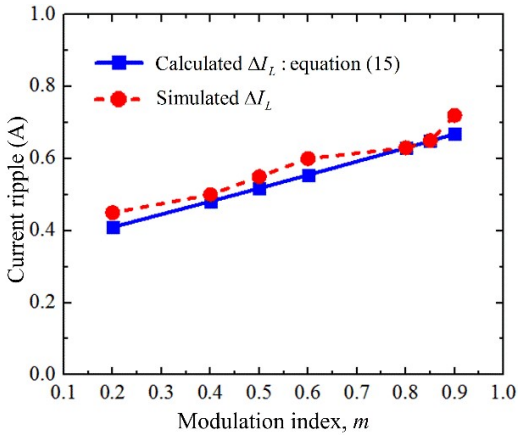

Fig. 10. Simulated inductor current ripple as a function of modulation index and the comparison with theoretical calculation.

B. Comparison against SSI3 [19]

Simulation was then performed to verify the advantages of the proposed S^{3}I with its modulation technique over the SSI3 and its corresponding hybrid PWM [19]. For fair comparison, the results were collected with the simulation settings and component values kept unchanged. It is interesting to point out that SSI3 requires a higher m of 0.92 (calculated using (11) in [19]), as compared to a lower m of 0.85 in the proposed topology for 240V rms generation. Fig. 11 reveals that the harmonics of the output voltage for SSI3 are centered in the vicinity of the switching frequency and its multiples. Considering the same switching frequency, this study confirms the superiority of the proposed S^{3}I over SSI3 in terms of its smaller power filter requirement.

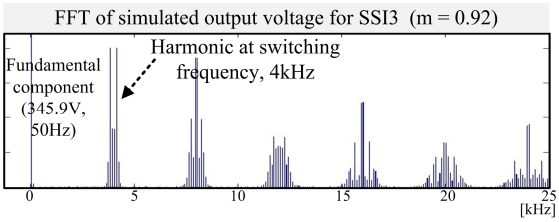

Fig. 11. Simulated voltage spectrum of the recent SSI3 generating approximately 240V rms (V_{dc} = 30V, m = 0.92).

With the input voltage now increased to 150V to emulate a typical application, Fig. 12 shows the corresponding simulated and calculated voltage gains for both the SSI3 and the proposed S^{3}I at different values of m. Note that the ON resistance of power switches used in the experimental prototype were considered in this study as well. Evidently, the proposed S^{3}I exhibits significantly higher gain than SSI3 for any particular value of m. This also means that SSI3 requires higher m than the proposed S^{3}I in obtaining the same voltage gain. This finding is anticipated, since when referring to (11) in [19], the voltage gain as a function of modulation index in SSI3 is only m/(1-m), which is half compared with that in the proposed S^{3}I (shown in (6)). A specific voltage gain can always be achieved by operating SSI3 at a rather high m. However, the implication on the efficiency becomes prominent when it is to be operating at higher m, i.e. lower efficiency at higher m [19].

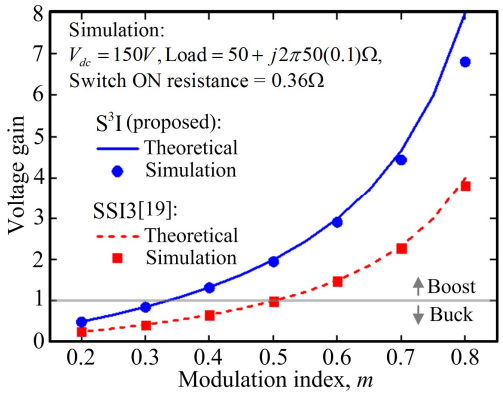

Fig. 12. Comparison of voltage gain.

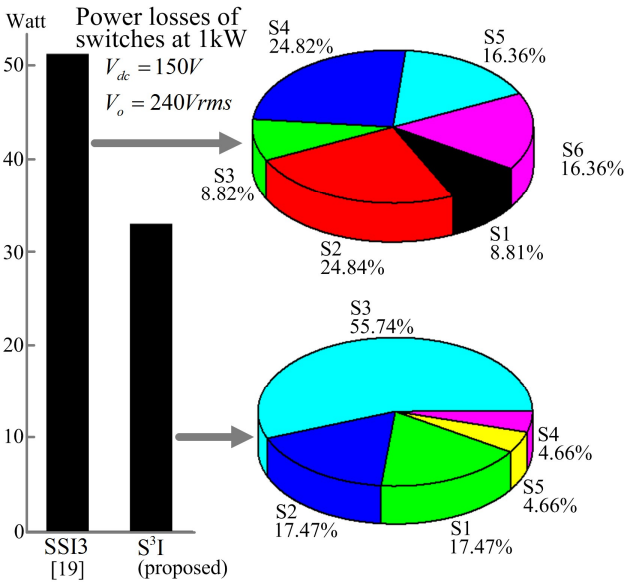

Fig. 13. Power losses and loss distribution of power switches at 1kW.

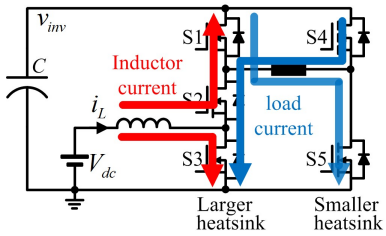

Fig. 14. Heatsink design consideration for the proposed S^{3}I.

Fig. 13 compares the power losses and loss distribution among power switches in both topologies under the same operating condition, i.e. input voltage of 150V, output voltage of 240Vrms and output power of 1kW. The power losses includes the switching and conduction losses which are numerically calculated based on the simulated current and voltage waveforms of each switch under steady-state condition.

One similarity between both topologies is their uneven power loss distribution among switches, implying the need of appropriate heat sink design [20]–[22] for commercial product

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implementations in the future. In the case of the proposed S^{3}I, three switches in the first leg (S1, S2, S3) generate substantially higher losses than the two switches in half-bridge (S4, S5). Almost 90% of the power losses are dissipated across the three-switch leg since it conducts the inductor dc current and the load ac current at the same time, as depicted in Fig. 14. Nonetheless, it shows significantly lower power losses (32.9W) as compared to SSI3 (51.1W), thus demonstrating superior power conversion efficiency and smaller overall heat sink requirement.

Concisely, the simulation studies verified that the proposed S^{3}I is superior to SSI3 [19], i.e. lower power filter requirement, twice voltage gain for a given modulation index, and enhanced power conversion efficiency.

V. Experimental Results

A low power experimental prototype depicted in Fig. 15 was implemented to further verify the operation of the proposed topology. Fig. 16 shows the details of the prototype implementation. The proposed PWM technique was computed in a host-pc running MATLAB Simulink equipped with Simulink Desktop Real Time toolbox and the PWM signals were generated through a data acquisition device. Electronic circuitry was used to introduce dead-time to prevent short circuit across the dc-link. The circuit diagram of the dead-time generator and its key waveforms are presented in Fig. 16. All the PWM signals were isolated and amplified by a gate driver circuitry prior to controlling the power MOSFETs. Components used for implementing the S^{3}I prototype are summarized in Table II.

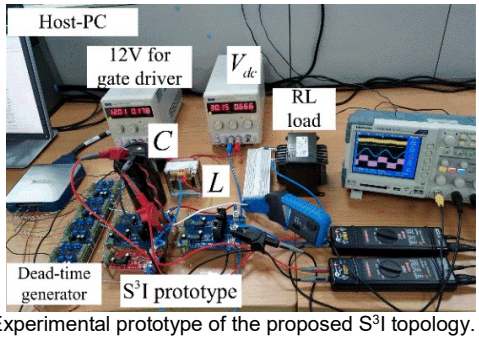

Fig. 15. Experimental prototype of the proposed S^{3}I topology.

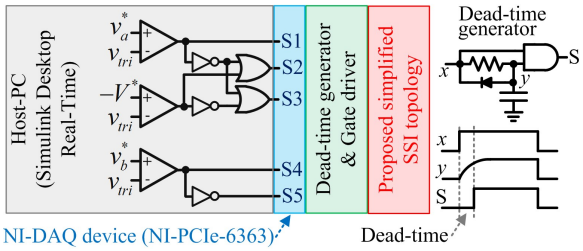

Fig. 16. Experimental prototype implementation of the proposed S^{3}I topology.

TABLE II
Components used In The Experimental Prototype

	Part number	Rating
Switch (MOSFET)	C3M0280090D	11.5A, 900V, Max ON resistance = 0.36Ω
Inductor	ZKD400/800-5,7	11mH, 5.7A
Capacitor	ALS30A472NP400	4700μF, 400V
Load resistor	NE7026	3000W
Load inductor	195T5	0.1H, 5A
DC supply 1	EL302R	0-30V, 0-2A
DC supply 2	TDK-Lambda	0-150V, 0-22A

Fig. 17 shows the measured experimental waveforms at m = 0.5. The measured average dc-link voltage was 120V, confirming a boosting gain of four from dc source to dc-link. The measured dc-link voltage ripple of 0.28V is slightly higher than its calculated value of 0.18V. The output current is sinusoidal and its peak is recorded as 0.94A. The peak of fundamental output voltage can be calculated by multiplying the peak of output current and the magnitude of impedance, which is equal to 55.5V. This confirmed the dc to ac output boosting gain of 1.85, which is slightly less than that from calculation.

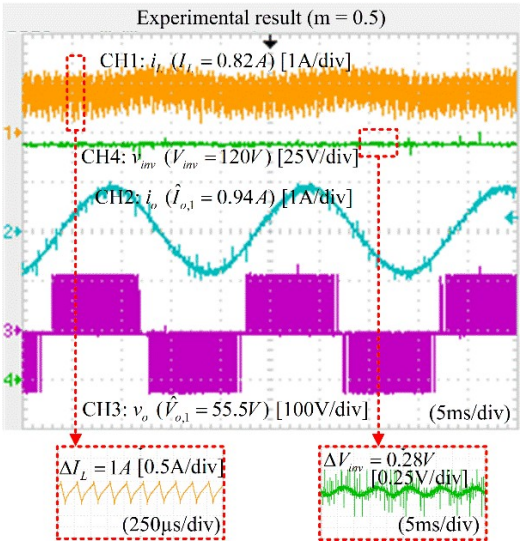

Fig. 17. Experimental results the proposed S^{3}I topology (m = 0.5).

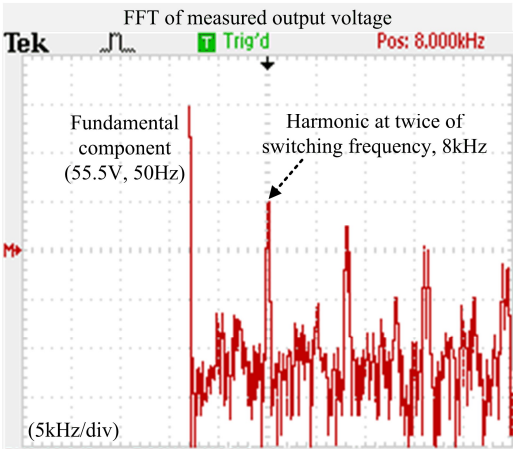

Fig. 18. FFT of the measured output voltage in Fig. 17.

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A zoomed view into the inductor current shows that the inductor is charged and discharged during each 250μs period with a constant duty-cycle of 0.75 and 0.25, respectively. To further validate the superiority of the proposed PWM technique presented in Fig. 4, Fast Fourier Transform (FFT) function of the digital oscilloscope is used to analyze the spectrum of the output voltage, as shown in Fig. 18. It is evident that the voltage harmonics concentrate around twice the switching frequency, i.e. 8kHz and its multiples.

Fig. 19 shows the measured experimental waveforms at m = 0.5 with resistive load of 57Ω. With an input voltage of 50V, the measured average dc-link voltage obtained is 179V, resulting a boosting gain of 3.58 from dc source to dc-link, slightly lower than the calculated dc-link voltage gain of 4. The output rms current obtained is 1.54A while the output rms voltage obtained is 82.98V. The inductor is charged and discharged with a constant duty cycle of 0.75 and 0.25 respectively for m = 0.5 while having a ripple of 1A.

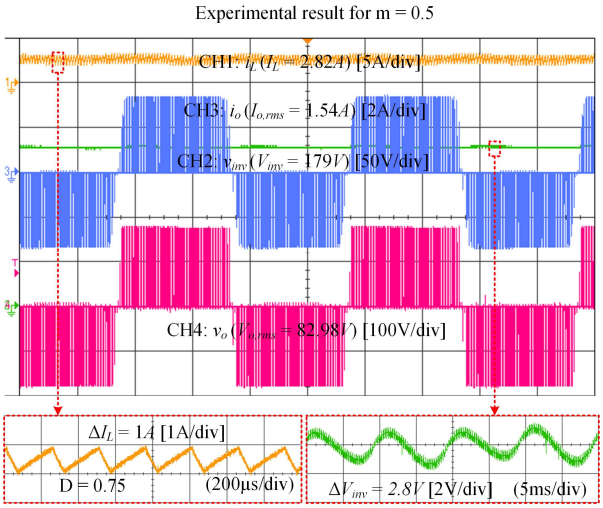

Fig. 19. Experimental results for m = 0.5.

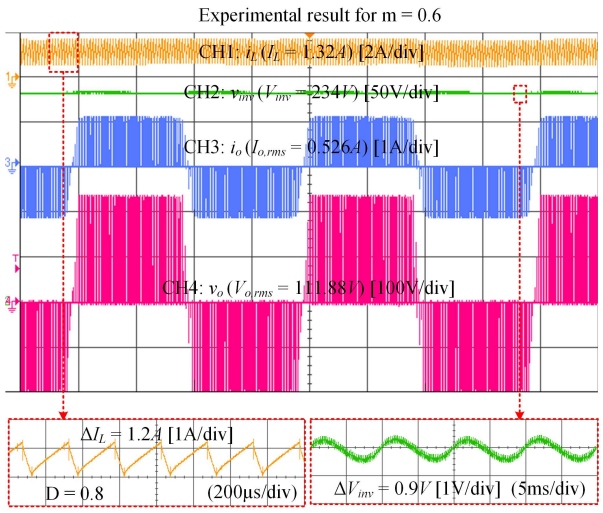

Fig. 20. Experimental results for m = 0.6.

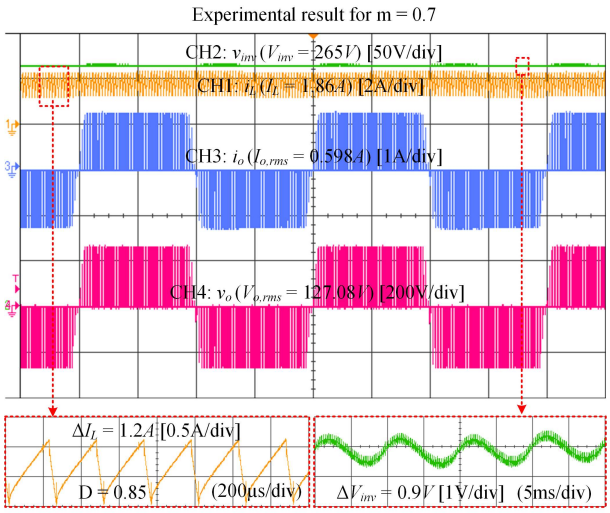

Fig. 21. Experimental results for m = 0.7.

Next, the prototype is tested for m = 0.6 with a higher load resistance of 228Ω and its experimental waveforms are shown in Fig. 20. The measured average dc-link voltage is 234V with input voltage of 50V. Hence, the dc-link voltage gain obtained is 4.68, close to the calculated value of 5. The output rms voltage and current in this case are 111.88V and 0.526A respectively. Meanwhile, the inductor current ripple and dc-link voltage ripple are 1.2A and 0.9V respectively. Subsequently, the experiment is repeated for m = 0.7 with an input voltage of 45V. The average dc-link voltage is measured to be 265V, hence achieving dc-link voltage gain of 5.89 as compared to calculated value of 6.67. Similarly, the prototype exhibits inductor current ripple and dc-link voltage ripple of 1.2A and 0.9V respectively. All experiment further verifies the operation of the proposed S^{3}I inverter.

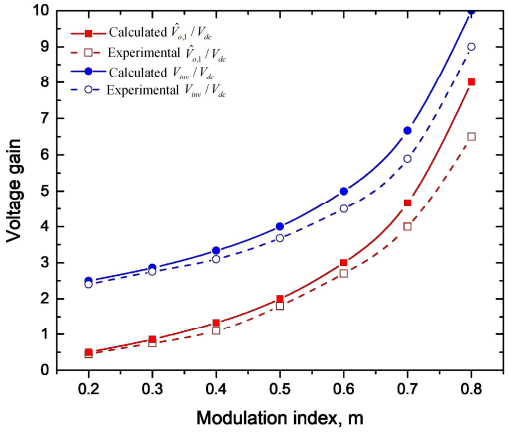

Fig. 22. Experimental voltage gain and dc-link voltage gain as a function of modulation index and the comparison with theoretical calculation.

Fig. 22 represents the experimental voltage gain and dc link voltage gain as a function of modulation index and the comparison with theoretical calculation. The experimental voltage gain and dc link voltage gain are almost equal to

theoretical value with low values of *m* and starts to deviate slightly at higher *m* values. Nevertheless, the results show good agreement between experimental result and theoretical analysis.

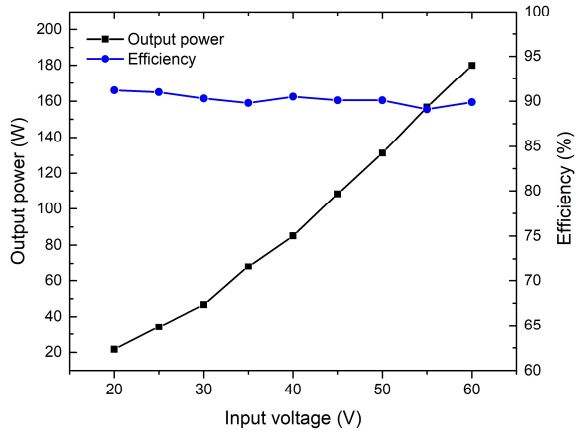

Fig. 23. Output power and efficiency as a function of input voltage for m = 0.5.

Fig. 23 presents the relation between output power and efficiency as a function of input voltage. With constant voltage gain, *RL* load and *m,* the load current can be adjusted by the input voltage which lead to a corresponding change in output power. Hence, output power increases with the increase of input voltage. The experimental prototype exhibits good efficiency from 88% to 92% for the whole range of input voltage.

VI. Conclusion

In this paper, a simplified topology for SSI is presented. Comprehensive analysis and detailed mathematical derivation were conducted followed by simulation studies and experimental testing of a low power prototype. Good agreement among theoretical analysis, simulations, and experiments verified the conceptual validity and operation of the proposed S^3I. It is superior to the recent SSI topologies such that:

- it requires only five semiconductor power devices
- it doubles the voltage boosting gain for a given modulation index , where the gain of the proposed S^3I is $2m/(1-m)$, as opposed to $m/(1-m)$ in other SSI topologies
- its voltage harmonics concentrate around twice the switching frequency and its multiples, as opposed to those concentrate around the switching frequency and its multiples in other SSI topologies
- it reduces power losses for efficiency enhancement

Therefore, the proposed S^3I is an interesting alternative for single-phase dc-ac power conversion system.

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