Properties of Al_2O_3 thin films deposited on 4H-SiC by reactive ion sputtering

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ABSTRACT

In this work, the electrical properties of Al_2O_3 films deposited by reactive ion sputtering were investigated by means of morphological, chemical and electrical characterizations. We observe that the electron trapping affecting the insulating layer is mitigated after a rapid thermal annealing (RTA) treatment. The RTA improved also the permittivity (up to $6\varepsilon_0$), although the negative fixed charge remains in the order of $10^{12}cm^{-2}$. However, the temperature dependent electrical investigation of the metal-oxide-semiconductor (MOS) capacitors demonstrates that the room temperature Fowler-Nordheim electron barrier height of 2.37 eV lies between the values expected for SiO_2/4H-SiC and Al_2O_3/4H-SiC systems.

INTRODUCTION

For several years, silicon carbide (4H-SiC) has been studied considering its potential applications for high power devices. Owing to this continuous impulse of the scientific community, the achievements in material quality and processing maturity led finally to the commercialization of several SiC power devices (i.e., diodes and MOSFETs) and modules [1]. Hence, nowadays novel scientific and technological problems are under consideration to improve or even to go beyond the currently available technologies [2]. In this context, even if SiO_2 is commonly used for 4H-SiC metal oxide semiconductor field effect transistors (MOSFETs) so far, new efforts have been devoted to study and optimize possible novel gate dielectric materials. In particular, the introduction of a dielectric with a high permittivity (*high-k*) is expected to improve the device performance and reliability in high-voltage applications [3], as the gate insulator in 4H-SiC MOSFETs must withstand a high electric field. Specifically, in blocking configuration, the electric field in the gate insulator (E_{ins}) is related to the electric field in the semiconductor (E_s) by the Gauss' law, $E_{ins} = (\kappa_s/\kappa_{ins})E_s$, where κ_{ins} and κ_s are the insulator and semiconductor permittivity values. Hence, in order to mitigate the stress in the gate insulator, its permittivity has to be close to the SiC permittivity.

However, in the choice of an alternative gate dielectric for 4H-SiC devices, the permittivity is not the unique factor to be considered. In fact, the band gap, band alignment and thermal stability are also key parameters. Namely, a high permittivity should be preferably combined with a high barrier height, in order to reduce the leakage current [3].

Because of its interesting properties, such as a high permittivity (κ~7-9), large band gap (~ 6.2 eV as shown in Fig. 1), thermal stability up to 1000°C, and reasonable conduction band offset with respect to 4H-SiC (~ 1.7 eV as shown in Fig. 1), aluminum oxide (Al_2O_3) has already attracted the interest as alternative dielectric in SiC-based devices [4,5]. Typically, the Al_2O_3 films, deposited by chemical vapor deposition (CVD) or atomic layer deposition (ALD), have shown a high trapped charge density (and flat band voltage shifts) and significant hysteresis during cyclic C-V measurements.

In this work, the electrical properties of Al_2O_3 films deposited by reactive ion sputtering were investigated by means of MOS capacitors. The capacitance *vs* voltage characteristics collected on

the different samples revealed the beneficial effect of a rapid thermal treatment that improved the permittivity and reduced the electron trapping in the insulating stack. The hysteresis is strongly reduced after the thermal treatment with respect to the as-deposited sample. Furthermore, temperature-dependent current *vs* voltage characteristics allowed to investigate the conduction mechanisms through the insulating stack, revealing a nearly ideal effective tunneling mechanism with an electron barrier height that lies between the ideal values for SiO_2 and Al_2O_3 layers. However, the low dielectric breakdown field is still a concern that deserves additional improvements. This deposition method is rather cost-effective compared to CVD and ALD and does not present any safety concerns, differently from the case when metal-organic precursors are used.

EXPERIMENTAL

A schematic of the fabricated MOS capacitors and the theoretical band alignment in the investigated 4H-SiC/SiO_2/Al_2O_3 system is reported in Fig. 1. The MOS capacitors were fabricated on n-type epitaxial 4H-SiC layers with a donor concentration of 1×10^{16} cm^{-3}, grown onto heavily doped substrates. First of all, a thermal oxidation in dry O_2 was carried out at 1150°C in order to grow a 6nm thick interfacial SiO_2 barrier layer. This thin oxide layer was introduced to increase the oxide/semiconductor barrier height (up to 2.7 eV). Indeed, in the absence of this thin SiO_2 barrier layer, it was not possible to perform a reliable electrical analysis, due to the high leakage current.

Thereafter, a large area Ohmic contact side was formed on the sample back by Ni-deposition followed by a rapid thermal annealing (RTA) at 950°C [6], prior to Al_2O_3 deposition on the front. The thin Al_2O_3 film was deposited by reactive ion sputtering from an Al target in oxygen ambient at low deposition rate. The reactive ion sputtering was carried out at base pressure of $5x10^{-7}$mbar and generator conditions of 20W, 274V, 50kHz. The resulting deposition rate was 0.4 nm/min. During deposition the sample was placed on a sample holder under rotation at 20 revolutions per minute to reduce materials inhomogeneities. The gate electrode was fabricated by Al sputtering and a sequence of photolithography and wet etch steps.

The electrical characterization of the deposited films was carried by 1 MHz capacitance–voltage (C–V) and current–voltage (I–V) measurements at different temperatures, using a Cascade probe station and a Keysight B5105 parameter analyzer. The morphology of the as-deposited and annealed insulators was investigated using a PSIA XE-150 atomic force microscope (AFM) operating in noncontact mode with highly doped silicon tips.

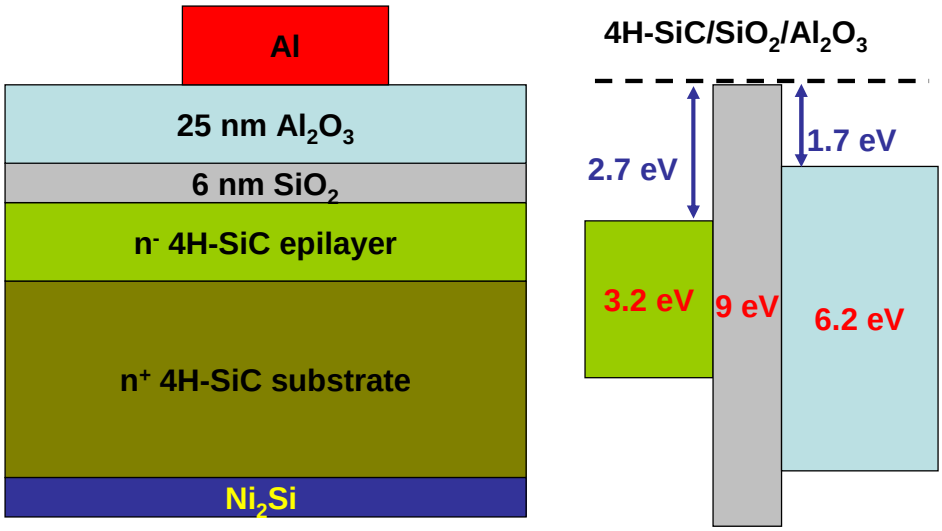

Fig. 1: Schematic MOS capacitor cross section and band alignment diagram for the 4H-SiC, SiO_2 and Al_2O_3 system.

RESULTS AND DISCUSSION

First, the composition and surface morphology of the insulating layers were monitored. The thin film composition was investigated with an ex-situ chemical characterization on blanket samples by XPS (Fig. 2). The position of the peak at 74.1 eV is related to the presence of Al^{3+} species confirming the formation of stoichiometric Al_2O_3. The thickness of this film was about 25 nm, as determined by ellipsometry measurements. Furthermore, the insulating Al_2O_3 films were annealed with a RTA process in N_2 at 800°C for 60 seconds maintaining the amorphous structure. Finally, the film morphology was studied by employing the atomic force microscopy (Fig. 3). The final film is conformal and smooth with a root mean square (RMS) of the height distribution of 2.0 nm and a peak-to-peak value in the order of 8 nm. The MOS capacitors were finalized with the fabrication of the gate electrode on the sample front, by the deposition of 100 nm Al-film and photolithography processes.

Thereafter, the electrical properties of the system were studied by means of I-V and C.V measurements on MOS capacitors.

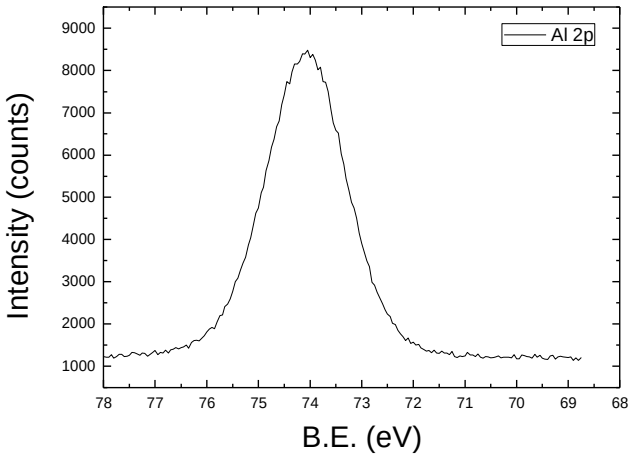

Fig. 2: XPS spectrum collected on the bare insulator surface.

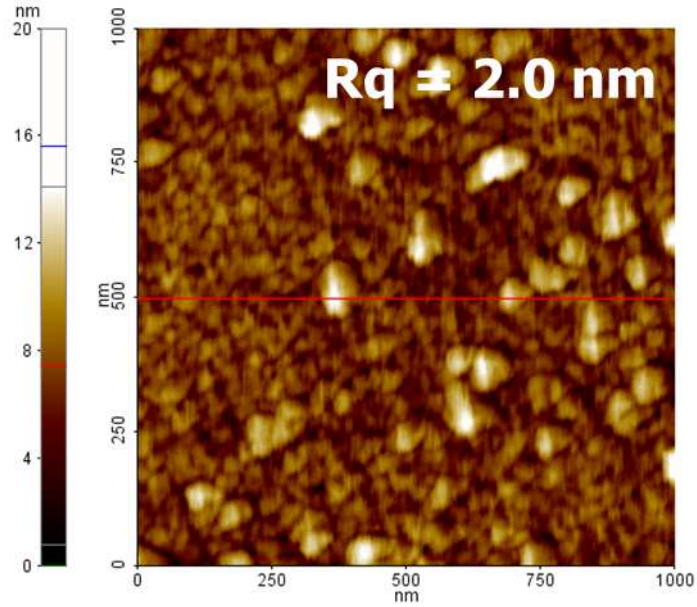

Fig. 3: AFM morphology map collected after the thermal annealing.

Fig. 4 shows the C-V curves acquired at 1 MHz on the MOS capacitors both before and after RTA in N_2. Evidently, before annealing a considerable positive shift of the flat band voltage ΔV_{FB} = +5V is observed after the first bias sweep from depletion toward accumulation. This behavior indicates the presence of a large amount of negative charges inside the oxide, i.e., in the order of $2\times10^{12}cm^{-2}$. After the first measurement, repeated measurements sweeping from depletion toward accumulation and backward, demonstrate that the curves are permanently shifted toward more positive gate bias. Clearly, a stable negative charge trapping occurred during the C-V measurements. Furthermore, from the value of the accumulation capacitance C_{ox} it was possible to estimate a permittivity value of 3.3 ε_0. The permittivity evaluation takes into account that C_{ox} is the series capacitance of the two layers in the insulator stack. The low permittivity value can be attributed to lower density of the as-sputtered film. However, after the annealing at 800°C, an improvement of the C-V curves is observed, as the pristine flat band voltage shift is significantly reduced, thus indicating a drastic decrease of the net negative effective charge in the oxide layer. Furthermore, the C_{ox} accumulation capacitance is increased and considering the physical thickness of the SiO_2 and Al_2O_3 layers, it was possible to determine an increase of the permittivity up to 6 ε_0 for the deposited Al_2O_3 films after the RTA. This value is fully in line with the literature values obtained with other growth methods.

The reduction of the net negative trapped charge in the oxide during the measurements obtained after RTA process is deduced by the significant reduction of the hysteresis in the C-V curves. In fact, as can be observed in Fig. 4, reporting the cyclic C-V curves acquired from depletion to accumulation and backward in the two cases, the hysteresis was almost completely suppressed in the annealed oxide; i.e., in the order of $1\times10^{11}cm^{-2}$. It is worth noting that in literature Al_2O_3 thin films synthesized using different techniques (e.g., ALD) suffer of similar electron trapping phenomena, likely due to the presence of oxygen vacancies [7].

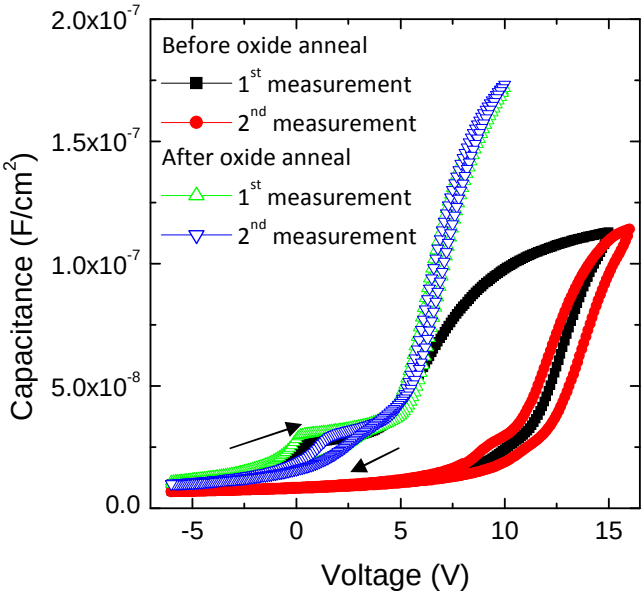

Fig. 4: C-V curves collected on Al_2O_3/SiO_2/4H-SiC MOS capacitors after two consecutive bias sweeps from depletion to accumulation, both for the as-deposited sample and for the sample subjected to RTA at 800°C

Comparing the C-V curves on the as-deposited and annealed samples it is possible to notice that the flat band voltage (V_{FB}) ranges in both cases between + 6V and + 7V. The V_{FB} is far from the ideal value (~0V), thus indicating the persistence pre-existence of a residual negative fixed charge , i.e., in the order of $2\times10^{12}cm^{-2}$. Furthermore, the forward curve – from depletion to accumulation –

shows a knee that is nearly absent in the reverse curve indicating the occurrence of energetically deep interface states trapping (in the order of $1\times10^{12}cm^{-2}$).

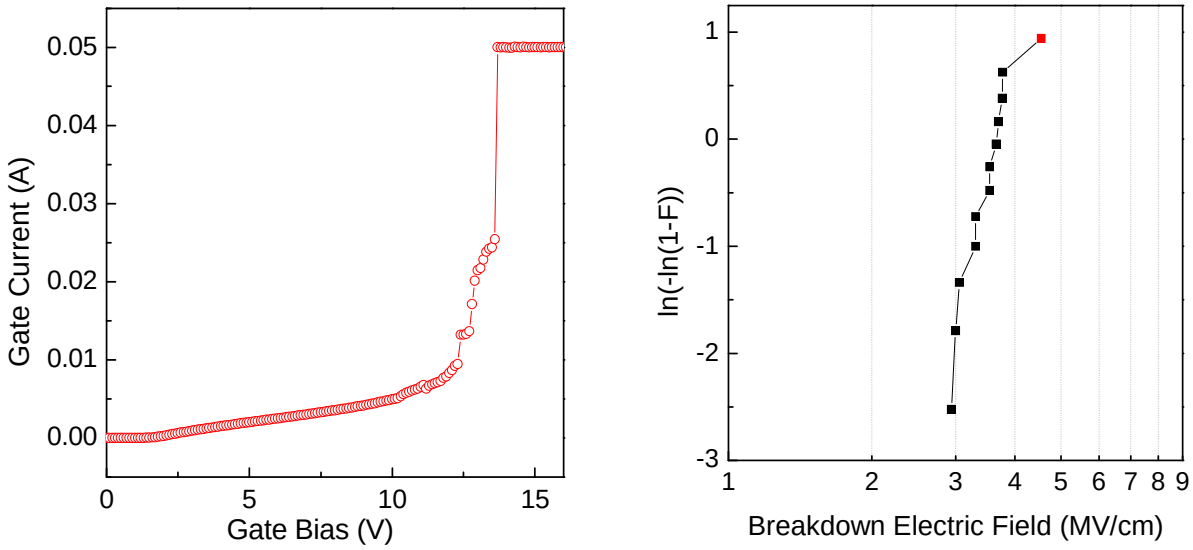

Fig. 5: (a) Example of BD I-V curve collected on a MOS. (b) Weibull statistic collected on 15 fresh MOS devices.

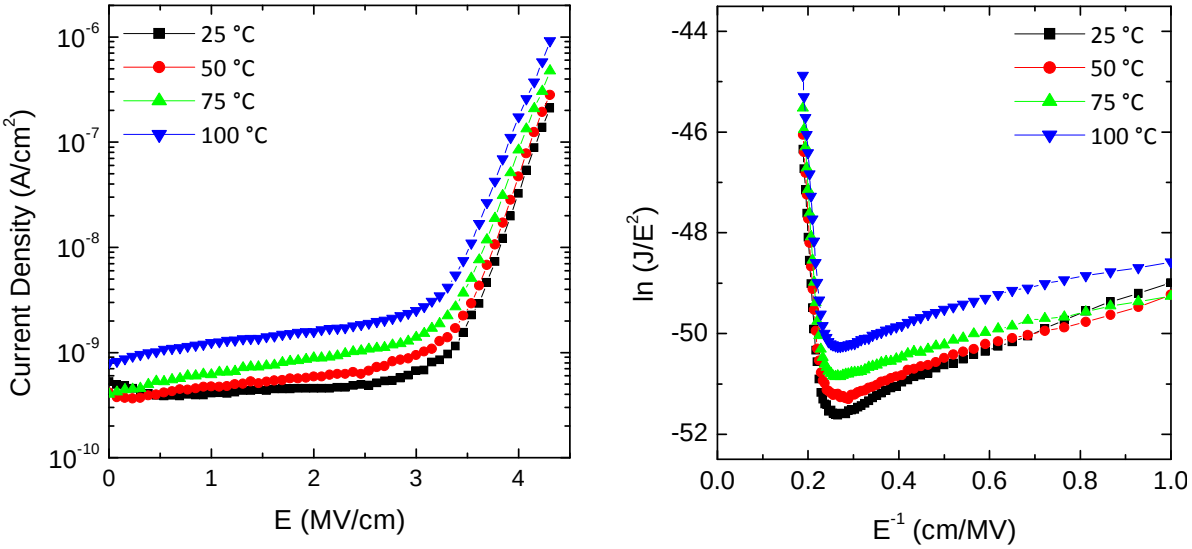

Fig. 6: (a) Current density vs electric field at different temperatures (b) Temperature dependent FN plots $\ln(J/E^2)$ vs E^{-1} curves from room temperature up to 100 °C.

Another important aspect of the characterization comes from the gate dielectric breakdown (BD) statistics. Fig. 5a shows a I-V characteristic collected for a MOS capacitor. The I-V curve shows a dielectric breakdown of the oxide occurring at approximately 14 V, corresponding to an electric field of 4.5 MV/cm. By performing statistical measurements on capacitors, we are able to apply the Weibull formalism to the experimental breakdown data. In particular, the Weibull distribution is given by [8]

$$F(x) = 1 - exp\left[-(x/\alpha)^{\beta}\right].$$

where F is the cumulative failure probability (representing in our case the ratio between the failed and the investigated MOS N_f/N_i), x is the electric field that induces the BD phenomena, α is the characteristic lifetime of the dielectric, and β is called the Weibull slope. In particular, the ln[-ln(1-F)] of the MOS capacitors is plotted versus the natural logarithm of the BD electric field. As a

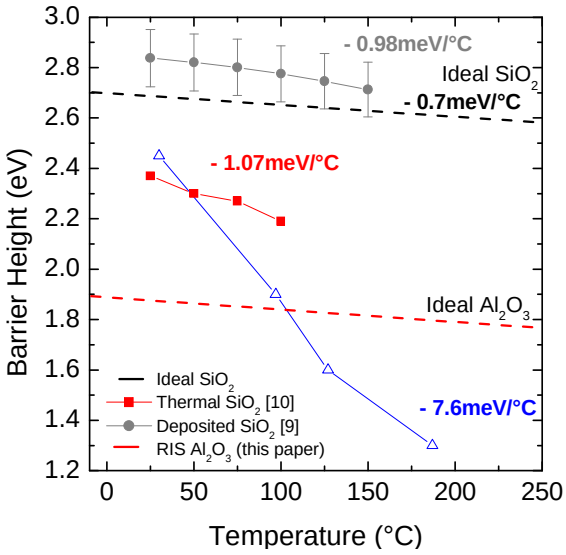

Fig. 7: Comparison between the experimental electron barrier height for the SiO_2/Al_2O_3 stack (this paper) and literature data on SiO_2, and the theoretical behavior.

consequence, the more robust is the insulator the larger the β value is and the steeper the Weibull plot is. As can be seen in Fig. 5b the BD occurred mostly between 3 and 5 MV/cm on the investigated MOS capacitors. However, even if the BD statistic is centered in a narrow electric field range (3-5 MV/cm), it is far away from the ideal value (~10MV/cm). This result suggests that some extrinsic contribution (i.e. the insulator surface roughness) can enhance the dielectric breakdown lowering the mean critical electric field value.

The insulating properties were also studied by monitoring the temperature dependence of the I-V characteristics of MOS capacitors, from room temperature up to 100 °C.

Once a MOS device is stressed and the electron trapping occurred, it becomes stable and it is possible to compare the I-V collected at different temperature. The I-V characteristics were analyzed using the Fowler-Nordheim (FN) formalism and the Lenzlinger-Snow (LS) equation:

$$ln\left(J/E^2\right) = ln\left(\frac{q^3\left(m_{SiC}/m_{ox}\right)}{8\pi h\Phi_B}\right) - \frac{8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qh}\frac{1}{E}$$

where J is the current density, E is the electric field across the oxide, m_{SiC} and m_{ox} are the effective electron masses in the SiC substrate and in the insulator, respectively, q is the electron charge, h is the Plank constant and Φ_B is the effective tunneling barrier height for electrons [9]. By the fits (not shown) in the linear region of the "FN plots" $\ln(J/E^2)$ *vs* 1/E shown in Fig. 6b, it was possible to determine the values of Φ_B for electrons as a function of the temperature.

As shown in Fig. 7, the FN tunneling can be used to describe the current conduction mechanisms of the system. In fact, ideally the FN tunneling possesses a weak temperature dependence, related to the shrinking of the SiC and insulator band gaps with increasing temperature [9]. On the other hand, it has been demonstrated that thermally grown SiO_2 layers onto 4H-SiC may contain residual carbon atom content that can affect the insulating properties of the gate oxide [10]. In defective insulators Poole-Frenkel (PF) emission can often rule the conduction mechanism. The ideality of the tunneling mechanism can be investigated looking at the variation of the fitting barrier height value and in particular looking at its slope $d\Phi_B/dT$. In literature, some thermal oxides grown onto 4H-SiC shown an experimental $d\Phi_B/dT$ slope (−7.6 meV/°C) one order of magnitude higher than the theoretical (−0.7 meV/°C) one and the experimental $d\Phi_B/dT$ slope (−0.98 meV/°C) of the deposited oxide, respectively [9,10].

Fig. 7 shows how both our experimental results, literature data and the ideal values of the electron barrier height Φ_B vary with a temperature increasing from 0 °C up to 250 °C for the SiO_2 and the Al_2O_3 cases. The ideal SiO_2 FN case possesses a barrier height Φ_B = 2.7 eV while ideal Al_2O_3 FN case possesses a barrier height Φ_B = 1.9 eV. In both cases the barrier height decreases with a slope of the $d\Phi_B/dT = -0.7$ meV/°C [11] with increasing temperature.

On the other hand, the experimental effective barrier height for the SiO_2/Al_2O_3 stack is Φ_B = 2.37 eV at room temperature, i.e., larger of the ideal value expected for Al_2O_3/4H-SiC interface and smaller than the SiO_2/4H-SiC interface. This result suggests that the FN formalism averaged the effective double tunneling occurring on the SiO_2/Al_2O_3 stack. However, an indication of the good quality of the insulating stack is obtained considering that the experimental slope of the $d\Phi_B/dT$ is −1.07 meV/°C is only slightly larger than the ideal value of − 0.7 meV/°C. Indeed, the experimental results on the SiO_2/Al_2O_3 stack are improved compared to some thermally grown SiO_2 layers [10].

CONCLUSIONS

In this paper, we have investigated the morphological, chemical and temperature dependent electrical properties of Al_2O_3/SiO_2/4H-SiC system in MOS capacitors. The Al_2O_3 films were grown by reactive ion sputtering onto a thin thermal SiO_2 layer. The insulating layer suffers from an electron trapping that is mitigated after a RTA treatment. The RTA improved also the permittivity, without significantly reducing the negative fixed charge. The temperature dependent electrical investigation of the MOS capacitors resulted in a Fowler-Nordheim barrier height of 2.37eV. The Fowler-Nordheim-like tunneling has been proved by monitoring the temperature coefficient of the electron barrier height ($d\Phi_B/dT$), which resulted noticeably improved with respect to thermally grown SiO_2 layers.

These preliminary results suggest that reactive ion sputtering can be a promising technique to synthesize novel gate dielectric for wide band gap semiconductor devices technology, even if the fabrication processing need to be improved in order to overcome some reliability issues.

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