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Electronic Packaging for Functional Electronic Textiles

by

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Abstract

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An electronic textile (e-textile) is a textile with integrated electronic functionality. It can be used in many areas, for example, clothing, medical, furniture and aerospace applications. The combination of electronics with textiles requires the use of flexible circuit technology, with electronic components mounted on polymer substrates with conductive tracks, to ensure the textile retains as much as possible their normal physical characteristics and feel. E-textiles in wearable applications are subject to human motion activities and as such the integrated electronic components can be vulnerable to different kinds of stresses such as bending. These forces can potentially shear, pull off or damage the components despite the electronic packaging methods used to protect them. Similarly, temperature changes in the environment can induce thermal expansion stresses in the electronic packaging or components which may result in failure. Therefore the need to develop a new reliable electronic packaging method for e-textiles to mitigate these stresses becomes increasingly important.

This thesis presents research into a new reliable packaging technique capable of protecting components against twisting, bending or shear stresses. The use of this packaging technique has been evaluated with the ultra-thin die mounted onto thin flexible polymer film strip which contains conductive tracks for electrical interconnections and power supply for electronics. This electronic strip can be subsequently formed into yarns or woven into a textile. The review of electronic packaging techniques for forming electronic connects between the die and substrate such as flip chip bonding, anisotropic adhesives bonding and wire bonding are also included in this thesis.

Finite element analysis (FEA) of the electronic strip is also presented. FEA simulations are used to evaluate the mechanical performance of different electronic packaging assemblies. An FEA investigation is presented in the materials and component dimensions in order to maximize the reliability of the packaging method. The three-point bending, shear, tensile and thermal expansion modelling have been simulated and, in the case of shear load and bending, results validated against an experimental evaluation. The shear and bending experimental results show good agreement with the simulation results and verify the

simulated optimal thickness of the adhesive layer. Three under-fill adhesives (EP30AO, EP37-3FLF and Epo-Tek 301 2fl), five highly flexible adhesives (MK055, Nu355, Loctite 4860, Loctite 480 and Loctite 4902) and three substrates (Kapton, Mylar and PEEK) have been evaluated and the optimal thickness of each is found. The Kapton substrate, together with the EP37-3FLF adhesive, was identified as the best materials combination, with the optimum under-fill and substrate thickness identified as 0.05 mm.

A novel method for packaging electronics using a thermally deformed Kapton was introduced. The design process for the jig that was used to deform the Kapton and the minimum temperature (360 °C) and time (60 Sec) needed to deform the Kapton has been investigated. This is also the first demonstrated method for reliably incorporating electronic circuits in a textile and that can withstand up to 45, 150,000 and 1470 cycles of machine washing, 180 degree twist test and 90 degree bending test respectively. The new ultra-thin silicon chip (0.025 mm thickness) fabrication method has also been introduced in this thesis to increase the flexibility of the electronic packaging method for functional electronic textiles.

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Abbreviations

3D	Three dimensional
ACA	Anisotropically conductive adhesive
ACF	Anisotropic Conductive Films
BGA	Ball grid array
COF	Chip on flex
CTE	Coefficients of thermal expansion
EPSRC	Engineering and Physical Sciences Research Council
LGA	Land grid array
LCP	Liquid crystal polymeric
FEA	Finite Element Analysis
PET	Polyethylene terephthalate
PCB	Printed Circuit Board
PEN	Polyethylene Naphthalate
PVC	Polyvinylchloride
PI	Polyimide
SMD	Surface-mount device
SOI	Silicon on Insulator
WLP	Wafer level package
EDIP	Electronic bare die in plastic

Chapter 1 Introduction

1.1 Research motivation and objectives

In today's society, microelectronics technology plays a very important role in people's lives evidenced by the abundance of devices such as mobile phone and laptops. Electronic textile (e-textile) technology seeks to personalize the microelectronics technology by combining electronics with textiles to provide a more convenient and comfortable access to the electronics.

The concept of combining textiles with electronic functionality is not new and many examples of the technology have been demonstrated. Early medical sensing vests, for example, incorporated knitted electrodes for ECG monitoring and piezoresistive motion detection [1]; sweat monitoring sensors were also located in a silicone patch that was subsequently mounted on the textile [2]. However, electronics functionality was provided by conventional printed circuit board (PCB) modules located in pockets and connected by cables. Commercial electronic textile offer similarly limited integration of the electronic circuit functionality within the textile. The limitation of rigid electronics in flexible applications was addressed in part by the FP7 project STELLA. This project developed stretchable meandering copper interconnections and embedded ultra-thin silicon die in silicone [3]. These stretchable circuit boards still contain rigid islands and have to be subsequently attached to textiles and the use of silicone reduces the breathability of the textile. The current production of e-textiles is limited by the flexibility and reliability of these approaches, their failure to withstand standard machine wash cycles and the size of mounted electronic components which alter the feel of the textile.

This thesis focuses on realizing reliable electronic packaging for mounting ultra-thin die onto the plastic substrate that contains conductive interconnects and bond pads for interconnecting the packaged die to other electronic components or power supplies to achieve flexible and reliable e-textiles product [4]. Each packaged die will form a die pod, conductive interconnects used to link die pod together to forming an electronic filament [4]. The textile fibres will be used to surround electronic filament and connected to conductive wires to form an electronic yarn as shown in Figure 1 [4]. This research is being carried out under the EPSRC project “Novel manufacturing methods for functional electronic textiles” [4]. These yarn can be woven or knitted together form an integrated e-textile with the electronic functionality hidden inside the yarns.

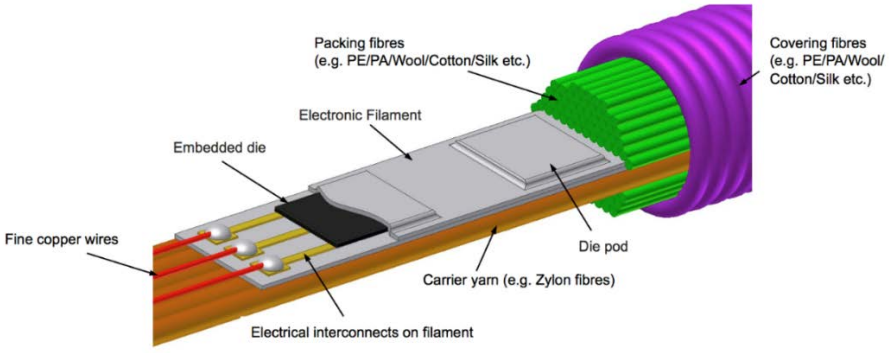


Figure 1. Schematic of electronic filament inside yarn [4].

However, the stresses induced within the flexible circuit strip that forms the electronic textile cause failure in the packaging of the electronic components. In this thesis, stress analysis of the flexible electronic strip with the different die, adhesive and substrate thicknesses and materials has been explored using Finite Element Analysis (FEA) and experimental evaluation allowing the optimal size and packaging approach to be identified that achieves reliable operation. The thesis explores novel encapsulation processes and evaluates these using bespoke text circuits fabricated using ultra-thin die.

The objectives of this research are as follow:

1. To determine suitable adhesive and substrate material for electronic packaging in electronic yarn to minimise stresses inside the electronic package.
2. To determine the optimal thickness of the die, adhesive and substrate for electronic packaging to minimise the stresses and packaging size.
3. To develop manufacturing processes to located die as close as possible to the neutral axis of the electronic package.
4. The development of a novel electronic packaging method for the electronic filament to provide waterproofing and improved reliability and flexibility of the package. The development of washing, twisting and bending experimental to test the novel packaging method to compare with conventional techniques e.g. glob top.
5. To experimentally evaluate packaging performance and reliability during washing, twisting and cyclical bending test, in the washing and cyclical bending test the electronic package has been weaved into the textile, the samples of package stripe without textile have been tested in twisting test.
6. To investigate the processes to fabricate ultra-thin silicon chip (0.025 mm thickness) to increase the flexibility of the flexible circuit and to package this in a reliable manner. The ultrathin die

will be fabricated using a sacrificial process to etch the buried oxide layer in SOI wafers to achieve 0.025 mm thick chips.

1.2 Statement of novelty

The novelty of this thesis are as follow:

1. An ANSYS stress analysis simulation method has performed to enable to the identification of the best size and material of die, substrate and adhesive for maximising the reliability of the electronic packaging.
2. A novel flip chip on flex electronic packaging method has been developed to achieve waterproof and minimizing stresses inside the package has discussed in this thesis.
3. To achieve more flexible electronic package the new process to fabricate ultra-thin electronic chip also been described in this thesis.

1.3 Electronic textiles

E-textiles are a type of fabric that incorporate electronic components and devices, and they are also known as smart fabrics. An e-textile is a textile with integrated electronic functionality and examples include a wearable medical sensor developed to monitor physiological health or to identify the potential threats to the health of the wearer [5]. Another example is the wearable electrochemical sensor (as shown in Figure 2) on underwater clothing that can detect environmental pollutants in marine environments [6]. These examples demonstrate the potential applications and importance of the electronic textile technology and further applications will develop as the technology matures.

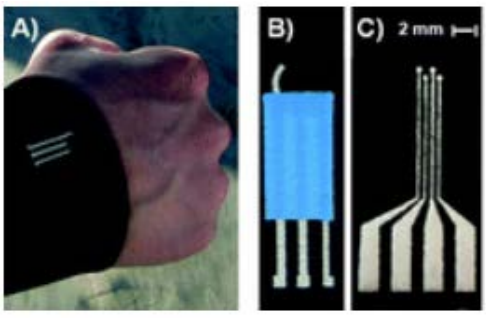


Figure 2. (a) Wearable electrochemical sensor, (b) and (c) two type of screen-printed electrode design [6].

Typical example of an e-textile system consists of an electrical network, sensor, processing unit, power supply and communications. The electrical network is used to transmit signals and power within the

textile and the communications component can transmit data to external networks. Sensors are used to detect required environment data or biometric data. The processing unit analyses acquired data and stores data and the power supply provides the electrical power to run the electronic textile system. A stable electronic textile system can independently detect, process and transmit data just like a normal electronic system. The applications of e-textiles are broad. It can be used to sense tank movement [7], support networks and communications for military use [8]. For home use, it can be used to detect noxious chemicals after refurbishing the house and also can be used to detect the movement of people in a smart home [7]. For medical use, it can be used to diagnose cardiovascular disease and can also be used for general surgery and wound care. E-textile technology is wildly used for the medical and military applications [7-12].

1.4 Thesis outline

Chapter two reviews the different types of electronic packaging technologies and the related examples for each type. The four electronic package failure test modes reviewed in this chapter are briefly introduced the different modes to detect the mechanical strength of the electronic package. Chapter three presents the theory around the different types of stresses that are important considerations in packaging. The four theories of failure for materials are discussed to ascertain the most significant stresses that are largely responsible for failure in electronic packaging. The chapter also introduces four different simulation models and boundary conditionals to determine the optimal material and thickness for the electronic package. Chapter four describes FEA methods for stress analysis, the stress simulation results have been obtained using ANSYS. Chapter five covers the validation of the simulation results by comparison with the experimental work. Chapter six describes a novel electronic packaging method and the experimental evaluation of this new approach. Chapter seven discusses an ultra-thin chip fabrication process and the results from packaging this thin die. Chapter eight includes the conclusion and future works.

1.5 List of publications

Menglong Li, John Tudor, Russel Torah and Steve Beeby “Stress analysis of flexible packaging for the integration of electronic components within woven textiles”, 2017 IEEE 67th Electronic Components and Technology Conference (ECTC).

http://ieeexplore.ieee.org/document/7999977/

Menglong Li, John Tudor, Russel Torah and Steve Beeby “Stress analysis and optimization of flexible electronic packaging for functional electronic textiles”, IEEE Transactions on Components, Packaging and Manufacturing Technology. 2017.

https://ieeexplore.ieee.org/document/8240725/

Menglong Li, John Tudor, Jingqi Liu, Komolafe Abiodun, Russel Torah and Steve Beeby “The thickness and material optimization of flexible electronic packaging for functional electronic textile”, 2018 IEEE 20th Design, Test, Integration and Packaging of MEMS/MOEMS Symposium.

https://ieeexplore.ieee.org/document/8394186/

Menglong Li, Russel Torah, Jingqi Liu, John Tudor and Steve Beeby “Finite element analysis (FEA) modelling and experimental verification to optimise flexible electronic packaging for e-textiles”, Journal of Springer Microsystem Technologies (submitted).

Steve Beeby, Russel Torah, John Tudor, Menglong Li, Komolafe Abiodun and Kai Yang, “Functional Electronic Textiles: Circuit Integration and Energy Harvesting Power Supplies” 2018 IEEE International Flexible Electronics Technology Conference (accepted).

A O Komolafe, R N Torah, Y. Wei, H Nunes-Matos, Menglong Li, D. Hardy, T. Dias, M J Tudor and S P Beeby, “Flexible thin film circuits for yarn based e-textiles”, Journal of IOP Smart materials and structures (submitted).

Menglong Li, John Tudor, Russel Torah and Steve Beeby, “Novel electronic packaging method for functional electronic textiles” IEEE Transactions on Components, Packaging and Manufacturing Technology (submitted).

Menglong Li, John Tudor, A. Komolafe, Russel Torah and Steve Beeby, “Ultra-Thin chip fabrication for functional electronic textiles” Journal of IOP Smart materials and structures (ready to submit).

1.6 Patent

Electronic encapsulation method for reliable and washable e-textiles (submitted)

Chapter 2 Literature review

The durability and wear ability of electronic textiles require that the integrated electronics and their electrical interconnections are reliably packaged. This chapter reviews the different electrical interconnections and packaging technologies reported in the literature. To identify the significance of the novel packaging technology proposed in this thesis, the limitations of these technologies in improving the durability of e-textiles against mechanical stresses resulting from shearing, bending and washing are also discussed [13, 14].

For e-textiles to be truly wearable, they have to be flexible [15]. To improve the flexibility, it is necessary for the thickness of the packaged chip to reduce considerably beyond 0.2 mm [16], which is the size of the smallest commercially available two-terminal resistors. This chapter hence reviews the fabrication methods for ultrathin chips of the thickness not more than 25 µm to enable the fabrication, integration and testing of ultra-thin chips in fabrics as described in chapter seven of this thesis.

2.1 Electronic textile-background and state of the art

In the early 1990s, smart clothing technologies were introduced by MIT students for military use. They have combined conductive structures, colour changing materials and electronics into soft interfaces [17], but the product is not wearable and very cumbersome to move around in. The more wearable e-textile technology have been introduced by Levi Stauss and Phillips electronic company, they have produced a commercial wearable electronic cloth for fashion [18]. The more functionalities of e-textiles have been introduced in 2001, the medical vest technology (as shown Figure 3) which was demonstrated by ZOLL Life Vest Company use sensing electrodes to detect heart diseases and to continuously monitor the patient's heart, this demonstration brings the medical functionality to e-textiles [19]. However, electrical interconnections are still achieved with standard rigid cables.

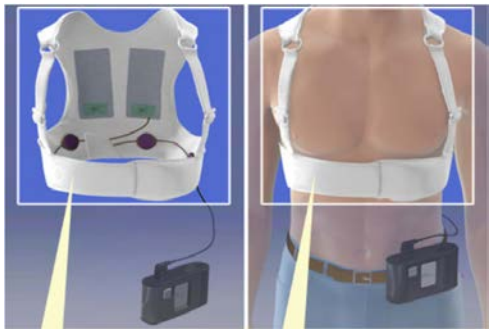


Figure 3.medical vest demonstrated by ZOLL Life Vest Company [19].

To increase the flexibility and reliability of e-textiles. The Wearable Computing Lab at ETH Zurich [20] developed an approach for embedding electronic chips in fabrics by weaving flexible electronic plastic strips (e-strips) into textiles as shown in Figure 4. Electronic functionalities such as temperature, humidity sensing and LED lightings on the fabric have been demonstrated. Similarly, Matijia Varga et al. also reported sandwiching thin film electronic circuits between two plastic substrates to form the e-textile composite circuit, the top and bottom plastic substrates both contain conductive tracks for providing electrical interconnections as shown in Figure 5 [21]. In 2015, Tilak Dias and A.Ratnayake [22] reported embedding semiconductor micro-devices are directly within the fibres of yarn, and these electronically functional yarns will be incorporated into fabrics using conventional textile machinery or used as sewing thread in garment manufacture to maximise the flexibility of e-textiles as shown in Figure 6. However, those researches either did not protect the components and circuit or evaluate the ability to withstand bending, shearing, tensile, thermal load and washing.

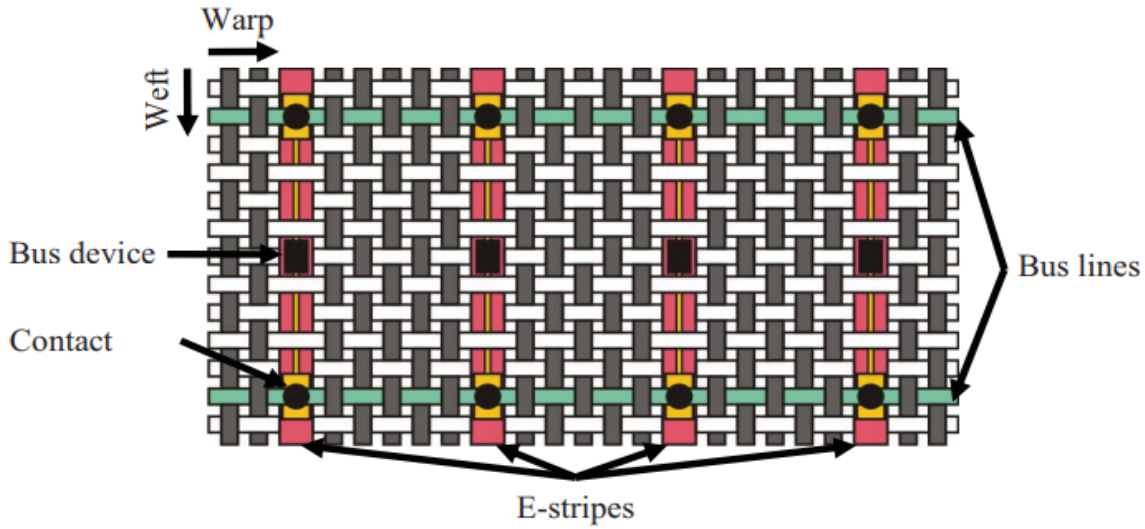


Figure 4.Schematic of integrated electronic plastic strips into a woven textile[20].

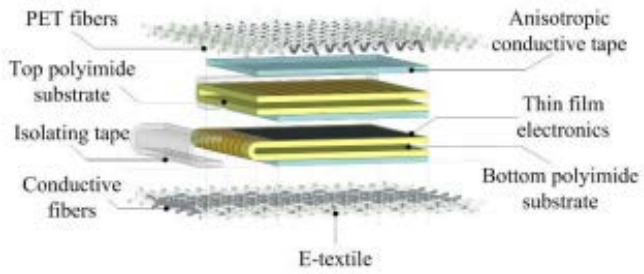


Figure 5.Schematic of packaging thin film electronics in between top and bottom plastic substrate [21].

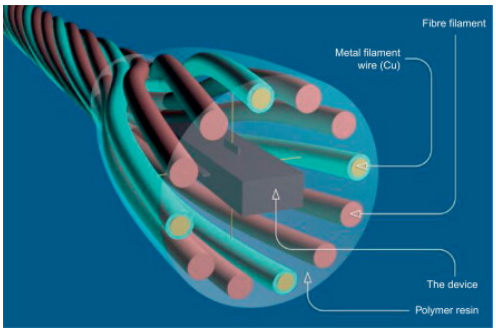


Figure 6.Schematic of electronic functional yarn [22].

2.2 Challenges to electronic textile

Currently, the design of electronic textile is challenged by several issues which are:

1. The poor reliability of the electrical interconnections for connecting embedded electronic component to other electronic component or power supply.
2. The lack of reliable packaging and waterproof methods for the electronic components within textiles.
3. In the real applications, e-textiles are subject to bending due to the movement of the wearer. Consequently, the electronic components within textile are also bent and could potentially get damaged. The lack of stress analysis to optimise the packaging material and the package size for durability against bending stresses.
4. The flexibility of electronic textile is still poor due to the use of thick electronic chips.

Hence, this thesis aims to investigate and develop a reliable electronic packaging method for mounting ultra-thin die onto plastic substrates that would be woven alongside textile fibres into an electronic yarn. The textile fibres add extra protection to the electronic plastic strip and are connected to power supply or an external system via conductive wires that do not comprise the flexibility, reliability and wash ability of the electronic circuit. The possible electrical interconnection technology for connecting the electronic plastic strip is first discussed.

2.3 Conductive interconnection on textile

Conductive interconnection is crucial to the functionality of electronic textiles. It provides data and electrical power transmission between the electronic devices integrated on the textile and to supply power to them. A variety of conductive interconnection materials with related examples are presented in the following section.

2.3.1 Conductive functionalized fibres

Electrically conductive fibres are used in many areas such as in electronics manufacturing, medical and military applications [13, 23, 24]. They have been used in textiles for control of static electricity, power supply, connections for data and heating [13].

Electronic conductive fibres are formed by three different manufacturing methods which are by coating, blending and integrating the textile fibres with electrically conductive materials [25]. The two types of conductive coatings used for electrically conductive fibres are metal coating and conducting polymer coating of the textile fibres [26]. Figure 7 shows a metal coated textile fibres with aluminium coatings [27]. By changing the top cover layer of the metal-coated fibre to a conducting polymer, a conducting polymer coated fibre is realised. Metal/ conductive polymer coated fibres are more flexible but less conductive than metal fires. The disadvantages of metal/ conductive polymer coated fibres is the quick degradation in their conductivity which results from the poor adhesion the coatings to fibres [28, 29].

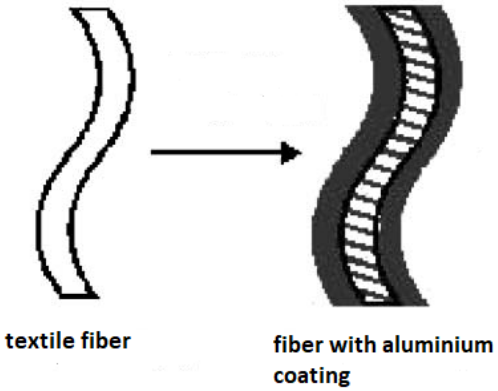


Figure 7. a metal coated textile fibre with aluminium coatings[27].

2.3.2 Conductive polymer

The polymer is usually used as an insulation material because of its low electrical conductivity. With some fillers in the polymer, it can become a thermally and electrically conductive material. The benefits of conductive plastics are their lightness, high tensile and compressive strength, easy to process, ecological, cost-effective and adjustable electrical conductivity [30, 31]. Conductive plastics are typically used in heating element, detection sensor, air cleaning system and metal replacement solutions etc. [31]. The disadvantage of this conductive polymer is low electrical conductivity [31].

2.3.3 Conductive functionalized yarn

Conductive yarn contains a mixture of the conductive material such as gold, steel, aluminium etc. and non-conductive textile yarns. Conductive yarns are include metal- wrapped yarn, metal-filled yarn, metal yarn [32] and metal coated yarn. The metal-wrapped yarn is formed when one or more conductive wires are wrapped around a strand of non- conductive yarn as shown in Figure 8a. In Metal-filled yarn, a conductive wire as a core and non-conductive fibres are used to cover conductive wire as shown in Figure 8b. The covering fibres protect the wire core [32]. Metal yarn does not have any core structure instead of a metal fibre is used to replace one strand of the textile yarn (see Figure 8c). The conductive yarn also can be achieved by coating conductive metal (such as gold, steel, aluminium etc.) onto textile yarn. In metal-wrapped, metal-filled and metal conductive yarns, the flexibility of textile yarns is significantly compromised due to the stiffness of the conductive material. Compare to the coated yarn, the conductive yarn has less flexibility but more conductivity.

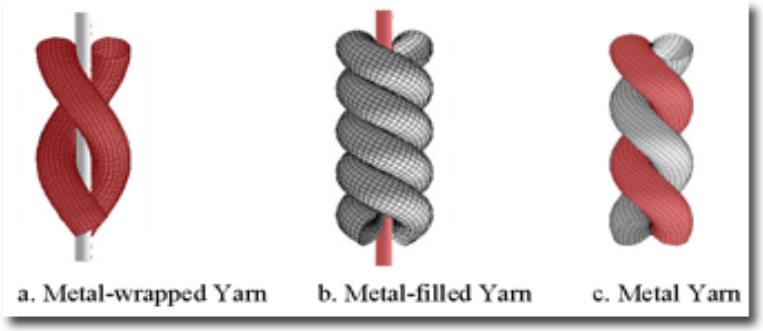


Figure 8. Three types of conductive yarns: (a) Metal-wrapped yarn, (b) metal-filled yarn, (c) metal yarn [26].

In 2017, Yong Ju Yun et al. reported a highly conductive and environmentally stable gold/ graphene yarns, they fabricated the gold/graphene yarns through a facile method by the electroless deposition of gold nanoparticles onto the surface of graphene yarns as shown Figure 9, and the gold/graphene yarns are fabricated using a completely solution-based process [33]. These new conductive yarns are more flexible than the common conductive yarn because of the less metal material used in this yarn.

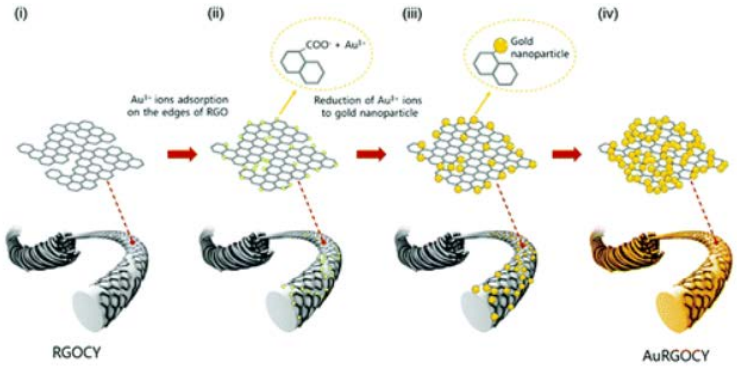


Figure 9.Schematic illustration for fabricating the gold/graphene yarns [33].

Conductive fabric is a textile with an electrical functionality. It is produced by integrating conductive yarns into fabrics. The integration methods include weaving, knitting, sewing and e-broidery [32, 34, 35]. The production of a conductive fabric is complicated by the need to ensure that the fabric is both flexible and conductive.

An example of using conductive fabric was introduced by Masayuki Inaba et al. [36], they used electrically conductive fabric to produce a full-body sensor suit. A total of 192 sensors were integrated into this suit and each sensor worked as a binary switch. The conductive fabric was used to provide electrical connection and data transmission from each sensor to the sensor processor [36]. Each sensor element in this suit was formed by six layers (see Figure 10) and each layer has they own functionality. Layer 1 and layer 6 are normal textile layers to protect the sensing part. Layer 2 is the wiring layer which provides an electrical connection between layer 3, the switch pattern and layer 5, the electrically conductive fabric. Layer 4 is a spacer layer that prevents a short circuit between layer 3 and layer 5. In contrast to the electronic yarn technology investigated in this report, the total thickness about 0.7 mm for this packaged textile sensor is increased by the stacking of six different layers and consequently reduces the flexibility of the textile sensor.

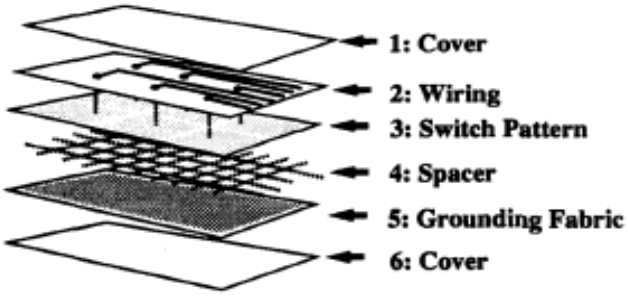


Figure 10.Structure of a textile sensor [36].

A comparison of these three interconnections shows that conductive polymers are unsuitable for providing electrical interconnection between plastic electronic strip (as shown Figure 1) to the external electronic module or power supply due to their low electrical conductivity. When more conductivity is required, conductive yarns are better while conductive fibres give more flexibility [37].

2.4 Conductive interconnection for a plastic substrate

In this research, plastic electronic strips containing conductive interconnects, electronic components and bond pads are to be woven or knitted with textile fibres to form an electronic yarn. This makes the plastic circuit technology central to the electronic yarn approach discussed in this thesis. Since the plastic strip is flexible, it is used as a carrier of the electronics and to provide electronic interconnection to each die pods in the electronic yarn. The typical conductivity range for a contacting sensor (basic electronic functional) is 0.01 to 50, 000 uS/cm, therefore the conductivity of interconnection onto plastic strip should be in range of 0.01 to 50, 000 uS/cm. The three main technologies to fabricate flexible circuit are ink-jet or screen printing approach and wet etch for copper clad Kapton [38-40], the washing test has undertaken in chapter six to compare the conductivity and reliability of those three technology.

2.4.1 Printed interconnections on plastic substrates

Electronic circuit printed onto a plastic substrate can increase the flexibility of circuit system compared with the traditional rigid PCBs [40]. Ink-jet and screen printing techniques are the two main printing methods for plastic circuit [38, 39]. Conductive inks are printed as conductive tracks on a plastic substrate to produce a flexible electronic circuit, the small surface mount or bare die electronic components can be bonded to this flexible electronic circuit by using soldering paste or conductive adhesive. This enables true electronic functionality to be realised on the surface of the fabric and the small size of the electronic components minimises the impact on the properties of the fabric [41]. The disadvantage of the printed flexible electronic circuit is the durability of these circuits is poor with cracks developing in the conductive inks and conductive adhesives due to mechanical forces and bending [42].

Electrically conductive silver ink patterns on paper, polyimide, polyethylene terephthalate (PET), fabric and polyvinylchloride (PVC) were reported by S.Merilampi et al. [38], the screen printing method was used to print conductive silver ink onto those flexible substrates. The electrical properties of the samples

were been measured and compared in variable curing time and temperature [34]. The resistance of conductive patterns by using polyimide is much lower than other flexible substrate material.

Kyoohee Woo et al. reported the use of ink- jet printing method to print Cu-Ag-based conductive tracks onto polyethersulphone substrate as shown in Figure 11[39]. Compared to the Cu metal film, the Cu- Ag film has higher conductivity. Kapton polyimide is a commonly used substrate for the flexible plastic circuit, A.Moya et al. [43] have also introduced the using ink-jet printing to print PH sensors onto Kapton polyimide film in 2017.

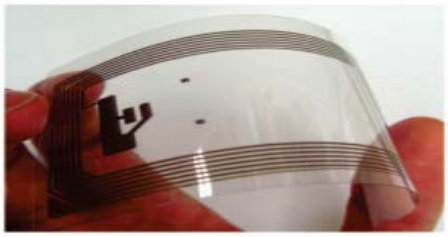


Figure 11. Ink-jet printed Cu-Ag-based conductive tracks onto plastic substrate [39].

2.4.2 Etched interconnections on plastic substrates

Metallic films that are adhesively bonded to plastics have been used to achieve flexible plastic circuit/PCB board. Flexible PCB's give you the freedom to wrap your Printed Circuit Board around corners and create the flat board to board connections [44]. The copper clad Kapton is a commercially available product. The copper film is adhesively bonded to the Kapton otherwise known as polyimide. The other plastic substrate typically used for flexible PCB manufacture is the Polyester film or Mylar [44].

Ckharnett et.al. reported a copper clad Kapton plastic circuit (as shown in Figure 12) fabrication method [40]. This plastic circuit was patterned using a wet copper etch and a resist masking layer. In their method, the resist masking layer is simply deposited onto copper clad Kapton by using the solid-ink printer. The circuit design can be drawn with any graphics program and printed on the copper clad Kapton sheet in black ink. To avoid light shades that are composed of tiny dots on a white background, printed areas will be protected with wax, and wind up as copper traces on your layout. The printed sheet is immersed in ferric chloride (copper etchant) for at least 5 minutes [40]. The advantage of this method is the waterproof ability compared with the method produced by shin et.al, they attached a copper foil and glued it on polyester fabric to realize interconnections for 16-bit microcontroller circuit [45], the Kapton plastic substrate has higher waterproof ability than the polyester fabric.

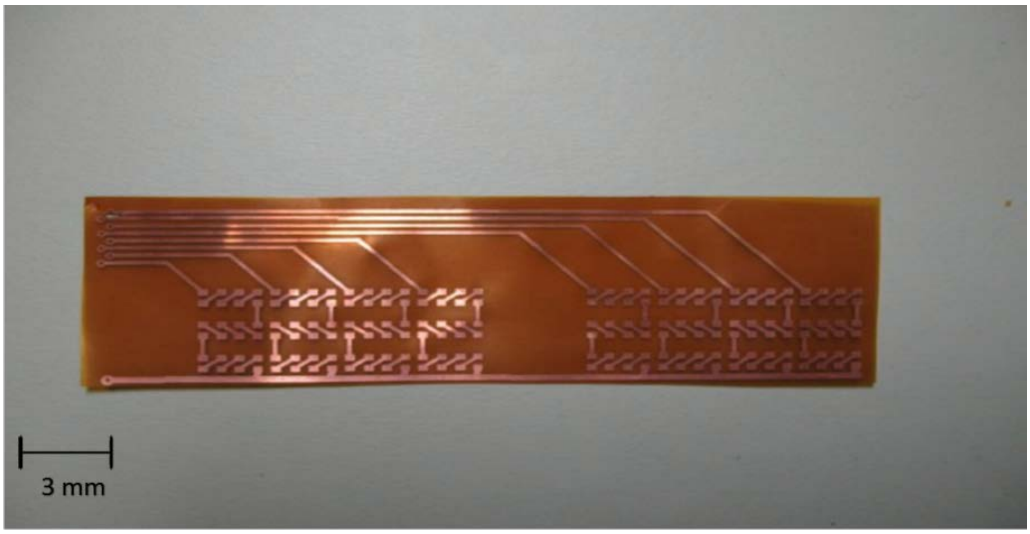


Figure 12. A 6 mm x 20 mm sample of the plastic circuit [40].

Electrical interconnections on plastic substrates have enabled an almost seamless integration of functional electronic circuits into fabrics with the use of plastic strips of 2 mm width. The different electronic packaging technologies for improving the reliability and waterproof ability of these interconnections and their circuits are discussed below.

2.5 Electronic packaging technology

Electronic packaging is the technology that provides protection for electronic components and their interconnections [46]. The prevalence of electronics places the huge requirement for better electronic packaging. Electronic packaging should be capable of resisting mechanical damage, should be waterproof and should have a good service life and reliability.

For electronic textiles to achieve good flexibility, the size of the electronic components must reduce in such a way that it is unnoticed within the fabric. The different types of electronic packages for components available include Though hole, Ball grid array (BGA) [43], Land grid array (LGA) [47] and wafer level package (WLP) [48], but the WLP are suited to achieve the flexibility of electronic textile as the small size characteristic of WLP [49].

2.5.1 Wafer level packaging (WLP)

The technology of Wafer level packaging (WLP) completes all the packaging process of an integrated circuit whilst in wafer form. The process includes electrical interconnections, mechanical protection and thermal management [50].

Figure 13 shows the schematic cross-section and process flow of a typical wafer level package [49]. This wafer level package has a total of eight layers namely; the backside coating, die, bond pad, die passivation, the first dielectric, metal, second dielectric and solder ball layers. The metal layer is used to connect die to external devices through solder ball layer. The first and second dielectric layers are used to provide protection to the metal layer.

Wafer level package technology is mainly used in devices with small size requirement for components, such as mobile phone, iPhone 5 which use more than 11 wafer level packaged components. Samsung Galaxy S3 uses 6 wafer level packaged components. In 2015, it was discovered that a WL-CSP chip on the Raspberry Pi 2 had issues with xenon flashes, inducing the photoelectric effect within the integrated circuit [48].

2.5.1.1 Related work of wafer level packaging (WLP)

Jiirgen Leib and Michael Topper reported a new wafer level packaging (WLP) technology named "SCHOTT OPTO-WLP" used for sensor application. The approach uses the SCHOTT micro-structured glass process [51]. The "SCHOTT OPTO-WLP" processes include: (1) choosing a standard silicon wafer, (2) bonding a glass cover layer to forming a cavity over the active sensor surface, (3) thinning the backside die, (4) using plasma etching to process via holes and streets, (5) distributing leads on top of passivation, (6) arranging contact solder balls and (7) using dicing to singularize packaged device. All steps are shown in Figure 14.

All process steps of "SCHOTT OPTO-WLP" are performed at wafer level and produce a true chip-size, low profile package for sensor devices. So, WLP packaging technology is suitable to use for packaging electronic components as the small size package requirements. In order to increase the flexibility of the electronic package itself to achieved electronic textile flexible, some researchers focus on a packaged electronic die in polymer [52, 53]. Section 2.4.3 gives the review of assembling the electronic chips in polymers.

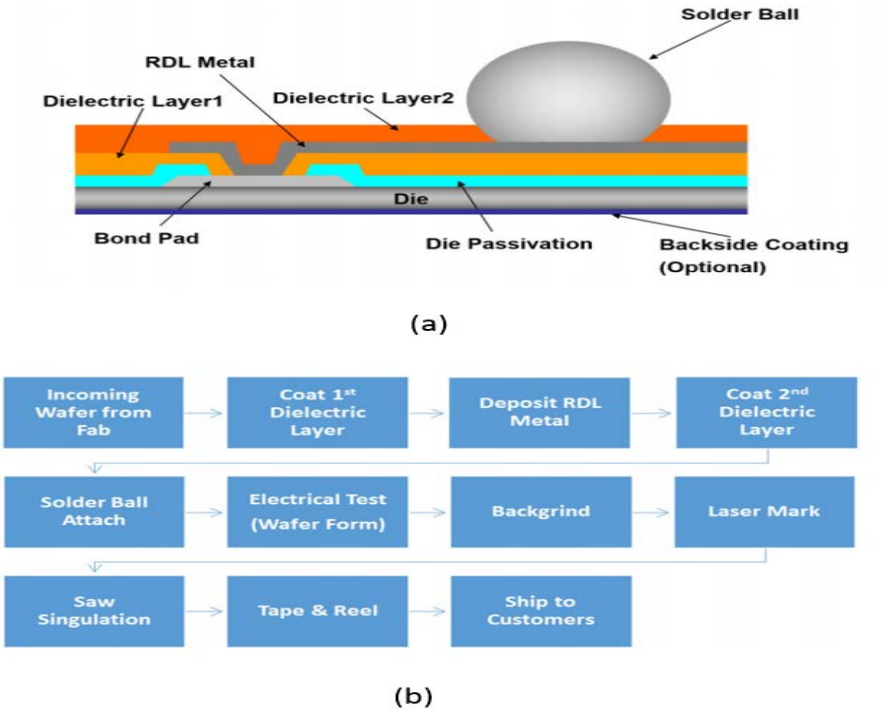


Figure 13. (a) Schematic cross-section and (b) process flow of a typical wafer level package [49].

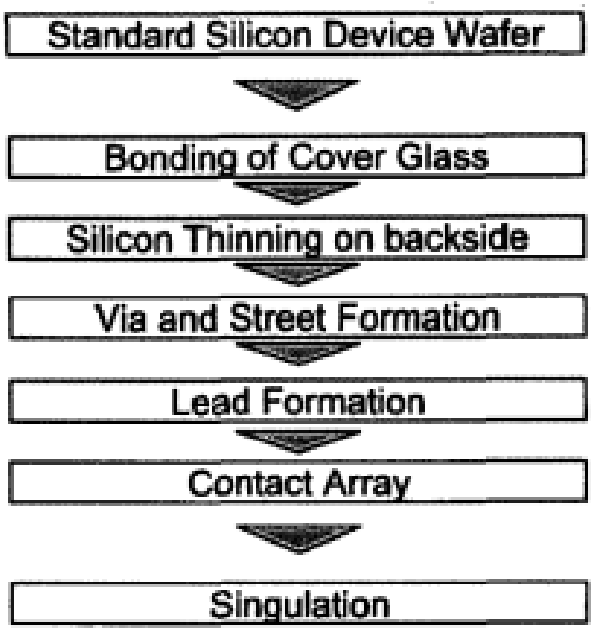


Figure 14. The process of "SCHOTT OPTO-WLP" [51].

To minimise the size of an electronic package, wafer level packaged chips are best mounted onto the substrates with flip-chip bonding technology [54]. A review of flip-chip bonding technology to bond die and the substrate is presented in following section.

2.5.2 Flip-Chip bonding

Flip chip bonding is a method of bond a die to a substrate [55-59]. Conductive bumps are usually used as interconnections to electrically connect die and substrate with the bumped die placed facing down[60]. This contrasts the common electronic packaging method where conductive wires are used as the interconnection between die and substrate, and the mounted die is placed face up.

The first flip chip technology was introduced in the 1960s by IBM and was used for individual transistor and diode for mainframe computer [61]. In 1992, Y. Tsukada the staff of IBM Japan branch introduced the under-fill used in between die and organic substrate for reliable flip chip packaging [62].

Flip chip packaging is a suitable packaging method for the smaller size or ultra-thin electronics [63]. The benefits of flip chip packaging method include: reduction in signal inductance by the shorter interconnection between die and substrate, reduction in the noise power, the performance of silicon is improved by having higher signal density than wire bonding technology and less silicon material required [63].

2.5.2.1 Related work of flip-chip bonding

Brian Holland et al [64] reported the use of three techniques to bond an ultra-thin die onto polyimide or liquid crystal polymeric (LCP) films. Figure 15 (a) shows ultra-thin die bonded on to polyimide or LCP, Figure 15 (b) describes a 50um silicon die laminated into LCP films, Figure 15 (c) shows a 10-20um ultra-thin die embedded in polyimide [64]. These three techniques divide flip chip packaging into two types which are die onto polymer and die into polymer.

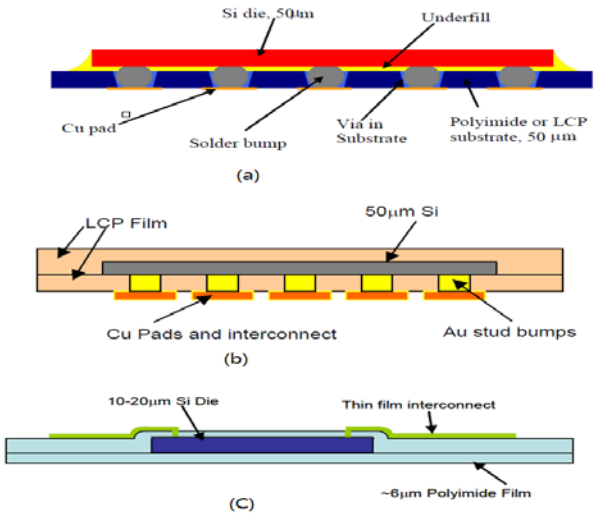


Figure 15. Three technologies to mount ultra-thin die to LCP films [64].

Zonghe Lai and Johan Liu used anisotropically conductive adhesive (ACA) to provide electrical interconnections between die and substrate for flip chip bonding die on rigid and flexible printed circuit substrates [65]. They showed four types of joint structures that may affect anisotropically conductive adhesive bonding as shown in Figure 16. Type 1 used deformed particles to connect the die contact pads and substrate contact pads. Type 2 and type 3, use equal sized of particles but of different shape, and different die contact pads. Type 4 use both deformed and undeformed particles between contact pads of die and substrate. The authors reported type 1 as the most reliable joint since it withstood various environmental tests due to the strong and uniform atomic interaction between the heavily deformed particles and the contacts from the chip and from the board" [65].

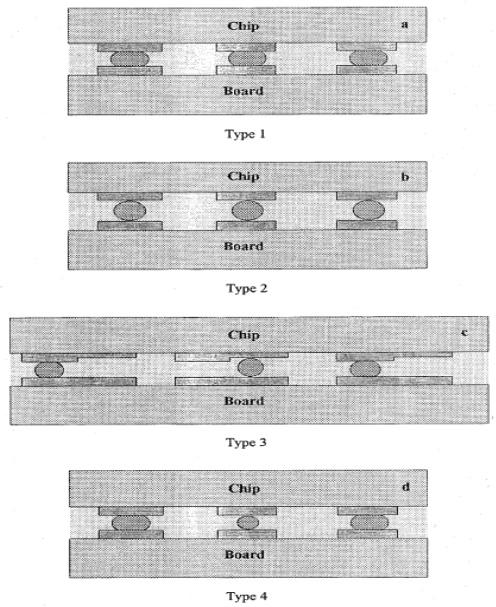


Figure 16.Four types of ACA joint structure [65].

2.5.3 Assembly and Embedding of Chips in Polymers

Recently, there has been increased research interest in embedding thin chips in a flexible polyimide substrate so as to achieve low-cost and flexible electronics [66]. Ranjan Rajoo et al. introduced a method of embedding of a 15 um thin chip in the thin flexible substrate as shown in Figure 17 [67]. The construction consists of five copper metal layers. M1 & M2 metal layers were used for fabricating the resistors and capacitors. Metal layers, M3, M4 and M5 were used for the embedding the thin chip and fabrication of inductors. The targeted total module thickness was less than 180μm [67]. An adhesive layer was used between M1 and M2 layers, and the polyimide flex substrate layer is located in between M3 and M4. The five metal layer used in this approach reduced the flexibility of the whole package.

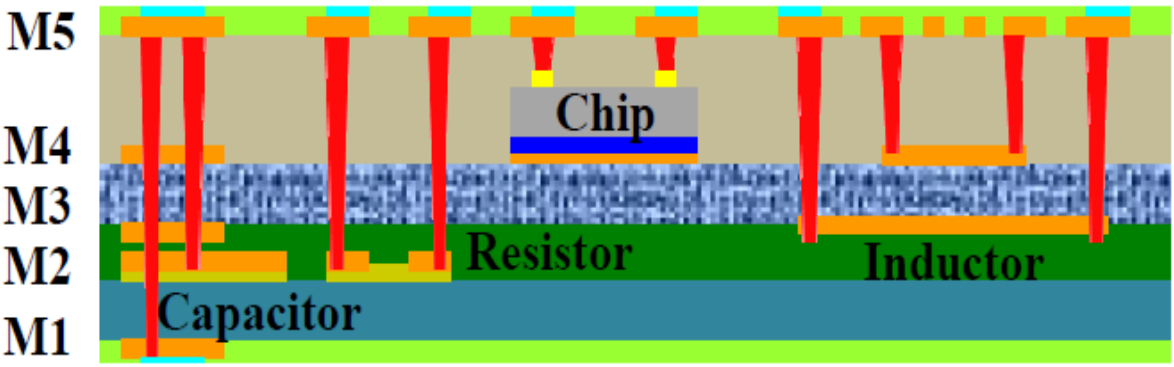


Figure 17.Schematic of embedded module [67].

Glob-topping is another approach for protecting electronic chips on plastics. Paul et.al [53] reported the use of polyurethane encapsulation to glob-top an electronic component mounted on screen printed silver circuit on thermoplastic polyurethane. This encapsulation shows high flexibility during the cyclical bending test [53]. Ji-Hye Kim et al. also reported the chip-on-flex (COF) assembly (as shown in Figure 18) using Anisotropic Conductive Films (ACFs) to improve the flexibility and compact package size [66]. The flip-chip packaging technology has been used to attach the 40 um thin silicon chips to a flexible substrate, which will minimize the total package thickness. The glob-top encapsulation method was being used in chapter six to compare with the novel electronic packaging method described in Chapter six. The flip-chip technology and anisotropic conductive adhesive were also used in the novel electronic packaging method to minimize package size and improve flexibility.

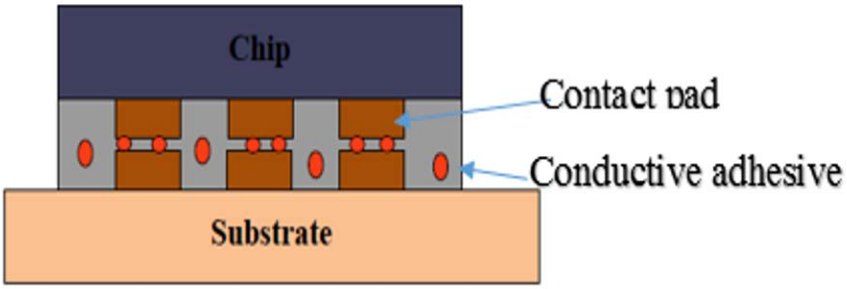


Figure 18. Schematic diagram of the package with conductive adhesive [66].

2.5.4 Conclusion

The review showed different packaging methods that have been attempted to improve the reliability of electronic circuits integrated into textiles. These methods majorly include the use of glob-topping of flip-chip packaged components and encapsulation of the embedded circuits with printable polymers such as thermoplastic polyurethane and silicone. The durability of the reported prototypes under tensile, shear,

bending and washing stresses are still not sufficient for the wearable electronic textile. Also, these approaches fail to optimise the design and material properties of the packaged textile such as thicknesses of the chip, under-fill, encapsulation and the substrate to achieve improved flexibility and reduced mechanical failures in the electronic textile system. In this thesis, the 0.025 mm thickness of die will be flip-chip packaged onto the 80 mm x 3 mm (length x width) plastic strip with total encapsulation thickness of 0.225 mm, the textile fibres will be used to surround the plastic strip to form electronic yarn to maximize the reliability and flexibility of electronic textile system.

2.6 Electronic package failure test modes

To minimize the failures of the packaged die, it is important to perform reliability tests on them before they can be used [68]. Electronic packaging for component provides many major functions of electronic dies such as electrical interconnections for electronic die and mechanical protection [69].

Various types of reliability tests that have been developed in last two decades. The most widely used testing methods are the three-point bending test [69, 70], shear test [71, 72], tensile test [73, 74] and thermal expansion test [75]. The three-point bending test, shear test, and tensile test are based on the industrial test standard document MIL-STD-883 [76].

2.6.1 Three-point bending test

Three-point bending test is widely used to detect the strength of the material. The failure strength of a material is the maximum stress at the moment of material breakage [77]. The main advantage of the three-point bending test is its ease of specimen preparation and testing [77]. A three-point bending test mode is shown in Figure 19. A specimen is placed on two supporting pins, the loading pin is located on the specimen and central to the two supporting pins. The force on the specimen is applied with the loading pin [78].

Three-point bending can be used in an electronic package to detect the mechanical strength of the die, PCB substrate and the solder/adhesive joint between the die and substrate. Edwin Bradley and Kingshuk Banerji reported that three-point bending test can be used to detect the fracture load of solder joints [79]. Four different types of solders and two different PCB boards were used in their report to compare how the different solder joints and substrates affect the strength electronic package [79].

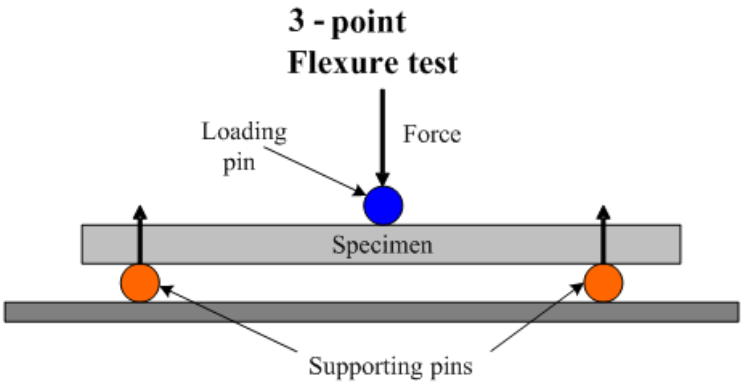


Figure 19.Three-point bending test mode [78].

2.6.2 Shear test

The shear test aims to detect the shear strength of the material. The shear strength is the maximum shear load stress at the moment of material failure. This test is usually performed on three or four specimens and the load stress is applied vertically to the specimen [80]. The shear test is mainly used to detect the shear strength of adhesives that are used to bond two or more surfaces [81, 82].

With FEM analysis, Eun-soo Hwang et al. simulated the effect of the bump dimensions to the shear load weight applying on a polymer-based flexible tactile sensor as shown in Figure 20 [14]. By increasing the bump dimensions to 4 mm (width), 4 mm (length), and 2 mm (height), the maximum 2.2-kg load can be applied to the polymer-based flexible tactile sensor. This investigation indicate that the dimension of bump affects the shear strength between electronic chip and substrate.

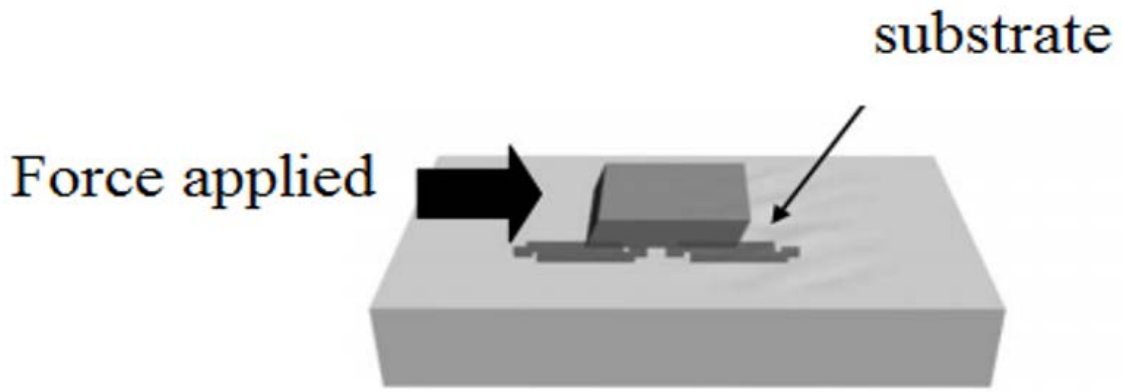


Figure 20.Shear test for polymer-based flexible tactile sensor [14].

The shear strength of the adhesive layer between the surface-mount device (SMD) and electrical interconnections made on the flexible and rigid substrate have been investigated by Damian Nowak et al. [83]. The shear strength of the adhesive was measured by applying a shear load on it with the tensile machine as shown in Figure 21. Three types of flexible substrate (Kapton, Mylar and Pyralux) and two types of rigid substrates (LTCC and alumina) were used to compare shear strength [83]. The experiment mainly investigated the effect of different substrates on the shear strength of the adhesive in the electronic package. The results showed that the adhesive shear strength was best on Kapton and LTCC for the flexible and rigid substrates respectively.

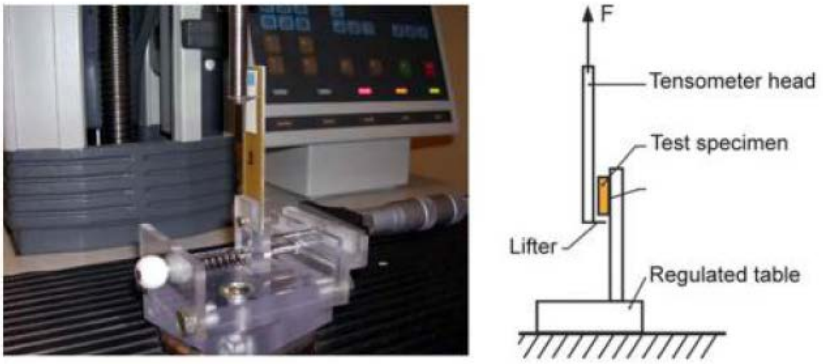


Figure 21. Tensile machine to measure the shear strength of adhesive

2.6.3 Tensile test

In this thesis, electronic die is mounted on the plastic substrate by using adhesive. The tensile test reported in this work is used to determine the tensile strength of adhesive. The tensile load test is similar to an electronic pull-off test. In the pull-off test, the load force is applied to the fixture of 90˚ to the adhesive layer. Figure 22 [84] is an example of the pull-off test to detect the tensile strength of coating adherent to a substrate. In this test, the loaded dolly is attached to the coating layer by the adhesive, the adhesion strength is detected by the force applied to dolly at the moment of the coating layer just separate from the substrate.

Umur Caglar et al. reported that use of the pull-off test to compare the adhesion of inkjet printer silver ink on PEN (Polyethylene Naphthalate), PI (Polyimide), and LCP (Liquid Crystal Polymer) substrates [85]. The silver ink showed the highest adhesion on the PEN substrate, and the adhesion between silver ink to PI and LCP shows similar adhesion.

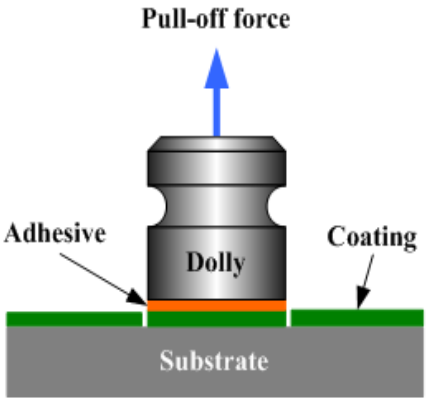


Figure 22.Pull-off test to test the tensile strength of the coating layer [84].

The finite element method (FEM) pull-off modelling method has be reported by Markus P.K. Turunen et al.[86] To determine the value of adhesion strength at printed wiring board metallisation/polymer interface. Modelling showed that the use of flexible substrate results in lower values of adhesion strength than when the rigid substrate is used because the tensile stresses are highly concentrated near the edges of the stud in the flexible construction.

2.6.4 Thermal test

A thermal test is mainly used to determine the thermal stress that causes material or product failure. Thermal stresses are produced by temperature changes. The thermal test is an Institute for Printed Circuits (IPC) standard test for thermal reliability [87-89]. It can be used to test a lot of material such as metal, glass and plastic. In this thesis, thermal load test is used to compare the thermal strength of the adhesive and plastic substrate.

Jussi Hokka et al [90] investigated the thermal cycling reliability of Sn-Ag Cu Solder interconnections in the electronic package. The authors aimed to identify the effects of temperature difference, lower dwell temperature and shorter dwell time, mean temperature, dwell time and ramp rate to the lifetime of ball grid array through repeated heat up the test sample until the test sample electrically fail [90, 91].

2.6.5 Textile properties test of e-textile

The textile properties is also one of the most important factors to cause the e-textiles failure, those properties are include drape able, washable and bendable et al [13, 92]. This section gives the review of the test methods for textile properties. The Shirley stiffness test is a common used method to test the drape ability of textile [93]. To test out the bend ability, Priyanka P.Bonde and S.D Asagekar have

reported using cloth bending hysteresis tester to test the bend ability of textile [94]. The wash ability of textile is normally tested by using washing machine, the better wash ability of textile used for e-textile will help to keep good electrical conductivity of e-textile.

2.6.6 Summary

The bending, shear, the tensile and thermal test described in the literature have used to test the reliability of electronic package, however, less of researchers use this test to determine the optimal size and materials for the electronic package.

In this thesis, simulations of a flexible flip chip electronic packaging method and experimental testing are described in order to minimise stresses in the assembly that occur due to bending, shearing and temperature changes during normal operation. The simulation and experiment have been used to determine the stresses in the mounted ultra-thin die/adhesive/plastic substrate under four conditions. The four conditions include a shear load, a tensile load, a three-point bending load and under a change in temperature. These analyses have been used to optimize the thickness of the die, the adhesive and substrate layers used in the assembly to minimise the stresses. The stress analysis has also been used to evaluate different adhesive and substrate materials.

2.7 Materials used for electronic packaging

Different types of substrates, underfill/adhesive, chip and encapsulation materials have been used to package electronics into the textile. Little has been mentioned of how to improve the reliability of the electronic package by analysing the stress distribution within the electronic package [53, 66]. Figure 23 shows a packaging method for encapsulating die in between two plastic films. This approach locates the die at the neutral axis of the assembly where the applied stress is minimum. This method will be used to package the electronic filament as shown in Figure 1. The packaged filament will achieve the wash ability compared with the other method to embedding the chip in polymers (described in section 2.4.3), those paper did not protect the components or evaluate the ability to withstand washing. In this packaging method, the interconnection between die and substrate can be solder bumps or conductive adhesives, and the empty space between die and substrate is filled by an adhesive. The adhesive is used as the under-fill to protect interconnections and release mechanical/thermal stresses applied in interconnections. In this case, the choice of material for the substrate and adhesive is the key factor to avoiding stresses.

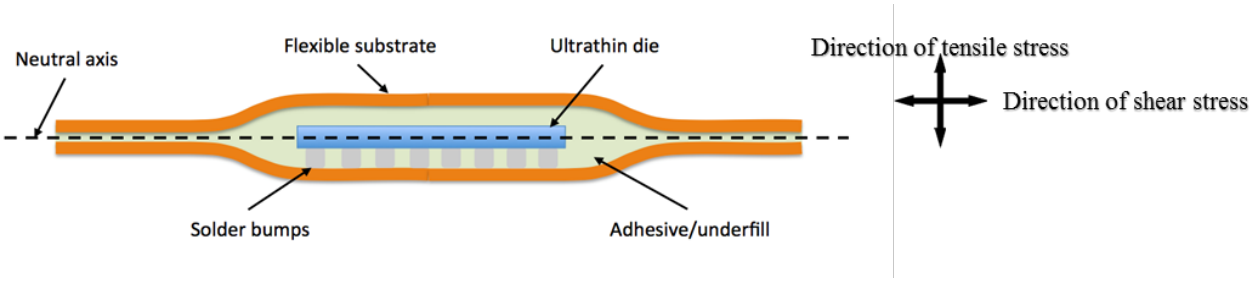


Figure 23.The schematic of flip-chip the die on the substrate.

2.7.1 Substrate

Substrates in electronic packaging provide the mechanical base for laying out electronic network consisting of the electrical interconnections and the die. The use of a mechanically reliable substrate material in electronic packaging can increase the lifetime of electronic components [95]. The normal substrates used for electronic packaging are ceramics, FR4 PCB board and polymers [96].

Since the flexibility is essential to the electronic packaging in this work, only plastic substrates will be examined. The most commonly used plastic substrates are polyimide (Kapton), polyether ether ketone (PEEK) or polyester film (Mylar) [95] and these are also investigated in this work.

The properties of these three substrates are shown in Table 1 and these were used for the FEA simulation in this thesis. The Young's modulus [97], Poisson's ratio [97, 98], coefficients of thermal expansion (CTE) [99], density and the tensile of those three plastic substrates are given in Table 1.

Table 1: The properties of three different substrates [100-102].

Product	Young's Modulus(MPa)	Poisson's Ratio	CTE (K^{-1})	Density(gcm^{-3})	Tensile Strength(MPa)
PEEK	3800	0.38	4.7E-05	1.32	98
Kapton	2500	0.34	2E-05	1.42	231
Mylar(MD)	3100	0.4	1.7E-05	1.39	138

The Young's modulus, also known as the elastic modulus, is a measure of the stiffness of a solid material [97]. It is a mechanical property of linear elastic solid materials and will be dependent on temperature, depending on the material being considered. It defines the relationship between the stress (force per unit area) and strain (proportional deformation) in a material [97]. Poisson's ratio is the

negative of the ratio of transverse strain to axial strain. It is a measure of the Poisson effect, the phenomenon in which a material tends to expand in directions perpendicular to the direction of compression [98]. CTE is a material property that is indicative of the extent to which a material expands upon heating, different substances expand by different amounts [99]. Over small temperature ranges, the thermal expansion of uniform linear objects is proportional to temperature change [99]. As shown in Table 1, Kapton has the highest tensile strength and the smallest of Young's Modulus and Poisson's ratio. Mylar has the lowest coefficients of thermal expansion.

2.7.2 Adhesive and under-fill

Adhesives are polymeric films applied between a chip and substrate to achieve mechanical and/or electrical bond when used as under-fills and conductors respectively [103]. Adhesives act as under-fills when the fill the empty spaces between a substrate and a die or chip that has been conductively bonded to it [103]. The two reasons to use under-fill in electronic packaging are to (a) reduce thermal stresses applied on interconnection i.e. those stresses caused by the difference of CTE (coefficient of thermal expansion) between silicon die and substrate and (b) increase reliability of the electrical interconnections between the chip and substrate against mechanical impacts and shock [104-110].

Epoxy-based conductive adhesives have been widely used in the electronic field given the lead-free development of electronic packaging [111], currently, more and more researchers are focused on the strength of adhesive materials researches. Xinkuo Ji et.al [111] investigated the effect of loading rate on the shear behaviour of epoxy-based isotropic conductive adhesive. The results show that fracture displacement and shear modulus increase with loading rate. The relationship among interface fracture energy, shear strength, and loading rate can characterize the interface fracture and shear strength of the conductive adhesive specimen under different loading rates. The parameters to affect the strength of under-fill for electronic package have also been reported by Fei chong Ng et. al. [112]. In their research, they proved under-fill extended filling time and incomplete filling at the upper layer of the multi-stacks Ball Grid Array (BGA) is the problem to affect the reliability of the package, this problem caused by the encapsulating lacks the energy to flow at the upper layer due to lower hydrostatic pressure. They also used a simulation to demonstrate how to add thermal energy in the under-fill to increases its flow ability.

The effect of the material properties of the under-fill on the reliability of the electronic package has been investigated in this thesis. Eight highly flexible under-fill adhesives (EP30AO, EP37-3FLF, Epo-Tek 301 2fl, Loctite 4860, MK055, NU355, Loctite 480 and Loctite 4902) have been compared by FEA simulations in chapter 4.

2.7.3 Ultra-thin chip

In today's industry, the thickness and stiffness of chip have prevented certain applications where minimum chip thickness and chip flexibility assembly are enabling requirements [113]. The ultra-thin chip is widely used in wearable and implantable electronics, displays and robotic skin etc. [114]. The flexibility of ultra-thin chip is usually used to support the product's reliability or bendability [16], some examples are the security chips in the bills or bank cards, and chips in RFID tags. Ultra-thin chips are usually fabricated industrially by the wafer level thinning of silicon wafer [115]. The steps for standard wafer thinning inculde: the use of a laminated grinding tape to protect the circuit side of the wafer from process chemistry, the coarse and fine grinding of the wafer, the chemical-mechanical polishing, the wafer mounting onto dicing foil and film frame carrier and the laminated protection tape removal [114]. However, when the silicon wafer is thinned to 150 μm thickness, the wafer has no rigidity and it is difficult to handle during the grinding process [114]. The back grinding process reported by J. Chen et.al [116, 117] is another technology to effectively thinning the silicon wafer, but it can only be used for thinning silicon wafer to 100 μm below which wafer warping and fragility becomes occurs.

R.Dekker et.al. [118] also reported the use of SOI (Silicon on Insulator) wafers to obtain thin silicon chips with a well-defined thickness. They temporarily attached the SOI wafer face down to a carrier wafer, followed by back-thinning of the silicon substrate while using the buried oxide as an etch-stop layer, trenching of the chips and chip removal from the carrier [118]. This concept presents considerable challenges in terms of fixing and transferring the thin chips during the removal process [114].

In this thesis, SOI wafer is also used to fabricate ultra-thin chip by trenching the edges of the chips down to the buried oxide and the oxide layer is removed to free the thin chips as described in Chapter 7. Compared to back-thinning process, this method does not need to remove the ultra-thin chip from the carrier which is very easy to break the chip during the chip thickness.

2.8 Conclusions

This review indicates the need to improve the reliability of electronic textiles by optimising the packaging for the electrical interconnections and the electronic chip on the fabric.

The materials for conductive interconnections and the method for integrating them into the textile Section 2.2 gives the materials and method selection to electrically connect the electronic filament (as shown Figure 1) to the power supply/ another filament. Section 2.3 reviews printed and etched interconnection methods on the plastic substrate to provide electrical connections to the die pod (as shown in Figure 1) to another die pod. These methods will be compared in Chapter six by washing test to determine the reliable conductive interconnection on plastic.

The different technologies for electronic packaging: flip chip bonding of wafer level packaged devices, chip on plastic and glob-topping methods have been discussed in section 2.4. These methods are investigated further in this thesis and compared with the novel electronic packaging method introduced in Chapter six. In this thesis, the main electronic packaging technologies used is the flip chip bonding and wafer level package because of the ultra-thin chips and packaging size requirement.

The four failure test modes presented in Section 2.5 gives the review of using this four tests to determine the reliability of the electronic package. In this thesis, the four failure test modes are used to optimise the package size and material of the electronic package described in chapters four and five. The three plastic substrates (Kapton, PEEK and Mylar) and eight highly flexible under-fill adhesives (EP30AO, EP37-3FLF, Epo-Tek 301 2fl, Loctite 4860, MK055, NU355, Loctite 480 and Loctite 4902) have been introduced in Section 2.6. To determine the optimal substrate and under-fill material, the FEA simulation was undertaken to compare substrate and adhesive materials as described in chapter four. To improve the flexibility of the electronic package by reducing the thickness of the electronic chip, the methods of fabricating ultra-thin chips were reviewed to enable the ultra-thin chip fabrication process described in Chapter seven.

Chapter 3 Theoretical stress analysis of the packaging of electronic components

3.1 Introduction

The stresses induced within an electronic textile contribute to the failure of electronic component packaging, external stresses are one of the main reason for die, adhesive and substrate to fail in electronic packaging. The external force will be applied to different textile fabrics during warp and weft is in range of 1.5 N to 46 N [119], in this thesis the corresponding external force in range of 1.5 N to 46 N is also applied to each simulation test module. This chapter introduces three material failure theories which are: (1) Maximum shear stress theory, (2) Maximum normal stress theory and (3) Maximum distortion energy theory [120]. Those theories determined different kind of stresses which caused materials to fail in the electronic package. Finite element analysis is introduced in this chapter to simulate the stresses inside the electronic packages.

3.2 Maximum shear stress theory

Maximum shear stress theory says that a failure will occur in a material when the maximum shear stress (t_{max}) in the material is higher than the shear strength (t_{yp}). The formula of maximum shear stress as shown in (1), the formula refer to Mohr's circle [121, 122].

$$t_{max} = \text{Max}\left[\frac{|s_1 - s_2|}{2}, \frac{|s_2 - s_3|}{2}, \frac{|s_1 - s_3|}{2}\right] \quad (1)$$

Where s_1, s_2 and s_3 are the three normal principal stresses in the material. The shear strength of the material can be determined from uniaxial test [120]. In the uniaxial test shown in Figure 24 the two equal forces, S_{yp} are applied on opposite sides of the material. The two stresses S_{yp} applied on the material should just make it fail. In this test s_1=S_{yp}, s_2=0 and s_3=0, using Mohr's circle t_{yp}=S_{yp}/2. The uniaxial test used in electronic packaging can help to determine the shear strength between the packaged die and substrate.

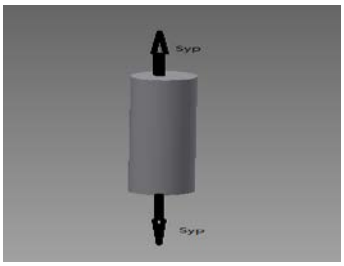


Figure 24. Uniaxial test [78].

3.3 Maximum normal stress theory

Also referred to as the maximum principal theory, the theory predicts a failure will occur in a material when the magnitude of any principal stress is bigger than the normal strength of the material [123, 124].

It is usually used for the brittle materials (brittle material is the material breaks without significant plastic deformation). Brittle materials have two kinds of strength which are compression strength and tensile strength [125, 126]. Tensile and compression stresses are usually in the opposite directions. Compared to all principal stresses, tensile stress is the maximum positive value stress and compression stress is the minimum negative stress. For example, let S1, S2 and S3 be the three principal stresses, as shown in Figure 25, in 3D mode S1, S2 and S3 are the principal stresses applied on the surface a, b and c. If given an example value of S1 = 180 MPa, S2 = 75MPa and S3 = -120 MPa, in this case, S1 is the maximum tensile stress (also called maximum principle stress), S2 is the middle principal stress and S3 is the compressive stress (also called minimum principal stress), all the stresses S1, S2 and S3 will been used in simulation software to calculate shear stress, von-Mises stress.

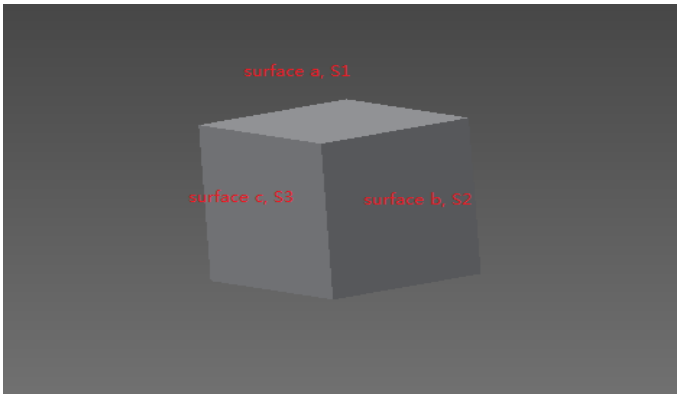


Figure 25.Three different principal stresses in different surfaces.

According to the maximum normal stress theory, to avoid the failure in a material the maximum tensile and compressive stresses should be less than the tensile and compressive strengths of the material respectively.

3.4 Maximum distortion energy theory

The Maximum distortion energy theory is also called von-Mises-Hencky theory [127, 128]. It is usually used for ductile materials (ductile material is the material which could be easily drawn into wire) like the under-fill adhesives and substrate in the electronic package. It is the most preferred failure theory in current manufacturing. This theory states that the material will fail when the distortion energy density due to the applied stresses equals the distortion energy density at the yield of the material. The distortion energy is given by [120]:

Distortion energy= $S_1{}^2+S_2{}^2+S_3{}^2-S_1S_2-S_2S_3-S_1S_3$ (3) [120]

Where S_1, S_2 and S_3 are the three principal stresses.

This theory can also be restated in terms of the von-Mises stress. Failure occurs in a material when the von-Mises [120] stress in it equals its yield strength. The von-Mises stress is considered as the safety factor in the industry and it is given by:

von-Mises stress=$\sqrt{\text{Distortion energy}}$

$=\sqrt{S_1{}^2+S_2{}^2+S_3{}^2-S_1S_2-S_2S_3-S_1S_3}$ (4) [120]

The von-Mises stresses of under-fill adhesive and substrate in the electronic package are measured by using the computer modelling software ANSYS in this thesis.

3.5 Finite Element Analysis (FEA)

Finite element analysis is a branch of solid mechanics and FEA is a numerical method for solving complex geometries problems. The analytical solution of these problems generally requires the solution to boundary value problems for partial differential equations [129-131]. The computer software tools for FEA are ANSYS, COMSOL Multiphysics and FEDEM. In this thesis, the very popular computer software (ANSYS) in the industry to do stress/strain analysis has been chosen for finite element analysis. The method yields approximate values of the unknowns at the discrete number of points over the domain [132]. To solve the problem, it subdivides a large problem into smaller, simpler parts that are called finite elements. The simple equations that model these finite elements are then assembled

into a larger system of equations that models the entire problem, FEM then uses variation methods from the calculus of variations to approximate a solution by minimizing an associated error function [133]. FEA can be used to do analysis in the following subject:

i. Structural analysis: in the analysis of bridge and car structure,
ii. Solid mechanics: in the area of a power system and gear,
iii. Dynamics: just like an earthquake,
iv. Thermal analysis: in the analysis of thermal stresses inside electronic packaging as the temperature increased,
v. Electronic analysis: electrical signal propagation,
vi. Biomaterials [134].

In electronic packaging system, FEA is usually used for analysis of mechanical stresses and thermal expansion stresses for the reliability of electronic package's design.

In finite element analysis, a geometric model is divided into a plurality of points that are interconnected and independent. The number of points is finite and each point in this geometric is analysed and the analysed results of each point are used to extrapolate over the geometric model. For example, in the mechanical stress analysis for the electronic package, shown in Figure 26, the whole electronic package is divided into a plurality of points by FEA. Stresses in the different parts of an electronic package should be different (as shown in Figure 27) because of the stresses for each part are formed by stress at each point. In this case, the electronic package stresses can be more accurately represented by using FEA technology to compare different electronic package materials, and also to optimize the package size though stress analysis.

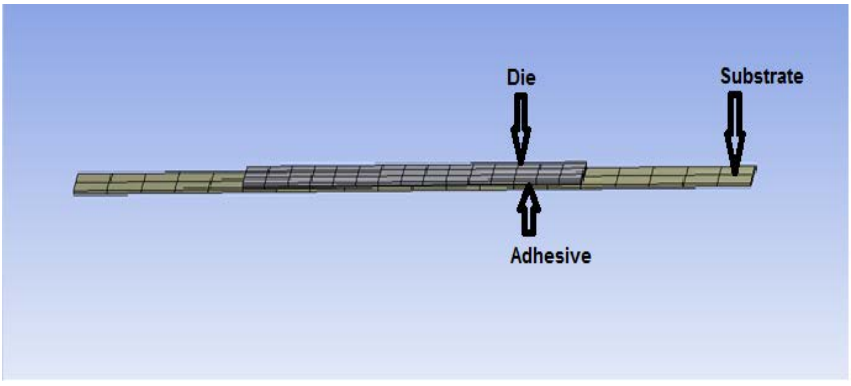


Figure 26. Finite element model of a die mounted on a flexible substrate. The dimension of substrate 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively.

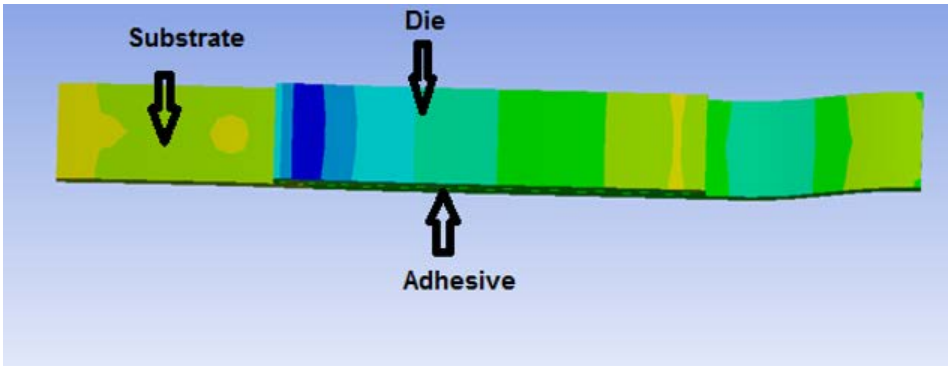


Figure 27. Stresses distribute on a cross-section of a die mounted on a flexible substrate. The dimension of substrate 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively.

When FEA is used for stress analysis, the more number of points to be divided in one geometric model, the more accurate of calculation result for the geometric model. Above a threshold number of points, the result does not change but the calculation time becomes longer.

The FEA tool can also be used in electronic packaging to determine how a parameter affects the failure of electronic packaging. The parameters in electronic packaging include: die size, die thickness, solder joint height, solder joint diameter, substrate thickness, under-fill thickness, the material of substrate and under-fill [135-138].

3.6 Simulation models and boundary conditions

The simulation is based on four test models namely: three-point bending test model, shear test model, tensile test model and thermal expansion test model. All test models are standard industrial testing models for microelectronic packaging [76, 139]. FEA has been used to determine the stresses in the mounted ultra-thin die/adhesive/plastic substrate assembly under four test models. These models have been used to optimize the thickness of the die, adhesive, substrate and also used to select the best adhesive and substrate materials used in the assembly to minimize the stresses.

3.6.1 Three-point bending test FEA simulation model

ANSYS FEA modelling method is used to simulate three-point bending test. The three-point bending tests will be simulated separately by using different sizes of the electronic package and different material combinations for the under-fill and substrate. Figure 28 shows the three-point bending model which replicates a practical testing set-up. The two stands are used in this bending test to allow space for the

packaged electronic die to bend. The two stands are fixed, and an external force is applied to location “a” at the centre of the electronic die.

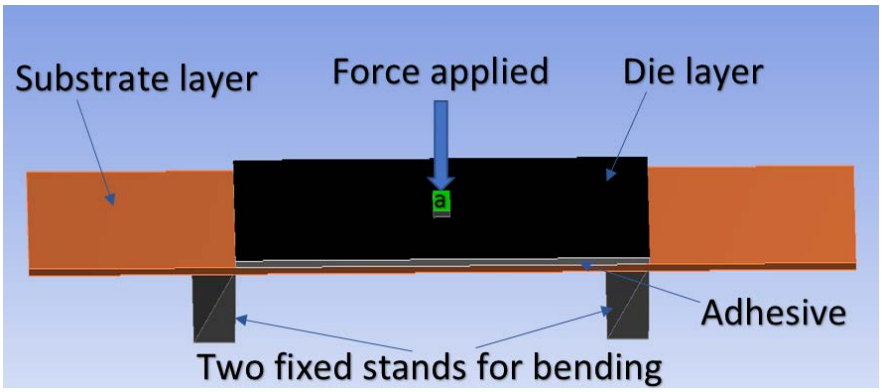


Figure 28. ANSYS simulation model for the three-point bending test. The dimension of substrate 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively.

3.6.2 Shear test FEA simulation model

The FEA simulation shear test model is guided by the industrial standard test document MIL-STD-883 [76]. In the document “section 3.1.4 test condition F- Bond shear (flip-chip) [76]” states that to do the shear test, a perpendicular force is to be applied to one edge of the die [76] as shown in Figure 29. In this diagram, a force is applied to the left edge of the die and perpendicular to the primary substrate. The top layer of the electronic package is the die, the middle layer is the adhesive and the bottom layer is the substrate. The length and width of the die, adhesive and substrate are the same as in the three-point bending test model.

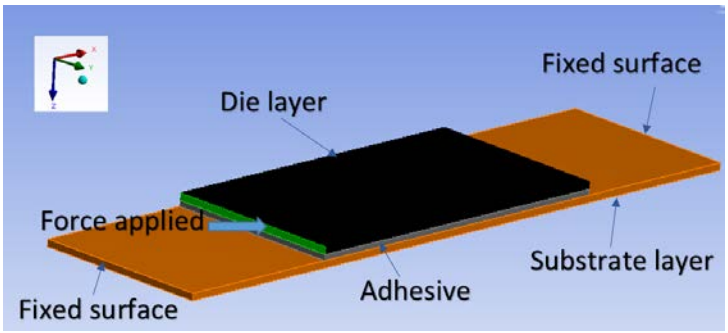


Figure 29. Diagram of shear test FEA simulation model. The dimension of substrate 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively.

The boundary conditions for the FEA simulation to identify the first principal stress, minimum principal stress, von-Mises stress and the maximum shear stress in the shear test model are:

(1) A force applied on the left edge surface of the die.

(2) The left and right edges surface of the substrate are fixed

(3) The top and bottom surface of the substrate will be fixed in the Z-axis whilst the X and Y axis are free to move as shown in Figure 29.

3.6.3 Tensile test FEA simulation model

The tensile test simulation model is also based on the industrial test standard document MIL-STD-883 [76]. In the document "section 3.1.6 test condition H- Pull-off test [76]" states that the substrate should be fixed while a pull-off stress is applied to the die as shown in Figure 30. The diagram shows a force applied to the top surface of the die. The length and width of the die, adhesive and substrate are also the same as in the previous test models.

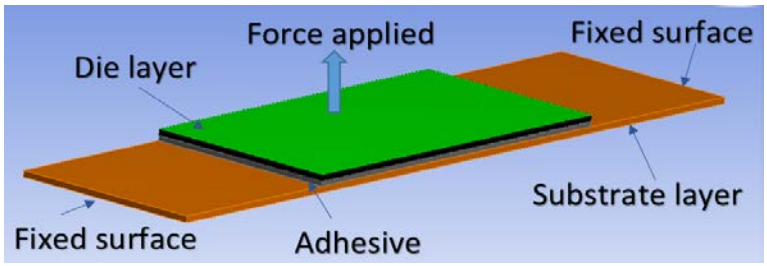


Figure 30. Diagram of tensile test model. The dimension of substrate 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively.

The boundary conditions for the FEA model to simulate stresses in tensile testing are:

(1) A force applied to the top surface of the die.

(2) The left and right end edges of the substrate film are fixed.

(3) The top surface of the substrate film will be fixed in all directions.

3.6.4 Thermal expansion test FEA simulation model

Thermal stress is produced by temperature changes (such as using high temperature in washing) in the electronic package. It is a key factor in the failure analysis of electronic packaging. Thermal expansion test model is developed to simulate the stresses inside electronic packaging caused by temperature changes (when washing the wearable electronic at high temperature) and a thermal coefficient of expansion mismatch between layers. Figure 31 shows the thermal expansion model, a long substrate layer will allow the die and adhesive to bend more easily.

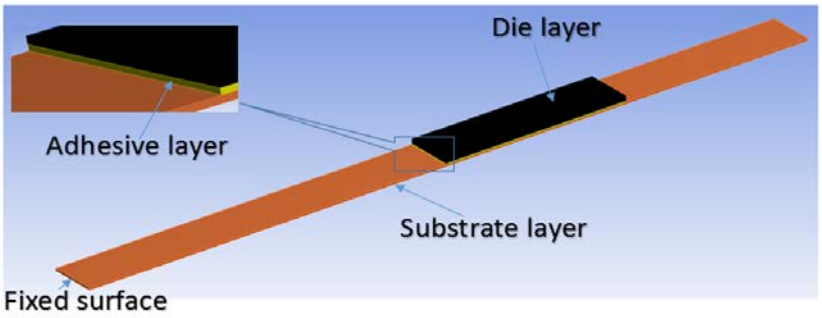


Figure 31. Diagram of thermal expansion test model. The dimension of substrate 200 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively.

The boundary conditions for the FEA model to simulate thermal caused stresses in shear test model are:

(1) The left edge of the substrate is fixed.
(2) The thermal conditions applied to the electronic packaging; in this case, heating the model from 0℃ to 100℃. (These values were chosen because wearable electronics should ideally be a washable product, hence when using a tumble dryer, the temperature may reach up to 100℃.).

3.7 Summary

This chapter discussed three failure theories which can help to determine the different types of stress that cause material failure. Of those theories, only the maximum normal stress theory is used for the brittle materials. The other three theories are for ductile materials. In this thesis, all three failure theories are used for stress analysis simulations.

The finite element analysis (FEA) was also described as the key technology for stress analysis inside an electronic package. The principal of FEA and how it is used in electronic packaging was discussed. The computer software ANSYS is used to do FEA.

The four stress test models were discussed and the boundary conditions of FEA simulations are described to analyse the effect of adhesive and substrate materials, and effect of die, adhesive and substrate thickness on the failure of electronic packaging in ANSYS.

In this thesis, the stress analysis of the electronic packaging will be performed under two types of analysis namely thermal condition and applied external stresses.

Charter 4 Finite Element Analysis simulations to determine optimal fabrication parameters

The finite element analysis (FEA) simulations in this chapter will determine the optimal thickness of die, substrate film and under-fill which will minimize the impact of bending or shear stress on components integrated within the yarn of an electronic textile. The effects of the choice of substrate and under-fill material on the stresses at the interface between the electronic packaging and the substrate have also been investigated.

The first principal stress, minimum principal stress, von-Mises stress and maximum shear stress have been analysed in four simulation models. In reference to the three failure theories, the first principal stress is the tensile stress, and the minimum principal stress is compressive stress. Shearing stress and von-Mises stresses are the most important factors for evaluating the under-fill adhesive layer failure in the electronic package.

4.1 The materials used for FEA simulations

The materials used in the die layer, adhesive layer and substrate layer for stress analysis simulations are shown in Table 2. Three under-fill adhesives (EP30AO, EP37-3FLF and Epo-Tek 301 2fl) and five highly flexible adhesives (Loctite 4860, Loctite 480, Loctite 4902, MK055 and NU355) have been simulated under four simulation models. Refer to Chapter 2.6.1 the three commonly used flexible substrate materials (Kapton, Mylar and PEEK) are also compared by four simulation models.

Table 2. The properties of materials used for FEA simulation[140-142].

Material	Layer	Young's Modulus(MPa)	CTE (K^{-1})	Density(gcm^{-3})	Tensile Strength(MPa)
Silicon	Die layer	150000	1.1E-0.6	2.33	7000
EP30AO	Under-fill adhesive layer	3447	2.5E-04	1.06	41
EP37-3FLF	Under-fill adhesive layer	344	9E-04	1.05	35

Epo-Tek 301 2fl	Under-fill adhesive layer	3664	5.6E-04	1.07	≥13.7
Loctite4860	Adhesive layer	430	1E-03	1.07	≥5
Loctite480	Adhesive layer	2000	8E-04	1.1	≥1.8
Loctite4902	Adhesive layer	400	4.25E-03	1.07	16
MK055	Adhesive layer	3200	6.4E-04	1.2	50
NU355	Adhesive layer	1700	1.5E-03	1.1	42
PEEK	Substrate Layer	3800	4.7E-05	1.32	98
Kapton	Substrate Layer	2500	2E-05	1.42	231
Mylar(MD)	Substrate Layer	3100	1.7E-05	1.39	138

4.2 Simulation results and discussion

The FEA simulation results identify the effect of the die, substrate and adhesive thickness for stresses inside the electronic package. The effect of the choice of adhesive and substrate materials on the electronic packaging will also be discussed in this section. Each of these is discussed under the four test modules. In all simulation modules the conductive tracks on the substrate will not be considered snice the simulation aim to determine the optimal material and thickness of die, adhesive and substrate.

In ANSYS FEA simulation, the element size was defined by specifying the number of elements along key dimensions of the model. The long edge (X direction in Figure 29) and short edge of the die and adhesive were divided into 10 and 5 elements respectively. The thickness of the die (Z direction) was divided into 5 elements whilst the adhesive has 3 elements through its thickness. The substrate has 20 elements along its length and 5 elements across its width and through its thickness. The ANSYS Multizone mesh setting was used to perform the mesh operation. To accommodate the different mesh sizes, two contacts were defined between the substrate and the adhesive and also between the adhesive and the die.

The maximum tensile, compressive, shear and von-Mises stresses have been determined from each model. The maximum tensile and compressive stresses can only be measured in the die layer while the maximum shear stress and von-Mises stress were obtained in both the substrate and adhesive layer because of the four failure theories. For example, Figure 32 shows the von-Mises stress distributed in the adhesive layer under a die of thickness 0.025 mm, and 10 N external shear load was applied on the left edge of die in X direction as shown in Figure 32, the 10 N force applied according to the external force applied to textile fabrics during warp and weft. The maximum simulated von-Mises stress is 2.2622 MPa on the left edge of the adhesive layer which is compared with other simulated maximum von-Mises stress in the adhesive layer under die thickness of 0.05 mm or more to determine the effects of die thickness on the von-Mises stress.

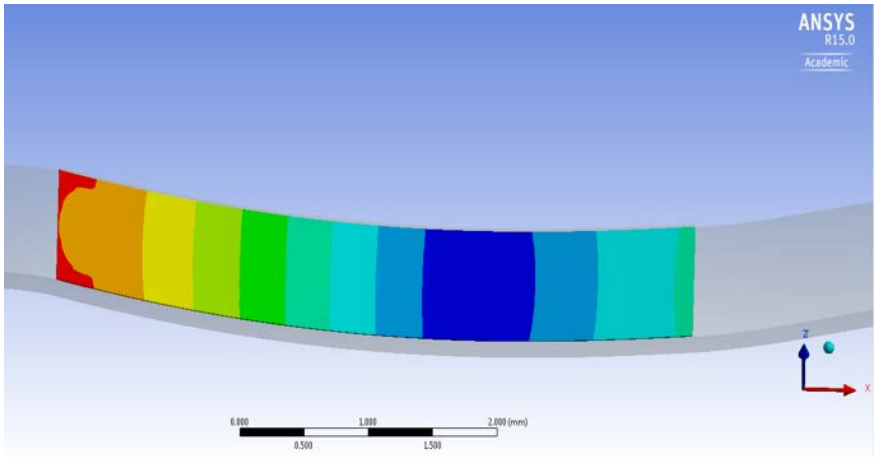


Figure 32. The von-Mises stress distributes in the adhesive layer, The dimension of substrate 200 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive is 0.05 mm.

4.2.1 The comparison of adhesive materials

The relationship between the adhesive materials and stresses inside the electronic packaging is discussed in this section. The thickness of the die, substrate and adhesive and the die and substrate materials are all fixed in every test model. The FEA boundary conditions also are fixed in every test module for simulations.

The substrate material is Kapton. The die material is silicon. In this section, the dimension of substrate used is 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively. A fixed loaded force of 10N was used for the tensile test, three points bend test

and the shear test, the 10N force applied in four tests is caused by when 1 Kg cloth loaded into the wash machine and the weight of the cloth itself will caused shear, bending and tensile load during the washing process, the 10 N force is also in range of the external force applied to textile fabrics during warp and weft (described in Section 3.1). The eight highly flexible adhesives Loctite 4860, Loctite 480, Loctite 4902, MK055 and NU355, EP30AO, EP37-3FLF and Epo-Tek 301 2fl have been compared in this section.

4.2.1.1 Comparison of adhesive materials in bending test model

The three-point bending test results are shown in Figure 33. The Maximum shear stress and von-Mises stress are respectively measured in the adhesive layer and the substrate layer. Figure 33 shows von-Mises stress and shear stress in the eight different adhesives. EP37-3FLF has the smallest von-Mises stress and shear stress in the adhesive layer. The results of von-Mises stress and shear stress in the substrate layer by using adhesive Loctite 4860, Loctite 480, Loctite4902, MK055, NU355, EP30AO, EP37-3FLF and Epo-Tek 301 2fl are also shown in Figure 33. The shear and von-Mises stress in the substrate layer do not change significantly for each under-fill material, because of the Kapton is being bent with the same force so the actual stress should be the same. The stress simulated in adhesive layer is the most important part to compare different adhesives, the lower stress value simulated represent the better the adhesive material.

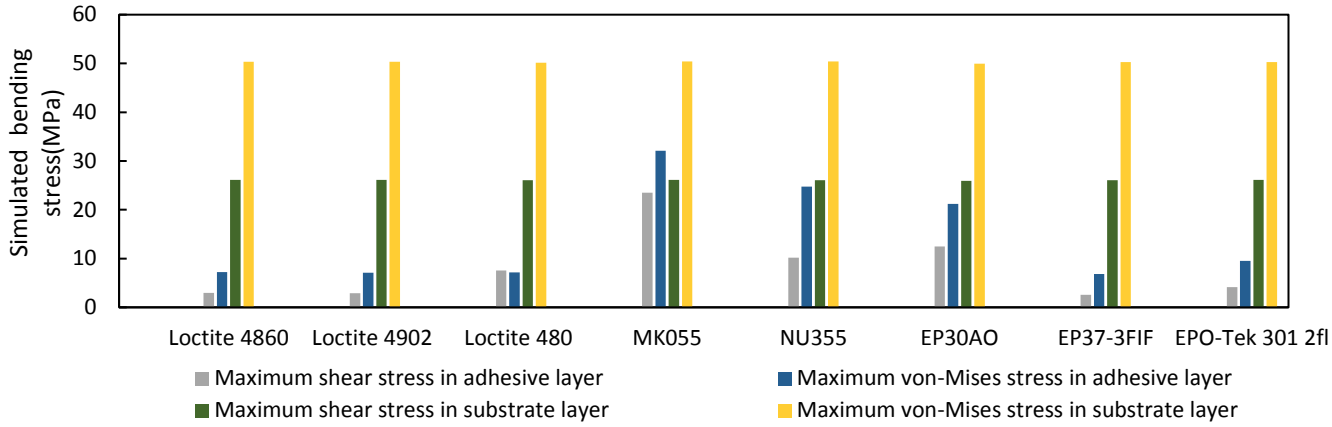


Figure 33. Shear and von-Mises stress simulations to compare adhesives with a Kapton substrate in bending test model.

Tensile stress and compressive stress have also been evaluated using the bending test model; for each of the different adhesive materials, the compressive stress and tensile stress in the die layer does not change.

4.2.1.2 Comparison of adhesive materials using the shear test model

Figure 34 shows the shear test simulation results for the maximum shear stress and von-Mises stresses in the adhesive and substrate layer. In the adhesive layer, EP37-3FLF produced the smallest von-Mises and shear stresses. The von-Mises and shear stress in the substrate layer do not change significantly for each under-fill material. Tensile stress and compressive stress have been evaluated using the shear test model, by change different adhesive materials the compressive stress and tensile stress in the die layer do not change.

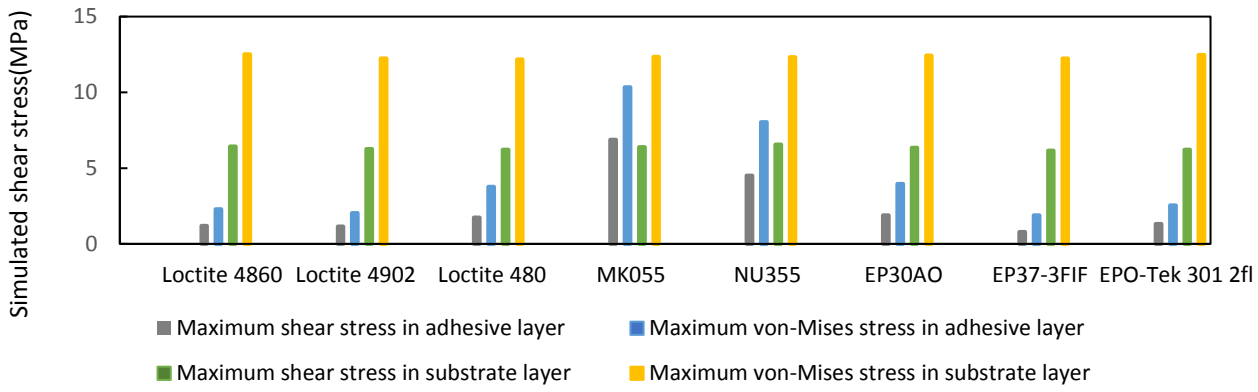


Figure 34. Shear and von-Mises stress simulations to compare adhesives with a Kapton substrate in bending test model.

4.2.1.3 Comparison of adhesive materials use the tensile test model

For the tensile test model, the adhesive material changes do not significantly affect the compressive and tensile stresses in the die layer, as shown in Figure 35 and Figure 36. The adhesive EP37-3FLF has the best performance in the tensile test model since it showed smaller von-Mises and shear stresses in comparison with the other adhesives. The EP37- 3FLF adhesive has strength of 35 MPa which is much higher than the stress simulated in the tensile test.

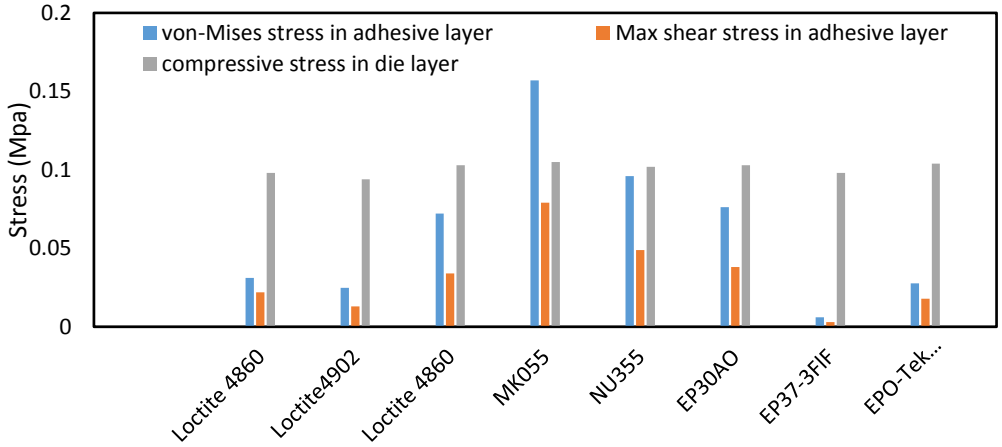


Figure 35. Compressive, von-Mises and shear stresses simulations to compare the combination of each of the adhesives and the Kapton substrate in the tensile test model.

Figure 36.Tensile stress simulations to comparing the combination of each of the adhesives and the Kapton substrate in the tensile test model.

4.2.1.4 Comparison of adhesive materials use the thermal expansion test model

For the thermal expansion test model, the left edge of the substrate is fixed and the whole structure of electronic package will be heating from 0℃ to 100℃ (the temperature increased in step of 5℃/ Sec), this temperature range is based on the typical tumble dryer temperature. The compressive and tensile stresses (as shown in Figure 37) in die layer does not change significantly compared to the strength of die for each under-fill material, because of in this thermal expansion model, the compressive and tensile stresses are simulated in die layer and only silicon die used in this test model. Figure 38 shows that EP37-3FLF produced the smallest von-Mises and shear stresses in the adhesive and substrate layer of all the adhesive materials.

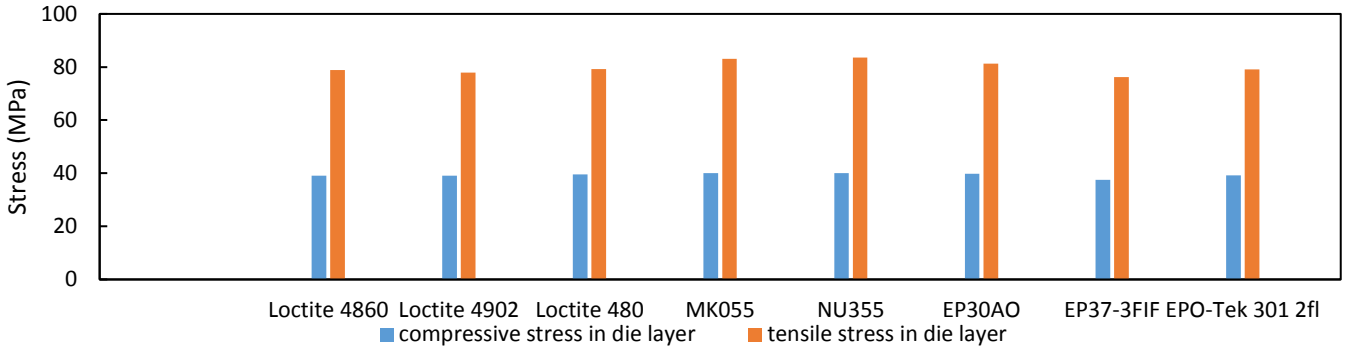


Figure 37.Compressive and tensile stress simulations to compare the adhesive layer and Kapton layer combination in thermal expansion test model in the temperature range of 0℃ to 100℃.

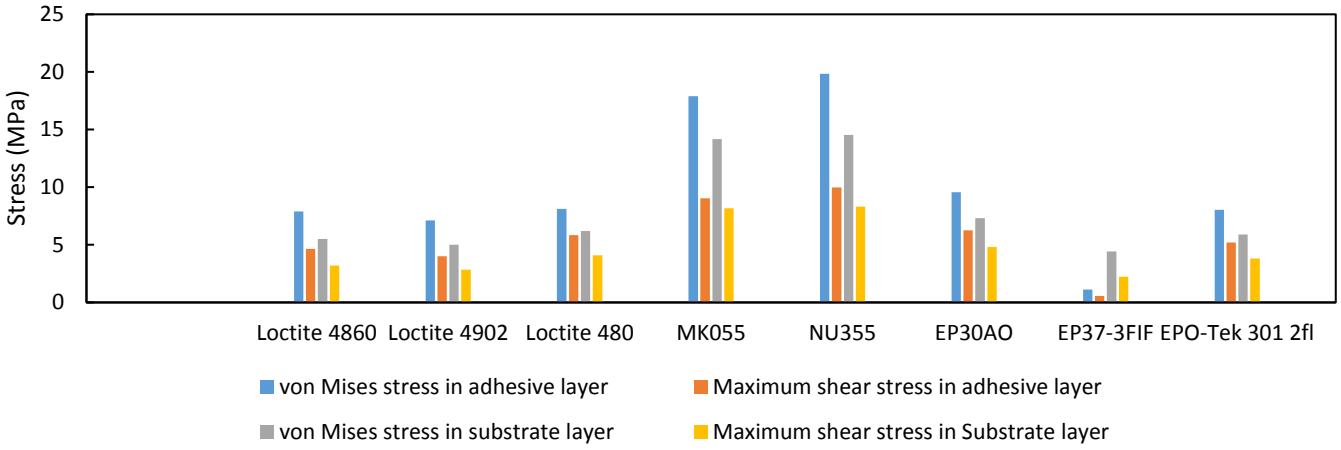


Figure 38. Shear and von-Mises stress simulations to compare the adhesive layer and Kapton layer combination in thermal expansion test model in the temperature range of 0°C to 100°C.

4.2.1.5 Summary of adhesive material simulation results

The three points test, shear test and tensile test models showed that the under-fill adhesive EF37-3FLF yielded the best performance because of the EF37-3FLF gave the lowest stress compared to other adhesives in those three tests. In the thermal expansion test, EF37-3FLF also produced the smallest von-Mises and shear stress in the adhesive layer. This means that the four test modules indicate that of the eight different adhesives, EF37-3FLF under-fill has the best stress performance with the 0.125 mm Kapton substrate and 0.025 mm silicon die.

4.2.2 The comparison of substrate materials

The simulations in this section aim to determine the optimal substrate material for the electronic packaging. Three different substrates have been simulated using four test models. In all test models, the dimension of substrate used is 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively. The die material is silicon and the adhesive is EF37-3FLF as identified in the previous sections. A 10 N force load is used for the bending, shear and tensile test models. FEA boundary conditions in all models also are the same as before. The most commonly used plastic substrates materials: PEEK, Kapton and Mylar [143] have compared.

4.2.2.1 Substrate material comparison using the bending test model

Figure 39 shows that the compressive and tensile stresses in the die layer using PEEK substrate are 529.42 MPa and 450.33 MPa. By using Mylar substrate, the respective stresses are 530.23 MPa and 449.81 MPa, and for Kapton substrate 530.41MPa and 450.63 MPa. The von-Mises and shear stresses in the substrate layer by using PEEK substrate are 61.91MPa and 31.32 MPa. For Mylar substrate, 60.09 MPa and 30.20 MPa, and for Kapton substrate are 59.99 MPa and 29.77 MPa as shown in Table 3. There is no significant difference in the von-Mises and shear stresses in the adhesive layer for all the three substrates.

Table 3.Stresses simulated in bending test model for three different substrate materials.

Stress type	PEEK	Mylar	Kapton
tensile stress in die layer (MPa)	529.42	530.23	530.41
compressive stress in die layer (MPa)	450.33	449.81	450.63
von-Mises stress in substrate layer (MPa)	61.91	60.09	59.99
Max shear stress in substrate layer (MPa)	31.32	30.2	29.77

The compressive and tensile stresses obtained with PEEK, Mylar and Kapton substrates have similar values, so the substrate material changes have a minor effect (0.2% maximum) on the compressive and tensile stress in the die layer. The yield strength of PEEK is 98 MPa, for Kapton is 231MPa and for Mylar is 138 MPa [100-102]. The measured von-Mises stress in the substrate layer by using PEEK is 61.91MPa which is close to the yield strength of 98 MPa. The smallest von-Mises stress in the substrate is 59.99MPa obtained using Kapton, which is much lower than the yield strength of Kapton (231MPa). Therefore, Kapton is the more stable substrate in the three points bend test model. Figure 40 shows the von-Mises and maximum shear stress in adhesive layer in bending test, the results in Figure 40 show that the stresses in the adhesive layer do not change significantly because their Young's modulus (only about 10% of substrate Young's modulus) are much smaller than Young's modulus of the substrate materials.

4.2.2.2 Compare substrate materials in the shear test model

Figure 41 shows the tensile and compressive stresses in the die layer using the three substrate materials tested, and as the results shown the substrate material changes also have a minor effect (0.2% maximum) on the compressive and tensile stress in the die layer.

The simulation results of von-Mises stress and shear stresses in the substrate layer are shown in Figure 42, the Kapton substrate produced the smallest von-Mises and shear stresses compared with PEEK and Mylar substrate.

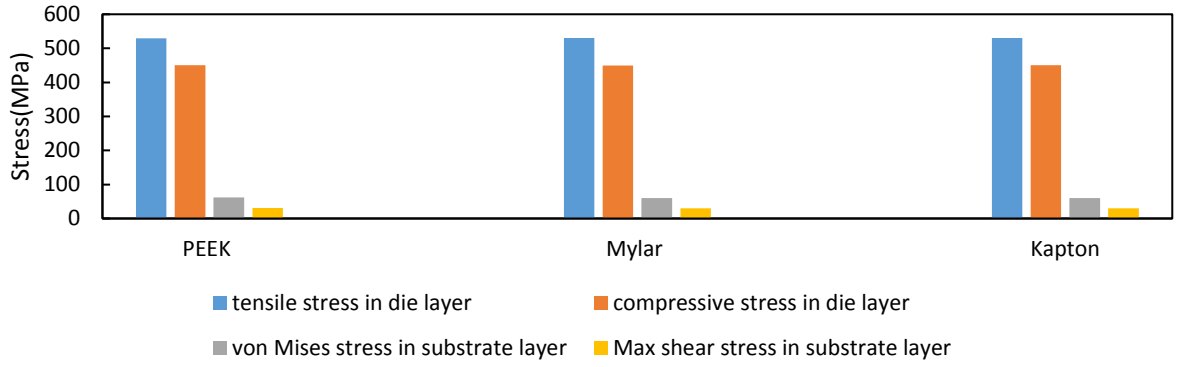


Figure 39. Tensile stress, compressive stress, von-Mises and shear stress in the substrate layer for the three-point bending test.

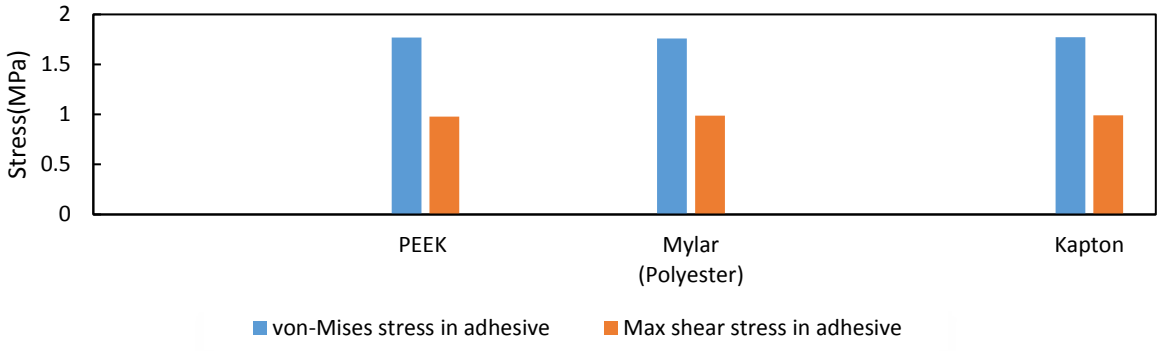


Figure 40. von-Mises and shear stress in the adhesive layer for the three-point bending test.

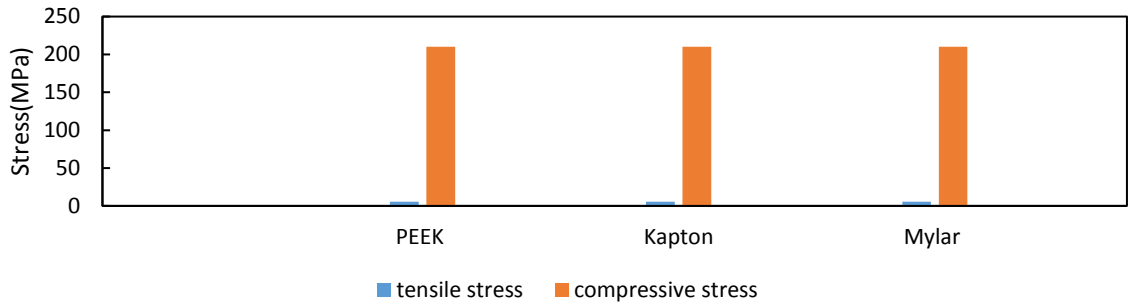


Figure 41. Tensile and compressive stress in the substrate layer during the shear test for each substrate material.

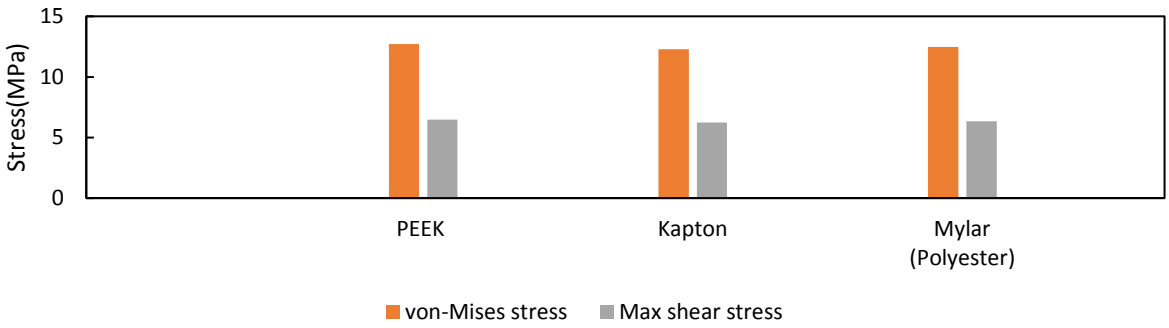


Figure 42.von-Mises and shear stress in the substrate layer during the shear test simulation for each substrate material.

4.2.2.3 Comparison of substrate materials in the tensile test model

The simulation results using the tensile test model and varying the substrate material are shown in Figure 43. The results indicate that the von-Mises and shear stresses simulated in the substrate layer for each substrate material are negligible (<0.001 MPa). Also, the compressive stress simulated in the die layer is also approaching 0.8MPa. The tensile stress simulated in the die layer by using three different kinds of substrate all are near to 1MPa as shown in Figure 43. These results indicate that the use of different substrate materials only caused minor effect (0.01% maximum) to tensile and compressive stresses in the tensile test model. Because of the external stress was applied to the electronic die for tensile test, so the adhesive layer is the key factor to caused electronic package failure.

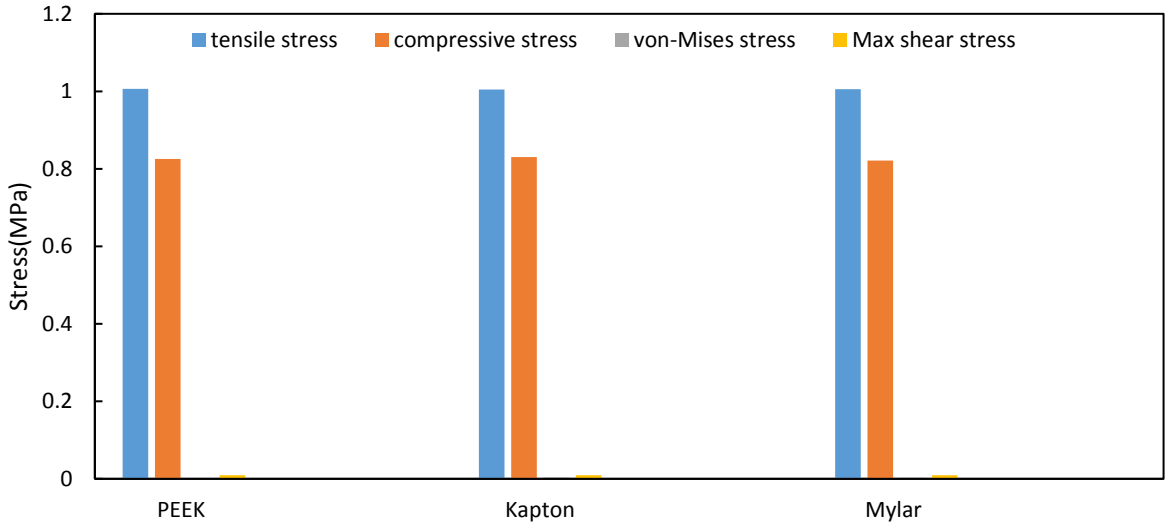


Figure 43.Tensile, von-Mises, Max shear and compressive stresses simulated using the tensile test model using different substrate materials.

4.2.2.4 Comparison of substrate materials in thermal expansion test model

Figure 44, the von-Mises and shear stresses in the adhesive layer by using PEEK are 1.62 MPa and 0.89 MPa. For Mylar, they are 1.10 MPa and 0.57 MPa, and for Kapton, they are 1.12 MPa and 0.57 MPa. The tensile and compressive stresses in the die layer by using PEEK are 156.23 MPa and 114.35 MPa. For Mylar, they are 70.89 MPa and 34.64 MPa and for Kapton, they are 51.16 MPa and 37.55 Mpa. The von-Mises and shear stresses in the substrate layer by using PEEK are 17.57 MPa and 8.88 MPa. For Mylar, they are 4.86 MPa and 2.46 MPa, and for Kapton, they are 4.43 MPa and 2.24 MPa as shown in Table 4.

Table 4.stresses simulation result for three different substrate used in electronic package for thermal expansion test.

Stress type	PEEK	Mylar	Kapton
von-Mises stress in adhesive	1.62 MPa	1.14 MPa	1.12 MPa
Max shear stress in adhesive	0.89 MPa	0.57 MPa	0.57 MPa
von-Mises stress in substrate	17.57 MPa	4.86 MPa	4.43 MPa
Max shear stress in substrate	8.88 MPa	2.46 MPa	2.24 MPa
tensile stress in die layer	156.23	70.887	71.158
compressive stress in die layer	114.35	36.635	37.548

Figure 45 shows that Kapton produces the smallest von-Mises stress and shear stress compared with the PEEK and Mylar substrate, and Kapton substrate also produced the smallest tensile stress and compressive stress in the die layer. Overall, Kapton substrate has the best performance in thermal expansion test model.

Kapton also has the lowest coefficient of thermal expansion (CTE). Therefore, the smaller CTE produced smaller stress in the electronic package for thermal expansion test.

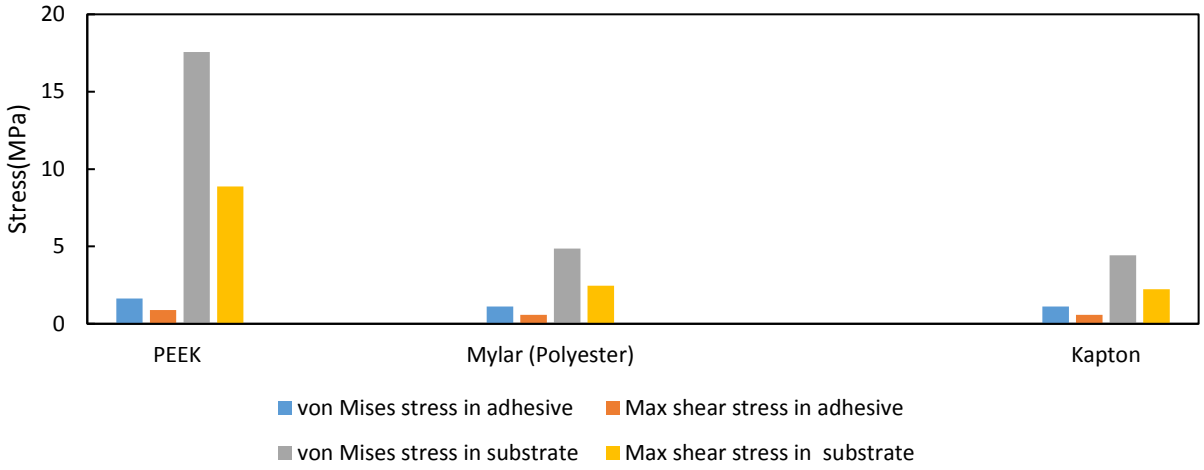


Figure 44. The von-Mises and shear stresses simulated at the adhesive and substrate layer via thermal expansion test.

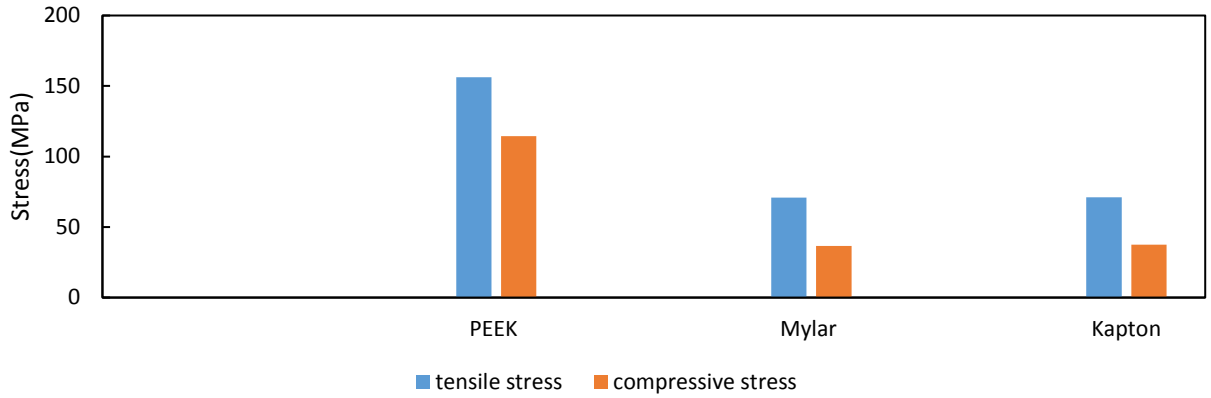


Figure 45. The tensile and compressive stresses simulated via the thermal expansion test.

4.2.2.5 Summary of substrate material simulation results

For the three points bending, shear, tensile and thermal expansion test models, Kapton substrate showed the best stress performance. Therefore Kapton offers the best reliability for electronic packaging.

4.2.3 Effect of adhesive thickness

In this section, the relationship between stresses inside the electronic package and the adhesive layer thickness is studied to determine the optimal adhesive layer thickness. The EP37-3FLF adhesive and Kapton substrate are selected in this section as they produce the best stresses performance in previous simulations. The die material is silicon, the dimension of substrate used is 100 mm (length) x 20 mm (width) x 0.125 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of die is fixed at 0.025 mm. the adhesive thickness has been simulated in the range of 0.01 to 0.07 mm for the four test models, this range is chosen to minimize the electronic

package size whilst providing sufficient strength. A 10N force was used for the shear, tensile and bending test models. A temperature range of 0℃-100℃ used for the thermal expansion test.

4.2.3.1 Effect of adhesive thickness for the bending test model

The von-Mises stress and shear stresses in the adhesive layer are discussed in the bending test. Compressive and tensile stresses in the die layer vary with the same trend as von-Mises stress and shear stress in the adhesive layer. Figure 46 shows that, if the adhesive thickness is less than 0.048 mm, when the adhesive thickness increases, the shear and von-Mises stresses decrease. When the thickness of the adhesive is more than 0.048 mm, the opposite effect is observed. Between0.048 and 0.05 mm, the minimum stress performance occurs. Therefore, the optimal EP37-3FLF adhesive thickness for the electronic package is determined to be between 0.048 and 0.05 mm.

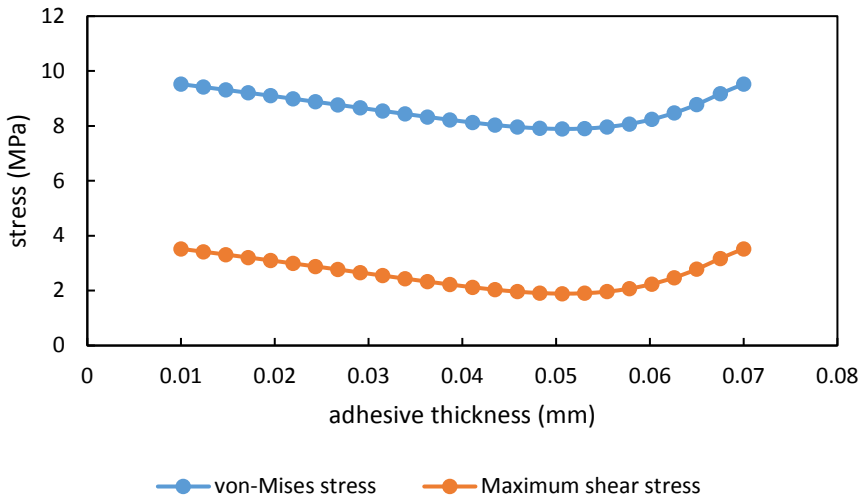


Figure 46. Changes in Shear stress and von-Mises stress during the bending test.

4.2.3.2 Effect of adhesive thickness in the shear test model

The von-Mises and shear stresses in the shear test model are discussed. As shown in Figure 47 when the adhesive thickness is less than 0.048mm the von-Mises and shear stresses decrease as adhesive thickness increased. Above 0.048 mm, the shear and von-Mises stresses increase as adhesive thickness increased.

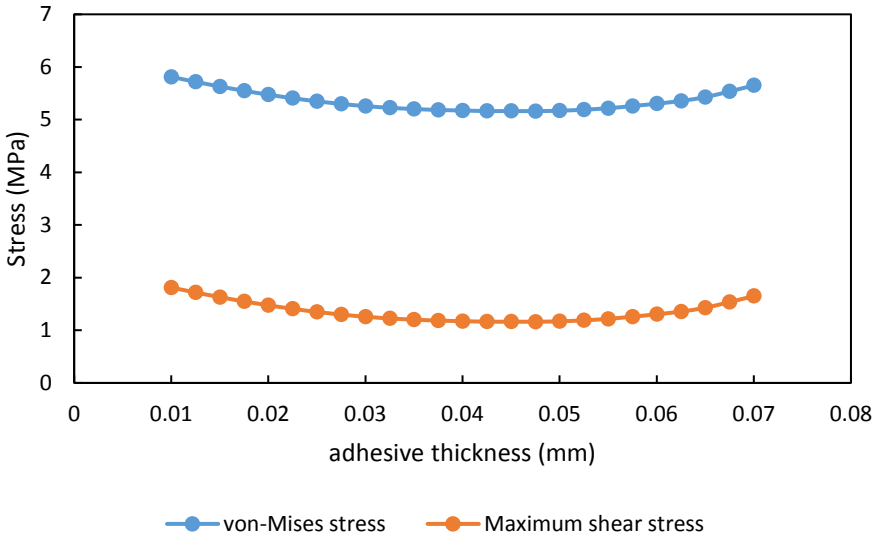


Figure 47.Shear and von-Mises stress changing trends in the shear test.

4.2.3.3 Effect of adhesive thickness in the tensile test model

The von-Mises and shear stresses have been simulated in the tensile test model. As shown in Figure 48 when the adhesive thickness is less than 0.05 mm the von-Mises and shear stresses decrease as adhesive thickness increased. Above 0.05 mm, the shear and von-Mises stresses increase as adhesive thickness increased. The 0.05 mm adhesive thickness shows the best stresses performance in the tensile test model.

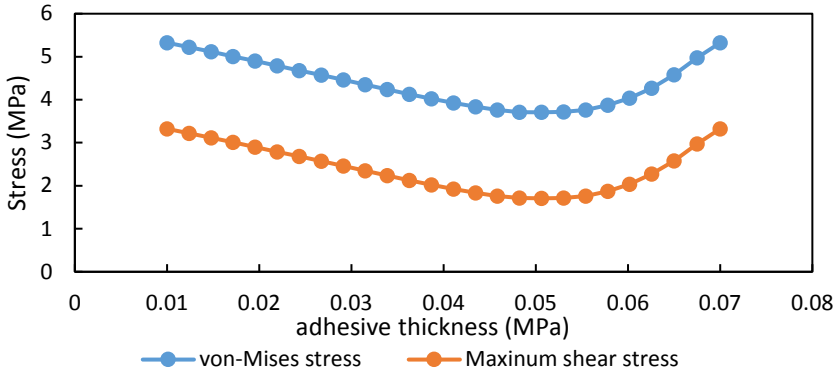


Figure 48. Shear and von-Mises stress variations when using the tensile test simulation.

4.2.3.4 Effect of adhesive thickness in thermal expansion test model

The von-Mises and shear stresses in the adhesive layer do not change significantly as the adhesive thickness increases as shown in Figure 49. In the substrate layer, these stresses show the minor change in value across the adhesive thicknesses. The tensile and compressive stresses in the die layer are

minimally affected by the change of adhesive thickness. The temperature range used in this test is 0℃-100℃. The results show that changes in the adhesive thickness do not significantly affect the stresses inside electronic package when considering the thermal expansion model, because only CTE (coefficient of thermal expansion) of the material affect the stresses change in the thermal test.

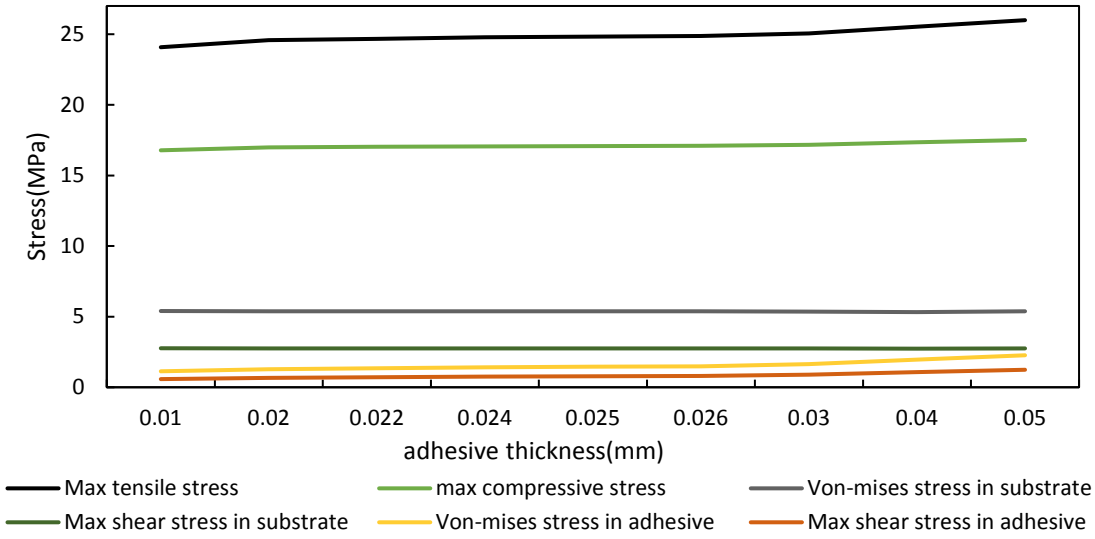


Figure 49. Stresses in the adhesive layer using the thermal expansion test.

4.2.3.5 Summary of adhesive thickness simulation results

In this section, the 0.125 mm Kapton substrate, 0.025 mm silicon die and the EF37-3FLF under-fill adhesive are used to determine the optimal adhesive thickness using four simulation models. For the bending test model, the optimal adhesive layer thickness is between 0.048 and 0.05 mm, for the shear and tensile test the optimal adhesive layer thickness is 0.05 mm. In thermal expansion test mode shows that adhesive thickness does not significantly affect the stresses in the electronic package; therefore the optimal thickness for EF37-3FLF is around 0.05 mm. Different adhesives have a different optimal thickness in the electronic package because of their different Young's modulus.

4.2.4 Effect of substrate thickness

This section presents the investigation into the effect of substrate thickness on the stress induced in the adhesive. The die material is silicon. In this section, the dimension of substrate used is 100 mm (length) x 20 mm (width), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively. EF37-3FLF adhesive and Kapton substrate were used for all test models. The FEA boundary conditions for simulation are same

as the previous test. The external force applied to shear test, bending and tensile tests are 10 N. The temperature range of 0-100 ℃ is used for thermal expansion test. The adhesive thickness in the range of 0.01 to 0.07 mm have been examined in four test models, the thickness range is chosen to minimize as far as possible the electronic package size whilst providing sufficient strength.

4.2.4.1 Effect of substrate thickness in the bending test model

Figure 50 shows when the Kapton substrate has a thickness between 0.01 and 0.048mm, as the substrate thickness increases, the stresses decrease. If the substrate thickness is more than 0.052mm, as the substrate thickness increases, the stresses increase. A Kapton thickness in the range of 0.048 to 0.052mm shows the lowest stresses simulated in the bending test. When a fixed external stress is applied, the smaller the value of stress detected in the package the more reliable the package. So the range 0.048 to 0.052mm thickness of the Kapton substrate is identified as the optimal thickness of the substrate layer under the bending test.

4.2.4.2 Effect of substrate thickness in the shear test model

The maximum shear and von-Mises stresses have been simulated using a 10 N shear load external force. The simulation results are shown in Figure 51. When the Kapton substrate is between 0.01 and 0.05mm thick, as the substrate thickness increases, the stresses decrease. When the substrate thickness is above 0.052mm, as the substrate thickness increases, the stresses increase. A Kapton thickness between 0.05 to 0.052mm shows the lowest stress in the adhesive layer.

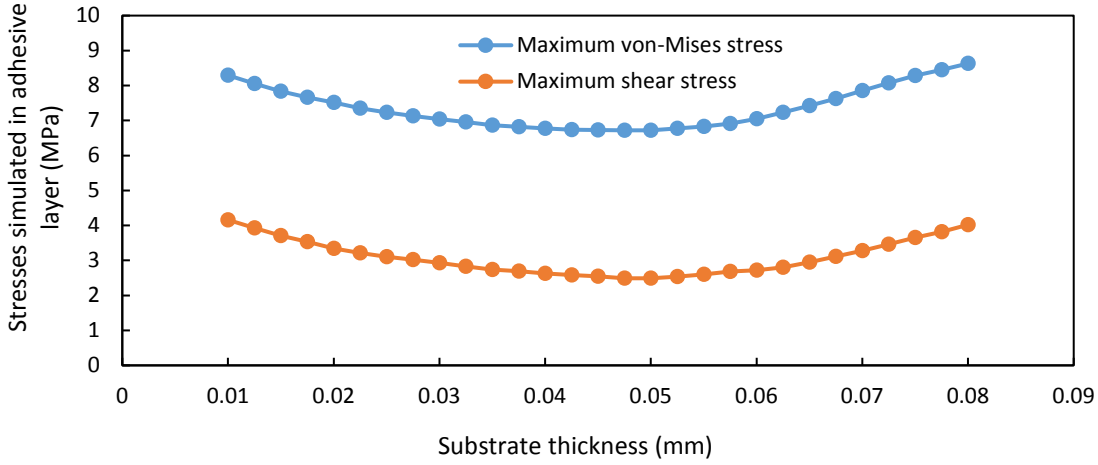


Figure 50. Bending test modelling to simulate maximum shear and von-Mises stress versus substrate thickness.

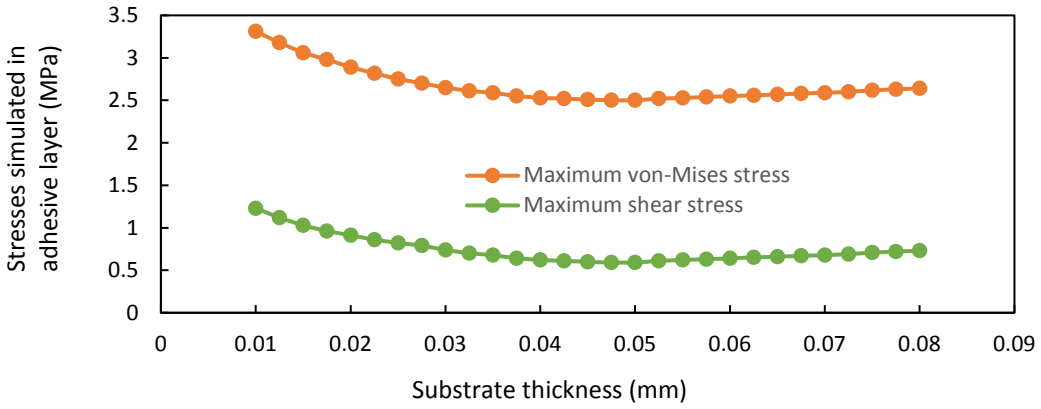


Figure 51. Shear test modelling results, to simulating maximum shear stress and von-Mises stress VS substrate thickness.

4.2.4.3 Effect of substrate thickness using the tensile test model

Figure 52 shows the tensile test results, when the Kapton substrate is between 0.01 and 0.05mm thick, as the substrate thickness increases, the stresses decrease. When the substrate thickness is above 0.052mm, as the substrate thickness increases, the stresses increase. A Kapton thickness of 0.05 to 0.052 mm shows the lowest stress in the adhesive layer.

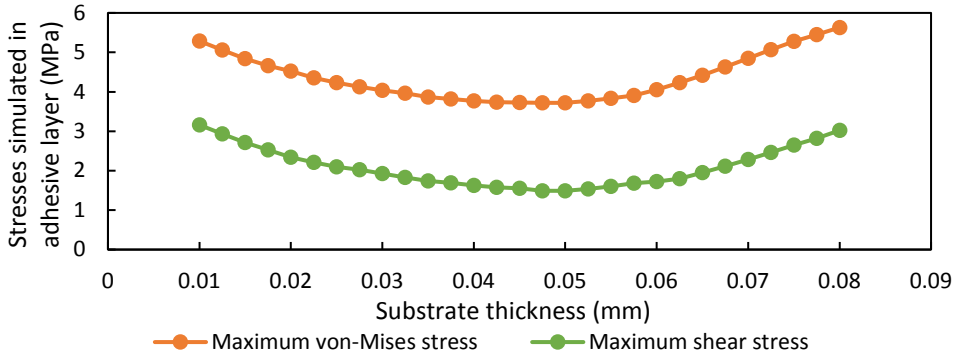
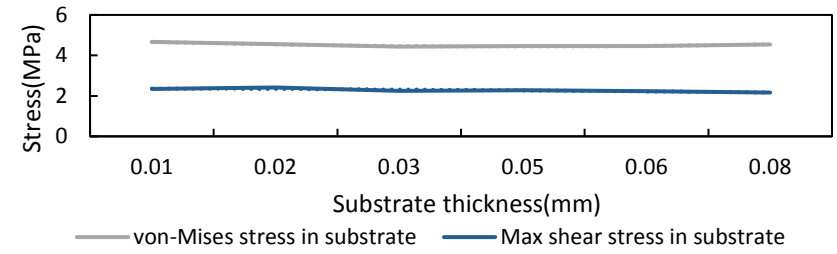


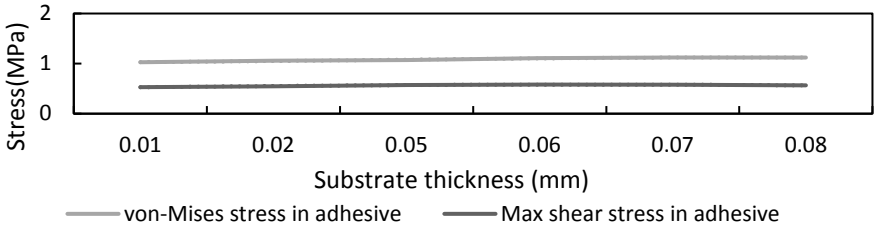
Figure 52. Changes in Stress due to change in substrate thickness for the tensile test; Die and EF37-3FLF adhesive thickness are 0.025mm and 0.05mm, substrate material is Kapton.

4.2.4.4 Effect of substrate thickness in the thermal expansion test model

The von-Mises and maximum shear stresses in both substrate and adhesive layer have been simulated using the thermal expansion test to determine the optimal substrate thickness. Figure 53(a) shows the von-Mises and shear stresses in the substrate layer, these stresses do not change significantly(less than 5%) when using different substrate thicknesses. The von-Mises and shear stresses in the adhesive layer were also simulated, as shown in Figure 53(b). The results show that between0.01 mm and 0.08 mm for the substrate thickness the von-Mises and shear stresses do not change significantly(less than 5%).



(a)



(b)

Figure 53. Stress simulation to determine the optimal substrate layer thickness, shear stress and von-Mises stress simulated in the (a) substrate layer and (b) adhesive layer.

4.2.4.5 Summary

In these sections, the Kapton substrate, 0.025 mm silicon die and 0.05 mm EF37-3FLF under-fill adhesive were used to determine the optimal substrate thickness using four simulation models. In the bending test model, the substrate thickness between 0.048 mm- 0.052 mm was identified as optimal thickness. For the shear and tensile test, the substrate thickness in the range of 0.05 mm- 0.052 mm was identified as optimal thickness. The simulation results of thermal expansion test model show that the thickness of substrate does not significantly affect the stresses inside the electronic package. So, it is clear from these simulations that the optimal substrate thickness is between 0.05mm to 0.052 mm. The thicker substrate can withstand bigger force, however, in the electronic package structure when a very thicker substrate used, the neutral axis will move to substrate layer and thinner substrate move neutral axis to die layer which will cause adhesive layer failed easily (adhesive material has much smaller strength than substrate and die material).

4.2.5 Effect of die thickness on the stresses within the electronic package

To determine the relationship between the die thickness and stresses inside the electronic package, the substrate and adhesive thickness, and the materials used for die, adhesive and substrate all are fixed in every test models. The FEA boundary conditions also are fixed in every simulation using the same previous constraints.

The silicon die, Kapton substrate and EF37-3FLF adhesive are used for the simulations. In this section, the dimension of substrate used is 100 mm (length) x 20 mm (width) x 0.05 mm (thickness), and die has same dimension with under-fill which is 50 mm (length) x 20 mm (width), the thickness of adhesive is 0.05 mm. A 10N loaded force is used for the shear, bending and tensile simulations. Die thicknesses of 0.025mm, 0.050mm, 0.075mm and 0.125mm have been simulated and compared as those thickness of die are commercial available which will more easy to buy and do experimental tests to verify the simulation results. The objective of this research is to mount ultra-thin die onto circuits on a plastic substrate, the thick die used in the plastic strip (as shown in Figure 1) affect the flexibility of strip, so in this section, only the die thickness below 0.125mm have been simulated.

4.2.5.1 Effect of die thickness on the bend test model

The bending test results in Figure 54 (plotted line is for eye-guide) show that in between the die thickness of 0.025 mm to 0.075 mm, the von-Mises and maximum shear stress are similar. However, in the die thickness range of 0.075 mm to 0.125 mm, as the die thickness increases, the von-Mises and shear stress increase.

In between the die thicknesses of 0.025mm to 0.125mm, increasing the die thickness increases the maximum tensile and compressive stresses. A comparison of all the results shows that the 0.025mm thick die had the best performance in three points bending test model. The maximum compressive and tensile stresses in 0.125mm die reached 2533.3MPa and 2084.3MPa, although the silicon die has a tensile strength of 7000MPa.

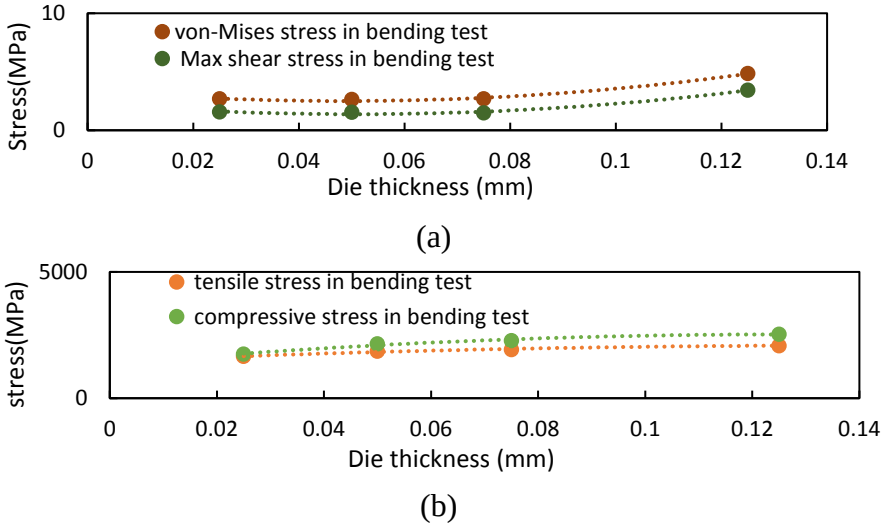
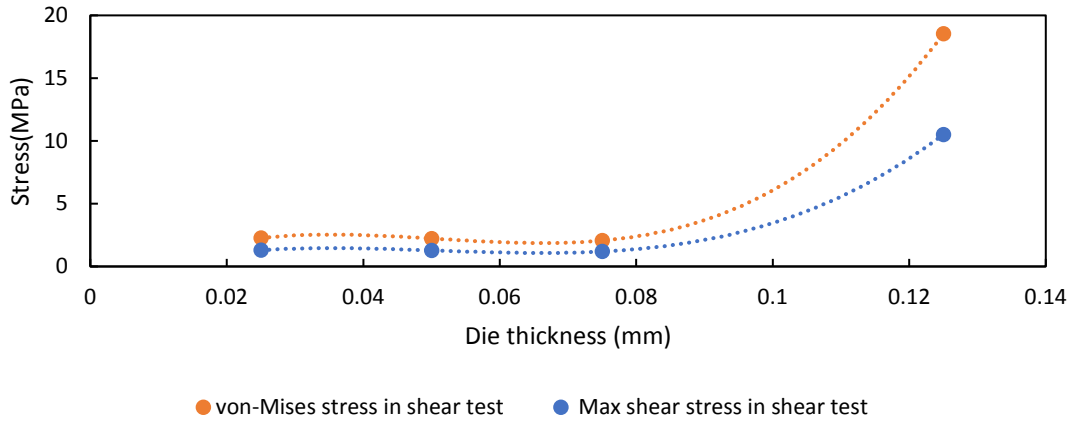


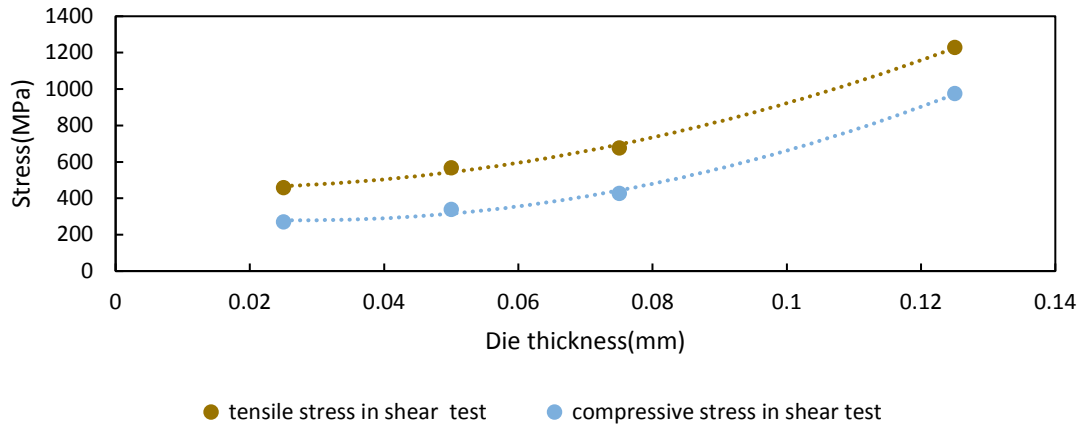
Figure 54. Stress simulation to determine the optimal thickness of the die layer using the bending test model, (a) shear stress and von-Mises stress simulated, (b) tensile and compressive stress simulated.

4.2.5.2 Effect of die thickness on the shear test model

Figure 55 (plotted line is for eye-guide) shows the von-Mises, shear, tensile and compressive stresses simulation results to determine the optimal die thickness. For the simulation results shown in Figure 55(a), with a die thickness range of 0.025 mm to 0.075 mm the von-Mises and shear stresses do not show significant change as the die thickness changes, in the die thickness range of 0.075 mm to 0.125 mm the thicker the die, the higher the von-Mises and shear stress in the die.



(a)



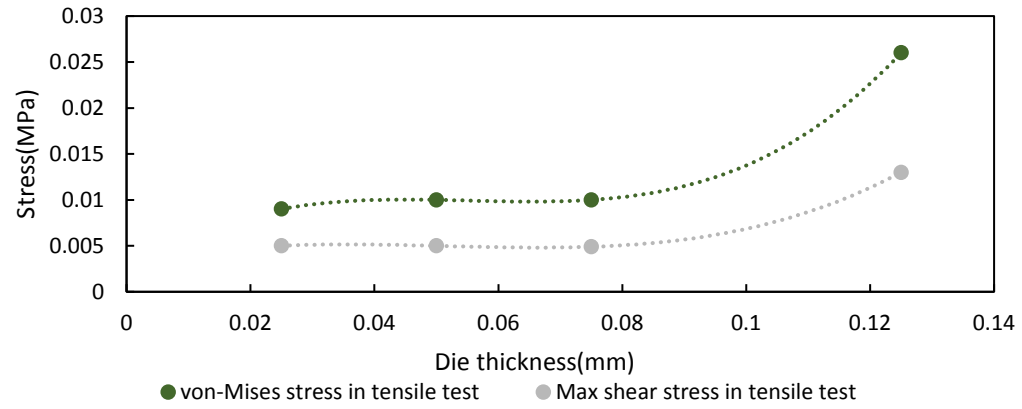
(b)

Figure 55. Shear test model simulation to determine the optimal thickness of the die layer in, (a) shear stress and von-Mises stress simulated, (b) tensile and compressive stress simulated.

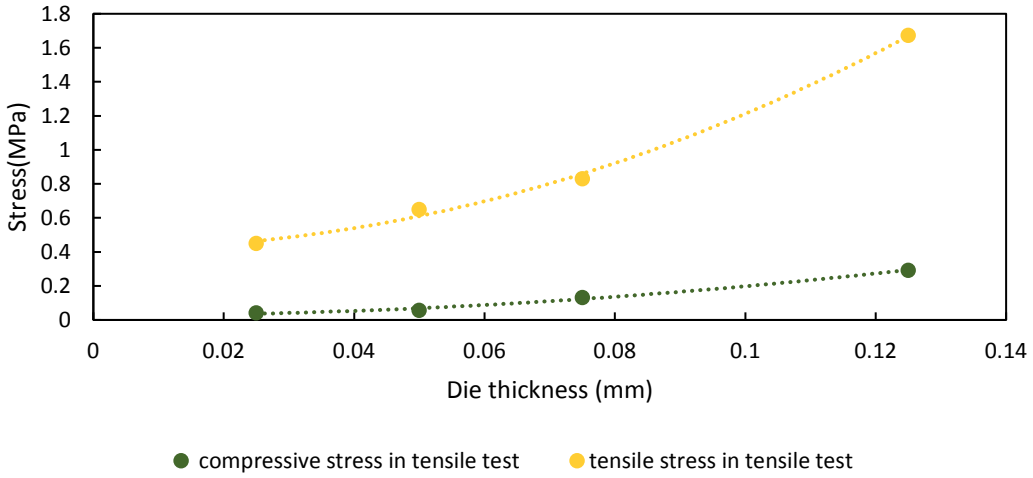
In the shear test, the maximum compressive and tensile stress are affected by increasing die thickness. The maximum difference in the tensile stress in the dies of thicknesses within 0.025 mm to 0.125 mm is about 731MPa while the maximum difference in compressive stress is about 680MPa. So, thicker die increased the failure possibility of die layer.

4.2.5.3 Effect of die thickness in the tensile test model

The tensile test model results are shown in Figure 56 (plotted line is for eye-guide). For die thickness ranging from 0.025 mm to 0.075 mm, the increase in die thickness does not significantly increase the von-Mises and shear stresses. For die thicknesses within 0.075 mm to 0.125 mm, increasing die thickness increased von-Mises and shear stresses. For die thicknesses from 0.025 mm to 0.125 mm, the compressive and tensile stresses increased as the die thickness increased. Die with thicknesses of 0.025 mm shows the best performance in this test model.



(a)



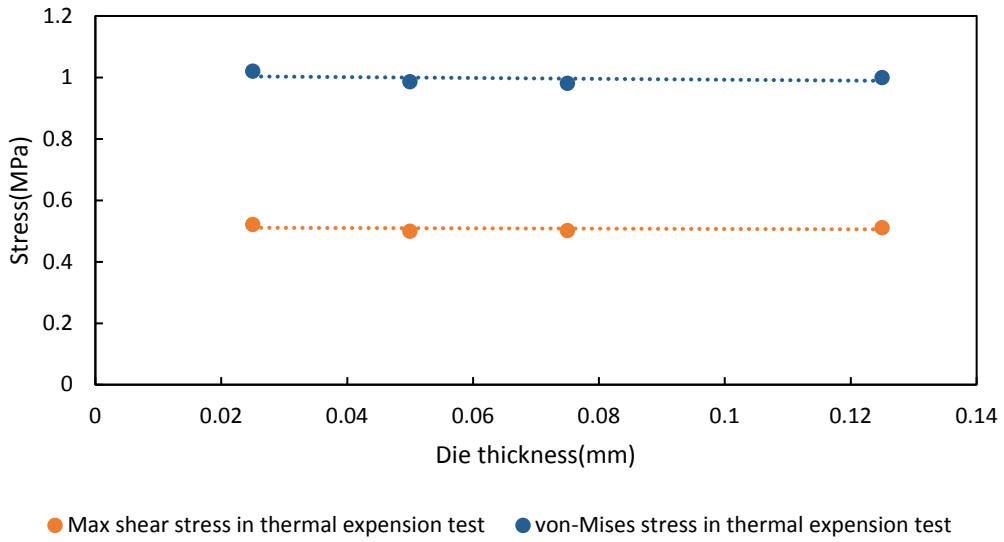
(b)

Figure 56. Stress simulation to determine the optimal die thickness in the tensile test model, (a) shear stress and von-Mises stress simulated, (b) tensile and compressive stress simulated.

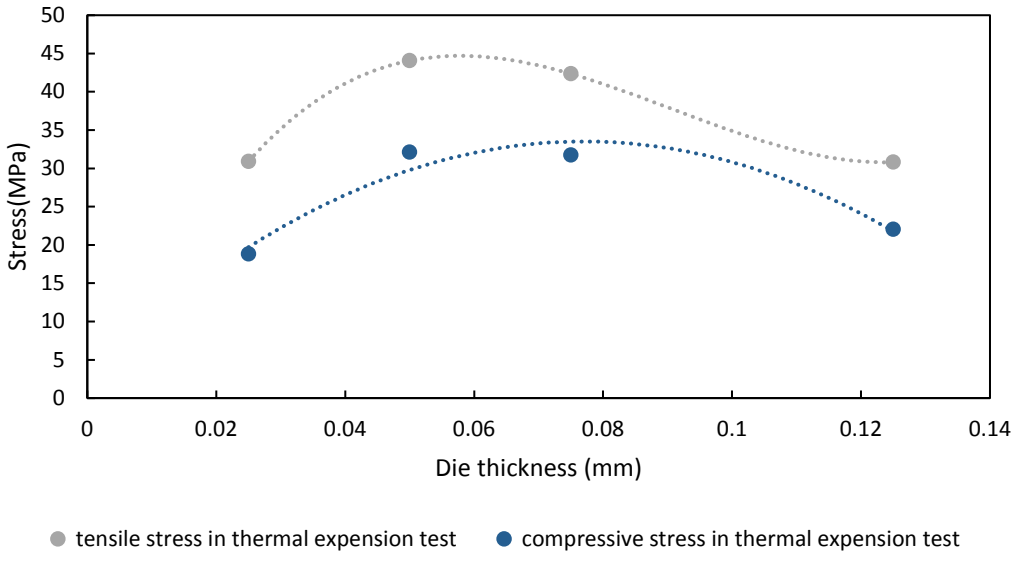
4.2.5.4 Effect of die thickness in thermal expansion test model

The shear stress and von-Mises stress are not significantly affected by changes in die thickness. When the die thickness is within 0.025 mm to 0.05 mm, the tensile and compressive stress increased when die thickness increased, but within the range of 0.05 mm to 0.125 mm the stresses decreased when die

thickness increased as shown in Figure 57 (plotted line is for eye-guide). With the consideration of package size, the die thickness of 0.025 mm has the best performance in tensile and compressive stress.



(a)



(b)

Figure 57. Stress simulation to determine the optimal die thickness in thermal expansion test model, (a) shear stress and von-Mises stress simulated, (b) tensile and compressive stress simulated.

4.2.5.5 Summary

In the bending, shear and tensile tests, a die thickness of 0.025 mm shows the smallest stresses. In thermal expansion test, the 0.025 and 0.125 mm thickness of die showed the similar tensile and

compressive stresses which are the smallest, so in this research 0.025 mm thick die should be selected to mounting onto the plastic substrate.

This section investigated the influence of the adhesive, substrate and die thickness on the stresses in the electronic packaging. The different material combinations of the electronic package of different adhesive materials (EP30AO, EP37-3FLF, Epo-Tek 301 2fl, Loctite 4902, Loctite 4860, Loctite 480, Nu355 and MK055) and different substrate (Kapton, Mylar and PEEK) have been compared. A 0.025 mm thick silicon die, 0.05 to 0.052 mm thick Kapton substrate, and a 0.05 mm EP37-3FLF adhesive layer were identified as the optimum materials and thicknesses for the electronic package.

4.2.6 Simulation for electronic packaging with top Kapton encapsulation

Electronic package with top Kapton encapsulation was simulated in this section as discussed in Section 2.6, a top encapsulation layer will be used to locate the die at the neutral axis of the assembly where the applied stress is minimum. The simulated electronic package is a five layer assembly, building on the previous model by adding an additional top adhesive and top Kapton encapsulation layer (see Figure 58). In this electronic package, the electronic die is completely encapsulated by adhesive and Kapton and since no area of the die is exposed to apply any load, it is impossible to perform shear load and tensile load tests.

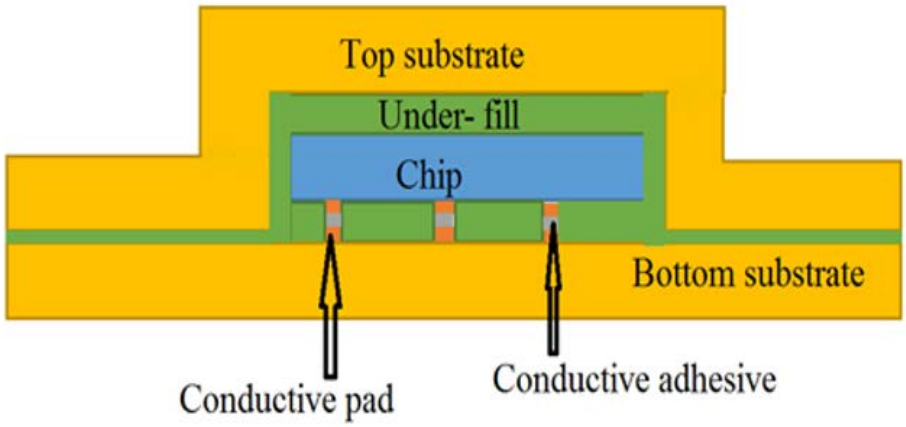


Figure 58. Cross-section of the electronic package with top Kapton cover.

Figure 59 shows the simulation geometry for the bending test for the electronic assembly described above. In this simulation, 0.05 mm thick Kapton was used as top and bottom cover, 0.025 mm thick electronic die was mounted between the Kapton layers. The adhesive used in bonding the package together is EP37-3FLF and a constant force of 30 N was applied to the centre of the top Kapton layer during the bending simulations. The 30 N external force used in this section is because of assumed 3 Kg

load into wash machine which can further prove the simulation results and give more confidence to do simulation for more complex electronic package.

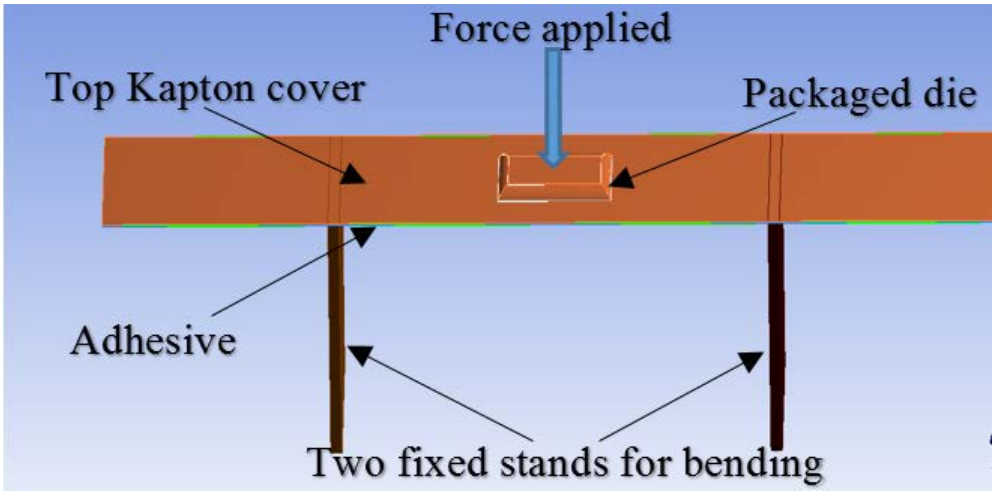


Figure 59. Simulation geometry for the electronic package with top Kapton cover, the dimension of substrate used is 100 mm (length) x 10 mm (width) x 0.05 mm (thickness), and die has dimension of 5 mm (length) x 2 mm (width), the thickness of adhesive and die are 0.05 mm and 0.025 mm respectively.

4.2.6.1 Effects of top layer adhesive thickness on stress in the electronic package

Following the previous results, in this section, the bottom layer adhesive thickness is set to the optimal thickness of 0.05 mm. The relationships between the top adhesive layer and von-Mises stress, maximum shear stress are discussed.

Figure 60 shows the relationship between the thickness of the top adhesive and the Maximum von-Mises stress. When the thickness of the top adhesive layer is in the range of 0.01 – 0.048 mm, the maximum von-Mises stress decreases as the thickness of the adhesive increases. In thickness range of 0.05 mm and 0.065 mm, maximum von-Mises stress increases as the thickness of the adhesive increases. This simulation indicates that 0.048 mm -0.05 mm of the top adhesive layer gives the optimal von-Mises stress performance.

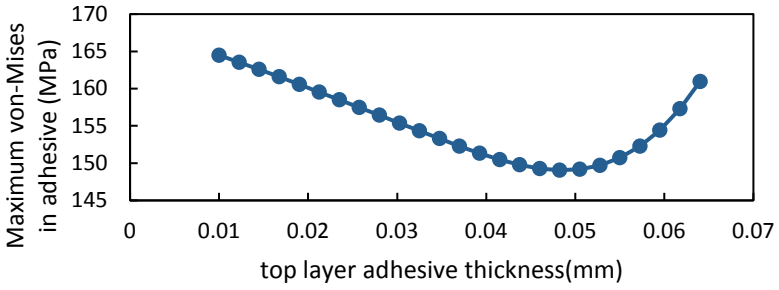


Figure 60. Simulation of top layer adhesive thickness VS maximum von-Mises stress in bending test.

The relationship between the thickness of the top layer adhesive and the maximum shear stress has also been simulated (see Figure 61). In Figure 61, the X-axis shows the thickness of the top adhesive layer and the Y-axis is the maximum shear stress in the adhesive. When the thickness of the top adhesive is in the range of 0.01 mm and 0.048 mm, the shear stress decreased as the adhesive thickness increased. In the 0.05 – 0.06 mm adhesive thickness range, the shear stresses increased with increasing adhesive thickness.

The simulation results are shown in Figure 60 and Figure 61 indicated that a 0.048 mm-0.05 mm thick top adhesive layer will yield the optimal maximum shear stress and von-Mises stress respectively.

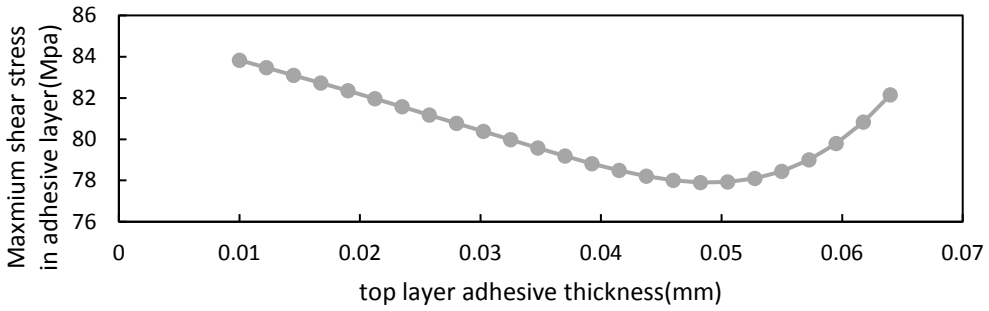


Figure 61. Simulation of top layer adhesive thickness VS maximum shear stress in the bending test.

4.2.6.2 Summary

In the bending test modelling of the electronic package with a top Kapton cover, the optimal thickness of top adhesive layers is between 0.048 to 0.05 mm. At this thickness, the top adhesive layers show the best performance for Maximum von-Mises stress and shear stress. The simulated optimal thickness of bottom adhesive layer is 0.05 mm, in this section the simulation results are further proved the adhesive thickness around 0.05 mm is the optimal thickness used in electronic package. The 0.05 mm top adhesive layer is completely symmetric with the optimal thickness of bottom adhesive simulated pervious which will located die in the neutral axis of electronic package, it can minimize the stresses in the die.

4.2.7 Simulation for the neutral axis of the electronic package

To protect the electronic die in the electronic package, the electronic die needs to be located as close to the neutral axis of the complete electronic package to minimise stresses. The neutral axis can be found by using the formula given in Appendix C.

In this section, the simulation method to find the neutral axis in the electronic package is described. The neutral axis simulation in this section can also be used to prove the optimal thickness of adhesive and top Kapton cover. The simulation steps to determine the position of the neutral axis are: (A) Simulate the stress distribution within the electronic package using the bending test model. (B) Simulate the stress distribution along a single line within the electronic package, this line starts from the centre of the top Kapton layer and ends in the centre of the bottom Kapton layer (see Figure 62). In Figure 62, point 1 is the centre of the top Kapton layer and point 2 is the centre of the bottom Kapton layer.

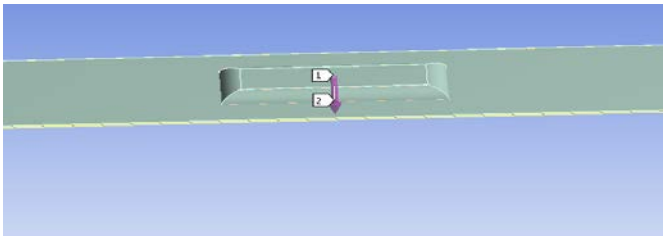


Figure 62. Centre line in electronic package.

Step A is used to determine the neutral region within the electronic package but cannot be used to determine the exact location of the neutral axis because of Step A only give neutral region not the exact position of neutral axis. Step B is used to detect the distance between the neutral axis and the top Kapton layer. Figure 63 shows the stress distribution on the electronic package, the green area in the middle of the stack package is the neutral axis area. The stress applied in the bending simulation is 20N while the top and bottom Kapton layers both have a thickness of 0.050 mm. The 20 N (assumed 2 Kg load into wash machine) used to help further prove the simulation result in Section 4.2.6. The top and bottom adhesive layers also have a thickness of 0.05 mm and the electronic die have the thickness of 0.025 mm; the adhesive used in this simulation is EP37-3FLF.

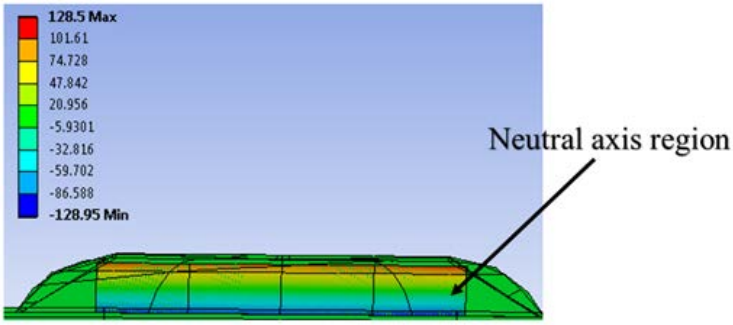


Figure 63. The cross section of stress distribution in the electronic package; green area shows the neutral axis.

Figure 64(a) and (b) shows the stress distribution in the centre line of the electronic package. Figure 64 (a) shows the overview of where the centre line is located in the electronic package and the stress in the

centre line. This figure shows that the maximum compressive stress above the neutral axis is 124.57 MPa and the maximum tensile stress below the neutral axis is 127.3 MPa.

The X-axis of Figure 64(b) is the distance between the top and bottom Kapton layers. This figure shows that the distance between the top Kapton and neutral axis is 0.1125 mm. A non-linear change in the stress is observed at the distances 0.045 mm and 0.056 mm, the reason of this non-linear change is because of these distances are the joining points of the top substrate and top adhesive layer, the large difference of Young's modulus between adhesive and substrate caused this changes. The same non-linear changes happened at distances of 0.093 mm-0.104 mm, 0.124 mm - 0.135 mm and 0.172 mm - 0.183 mm, which are the joining points between each consecutive layers of top adhesive and die layer, die and bottom adhesive layer, bottom adhesive and bottom substrate layer respectively. The stresses between 0.11 mm to 0.1125 mm are all small negative values (-0.65 MPa)while the stresses between 0.1125 mm to 0.125 mm are all small positive values (+0.65 MPa). The stress is zero at the distance of 0.1125 mm and this means that the distance between the neutral axis and top adhesive Kapton is 0.01125 mm which is half of this electronic package. The location of the neutral axis at the centre of electronic package proved the simulation result in section 4.2.6.1 which indicated that if the material and thickness of the top and bottom Kapton layers are the same, and the material and thickness of the top and bottom adhesive layers are equally the same, then the neutral axis will be located to the centre of electronic die.

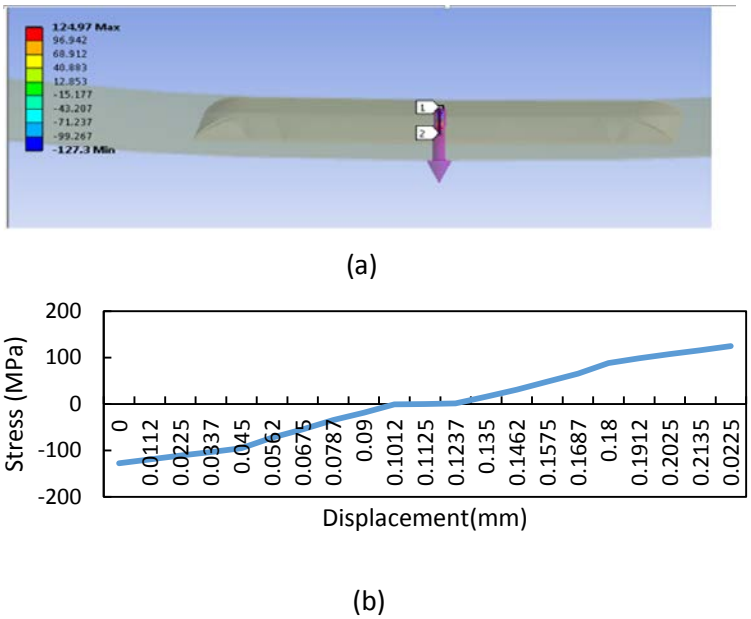


Figure 64. (a) Stress distribution of centre line, (b) distance and stress distribution in between the top to bottom Kapton layers of the electronic package.

4.3 Conclusions

In this chapter, four stress test models were shown and ANSYS FEA simulations were used to analyse the effect of adhesive and substrate materials, and effect of the die, adhesive and substrate thickness on the failure of the electronic package. The different material combinations for the electronic package using different adhesive materials (EP30AO, EP37-3FLF, Epo-Tek 301 2fl, Loctite 4902, Loctite 4860, Loctite 480, NU355 and MK055) and three different substrates (Kapton, Mylar and PEEK) have been compared. A 0.025 mm thick silicon die, 0.05 to 0.052 mm thick Kapton substrate, and a 0.05 mm EP37-3FLF adhesive layer were identified as the optimum materials and thicknesses for the electronic package. In the literature, Damian Nowak et. al [83] compared three different flexible substrates (Kapton, Mylar and Pyralux) by using a tensile tester machine to measure shear strength, Kapton produced the optimal shear force performance. Using FEA simulation to determine optimal thickness and material of each packaged layer has not been previously used in the literature is the first demonstration to used simulation method to compare different electronic package materials and thickness. The most related work is Gang Chen and Xu Chen [135] used FEA stress analysis to determine how the size of solder ball affects the electronic package, but they did not consider how the substrate and under-fill material, under-fill and substrate thickness will affect the reliability of the electronic package.

The Kapton material has the lowest Young's modulus than PEEK and Mylar material, the lower Young's modulus produces lower stresses in the bend, shear and tensile test. Kapton also has a lower coefficient of thermal expansion (CTE) than PEEK, the CTE of Kapton and Mylar are a similar value. Overall, the simulation results show that the lower Young's Modulus of the materials produces smaller von-Mises and shear stresses in the shear and bending models. The lower CTE of these materials also produces lower von-Mises and shear stresses in the thermal simulation.

In all the simulations the changing parameters are independent of each other, the varying multiple parameters at the same time have also been simulated to verify the simulation result. The under-fill adhesives were simulated on each substrate material in turn and the stress induced in the adhesive and substrate layers determined. The best combination of substrate and adhesive materials for the electronic package is identified by the lowest stress in the adhesive and substrate layers, the all simulation results

as shown in Appendix A. The Kapton substrate, together with the EP37-3FLF adhesive, were identified as the best materials combination which shows the same results as in section 4.2.1 and 4.2.2.

Chapter 5 Stress analysis experiment

The shear and bending stress experiment in this chapter aim to verify the results from the shear and bending stress simulations in chapter 4. In the experiments, the failure modes due to an externally applied force on an electronic package were investigated as the thickness of the adhesive layer is varied. This helps to determine the optimal adhesive thickness for which the failure in the electronic package is minimal. The external force is very difficult to applied onto the top surface of packaged die for the tensile experiment test, so, the tensile experiment test will not be used to do verification.

The values of these shearing forces from the shear experiment can also be used in simulation to determine the shear strength of adhesive which can be used to compare the adhesion strength of different materials. This new method to determine the adhesive strength has also introduced in this chapter.

5.1 Shear load test experiment

The shear load experiment was conducted using an electronic package holder and an Electroplus 1000 mechanical test machine shown in Figure 65. The electronic package holder (homemade) in Figure 65(a) consists of the platform “a” for applying force to the electronic package “b”, which is held in position by two clams which hold the substrate flat against the rig back plate. The force is exerted on the package by the edge of the platform “d” which is aligned to the side of the die to enable shearing. The force is applied to the platform “a” using the Electroplus 1000 mechanical test machine in Figure 65(b). The machine is designed for dynamic and static testing on a wide range of material and components. It is digitally controlled by a computer software Instron plus and has a dynamic load capacity of ± 1000 N and a long-term static load capacity of ±710N.

To validate the simulation results, the boundary conditions for the simulations were replicated for the shear load experiment. The boundary conditions for the shear load simulation are: (1) external force applied is on the left edge surface of die; (2) the left and right edges surface of substrate are fixed; (3) the top and bottom surface of substrate will be fixed on Z direction while it is free to move along the X, Y directions. Similarly, the procedures for the experiment are closely correlated to the simulations as: (1) the Electroplus machine is used to apply an external force to one edge surface of die; (2) the two edges of substrate are fixed by the two clamps; (3) Z direction of substrate is fixed by back plate of rig.

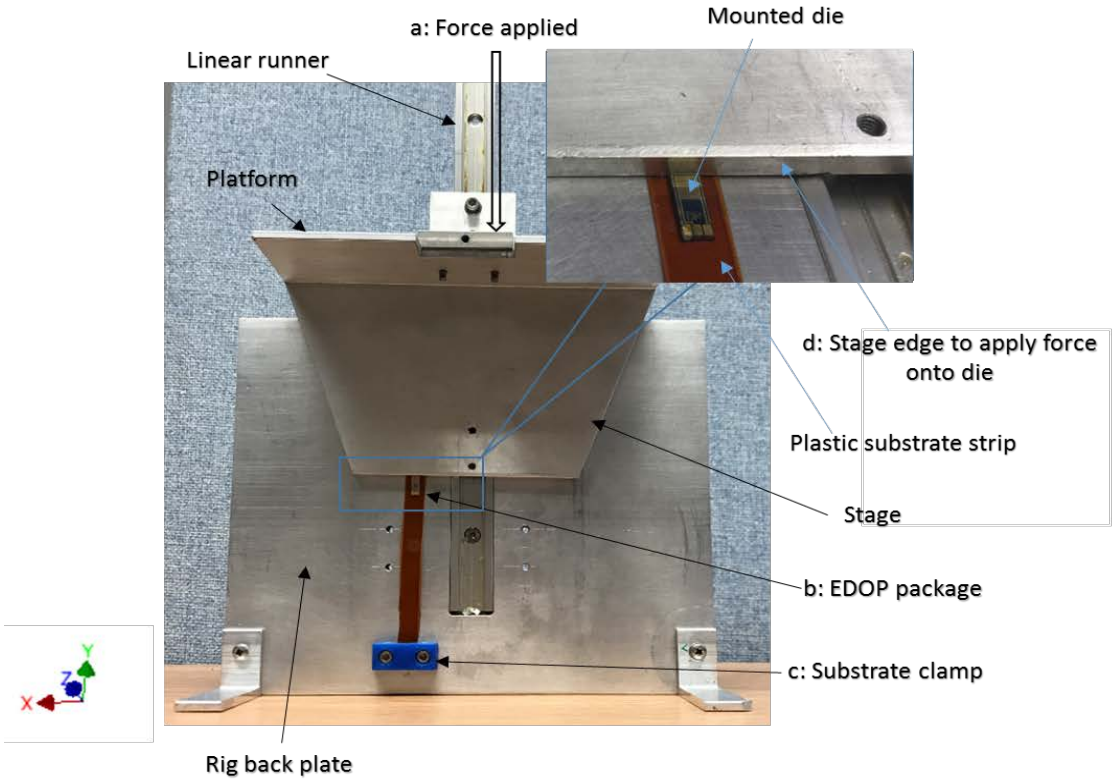


Figure 65. Equipment for shear load experiment, (a) electronic package holder; (b) Electroplus 1000 mechanical test machine used to apply force.

5.1.1 Shear load experiment results

Three flexible adhesives (Loctite 4860, Loctite 480 and Loctite 4902) and three under-fill adhesives (EP30AO, EP37-3FLF and Epo-Tek 301 2fl) were shear tested in the experiment, for each adhesive

multiple samples (between 6 and 18, one sample at each thickness) were tested. The thickness of each adhesive was varied from 0.01 mm to 0.08 mm within the test samples which comprise a Kapton substrate 180 mm (length) x 10 mm (width) x 0.125 mm (thickness), and an 8 mm (length) x 3.5 mm (width) x 0.53 mm (thickness) silicon die for the shear load, It is very hard to apply force to a thinner die since the force need apply to the edge surface of die as shown in Figure 65(a). The shear force at the point of failure in the adhesives was obtained to produce Figure 66 – 71 which gives a relationship between the adhesive thicknesses versus maximum shear stress (caused package break). The maximum shear force required to break the package across the whole range of adhesive thicknesses will indicate the optimum thickness, below the optimal thickness, the shear force at which the electronic packaged fails begins to increase as the adhesive thickness increased, and above the optimal thickness, the shear force at which the electronic packaged fails begins to decrease as the adhesive thickness increased.

The shear test result for the Loctite 4860 (as shown in Figure 66) shows that the optimal Loctite 4860 thickness to be used in an electronic package should be within the range 0.042 mm to 0.048 mm. This is because the shear force at the point where the adhesive fails or breaks (that is the failure force) increasing when the adhesive thickness in the range of 0.01 mm to 0.042 mm, and starts decreasing when the adhesive thickness increased from 0.048 mm to 0.065 mm. The measured tolerances in the experiment of the adhesive thickness and the failure force are ± 0.002 mm and ± 4N respectively (this tolerances also are error bars in Figures).

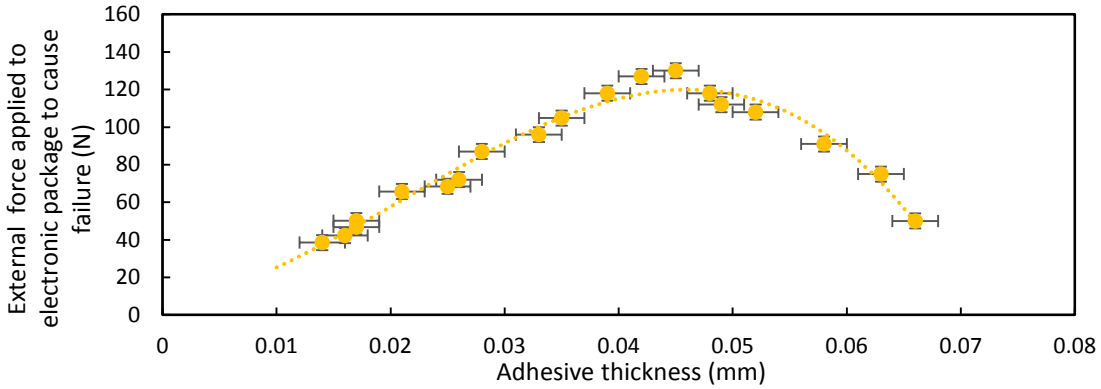


Figure 66. Shear load experiment results for loctitle4860 (plotted line as eye-guide).

For Loctite 480 adhesive, the thickness of adhesive in the experiment was varied between 0.012 mm to 0.068 mm as shown in Figure 67. The result shows an increase in the failure force as the adhesive thickness increased within the adhesive thickness in the range of 0.012 mm to 0.038 mm. In the range of 0.04 mm to 0.068 mm, the adhesive thickness increased as the failure force decreased as shown in

Figure 67. Therefore the optimal adhesive thickness of the Loctite 435 layer is in range of 0.038-0.04 mm. The measured tolerances of adhesive thickness and failure force in the experiment are ±0.002 mm and ± 4N.

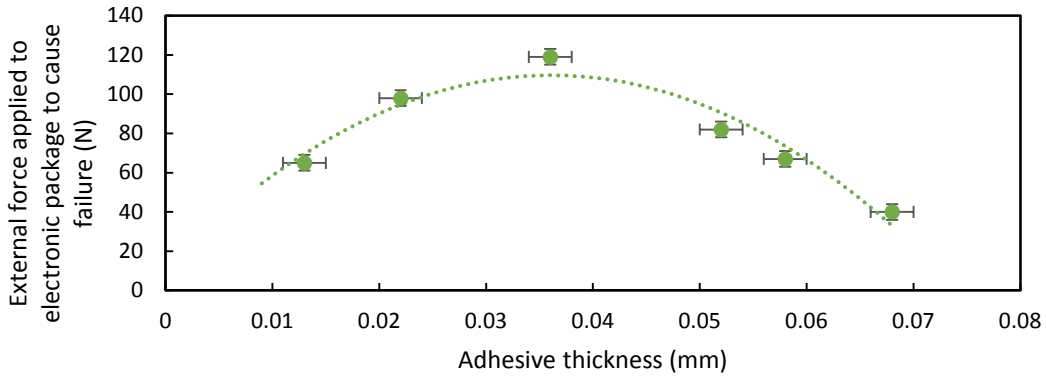


Figure 67. Shear load experiment results for Loctite 480 (plotted line as eye-guide).

Figure 68 shows the shear load experiment results for Loctite 4902 with the adhesive thickness varied between 0.013 mm and 0.068 mm. The result shows that the failure force increased as the adhesive thickness increased within the adhesive thickness range of 0.013 mm to 0.042 mm. In the adhesive thickness range of 0.042 mm to 0.068 mm, the failure force decreases as the adhesive thickness increases. These results give that the optimal thickness for Loctite 4902 adhesive layer is 0.042 mm. The measured tolerances of adhesive thickness and failure force in the experiment are ±0.002 mm and ± 4N.

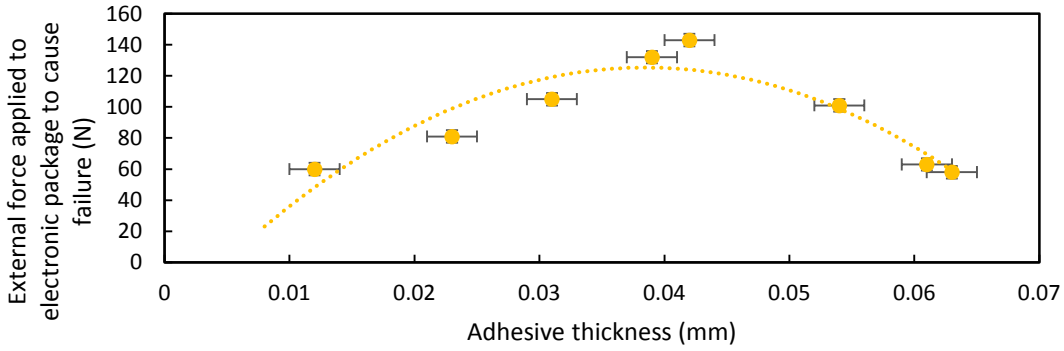


Figure 68. Shear load experiment results for Loctite4902 (plotted line as eye-guide).

The EP30AO under-fill adhesive was also shear tested within the adhesive thickness in the range of 0.013 mm to 0.072 mm, the results are shown in Figure 69. The failure force increased when the adhesive thickness increased from the range of 0.013 mm to 0.047 mm but as the adhesive thickness increased from 0.049 mm to 0.072 mm, the failure force decreased. The maximum shear force at the point where the electronic packaged failed when using the EP30AO under-fill is obtained within the

thickness of 0.047 mm to 0.049 mm. The measured tolerances of adhesive thickness and failure force in the experiment are ±0.002 mm and ± 4N.

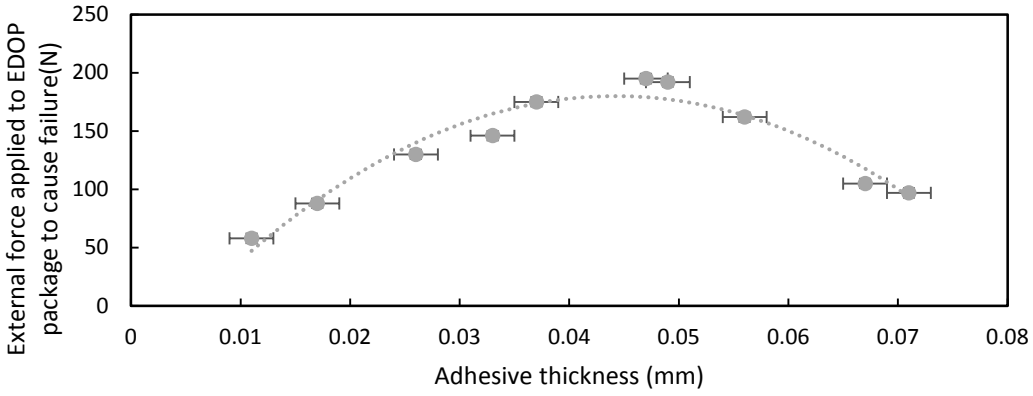


Figure 69. Shear load experiment results for EP30AO (plotted line as eye-guide).

Figure 70 shows the shear load experiment results for EP37-3FLF under-fill adhesive. The thickness range of 0.008 mm to 0.068 mm has been tested. In the thickness range of 0.008 mm to 0.048 mm, the shear force increased as the adhesive thickness increased while the shear force decreased as the adhesive thickness increased from 0.05 mm to 0.068 mm. This result shows that the under-fill thickness within the range of 0.048 mm to 0.05 mm is best when EP37-3FLF is used in the electronic package. The measured tolerances of adhesive thickness and failure force in the experiment are ±0.002 mm and ± 4N.

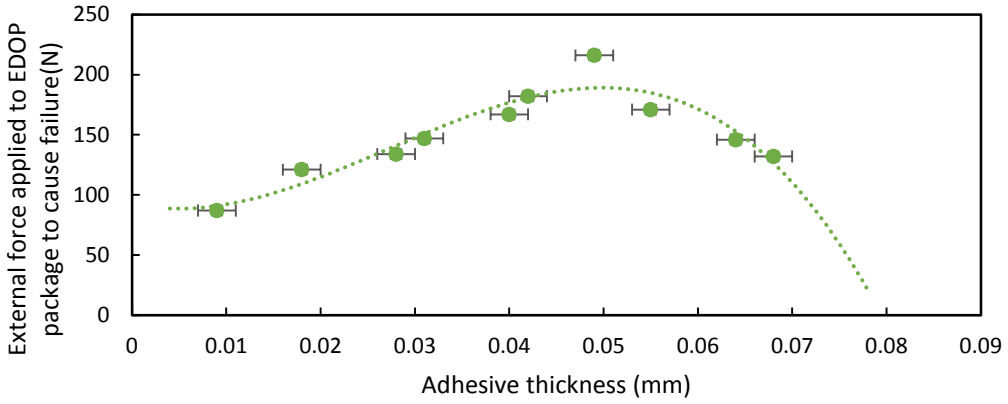


Figure 70. Shear load experiment results for EP37-3FLF (plotted line as eye-guide).

For the Epo-Tek 301 2fl, the adhesive thickness in the range of 0.01 mm to 0.078 mm has been tested as shown in Figure 71. The result shows that the electronic package has a better resistance to shear loading when the thickness of the Epo-Tek 301 2fl adhesive is in the range of 0.043 mm to 0.045 mm. Above

this thickness range, the shear force at which the electronic packaged fails begins to decrease. The measured tolerances of adhesive thickness and failure force in the experiment are ±0.002 mm and ± 4N.

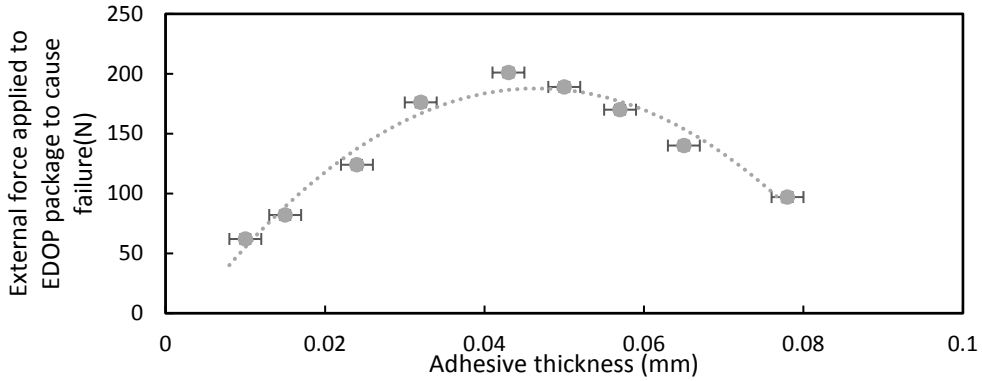


Figure 71. Shear load experiment results for Epo-Tek 301 2fl (plotted line as eye-guide).

5.1.2 Summary

In section 5.1, the six different adhesive materials have been tested under shear load experiment. The optimal ranges of adhesive thickness for Loctite 4860, Loctite 480, Loctite 4902 , EP30AO, EP37-3FLF and Epo-Tek 301 2fl are 0.042-0.048 mm, 0.038-0.04 mm, 0.042 mm, 0.047-0.049 mm, 0.048-0.05 mm and 0.043-0.045 mm respectively. The shear force at these thicknesses for Loctite 4860, Loctite 480, Loctite 4902 , EP30AO, EP37-3FLF and Epo-Tek 301 2fl are 130 N, 119 N, 143 N, 192 N, 216 N and 201 N respectively, as shown in Table 5. The largest shear force for the EP37-3FLF shows that the adhesive more resistant to shear loading and this also indicates that the EP37-3FLF has the best stress performance.

Table 5. Maximum failure force and optimal thickness of six adhesive materials.

Adhesive	Maximum failure force (N)	Optimal thickness (mm) – shear load experiment
Loctite 4860	130	0.042-0.048
Loctite 480	119	0.038-0.04
Loctite 4902	143	0.042
EP30AO (under-fill)	192	0.047-0.049
EP37-3FLF (under-fill)	216	0.048-0.05
Epo-Tek 301 2fl (under-fill)	201	0.043-0.045

5.2 Bending test experiment

The shear test rig was slightly modified as shown in Figure 72 to perform the bending test experiment. In this case, a probe is attached to the underside of the platform “a” to apply the external force at the mid-point of the electronic package which is clamped at either end by clamps “c” and “d” to realise the 3 point bending test undertaken in the simulation.

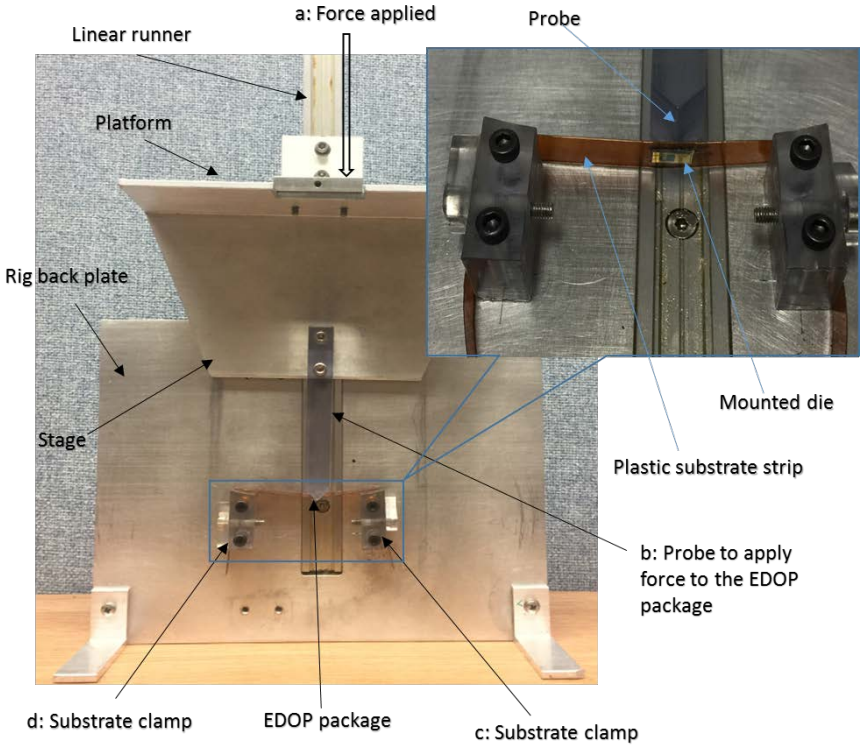


Figure 72. Electronic package holder for bending experiment.

The experiment was conducted with a Kapton substrate 180 mm x 10 mm x 0.125 mm, and a smaller 2 mm x 2 mm x 0.1 mm metal die for the bending case which is different with the chip size used for shear experiment test. The experimental and simulated evaluation of two different die sizes and materials in shear and bending experiments enable a more in depth comparison between the experimental and simulation results providing greater confidence in the validation process. In the bending experiment, the optimum adhesive thickness is obtained at the adhesive thickness where the maximum bending force required to break the electronic package is greater than the bending forces at other thicknesses.

For each adhesive multiple samples (between 6 and 18, one sample at each thickness) were tested. The bending test results for under-fill adhesive Loctite 4860 for the thickness range of 0.01 mm to 0.06 mm are shown in Figure 73. The results show the electronic package can withstand up to 77.56 N provided the Loctite 4860 thickness in the package is maintained between 0.045 mm to 0.048 mm. As the thickness of the adhesive exceeds or falls from this value, the electronic package fails at lower bending forces. The measured tolerances of adhesive thickness and failure force in the experiment are ±0.002 mm and ± 4N.

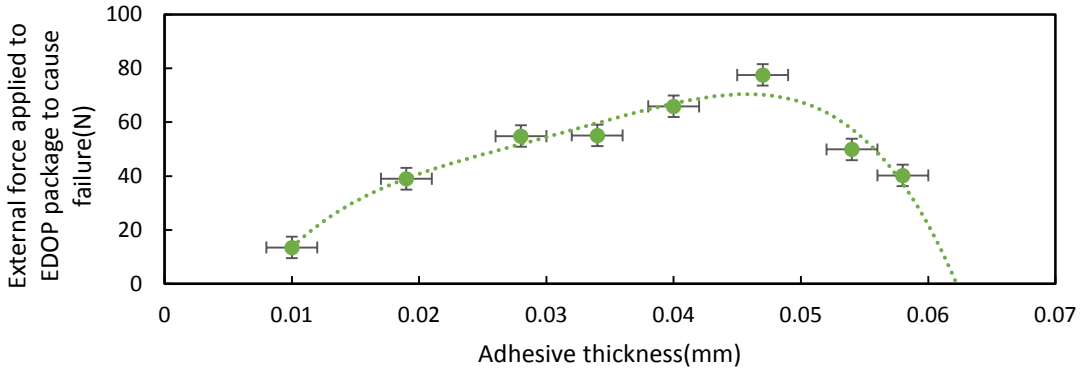


Figure 73. Bending experiment results for Loctite 4860 (plotted line as eye-guide).

Figure 74-78 show the bending test experiment test results for adhesive Loctite 480, Loctite4902, EP30AO, EP37-3FLF and Epo-Tek 301 2fl respectively. The results show that the optimal adhesive thicknesses for these materials are 0.038 mm to 0.04 mm, 0.042 mm, 0.047 mm to 0.048 mm, 0.048 mm to 0.05 mm and 0.043 mm respectively. The measured tolerances of adhesive thickness and failure force in the experiment are ±0.002 mm and ± 4N.

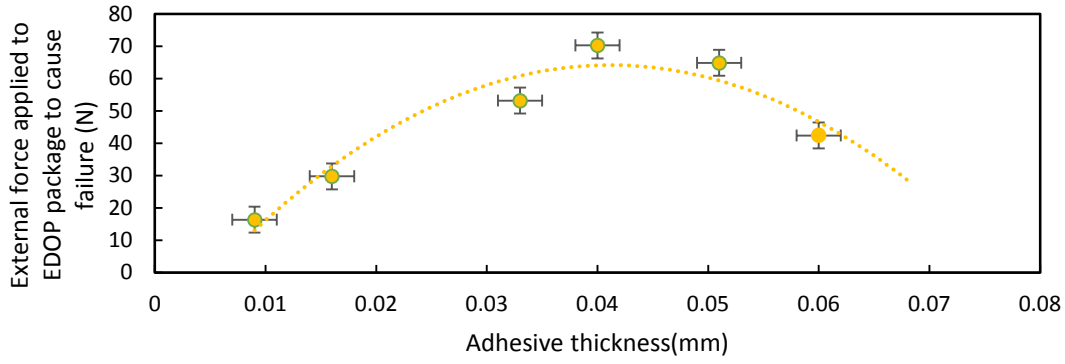


Figure 74. Bending experiment results for Loctite 480 (plotted line as eye-guide).

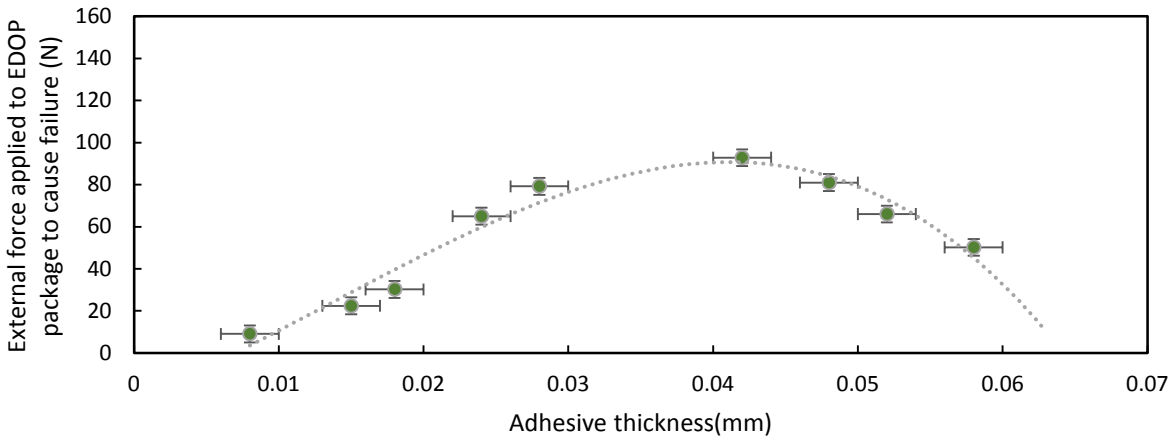


Figure 75. Bending experiment results for Loctite 4902 (plotted line as eye-guide).

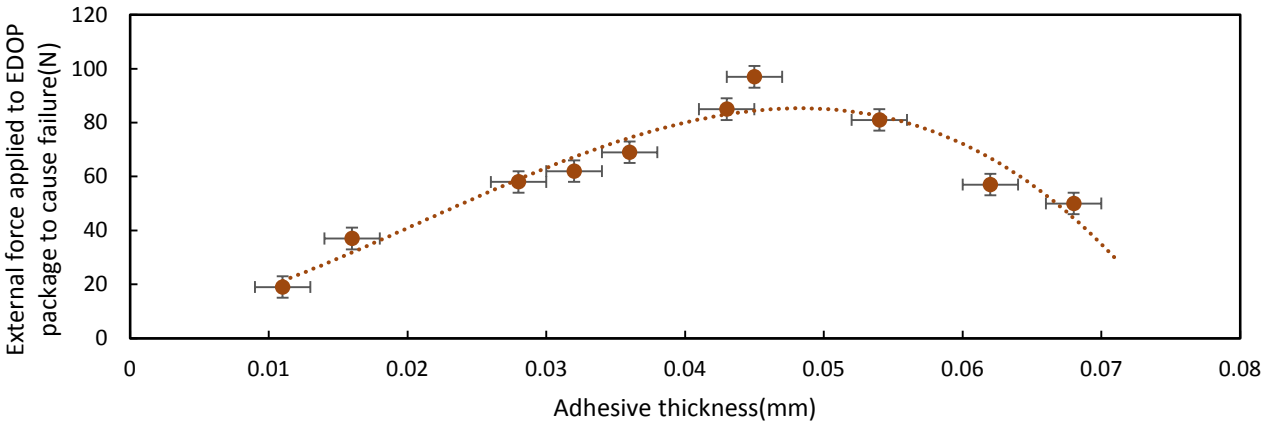


Figure 76. Bending experiment results for EP30AO (plotted line as eye-guide).

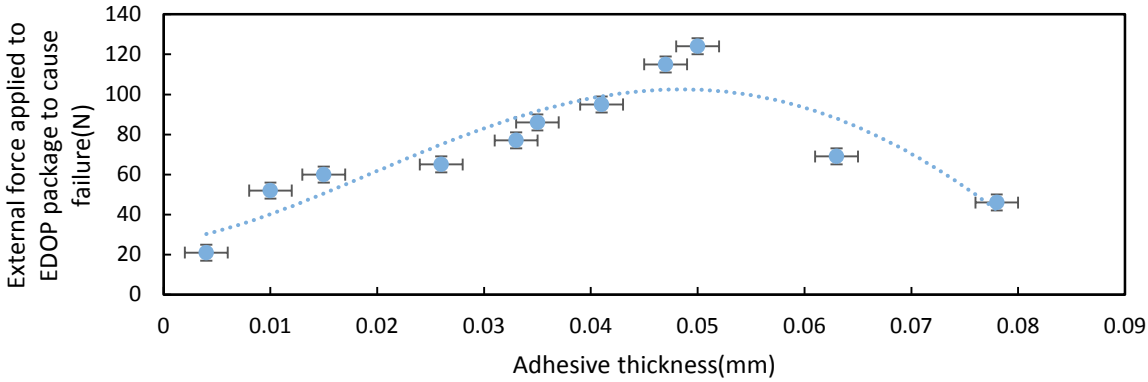


Figure 77. Bending experiment results for EP37-3FLF (plotted line as eye-guide).

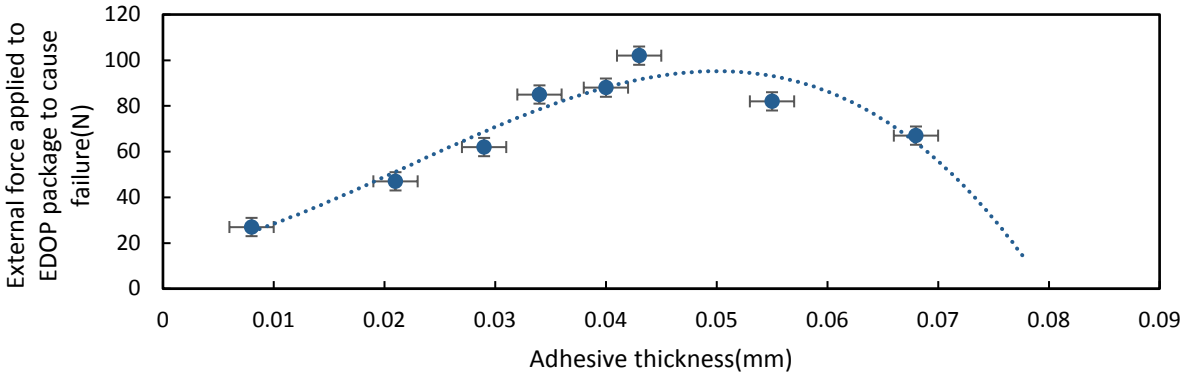


Figure 78. Bending experiment results for Epo-Tek 301 2fl (plotted line as eye-guide).

5.2.1 Summary

In this section, the adhesive Loctite 4860, Loctite 480, Loctite4902, EP30AO, EP37-3FLF and Epo-Tek 301 2fl have been experimentally tested under bending. The results show that the EP37-3FLF adhesive with the optimal thickness of 0.048 mm to 0.05 mm performs better than other adhesives in bending and can survive a maximum bending force of up to 124 N beyond which it fails as shown in Table 6. This also shows that the EP37-3FLF adhesive has the best stress performance just as in the shear test experiment and bending simulations.

Table 6. Maximum failure force and optimal thickness of six adhesive materials.

Adhesive	Maximum failure force (N)	Optimal thickness (mm) shear load experiment
Loctite 4860	77.56	0.045-0.048
Loctite 480	70.25	0.038-0.04
Loctite 4902	92.8	0.042
EP30AO (under-fill)	97	0.047-0.048
EP37-3FLF (under-fill)	124	0.048-0.05
Epo-Tek 301 2fl (under-fill)	102	0.043

5.3 Validation of shear load and bending simulation

The shear load and bending experiments have been undertaken to determine the force at which the package fails when the thickness of the adhesive layer in the electronic package is varied. For each adhesive multiple samples (between 6 and 18, one sample at each thickness) were tested and the external force required to cause the electronic package to fail is plotted in Figure 79-84 versus adhesive thickness. All six under-fill adhesives have been tested in this way with different adhesive thicknesses being achieved by controlling the amount of adhesive dispensed. Each of these adhesives was tested with the varying adhesive thickness in the samples and experimental results were then compared with the simulations. The geometry and material properties affect the coupling of the stress between the films and alter the position of neutral axis of the assembly. For every adhesive, there is an optimum thickness where the stress in the adhesive is minimised.

The simulation in this section was conducted with a Kapton substrate 180 mm x 10 mm x 0.125 mm, and an 8 mm x 3.5 mm x 0.53 mm silicon die for shear or a smaller 2 mm x 2mm x 0.1 mm metal die for the bending case. In each case, the length and width of the adhesive layer match the die dimension in the electronic package. The materials and size of materials used in the simulation are same as used in shear and bending experiment.

The simulation results in this validation exercise consist of the stress in the adhesive for different thicknesses. At the optimum thickness, the simulation results should indicate minimum stress in the adhesive compared with other thicknesses. For the experimental results, the maximum force required to break the package compared with other thicknesses will indicate the optimum thickness. The validation exercise compares the simulation result with the experimental result. The thicknesses of the adhesive layer are between 0.01 mm and 0.08 mm and a 20 N shear load and bending force is applied in the simulations.

Figure 79 shows the simulation and experimental results for Loctite 4860. The simulation results for shear load and bending are shown in Figure 79(a), which indicates the optimal thickness of the adhesive is between 0.042 mm to 0.047 mm in both bending and shear cases. The experimental results are shown in Figure 79(b) and this indicates that the optimal adhesive thickness of the Loctite 4860 layer in the shear load experiment is in the range 0.042 mm to 0.045 mm, the experimental result is same as described in section 5.1.1 and the result figure shows here again for easily compare with the simulation results. For the bending experiment, the optimal thickness is between 0.045 and 0.048 mm. The optimal

thickness in both simulation and experimental results closely correlate and the optimum adhesive thickness shows good agreement, which indicates that at that thickness the stress in the adhesive layer is minimised. The fact the adhesive fails in-elastically and the simulation was performed elastically does not affect the agreement between the results - there is clearly an optimum adhesive thickness where the stress induced in the adhesive by the applied load is minimised. The small error between simulation and experiment is due in part to the tolerance in measuring the adhesive thickness. The thickness of the adhesive layer for each sample was determined by measuring the total thickness of the sample minus the thickness of the substrate and die. All thicknesses were measured using a digital micro-meter with a tolerance of 0.002 mm.

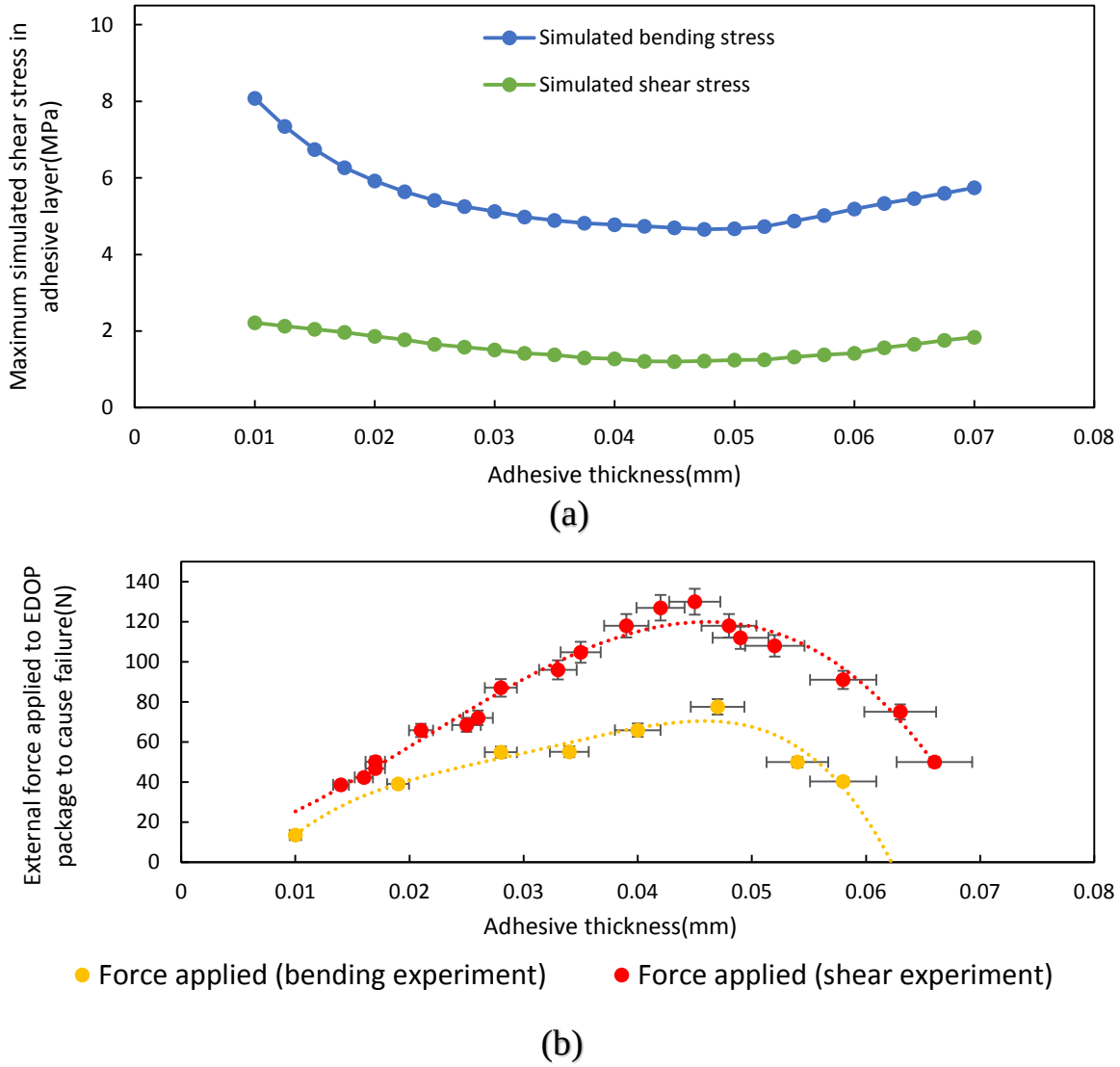


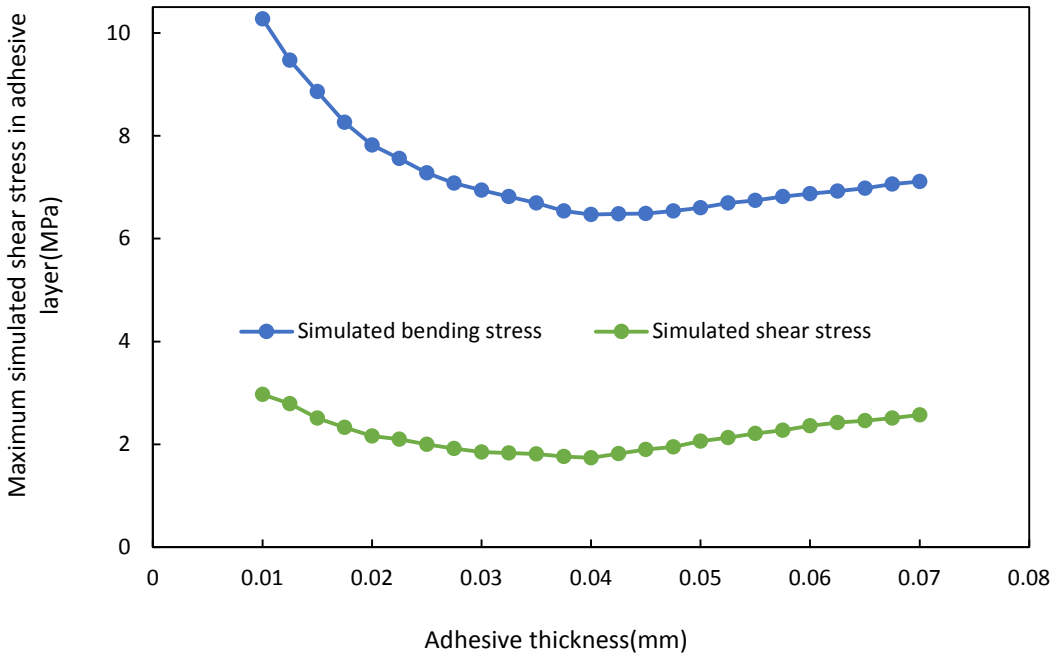
Figure 79. Comparison of results for Loctite 4860, (a) simulated bending and shear stresses versus adhesive thickness (20 N force) (b) external force required to cause failure versus adhesive thickness (plotted line as eye-guide).

Both simulation and experimental results have indicated an optimum thickness exists for all adhesives tested. The comparison between simulation and experiment for Loctite 480, Loctite 4902, EP30AO, EP37-3FLF and Epo-Tek 301 2fl are shown in Figure 80 - 84 respectively. The optimum adhesive thickness for each material is shown in Table 7.

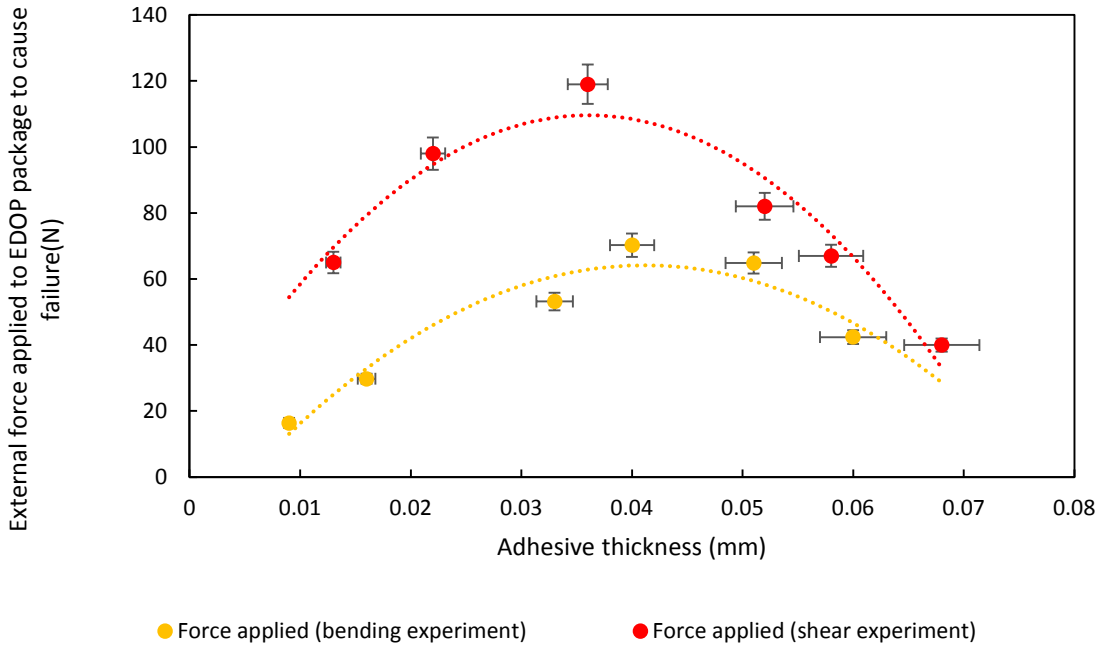
In the simulation, for the same adhesive thickness, the simulated shear stress in the EP30AO and Epo-Tek 301 2fl adhesive in shear and bending cases is much higher than for the Loctite 4902. However, in the shear and bending experiments, the force needed to break the EP30AO and Epo-Tek 301 2fl package is much higher than the Loctite 4902 package. This is because the EP30AO and Epo-Tek 301 2fl adhesives have much higher shear strength than Loctite 4902. So for the adhesives with similar shear strength, the smaller shear stress simulated in bending and shear cases shows improved stress performance.

Table 7. Optimum thickness results for six adhesive materials.

Adhesive	Optimum thickness (mm) - simulation	Optimal thickness (mm) - experiment
Loctite 4860	0.042-0.047	0.042-0.048
Loctite 480	0.04	0.038-0.04
Loctite 4902	0.04-0.045	0.042
EP30AO (under-fill)	0.047	0.047-0.049
EP37-3FLF (under-fill)	0.05	0.048-0.05
Epo-Tek 301 2fl (under-fill)	0.045-0.047	0.043-0.045

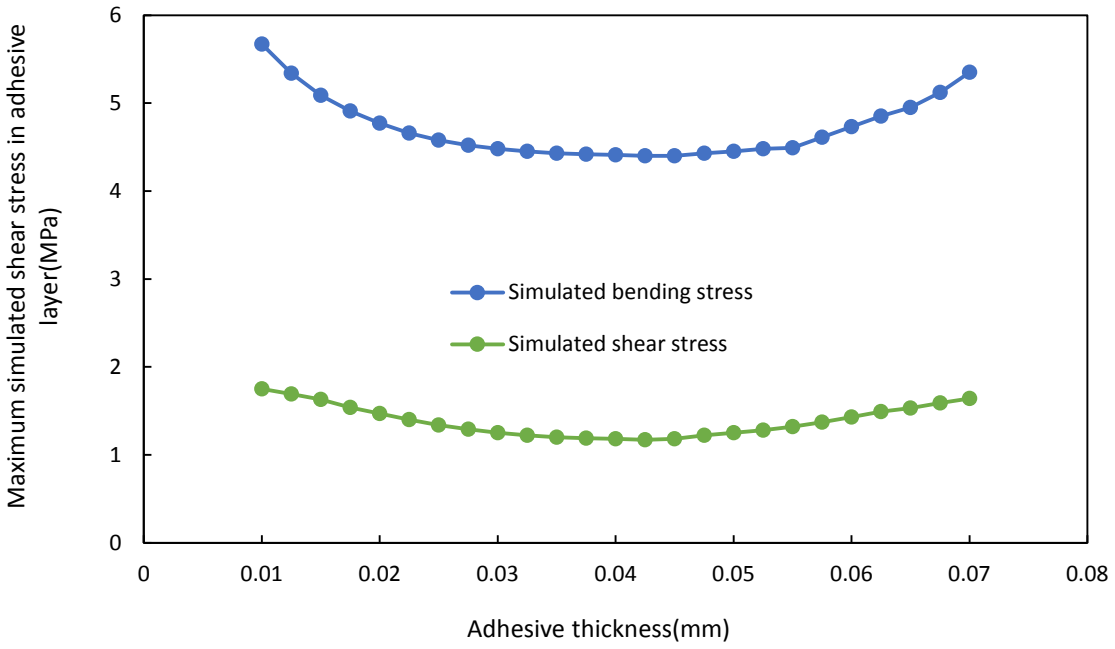


(a)

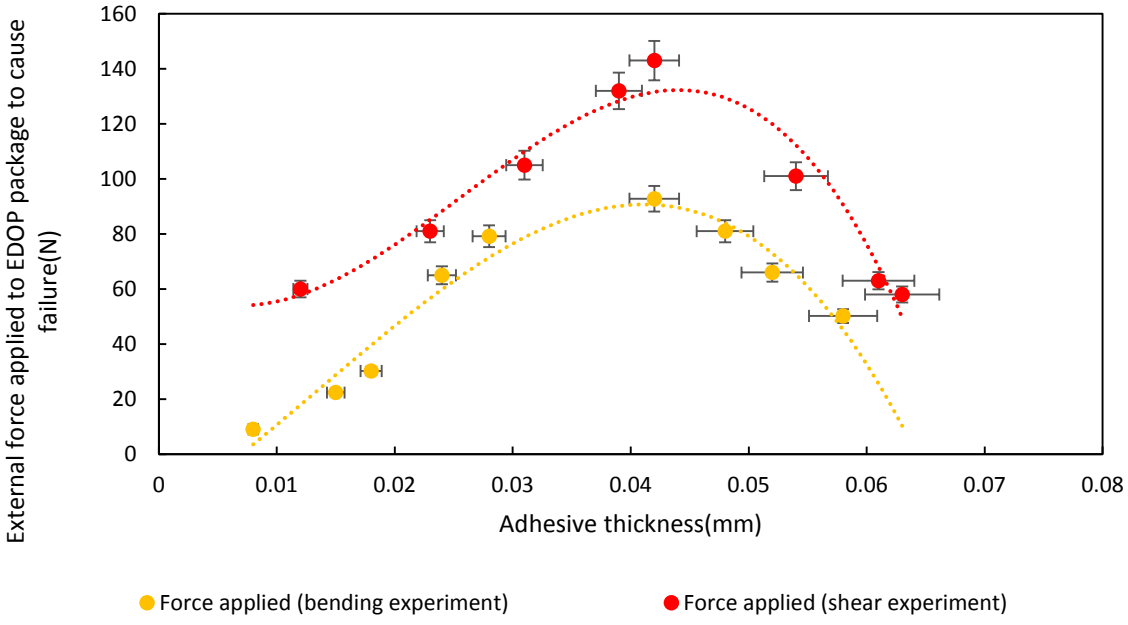


(b)

Figure 80.Comparison of results for Loctite 480, (a) simulated bending and shear stresses versus adhesive thickness (20 N force) (b) external force required to cause failure versus adhesive thickness (plotted line as eye-guide).

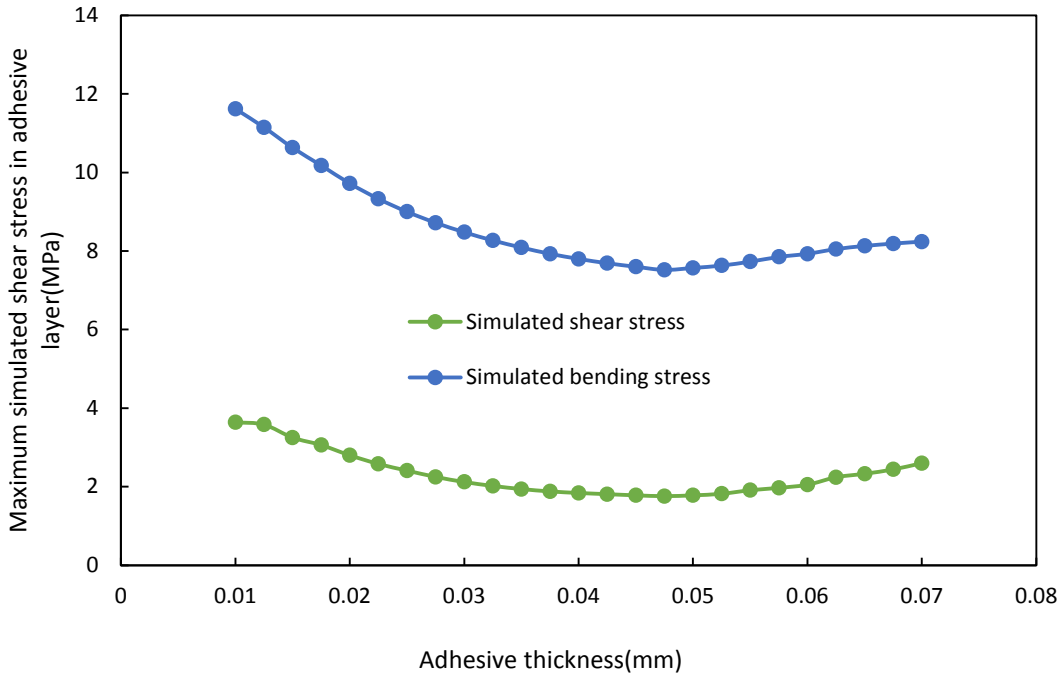


(a)

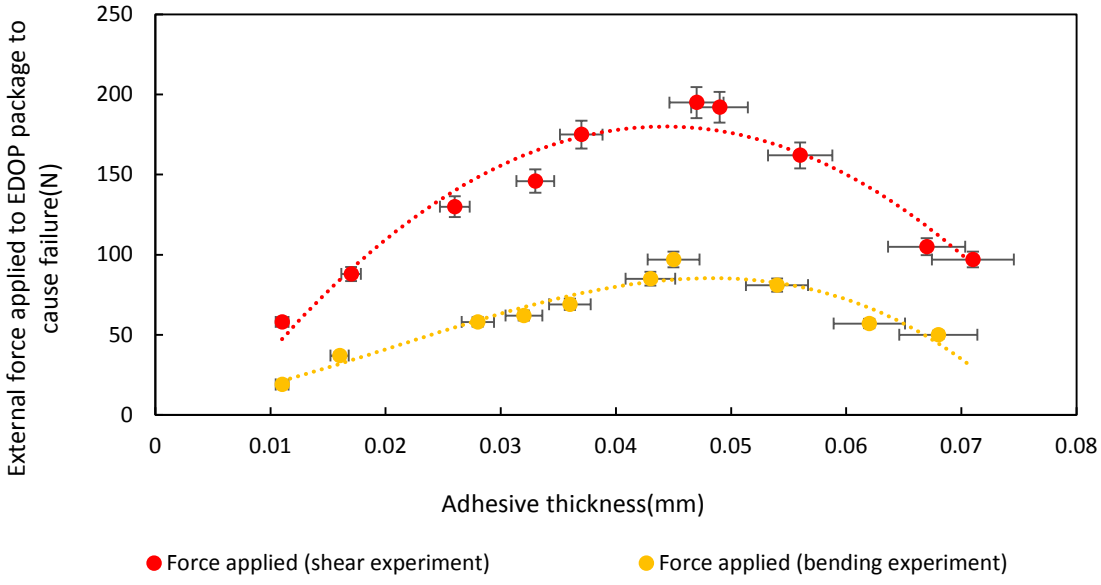


(b)

Figure 81. Comparison of results for Loctite 4902 (a) simulated bending and shear stresses versus adhesive thickness (20 N force) (b) external force required to cause failure versus adhesive thickness (plotted line as eye-guide).

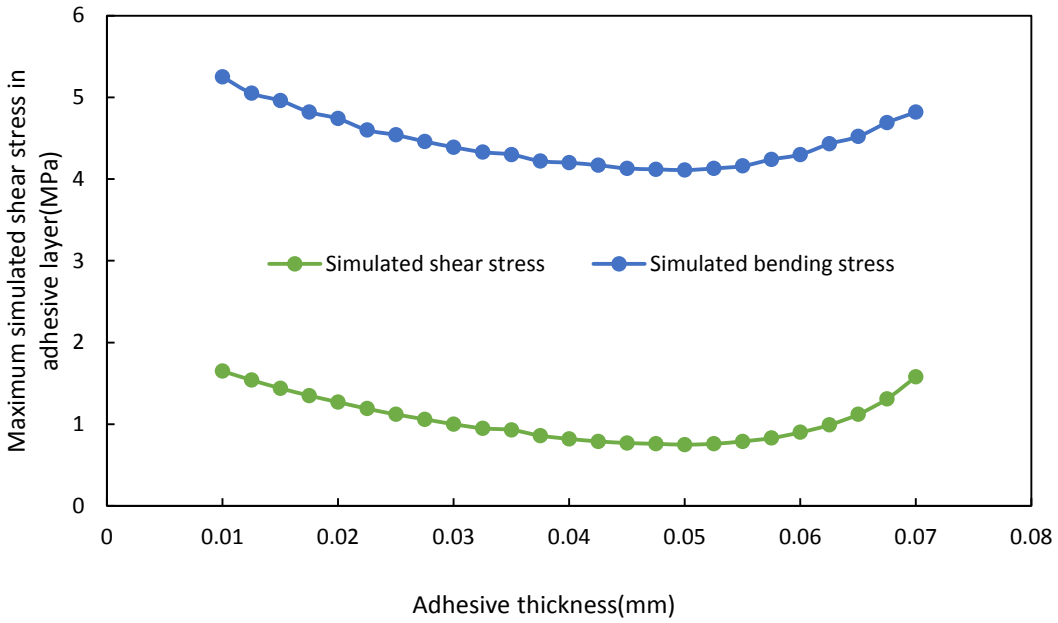


(a)

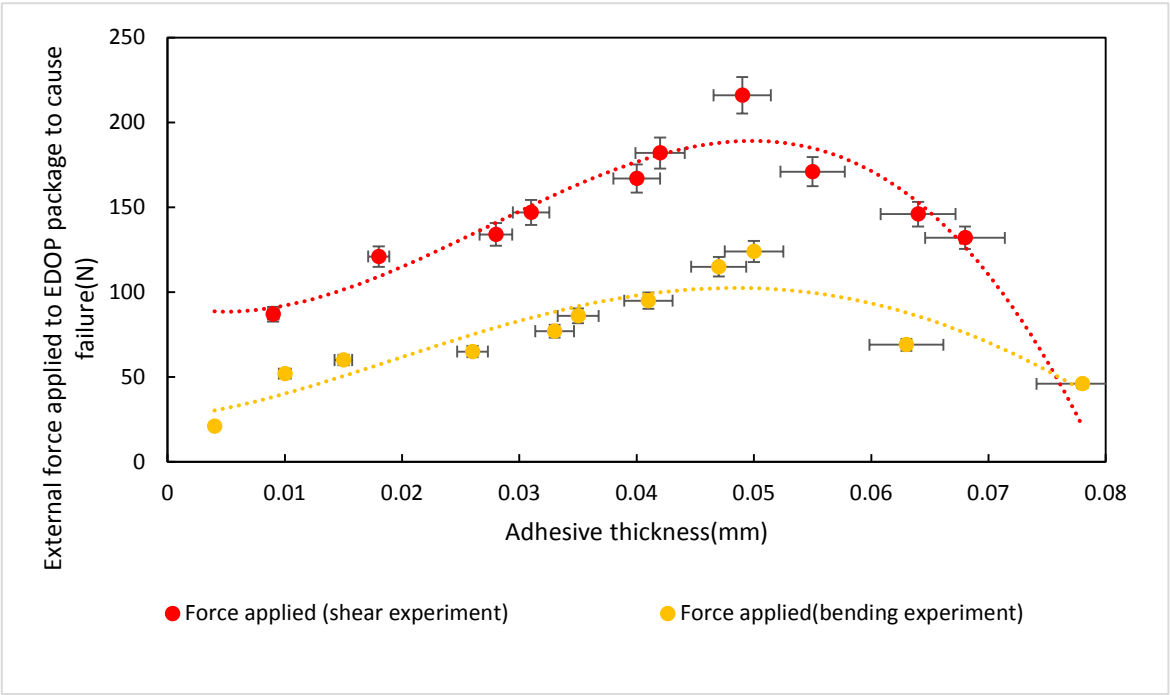


(b)

Figure 82. Comparison of results for EP30AO, (a) simulated bending and shear stresses versus adhesive thickness (20 N force) (b) external force required to cause failure versus adhesive thickness (plotted line as eye-guide).

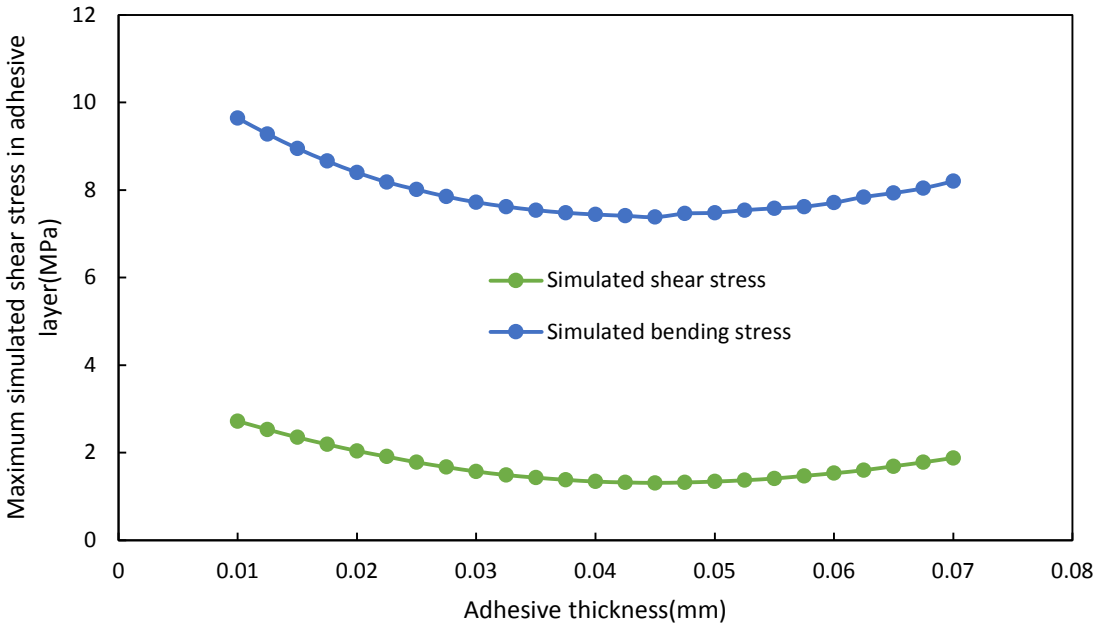


(a)

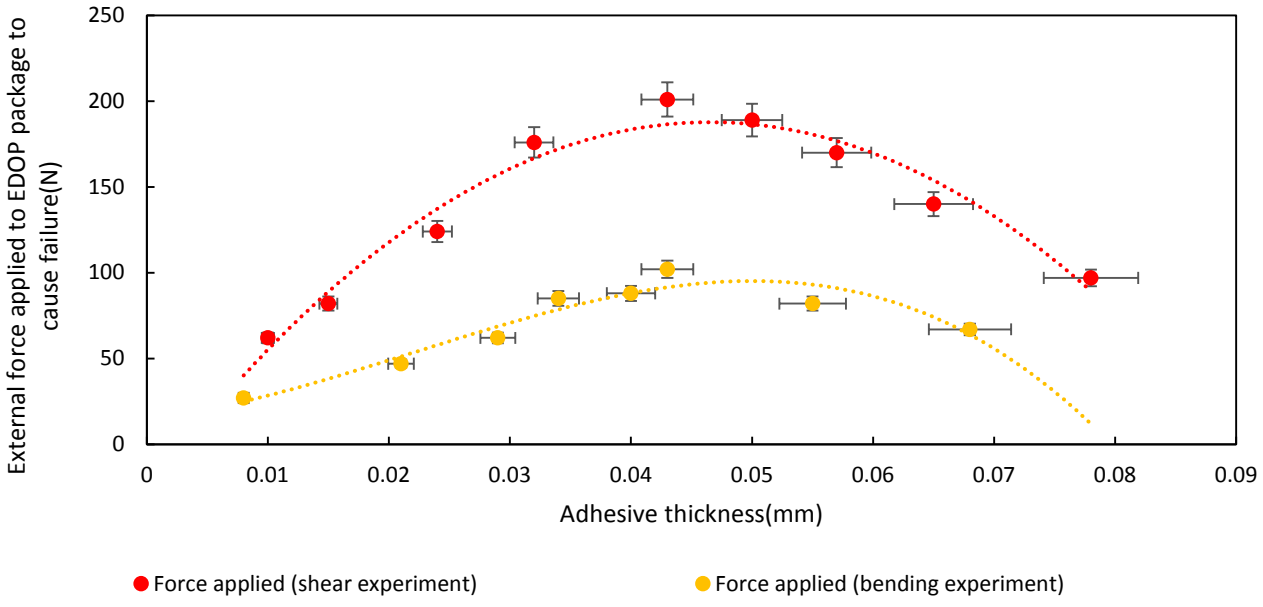


(b)

Figure 83. Comparison of results for EP37-3FLF, (a) simulated bending and shear stresses versus adhesive thickness (20 N force) (b) external force required to cause failure versus adhesive thickness (plotted line as eye-guide).



(a)



(b)

Figure 84. Comparison of results for Epo-Tek 301 2fl, (a) simulated bending and shear stresses versus adhesive thickness (20 N force) (b) external force required to cause failure versus adhesive thickness (plotted line as eye-guide).

5.3.1 Summary

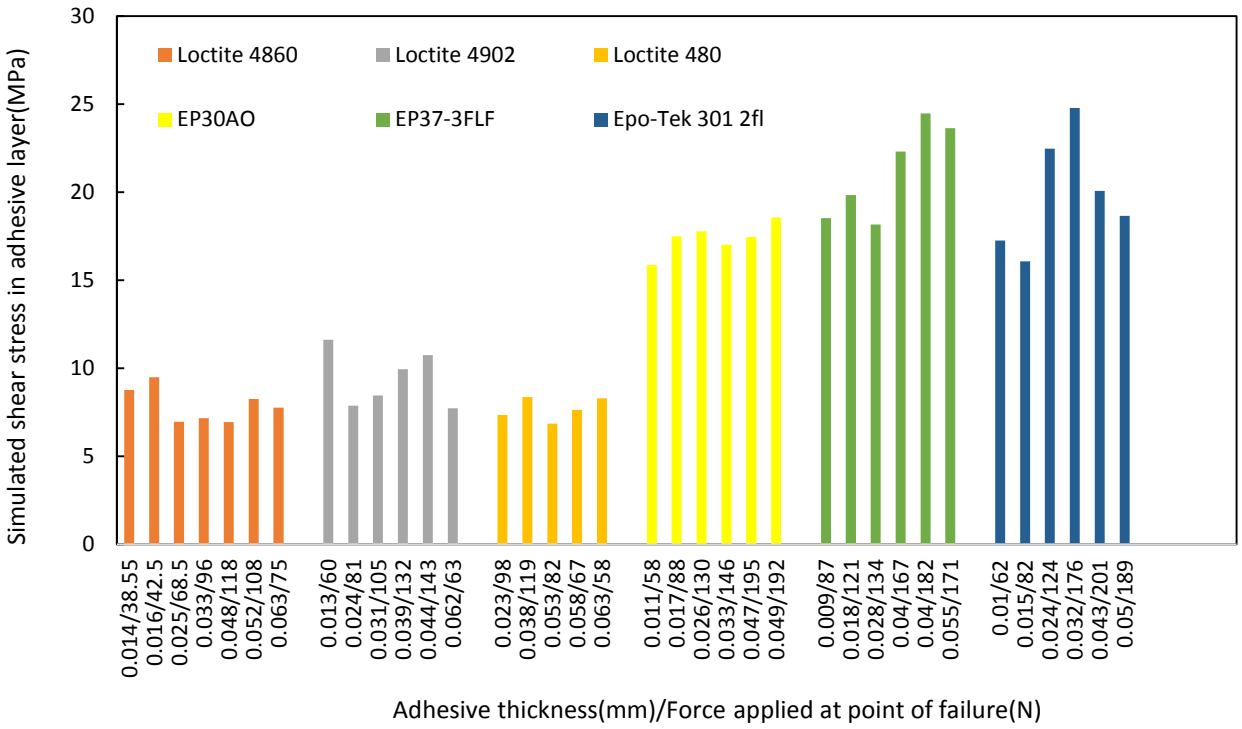
The simulation and experiment results for Loctite 4860, Loctite 480, Loctite 4902, EP30AO, EP37-3FLF and Epo-Tek 301 2fl adhesives were compared in this chapter. The comparison shows a very good correlation between the experimental and simulation results in both shear and bending cases for all materials and dimensions. While the optimal adhesive thickness in both sets of results closely correlates, the small error between simulation and experiment results from the frictional force in the track of electronic package holder and due in part to the tolerance in measuring the adhesive thickness.

5.4 Adhesive strength determined by simulation method

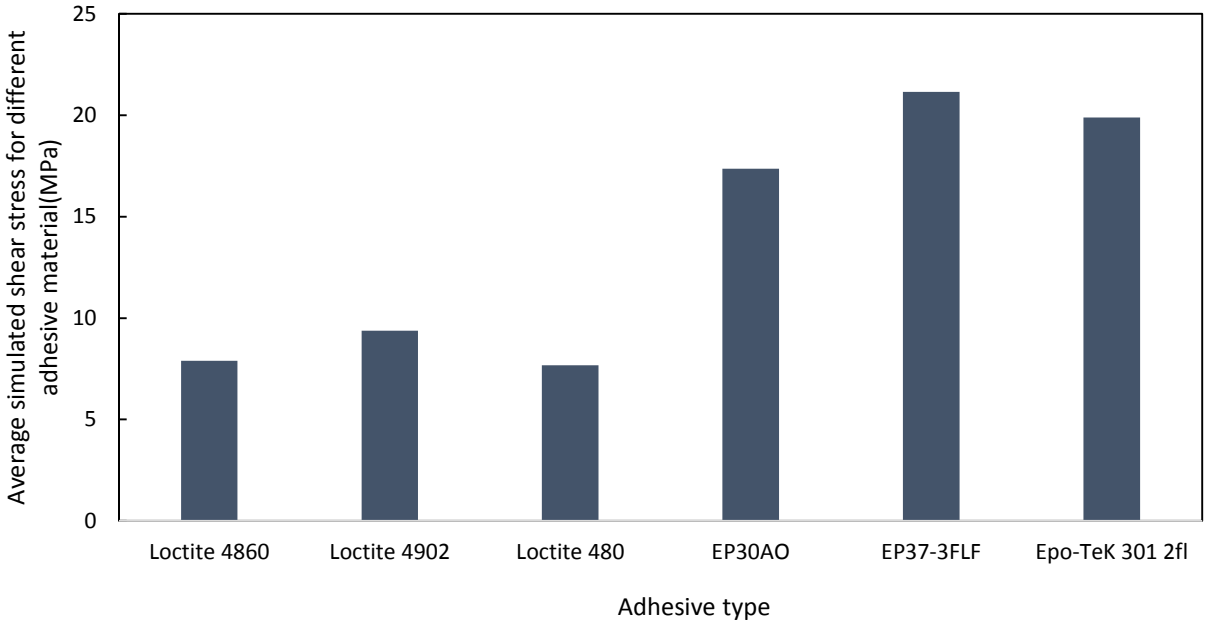
The magnitude of the experimental forces resulting in failure of the Loctite 480, Loctite 4860, Loctite 4902, EP30AO, EP37-3FLF and Epo-Tek 301 2fl adhesives during the shear test can be applied in the simulations to identify the practical shear strength of each adhesive. To do this, the failure force identified for each sample in the shear load experiment was applied in the simulation along with the adhesive thickness to determine the stress in the adhesive at the point each sample failed. The shear strength of the adhesive can be determined by averaging the simulated failure shear stresses from all the samples. The failure origin was found to be the corners of the die close to the location of the applied force. All shear stress values in the simulations are taken from the corners where the external the force was applied. The failure mode in both the shear and bending experiments indicated the adhesive failed at the chip/adhesive interface or within the adhesive itself.

Figure 85(a) shows how to use this approach to obtain the shear strength the 6 adhesives. For Loctite 4860, for example, the forces at which the package failed are 38.55 N, 42.5 N, 68.5 N, 96 N, 118 N, 108 N and 75 N for the adhesive at thicknesses of 14 µm, 16 µm, 25 µm, 33 µm, 48 µm, 52 µm and 63 µm respectively. The simulated shear strength in each instance is 8.75 MPa, 9.49 MPa, 6.96 MPa, 7.15 MPa, 6.93 MPa, 8.24 MPa and 7.75 MPa as shown in Figure 85(a). The average shear strength of Loctite 4860 is 7.89MPa.

This approach has been applied to all the adhesives and the average shear strength of each adhesive when bonding silicon to Kapton is shown in Figure 85(b). This simulated result shows that, of the six adhesives, the EP37-3FLF adhesive has the highest practical shear strength.



(a)



(b)

Figure 85. (a) Shear strength in different thickness of six adhesives in the simulation. (b) Shear strength comparison of the six adhesives.

5.5 Conclusions

This chapter experimentally investigated the influence of the adhesive thickness on the stresses in the electronic package. The shear and bending test experiment were performed on an electronic package using different adhesive materials (EP30AO, EP37-3FLF, Epo-Tek 301 2fl, Loctite 4902, Loctite 4860 and Loctite 480) and thicknesses. The 0.048 mm to 0.05 mm thick EP37-3FLF adhesive layer was identified as the optimum combination of adhesive material and thickness for the electronic package. The simulation results show a very good correlation with experimental results that gives a high level of confidence in this simulation approach. The method to determine the practical shear strength presented in section 5.4 is useful for determining the shear strength for any adhesive desired for electronic packaging of components on plastic substrates.

Chapter 6. Novel electronic packaging method for functional electronic textiles

A novel packaging method that enables the reliable mounting and protection of thin bare die within a textile yarn has been investigated. In order to maximize the reliability and to minimize stresses in the electronic package, the thin die should be located as close as possible to the neutral axis of the packaged assembly. The die is bonded to a bottom Kapton substrate which contains patterned conductive interconnects and bond pads forming the functional circuit. The circuit is protected by a moulded Kapton film that has recesses formed where the die is located. The novel method to package the electronic bare die in plastic (EDIP) is shown in Figure 86. This package includes six layers which are: top moulded Kapton cover, top adhesive, embedded silicon die, adhesive under-fill, conductive adhesive/ solder paste and Kapton substrate layer with conductive tracks. The conductive track can also be used to form long, very thin, flexible circuit as shown in Figure 1. Reliability, wash ability and flexibility are essential factors for a durable practical wearable e-textile [15]. The novel EDIP (also known as Type 4 in this Chapter) package described in this chapter aims to maximize the reliability, flexibility and the wash ability of the overall assembly compared with other three electronic packaging technologies. The three packaging technologies are:

- Type 1: mount die on the plastic substrate using conductive adhesive without under-fill (as shown in Figure 87),
- Type 2: mount die on the plastic substrate using conductive adhesive and under-fill (as shown in Figure 88),
- Type 3: mount die using conductive adhesive, under-fill and glop-top adhesive to cover die (as shown in Figure 89).

6.1 Electronic packaging method and materials

Figure 86(b) shows an idealized cross-section through the die in which has been completely encapsulated using a thin top Kapton layer. In order to minimize the stresses on the die and thereby increase reliability, it should be located as close as possible to the neutral axis of the overall assembly. The non-conductive adhesive is injected into the empty space between die and substrate to act as under-fill. Under-fill is used in standard electronic die packaging to increase the mechanical reliability of

electronic package by providing additional mechanical support, reduce thermal stresses caused by the difference in the coefficient of thermal expansion between the silicon die and the substrate and improve the ability to withstand mechanical shocks [144]. Flip chip packaging is the assembly method used in this chapter, which is a widely-used method of bonding an electronic die to a substrate or package carrier [145]. Conductive adhesives or solder bumps formed on the chip pads on the top side of the wafer are used to electrically connect the die to a substrate with the bumped die area placed facing downward [146]. The twisting, cyclical bending and washing test results of the EDIP packaging have been compared to type 1, 2 and 3 packaging assemblies which are shown schematically in Figure 87, 88 and 89.

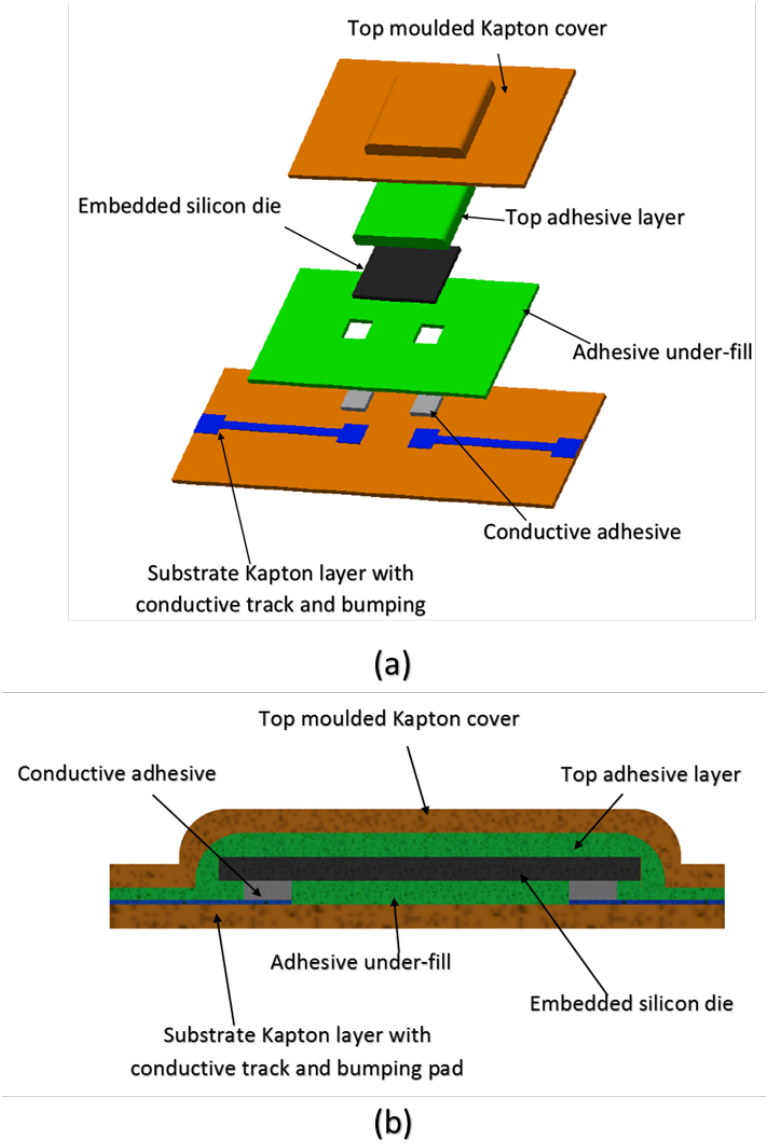


Figure 86. Schematic of novel packaging method, (a) six layers of EDIP package, (b) cross-section of EDIP package.

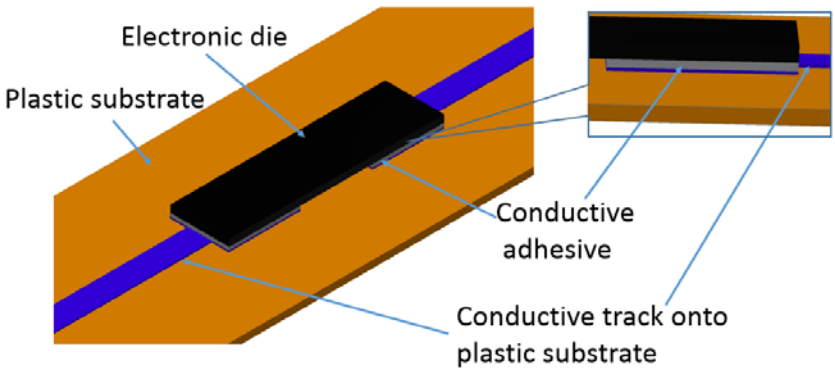


Figure 87. Type 1: Mount die on the plastic substrate using conductive adhesive without under-fill.

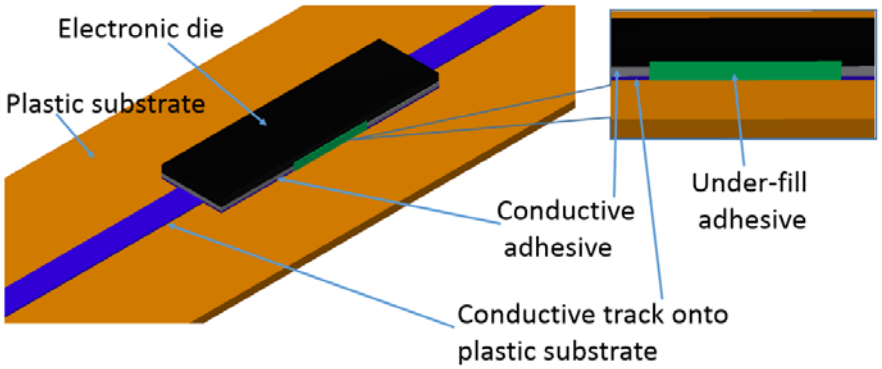


Figure 88. Type 2: Mount die on the plastic substrate using conductive adhesive and under-fill.

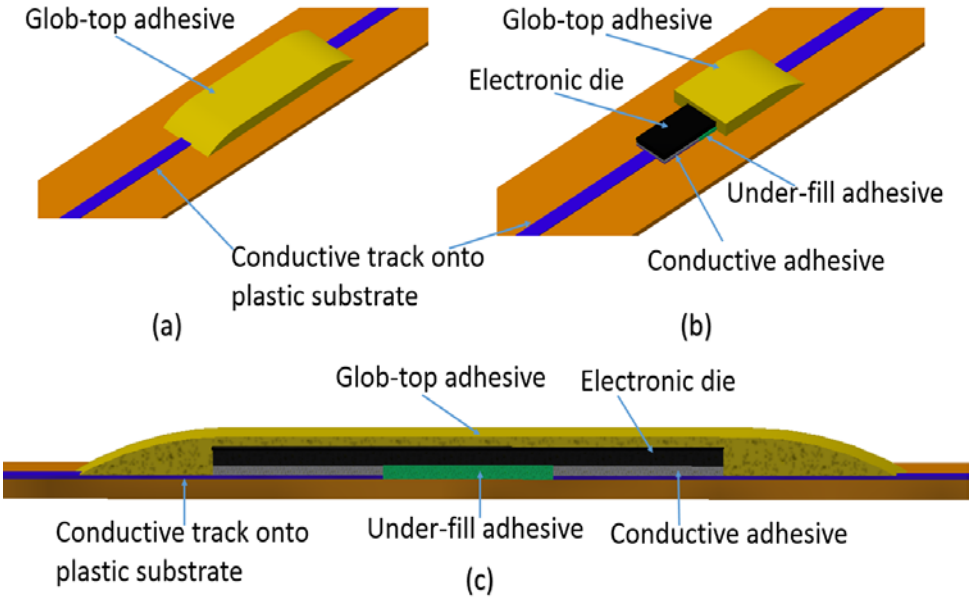


Figure 89. (a) Type 3: Mount die using conductive adhesive, under-fill and glop-top adhesive to cover die, (b) cut away the package to showing the embedded electronic die, (c) schematic cross section through type 3 package.

In the EDIP package (as shown in Figure 86), the top Kapton cover has the same thickness as the Kapton substrate and the thickness of the under-fill and top adhesive layer is identical to form a symmetrical assembly and locate the die on the neutral axis of the EDIP package. The steps to fabricate EDIP package are includes the following four steps:

1. Attached electronic die onto bottom Kapton layer by using conductive adhesive/ soldering paste.
2. Apply under-fill adhesive to space in between die and substrate.
3. Use dispenser to dispense a required thickness of adhesive into the groove of the deformed Kapton.
4. Attach die and bottom Kapton to deformed Kapton and use the syringe to dispense adhesive to empty space of groove.

The photograph of the EDIP packaged strip is shown in Figure 90(a) containing one electronic die. Figure 90(b) is a scanning electron microscope (SEM) photo of a cross-section of the assembly that clearly shows the layers of the EDIP package and the symmetrical configuration.

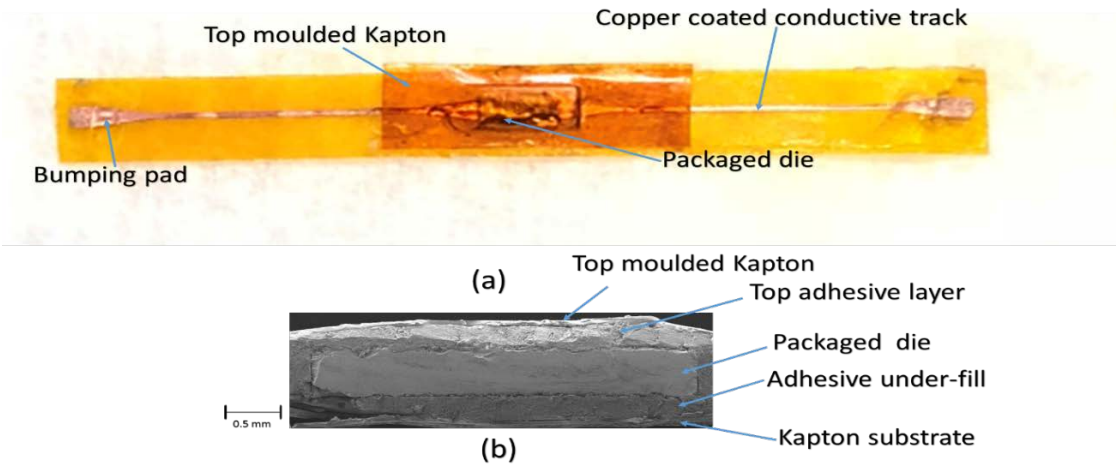


Figure 90. (a) Electronic strip with one packaged electronic die, (b) SEM photo in the cross section to show a sample of EDIP package (this sample used a 0.53 mm thickness of die).

Die sizes of 2 mm x 1 mm x 0.1 mm have been used for all experiments, there were mounted using silver conductive adhesive with a 50 g weight used to provide a constant pressure to the chip after placing the chip on the substrate. Stainless steel test chips were used in this investigate since they can be used to form a basic conductive test circuit for exploring durability, and 0.1 mm thickness of stainless steel chip is most common used thickness. The further investigation by using silicon chip will be discussed in chapter 7. A Kapton substrate of dimensions 80 mm x 3 mm x 0.05 mm was used for all four packaging methods. The EP37-3FLF under-fill adhesive was used in type 2, type 3 and EDIP

packages. The adhesive and substrate materials used have been previously identified as an optimum combination under shear and bending loads [147]. The properties of the under-fill adhesive, Kapton substrate, conductive adhesive and glob-top adhesive materials are given in Table 8.

Table 8. The properties of materials used for all packaging method.

Materials	Young's Modulus(MPa)	CTE (k^{-1})	Density (gcm^{-3})	Tensile Strength (MPa)
EP37-3FLF Under-fill adhesive	344	0.0009	1.05	35
Substrate (Kapton)	2500	0.00002	1.42	231
Conductive adhesive (RS1863616)	NA	NA	1.9	<6.9-13.7
Glob-top adhesive(EC-9519)	317	0.000069	0.96	<30

The conductive adhesive is a two part thermosetting material with an epoxy resin adhesive base which contains silver flakes. The manufacture's datasheet only gives the joint strength and density of the conductive adhesive.

6.1.1 Two types Kapton substrate with circuit

Kapton substrate with a patterned circuit is used for all four packaging methods in this chapter. Two types of metallisation were evaluated for the fabrication of the Kapton substrate containing the patterned test circuit used for all four packaging methods: (1), screen printed silver patterns on Kapton substrate and (2), copper coated circuit onto the Kapton substrate. Figure 91 shows the screen-printed silver polymer circuit, the DEK 248 screen printer is used to print 0.001 mm thickness of silver onto Kapton substrate. The bonding of electronic components onto printed inks using solders can be challenging due to the temperature of the soldering process, typically 150-350°C. In contrast, components can be attached routinely using conductive adhesives. As circuit complexity increases, the required feature size shrinks beyond the limits of standard screen printing (around 0.1 mm) [148], but this approach is fine as proof of concept.

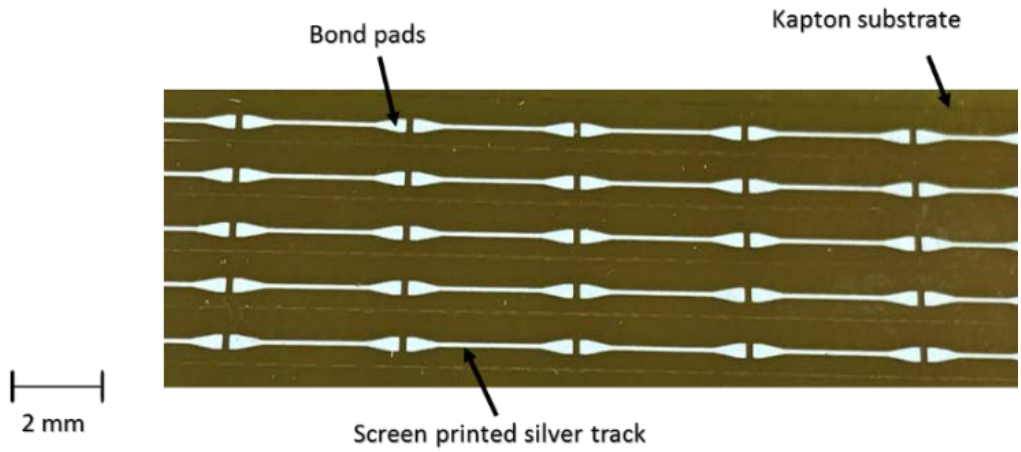


Figure 91. Screen printed silver polymer circuit onto Kapton substrate

Figure 92 shows the copper circuit substrate formed using commercial copper clad Kapton sheets [149]. The circuit was patterned using a wet copper etch and a resist masking layer. AZ9260 positive photoresist was spin coated for 30 seconds and oven baked for 3 minutes at 110 °C. An EVG 620T contact mask aligner was used to expose the resist and AZ400K developer with water in a 1:4 solution used for 7 minutes to remove the exposed resist. The PCB etch crystal solution (Sodium Peroxidsulfate) was used to remove the exposed copper forming the tracks shown in Figure 92. The fabrication processes for copper coated circuit onto the Kapton substrate as shown in Figure 93.

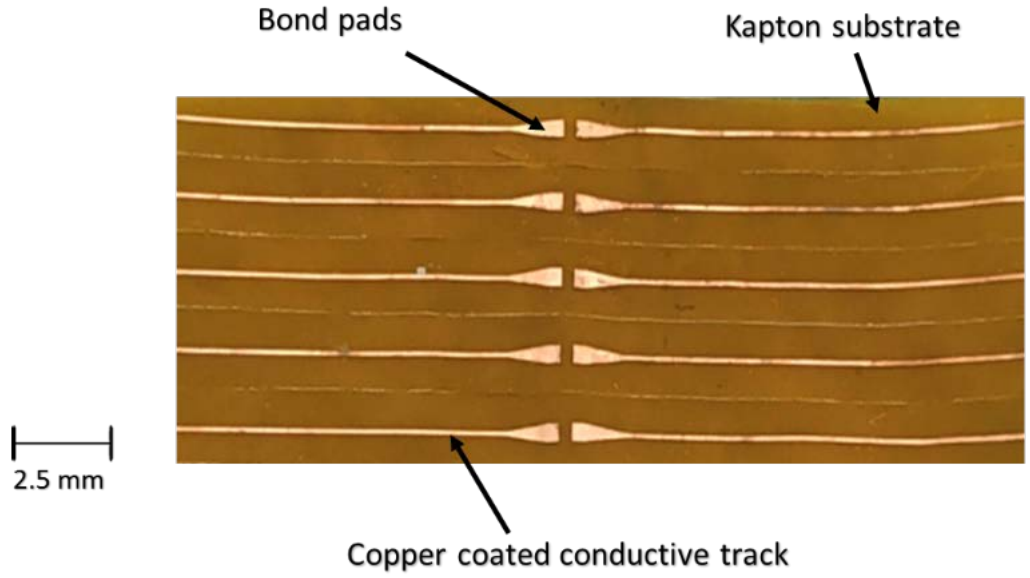


Figure 92. Copper coated circuit onto Kapton substrate.

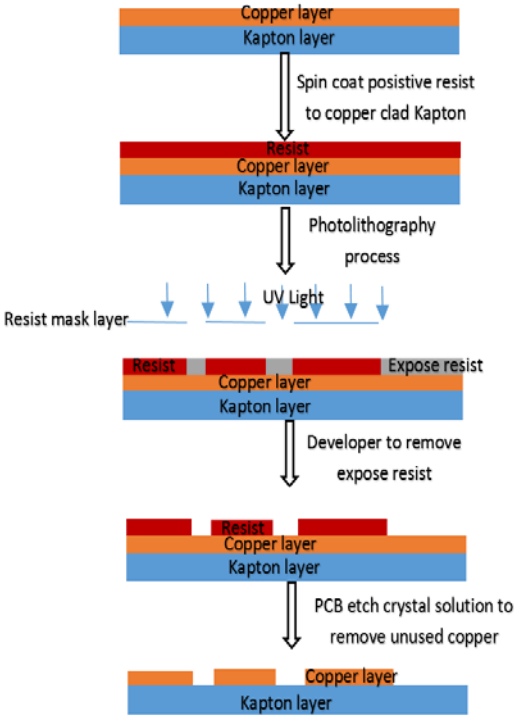


Figure 93. Fabrication process for copper coated circuit onto Kapton substrate.

The two types of Kapton circuit without chip were experimentally compared in a wash test. The circuit substrates were sewn on to a T-Shirt and placed in a standard household washing machine using a 41 minutes, 30 °C wash cycle including a spin dry at 900 rpm, this is standard wash cycle in commercial machine. The resistance of the screen printed silver polymer conductive track was found to significantly change from 2 Ω to 38 Ω after 20 wash cycles (the resistance of the silver ink itself was changed), whereas the copper tracks were unaffected. Copper coated Kapton circuits where therefore used throughout the remainder of this investigation.

6.1.2 Fabrication process for deformed Kapton cover

The EDIP packaging method aims to minimize stresses in the electronic package so the die needs to be encapsulated in a symmetrical assembly as shown in Figure 86(b). A moulding process has been used to form a recess in the top Kapton film into which the die is located. The Kapton PV9100 can be softened by heating it up and a series of experiment was performed to determine the minimum temperature and time to deform different thicknesses (0.025 mm, 0.05 mm, 0.075 mm and 0.125 mm) of Kapton. For this work, 0.05 mm thick Kapton was used to match the thickness of the substrate since a 0.05 mm thick Kapton substrate was previously identified as the optimal thickness under bending and shear test [147]. The moulding process for 0.05 mm thick Kapton requires a minimum temperature of 360 °C applied for

60 seconds, the Kapton thickness is not influenced by the moulding process. The oven will be used to heat up the jig and Kapton to 360 °C.

Figure 94(a) shows the jig used to deform the top Kapton film. The strip width was 7 mm and a round centre feature with a radius of 7 mm was initially included to avoid the effects of the Kapton shrinking and narrowing during the moulding process. At the centre of the circular feature is the rectangular recess with dimensions of 10.1 mm x 5.1 mm x 0.3 mm forming one half of the mould. The top part of the jig matches the bottom with a rectangular flange to fit in the recess in the bottom part of the jig with dimensions of 10 mm x 5 mm x 0.2 mm.

Figure 94(b) shows the cross-section of the jig assembly with a moulded Kapton strip. During initial tests, the circular part of the Kapton strip was compared before and after moulding to measure the degree of shrinkage. Figure 95(a) shows the circular feature of Kapton film has a diameter of 14.38 mm before moulding, and Figure 95(b) shows the circular feature of the moulded Kapton film has shrunk to 14.27 mm. This comparison indicates that there is only a small degree of shrinkage and this is not enough to be a concern. Therefore the circular feature was not included in later designs.

Different circuit designs will require a corresponding jig to match component location. Figure 96 shows a more complex jig used to deform Kapton to packaging an electronic circuit that contains multiple electronic chips. All jigs are designed by computer software Invertor and fabricated by University of Southampton Workshop.

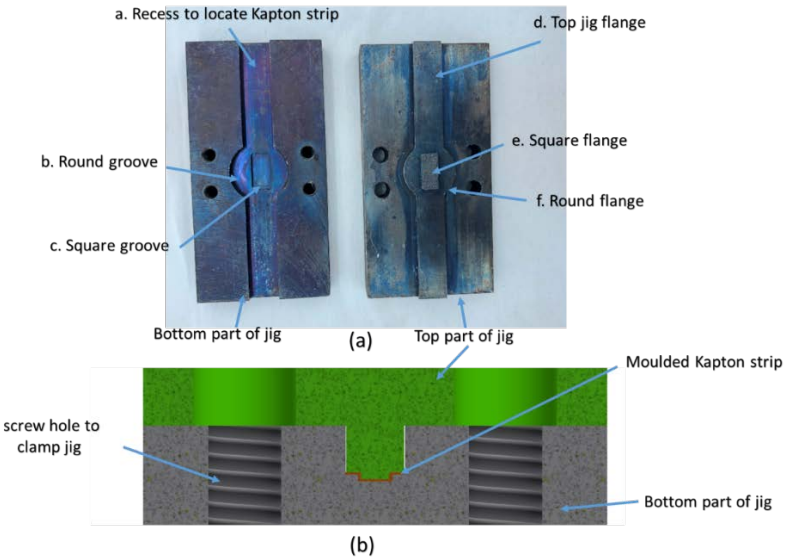


Figure 94. Jig used to deform top cover Kapton for packaging single chip, (b) schematic cross-section of two part jigs with a moulded Kapton strip.

Figure 95. The diameter of circular feature for a Kapton film (a) before moulding and (b) after moulding.

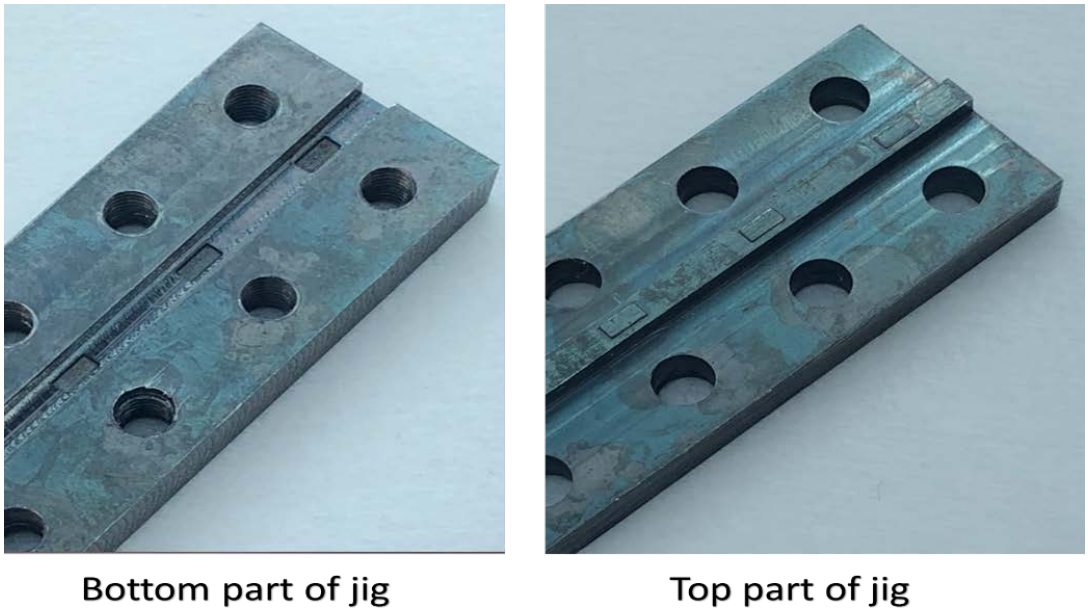


Figure 96. Jig used to deform Kapton for packaging multiple chips.

6.2 Experimental methods

The three test methods used were washing, twisting and cyclical bending to compare four different packaging method. For the wash test, the packaged circuits were attached to a woven textile using overstitching (or couching), as shown in Figure 97. Each Kapton strip only contained one test die for all samples. The test die formed a conductive path that bridges the gap in the test circuit. Any failure

in the package will alter the resistance along the length of the track. Joint failure will result in the circuit becoming open circuit entirely. All wash tests used a 41 minutes cycle at 30 °C including a 4 minute spin dry at 900 rpm. After each washing cycle, the tested sample was left to dry at room temperature.

The four packaging methods were also compared by a 180° cyclical twisting test to replicate the type of strain that could be experienced in use. Figure 98 shows the PROWHITE twist tester which provided 180° twisting at a controlled twisting speed. The twisting speed used was 9.09 cycles/sec. Two clamps were used to fix the circuit strip with the die being located 50 mm away from right twist clamp and the left clamp has weight of 200 g attached to the one end of the test strip to keep it in tension as shown in Figure 98. A copper wire was soldered to each end of the electronic strip to enable the resistance to be continuously monitoring during the test using a multimeter.

Figure 97. Packaged electronic strip knitted to the textile.

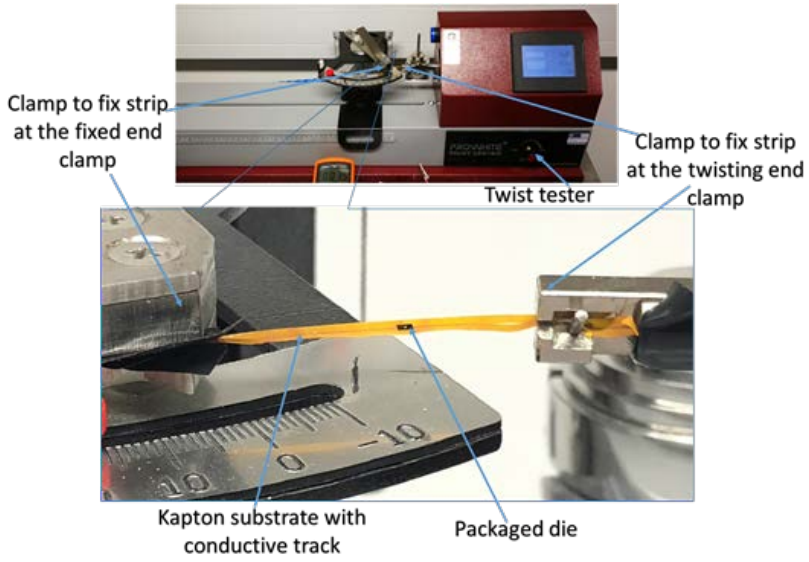


Figure 98. PROWHITE twist tester with two clamps to fix the electronic strips.

Cyclical bending was used to replicate bending forces commonly encountered in textile processes (e.g. knitting) and the bending test rig is shown in Figure 99. The electronic strip was clamped at the top end and during the test the clamp moves back and forth a distance of 30mm with a 200 g weight attached to the other end of the test strip to keep it in tension. The circuit passes around a roller of radius 3.5 mm. A multimeter was connected to the electronic strip in parallel to measure the resistance of the strip.

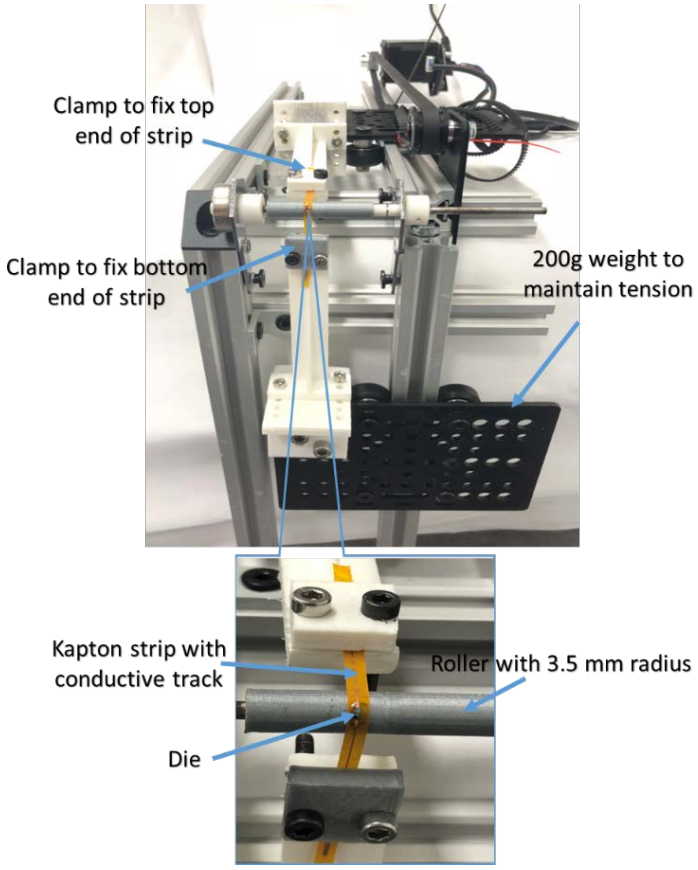


Figure 99. A bending test rig used for cyclical bending tester.

6.3 Experimental results

To identify the best wash ability, reliability and durability electronic packaging method, the four electronic packaging methods have been compared by wash test, twist test and cyclical bend test. The electrical resistance of each test sample will be measured to compare the different packaging method. The various initial resistance measured from each test sample before test is due to variations in the amount of conductive adhesive and the thickness of the cured joints, the conductive adhesive is manual applied by using syringe, the amount of conductive adhesive can further controlled by using industrial equipment such as stencil.

6.3.1 Wash test results

Table 9 shows the washing test results for five type 1 samples. Before washing all the samples had resistances in the range of 2.3 Ω to 13.4 Ω. The resistance of the five samples increased by 5 to 25 times after the first wash cycle. Samples 1, 3, and 5 failed after the second wash cycle, and samples 2 and 3 failed after the third washing cycle. All samples fail in this chapter is defined as the conductive adhesive delaminates at one or both ends as shown in Figure 100.

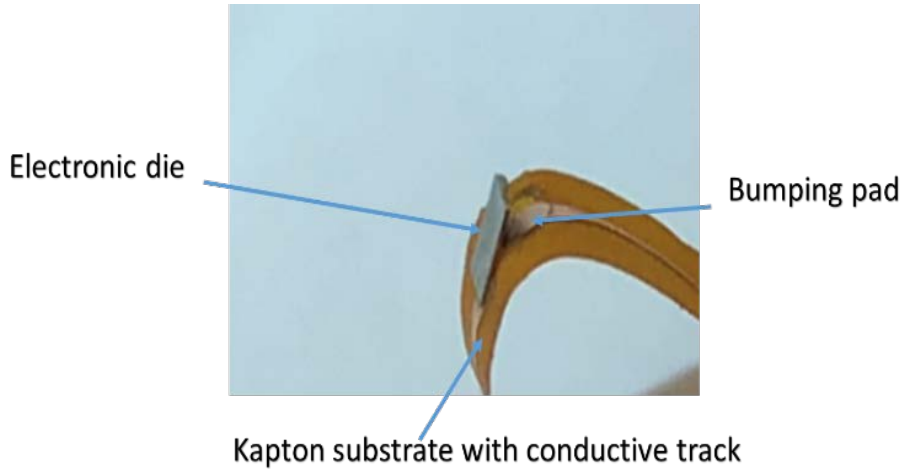


Figure 100. Conductive adhesive failure between the electronic die and the contact pad on Kapton.

Table 9. Washing test result for type 1 packaging method.

Sample	Resistance (R) before wash (Ω)	R after 1st wash cycle(Ω)	R after 2nd wash cycle(Ω)	R after 3rd wash cycle(Ω)
1	12.5	48	Fail[a]	
2	2.5	57	72	Fail[a]
3	13.4	136	Fail[a]	
4	4.8	154	168	Fail[b]
5	2.3	43	Fail[a]	

Fail[a] indicates a failure at one end only.

Fail[b] indicates a failure at both ends.

The washing test results for five type 2 samples are shown in Table 10. The type 2 samples had resistances in the range of 1.2 Ω to 5.7 Ω and these increased by 70% to 200% after the 1st wash cycle.

Sample 5 failed after the 3rd wash cycle, samples 1, 2 and 3 failed after the 4th washing cycle, whilst the resistance of sample 4 increased to 2600 Ω.

Table 11 shows washing test results for five type 3 samples that had resistances in the range of 1.0 Ω to 23 Ω. The resistance of the five samples increased by 20% to 50% after the 1st wash cycle, and increased by 3 to 60 times after the 5th wash cycle. All samples survived at least 18 washing cycles with sample 2 failing after the 19th wash cycle, sample 3 failed after the 24th wash cycles and sample 4 failed after the 27th wash cycles.

Table 10. Washing test result for type 2 packaging method.

Sample	Resistance (R) before wash(Ω)	R after 1st wash cycle(Ω)	R after 2nd wash cycle(Ω)	R after 3rd wash cycle(Ω)	R after 4th wash cycle(Ω)
1	1.2	3.5	225	614	Fail[a]
2	3.4	6.4	238	783	Fail[b]
3	3.3	6.9	195	642	Fail[a]
4	2.2	3.7	76	394	2600
5	5.7	7.5	1500	Fail[a]	

Fail[a] indicates a failure at one end only.

Fail[b] indicates a failure at both ends.

Table 11. Washing test result for type 3 packaging method.

Sample	R(Resistance) before wash(Ω)	R after 1st wash cycle(Ω)	R after 5th wash cycle(Ω)	R after 10th wash cycle(Ω)	R after 15th wash cycle(Ω)	R after 20th wash cycle(Ω)	R after 25th wash cycle(Ω)	R after 27th wash cycle(Ω)
1	23	26.5	86	268	2300	Fail[a] after 18th cycles		
2	2.7	3.2	37	68	1310	Fail[a] after 19th cycles		
3	21	23	73	263	1530	2610	Fail[b] after 24th cycles	
4	1.0	1.5	62	79	522	638	4150	Fail[a] after 27th cycles
5	13	18	114	365	3200	Fail[b] after 18th cycles		

Fail[a] indicates a failure at one end only.

Fail[b] indicates a failure at both ends.

The washing test results for five EDIP package samples are shown in Table 12. These samples had resistances in the range of 1.0 Ω to 28.6 Ω, which increased by 10% to 30% after the 1st wash cycle. The resistance of five samples increased by 2 to 16 times by the 5th wash cycle. All samples survived at least 39 wash cycles, with sample 5 failing after the 41st cycle. Sample 3 failed after the 42nd and sample 4 failed after the 44th wash cycles. Sample 2 has the longest life and survived 45 wash cycles. Compared with the type 1, 2 and 3 packages, the EDIP performed the best in the washing test.

Table 12. Washing test result for EDIP packaging method.

Sample	R (Resistance) before wash(Ω)	R after 1st wash cycle (Ω)	R after 5th wash cycle (Ω)	R after 10th wash cycle (Ω)	R after 15th wash cycle (Ω)	R after 20th wash cycle (Ω)	R after 25th wash cycle (Ω)	R after 30th wash cycle (Ω)	R after 35th wash cycle (Ω)	R after 40th wash cycle(Ω)	R after 50th wash cycle(Ω)
1	28.6	32.1	46	134	175	221	276	321	432	Fail[a] after 39th cycle	
2	1.0	1.3	17	23	31	37	49	83	103	853	Fail[b] after 46th cycle
3	2.7	2.8	26	30	38	47.3	65	105	168	1690	Fail[b] after 42nd cycle
4	1.6	2.2	23	45	53.4	63	78.5	98	143	1235	Fail[a] after 44th cycle
5	14.7	18.6	34	82	128	145	178.5	196	245	4200	Fail[a] after 41st cycle

Fail[a] indicates a failure at one end only.

Fail[b] indicates a failure at both ends.

6.3.2 Twist test result

Five samples for each package type were twist tested. Table 13 shows the twist test results for the type 1 and 2 samples. The resistance of the five type 1 samples increased by 15% to 80% after 100 twisting cycles and further increased by a factor of 8 to 32 times after 1,000 twisting cycles. All type 1 samples

electrically fail after 5,000 twisting cycles. These samples failed because the electrical connection at the twisting end breaks. The resistance of the five type 2 samples increased by 8% to 20% after 100 twisting cycles, and further increased by 50% to 150% after 1,000 twisting cycles. All samples failed after 35,000 twisting cycles.

Table 13. Twisting test result for type 1 and 2 packaging method.

Sample	R(resistance) before test (Ω)	R after 100 cycles (Ω)	R after 1000 cycles (Ω)	R after 5000 cycles (Ω)	R after 10000 cycles (Ω)	R after 15000 cycles (Ω)	R after 20000 cycles (Ω)	R after 30000 cycles (Ω)	R after 35000 cycles (Ω)
1 (Type 1)	8.1	10.2	63.2	Fail[a]					
2 (Type 1)	6.3	7.4	58.4	Fail[a]					
3 (Type 1)	1.5	1.8	33	Fail[a]					
4 (Type 1)	3.1	5.4	36.8	Fail[a]					
5 (Type 1)	10.5	13.6	89.2	Fail[a]					
1 (Type 2)	1.5	1.6	2.3	40.2	83	138	206	516	Fail[a]
2 (Type 2)	10	11.7	14.2	68.3	109	164.9	365	735	Fail[a]
3 (Type 2)	2.0	2.1	3.0	52	102	153.3	268	415	6300
4 (Type 2)	1.2	1.6	2.6	46.3	96.5	142.1	232	643	Fail[a]
5 (Type 2)	4.2	4.8	6.9	63.2	112.7	187.5	394	982	Fail[a]

Fail[a] indicates a failure at one end only.

Table 14 shows the twisting test results for the type 3 and EDIP packages. The resistance of the five type 3 samples increase by 10% to 25% after 1,000 twisting cycles, and further increase by a factor of 15 to 20 times after 150,000 twisting cycles. All EDIP package samples have small resistance change (< 5%) after 1,000 twisting cycles. The EDIP samples all survived 200,000 twisting cycles and the resistance only increased by a maximum factor of 10. The EDIP package exhibits the least change in resistance during the twist test indicating the conductive adhesive joints are well protected against twisting stresses.

Table 14. Twisting test result for type 3 and EDIP packaging method.

Sample	R(resistance) before test (Ω)	R after 1000 cycles (Ω)	R after 10000 cycles (Ω)	R after 30000 cycles (Ω)	R after 50000 cycles (Ω)	R after 70000 cycles (Ω)	R after 100000 cycles (Ω)	R after 150000 cycles (Ω)
1 (Type 3)	4.6	5.1	20	38	46	59	68	97
2 (Type 3)	4.0	4.3	16	37	43	56	64	84
3 (Type 3)	6.9	7.8	26	42	57	73	85	103
4 (Type 3)	9.7	11.5	32	53	61	82	96	112
5 (Type 3)	12.6	15.8	39	64	76	97	107	131
1 (EDIP)	4.9	5.1	6.8	15.4	26	32	36	42
2 (EDIP)	3.4	3.5	4.6	13.8	24.5	28.9	32	37
3 (EDIP)	2.5	2.6	3.2	12.9	20.6	26	29	33
4 (EDIP)	7.6	7.8	8.7	20	31	40	49	58
5 (EDIP)	13.1	13.3	14.8	23	36	44	51	74

6.3.3 Cyclical bending test result

Cyclical bending tests were also undertaken on five samples from each of the four package types. Table 15 shows the cyclical bending test results for the type 1 and 2 package. Initial resistances in the range of 3.7 Ω to 9.2 Ω for the type 1 samples, increased by 4 to 8 times after 10 bending cycles, and further increased by 40% to 100% after 20 bending cycles. All samples failed after 40 bending cycles. The resistance of the five type 2 samples increased by 80% to 220% after 10 bending cycles, and further increased by 20% to 90% after 20 bending cycles. Samples 4 and 5 failed after the 66^{th} and 69^{th} bending cycle respectively and all failed by the 74^{th} bending cycle.

Table 15. Cyclical bending test results for type 1 and 2 packaging method.

Sample	R(resistance) before test (Ω)	R after 10th cycle(Ω)	R after 20th cycle(Ω)	R after 30th cycle(Ω)	R after 40th cycle(Ω)	R after 50th cycle(Ω)	R after 60th cycle(Ω)	R after 70th cycle(Ω)	R after 75th cycle(Ω)
1 (Type 1)	3.7	36	58.2	99	Fail[a] after 33th cycle				
2 (Type 1)	8.6	42.5	63	114	Fail[a] after 31th cycle				
3 (Type 1)	9.2	53	75.5	Fail[a] after 30th cycle					
4 (Type 1)	6.8	24.8	49	86.3	Fail[a] after 37th cycle				
5 (Type 1)	8.9	39	56	108	Fail[b] after 35th cycle				
1 (Type 2)	10.7	18.5	24.3	29.4	42.5	57.3	97.2	143	Fail[a] after 74th cycle
2 (Type 2)	4.2	14.1	21	28	35.4	43	84.1	136	Fail[a] after 72th cycle
3 (Type 2)	12.5	20.3	28.7	30.8	43.2	55.6	89	121	Fail[a] after 71th cycle
4 (Type 2)	8.2	17.6	23.9	31.4	49.8	58.7	107	Fail[b] after 66th cycle	
5 (Type 2)	14.3	29.6	36.8	42.3	53.1	64.8	123	Fail[a] after 69th cycle	

Fail[a] indicates a failure at one end only.

Fail[b] indicates a failure at both ends.

Table 16 shows the cyclical bending test results for the type 3 and EDIP package. The resistance of the type 3 samples increased by 10% to 40% after the 10th bending cycle, and further increased by 120% to 160% after the 100th bending cycle. The five samples survived an average of 908 bending cycles. The cyclical bending test results for EDIP package shows that the resistance of all samples are increased by 5% to 15% after the 10th bending cycle, and by 15% to 80% after the 100th bending cycle. Compared to the type 3 package, the resistance of the EDIP samples increases at a lower rate. The five samples

survived an average of 1386 bending cycles. The EDIP package offers the best performance in cyclical bending.

Table 16. Cyclical bending test results for type 3 and EDIP packaging method.

Sample	R(resistance) before test (Ω)	R after 10th cycle(Ω)	R after 100th cycle(Ω)	R after 500th cycle(Ω)	R after 1000th cycle(Ω)	R after 1300th cycle(Ω)	R after 1400th cycle(Ω)	R after 1500th cycle(Ω)
1 (Type 3)	6.8	7.5	18.6	92	Fail[a] at 812th cycle			
2 (Type 3)	3.1	4.3	10.6	59.8	Fail[a] at 913th cycle			
3 (Type 3)	2.7	3.6	9.1	53.2	Fail[b] at 981th cycle			
4 (Type 3)	5.2	6.1	15.7	74.1	Fail[a] at 886th cycle			
5 (Type 3)	4.3	5.7	13.5	68.3	Fail[a] at 946th cycle			
1 (EDIP)	1.7	1.8	4.9	23.8	64.3	97.5	Fail[a] at 1390th cycle	
2 (EDIP)	2.6	2.7	9.0	36	83.2	132	Fail[a] at 1348th cycle	
3 (EDIP)	1.6	1.8	3.6	27.1	68.6	102	Fail[a] at 1357th cycle	
4 (EDIP)	4.3	4.5	6.3	32.4	72.8	89.4	103	Fail[a] at 1470th cycle
5 (EDIP)	3.8	3.9	5.9	29.5	73.5	95.8	Fail[a] at 1364th cycle	

Fail[a] indicates a failure at one end only.

Fail[b] indicates a failure at both ends.

6.3.4 Summary

E-textiles in wearable applications are subject to human motion activities and as such the integrated electronic components can be vulnerable to different kinds of stresses such as bending and twisting. The

four packaging technologies for E-textiles have compared in this section using wash testing, twisting and cyclical bending. The type 1 packaging approach performed the worst washing, twisting and bending results, which because of the type 1 packages do not have the under-fill layer to provide additional mechanical support to increase the mechanical reliability, and also have no encapsulation layer to offer further protections to packaged die. Compared to the type 1 packaging method, the type 2 packaging method provide better washing, twisting and bending performance which indicated the under-fill material increased the reliability of the electronic package. The type 3 package method performed better than the type 1 and 2 package method in all tests which further proved the encapsulation layer offered protections to packaged die. The best package (EDIP) survived up to 45, 150,000 and 1470 cycles of wash test, 180° twist testing and 90° bending testing are respectively, the EDIP package method located the electronic die into the neutral axis of the overall package which minimized the stresses in the die layer during washing, twisting and bending.

6.4 Conclusions

A novel method (EDIP) for packaging electronics using a thermally deformed Kapton was introduced. The design process for the jig that was used to deform the Kapton and the minimum temperature and time needed to deform the Kapton has been investigated. The EDIP packaging method have been compared with the other three traditional packaging methods (type 1, 2 and 3) during washing, twisting and cyclical bending. The EDIP package shows the best performance in washing, twisting and bending. This new packaging method for the electronic die adds waterproof property and increased flexibility to the electronic package.

The failure of all EDIP samples in wash testing, twisting and cyclic bending caused by the failure of the conductive adhesive between die and substrate. The higher adhesion strength material (such as solder paste) used to provide electrical connections between die and substrate can improve the reliability of EDIP package to withstand washing, twisting and cyclical bending stresses.

Chapter 7. Ultra-thin chip fabrication and packaging for e-textiles

An ultra-thin silicon chip based fabrication method for electronic textiles (e-textiles) is investigated in this chapter; the target is to maximize the flexibility and reliability of the realised e-textiles. An SOI (Silicon on Insulator) wafer based process with different device layer thicknesses is used to achieve various thicknesses of the ultra-thin chip. As an example, a device thickness of ~25 μm is realised in four different silicon chip sizes (1 mm x 1 mm, 0.5 mm x 2 mm, 2 mm x 1 mm, 2 mm x 2 mm) using a 6 inch SOI wafer. Photolithography and lift-off technology are used for the metallization of the chip and Hydrogen Fluoride (HF) etching for thinning the device layer. The 2 mm x 1 mm sized chip is configured in four different packages and experimentally evaluated under washing, twisting and cyclical bending to assess reliability and flexibility.

7.1 Ultra-thin chip fabrication

A 6 inch of commercial SOI wafer (bought from UltraSil Corporation) with a 25 μm device layer, 2 μm buried oxide layer and 654 μm handle layer is used to fabricate the ultra-thin chips. As shown in chapter four, a 25 μm thickness of silicon die is the optimal die thickness for packaging into an electronic yarn so an SOI wafer with device layer of 25 μm is selected. The thickness of the buried oxide and handle layer do not affect the thickness of the ultra-thin chip. The four steps used to fabricate the ultra-thin chip are: deposit protective silicon nitride onto the device layer of the SOI wafer; pattern and metallize the silicon nitride layer to produce conductive tracks and pads on the ultra-thin chip; partially dice to achieve trenches at the chip edges down to the buried oxide layer; HF vapour etch the buried oxide layer to release the handle layer of the SOI wafer. So the total thickness of the ultra-thin chip is the sum of the device layer thickness, the silicon nitride layer thickness and the metallization thickness.

7.1.1 Silicon nitride deposition

Silicon dioxide, silicon nitride and aluminium oxide are the three most commonly used dielectric materials using in silicon wafer processes [150]. Silicon nitride is chosen in this thesis because of the extremely low HF etching rate compared with silicon dioxide and aluminium oxide [151, 152]. The silicon nitride layer is deposited onto the device layer of the SOI wafer to avoid short circuits between the metal conductive layer and the device layer of the SOI wafer and to avoid mechanical damage to the

device layer during etching and metallization. An Oxford Plasmalab 100 Plasma-enhanced chemical vapour deposition (PECVD) system shown in Figure 101(a) is used for a standard process to do silicon nitride deposition. A thickness of 100 nm of silicon nitride is deposited to protect the device layer of the SOI wafer.

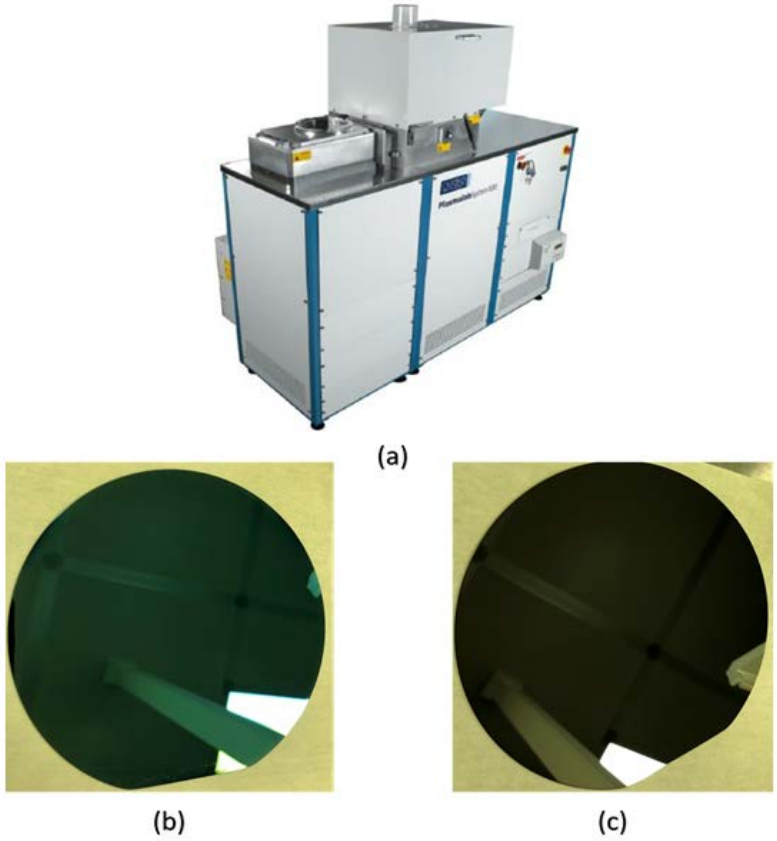


Figure 101. (a) Oxford Plasmalab 100 Plasma-enhanced chemical vapour deposition system (b) SOI wafer before silicon nitride deposition (c) SOI wafer after silicon nitride deposition.

Figure 101(b) shows the SOI wafer before silicon nitride deposition showing only the silicon device layer. After silicon nitride deposition the SOI wafer is darker as shown in Figure 101(c) because of the colour of the silicon nitride material.

7.1.2 Ultra-thin chip Metallization

Metallization, based on lift-off technology, is undertaken to fabricate conductive tracks and pads onto the ultra-thin chip and the metallization processes flowchart is shown in Figure 102. There are four main steps: deposit an AZ 2070 resist onto the SOI wafer device layer; photolithographically expose the photoresist and use developer AZ 400K liquid to remove the unwanted resist; metallise and remove

resist using N-Methyl-2-pyrrolidone (NMP) leaving the metal tracks and pads on the device layer where required.

In the process of metal deposition, the 50 nm chromium is first deposited onto the SOI wafer, 300 nm of gold is then deposited onto the chrome layer by using E-Beam metal evaporator. The adhesion of chromium to silicon nitride is much higher than gold to silicon nitride [153, 154], and the gold has very good adhesion to chromium. So to improve adhesion between the metal layers and the SOI wafer, chromium is used before gold deposition, this is also a commonly used method used to improve adhesion between gold to Si wafer.

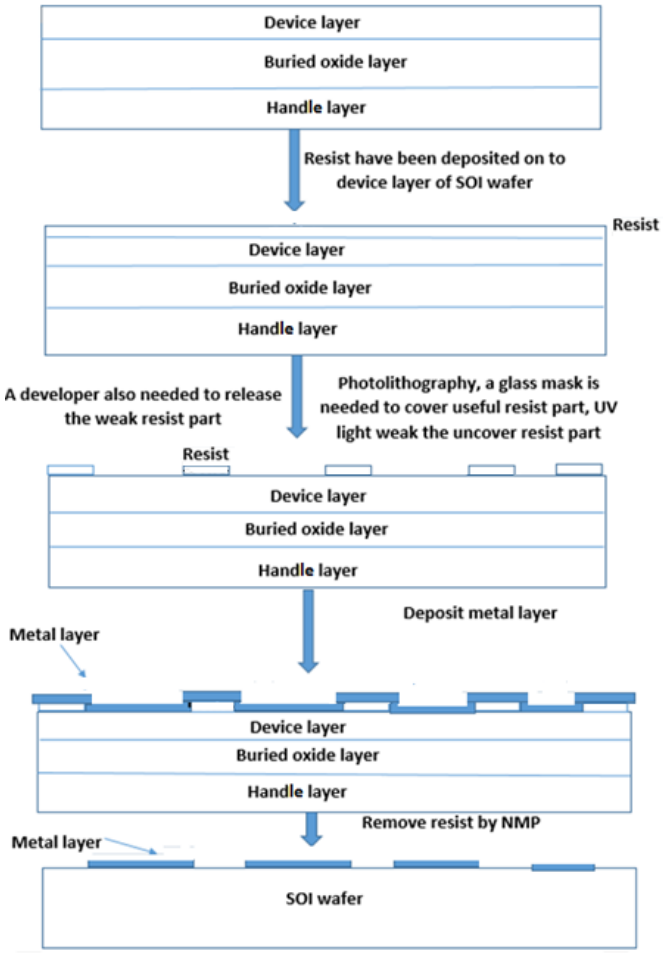


Figure 102. Metallization processes flow chart for ultra-thin chip fabrication.

The SOI wafer with gold metallization layer is shown in Figure 103(a), the combined thickness of the gold and chromium metal layers is 350 nm. Figure 103(b) shows the SOI wafer after the lift-off of the unwanted metal layer.

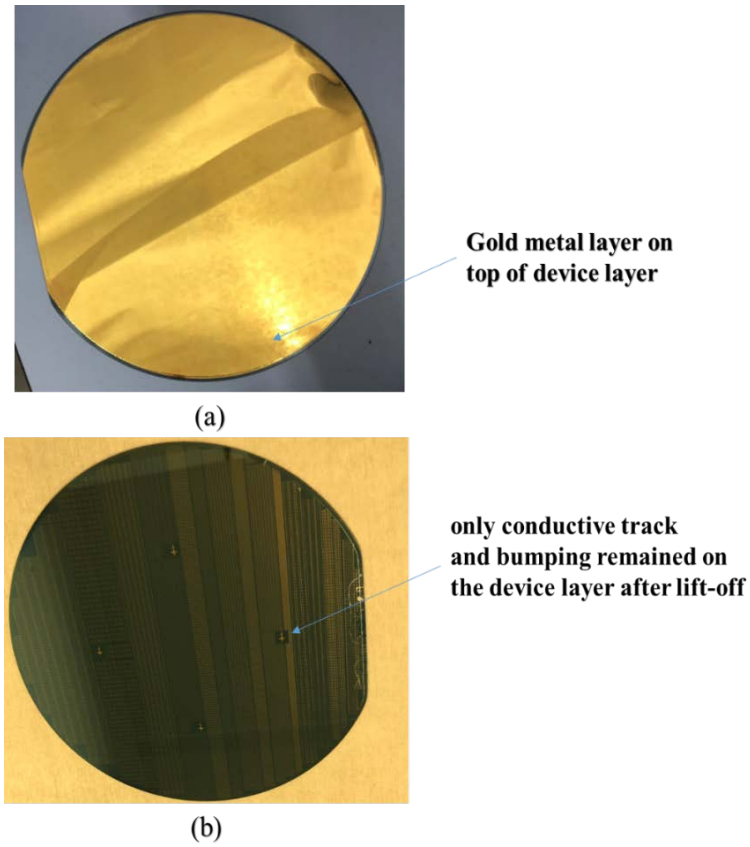


Figure 103. SOI wafer with the metal layer, (a) before lift-off of the metal layer on top of the device layer, (b) Only the conductive tracks and pads are left on the wafer after lift-off.

7.1.3 Achievement of Trenches in the SOI wafer down to the buried oxide layer

In order to achieve trenches at the chip edges down to the buried oxide layer of the SOI wafer before HF vapour etching, a DAD 320 dicing saw shown Figure 104(a) is used to cut through the device layer of the SOI wafer. To expose the buried oxide layer, a 30 µm depth cut is used to pass through the 25 µm device layer. Figure 104(b) shows the pattern of the chips and this cutting step subsequently allows easy separation into single ultra-thin chips after HF etching.

The AZ 2070 resist is also applied to the device layer of the SOI wafer to protect the metal layer during dicing; it also protects the metal layer and silicon nitride during the HF etching process. Figure 105 shows the SOI after dicing with the 30 µm deep chip trenches.

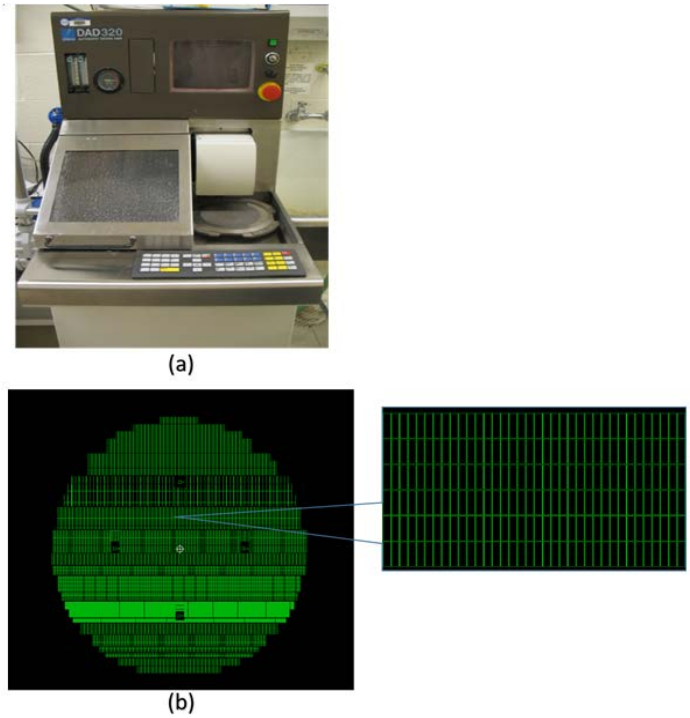


Figure 104. (a) DAD 320 dicing saw, (b) pattern of signal chips.

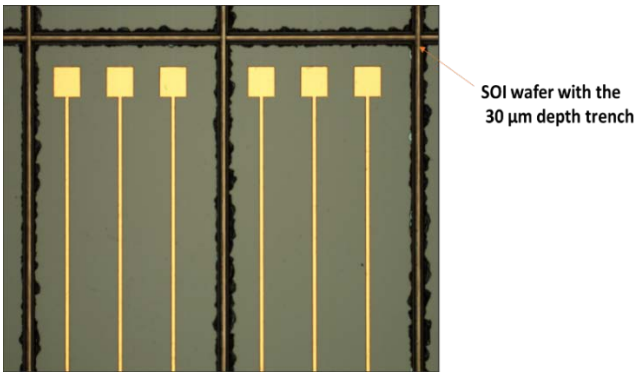


Figure 105. SOI wafer with the 30 µm depth trenches before HF etching.

7.1.4 HF etching to release the SOI wafer handle layer

The buried oxide of the SOI wafer was etched by 49% HF (49% Hydrofluoric Acid: 51% Water). The SOI wafer is immersed in HF vapour at 80 °C and it takes about two hours to fully etch the buried oxide layer. To subsequently remove the AZ 2070 resist, N-Methyl-2-pyrrolidone (NMP) is used at 60 °C [155] in an ultrasonic cleaner for 10 minutes. Figure 106 shows the fabricated ultra-thin silicon chips of thickness ~25 µm and the conductive tracks and pads, in four different widths/lengths.

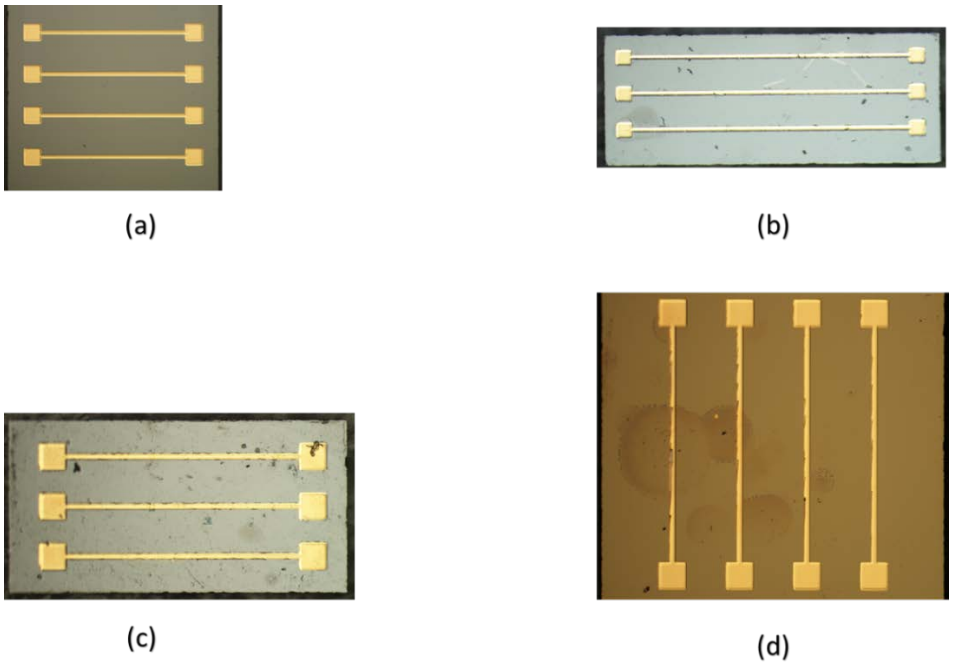


Figure 106. 25 µm thick ultra-thin chips with conductive tracks and pads. The width and length of the chips are: (a) 1 mm x 1 mm, (b) 0.5 mm x 2 mm, (c) 2 mm x 1 mm and (d) 2 mm x 2 mm.

7.2 Ultra-thin chip electrical conductivity test

Electrical conductivity tests of the silicon chips were undertaken using a DC probe station with an Agilent 4155c semiconductor parameter analyser. Figure 107(a) shows the DC probe station and the two probes attached to the two pads at the end of the conductive track. A maximum 0.8 V voltage is applied to the two probes to form a circuit as shown Figure 107(b), and the Agilent 4155c, as shown in Figure 107(c), is used to plot voltage against the current for each track. Figure 107(d) shows an example test result: 0.072 V voltage provide 9.23 mA, 0.36 V voltage provide 46.15 mA and 0.788 V voltage provide 101 mA, so the resistance of the track on silicon chip is 7.8 Ω and electrically conductive.

The electrical conductivity has also been tested by mounting the chip on a Kapton substrate containing a copper track. Figure 108(a) shows the Kapton conductive track pattern; the size of the Kapton substrate pads are the same as those on the chip. Alignment marks in each pad area of the Kapton substrate are used to aid mounting. A multimeter is used to measure the resistance of the Kapton substrate with the mounted chip. 12.9 Ω resistance was measured as shown Figure 108(b); the difference of 5.1 Ω between the resistances measured by the DC probe station is because of the additional resistance of the copper track (usually 2 Ω) and the resistance of the conductive adhesive used to provide electrical connection between the chip and the substrate.

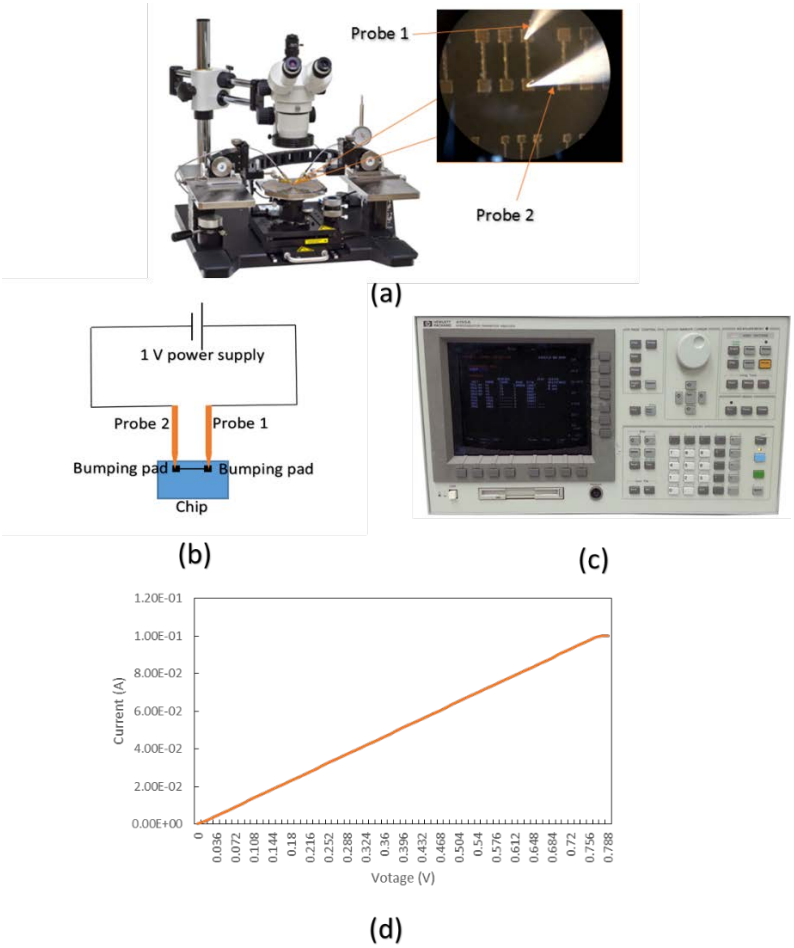


Figure 107. Ultra-thin chip conductivity test equipment and results, (a) DC probe station, (b) electronic circuit for conductivity testing, (c) Agilent 4155c used to plot the voltage against current graph, (d) voltage against the current plot.

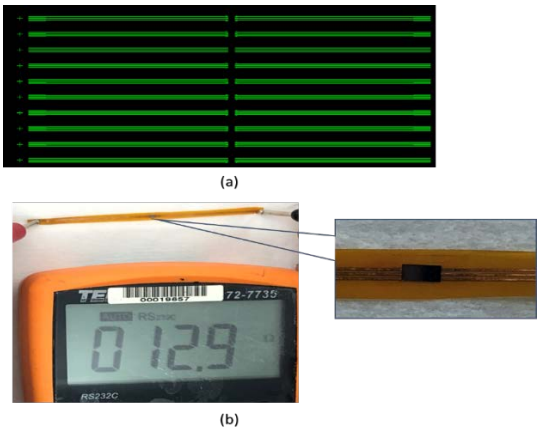


Figure 108. Chip electrical conductivity test, (a) CAD layout of Kapton substrate with the copper track, (b) the resistance of the Kapton substrate with the chip mounted, measured by multimeter.

7.3 Experimental test of the packaged Ultra-thin chip

The ultra-thin chips were packaged using four different packaging technologies before washing, twisting and cyclical bending testing to identify the optimal packaging method for the ultra-thin chip. The four

packaging technologies are type 1, type 2, type 3 and EDIP that have already introduced in chapter six. The 0.125 mm thickness of flange in the mould has been used to deform Kapton in this chapter snice the thickness of chip used in this chapter is much smaller than chapter six.

The plastic substrate with conductive tracks, as shown in Figure 108(b), is used for all four packaging technologies. Five samples of each packaging method are used for the twisting, cyclical bending and wash tests. The twisting, cyclical bending and wash experiment method and conditions used in this chapter are the same as described in section 6.2. The various initial resistance measured from each test sample before test is due to variations in the amount of conductive adhesive and the thickness of the cured joints, the conductive adhesive is manual applied by using syringe.

7.3.1 Wash test results

The four packaging methods were compared in terms of wash resistance. Table 17 shows the wash test results for the five type 1 packaged samples. Before washing all the samples had resistances in the range of 18 Ω to 31 Ω. All five type 1 samples failed after the 1st wash cycle. Table 18 shows the wash test results for the five type 2 packaged samples. Before washing all the samples had a resistance in the range of 18 Ω to 34 Ω. The resistance of the five samples increased by 300% to 500% after the 1st wash cycle. Samples 1, 2 and 5 failed after the 2nd wash cycle, and samples 3 and 4 failed after the 3rd wash cycle. All samples in the test failed because of the ultra-thin silicon chip broken.

Table 17. Wash test results for type 1 package

Sample	Resistance (R) before wash (Ω)	R after 1st wash cycle(Ω)
1	18	fail
2	25	fail
3	23	fail
4	31	fail
5	27	fail

Table 18. Wash test results for type 2 package

Sample	Resistance (R) before wash(Ω)	R after 1st wash cycle(Ω)	R after 2nd wash cycle(Ω)	R after 3rd wash cycle(Ω)
1	22	127	fail	
2	34	189	fail	
3	18	86	195	fail
4	25	143	324	fail
5	32	162	fail	

Table 19 shows the wash test results for the five type 3 packaged samples. Before washing all the samples had resistances in the range of 19 Ω to 31 Ω. The resistance of the five samples increased by 20% to 30% after the 1st wash cycle. The resistance of the five samples increased by 60% to 90% after the 5th wash cycle. Samples 5, 3 and 1 failed after the 12th, 14th and 15th and wash cycle respectively. Samples 4 and 2 failed after the 16th and 18th wash cycle respectively. Compared with the type 1 and 2 packages, the type 3 package higher resistance to washing.

Table 20 shows the wash test results for the five EDIP packaged samples. Before washing all the samples had resistances in the range of 19 Ω to 34 Ω. The resistance of the five samples increased by 10% to 20% after the 1st wash cycle. The resistance of the five samples increased by 40% to 50% after the 5th wash cycle. Sample 1 and 4 failed after the 23rd and 22nd wash cycle respectively. Sample 2 and 5 are failed after the 25th wash cycle, and sample 3 failed after the 26th wash cycle. Compared with the type 1, 2 and 3 packages, the EDIP package performed the best in the wash test.

The best EDIP with 0.025 mm silicon die survived 25 wash cycles, all EDIP package sample failed because of the silicon chip broken. The wash test in chapter six shows that the EDIP package with 0.1 mm metal chip survived 45 wash cycles without chip itself broken (all samples failed because of conductive adhesive fail). Compare this to wash test result which proves that the metal chip has better strength than silicon chip.

Table 19. Wash test result for type 3 package

Sample	Resistance(R) before wash(Ω)	R after 1st wash cycle(Ω)	R after 5th wash cycle(Ω)	R after 10th wash cycle(Ω)	R after 15th wash cycle(Ω)	R after 20th wash cycle(Ω)
1	28	32	46	152	fail at 14th cycle	
2	25	29	42	104	196	fail at 18th cycle
3	27	34	51	148	fail at 15th cycle	
4	19	26	35	81	143	fail at 16th cycle
5	31	35	59	162	fail at 12th cycle	

Table 20. Wash test results for EDIP package

Sample	R (Resistance) before wash(Ω)	R after 1st wash cycle(Ω)	R after 5th wash cycle(Ω)	R after 10th wash cycle(Ω)	R after 15th wash cycle(Ω)	R after 20th wash cycle(Ω)	R after 25th wash cycle(Ω)	R after 30th wash cycle(Ω)
1	26	30	37	52	93	148	fail at 23rd cycle	
2	19	21	28	48	87	134	fail at 25rd cycle	
3	27	32	40	43	72	127	182	fail at 26th cycle
4	34	38	48	71	123	206	fail at 22nd cycle	
5	30	34	44	62	115	171	fail at 25rd cycle	

7.3.2 Twist test results

Twisting tests the mechanical strength of the four different packaging technologies. Table 21 shows the results for the type 1 package. Before twisting, the resistance of the five samples were in the range of 17 Ω to 28 Ω. The resistance of the five samples increased by 10% to 25% after 1,000 twisting cycles. The resistance of the five samples increased by 35% to 50% after 5,000 twisting cycles. The resistance of the five samples increased by 85% to 100% after 10,000 twisting cycles. The resistance of the five samples increased by 7-10 times after 30,000 twisting cycles. Sample 1, 2 and 5 failed after 40,000 twisting cycles, and also the resistance of sample 3 and 4 increased to 468 Ω and 789 Ω respectively. Table 22

shows the twist test results for the type 2 package. Before twisting, the resistance of all five samples were in the range of 19 Ω to 32 Ω. The resistance of the five samples increased by 5% to 15% after 1,000 twisting cycles. The resistance of the five samples are increased by 20% to 30% after 5,000 twisting cycles. The resistance of the five samples increased by 40% to 55% after 10,000 twisting cycles. The five type 2 samples all survived after 70,000 twisting cycles, however, sample 1 and 2 failed after 90,000 twisting cycles. Compared to the type 1 packages the type 2 packages achieve better performance as a result of the under-fill.

Table 21. Twist test results for type 1 package

Sample	R (resistance) before test (Ω)	R after 1000 cycles (Ω)	R after 5000 cycles (Ω)	R after 10000 cycles (Ω)	R after 20000 cycles (Ω)	R after 30000 cycles (Ω)	R after 40000 cycles (Ω)
1	19	21	25	38	43	146	fail
2	23	28	32	42	51	163	fail
3	17	21	26	32	41	172	468
4	20	23	29	37	42	126	789
5	28	32	47	53	62	268	fail

Table 22. Twist test results for type 2 package

Sample	R (resistance) before test (Ω)	R after 1000 cycles (Ω)	R after 5000 cycles (Ω)	R after 10000 cycles (Ω)	R after 20000 cycles (Ω)	R after 30000 cycles (Ω)	R after 50000 cycles (Ω)	R after 70000 cycles (Ω)	R after 90000 cycles (Ω)
1	28	32	35	42	45	53	68	176	fail
2	32	36	40	45	49	61	72	231	fail
3	19	21	24	30	36	46	57	128	438
4	24	27	30	36	41	50	63	134	752
5	32	34	37	40	43	52	65	151	863

Table 23 shows the twist test results for the type 3 package. Before twisting, the resistance of all five samples were in the range of 18 Ω to 32 Ω. The resistance of the five samples

increased by 5% to 12% after 20,000 twisting cycles. The five type 3 samples all survived 200,000 twisting cycles, however, the resistance of all five samples increased by 3 - 4 times. Compared with the type 2 package the type 3 package shows a significantly higher strength. Table 24 shows the twist test results for the EDIP package. Before twisting, the resistance of all five samples were in the range of 16 Ω to 31 Ω. All the EDIP package samples had a small resistance change (< 4%) after 20,000 twist cycles. The EDIP samples all survived 200,000 twist cycles and the resistance only increased by less than 1.3 times the original resistance. So, the EDIP package shows the best strength performance in twisting.

Table 23. Twist test results for type 3 package

Sample	R (resistance) before test (Ω)	R after 20000 cycles (Ω)	R after 50000 cycles (Ω)	R after 80000 cycles (Ω)	R after 110000 cycles (Ω)	R after 140000 cycles (Ω)	R after 1700000 cycles (Ω)	R after 200000 cycles (Ω)
1	25	26	28	32	42	48	65	82
2	23	24	25	30	36	46	58	73
3	18	20	22	28	34	42	52	70
4	32	33	34	37	51	63	72	91
5	30	32	35	39	56	71	83	102

Table 24. Twist test results for EDIP package

Sample	R (resistance) before test (Ω)	R after 20000 cycles (Ω)	R after 50000 cycles (Ω)	R after 80000 cycles (Ω)	R after 110000 cycles (Ω)	R after 140000 cycles (Ω)	R after 170000 cycles (Ω)	R after 200000 cycles (Ω)
1	16	16	18	20	23	26	32	36
2	23	24	25	26	29	32	35	38
3	26	26	28	29	32	34	38	42
4	31	32	33	35	37	40	43	46
5	28	29	30	33	36	38	41	44

7.3.3 Cyclical bending test results

Cyclical bending tests were also undertaken on five samples of each of the four packages. Table 25 shows the cyclical bending test results for the type 1 package. The type 1 samples have initial resistances in range of 3.5 Ω to 6.4 Ω, increased by 2 to 4 times after 10 bending cycles, and further increased by 70% to 110% after 20 bending cycles. All samples failed after 43 bending cycles. Table 26 shows the cyclical bending test results for the type 2 package. Before bending, the resistances of all five samples were in the range of 3.3 Ω to 7.3 Ω, increased by 50% to 110% times after 10 bending cycles, and samples 1 and 5 failed after the 70th and 68th bending cycle respectively and all failed by the 79th bending cycle.

Table 25. Cyclical bending test results for the type 1 package

Sample	R(resistance) before test (Ω)	R after 10th cycle(Ω)	R after 20th cycle(Ω)	R after 30th cycle(Ω)	R after 40th cycle(Ω)	R after 50th cycle(Ω)
1	3.5	12.6	22	74.1	Fail at 39th cycle	
2	4.4	10.9	19.3	49.6	86.3	Fail at 43th cycle
3	4.2	12.3	20.7	73.5	Fail at 40th cycle	
4	5.1	13.8	27.3	85.4	Fail at 37th cycle	
5	6.4	15.2	30.6	89.1	Fail at 35th cycle	

Table 26. Cyclical bending test results for type 2 package

Sample	R(resistance) before test (Ω)	R after 10th cycle(Ω)	R after 20th cycle(Ω)	R after 30th cycle(Ω)	R after 40th cycle(Ω)	R after 50th cycle(Ω)	R after 60th cycle(Ω)	R after 70th cycle(Ω)	R after 80th cycle(Ω)
1	3.3	6.1	18.2	33	46.1	59.9	72.8	86.7	Fail at 70th cycle
2	4.7	8.3	22.9	37.8	49.8	63.2	75.4	92.4	Fail at 75th cycle
3	5.1	9.7	26	40.7	50.3	67.3	79.1	89.3	Fail at 73th cycle
4	2.9	5.9	16.7	29.3	42.6	58.2	69.7	81.6	Fail at 79th cycle
5	7.3	11.2	27.4	42.1	53.8	73.4	88.7	Fail at 68th cycle	

The resistances of all type 3 package samples increased by 25% to 70% after the 10 bending cycles as shown in Table 27, and further increased by 1.5 to 2.5 times after the 50th bending cycle. The five samples survived an average of 487 bending cycles. Table 28 shows the cyclical bending test results for the EDIP package. Before the test, the resistances for all five samples were in the range of 6.8 Ω to 13.2 Ω. All samples are increased by 50% to 90% after the 50th bending cycle. Compared to the type 3 package, the resistance of the EDIP samples increases at a lower rate. The five EDIP samples survived an average of 896 bending cycles offering the best performance in cyclical bending.

Table 27. Cyclical bending test results for the type 3 package

Sample	R(resistance) before test (Ω)	R after 10th cycle(Ω)	R after 50th cycle(Ω)	R after 100th cycle(Ω)	R after 200th cycle (Ω)	R after 300th cycle(Ω)	R after 400th cycle(Ω)	R after 500th cycle(Ω)	R after 600th cycle(Ω)
1	6.2	8.3	17.5	31.3	53.2	78.3	97.2	Fail at 473th cycle	
2	8.1	12.5	19.3	32.5	47.5	72.9	84.1	104.3	Fail at 517th cycle
3	4.3	6.6	14.8	23.9	39.1	57.6	75.8	92.2	Fail at 525th cycle
4	9.2	13.3	22.7	39.4	58.7	83.4	96.3	Fail at 495th cycle	
5	14.7	17.9	27.2	42.7	57.9	81.7	98.5	Fail at 484th cycle	

The best EDIP with 0.025 mm silicon die survived 927 bending cycles, all EDIP package sample failed also because of the silicon chip broken. The bending test result shows that the best EDIP with 0.1 mm metal chip survived 1470 bending cycles and failed because of conductive adhesive fail. This comparison further proves the metal chip has better strength than silicon chip. This result does not conflict with the simulation result shows in chapter four (0.025 mm is the best thickness of die) which because of in chapter five all simulations only considered silicon die.

Table 28. Cyclical bending test results for the EDIP package

Sample	R(resistance) before test (Ω)	R after 50th cycle(Ω)	R after 200th cycle(Ω)	R after 400th cycle(Ω)	R after 600th cycle(Ω)	R after 800th cycle(Ω)	R after 900th cycle(Ω)	R after 1000th cycle(Ω)
1	6.3	12.1	33.6	51.7	72.5	93.6	Fail at 872th cycle	
2	4.7	7.3	27.1	43.6	62.3	77.8	93.8	Fail at 927th cycle
3	13.2	19.8	42.4	59.3	84.6	102.4	Fail at 883th cycle	
4	9.5	14.7	37.2	57.5	78.9	97.5	Fail at 895th cycle	
5	7.9	13.6	35.7	54.8	76.3	92.1	92.1	Fail at 904th cycle

7.4 Conclusions

25 μm silicon chips of four different sizes (1 mm x 1 mm, 0.5 mm x 2 mm, 2 mm x 1 mm, 2 mm x 2 mm) were fabricated using photolithography, lift-off and HF etch technology. A thinner silicon chip improves the flexibility of the e-textiles. The four packaging technologies for E-textiles have compared in this chapter using wash testing, twisting and cyclical bending. The type 1 packaging approach performed the worst washing, twisting and bending results, which because of the type 1 packages do not have the under-fill layer to provide additional mechanical support to increase the mechanical reliability, and also have no encapsulation layer to offer further protections to packaged die, but type 1 package is the most flexible package as it is the most thinner package. Compared to the type 1 packaging method, the type 2 packaging method provide better washing, twisting and bending performance which indicated the under-fill material increased the reliability of the electronic package. The type 3 package method performed better than the type 1 and 2 package method in all tests which further proved the encapsulation layer offered protections to packaged die. The best package (EDIP) survived up to 25, 200,000 and 927 cycles of wash test, 180° twist testing and 90° bending testing are respectively.

Chapter 8 Conclusion and future work

8.1 Conclusion

This thesis seeks to develop the reliable electronic packaging to mounting ultra-thin die onto the plastic substrate that contains conductive interconnects and bond pads for interconnecting the packaged die to other electronic components or power supplies, the reliability, wash ability and flexibility of electronic package are three key points.

Stresses analysis simulation in electronic packaging be used in this thesis aims to determine the optimal thickness and materials for each packaging layer (such as substrate layer, adhesive under-fill layer and die layer) to increase the reliability of the electronic package. A 0.025 mm thick silicon die, 0.05 to 0.052 mm thick Kapton substrate, and a 0.05 mm EP37-3FLF adhesive layer were identified as the optimum materials and thicknesses for the electronic package. Using stress analysis simulation to determine optimal thickness and material of each packaged layer is the first demonstration to used simulation method to compare different electronic package materials and determine optimal thickness. The bending and shear experiment test discussed in Chapter 5 used to verify the simulation result described in Chapter 4. The simulation results show a very good correlation with experimental results that gives a high level of confidence in this simulation approach. The new method to determine the practical shear strength presented in section 5.4 can be used to determine the shear strength for any adhesive when combined with a specific material (such as Kapton or silicon).

A packaging approach that uses a moulded plastic film to encapsulate a flexible electronic circuit comprising, for example, bare silicon chips and ultrathin die, has been developed and tested in Chapter 6. By encapsulating die between two films, it also possible to locate the die at the neutral axis of the assembly which means that the stresses applied to the silicon are minimised. This is also the first demonstrated method for reliably incorporating electronic circuits in a textile and that can withstand numerous, typically >35, machine washing cycles.

An ultra-thin silicon chip fabrication method for electronic textiles (e-textiles) has been investigated in Chapter 7 aims to maximize the flexibility of e-textiles, SOI (Silicon on Insulator) wafer be used to fabricate various thickness of ultra-thin chip by changing the

different thickness of device layer on SOI. An example thickness about 25 μm with four different sizes (1 mm x 1 mm, 0.5 mm x 2 mm, 2 mm x 1 mm, 2 mm x 2 mm) of silicon chip has been fabricated in this thesis, a 6 inch of SOI with 25 μm thickness of device layer has been used for fabricate ultra-thin chip, photolithography and lift-off technology are used for metallization of the chip, the Hydrogen Fluoride (HF) be used for thinning the silicon chip, The most commonly used chip size for e-textiles 2 mm x1 mm has been packaged by four packaging methods and experimentally evaluated under washing, twisting and cycle bending test to discuss characterization of the chip's reliability and flexibility. The minimum survived cycles for EDIP package samples in 180° twisting test, 90° bending test and washing test are 200000, 23 and 22 respectively, EDIP packaging method shows the best strength to withstand the washing, twisting and cycling bending test compared with type 1, 2 and 3 packaging methods.

8.2 Future work

The electrical connection between the die and Kapton substrate in the novel electronic packaging method developed in this thesis is used as the conductive adhesive, the solder paste is another material to provide electrical connection. A future study to compare the solder paste and conductive adhesive used in novel electronic packaging method need to be tested under shear, bending, twisting and washing test to determine the better conductive material to improve the reliability of the novel electronic package method.

The daisy chain ultra-thin chip fabricated in chapter 7 just shows the new processes to do the ultra-thin chip fabrications, the future investigation needs to add the electronic function, such as sensor function to the ultra-thin chip.

The future investigation also can focus on using the EDIP technology to package commercial sensors such as RFDI tag to tracking textile products, monitoring wearer’s safety and providing security access control as an alternative to the access card.

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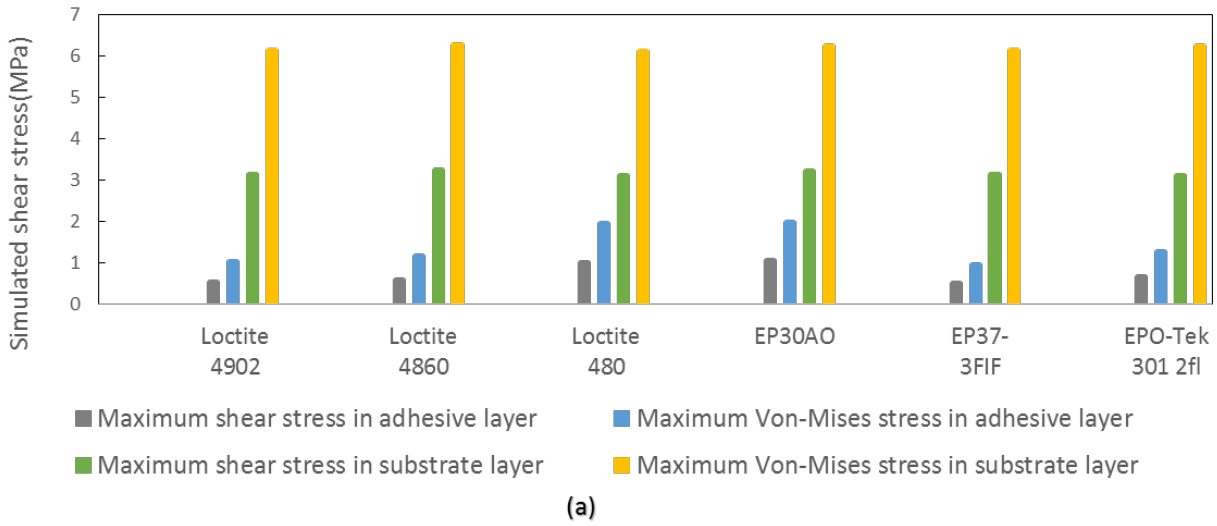
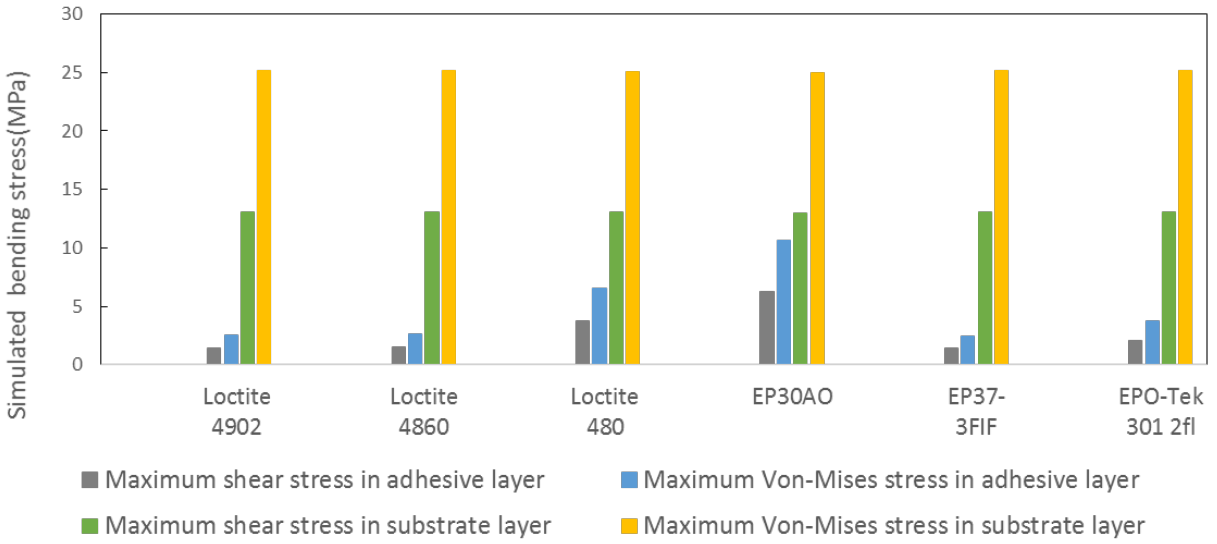
Appendix A



(a)



(b)

Figure 109. Shear and von-Mises stress simulations to compare adhesives with a Kapton substrate, (a) shear load model, (b) bending model.

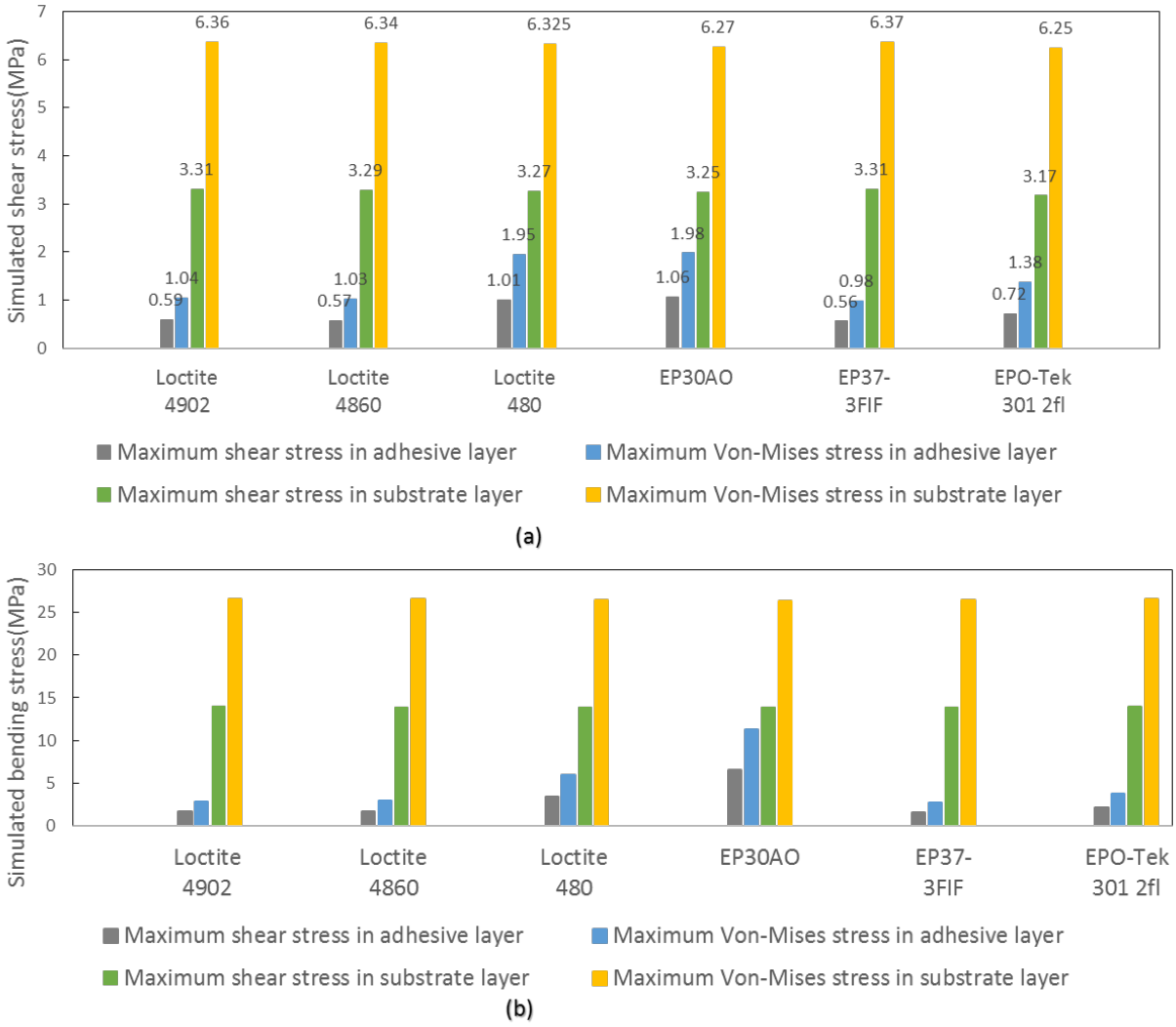
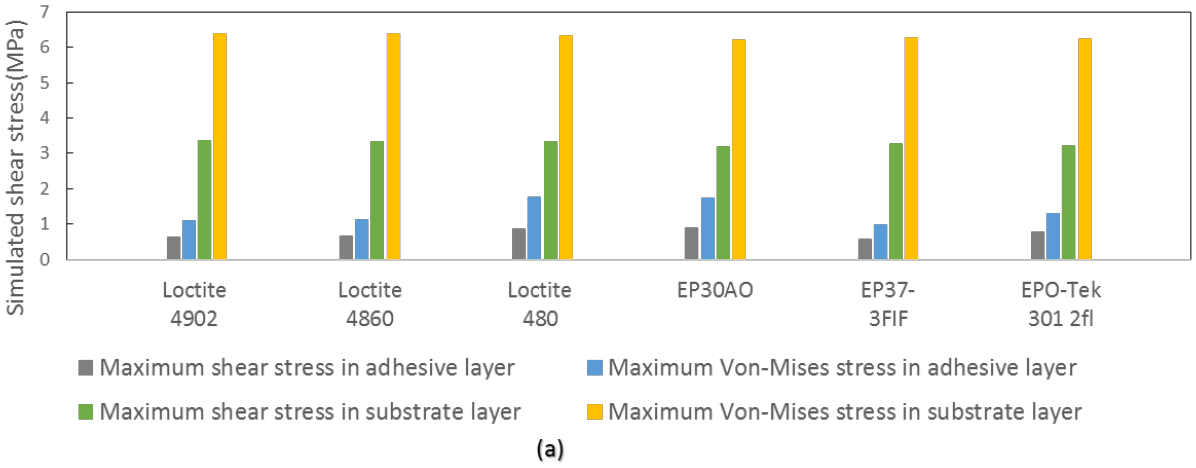
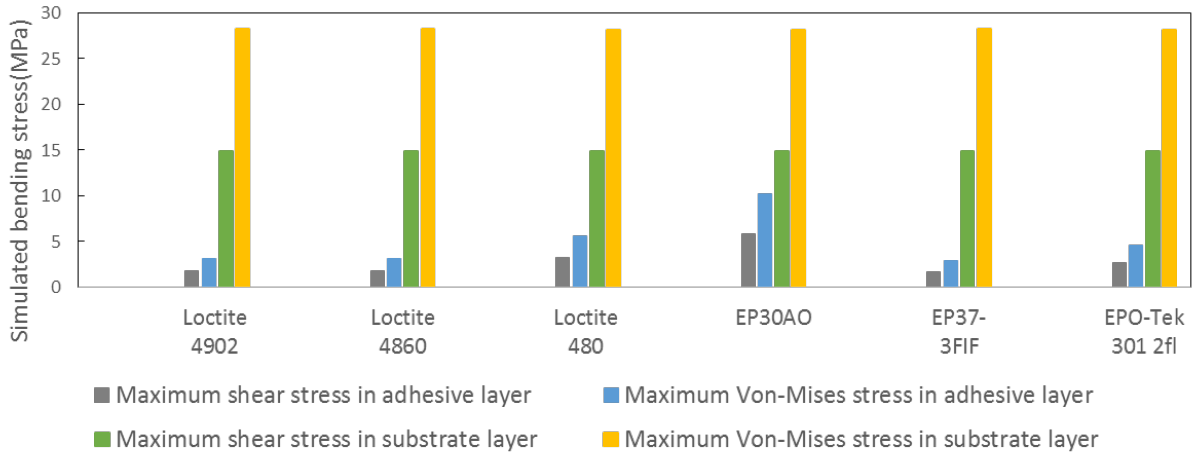


Figure 110. Shear and von-Mises stress simulations to compare adhesives with a Mylar substrate, (a) shear load model, (b) bending model.



(a)

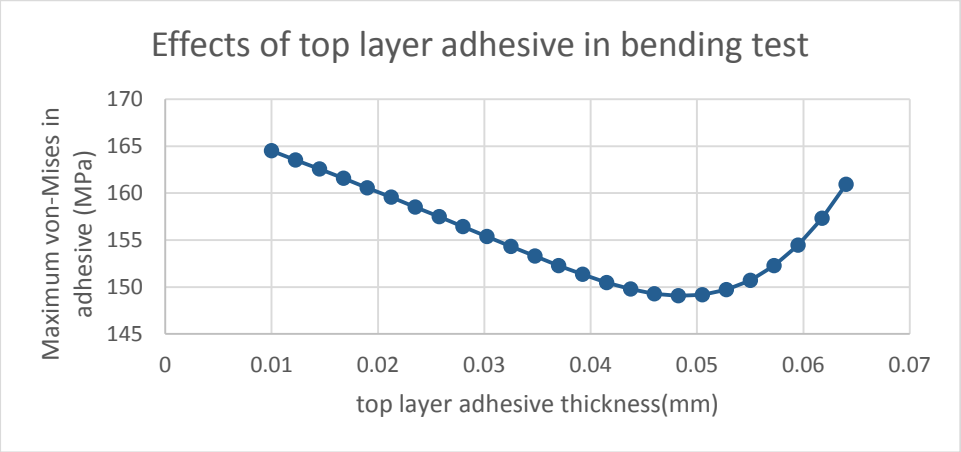


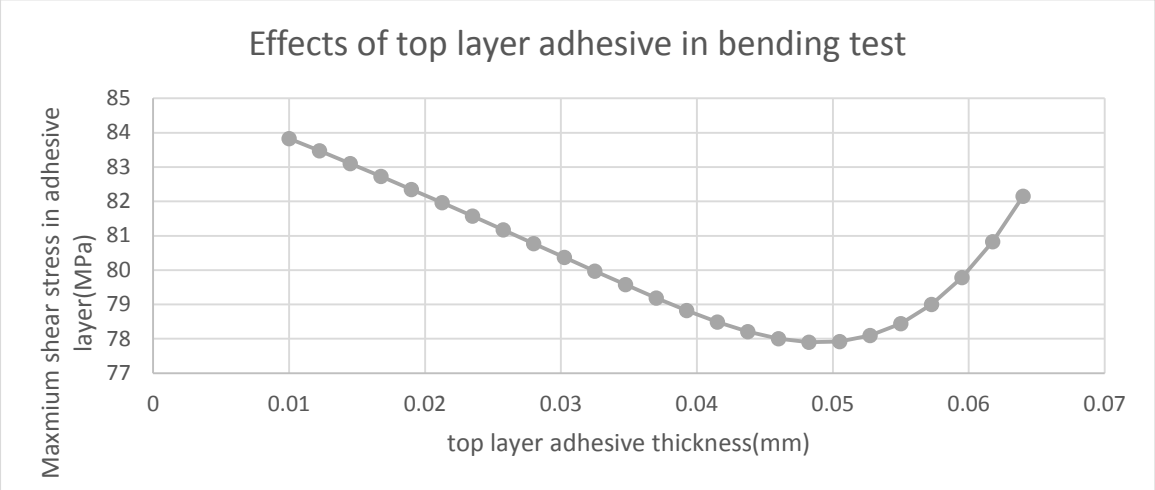
(b)

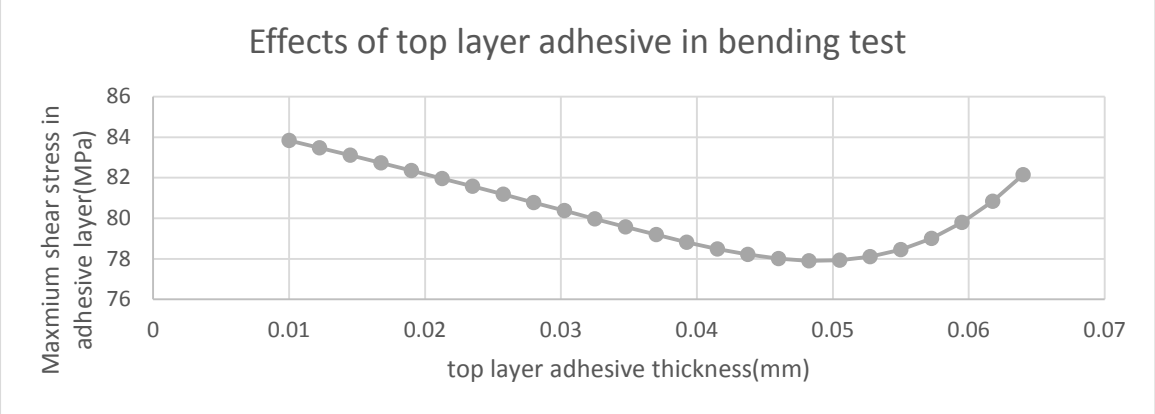
Figure 111. Shear and von-Mises stress simulations to compare adhesives with a PEEK substrate, (a) shear load model, (b) bending model

Appendix B

Simulation results indicate the relationship between the bottom adhesive layer and von-Mise stress, maximum shear stress and strain energy.







Appendix C

Neutral axis in the electronic package

Neutral axis is an axis in the cross section of a beam along which there are no stresses or strain. When the beam is under pure bending condition (see Figure 109), the stress or strain in XY plane and ZX plane on the neutral axis is zero.

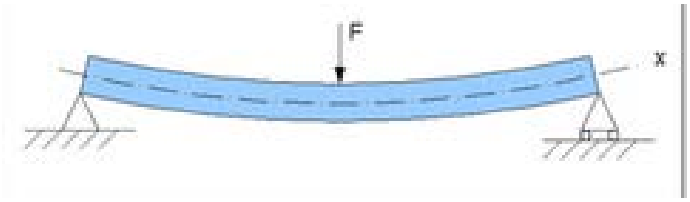


Figure 112. Beam in pure bending condition.

In Figure 109, X is the neutral axis of the beam, r_{xy}=r_{xz}=t_{xz}=t_{xy}=0 where r is the shear strain and t is the shear stress. The negative strain or stress is on the top of the neutral axis and positive strain or stress is in the bottom of the neutral axis.

Neutral axis for single layer beam

Normally the neutral axis located in the centreline of the cross section of beam. The neutral axis and the Maximum bending stress can be calculated by:

$$\frac{M}{I_{xx}} = \frac{E}{r} = \frac{Q_b}{y}$$

Where M is the bending moment at section, I_{xx} is the second moment of area, E is Young's Modulus of the materials, r is the radius of curvature, Q_b is the bending stress at the section and y is the distance from neutral axis to edge.

The bending moment *M* is defined as the turning effect of two forces on a beam about its neutral axis during bending. One force is the negative force and located on top of neutral axis while the other force is a positive force and below neutral axis, however, the bending moment must be produced by an external force acting on the beam cause the first bending. The bending moment M has the formula of:

$\frac{\delta M}{\delta F}$=y

Where y is the distance from the neutral axis, F is the force applied on the elementary strip caused the moment of beam first bend.

If δy tends to zero the total moment is found by:

M= $\sum y\ \delta F = \int_{bottom}^{top} y\ dF = \int_{bottom}^{top} y \frac{Ey}{R}$ dA= $\frac{E}{R}\int_{bottom}^{top} y^2$ dA

The $I_{xx} = \int_{bottom}^{top} y^2$ dA is defined by the second moment of area about the neutral axis. So M= $\frac{E}{R}$ I, then M/I=E/R.

The young modulus E is related to the direct stress (Q) and direct strain (e),
E= direct stress/ direct strain=Q/e.

Figure 110 is a bending beam and a layer of stretched material have the distance of y from the neutral axis.

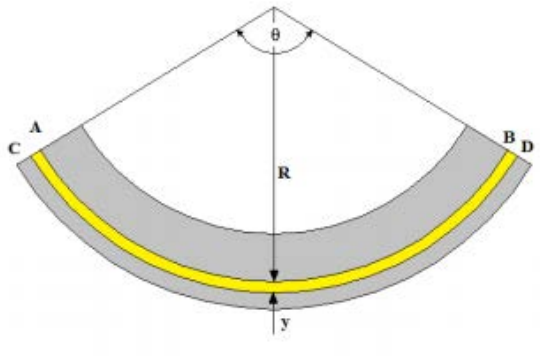


Figure 113. A bending beam.

The length of AB=Rθ, DC= (R + y) θ. The strain in this layer e = changed in length/ original length = (DC-AB)/AB= [(R + y) θ – Rθ]/ Rθ =y/R

Substitute e=y/R to E=Q/e, so E=QR/y E/R=Q/y

Neutral axis for multi-layered beam

Figure 111 shows a multi-layered beam containing a total of n layers. Z1 represents the position of the neutral axis of the beam.

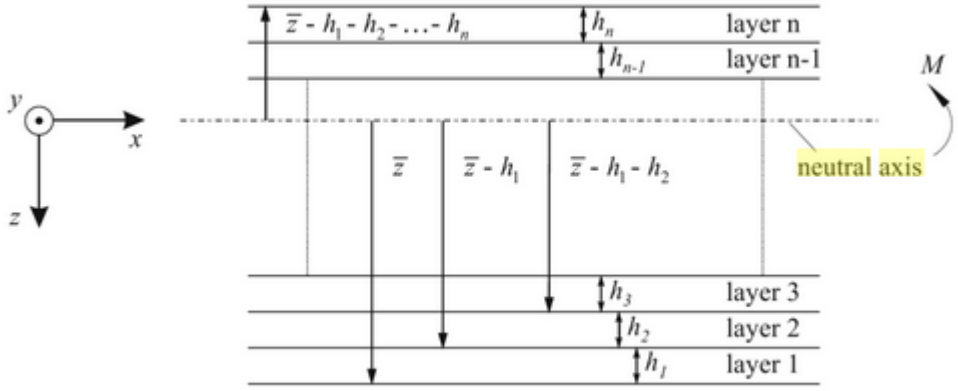


Figure 114. N layers of beam

$$Z1 = \frac{\sum_{i=1}^{n} E_i x_i h_i \quad (2\sum_{j=1}^{i} h_j - h_i)}{2\sum_{i=1}^{n} E_i x_i h_i}$$

Where, E_i is Young's modulus of the i-th layer, $x_i$is the width of the i-th layer and h_i is the height of the i-th layer.

In electronic packaging, the electronic die and the conductive tracks are better protected by locating them as close as possible to the neutral axis. Neutral axis of the electronic package has been simulated and reported in chapter 4.