UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND APPLIED SCIENCE

ELECTRONICS DEPARTMENT

LASER TESTING OF INTEGRATED CIRCUITS

A thesis submitted for the degree of

Doctor of Philosophy of the University of Southampton

by

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- August 1977 -

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ABSTRACT

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Comprehensive testing is one of the major problems in the production of l.s.i. : principally this is because of the small number of circuit nodes which are directly accessible to the tester and the extremely long input sequences needed for exhaustive testing.

A technique is presented in which information is injected directly into the internal circuitry of an integrated circuit via a finely focussed laser beam. The intensity of the light input is controlled by an electro-optic modulator, enabling data patterns to be inserted at high speed. The laser beam power necessary to achieve this task in an i.c. is dependent upon the circuit implementation: a small 2mW laser has proved to be adequate for the testing of M.O.S. and I^2L circuitry but more than 10mW is needed for some forms of T.T.L., E.C.L. and C.M.O.S.

The non-contacting, non-destructive laser probe has also been used to determine some features of the operation of the internal circuitry, including measurement of transient waveforms, and two important semiconductor parameters – diffusion length and lifetime.

Fault diagnosis with improved resolution can be performed quickly and easily by using the moveable laser input and large savings in the time taken for fault detection are also envisaged from this technique, especially when used in conjunction with conventional automatic test equipment.

ACKNOWLEDGEMENTS

I would like to thank my supervisor, Mr J.G. Smith, for his continuing support and encouragement and the other members of the Microelectronics Group, in particular Mr H.A. Kemhadjian and Dr. A. Brunnschweiler, for helpful discussions and comments throughout this work. It is also a pleasure to acknowledge the invaluable assistance and enthusiasm of my colleague Mr J.C. White at all levels and on many topics during the past three years.

H.E. Oldham

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CHAPTER 1

INTRODUCTION

1. INTRODUCTION

Electronic circuits have been shrunk by modern technology to a fraction of the size occupied by their predecessors, particularly since the introduction of integrated circuits. The reliability of these devices is very high, they are relatively cheap and in many cases can operate faster and with less power dissipation than previous circuits.

However, as they increase in complexity, it becomes much harder to ensure that they are working correctly in every detail. The evolutionary refinements in circuit design and manufacturing techniques have outpaced testing methods so that today very large scale integrated circuits (vlsi) are being produced which cannot be tested economically, because the test routines can only cope efficiently with medium scale integration (msi) where the ratio of input and outputs to the circuit interior is much larger. The only way to test large complicated circuits has been to apply extremely long test sequences to the devices' inputs in order to exercise them through all, or most of, the possible conditions they may encounter in service. This process may take so much time and involve such vast amounts of information storage that the cost of testing becomes much larger than the cost of producing the device; thus the problem of quick and efficient integrated circuit testing must be solved if the trend towards cheaper and more comprehensive circuitry is to be maintained.

A technique is presented in this thesis which can be used to speed up the test process and improve the testability of a circuit by introducing extra inputs without the need for major redesign of the circuit itself. The method is based upon the fact that a laser beam produces a current when it hits the surface of an integrated circuit: this behaves in the same way to a current injected by a conventional probe positioned at the same point, but the laser 'probe' has the advantage of being non-contacting, very small and easily moved from site to site.

The operation, characteristics and capabilities of the laser probe are detailed in sections 3 and 5 and another use of the method is described in section 4, under the heading 'Evaluation of the semiconductor substrate'. Present methods of integrated circuit testing are described in section 2, and the advantages and changes which laser probing would bring in this context are discussed in the penultimate section.

A summary of the results is presented in section 7, by which stage it is to be hoped that laser testing of integrated circuits will be seen to be useful in counteracting the situation where testing integrated circuits is often more of a problem than making them.

CHAPTER 2

A BACKGROUND TO INTEGRATED CIRCUIT TESTING

- Faults and failure mechanisms
- Methods used in i.c. testing
- Fault detection in digital i.c.'s
- L.S.I. testing problems
- Testability of integrated circuits
- Provision of extra circuit inputs

2. A BACKGROUND TO INTEGRATED CIRCUIT TESTING

In the most general sense, i.e. testing means an application of an input sequence to a device followed by a comparison between the precomputed 'expected' output sequence and the one actually observed. Any discrepancy implies a failure, the cause of which is a fault.

2.1 Faults and Failure Mechanisms

Faults can be categorised into two broad groups: logical and parametric. A logical fault is one which causes the logical operation of a circuit to be changed to some other function, but a parametric fault alters the magnitude of a circuit parameter, such as speed, current or voltage, without necessarily changing the logical behaviour of the circuit. For example, a short would probably be a logical fault whereas a 'leaky' reverse characteristic of a transistor could be a parametric fault.

A fault may occur at any time during the life of an integrated circuit: in the manufacturing process or during assembly, testing, storage and in service. The nature of the faults encountered in each of these periods is different, so consequently the type of testing which is performed at each stage differs.[1] A mixture of logical and parametric faults may occur during manufacture (such as masking defects and bulk shorts) then further failure modes can be introduced during the assembly and testing processes (for example, open bonds or shorting leads). Factors such as high temperature and humidity may produce parametric faults during the storage phase and finally when the circuit is actually used, more failures can be introduced because of heat dissipation, vibration, voltage stress and ageing. A typical graph of failure rate against time for an integrated circuit family shows a 'bathtub' distribution[2] with a high initial failure rate, reaching a low value after the early failures are discarded and finally rising again when component ageing becomes significant.

Failures are caused by an imperfect manufacturing process or an unsatisfactory operating environment; thus not only does a fault have to be found, but its location and cause needs to be determined in order to prevent its recurrence in future devices. Emphasis is therefore given to diagnostic testing during the initial stages of the manufacture of a new circuit but when the 'teething troubles' are overcome and production begins on a large scale, then commonly fault detection alone is used (a go/no-go test).

2.2 Methods used in I.C. Testing

The performance of an integrated circuit is monitored at each stage of its life in order to discover any failures as soon as they arise[3]. A typical test routine is as follows[4]:

(i) In-process inspection: this is a sampling test made to a specific acceptable quality level which is performed throughout the processing of the device, for example slice inspection after the oxide etch prior to diffusion. The final test is often a visual screen.

(ii) Wafer test: some manufacturers perform only a minimal test at the wafer stage, usually a simple continuity test, when the faults introduced during assembly are considered to be significant, but others give a full test of type (iv) before bonding. Clock rate testing may not be possible for very high speed circuits because of probe loading.

(iii) Accelerated ageing: the circuit is stressed to precipate any time-related failure modes and weed out any latent early failures. This process, which may last for up to 1000 hours, usually includes thermal shock and thermal cycling, electrical and mechanical stressing and a hermiticity check.

(iv) Functional, parametric and clock rate testing: these tests are to ensure that the device performs according to its electrical specifications. Only simple d.c. tests are used if a full wafer test has been performed prior to bonding.

(v) Incoming inspection: many i.c. users perform their own tests (of type (iv)) upon bought devices before incorporation into a final system.

Of these classifications, by far the most effort, time and money is spent on categories (ii) and (iv), but only full wafer testing will be considered in this work.

2.3 Fault Detection in Digital I.C.'s

Analogue circuit tests are usually specifically designed for the particular type of circuit being tested, so no generalizations can be made for testing this type of device.

Digital circuits are characterized by the feature that the steady-state circuit responses can only assume one of two values. They may be studied at the circuit level where the analysis is concerned with waveforms and currents etc., or at the logic level when only two states, logical '0' and '1', are possible.

Digital circuit tests can be sub-divided into three branches[5]:

(a) Functional (DC) testing in which all parts of the circuit are exercised by applying binary input patterns and analysing the corresponding steady-state outputs to check the functional operation of the device. This type of testing usually involves a large number of tests and is performed as fast as possible.

(b) Parametric (AC) testing is used to check the time-related behaviour of the circuit and involves the measurement of actual voltage and current levels to high accuracy, but the test rate is usually low.

(c) Clock rate testing is similar to functional testing, but is performed at rates near the maximum and minimum clock speed of the circuit under test.

Integrated circuit testers range in complexity from a simple comparison tester which can perform some limited functional tests to fully computerised automatic systems with multiple test stations which can perform all of the above tests on i.c.'s fabricated using many different technologies[6]. A schematic diagram of a comprehensive computer-controlled system is shown in figure 1. Typical specifications of a commercial general purpose tester at the top end of its class[7] include functional tests at a 10MHz rate, parametric tests to 160psec resolution, the ability to test TTL, DTL, ECL, MOS and CMOS devices in all types of package up to 120pin and a computer with 16k words of main memory and an 18Mbit disc store. The price is over £ 200,000.

2.4 L.S.I. Testing Problems

Even with such versatile and powerful testers of the type mentioned in the previous section, every user of automatic test equip-ment interviewed in a 1976 survey was dissatisfied with the systems presently available[8]. The main trouble has arisen from the introduction of l.s.i., which is being closely followed by v.l.s.i. (over 1000 gates on a single chip): as the circuits become more complicated, the time taken to test them becomes much longer so the contribution of testing costs to the price of the final product becomes proportionally larger. The percentage of the cost which arises from the testing alone has not been determined for l.s.i. circuits in general, but the trend can be followed from the change from discrete transistors through s.s.i. to m.s.i. circuits, where the testing cost was 5 percent, 15percent and 30percent respectively of the total[9].

Most of this increase arises because more time is needed to apply the functional tests, when the number of input patterns needed to check every aspect of the circuit operation becomes astronomically large. For

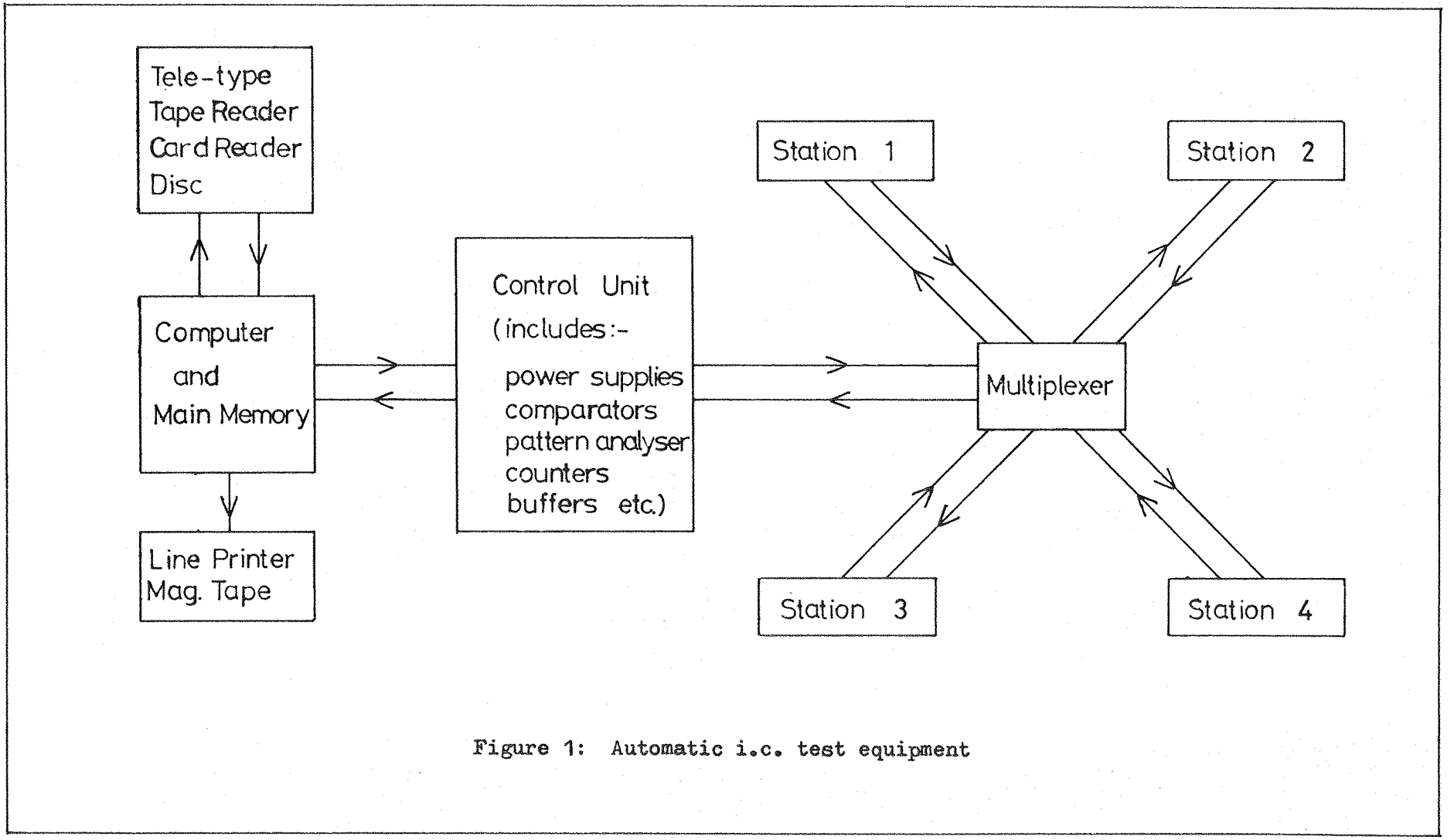


Figure 1: Automatic i.c. test equipment

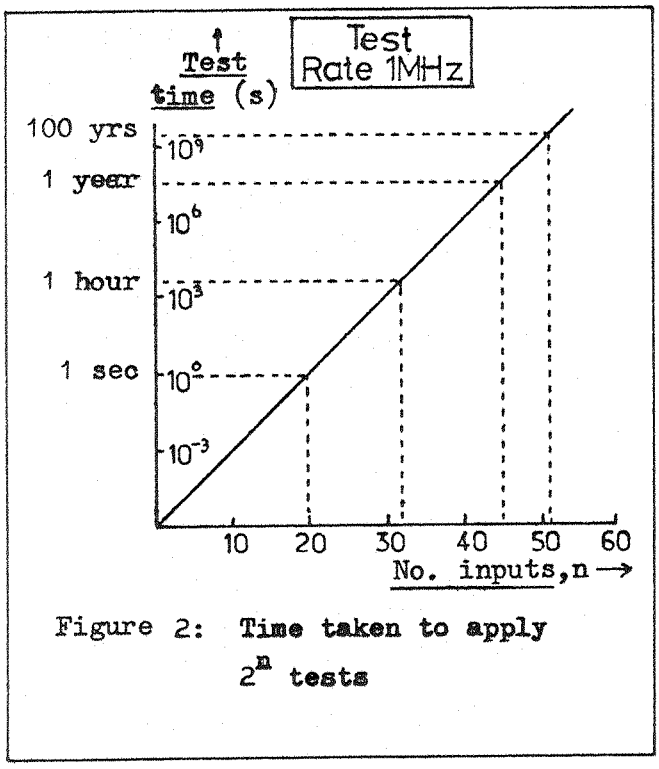


Figure 2: **Time taken to apply 2^n tests**

the case of a combinational circuit (i.e. no feedback loops) with n active inputs, the nu-mber of tests needed to cover every combination is 2^n. The time taken to apply these tests for various values of n is shown in figure 2, assuming a test rate of a million tests per second. If sequential circuits are considered, the presence of feedback loops and storage elements can increase the test time by many orders of magnitude: if m, the number of internal storage states, can be defined, then the number of tests rises to 2^{n+m}. Not only does the time taken to apply the test patterns pose a problem, but the patterns, which may be many millions of bits in length, have to be generated then the outputs compared with the computed 'expected' response, so vast amounts of data must be stored in some memory system. This process can be reduced by techniques such as pseudo-random sequence generation or transition counting but still a very large and expensive store is required.

Circuits are often built which cannot be tested comprehensively in a reasonable time, so 'adequate' testing is then used, where the intention is to cover perhaps 90percent of all possible faults. It is necessary to ensure that worst-case conditions are fully covered, as are all the common failure modes, so the fault diagnosis which is performed during the initial stages in the production of a new circuit is of great importance.

2.5 Testability of Integrated Circuits

Modern i.c.'s are becoming harder to test because there is less access to the internal circuitry than with the earlier, smaller circuits. Package and chip size is kept to the minimum for yield and economic reasons, so as the devices become more complex, the proportion of the circuitry which can be directly reached from the external pins decreases rapidly. If more observation points[10] (i.e. extra outputs) or control points[11] (extra inputs) were provided then testing could be performed more easily and significantly faster.

Theoretical work in the field of circuit design for maximum testability has produced schemes which provide 100percent fault cover with excellent diagnostibility in a very small number of tests (down to three)[12,13,14] by implementing the circuit function in terms of simple units and using a large number of extra input and output pins. In practice such methods are unworkable[15]: for example a 16 pin m.s.i. circuit is transformed to a 180 pin l.s.i. device with a chip area four times larger than previously, in order to reduce the number of tests from ten to six and enable each failure mechanism to be uniquely determined (section 5.6).

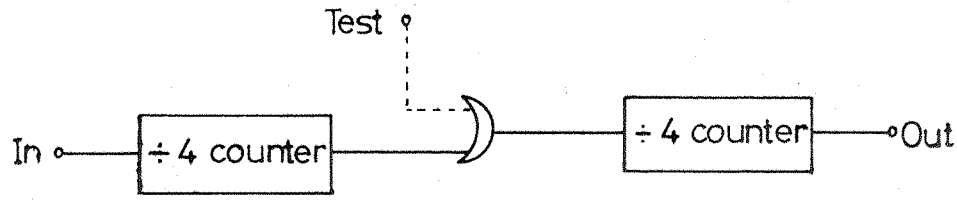
Between the two extremes of circuits designed specifically from the testing viewpoint (as in the above example) and those built with no consideration of testing problems (as the vast majority now are), large benefits can arise from the provision of a few test sites[16]. In the following examples of actual circuits, one or more extra inputs have been added to improve the testability. More output points would be beneficial for diagnostic testing and to determine the states of internal sites, but have not been included here.

Figure 3(a) shows a simple 16-bit counter in which the test pattern length can easily be shortened by adding the test input as shown. Pulses via this test input will force the second half of the counter to advance at a faster rate than normal, so the total number of tests can be reduced from 16 to 7 (4 at the normal input and 3 at the test input). Any fault can obviously be isolated to either the first or the second counter blocks.

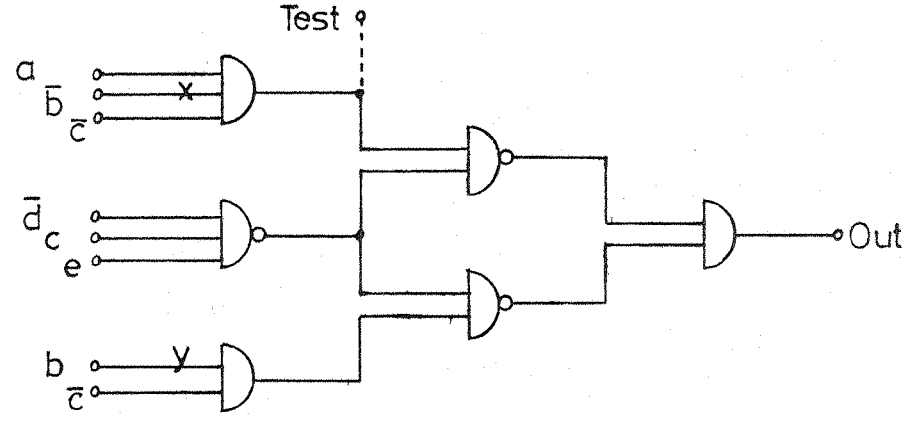
Circuits are commonly designed with some logical redundancy which is introduced in order to eliminate certain potential hazard conditions or improve reliability. In such cases, failures often cannot even be detected and fault diagnosis proves to be almost impossible. The effect of a fault in the redundant branch of a circuit could be to reintroduce the hazard or even to mask the detection of a normally detectable logical fault on a non-redundant connection. Such a situation can arise with the circuit shown in figure 3(b). A stuck-at-1 fault at point X is not detectable at all, but if Y was stuck-at-0 at the same time, then the output would give the correct response to the normal node Y test (a = b = e = '1', c = d = '0'). The inclusion of the test input as shown would enable the whole circuit to be tested, including point X, and similarly all redundant paths in other circuitry can be isolated and tested individually with a suitable choice of test input site.

A small sequential circuit is given as figure 3(c). The state table of simple circuits of this type can be very large, but if the feedback loop is disabled then the circuit reduces to a much simpler one; in this case the test sequence can be reduced from 16 to 5 bits in length by using the extra input shown.

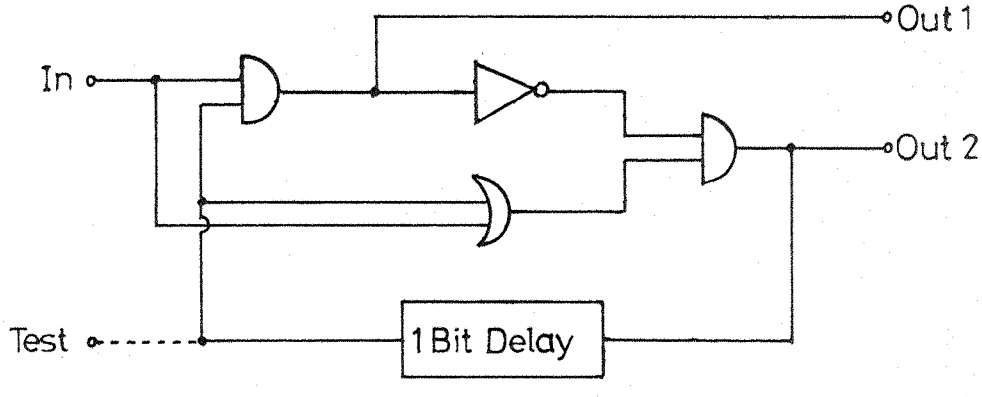
A common difficulty encountered in testing large circuits is that the initial state of certain parts of the circuit needs to be determined before the test pattern can usefully be applied. The common clock generation circuit shown in figure 3(d) illustrates this problem: it is self-initialising but there is no direct reset control, so between 0 and 3 clock pulses (depending upon the present state of the system) must be applied after the inhibit control goes high before both ϕ_1 and ϕ_2 are held at '0' and the test pattern could be meaningfully applied. If a cascade of such circuits is used or if the clock and inhibit controls are derived functions, then the initialisation sequence can become very large. This could be reduced by the provision of extra inputs as shown; an additional advantage of these extra controls is that any faults present in the initialisation circuitry itself can be isolated - this may otherwise be impossible because the starting conditions for the test sequence would not be repeatable.



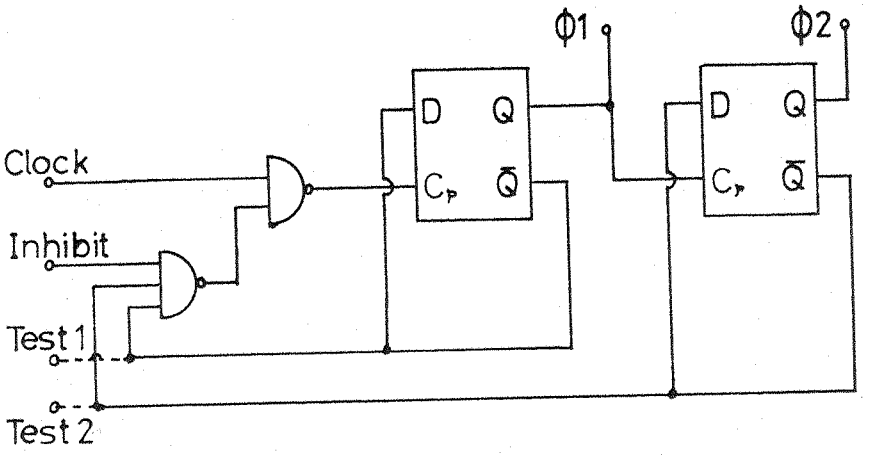
(a) Test sequence reduction (16-bit counter)



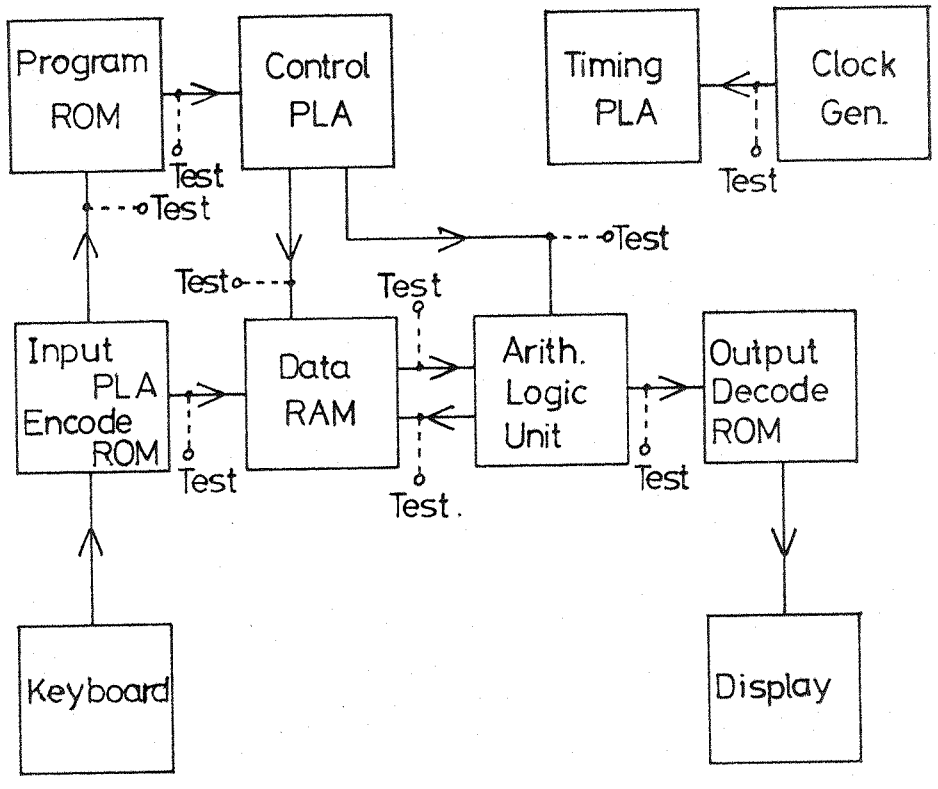
(b) Testing of logically redundant circuitry



(c) Simplification of sequential circuitry



(d) Circuit initialisation (clock generator)



(e) Partitioning into modules (TMS0100 calculator)

Figure 3: Improving testability by the addition of extra inputs

The more complicated 1-chip calculator circuit of figure 3(e) is used to demonstrate a very important benefit which extra inputs can bring. If the interconnections between the various circuit blocks or modules were accessible then each could be isolated and tested individually with a relatively simple sequence. This partitioning method is presently used for microprocessor testing[17].

The addition of extra test inputs to key circuit nodes can therefore be used to speed up the testing process and improve the chances of locating any fault which may occur. Greatest benefit will be gained if a large number of inputs is available, but a compromise between the enhanced testability and the difficulty and expense involved in the provision of these controls will have to be reached.

2.6 Provision of Extra Circuit Inputs

Integrated circuit chip area and package size is at a premium, so any increase in the number of contact pads and internal connections, together with the associated rise in failure rate, is not favoured by manufacturers. Some efforts have been made to give the existing contacts a bifunctional role, with 'can't happen' input conditions used for test purposes or by adding a control signal which modifies the logical behaviour slightly to allow access to different parts of the circuit, but such systems are often complicated and the extra control circuitry itself is often extremely hard to test.

Another method occasionally used is to have a separate metallization mask for one chip on a slice, in which certain internal nodes are brought out to the contact pads instead of the normal inputs and outputs. Only one device per slice is lost in this way but the technique is only useful in diagnostic testing. The usual method of fault diagnosis is to delve into the internal circuitry with a needle probe, typically about 10-20μm wide[18]. This can give accurate dc-level measurements but its capacitance loads down most internal nodes so that meaningful transient readings cannot be taken. The relatively large size of these probes and their clumsiness is very likely to result in some damage to the circuit[19].

Information can be introduced into a circuit via a non-contacting probe, which has the advantage of being non-destructive and easily and accurately moveable. Electron beams have been used to scan the surface [20,21] but in the present study a focussed optical beam is used [22,23] as an active probe. The production and operation of the light probe are described in the following section.

CHAPTER 3

THE LASER PROBE

- Optical illumination of a semiconductor
- The light source
- Characteristics of the laser
- Production of the laser probe
- Laser probing of a silicon integrated circuit
- Light beam modulation
- The laser input

3. THE LASER PROBE

3.1 Optical Illumination of a Semiconductor

Radiation in the visible region of the electromagnetic spectrum can affect the properties of a monolithic integrated circuit. Two mechanisms of importance in relation to this phenomenon are photo--conductivity in the semiconductor and the photovoltaic effect[24].

3.1.1 Photoconductivity

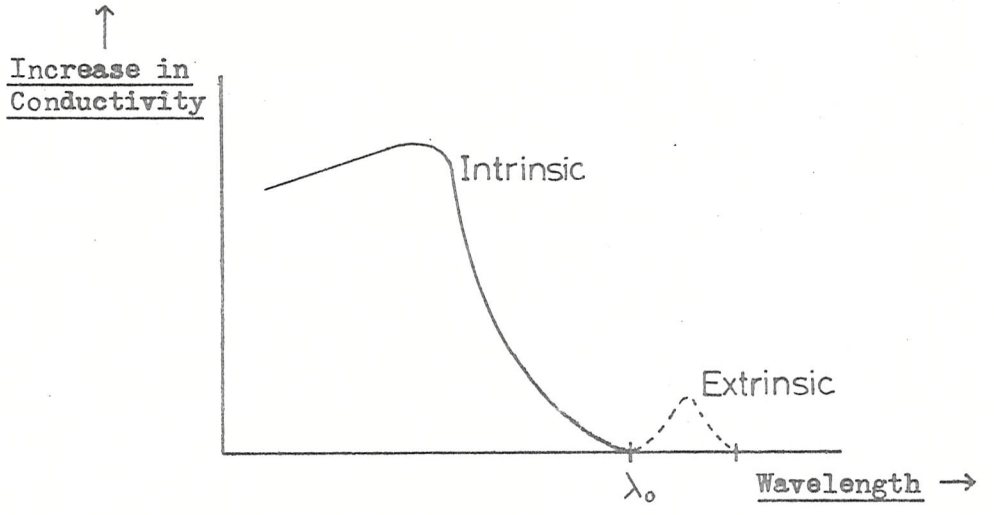
At room temperature, a number of free carriers are present in all intrinsic semiconductors, so a current will flow when a field is applied. If the material is exposed to sufficiently intense radiation of a suitable energy, then a larger current will flow until the radiation is removed. The change in conductivity results from a transfer of energy from the incident photons to the valence band electrons, which can then be excited into the conduction band energy states. In the steady-state, the rate of free carrier generation is balanced by recombination, and when the source of illumination is removed, it is the recombination process that determines the rate of decay of the excess carriers.

The energy of the incident photons must be greater than the energy gap (E_g) of the semiconductor for the photoconductive effect to become significant, so

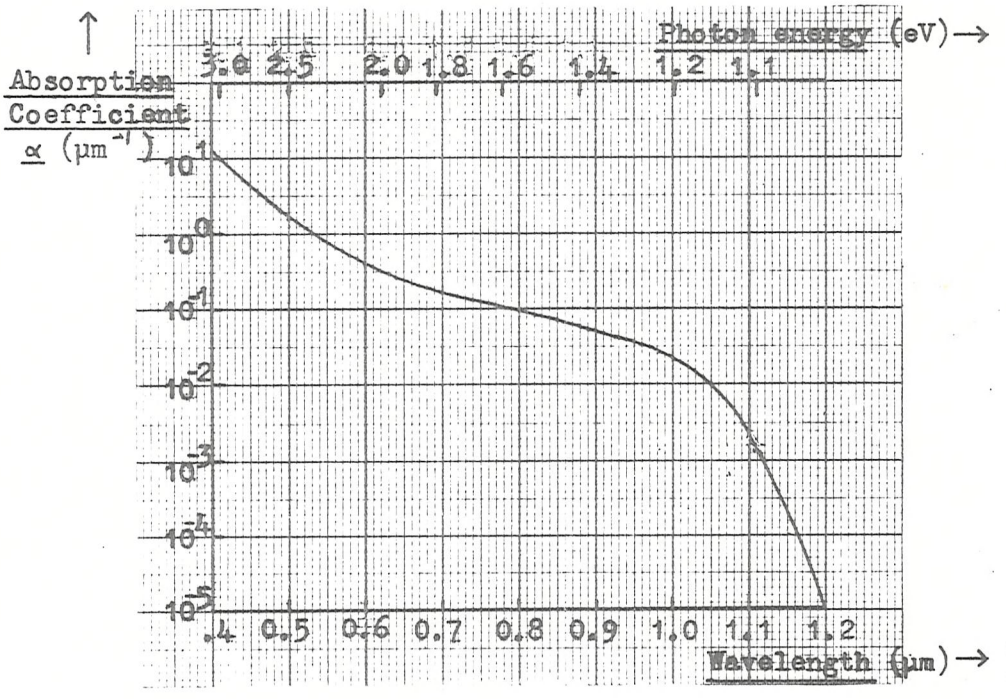
$$h\nu \geq E_g \qquad \ldots (3.1)$$

where h is Planck's constant and ν is the frequency of the illumination. There is therefore a wavelength λ_o above which no change in conductivity is noted, as shown in figure 4(a).

In an extrinsic semiconductor, some conductivity change is noted at wavelengths larger than λ_o since the difference in energy between impurity levels and the valence and conduction bands becomes the effective energy gap; the photon energy may also be absorbed by free carriers and



(a) Photoconductivity in silicon



(b) Absorption coefficient in silicon[25]

Figure 4: Photo-effects in silicon

excitons or create multiple electron-hole pairs, so equation (3.1) is only approximately true in practice.

The light intensity (I) drops by a factor α per unit distance of travel inside the semiconductor because of absorption:

$$\frac{dI}{dz} = -\alpha I \qquad \ldots (3.2)$$

If the absorption coefficient, α, is not a function of the intensity then at a depth z the intensity is

$$I(z) = I_o . \exp(-\alpha z) \qquad \ldots (3.3)$$

where I_o is the intensity just inside the surface, at z = 0. The characteristic length, $1/\alpha$, is called the penetration depth, and nearly 90percent of the incident illumination is absorbed within two penetration depths. The variation of absorption coefficient with the wavelength of the incident light is shown in figure 4(b) for silicon at room temperature[25].

The rate of carrier generation per unit volume is dependent upon the light intensity, as shown by the equation

$$g = \frac{\alpha I}{h\nu} = \frac{\alpha I_o . \exp(-\alpha z)}{h\nu} \qquad \ldots (3.4)$$

assuming that every absorbed photon produces an electron-hole pair.

3.1.2 The photovoltaic effect

Photocurrents can be detected in a homogeneous semiconductor when an electric field is applied, but they also can be found in the absence of an applied field in an inhomogeneous semiconductor, due to the existence of localised 'built-in' fields. The light produces an excess of free carriers which move in response to these electric fields and accumulate in regions where they produce a net space charge. This generation of a voltage across a portion of the semiconductor by light is called the photovoltaic effect.

The internal field arising from a variation in the semiconductor doping at a pn-junction will be considered here, but discontinuities such as a heterojunction, and strains or impurities can also give rise to local fields. The built-in field at the junction drives the free electrons

and holes generated by the light in opposite directions, with the electrons moving to the n-type and holes to the p-type region; this charge separation results in the appearance of a potential difference across the junction with the p-region becoming positive with respect to the n-type. The pn-junction is therefore biassed in the forward direction, so more carriers will overcome the lowered potential barrier and be injected into the opposite region, where they become minority carriers and recombine.

If an external circuit is connected across the junction, then either a photovoltage or, if the load resistance is low, a photocurrent will be detected, with the illuminated pn-junction behaving like a battery. The effect of light upon the junction characteristic is shown schematically in figure 5. The photocurrent adds to the reverse saturation current (I_s), so if the light generates a current I_{sc} with the junction short-circuited, then the normal diode equation is modified to

$$I_L = I_s(\exp(qV/kT) - 1) - I_{sc} \qquad \ldots (3.5)$$

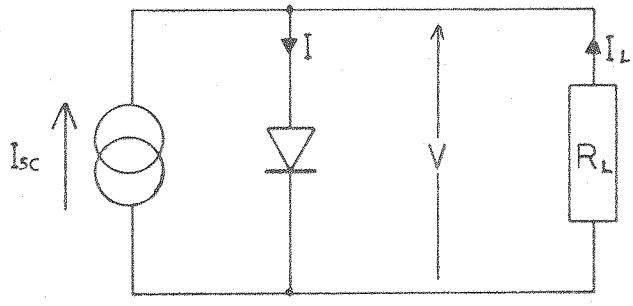
where I_L is the current through the load, k is Boltzmann's constant, V is the voltage across the junction, q is the electronic charge and T the temperature. For an open-circuited diode, $I_L = 0$ and

$$V_{oc} = \frac{kT}{q} \log_e(I_{sc}/I_s + 1) \qquad \ldots (3.6)$$

where V_{oc} is the voltage appearing across the junction in the absence of current flow.

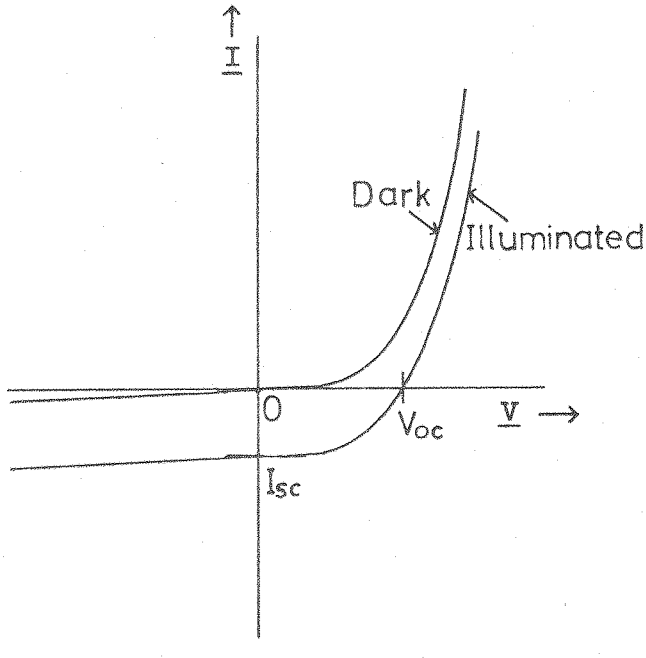
The value of I_{sc} is related to the light power (P), the photon energy ($h\nu$) and quantum efficiency (η) i.e. the number of electron-hole pairs generated per incident photon, by the equation

$$I_{sc} = \frac{P}{h\nu} \cdot q \cdot \eta \qquad \ldots (3.7)$$



$$I_{sc} = \frac{qP\eta}{h\nu} \qquad I_L = I_s[\exp(qV/kT) - 1] - I_{sc}$$

(a) Equivalent circuit



(b) Diode characteristic

Figure 5: Illumination of a pn-junction

3.2 The Light Source

'Probe' diameters of well under a micron have been obtained using focussed electron beams, with beam energy and penetration capable of accurate control,[26,27,28] but such systems must have the semiconductor sample enclosed in a vacuum chamber and the 'charged' probe can itself influence the properties of the material under test[29,30]. Optical beams cannot be focussed to such a small size but are much easier to use and cheaper, neither do they interact detrimentally with the illuminated semiconductor: as a result, an optical source has been considered to be more suitable for the present system.

Semiconductor silicon is the most widely used material in modern integrated circuits, so the choice of the source has been governed by its properties. At room temperature, the energy gap is about 1.1eV, so the critical wavelength λ_o is 1.1μm. The region of most interest in an i.c. is the surface and the layer immediately below it, down to the junction depth which is typically up to 3μm deep. The radiation should therefore be mainly absorbed within this region: from figure 4(b) it can be seen that the penetration depth (α^{-1}) is 3μm when the wavelength is 6440Å, and over 90percent of the light is absorbed within this depth if the wavelength is less than 5340Å.

A strong light source is needed so that the focussed beam will produce a significant number of excess carriers in the semiconductor. Quartz-halogen lamps with a monochromator have been used for this purpose[31], but a large part of the power output is lost in focussing down to a small spot. The advent of the laser has brought the opportunity to use a collimated beam with high power density, but in general the output wavelength is fixed. A common laser whose wavelength satisfies the criteria mentioned above is the helium-neon laser with λ= 6328Å. Other suitable choices would include the krypton laser (λ= 4131, 5309, 5681, 6471, 7525Å) and Nd:YAG (λ= 5320Å, α^{-1} = 1.28μm). By using different or multiple-wavelength lasers, the penetration depth could be varied from 0.2μm to 8μm, but for the present work, the cheap HeNe c.w. laser has proved satisfactory. At this particular wavelength the photon energy is 1.96eV and the penetration depth is 2.4μm.

3.3 Characteristics of the Laser

The beam of light emerging from a laser has a gaussian intensity distribution if it is operated in the TEM_{oo} mode[32]. The properties of these beams and the equations governing their propagation are detailed in Appendix 1.

The width of the beam must be determined at various points along the optical path in order to calculate the size and position of the focus; however a gaussian beam width, which is defined as the distance over which the intensity drops to e^{-2} of its peak value, cannot simply be measured from visual observation because of the non-uniform intensity across the beam. Two methods have been used to measure this parameter:-

(i) a pinhole is scanned across the beam and the intensity measured at each point

and (ii) an iris is used to restrict the beam and its aperture adjusted until its radius is equal to the beam width.

A 0.4mm diameter pinhole has been used to measure beam widths of greater than 1mm, and the results of a scan across the beam at a distance 2000mm from the laser are shown in figure 6, from which the beam width can be calculated to be 1.11mm; a gaussian curve is super-imposed upon the plot to demonstrate that the laser is operating in the TEM_{oo} mode.

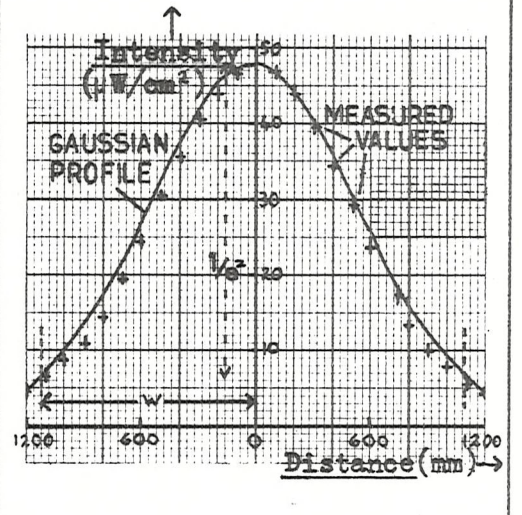


Figure 6: Gaussian beam intensity distribution

The proportion of the power intercepted by a circular iris of radius a is

$$P_{iris} = P.(1-\exp(-2a^2/w^2)) \quad \ldots (3.8)$$

where w is the beam width, so by adjusting the aperture till 13.5percent of the power is lost, the beam width can be found directly by measuring the iris radius. The diameter of the aperture could be measured to within 50μm and this method was used for beam

widths up to 5mm; the values obtained agreed well with those from the intensity scan using the pinhole.

After the radius has been found at various positions along the beam, an iterative procedure is used with equation (A1.2) in Appendix 1 to find the beam focus and its position. Measurement of the beam transformation by lenses has been found to be usually in good agreement with the theory outlined in the Appendix.

Both a 1mW* and a 7.5mW† laser have been used in the present study, and each produced a vertically polarized output beam. For the larger laser, the untransformed beam waist was measured to be 0.56mm at a position 200mm behind the output mirror; its far field divergence angle is 0.36mrad.

Laser power levels have been measured in radiometric units using a silicon pin diode of 1cm^2 active area‡, but conversion can be made to photometric units by using the identity

$$\text{Flux (lumens)} = 137 \times \text{Power (watts)} \qquad \ldots (3.9)$$

The stability of the laser output has also been investigated: after a warm-up period of about two hours, only a 4percent drift in the output power has been observed during a five hour period, and in the short term (under 1 minute), less than 0.8percent variation was noted.

3.4 Production of the Laser Probe

3.4.1 Beam focussing

The laser beam must be focussed so that it is smaller than the inter-element spacing of the integrated circuit which is to be probed, so a beam diameter of typically less than 10μm will be required.

* Spectra Physics model 132

† Scientifica and Cook model SLH/7.5

‡ United Detector Technology type 40X Optometer

The wavelength of light is the limiting factor in the focussed spot size (see Appendix 1), and since this is 0.63μm for the HeNe laser, a near diffraction-limited spot will be needed. For convenience the light spot should also be visible upon the i.c. surface, so a microscope system has been chosen to meet both needs; in one configuration the laser entered the microscope via an eyepiece[33] but the arrangement illustrated in figure 7 has proved to be the most convenient.

The beam focussing is achieved in two stages: an intermediate focus is formed by a low-powered lens then this is transformed by a second, stronger lens to produce the final small laser spot. The initial focussing is necessary to increase the beam divergence so that the aperture of the second lens is filled (to produce a diffraction-limited spot) and also to allow the image of the focussed beam and circuit surface to appear in focus together when viewed through the eyepiece.

In order to produce a small undistorted laser spot, the second focussing lens must be of good quality and have a large numerical aperture (see equation (A1.9), Appendix 1); in addition the aperture stop and working distance of the lens should be as big as possible (see sections 6.2.1 and 6.2.2) The lenses which have been used for this task are detailed in table 1; all but one are microscope objectives, the exception being a high-quality camera lens designed for use in mask-making equipment. This lens has a much larger working distance than the objectives of similar power.

The choice of the first lens is not so critical and the two whose properties are listed in table 1 have proved satisfactory. Beam expansion by the 43mm focal length lens was not quite sufficient to fill the aperture of any of the focussing lenses, but the slightly larger spot size was considered to be preferable to the power loss resulting from the over-expansion of the more powerful lens. This x 6 objective was used in conjunction with the Ultra-Micro Nikkor camera lens though, where the input aperture was much larger.

The combination of lenses most commonly used was the 43mm expander lens followed by either the x10 or x20 microscope objectives. This resulted in final spot diameters of 2.5μm and 1.5μm respectively.

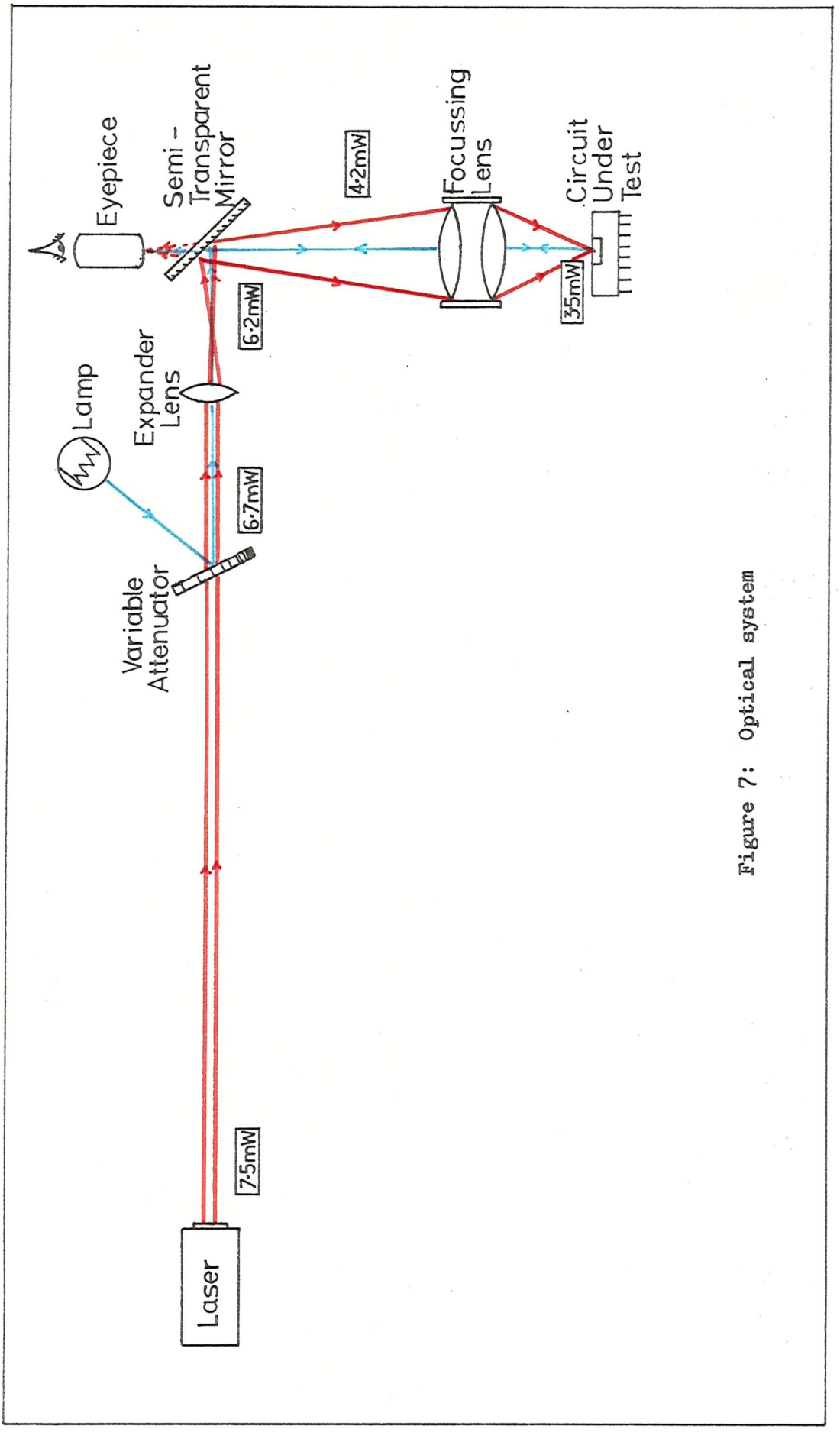


Figure 7: Optical system

Focussing lens	Numerical aperture	Working distance (mm)	Focal length (mm)	Optical tran-smission (%)
x5 Objective	0.15	17.0	11.7	93
x10 Objective	0.25	5.0	4.55	93
x20 Objective	0.50	1.2	1.14	83
x40 Objective	0.65	0.68	0.66	77
Ultra-Micro Nikkor lens	0.28	13.6	28.2	77

(a) Focussing lenses (λ=6328Å)

Expander lens	Numerical aperture	Aperture (mm)	Focal length (mm)	Optical tran-smission (%)
Biconvex	0.06	15.0	43.0	93
x6 Objective	0.12	7.5	12.0	91

(b) Expander lenses (λ=6328Å)

Table 1: Lenses used for beam focussing

3.4.2 Other aspects of the optical system

The light power is controlled by neutral density filters and a variable attenuator (density range 0 to 2, or 100percent to 1percent transmission), which is used both as a fine power control and as a reflector for the light from an external 60W lamp which illuminates the integrated circuit around the laser spot.

The chassis of a microscope has been used to hold the focussing lens and circuit under test. The expanding laser beam from the intermediate focus enters through the illumination porthole and is then deflected onto the second lens by a specially prepared front-silvered 70percent-reflecting mirror; this arrangement is used to reduce multiple reflections, to divert most of the power onto the final lens and prevent too much reaching the eyepiece. Some secondary images can be observed, but over 97percent of the total power is concentrated in the primary focus so these other 'probes' will not affect the operation of the overall system. In an effort to eradicate this problem, a small piece of aluminium has been tried in place of the mirror, but the distorted image which resulted when viewed through the eye-piece was found to be more of a drawback.

3.5 Laser Probing of a Silicon Integrated Circuit

3.5.1 Circuit preparation and mounting

All the integrated circuits probed by the laser beam have come from the manufacturer in a fully passivated and packaged form. The silicon chips are exposed to view by decapping the dual-in-line or TO-type packages, but in some cases it has been necessary to rebond the device in a new pack because of damage to the original. Often the chip is recessed well below the upper surface of the package, so a working distance of 1mm or more has to be allowed in order to bring it into focus; this factor has restricted the use of the higher-powered microscope objectives.

The circuit is mounted in a holder which is situated on the manual xy stage of the microscope, and connections to the power rails, clocks and conventional inputs and outputs are made by shielded cables. The light spot position on the chip surface is adjusted by moving the circuit and holder with the stage vernier controls.

3.5.2 Laser damage to the i.c.

An indication of the maximum power levels reached at each point in the optical system is given in figure 7. The power density is always well below the threshold level for damage to the optical components[34] but at the final focus a very large density is attained ($200 kW/cm^2$), so the physical interaction between this high energy beam and the silicon surface must be studied.

The temperature rise of the chip in the steady-state has been calculated by using a simple hemispherical model of heat distribution. From a point source, the thermal energy spreads a distance d, where

$$d = \sqrt{\frac{4 K \tau_t}{\rho C_p}} \qquad \ldots (3.10)$$

and K is the thermal conductivity ($1.5 W/cm^{\circ}K$ for silicon), τ_t is a thermal time constant, ρ is the density and C_p is the specific heat of the material[35]. This distance is calculated to be 15mm in silicon (assuming a time constant of 1 second), considerably larger than the integrated circuit dimensions. The radial heat flow in the steady-state is

$$q_r = - K.A. \frac{dT}{dr} \qquad \ldots (3.11)$$

where A is the area and dT/dr is the radial temperature gradient. Assuming a hemispherical distribution of heat, the thermal resistance R_j is found to be

$$R_j = \frac{1}{2\pi Kw} \qquad \ldots (3.12)$$

where w is the radius of the generation region. For the case of laser beam illumination with a power of 3.5mW and beam width of 0.75μm, the maximum temperature rise is calculated to be 5°C. The model does not take into account the fact that the chip is bonded down to a kovar header which will act as a heat sink, so this value should be an over-estimate. Measurements on a thermally insulated chip using a similar system have shown that the maximum temperature rise was 9.2 ± 1°C,[36] so the increase is not very significant. Reported results[37] on the irradiation of a silicon pin diode with ruby laser light (wavelength 0.69μm) have shown that a power of the order 50-200W is needed to produce any permanent damage to the device when long light pulses are used (approaching the limiting case of the steady-state assumption); in addition, observable characteristics such as craters and surface charring or a degraded diode response are always found once the damage threshold is crossed. No such surface damage or effect upon the device performance has been noted with the present system, confirming the calculation of a low temperature increase, so it may be assumed that the focussed laser spot will not damage the circuit under test and the method is truly non-destructive. The retina of the eye is more prone to damage though, so safety precautions have had to be carefully observed.

3.6 Light Beam Modulation

The intensity of the laser probe must be accurately controlled if it is to be used to inject time-varying information into an i.c. High speed operation is also required (1-10MHz) for integrated circuit testing applications, so an electro-optic modulator has been chosen for use in this system.

Other modulators include mechanical systems, such as rotating and oscillating blades or multi-faceted spinning mirrors[38] which can only operate up to about 10kHz and offer limited control of the light intensity pattern, and acousto-optic devices[39], which consist of a piezoelectric transducer bonded to a high quality, low optical-loss material and can operate up to about 1MHz. The solid state electro-optic modulator has an upper frequency limit of over 100MHz and is

cheaper than the acoustic wave version. The output intensity is approximately a linear function of applied voltage and can be easily synchronised with other equipment, so this system has proved to be very suitable for purposes of this study.

3.6.1 The electro-optic modulator

The basic element in an electro-optic modulator is the pockel cell, which is a crystal that undergoes an index of refraction change with the application of an electric field, i.e. it is birefringent. The incident light beam is split into two mutually perpendicular components which meet different indices of refraction within the crystal and therefore travel with different velocities, resulting in the introduction of a phase difference between the two parts at the output face of the cell. If the cell is positioned between crossed polarizers then the phase-modulated light can be converted into amplitude-modulated light, with the light transmission through the system controlled by the application of a voltage along the crystal axis. The modulator is shown schematically in figure 8(a).

The electro-optic effect may be described mathematically by[40]

$$\Delta(1/n^2) = r_p E + P_K E^2 \qquad \ldots (3.13)$$

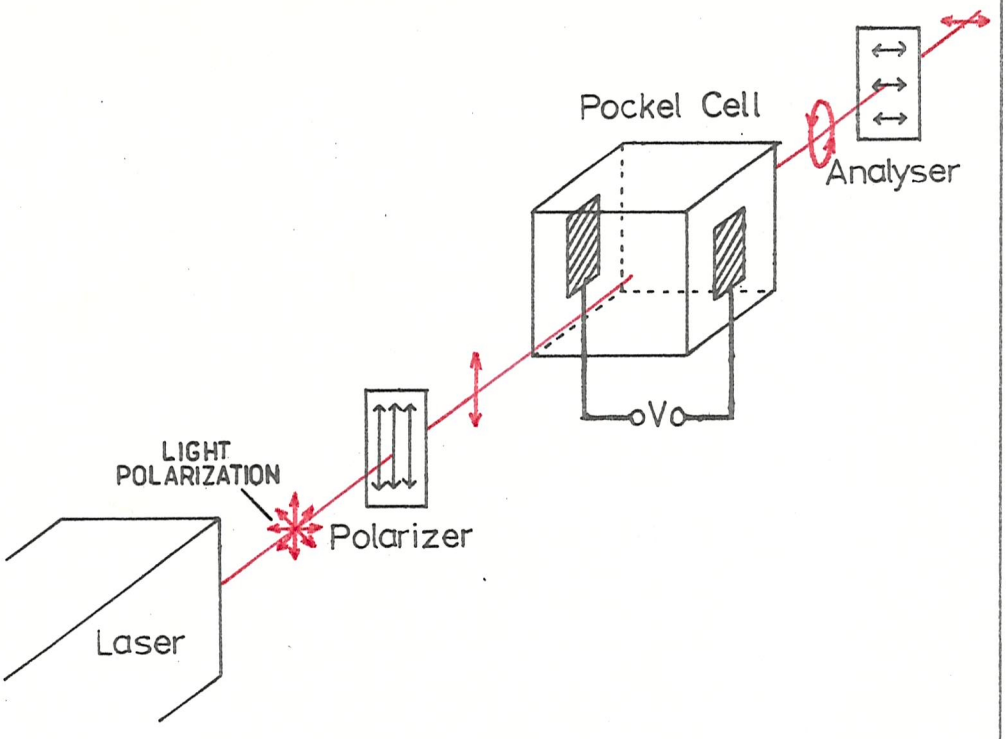
where n is the refractive index, E the applied field, r_p the linear electro-optic coefficient and P_K is a coefficient associated with the quadratic (Kerr) effect. The linear variation of the index term $r_p E$ is known as the Pockels Effect and will be the only one considered here. The operation of the modulator is based on two factors:

(i) a phase retardation is introduced between the two polarized components of the incident beam

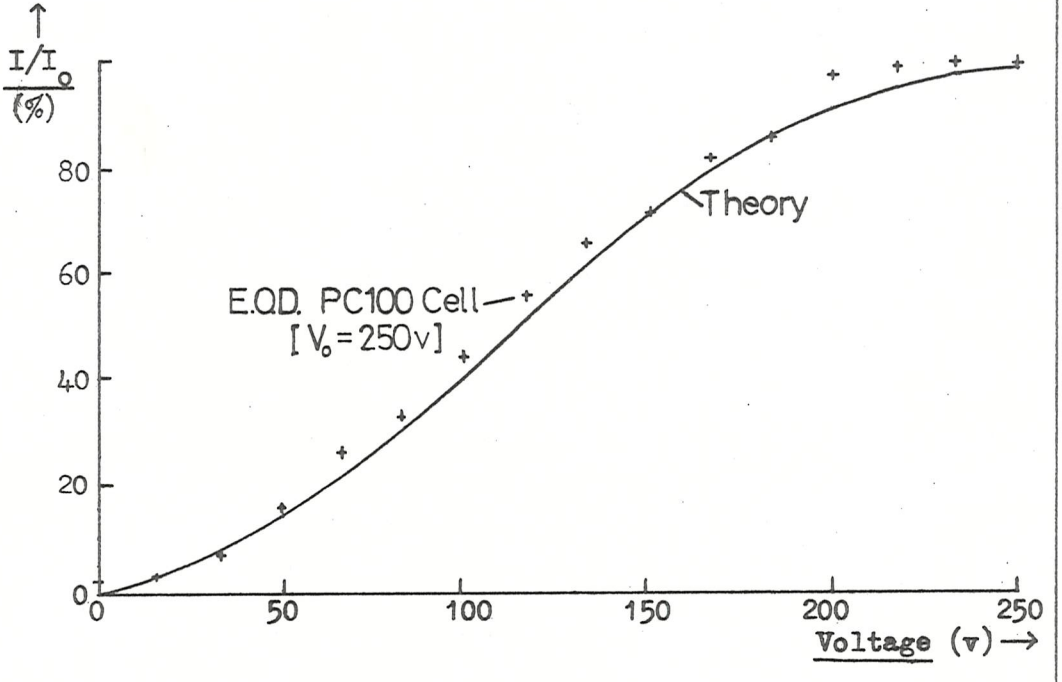
and (ii) the two waves interfere with each other.

The intensity of the light output is

$$I = I_o . \sin^2(\phi/2) \qquad \ldots (3.14)$$



(a) The electro-optic modulator



(b) Modulator intensity response

Figure 8: Electro-optic modulation

where ϕ is the total phase difference between the two waves traversing the electro-optic crystal and I_o is the incident light intensity; since the phase retardation in the linear Pockels Effect is proportional to the voltage, then

$$I = I_o \cdot \sin^2 \left(\frac{\pi}{2} \cdot \frac{V}{V_o} \right) \qquad \ldots (3.15)$$

where V_o is the voltage needed to produce maximum transmission ($I = I_o$), often called the half-wave voltage. The operating point on this characteristic can be shifted to the near-linear central region of the $\sin^2$ curve by the application of a d.c. bias, so that any superimposed time-varying voltage will be faithfully reproduced in the light-intensity domain.

Mechanical strains in the crystal can produce variations in the refractive index and in the birefringence. Changes in the former cause scattering of the incident light and distort the wavefronts and variations in the birefringence tend to reduce the degree of modulation and degrade the optimum optical bias[41]. By restricting the output aperture of the crystal, the modulator response can be improved by confining the light beam to the relatively strain-free central region of the crystal.

3.6.2 Experimental arrangement

A transverse modulator system has been used in the final arrangement, which includes an ammonium dihydrogen phosphate (ADP) pockel cell with a half-wave voltage of 250v.* This voltage is supplied by a high power video amplifier, which can operate up to 7MHz with a 10-90percent response time of 150nsec and also provide a d.c. bias of ±280v to the cell. The need for a separate polarizer is obviated by the vertically polarized laser output, but a calcite prism, mounted in a precision rotary unit, is used as the analyser.

The crystal alignment is highly critical, so a special pin-mounted gimbal cell holder has been built so that the crystal axis and light beam can be matched to within 0.1^o. A 1mm diameter pinhole

*Electro-optic Developments PC100 Pockel Cell and VLA30 video linear amplifier

has been used to restrict the output beam from the modulator in order to improve the response of the system; by careful adjustment, the extinction ratio (maximum to minimum transmission) can be raised from 30 to about 60. The modulator response is shown in figure 8(b).

3.7 The Laser Input

3.7.1 Electronic control system

The modulated light beam must be synchronised with the integrated circuit clocks and other time-dependent controls if it is to be used as an extra input. In the system shown in figure 9, this has been achieved by using the same clock generator to control both the circuit under test and the pockel cell driver. An intermediate pattern generation and bias adjusting network has also been used; this consisted of a 32-bit shift register with associated loading circuitry and a buffer stage to provide the 2v into 50Ω amplifier input. This test system configuration has proved useful for work with the various shift registers which have been probed with the laser, where the 'prog--rammable' 32-bit digital light input sequence (with '1' equivalent to the light ON and '0' to the no-light condition) has helped to determine the properties of the laser probe, but more sophisticated systems have had to be used for i.c.'s which use multi-phase clocks or need an analogue form of light input.

3.7.2 Overall system performance

From figures 7 and 9 it can be seen that the maximum laser powers incident upon the circuit surface are 3.5mW and 2.1mW for the unmodulated and modulated cases respectively. Using equation (3.7) and assuming a quantum efficiency of 70percent (see section 4.1), these values can be related to the photocurrent which would flow across a pn-junction lying under the incident light beam - numerically these currents are 1.25mA and 0.75mA.

The laser beam input can therefore supply a current of 0.75mA at a maximum repetition rate of 7MHz or in 0.2μsec pulses via a non-contacting, non-destructive probe of diameter 2μm.

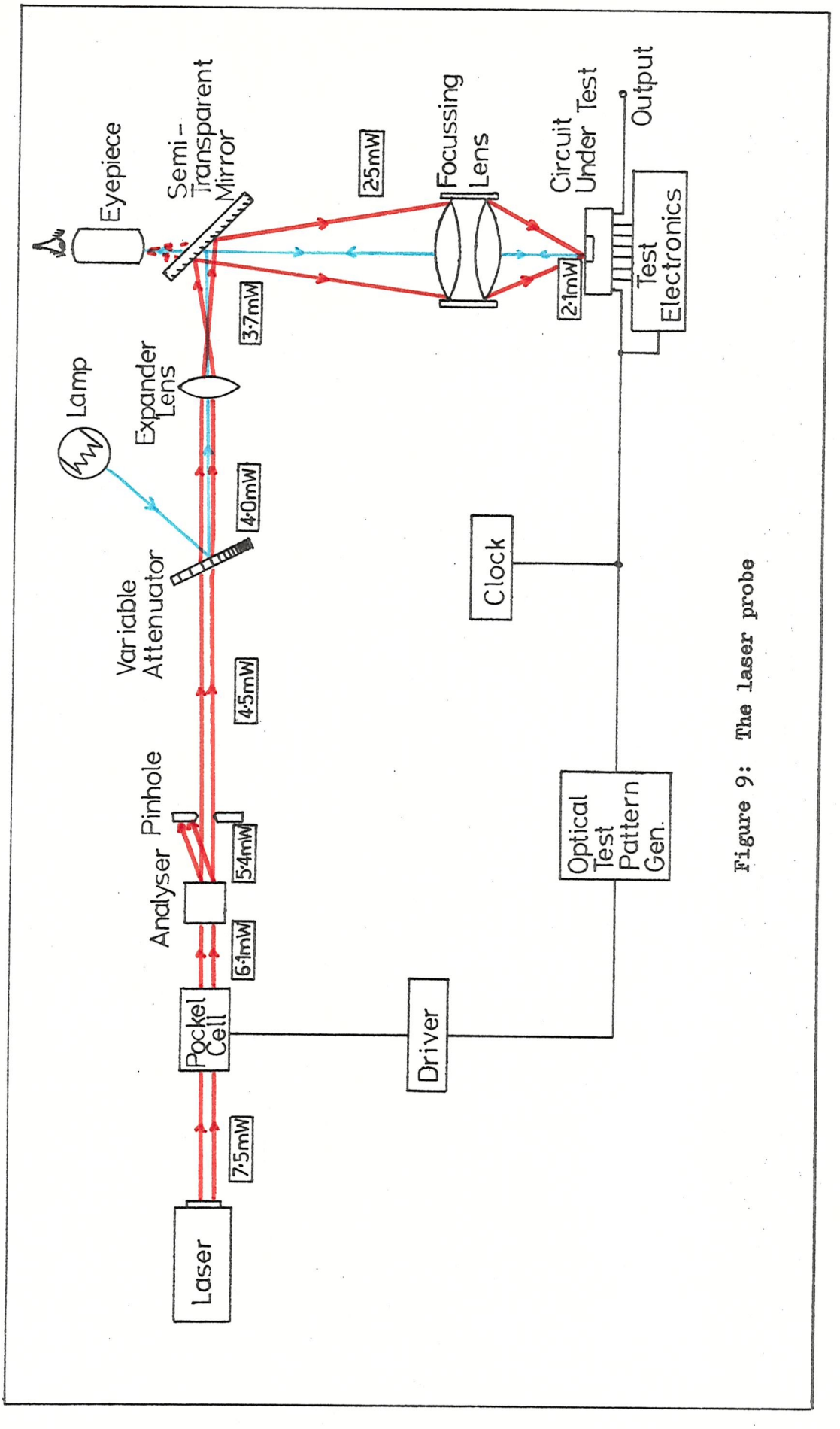
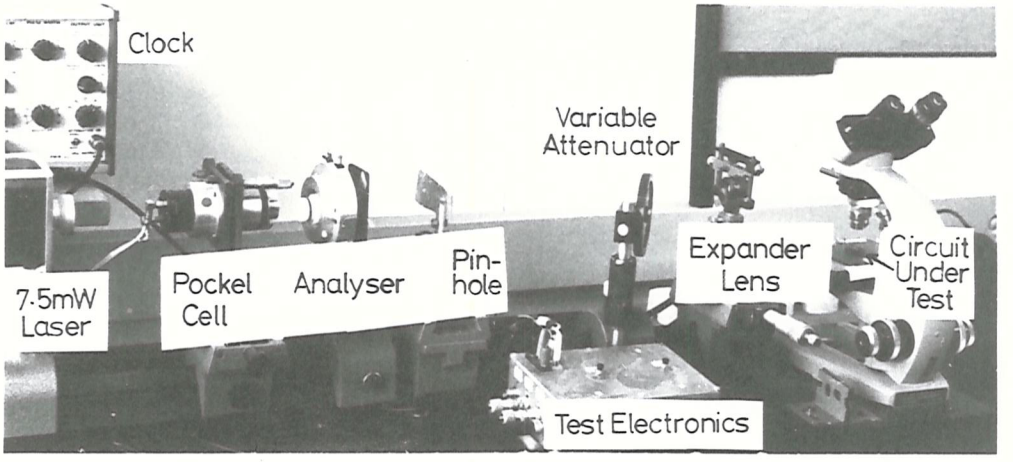
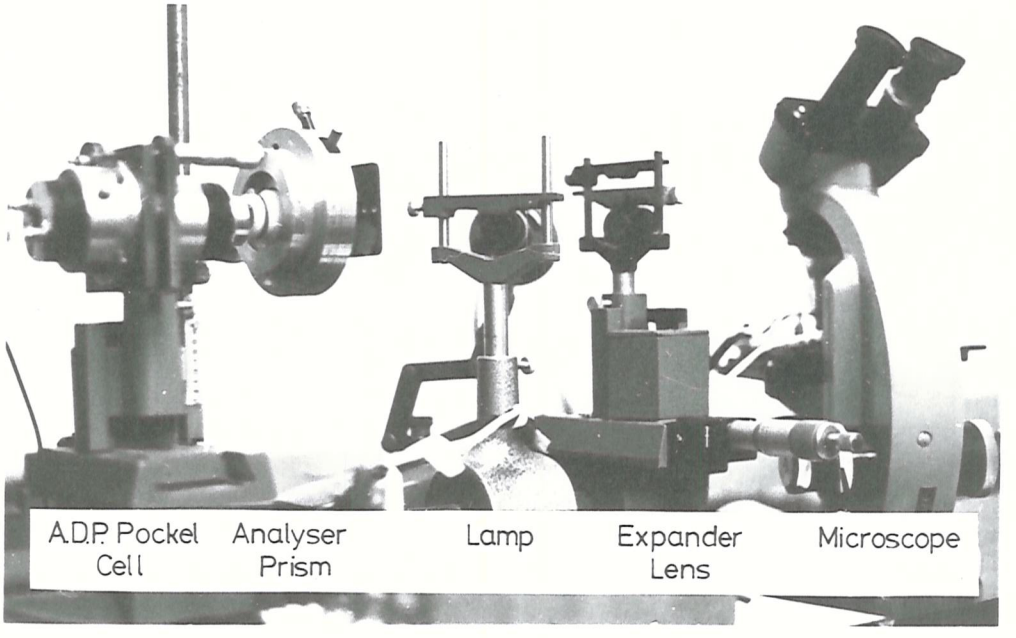


Figure 9: The laser probe

A photograph of the complete system is shown in figure 10(a), in which the external lamp and safety cover have been removed; the x5 microscope objective is used as the focussing lens and this can be seen just above the circuit under test. In the close-up of the optical system, figure 10(b), the pockel cell and analyser holders can be clearly seen, and in addition the accurate expander lens movement apparatus (section 4.3.2) is also visible. A glass plate has replaced the variable attenuator in order to show the 60W lamp.



(a) Overall view



(b) Modulator and optical system

Figure 10: Experimental arrangement

CHAPTER 4

LASER BEAM EVALUATION OF A SEMICONDUCTOR

- Quantum efficiency
- Carrier injection levels
- Diffusion length
- Lifetime
- Semiconductor substrate characterization

4. LASER BEAM EVALUATION OF A SEMICONDUCTOR

4.1 Quantum Efficiency

4.1.1. Introduction

For a given incident light power, the magnitude of the photocurrent flowing across an illuminated pn-junction is dependent upon the quantum efficiency (the number of electron-hole pairs generated per incident photon) and the photon energy, as described by equation (3.7) which is repeated here:

$$I_{sc} = \frac{P}{h\nu} \cdot q \cdot \eta \qquad \ldots(4.1)$$

therefore in S.I. units, $\eta = \frac{I_{sc}}{P} \times 1.96 \times 100\%$ $\qquad \ldots(4.2)$

for the helium-neon laser light.

The value of quantum efficiency (η) is determined by several factors, which include reflection, absorption and interference of the light in the surface layers or at the various interfaces and also device parameters such as junction depth and diffusion length.

The position and size of the focussed laser beam can play an important part in the deter--mination of the effective quantum efficiency. This is illustrated in figure 11 which shows the variation in photocurrent as a very small laser spot of constant power is moved along the upper surface of the semiconductor and across a pn-junction. A maximum value is reached when the beam is directly over the junction, but on each side of this position some of the generated carriers are lost by recombination. If the laser 'spot' overlaps the depletion layer, then

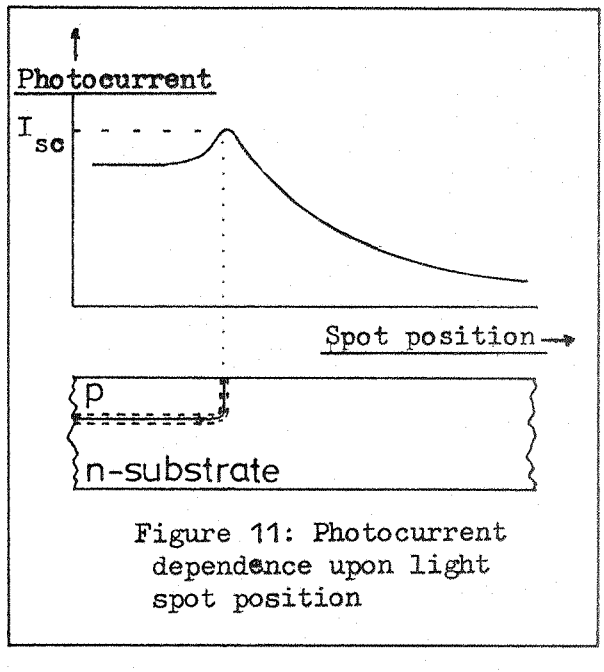


Figure 11: Photocurrent dependence upon light spot position

again not every one of the photo-carriers is collected by the junction, even when the centre of the generation region is coincident with the junction edge. Therefore for measurements of quantum efficiency, care must be taken to accurately position the beam and use as small a laser beam width as possible.

4.1.2 Results

Measurements of quantum efficiency have been made on a variety of devices, and in each case a reverse-biassed pn-junction which is directly accessible from contact pads has been used as a photocurrent monitor. A 3v bias has been found to be necessary to prevent the self-biassing of the junction in the forward direction, which arises because of the voltage drop in the substrate; if not prevented, this would result in the measured photocurrent being too low (see figure 5).

The values of quantum efficiency which have been measured are listed in table 2: each quoted result refers to a separate device, and the average for each class is shown bracketed. The minimum laser power needed to produce a photocurrent of 0.5mA has been measured, from which the value for η has been calculated. No dependence of this value upon the light power level in a 10μW-1mW range has been noted, and the choice of focussing lens did not have a significant influence upon the readings, except when the smallest x5 objective was used - here the larger diameter laser spot caused an apparent reduction in quantum efficiency by up to 6percent; for the other lenses, less than 0.5percent variation was noted.

The majority of the devices tested have been M.O.S. i.c.'s but some bipolar types have been studied. Three conclusions can be drawn from the results obtained:

(i) the variation in quantum efficiency from one region to another region on the same device is small

(ii) between different devices of the same type there is also little change in the results

(iii) there is a correlation between the quantum efficiency values and the circuit manufacturer.

I.C.family	Manufacturer	Device type	Quantum efficiency (%)
M.N.O.S. p-channel Al-gate	General Instruments	SS-6-1032	69.6,72.0 (70.8)
		SL-6-4025	67.0
		SL-6-4032	66.1,62.8 (64.5)
		SL-6-2064	69.3,63.9 (66.6)
		DL-6-2128	62.8
		AX-6-8591	73.5,69.3 (71.4)
		Q2-2	72.8
M.O.S. p-channel Al-gate	Plessey	ML232B	81.5,79.6,76.5 82.3 (80.0)
M.O.S. p-channel Si-gate	Mullard	GYN111	66.6,63.5 (65.1)
		GYN141	67.0,64.8 (65.9)
		GYQ101	72.7,76.1,76.5,74.0, 75.3,73.0,76.9 (74.9)
C.M.O.S.	R.C.A.	CD4012	81.4
		CD4013	68.0
Bipolar	Fairchild	709C	70.7,70.3,76.1 (71.5)
	Southampton University	142 ABAB	60.9,63.3,55.6,51.4, 55.0,55.6,57.5 (57.0)
		166 JGSJCW	54.2,53.5 (53.9)
Bipolar (n-sub)	Southampton University	166 JGSJCW	68.1,71.5,71.1 (70.2)

Table 2: Quantum efficiency

From measurements on a single SS-6-1032 circuit with seven accessible pn-junctions, a 2percent difference between the values of η measured at each site was found, and similarly from the results of tests performed on seven GYQ101 memories, only a small (3percent) variation was noted. This close agreement is to be expected since in each case the manufacturing process should be identical and so the factors influencing the quantum efficiency should also be the same; in addition it is probable that devices in the same family, for example the G.I. static shift register series SS-6-1032, SL-6-4025, SL-6-4032 and SL-6-2064, will also have similar quantum efficiencies.

Different manufacturers will not use the same processing methods, so variations in passivation layer thickness or junction depth for example will be found, and this could explain the significant differences in values of quantum efficiency, such as the 80percent for Plessey M.O.S. and 65percent for General Instrument devices. Similarly a modification of the processing steps used by one producer can also have a large effect: this has been noted for two sets of 166 JGSJCW devices in which a change from 0.46μm to 0.52μm oxide thickness produced a corresponding change in quantum efficiency from 53percent to 70percent.

All the measured values of η lie in the range 55-85percent, but differences of this magnitude are not very significant for the application of integrated circuit testing, where the power requirements can vary over many decades; however in the following section an attempt is made to predict the quantum efficiency theoretically, which will be useful for circuits in which it cannot be directly measured.

4.1.3 Analysis

Interference, reflection and absorption of light in the silicon dioxide layers and at the air-oxide and oxide-silicon interfaces are expected to be the most significant factors which govern the value of the quantum efficiency, but photo-carrier loss mechanisms in the bulk semiconductor may also play an important part, as shown schematically in figure 12(a).

The theoretical analysis of this problem will be treated in two parts, where first the optical parameters and secondly the effects

inside the semiconductor are considered. It will be assumed that only a negligible fraction of the photon energy is absorbed by free carriers or excitons for illumination at this laser wavelength, so that each photon reaching the silicon will produce one electron--hole pair.

Details of oxide thickness, junction depth and doping profile are known for two devices, and measurements from these have been used to justify the theoretical calculations. Both were 166 JGSJCW bipolar circuits fabricated at this university: one was pink in colour when viewed vertically and had an oxide thickness of 0.46μm, a p-type substrate and an epitaxial layer 6μm deep; the other was a green colour (thickness 0.52μm) but it had an n-type substrate. The diode used for quantum efficiency measurements was formed between a p-type diffusion (junction depth 2.6μm) and the n-type 'collector' material, and the values for η were found to be 53percent for the 'pink' device and 70percent for the 'green' one (table 2).

(a) Absorption, reflection and interference

The oxide thickness on each circuit tested will be less than 2μm[42], and since extrapolation from results quoted by Wolf[43] gives a penetration depth in the oxide at the laser wavelength of 1mm, absorption losses here can be ignored.

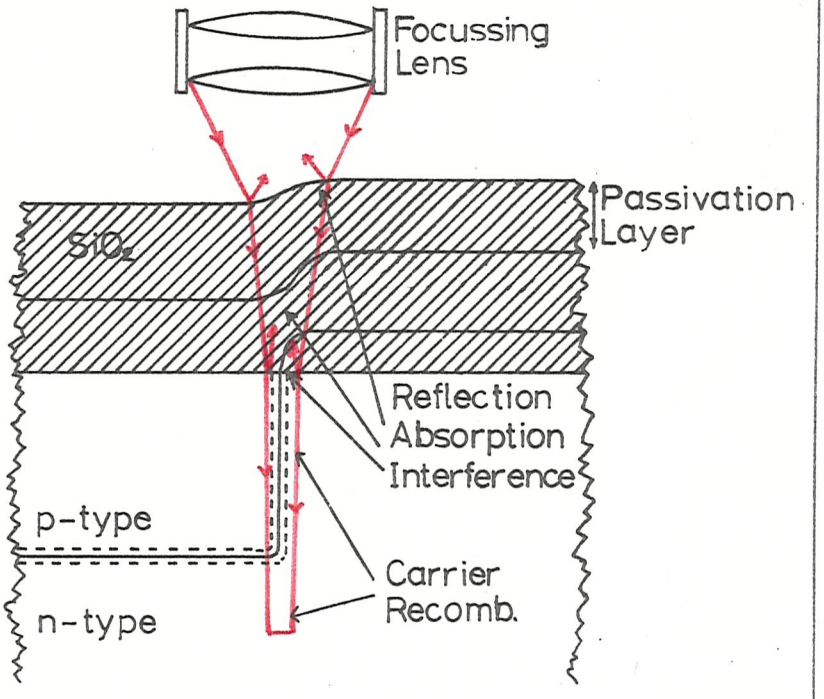
Reflection will be significant at both the air-oxide and oxide--silicon boundaries. The reflectance, R, at an interface between two non-absorbing dielectrics can be determined from the Fresnel relationships which are given in Appendix 2: for a simple air-silicon dioxide system with light incident normally, the intensity reflectance is calculated to be 13percent; and for light polarization parallel to the plane of incidence, the reflectance drops as the angle of incidence is increased, reaching zero at the Brewster angle (55°) then rising again for larger angles.

Measurements using the laser, which is polarized in this plane, have been taken with three devices to determine the variation of reflectance with angle of incidence for an air-oxide-silicon system.

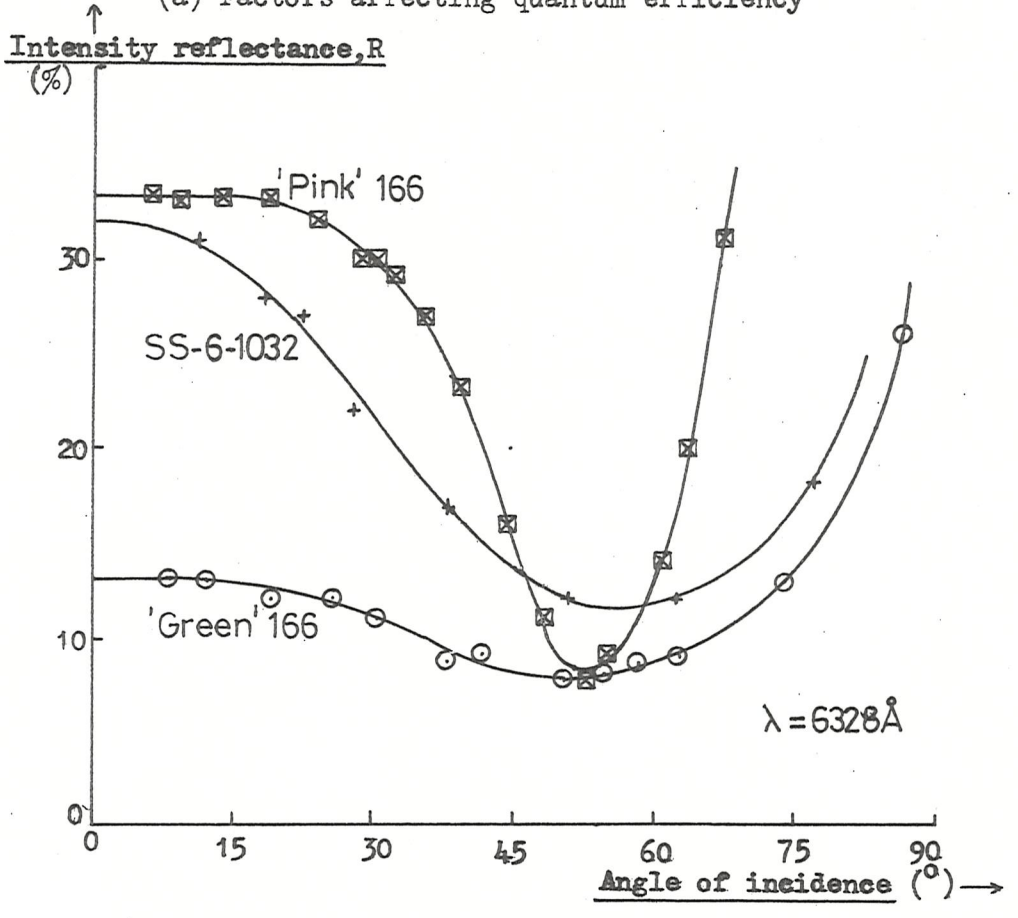
The laser (assumed to be producing a parallel beam) is directed at a metal-free oxide area, and the reflected light intensity measured as a function of incident beam angle with the results as shown in figure 12(b). The devices tested were the pink and green 166's and a passivated shift register cirucit, which was dull grey in appearance. A dip in the response around the oxide Brewster angle is found in each case, but the magnitudes of the reflectance are significantly different from the simple air-oxide prediction, and each other. This can only be explained by a consideration of the interference between the various reflections at the two boundaries, a factor which is strongly dependent upon oxide thickness. It has been shown in Appendix 2 that in an air-oxide-silicon system with a zero angle of light incidence, a plot of the transmission into the silicon (or alternatively total reflectance) shows a periodic variation as the oxide thickness is increased (figure 12(c), solid line). However the lenses used to focus the beam do not produce a single angle of incidence, so this periodic response will be 'smeared' out, particularly for thick oxide layers and large numerical aperture lenses. A simple calculation has been made to estimate the net transmission/oxide thickness variation which would be obtained if the x20 microscope objective was used (half angle 30^{o}), and this is the dotted line shown in figure 12(c). For large oxide thickness, the transmittance is tending to a limit of 79percent.

The overall reflectance of the two 166 devices has been measured, so a check upon the theoretical curve can be made. For oxide thicknesses of 0.46μm and 0.52μm, the theory predicts a reflectance of 32percent and 11percent, which compares very well with the measured 33percent and 13percent respectively (assuming no absorption).

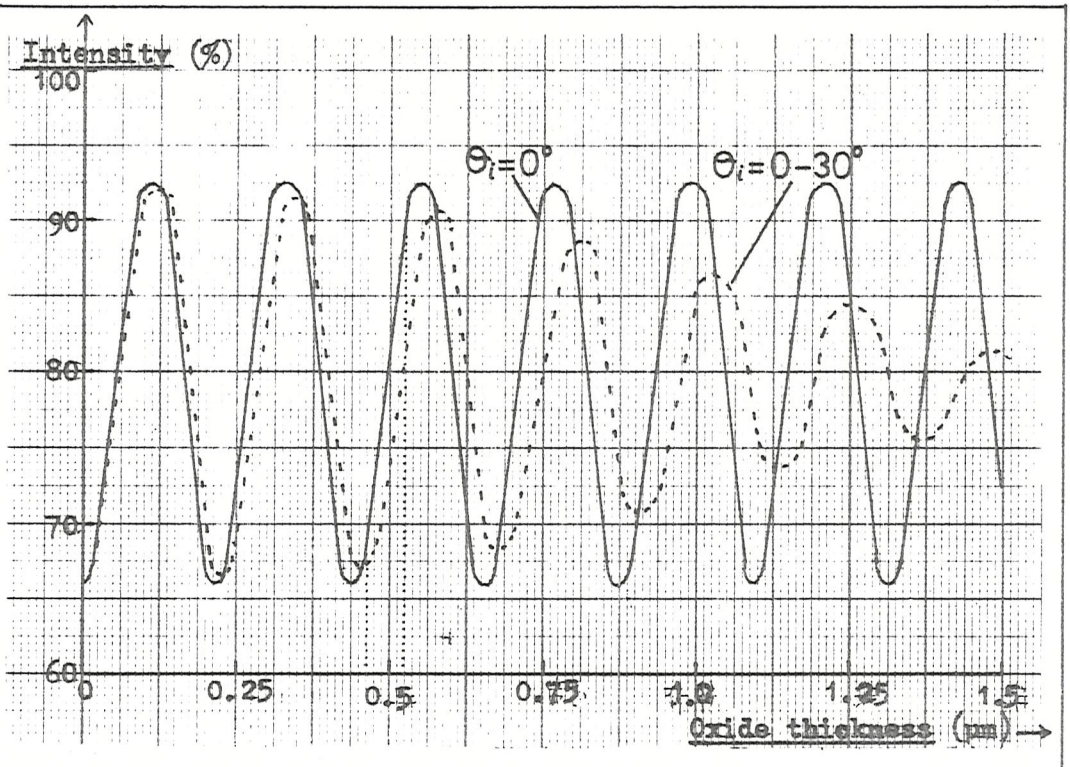
The proportion of the incident light intensity which reaches the silicon is therefore heavily dependent upon the thickness of the oxide layer, but this could be calculated if the depth of oxide is known or can be determined from its colour. However transmission losses alone do not give rise to the quantum efficiency value, and so effects inside the semiconductor must also be studied.



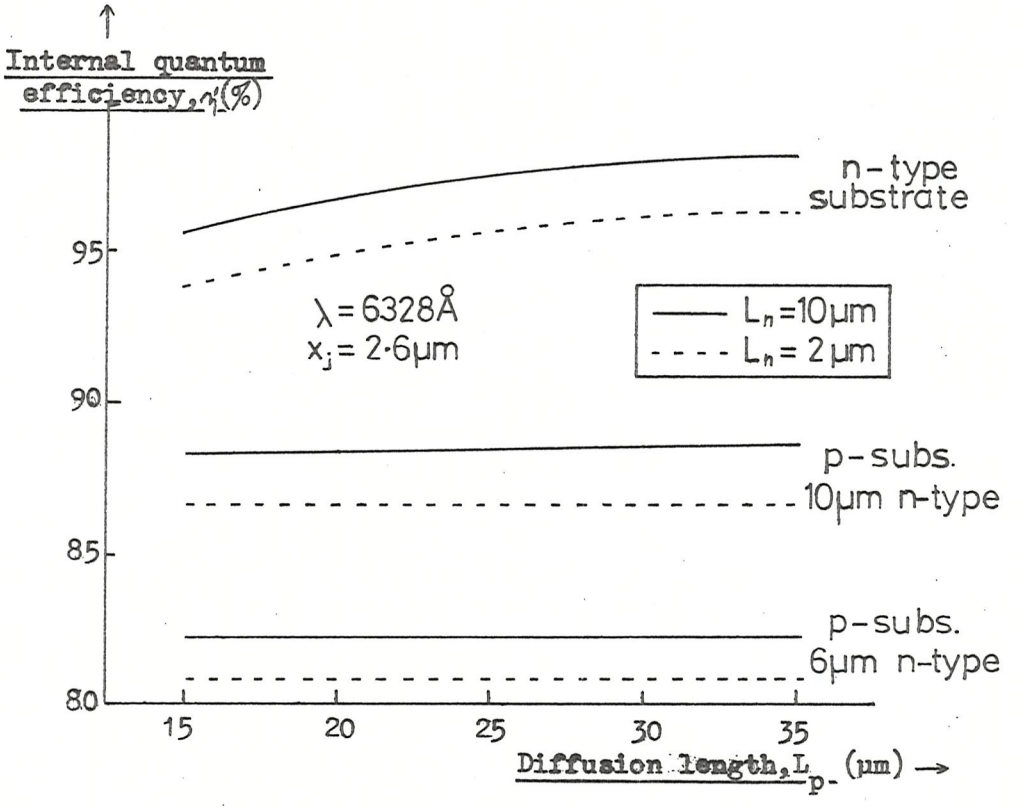
(a) Factors affecting quantum efficiency



(b) Surface reflectance of three integrated circuits



(c) Transmission of light through a thin oxide layer



(d) Internal quantum efficiency

Figure 12: Quantum efficiency

(b) Losses in the semiconductor

An internal quantum efficiency, η', is defined to be the number of carriers which cross the pn-junction per each incident photon in the semiconductor. Its value will be influenced by surface recombination velocity, junction and penetration depths, carrier diffusion lengths, doping profile with associated drift field and the substrate thickness, but a one-dimensional analysis of the problem has been made[44] from which it has been found that only the penetration, junction and epitaxial layer depths are significant. Three sets of curves have been calculated (figure 12(d)) assuming a junction depth of 2.6μm and radiation of 6328Å: diffusion length has been plotted as the variable, and the cases of n-type substrate and p-type substrate with epitaxial layer of 6μm and 10μm have been chosen to illustrate the influence of a second pn-junction below the surface. The pink 166 device had a 6μm deep n-type layer, and the diffusion length is known (see section 4.3.2), so a value for η' of 82percent is predicted; similarly for the 'green' device η' is expected to be 95percent. The contribution of the η' factor to the total quantum efficiency is therefore much less than the losses from interference and reflection.

It has been assumed that all the photon energy which reaches the bulk semiconductor is used to generate electron-hole pairs at this particular wavelength. The validity of this assumption can be roughly checked by comparing the overall quantum efficiency predicted from the above analyses with actual measurements for the two 166 circuits. For the p-substrate pink device, the true value of 53percent is very close to the calculated 56percent and similarly for the n-substrate chip, 70percent was measured and 75percent predicted. Thus it seems probable that within the accuracy limits of the present experiments, all the photon energy is used to generate free carriers.

The theoretical treatment of quantum efficiency does give a reasonable agreement with measured results in two cases, but it is possible that if any dielectric layers as well as the oxide are used in the processing then the model will not give the correct answer. However to a first approximation, for thick passivation layers the

quantum efficiency will tend towards a value of about 77percent for n-substrate devices or 65percent for 6μm deep epi-layer on a p-substrate (with thicker layers giving a higher η value). These relatively small differences will not be very significant in the context of integrated circuit testing but an average value of 70percent will be assumed throughout this work in all calculations involving photocurrent in which the true value has not been measured.

4.2 Carrier Injection Levels

Approximately 70percent of the incident photons produce electron--hole pairs inside the silicon semiconductor, so by using a very powerful light source it is possible that the injected carrier concentration could be greater than the substrate doping concentration, and high level injection conditions (conductivity modulation of the semiconductor) would prevail. A knowledge of the laser powers necessary to reach this state and the boundaries of the region over which it occurs is therefore essential if measurement of minority carrier diffusion length and lifetime is to be made with the laser probe. These parameters vary as a function of injection level[45] (see Appendix 3(a)) and experimental measurements[46] have shown that the lifetime can change by a factor of up to 20 as the injection conditions are altered. The transition between the high and low level injection limits has been found to take place over a two-decade range of injected carrier concentration, centred on the initial substrate concentration level; for carrier concentrations outside this range, the lifetime and diffusion length remain constant at either the high or low injection value.

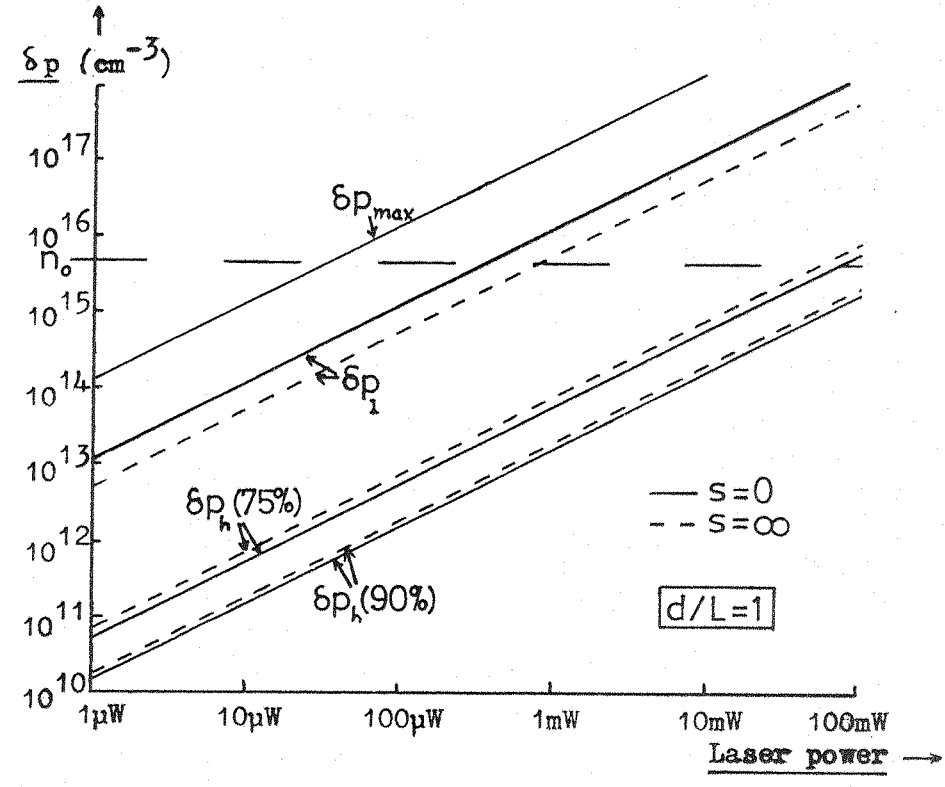
Delineation of the injection levels as a function of incident light power is complicated by the fact that the carrier generation occurs in a finite volume close to the illuminated portion of the semiconductor surface, whose dimensions are determined by the penetration depth in the material and the gaussian laser beam profile, and away from this source the excess carrier concentration decreases as a function of distance and diffusion length. As a result, a localised high injection regime could be formed around the generation region, but at a pn-junction some distance away, low injection conditions may still hold.

Theoretical analysis of this problem has been based upon the published work of Berz and Kuiken [47]. Their treatment is more comprehensive than other analyses [48,49] and considers both a finite generation volume (not simply a point or line source) and the effects of non-zero surface recombination. Only slight modifications are needed to adapt this theory to the case of laser beam carrier-generation, and experimental measurements give satisfactory agreement with its predictions. Mathematical details are given in Appendix 3(b) : three simple approximations to the shape of the generation volume have been attempted and compared with a measured value of injected carrier concentration in order to obtain the best analytical solution of the differential equations.

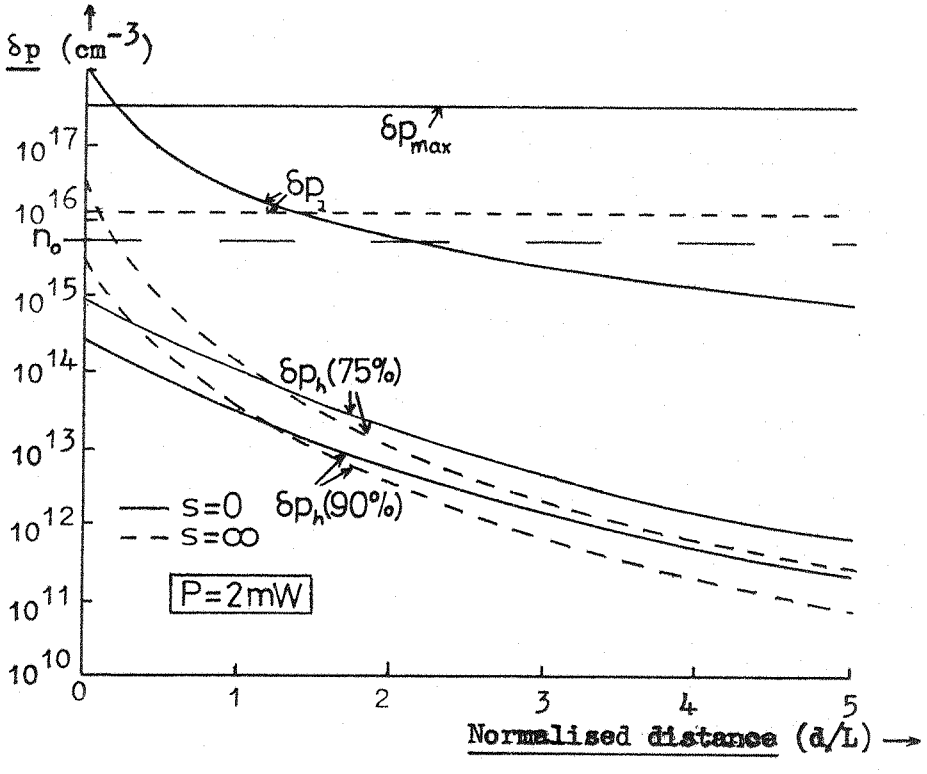
The results obtained from an application of the theory are shown in figure 13. Three regions of excess carrier concentration have been defined:- δp_{max} is the maximum carrier concentration which is found within the generation volume, δp_l is the low level injection boundary, i.e. if δp_l is less than the substrate doping concentration at a certain point, then low injection conditions apply at that point, and similarly δp_h is the high injection limit where a substrate doping level less than δp_h indicates high level carrier injection. Two definitions of the high injection region have been used (see Appendix 3) so two δp_h values have been shown and these are denoted $\delta p_h(75\%)$ and $\delta p_h(90\%)$.

Device parameters which apply to the SS-6-1032 shift register have been used to calculate the family of curves shown in figure 13 but these are typical of most of the devices tested. The substrate doping concentration (n-type) is 5×10^{15} cm^{-3}.

The first graph shows the variation of excess carrier concentration with laser beam power, where the pn-current-collecting junction has been assumed to be one diffusion length away from the 2μm wide laser spot. At the junction under these conditions, low injection applies for laser powers of below 0.4mW and high injection for powers above 100mW.



(a) Dependence of carrier concentration upon laser power



(b) Carrier concentration at a distance d from the source

Figure 13: Injected carrier density

The second curve, figure 13(b), shows the variation of the injection level boundaries as a function of laser spot position. The laser power is constant at 2mW, producing a maximum excess carrier concentration of 3×10^{17} cm^{-3}, and low injection conditions can be seen to hold for laser beam-junction separations of greater than two diffusion lengths but high injection is never reached, even when the generation region is close to the junction.

The effects of a change in surface recombination velocity are included in these plots, where the solid lines indicate the results obtained for the case of no surface recombination and the dashed line shows the other extreme, infinite recombination velocity. Typical values of 1-10cm/sec have been quoted[50], so the solution for zero surface recombination velocity will probably apply, but this could lead to an overestimate of the size of the high-injection region.

Both the lifetime and diffusion length have been measured using different laser powers in the range 20μW-2mW (see also sections 4.3.2 and 4.4.2), and no power-dependent variation of these parameters has been observed. Some deviation would be expected if the injection conditions close to the collecting pn-junction changed, so it appears that low injection conditions always prevail for laser powers upto 2mW, independent of distance. The theoretical prediction that the low injection region boundary lies two diffusion lengths away from the junction for a 2mW beam therefore is not confirmed by these measurements; the definitions of the low and high injection regions are probably too stringent and the effect of a finite surface recombination velocity could also help to explain this discrepancy. However the theoretical limits for power levels and beam-junction separation have been observed in all measurements of diffusion length and lifetime to ensure that the low-level values are determined.

4.3 Diffusion Length

4.3.1 Elementary theory

Injected minority carriers diffuse a characteristic distance L, the diffusion length, into the semiconductor before they recombine, so as the separation between the laser spot and collecting pn-junction is increased, the photocurrent flowing across the junction will decrease as a function of this distance and the diffusion length. Very close to the junction, typically within one or two microns, the built-in field arising from the impurity gradient will become significant and the simple carrier diffusion will be disturbed. For this reason, the analyses presented in this section will only apply for laser spot-junction separa--tions of greater than about 2μm, when this field component can be ignored.

The continuity equation describing carrier motion in a semiconductor is, for n-type material,[50]

$$\frac{\partial(\delta p)}{\partial t} = D.\nabla^2(\delta p) - \frac{\delta p}{\tau} + g + \mu_p.E.\nabla(\delta p) \qquad \ldots(4.3)$$

where δp is the excess hole concentration, g is the generation rate per unit volume, μ_p is the hole mobility, E the electric field, D the ambipolar diffusion coefficient and $1/\tau$ is the recombination rate.

In the steady state with no field term, the equation reduces to

$$D.\nabla^2(\delta p) - \frac{\delta p}{\tau} + g = 0 \qquad \ldots(4.4)$$

A simple solution can be found if the following assumptions are made: the semiconductor is semi--infinite with hole diffusion in one dimension only, and the material is uniformly illumin--ated on one side with all photons absorbed very close to the surface (see figure 14.). Then,

$$\delta p(x) = \delta p(0).\ \exp(-x/L) \qquad \ldots(4.5)$$

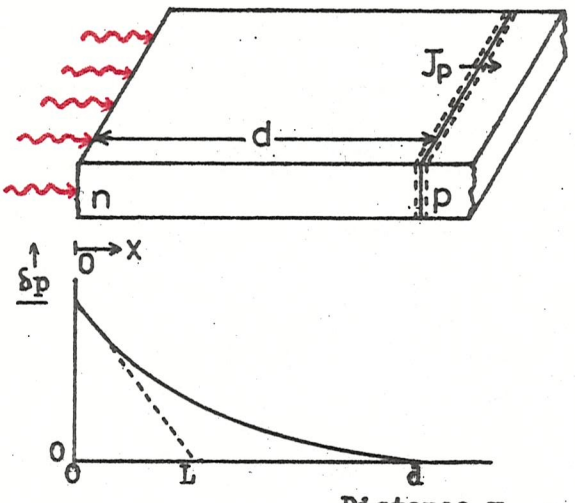


Figure 14: 1-D steady-state hole diffusion

where $\delta p(0)$ is the excess hole concentration at the illuminated surface (x=0).

The current collected by a pn-junction of area A positioned at x=d is given by

$$I = A.q.D_1.\left[\frac{\partial \delta p(x)}{\partial x}\right]_{x=d} \qquad \ldots(4.6)$$

where the effective diffusion coefficient, D_1, is defined in Appendix 3(d). Hence

$$I(d) = I(0).\ \exp(-d/L) \qquad \ldots(4.7)$$

where I(0) is the current measured when the carrier source and pn-junction are coincident, or

$$I_{ph}(d) = I_{sc}.\ \exp(-d/L) \qquad \ldots(4.8)$$

where I_{ph} is the photocurrent collected at a distance d from the illuminated area and I_{sc} is as defined in equation (4.1).

4.3.2 Measurements

An accessible pn-junction has to be used to measure the photocurrent for diffusion length determinations, and in addition this junction should be well separated from other junctions (by more than about 100μm) in the region over which the experiment is performed, otherwise the carrier diff--usion away from the generation region could be disturbed (see section 4.3.4). These restrictions normally mean that the only suitable photo--current-collection junction is formed by the diffusion linking an input pad to the rest of the circuit; such a situation is illustrated in figure 15.

The laser spot is positioned over the junction edge and then moved away in a perpendicular direction, and the photocurrent collected by the reverse-biassed junction is then simply measured as a function of the junction edge - laser spot separation. The circuit could be moved with respect to the stationary laser beam, but a more accurate beam movement system has been used: the expander lens is moved across the unfocussed beam, resulting in a deflection of the spot on the integrated circuit surface; this lens could be moved in 10μm steps, so after focussing repeatable sub-micron movement of the beam was possible.

The result of one such experiment is shown in figure 16(a) where the laser spot power was maintained at 1.8mW. A simple exponential decay forms the major part of the response, but close to the junction there is a deviation because of the finite spot size and carrier extraction by the built-in field at the junction. The simple theory outlined in the previous section does predict just such a response, but a more rigorous analysis, using realistic boundary conditions, will be presented in section 4.3.3 in order to explain this result.

A variation of this measurement technique has been used to ensure that low level injection conditions prevail at the junction throughout the experiment, otherwise the effective diffusion length would vary with laser beam position (see section 4.2). The laser power was adjusted after each change in position so that the photocurrent collected by the junction remains constant. For a 15μA current, laser beam powers in the range 36-510μW have been used to obtain the result shown in figure 16(b).

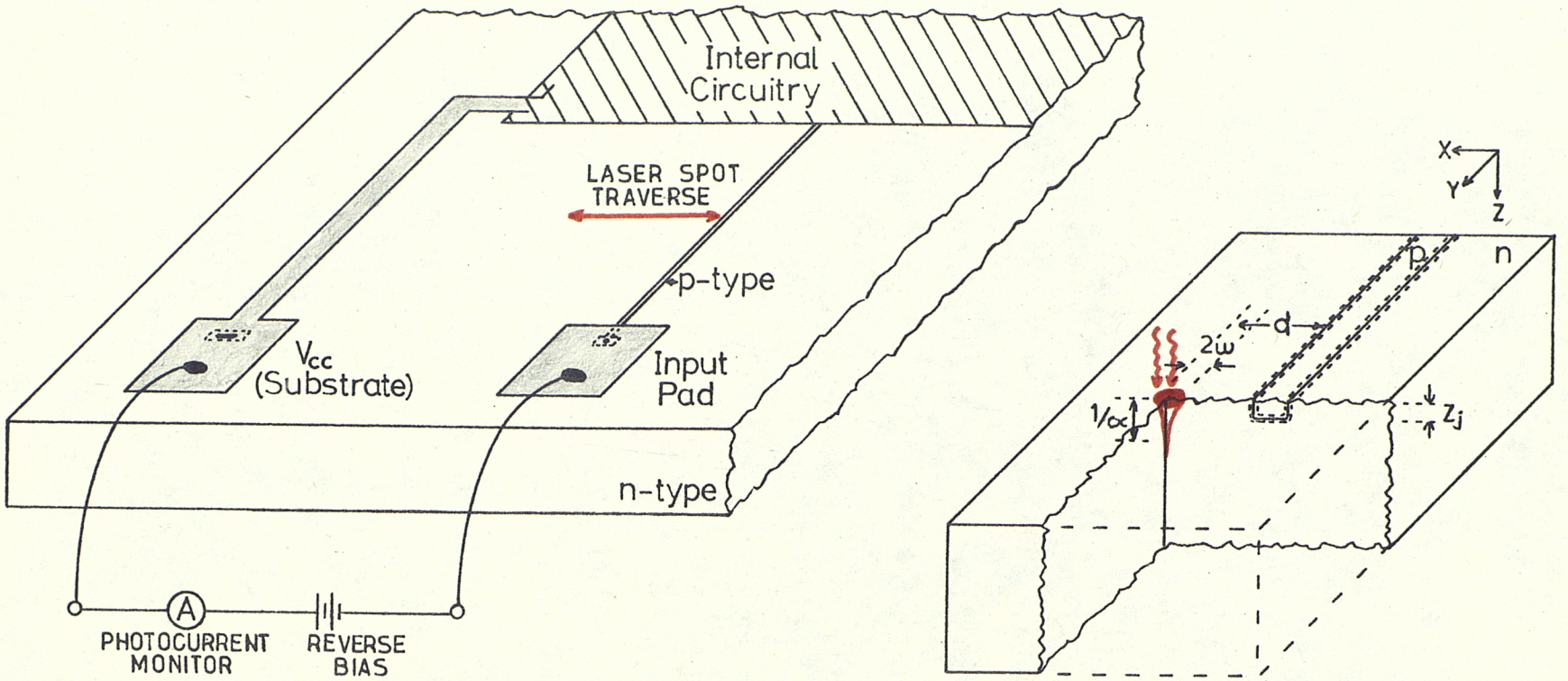
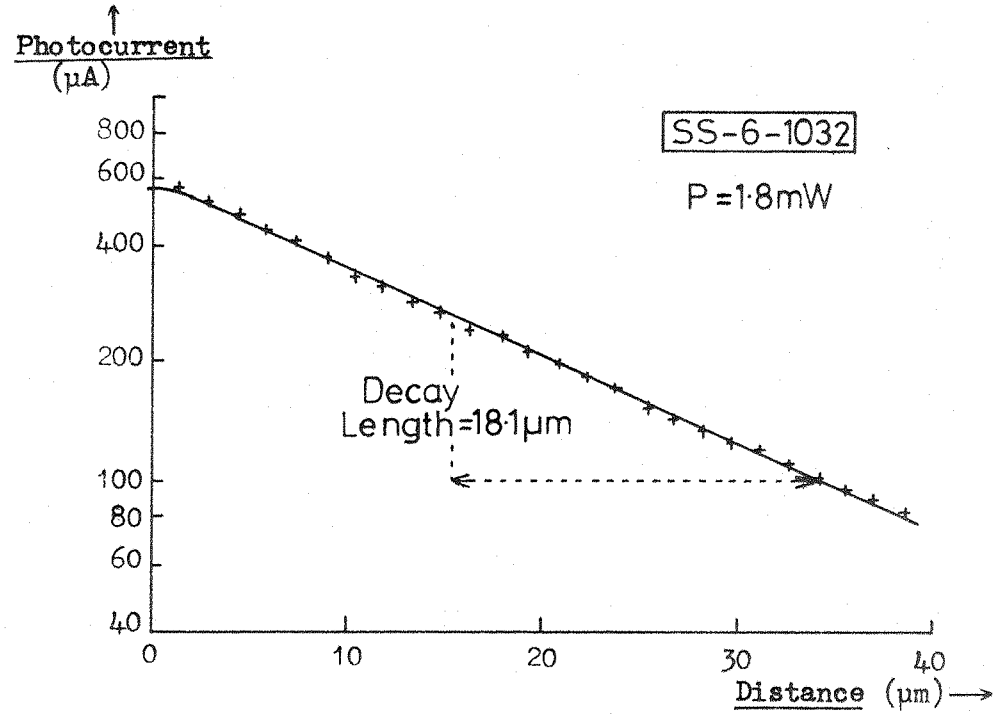
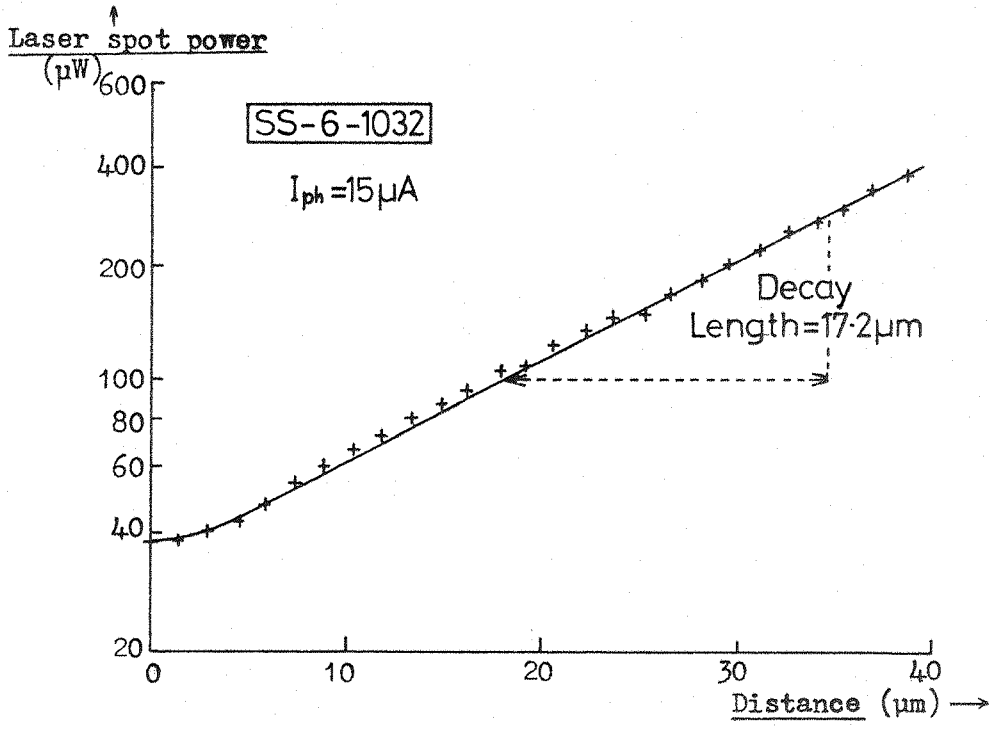


Figure 15: Diffusion length measurements



(a) Photocurrent measured for a laser power of 1.8mW



(b) Laser power required to maintain a photocurrent of 15μA

Figure 16: Variation of photocurrent with distance (readings)

According to the injection level theory (figure 13), these conditions will ensure that only low level injection will occur, but the value of the decay length obtained in this experiment is equal to the one previously found when using a fixed beam power of 1.8mW (figure 16(a)). Thus even with this powerful beam positioned close to the pn-junction, low injection conditions must still apply.

In a third experiment upon the same device (a SS-6-1032 M.O.S. shift register), the light beam path was chosen to cross two aluminium interconnections (see figure 17). The photocurrent is again measured as a function of beam-junction separation for a fixed laser power, but the effect of the finite spot size can be clearly seen as its path crosses the opaque metal regions. An exponential decay is again noted, with the same slope as the two previous cases.

This simple exponential relationship between photocurrent and beam position is a feature of all the measurements of this type which have been made using a variety of different devices. A summary of these results is given in table 3; the readings have been repeated many times in some cases, so a statistical treatment of the values of decay length has been performed. The decay length is defined as the distance over which the photo--current drops by a factor 'e' and will be used extensively in the following sections to compare the results from exponential-type graphs.

Readings taken using different pn-collecting junctions on the same device or with different devices of the same type did show some slight variation in the values of decay length (less than 10percent) but this is indicative of the accuracy of the measurements rather than evidence of spatial variation in diffusion length.

4.3.3 Analysis of the results

A simple exponential relationship between the photocurrent collected by a pn-junction and the distance of the laser beam from the junction edge was predicted in section 4.3.1, but to reach this conclusion, various assumptions were made, some of which will not strictly hold for the experimental situation described in the previous section. The essential

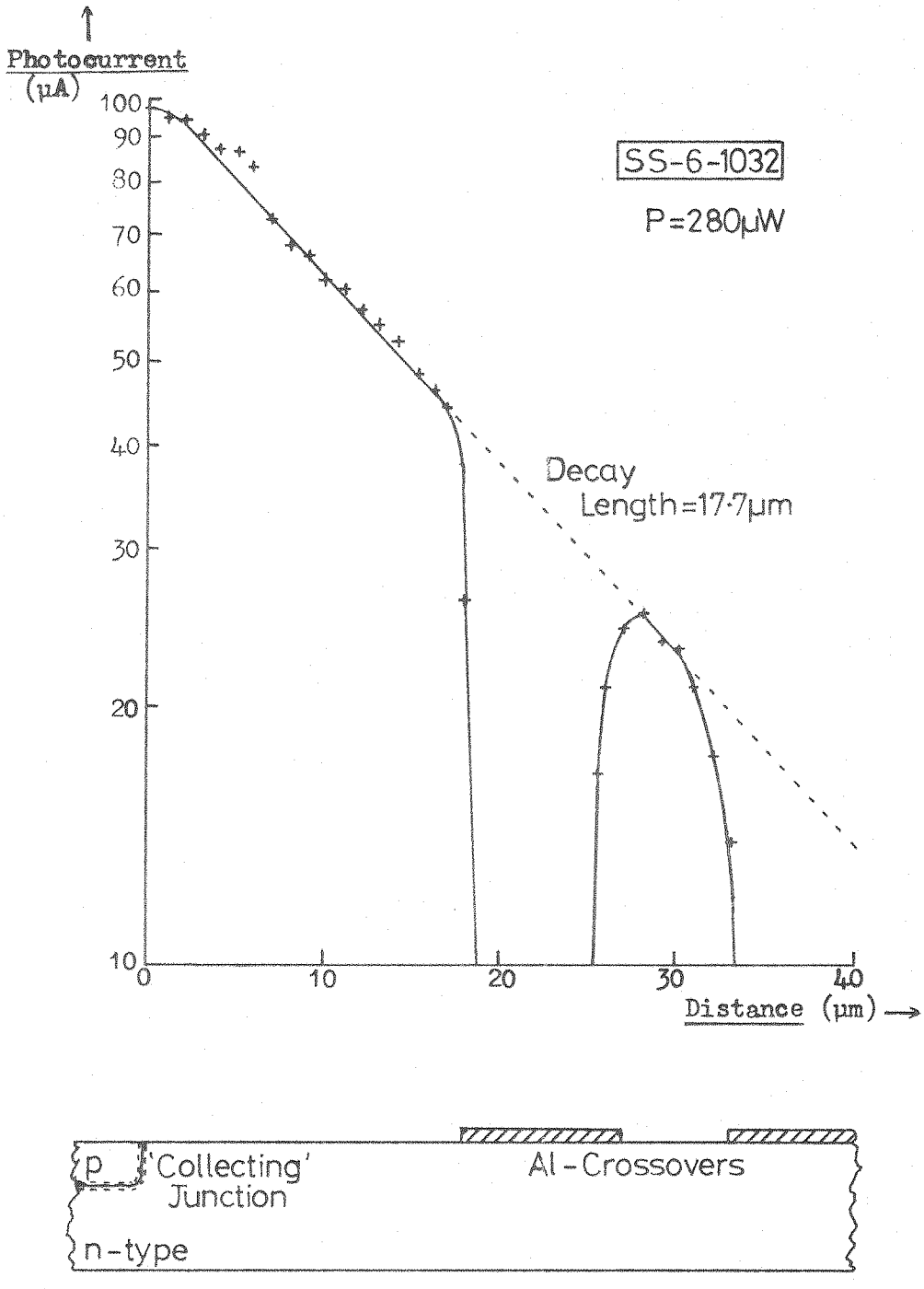


Figure 17: Laser spot traverse over aluminium interconnections

I.C.family	Manufacturer	Device type	Decay length (μm)	Number of readings
M.N.O.S. p-channel Al-gate	General Instruments	SS-6-1032	17.6 ± 2.2	14
		SL-6-4032	17.4 ± 0.4	8
		DL-6-2128	7.8 ± 0.45	8
		Q2-2	17.5 ± 1.4	19
M.O.S. p-channel Al-gate	Plessey	ML232B	40.7 ± 2.9	7
M.O.S. p-channel Si-gate	Mullard	GYN111	33.6 ± 3.0	11
		GYN141	16.1 ± 1.0	4
C.M.O.S.	R.C.A.	CD4027	19.1 ± 1.6	6
Bipolar	Southampton University	142 ABAB	16.7 ± 2.0	4
		166 JGSJCW	7.5 ± 0.6	4
Bipolar (n-sub)	Southampton University	166 JGSJCW	21.7 ± 0.8	15

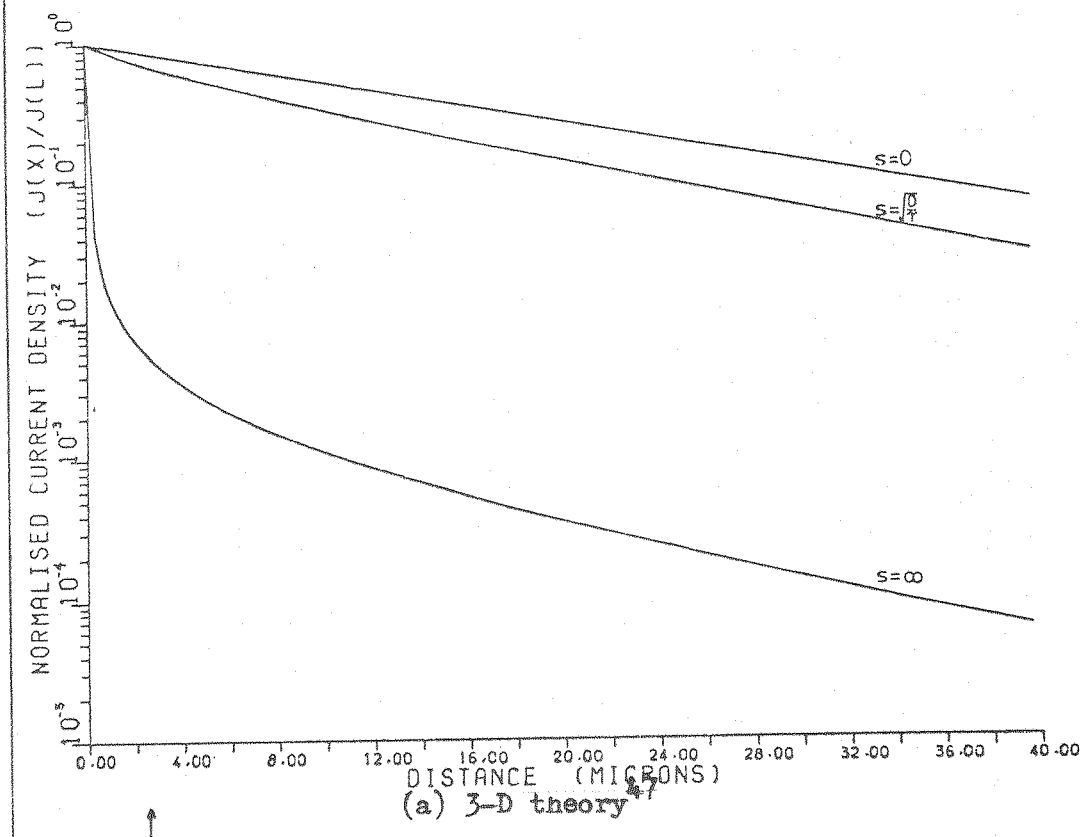
Table 3: Measurements of diffusion length

differences are that in practice the carriers are generated in a small localised region and diffuse in all directions, and also the long shallow collection junction lies very close to the surface and its presence may influence the carrier motion.

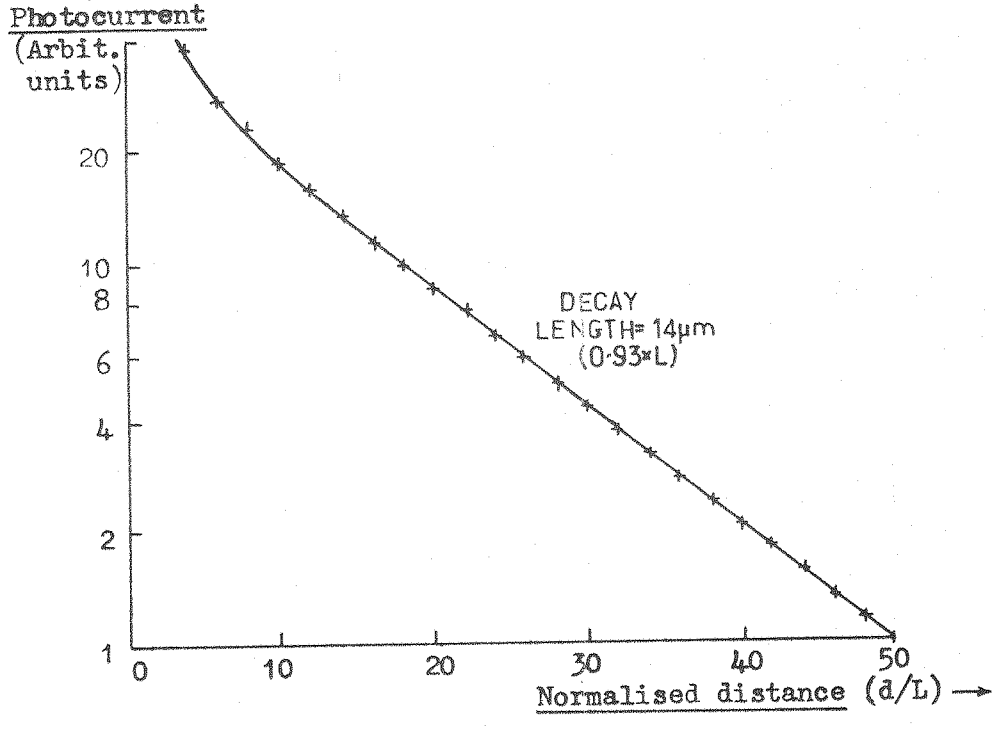
The 3-D continuity equation can be solved analytically if cylindrical symmetry is assumed, and a Bessel-function dependence of the photocurrent upon beam position results for the case of a line of light and point contact,[51] but this type of relationship has not been found experimentally here. The paper by Berz and Kuiken[47] treats a similar problem to the present case, and details are given in Appendix 3(d). The results of their analysis are shown in figure 18(a) where three different values of surface recombination velocity have been assumed, i.e. s = zero, infinity and the diffusion velocity $\sqrt{D/\tau}$. An exponential decay of photocurrent as a function of distance is found in the first of these cases, with decay length equal to the diffusion length (chosen to be 15μm); for non-zero surface recombination, there is an initial steep drop in the collected photocurrent as the generation region is moved away from the junction, but for separations greater than about one diffusion length, an exponential decay of 0.85 x L and 0.9 x L for $s = \infty$ and $s = \sqrt{D/\tau}$ respectively is found.

A computer simulation of the carrier distribution has also been attempted in order to determine the relationship between collected photo-current and laser spot position. Results from a 3-D model assuming a point carrier generation source and a semi-infinite semiconductor have shown that in all directions the number of excess carriers decays exponentially as a function of diffusion length[36], but a 2-D case has also been simulated, in which the finite laser beam size and perturbing effect of the collector junction upon carrier motion have been included. Details are given in Appendix 4(a), and the result shown in figure 18(b). Again a diffusion length of 15μm has been assumed, and an exponential decay of 14μm is predicted, except for beam positions close to the junction where the finite spot size becomes significant.

No second-order effects are apparent in this response so it seems probable that a fully comprehensive 3-D programme would also produce the same result, i.e. a simple exponential decay with the photocurrent dropping by a factor 'e' in a distance equal to the diffusion length. This is



(a) 3-D theory [47]



(b) 2-D computer simulation

Figure 18: Variation of photocurrent with distance (theory)

supported by the analytical predictions, so therefore the values of decay length listed in table 3 are equivalent to the diffusion length of holes in the n-type substrate.

Electric fields in the semiconductor have been assumed to be negligible, except close to the junction itself, but if this was not true the effective value of diffusion length could be significantly altered. A one-dimensional analysis leads to the following result[52]:

$$L_e = \frac{1}{\frac{1}{2L}\sqrt{\left(\frac{E}{E_c}\right)^2 + 4} \pm \frac{|E|}{2LE_c}} \qquad \ldots(4.9)$$

where the effective diffusion length, L_e, is dependent upon the orientation of the electric field (E) and the direction of light beam movement. The field term E_c has been called the critical field, and its value given by:

$$E_c = \frac{kT}{qL} \qquad \ldots(4.10)$$

This prediction has been confirmed by measurements upon a 166 JGSJCW device, when a field of 15V/mm produced a change of measured diffusion length from 22μm to 13μm for an 'upfield' and 33μm for a 'downfield' movement of the beam[36]. However using the normal measuring system, no such dependence of the exponential photocurrent decay upon the beam path has been found, and the field generated by the reverse bias supply is at least an order of magnitude below the critical field, so field effects can be assumed to be negligible.

Quite a large variation in the values of diffusion length has been found when different types of circuit have been studied (see table 3), even though the substrate material used by each manufacturer is expected to be similar in type. An individual company will probably use identical starting material for different products, so in these cases close agreement between the measured diffusion lengths is expected: this has been noted for the General Instruments static M.N.O.S. class of circuits.

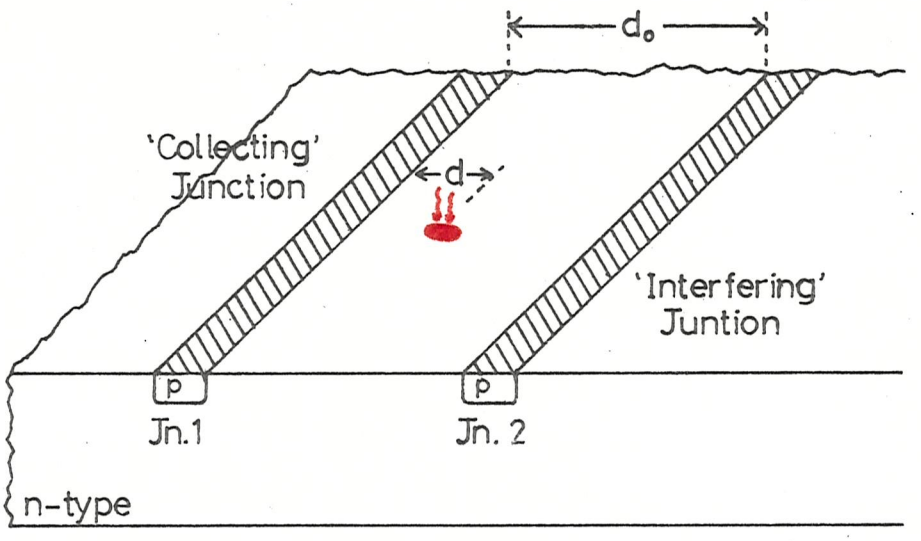
The laser probe method of measuring diffusion length could be used to find evidence of spatial variation, but the region over which readings

can be taken is limited to the periphery of the circuit in the proximity of the accessible junctions. However the technique is easy to perform (unlike the electron beam induced current (EBIC) methods where a vacuum chamber is required[53]) and the measurements can be taken after all the processing has been completed and without the need for special purpose--built test sites[54].

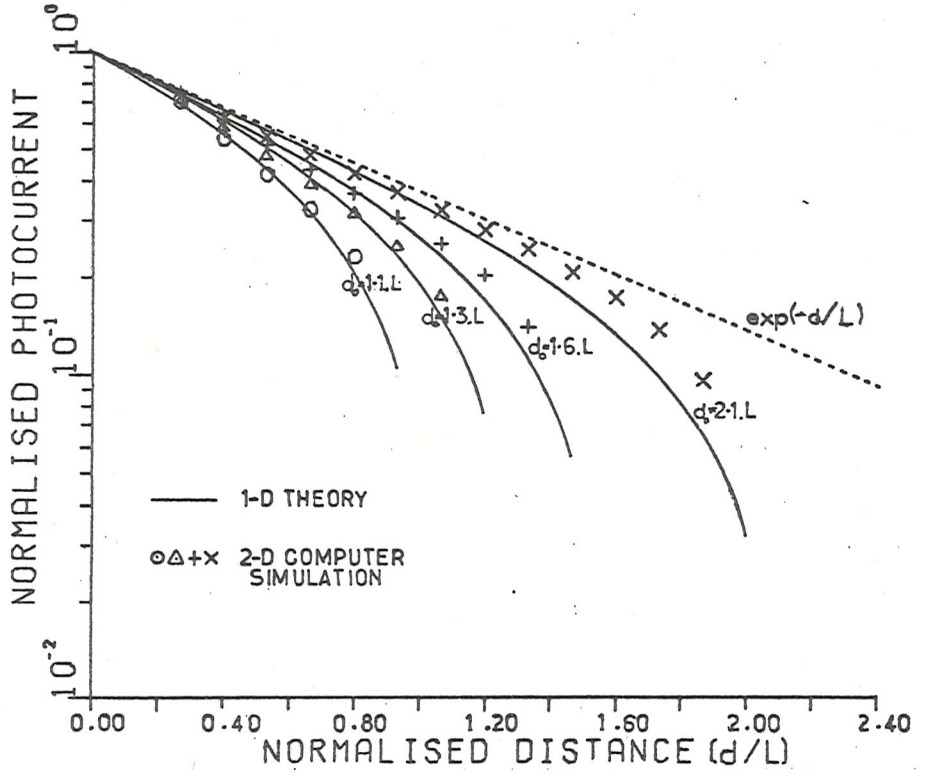
4.3.4 Interference from other junctions

Diffusion length measurements have been taken on two types of 166 JGSJCW circuit. One had a thick n-type substrate and the other p--substrate with a 6μm deep epitaxial layer, and, as shown in table 3, the measured values of diffusion length were 22μm and 7.5μm respectively; for this reason, diffusion length measurements cannot be taken in diffused regions, because the layer is only a few microns deep. The difference in these results can be explained if the influence of the pn-junction 6μm below the surface upon the carrier distribution is taken into consideration, since many of the excess carriers produced by the laser are swept down to the p-type substrate rather than diffusing close to the surface and being collected by the normal pn-junction photocurrent monitor. This result demonstrates the influence of two junctions upon carrier motion, an effect which must be analysed if the interaction between the generated carriers and an integrated circuit (where many junctions lie close together) is to be understood or if meaningful diffusion length measurements are to be taken when the collecting junction is not well removed from other diffused regions.

A two junction system is shown schematically in figure 19(a), and for the case of the laser beam positioned between them, the excess carrier distribution has been studied both by using a 1-D theoretical analysis (see Appendix 5) and with a 2-D computer model of the surface (Appendix 4(b)). A comparison between these solutions is presented in figure 19(b): four different junction separations (d_o) in the range 1.1 x L to 2.1 x L have been assumed, and the graph shows the variation in photocurrent collected by one of these junctions as the laser spot is moved a distance d away from it (the distance values are normalised with respect to diffusion length). The effective diffusion length can be seen to increase as the distance between the two junctions increases, and the asymptote (dotted line) is a simple exponential decay in a distance equal to the diffusion length, which is the



(a) Schematic diagram



(b) Analytical prediction of photocurrent collected by Jn.1

Figure 19: Interference between two pn-junctions

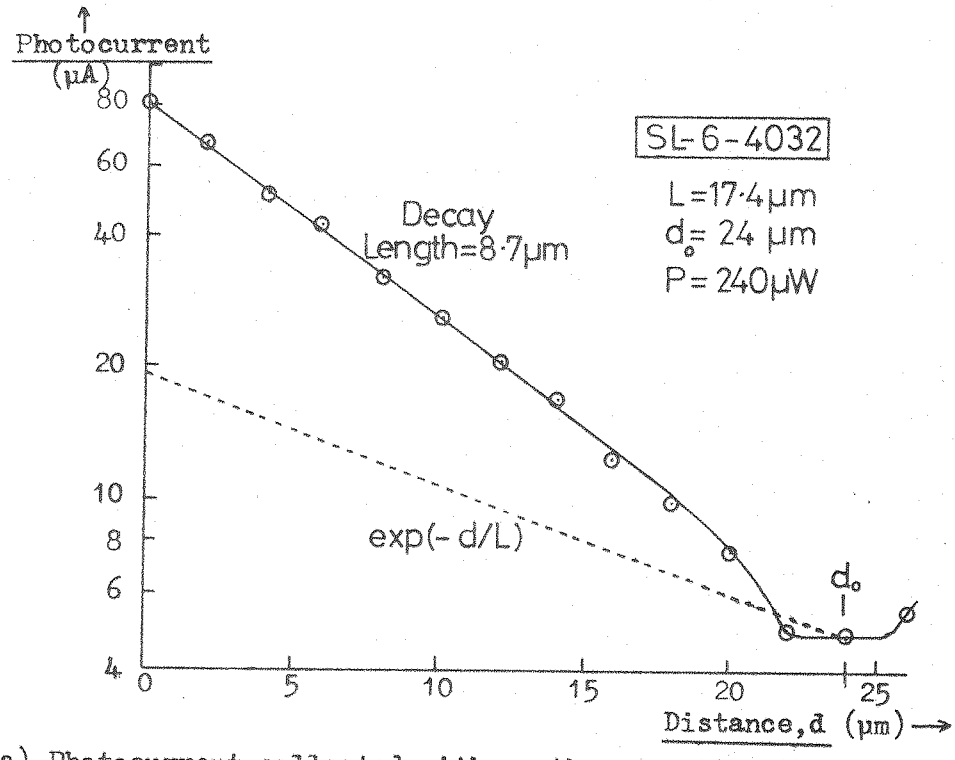
response that is expected for an isolated junction. Thus for inter--junction separations of more than about three diffusion lengths, the influence of the second junction can be ignored for practical purposes; this criterion has been used in all diffusion length measurements to ensure that the decay lengths were equal to the true diffusion length.

An example of two junctions close together is encountered in the static shift register cell of the SL-6-4032 circuit, where the gap between them is 24μm (the diffusion length has been previously measured to be 17.4μm). A plot of the photocurrent collected by junction number 1 as a function of laser beam position, d, is shown in figure 20(a); in this case neither junction was directly accessible so the photocurrent has been calculated from its effect upon the circuit action (see section 5.4.1.1). The dashed line again indicates the result which would be obtained if the collecting junction was at least three diffusion lengths away from all others.

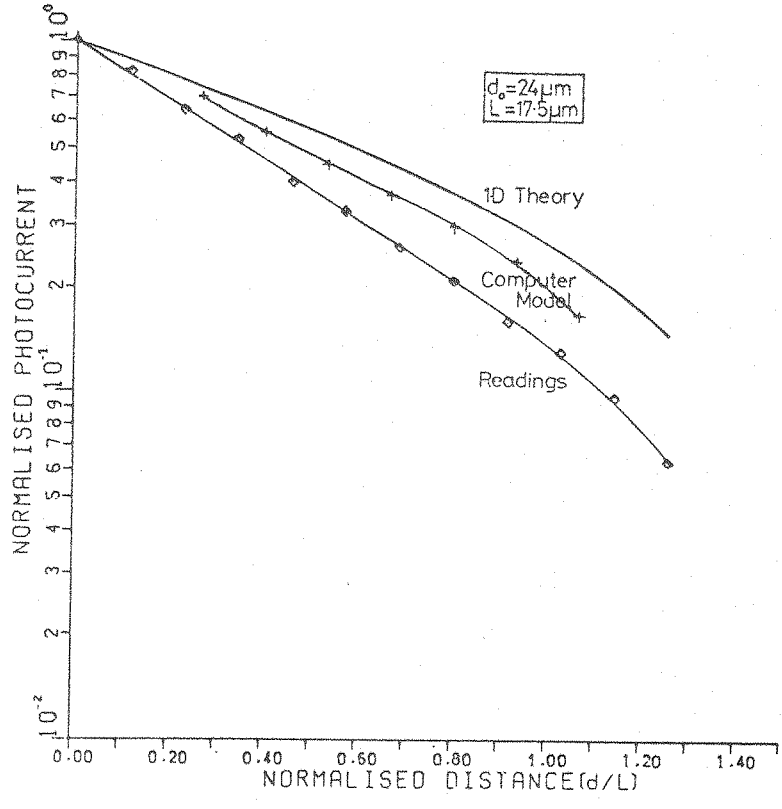
The analytical predictions for this situation can be compared with the readings in order to check the validity of the approximations which have been made. All three curves are shown in figure 20(b), from which it can be seen that the 2-D computer simulation gives closest agreement to the measured values but the error involved when using the 1-D theory is still less than 20percent.

A theoretical plot of the photocurrent variation with laser spot separation from the collecting junction is shown on linear axes in figure 21; again different inter-junction separations have been assumed and the distance values normalised. The asymptotic exponential decay is shown as the dashed line.

This characteristic can be used to determine the power of the laser beam which would be needed to supply enough photocurrent to both junctions so that in effect two circuit inputs are accessed at the same time. This is very important if the laser probe is to be used for integrated circuit testing, where the introduction of data at two sites simultaneously would cause many problems and may lead to a good circuit being rejected as faulty.



(a) Photocurrent collected with another junction 24μm away



(b) Comparison between theory and results

Figure 20: The effect of two junctions seperated by 1.4xL

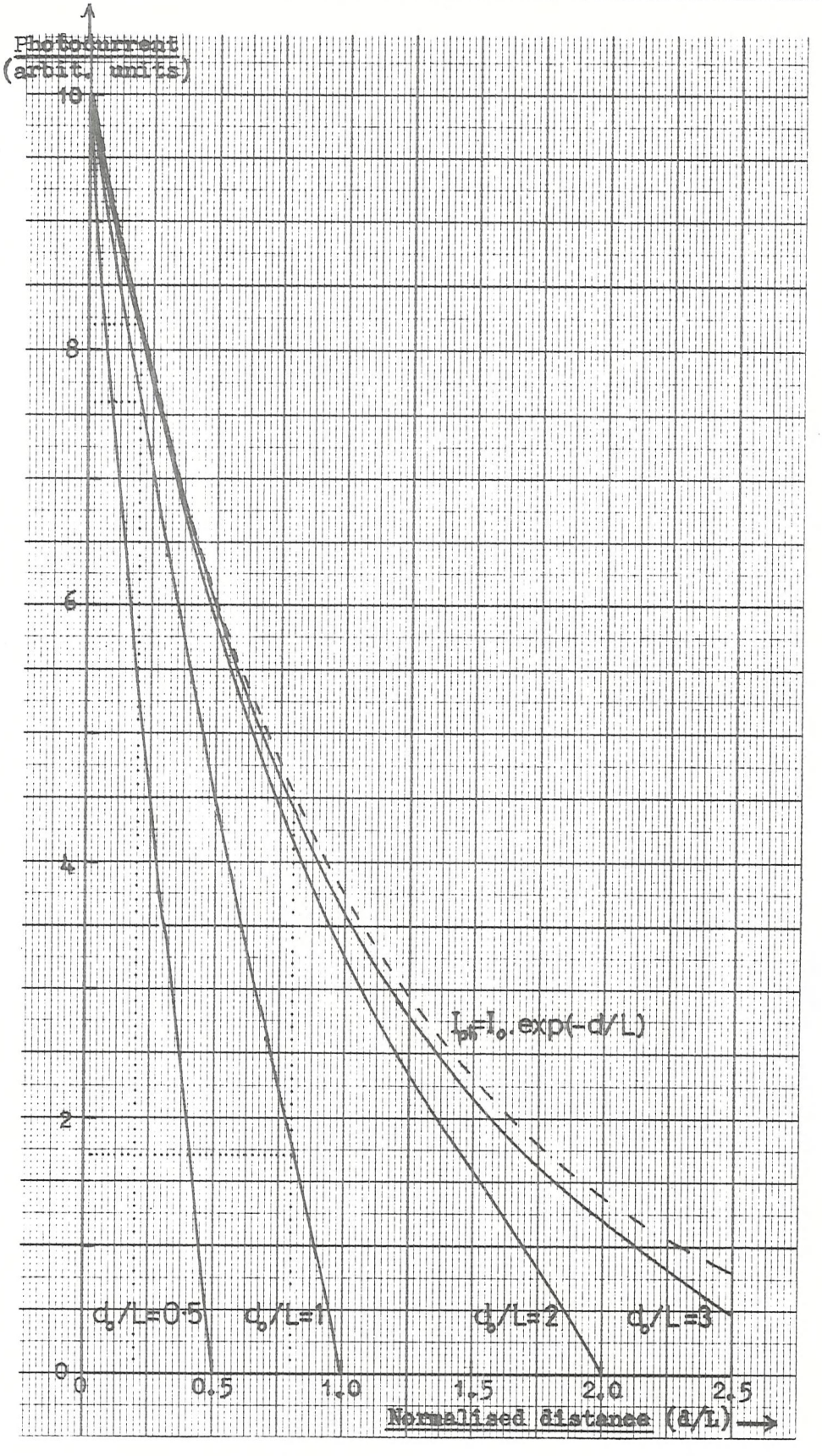


Figure 21: Nodal isolation

If the laser beam is positioned directly over the collecting junction then there will be little chance of a significant number of photocarriers reaching any other junction, but if there is some misalignment of the beam and the adjacent junction is close to the intended target junction, serious consequences may result. The interaction between the two junctions does produce some isolation though, as demonstrated by the following example.

If the two junctions were separated by a distance equal to the di--ffusion length and the laser beam was positioned one fifth of the distance between them, then for a given laser power, only 76percent of the maximum possible photocurrent would be measured by the closest junction (see figure 21); thus a 1.32-fold power increase would be needed to make up for the beam misalignment. If this junction was isolated though, the power ratio would be 1.22. The photocurrent which reaches the second junction 0.8 x L away is 17percent of the amount which would be measured if the beam was positioned directly over it, and this compares favourably with the 45percent which would be collected at this beam position if the second junction was itself isolated. A much larger increase in power is therefore needed to reach a certain photocurrent level because of the presence of the other junction. Hence if a laser power P produces a maximum photocurrent I_{ph} in each junction, then for a misalignment of 0.2 diffusion lengths, powers of 1.32P and 5.88P are needed to maintain this I_{ph} value in the first and second junctions respectively, but if the nodal isolation effect was not evident (if each junction is considered separately), the power levels would be 1.22P and 2.22P.

The practical implication of this result is that some beam misalign--ment can be tolerated even when two junctions are close together, and if the error in the laser probe position is less than about a quarter of the inter-junction separation, then it is very unlikely that both nodes will be affected by the laser at the same time, unless a light power many times stronger than the minimum requirement is used. As the distance between the junctions is increased, the accuracy constraints on beam positioning can obviously be relaxed.

4.4 Lifetime

4.4.1 Elementary theory

If the light source is switched off, the photocarrier concentration will drop because of recombination and eventually reach zero. For the case shown in figure 22, in which a block of n-type semiconductor material is uniformly illuminated up to a time t = 0, the excess hole concentration, δ_p, will be described by following equations:

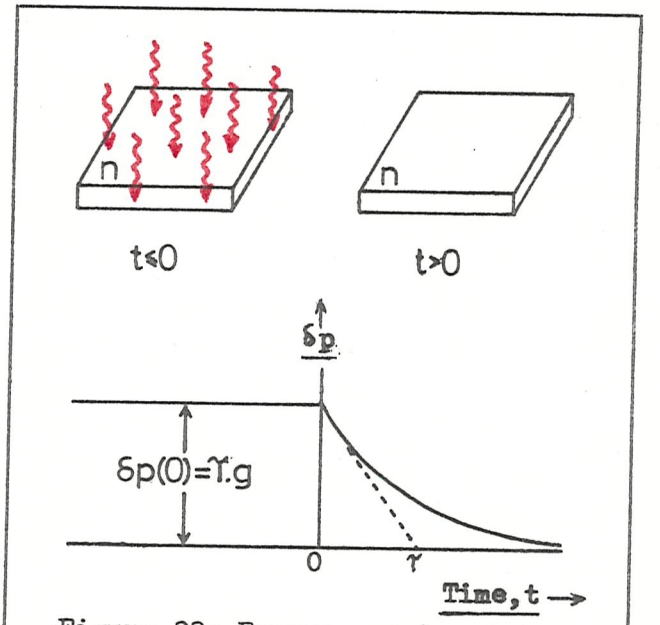


Figure 22: Excess carrier decay due to recombination

$$\underline{t \leq 0} \quad \frac{\partial \delta_p}{\partial t} = 0 = g - \frac{\delta_p}{\tau}$$

$$\underline{t > 0} \quad \frac{\partial \delta_p}{\partial t} = - \frac{\delta_p}{\tau} \qquad \ldots(4.11)$$

which have been obtained from the continuity equation (eqn. (4.3)) when carrier drift and diffusion are assumed to be negligible compared with recombination. It will be shown in section 4.4.3 that this latter condition is only valid if the generation source is well separated from a photocurrent-collecting junction (by more than about three diffusion lengths), otherwise the diffusion term must be included.

The time-variation of hole concentration as determined from equations (4.11) is also shown in figure 22: before the light is removed a steady-state level of

$$\delta_p(0) = \tau . g \qquad \ldots(4.12)$$

is reached and then at a later time, t, the concentration is given by

$$\delta p(t) = \delta p(0).\ \exp(-t/\tau) \qquad \ldots(4.13)$$

If this carrier decay is monitored by a pn-junction positioned at least three diffusion lengths away from the generation region, then the photocurrent collected at a time t is:

$$I_{ph}(t) = I_{ph}(0).\ \exp(-t/\tau) \qquad \ldots(4.14)$$

where $I_{ph}(0)$ is the steady-state value measured at the time t = 0. A simple exponential decay of photocurrent in the time domain is therefore predicted for this case, with a time constant equal to the hole life-time, τ .

4.4.2 Measurements

The same collecting pn-junction that was used for diffusion length measurements has commonly been used for lifetime determinations - this junction must be isolated (see section 4.3.4) and additionally the semiconductor surface up to a distance of at least three diffusion lengths away should be metal free, so again the p-type diffusion between the circuit and contact pad is often the only site suitable.

In order to measure the lifetime, the time decay of photocurrent following the removal of the light beam is recorded, and the time constant is determined from the resulting exponential response. This value is dependent upon the position of the light spot if it is less than about three diffusion lengths away from the collecting junction (because the carrier diffusion term in the continuity equation is no longer negligible), so the experiment is usually repeated for various beam displacements in order to ensure that the limiting value of time constant is reached.

A square-wave light modulation pattern is used so that a repetitive response can be observed and also to reduce the effects of traps (see section 4.4.3); a 1kHz repetition rate is usually satisfactory and slow enough to ensure that the steady-state condition is reached before the light is switched off. The pockel cell response (10-90percent rise and fall time of 150nsec) could impose a lower limit upon the values of time constant

which can be accurately measured, but the effects of this have been partially eliminated by 'correcting' the readings by using the relation--ship

$$\tau_e = \sqrt{(\tau_{measured})^2 - (\tau_{test\ system})^2} \qquad \ldots(4.15)$$

where $\tau_{measured}$ is the value of time constant found from the exponential decay, and τ_e is the corrected value. The test system response time, $\tau_{test\ system}$, can be found if the laser beam is directed onto the collecting junction, where τ_e is equal to zero (see section 4.4.3).

The photocurrent magnitude is very small because the laser spot could be more than three diffusion lengths away from the junction, so a good quality amplifier and oscilloscope have been needed, with all leads carefully screened to prevent pick-up of the 250v pockel cell driver voltage-swings.

A typical set of results is shown in figure 23, where three different light beam-junction separations (d = 0μm, 10μm and 20μm) have been used. Each decay is a simple exponential function of time except for the low photocurrent part of the response where some tailing-off is observed.

The exponential time constant obtained from these curves is plotted as a function of position in figure 24(a), and the correction to allow for the test system response time is also shown. A limiting value is reached for the laser positioned between 2 and 3 diffusion lengths away from the junction, which for this case (the SS-6-1032 shift register) is 260nsec. A similar type of response has been found from readings taken with other devices, and one example is shown in figure 24(b), where the limiting time constant is reached with a minimum spot-junction separation of under two diffusion lengths. These values of time constant are listed in table 4 for all the devices tested. An estimation of the error involved in each result has been included and it can be seen that these are quite large, principally because of the low-level photocurrents. However, if necessary a more sophisticated phase sensitive detector and preamplifier system could be used, possibly in conjunction with a faster pockel cell, but greater accuracy is not required for the present study.

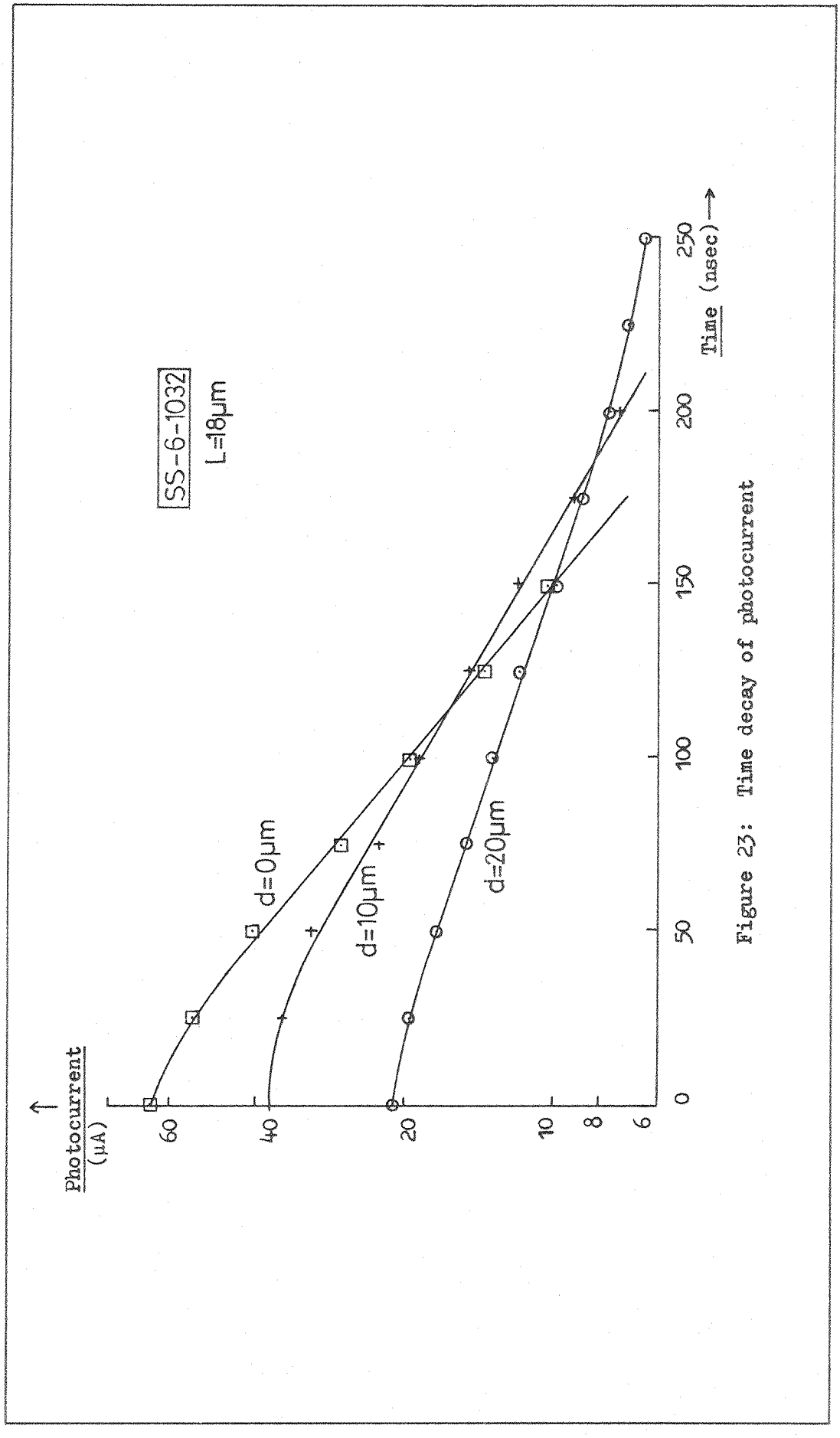
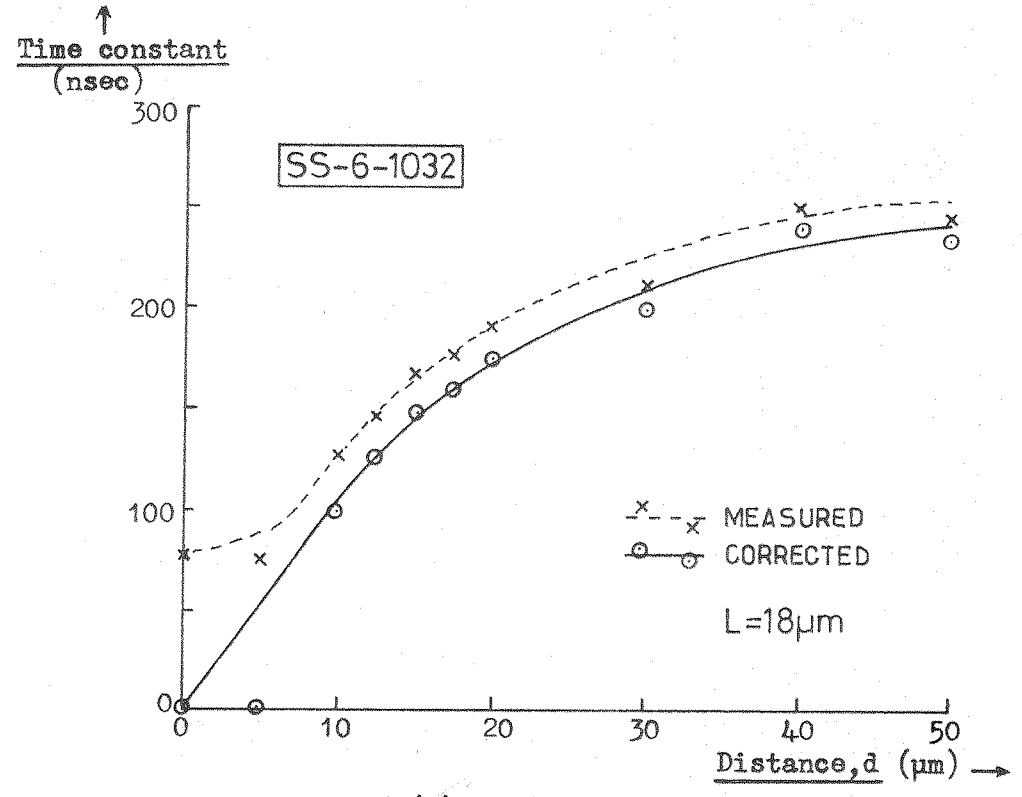
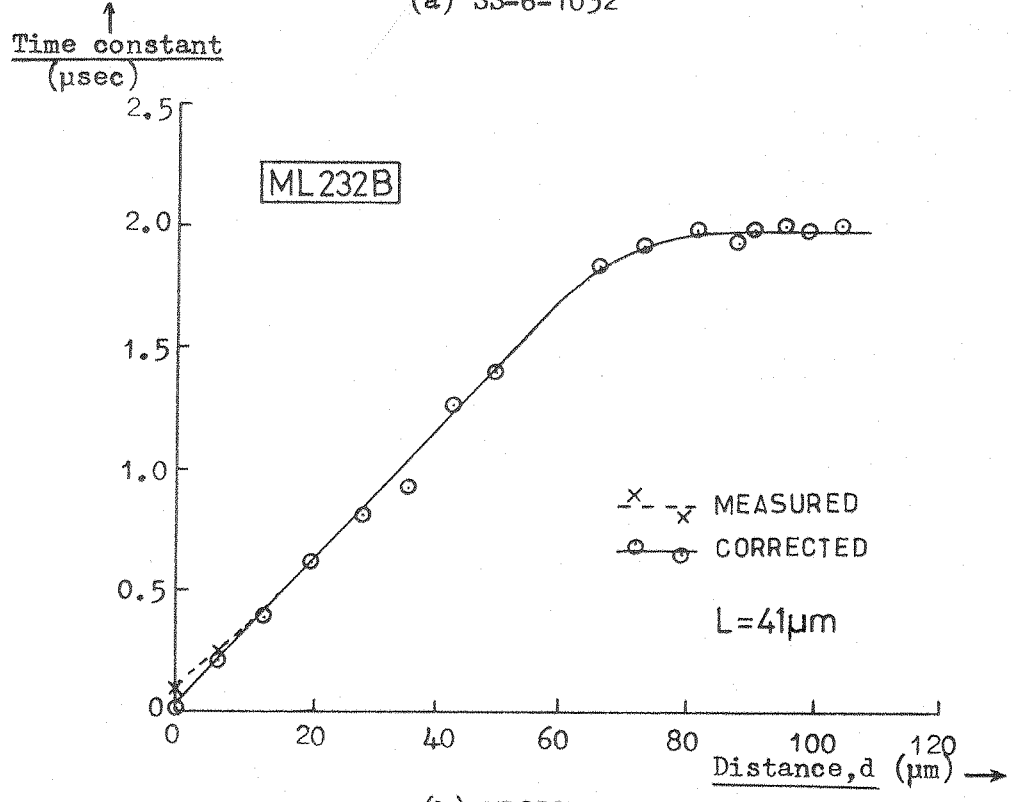


Figure 23: Time decay of photocurrent



(a) SS-6-1032



(b) ML232B

Figure 24: Positional dependency of decay time constant

I.C.family	Manufacturer	Device type	Limiting time constant (nsec)
M.N.O.S. p-channel Al-gate	General Instruments	SS-6-1032	260 ± 40
		SL-6-4032	240 ± 50
		DL-6-2128	120 ± 20
M.O.S. p-channel Al-gate	Plessey	ML232B	2100 ± 100
M.O.S. p-channel Si-gate	Mullard	GYN111	800 ± 200
C.M.O.S.	R.C.A.	CD4027	500 ± 60
Bipolar	Southampton University	142 ABAB	180 ± 40
Bipolar (n-sub)	Southampton University	166 JGSJCW	290 ± 40

Table 4: Measurements of lifetime

4.4.3 Analysis of the results

The carrier diffusion term in the continuity equation was ignored in the elementary theory presented in section 4.4.1, but this is only valid if the carrier decay with time is observed at a large distance from the generation region site. A 1-D solution of the continuity equation which includes the diffusion contribution is[55]:

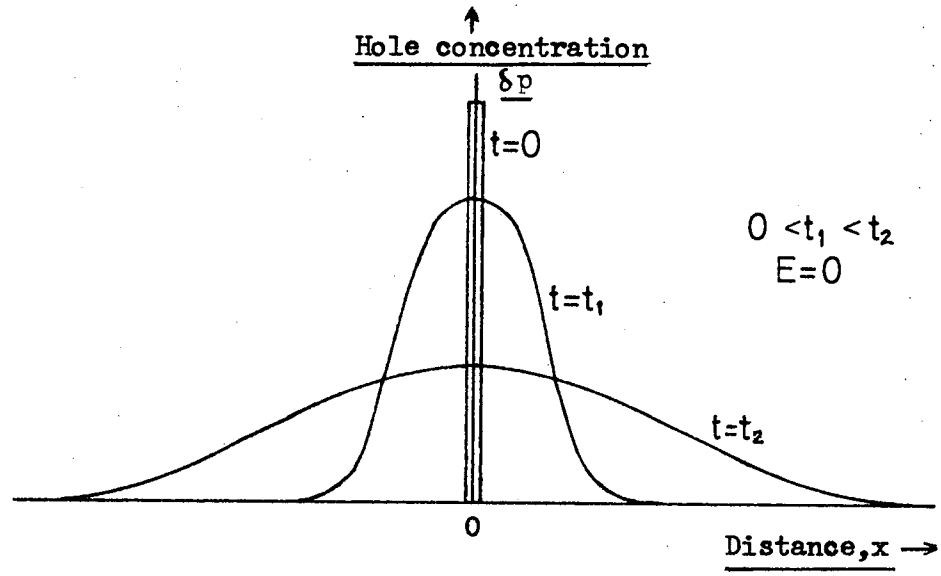
$$\delta p(x,t) = \frac{N}{\sqrt{4\pi Dt}} \cdot \exp\left(\frac{-x^2}{4Dt} - \frac{t}{\tau}\right) \qquad \ldots(4.16)$$

where N is the number of holes generated per unit area. The hole concentration is now dependent upon the distance, x, as shown in figure 25(a). The decay time, which is the time over which the hole concentration falls by a factor 'e,' can be plotted as a function of distance; this is shown in a normalised form in figure 25(b), from which it can be seen that the value of time does reach a constant value for a value of x greater than about two diffusion lengths, as expected.

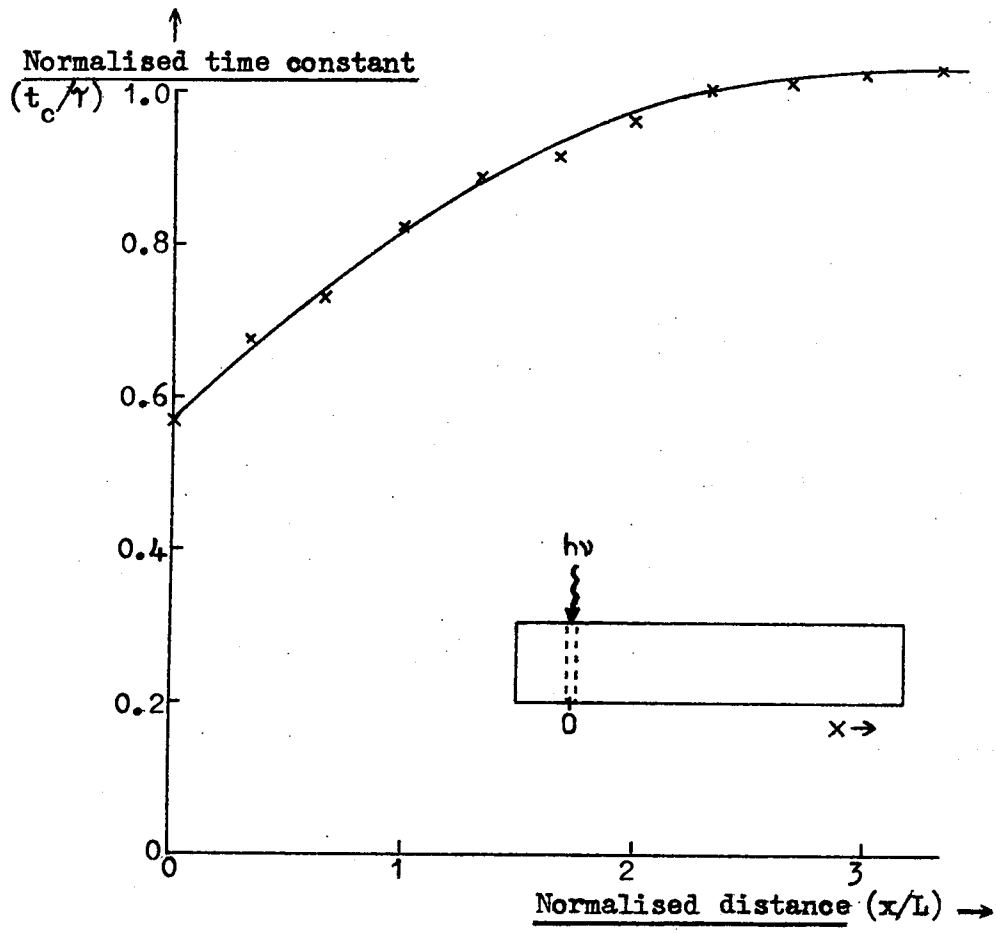
A more rigorous treatment of the same problem but in three dimensions has been published by Kuiken[56], in which some realistic boundary conditions have again been assumed (for details see Appendix 3(e)). A steady-state excess carrier distribution forms the initial condition, and this is derived in the same way as described in section 4.3.3. The results of this theory for the two cases of zero and infinite surface recombination velocity are given in figure 26(a), where photocurrent is plotted against time and various values of generation region-collecting junction distance (d) are used.

The time constant obtained from the exponential portion of each response is shown as a function of distance d in figure 26(b), and again a limiting constant value equal to the lifetime is reached, although the approach to this asymptote is not as rapid as for the 1-D solution.

A 2-D computer simulation has again been made, with details in Appendix 4(b), and this gave similar results to the theoretical analyses, as shown in figure 27.

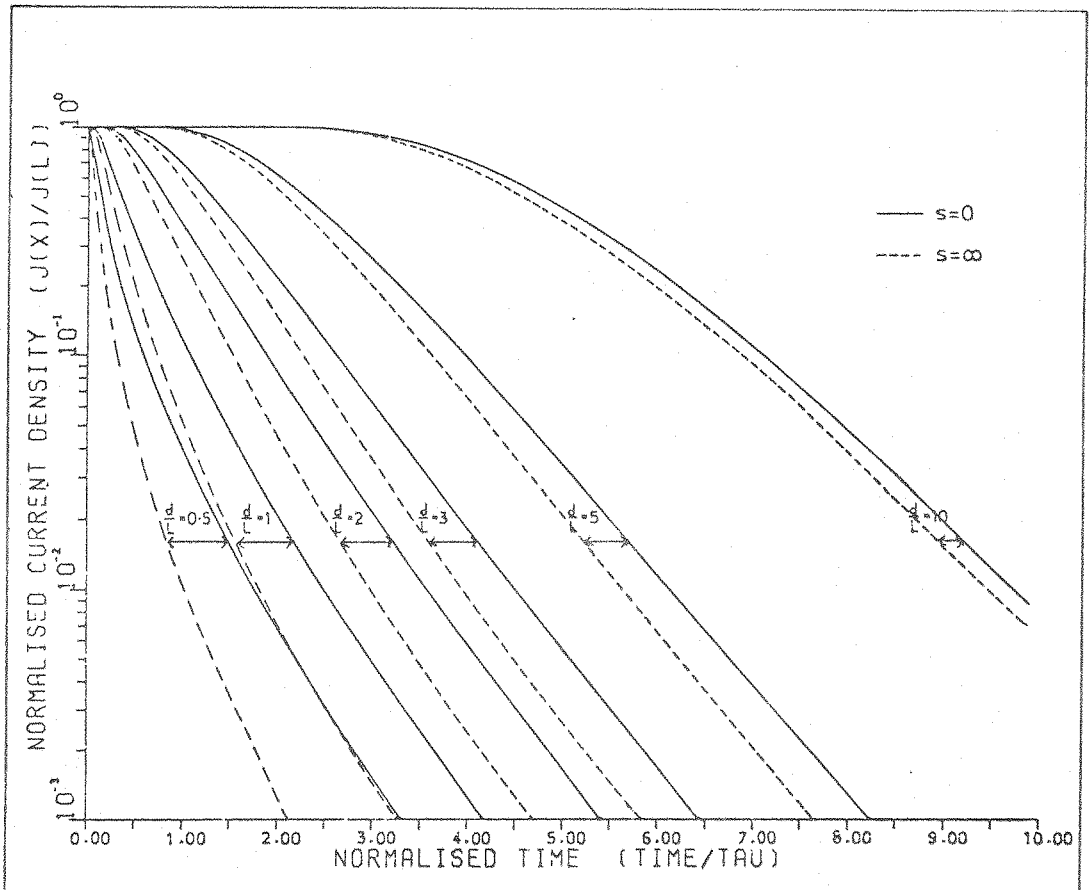


(a) Decay of excess hole concentration with time

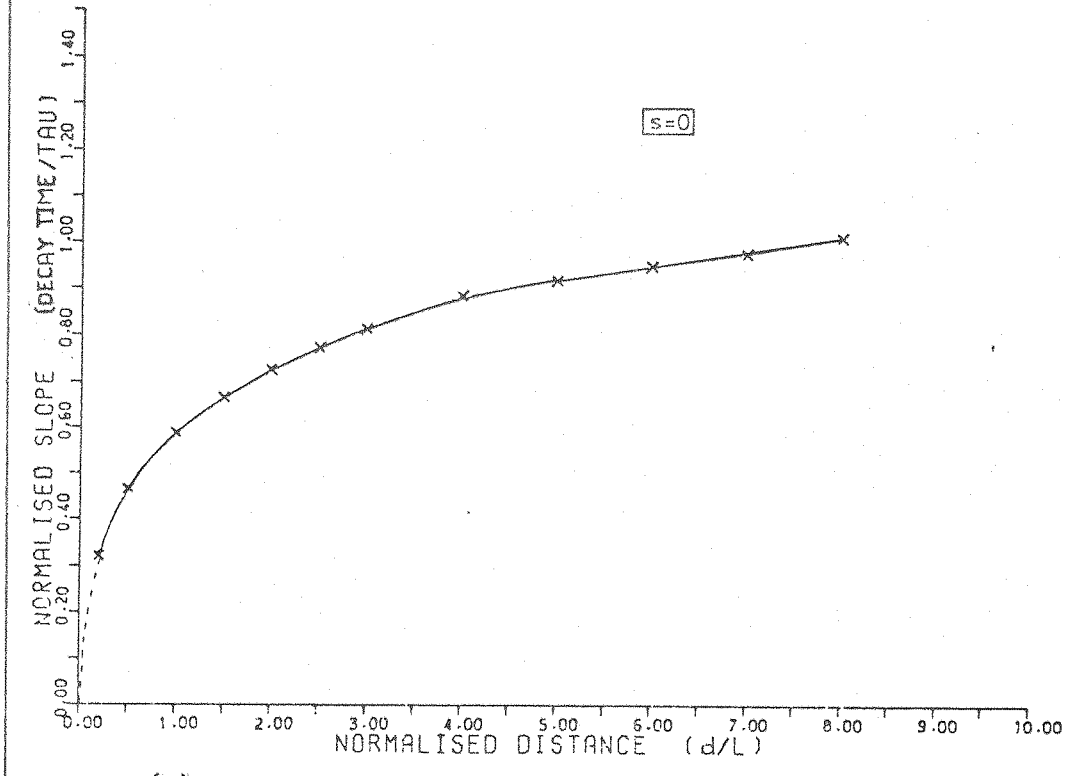


(b) Photocurrent exponential decay time constant

Figure 25: 1-D solution of the continuity equation

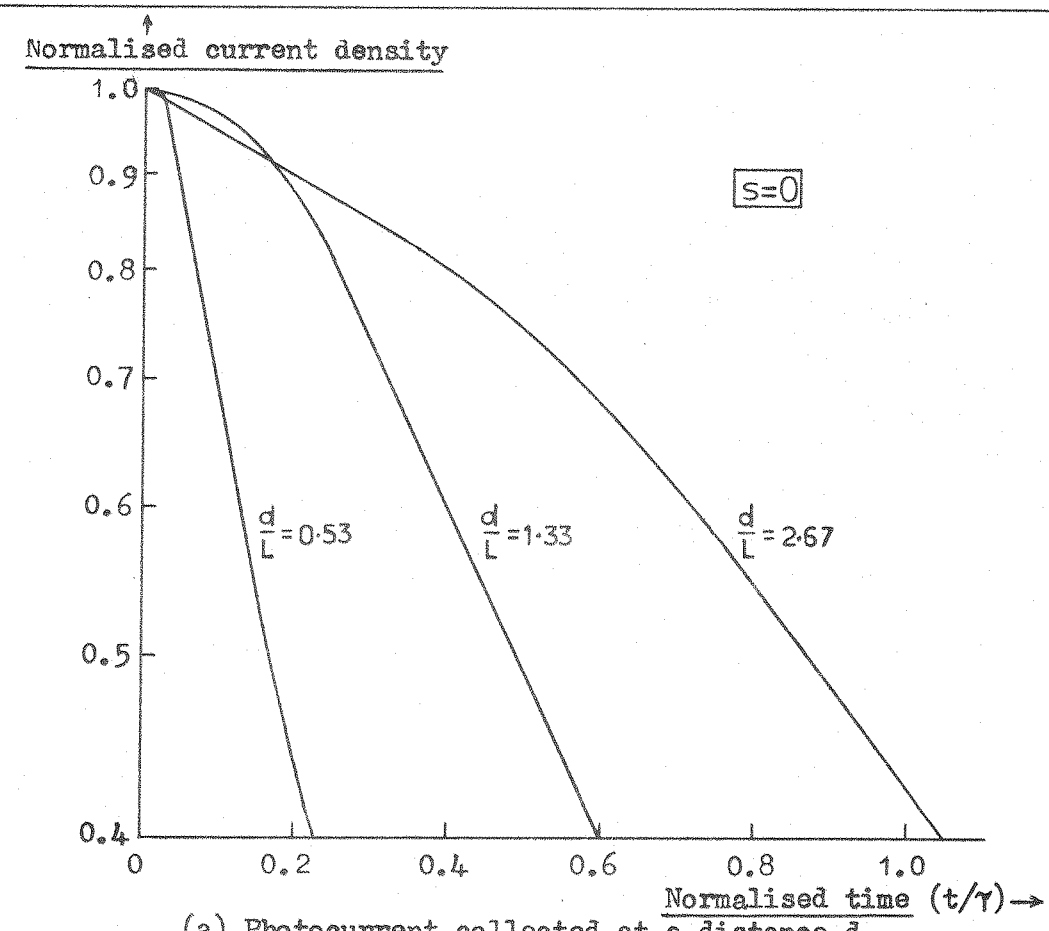


(a) Photocurrent collected at a distance d

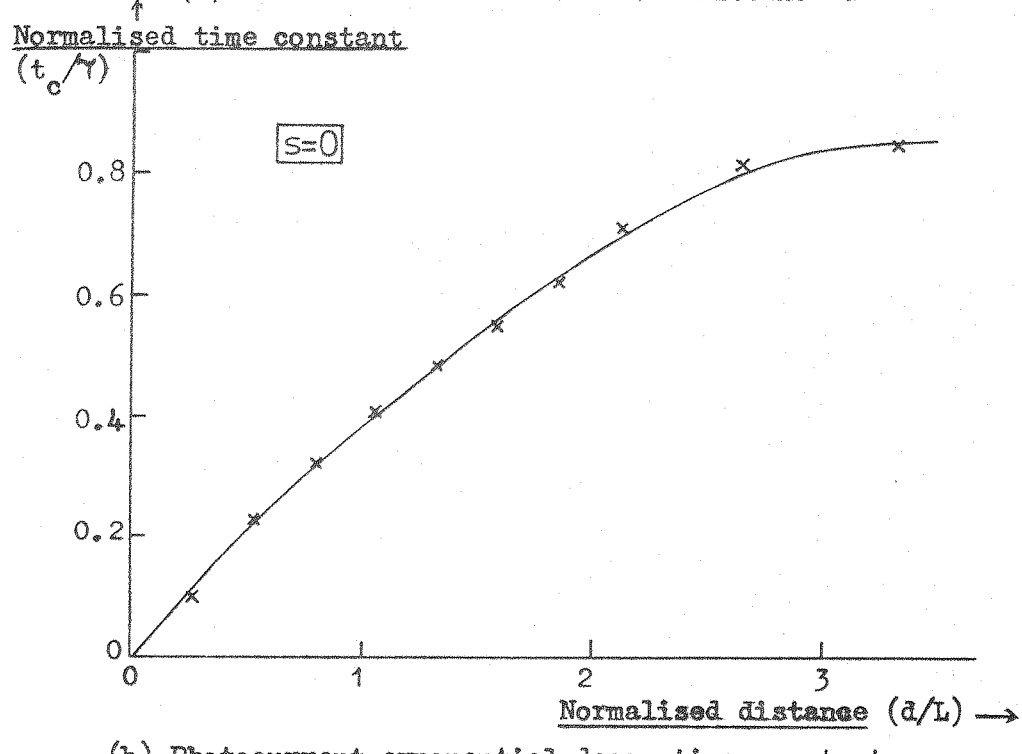


(b) Photocurrent exponential decay time constant

Figure 26: 3-D transient analysis (from Kuiken[56])



(a) Photocurrent collected at a distance d



(b) Photocurrent exponential decay time constant

Figure 27: 2-D computer simulation

A composite plot of the readings obtained from the SS-6-1032 device (figure 24(a)) and the predictions from each of the three cases mentioned above is given in figure 28. In each response, the time constant associated with the exponential decay of photocurrent reaches a limit equal to the lifetime, when the laser beam is positioned about three diffusion lengths away from the collecting junction.

The effect of a change in surface recombination velocity upon the results can be seen from figure 26(a) and Ridley[57] also reaches the conclusion that the measured lifetime will only vary by less than 5percent for a surface recombination velocity of zero or infinity. Only if the laser wavelength was much shorter with the absorption of carriers nearer to the surface would this effect be significant; it could then be possible that the surface lifetime and not the bulk value would be measured[58].

Traps can also affect lifetime measurements, and effective lifetimes much larger than the true value have been measured because of the long time constants associated with the capture process[59,60]. By using a sufficiently powerful modulated light beam of over about 100Hz repetition rate, the traps will on average remain full and have little effect upon the photo--current decay[61] and theexcess carrier concentration generated by the laser is considerably higher than the trap density, which has been quoted to be 2×10^{11} cm^{-3} for commercially available silicon[62] (see section 4.2). Direct measurements of lifetime have been made in a sample where a large number of recombination centres were present: for a laser power range of 30μW-1mW, no change in the observed lifetime value was noted which indicates that the traps are full[36], thus the effects of trapping in the measure--ments of lifetime can be ignored in this experiment.

For a 166 JGSJCW circuit, the lifetime has been measured to be 290nsec (table 4). A reverse recovery technique[63] has been used on the same device and a result of 270 ± 120nsec was obtained, and further confirmation has been found from an infra-red lifetime measuring technique[36] where at 100°C the lifetime of the 166 device was found to be 400nsec, although the practical temperature dependence of lifetime is uncertain.

The technique for lifetime measurement described in the previous section can be used at any stage during the manufacturing process after the

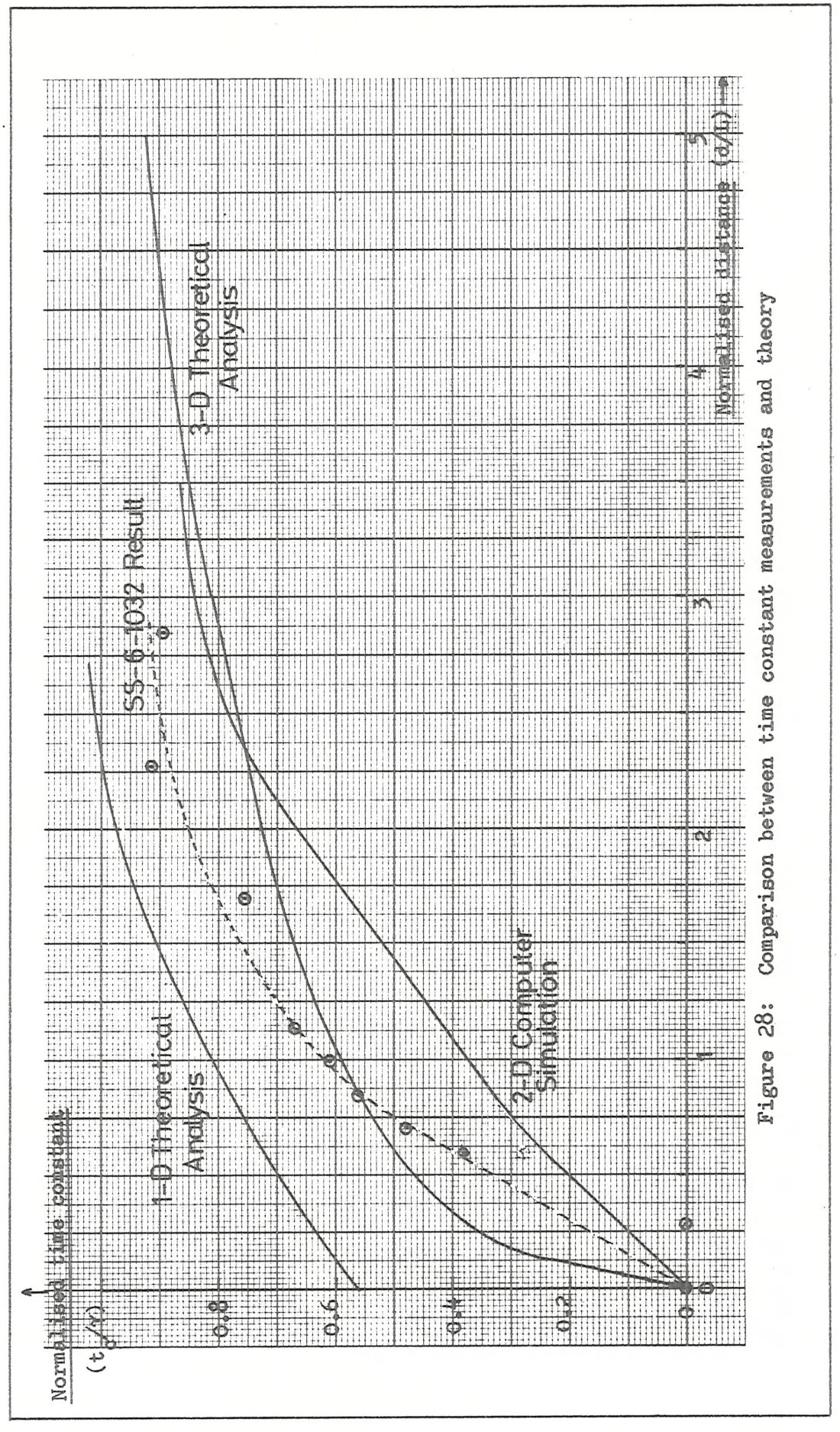


Figure 28: Comparison between time constant measurements and theory

collecting junction has been formed, and is much simpler than comparable electron-beam probe systems[64]. It is possible to find spatial variations in lifetime by changing the position of the laser beam, but unlike more accurate methods,[49,65] it is non-destructive.

4.4.4 The effect of lifetime upon the laser testing rate

If the laser probe was used to test an integrated circuit by injecting a photocurrent at various sites and this current decayed with a time constant equal to the lifetime, then the maximum rate at which data could be optically inserted into the circuit would be limited to a value which, for example, could be below 500kHz for a ML232B touch tuner (table 4). This would be unsatisfactory for commercial i.c. testing purposes, where test rates in the 1-10MHz range are generally used.

In practice, however, the laser beam is positioned directly over a pn-junction or as close as possible to it, so the effective carrier decay time constant is very much less than the true lifetime (see figure 28), and the maximum data input rate will therefore be governed more by the modulator response time. Pockel cells with 10-90percent rise and fall times of below 10nsec are available, so it should be possible to input information into an i.c. using an optical probe even when the circuit is tested at full speed. Drastic beam misalignment (by about a diffusion length or more) could reintroduce the slow carrier decay time problem, but this situation should never arise (see section 4.3.4).

4.5 Semiconductor Substrate Characterization

Both the diffusion length and lifetime of the excess carriers in the semiconductor substrate have been measured, so the diffusion coefficient, D, can be calculated since

$$D = \frac{L^2}{\tau} \qquad \ldots(4.17)$$

and hence the minority carrier mobility can be evaluated by using Einstein's relationship,

$$\mu = \frac{q}{kT} \cdot D \qquad \ldots(4.18)$$

A rough estimate of the doping level in the substrate can also be found from the value of diffusion coefficient,[66,67,68] but for majority carrier concentrations of less than about $10^{16} cm^{-3}$, the dependence of the mobility upon doping level is a weak function, so the results can only be used as an indicator of the overall processing situation.

Values of these derived parameters for some of the circuits tested are presented in table 5: for the 166 JGSJCW device, the resistivity of the n-type substrate is known to be 3-6Ωcm and the doping concentration $5 \times 10^{15} cm^{-3}$, with diffusion coefficient about $12 cm^2/sec$ and mobility $480 cm^2/v.sec$; the results agree quite well with these expectations.

Of the semiconductor parameters tabulated, mobility is the most important to the integrated circuit designer and manufacturer because it has a direct bearing upon device speed and power-handling capacity, but lifetime is also of interest, particularly in bipolar technologies where it can determine switching speed. Thus the ability to measure both diffusion length and lifetime separately is an important aspect of the laser probe operation, even if these measurements are not directly relevant to high speed production testing of integrated circuits. It has been shown that about 7percent of i.c. failures are caused by fault mechanisms in the bulk semiconductor[2], so a test strategy involving measurement of diffusion length and lifetime, particularly during the processing stages of a device, would be worthwhile because these failure modes could be eliminated before the full testing programme is started.

I.C.family	Device type	Diffusion coefficient (cm^2/sec)	Hole mobility (cm^2/v.sec)	Substrate doping concn. (cm^{-3})
M.N.O.S. p-channel Al-gate	SS-6-1032	11.9 ± 5.0	470 ± 200	$1\times10^{10}-2\times10^{17}$
	SL-6-4032	16.7 ± 3.5	500 ± 150	$1\times10^{10}-4\times10^{16}$
	D1-6-2128	5.1 ± 1.7	200 ± 70	$4\times10^{17}-3\times10^{18}$
M.O.S. p-channel Al-gate	ML232B	7.9 ± 1.5	310 ± 60	$5\times10^{16}-5\times10^{17}$
M.O.S. p-channel Si-gate	GYN111	14.1 ± 7.0	550 ± 275	$1\times10^{10}-5\times10^{16}$
C.M.O.S.	CD4027	7.3 ± 2.2	290 ± 90	$4\times10^{16}-8\times10^{17}$
Bipolar	142 ABAB	15.5 ± 8.0	610 ± 300	$1\times10^{10}-2\times10^{17}$
Bipolar (n-sub)	166 JGSJCW	16.2 ± 4.0	640 ± 150	$1\times10^{10}-1\times10^{15}$

Table 5: Semiconductor substrate characterization

CHAPTER 5

LASER PROBING OF I.C.'S

- Photoeffects in simple circuits
- Illumination of linear integrated circuits
- Laser probing of shift registers
- Laser probing of different i.c. families
- Measurement of the internal circuit operation
- Laser testing of the SN54LS191

5. LASER PROBING OF I.C.'s

5.1 Photoeffects in Simple Circuits

When a pn-junction is illuminated, a photocurrent flows in the same direction as the reverse saturation current I_{sat} (section 3.1.2), so the net current for a forward voltage of V volts is

$$I = I_{sat}.(\exp(qV/kT) - 1) - I_{ph} \qquad ...(5.1)$$

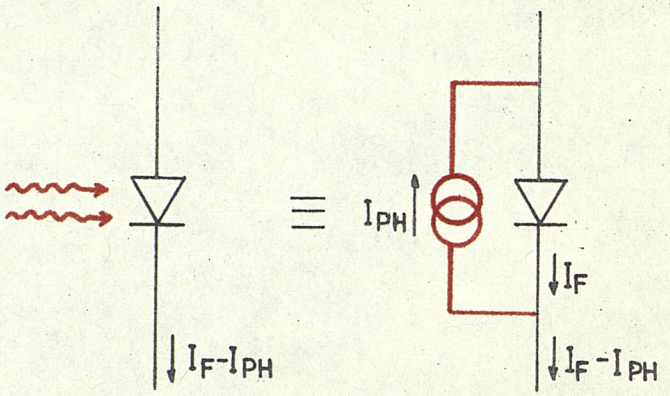
The effect of light upon the diode characteristic is therefore the same as if a current generator was added in parallel to the junction, as shown in figure 29(a).

In the planar bipolar transistor there are two pn-junctions which can act as photodiodes - the base-emitter and base-collector junctions. If this structure is uniformly illuminated, the generated carriers will be collected by both, but because of the relatively small metal-free surface area and shallow depth of the emitter, photoeffects at the base-collector junction will principally determine the effect of light upon the transistor characteristics. The photocurrent collected by this junction adds to the leakage current, I_{CBO}, as shown schematically in figure 29(b).

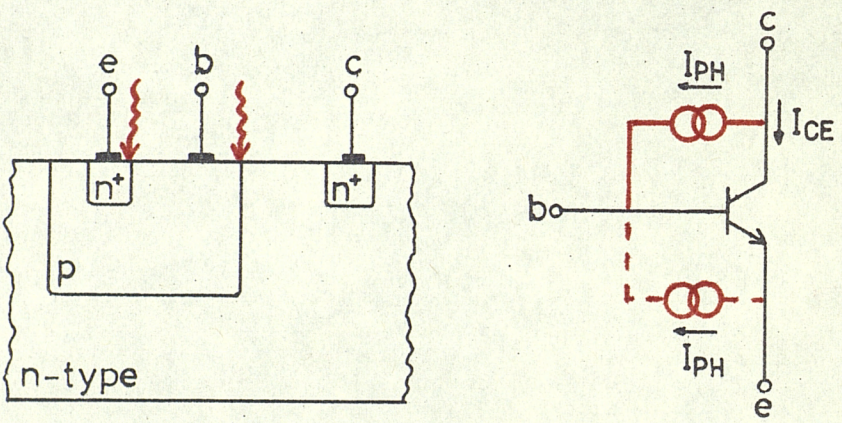
If the net base current is zero then the $(I_{ph} + I_{CBO})$ effective leakage current is balanced by an injection of minority carriers to maintain charge neutrality, and in effect it acts as a base drive which keeps the junction forward biassed. The output current, I_{CEO}, for this open circuit base configuration is given by[69]:

$$I_{CEO} = (I_{CBO} + I_{ph}).(h_{FE} + 1) \qquad ...(5.2)$$

where h_{FE} is the current gain; this magnified collector current resulting from the introduction of a photocurrent I_{ph} is the response normally associated with phototransistors[70]. Experimental confirmation of this prediction is presented in figure 30 where the collector current I_{CEO} has been measured as a function of laser beam power when the base-collector



(a) Illumination of a diode



(b) Illumination of a planar transistor

Figure 29: The effect of light on a pn-junction

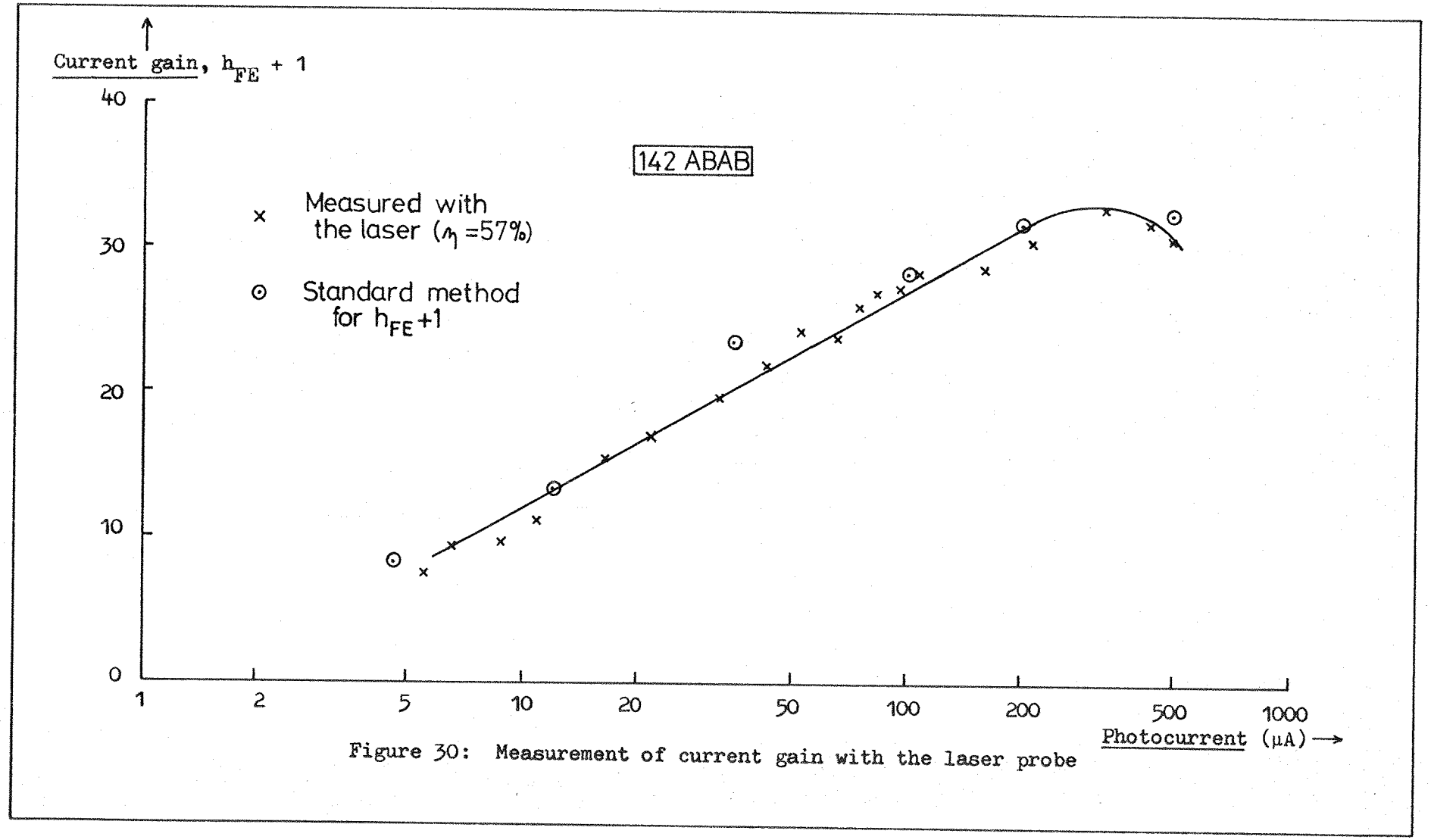
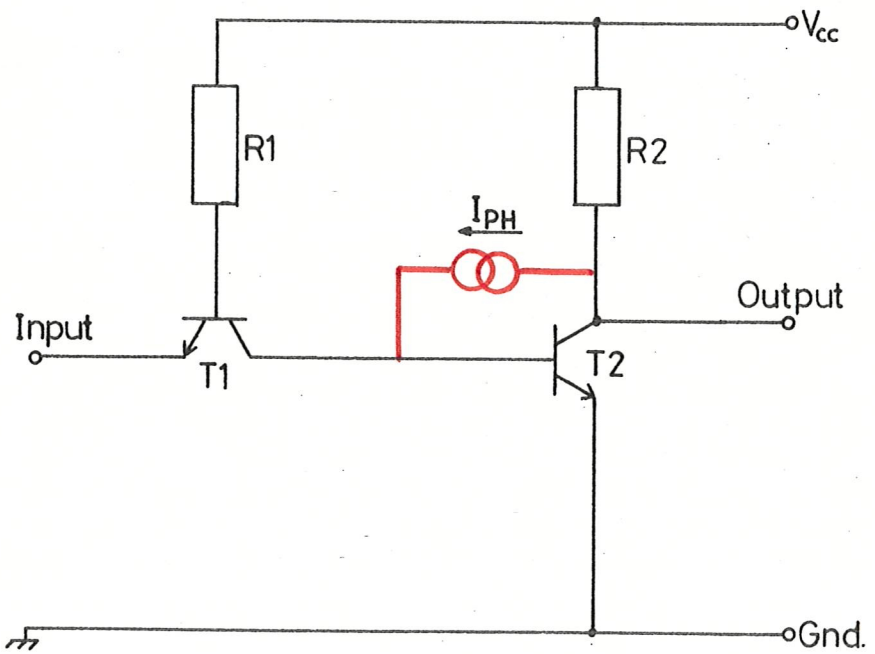


Figure 30: Measurement of current gain with the laser probe

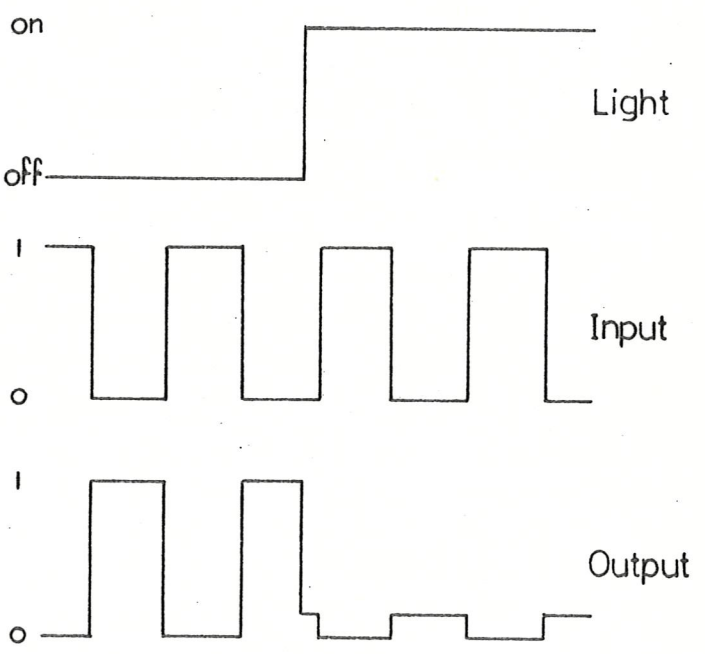
junction of a transistor on a 142 ABAB device was illuminated. The quantum efficiency is known to be 57percent (table 2), so the photocurrent equivalent of the power level can be calculated, and this has been plotted on the x-axis. The $(h_{FE} + 1)$ response as a function of base current for this transistor has also been included on the graph, by assuming that the photocurrent was identical to the total base current. The contribution of the normal 'dark' leakage current I_{CBO} can be seen to become significant for low values of photocurrent, causing a divergence between the two curves, but close agreement is found elsewhere.

The photocurrent will only have a significant effect upon the collector current if its magnitude is similar to or greater than the external base drive, which was assumed to be zero in the above example. In the simple two-transistor inverter shown in figure 31(a), the base current for T2 is only small when the input is grounded: in this case T2 is normally in the OFF or high impedance state and the output voltage approaches the V_{CC} level. If now the base-collector junction of transistor T2 is illuminated, I_{C2} will increase and as a result the output will drop in potential by an amount which is dependent upon the light intensity, R2 and the gain of T2. For the situation where the input is held at a high potential, the base current via R1 and T1 to T2 is relatively large and T2 will probably be saturated. The collector current is sufficient to hold the output voltage close to ground, so the contribution from the photocurrent will have no significant effect, as is shown schematically in figure 31(b).

Inverters implemented using different technologies also behave in a similar way when probed by the laser beam. A simple p-channel M.O.S. inverter is shown in figure 32(a); the p-type transistor drains and sources are formed in an n-type substrate, and these pn-junctions can be used to collect the photocurrent generated by the laser light. If the driver-drain/load-source diffusion is illuminated, then the photocurrent will flow from the substrate to the diffusion as indicated in the diagram, with the result that the output is pulled towards the substrate potential. In normal operation the output only reaches this level when the channel of the driver transistor is formed (with a negative gate voltage), so the photocurrent will only have a marked influence upon the action of the inverter if the input voltage is below the threshold, i.e. the driver transistor is in its high impedance state.

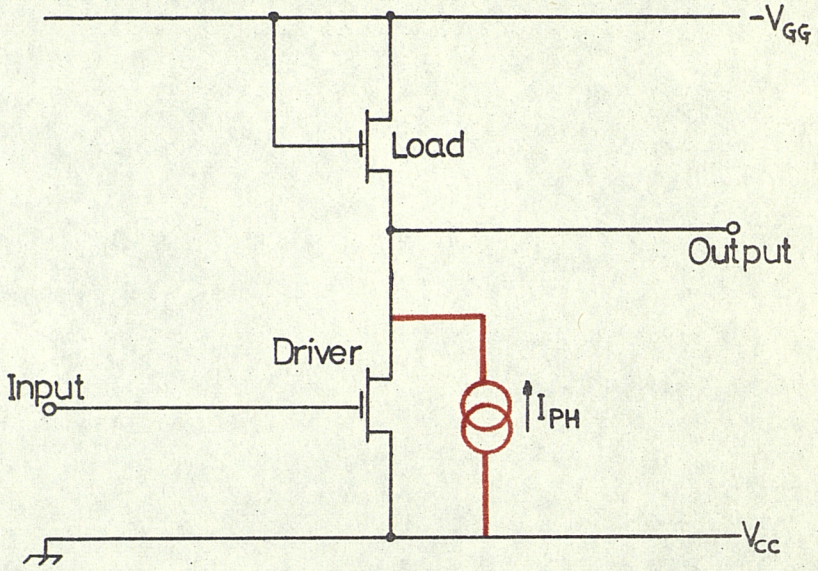


(a) 2-transistor inverter

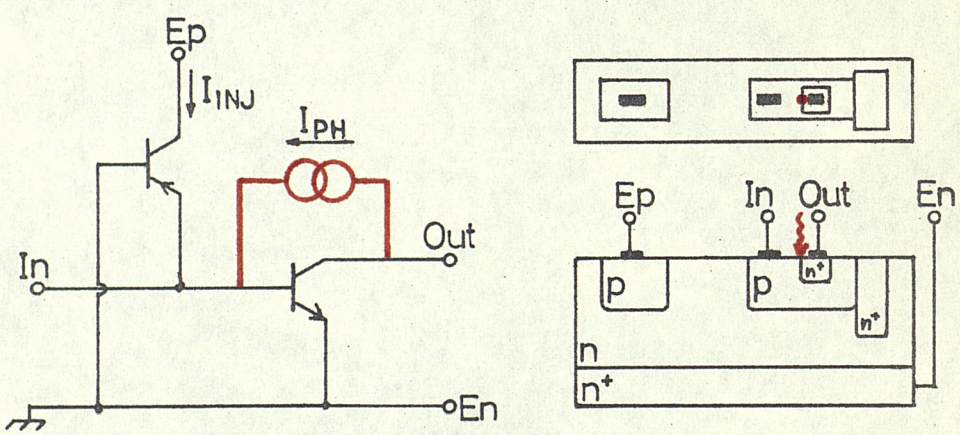


(b) Output response to light at T2 (b-c)

Figure 31: Illumination of a simple inverter



(a) M.O.S. inverter



(b) I^2L inverter and layout

Figure 32: The effect of light upon M.O.S. and I^2L inverters

The output of the I^2L inverter (figure 32(b)) can be significantly changed when the input is grounded and the laser beam is positioned close to the collector-base junction of the npn transistor. In this configuration, the 'injection' current from the lateral pnp device is diverted away from the base of the driver transistor and the photocurrent can then drive the output to the ground potential. Even though this collector-base junction is small and partially obscured by metal, the laser probe must be directed at this site and not at the emitter-base or base-collector junctions of the pnp transistor in order to force the output low.

The laser can therefore alter the functional behaviour of simple inverters, but its effect is dependent upon the currents which normally flow in the circuit - in general these should be less than the optically-generated photocurrent for the modification to be significant. Thus the power of the laser beam will be an important parameter, and this is demonstrated by the results obtained when more complex integrated circuits have been probed by the laser, as detailed in the remainder of section 5.

5.2 Illumination of Linear Integrated Circuits

The major part of this study has involved work with digital i.c.'s, but some of the characteristics of the laser probe can be established from the results of tests performed on three operational amplifiers.

5.2.1 The 709 op.amp.

The 709 operational amplifier is a three-stage circuit in which approximately one third of the total 45,000 open-loop voltage gain is developed in each stage. In the Fairchild circuit implementation shown in figure 33, resistive loads and npn transistors are used throughout, except for T12 which is a lateral pnp level shifter and T15, a vertical pnp device.

Transistors T1 and T2 are operated with a low collector current (about 20μA) to maintain a high input impedance and the gain of this differential stage, which is determined by the values of R1 and R2, is developed across the base-emitter of the unity-gain inverter T7. T6 and T8 are included to reduce the effects of second-stage loading and the constant current source is formed by T3, T4 and R3. The second stage gain is developed across R5 and the pnp transistor T12 shifts the d.c. voltage level towards the negative supply, so that the third stage consisting of T13 and R14 can drive the class B complementary output amplifier.

The op. amp. has been probed with the laser beam when it was operating in an inverting amplifier circuit, and the results of this experiment are shown in figure 33, where the observed change in output produced when the beam is directed at a particular transistor is indicated by a colour code on the circuit diagram. A red colour indicates a strong swing of the output in the positive direction (this usually means that it saturates at a potential close to $+V_{CC}$ for low laser powers) and purple shading marks the site where a less pronounced positive shift is produced. Similarly for the case of the circuit output forced towards the negative supply rail, green indicates a strong reaction for relatively low laser powers and the blue represents a weaker response in the same direction.

The light probe can be seen to have most effect when it is directed on the input circuitry, but very little reaction has been noted, even with full beam power, upon the second and third gain stages. The direction of the output shift is consistent with the fact that the injected photo--current increases the collector current flow through an illuminated transistor, and the 'strength' of each output reaction is related to the current levels which normally flow in the circuit. For example, if the laser beam is directed at the collector-base junction of transistor T2, the base potential of T8 drops and so the voltage developed across R5 also decreases; as a consequence, T13 and T15 will conduct more and the output voltage falls. Since the collector current for T1 and T2 is only about 20μA, a low-powered light beam will be sufficient to significantly alter the conduction in either the T1 or T2 branches of the differential

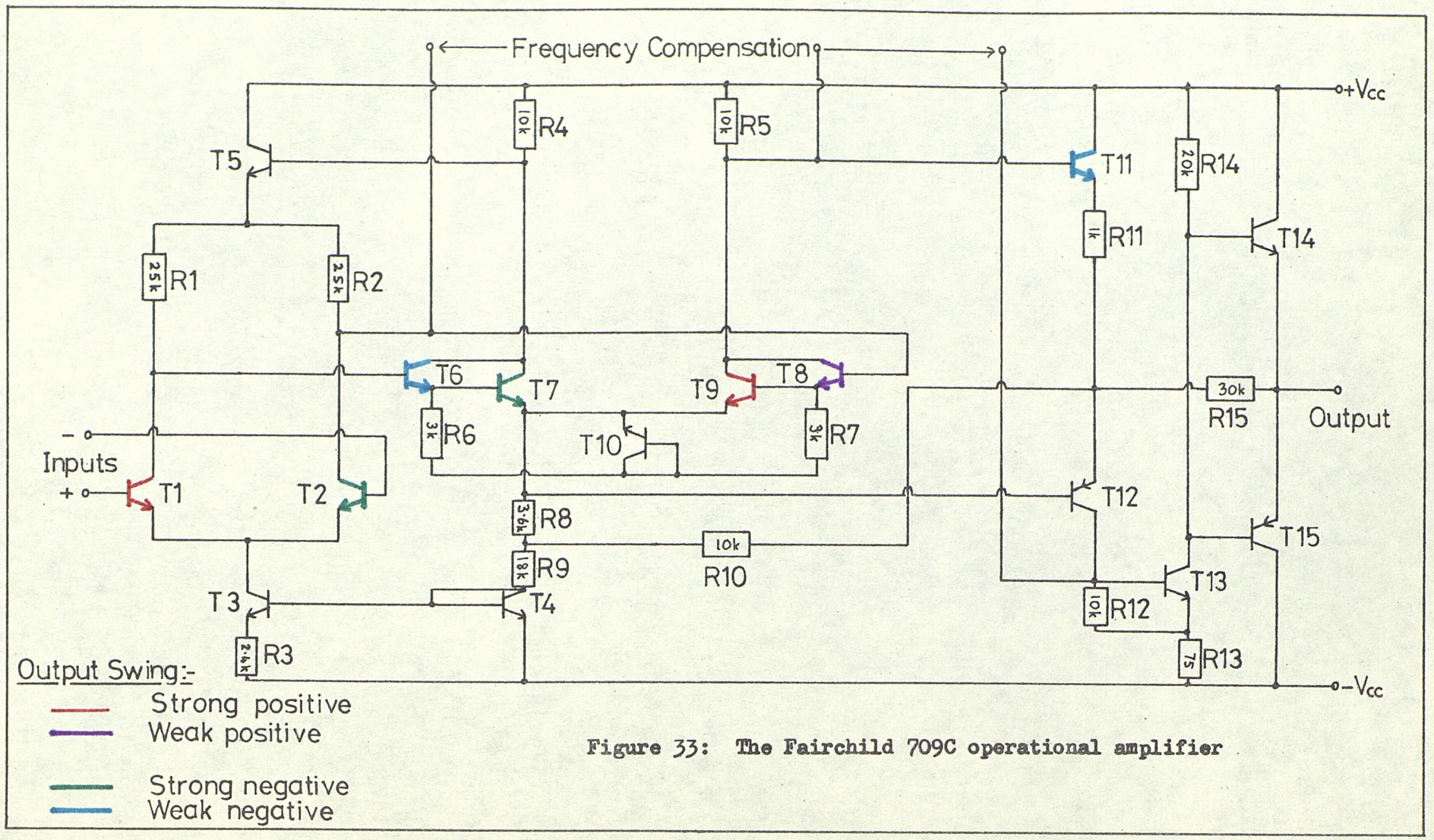


Figure 33: The Fairchild 709C operational amplifier

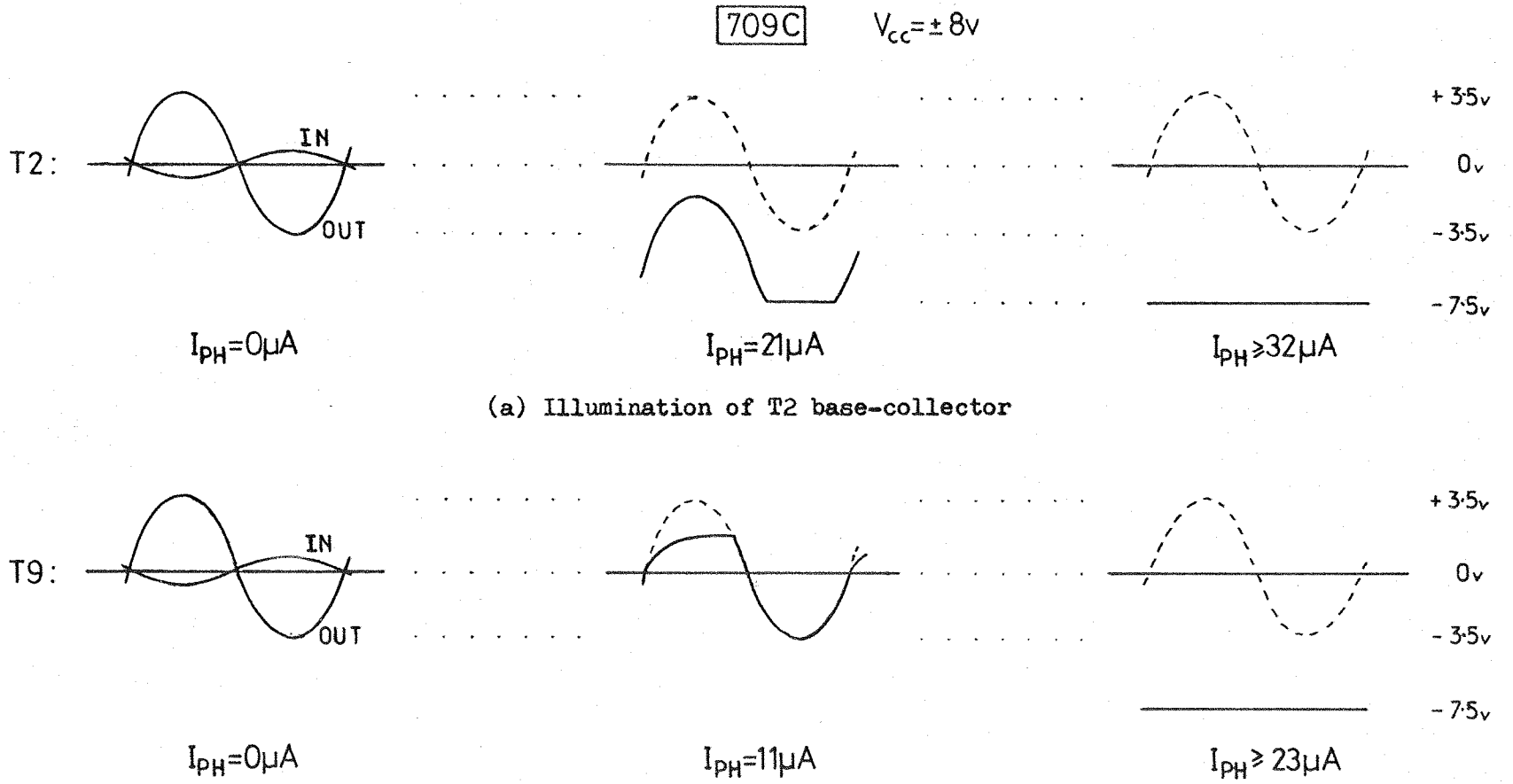
input, with any change strongly amplified by the following stages; thus it has been found that the output transistor T15 reaches saturation for an injected current of 32μA at T2, with the output voltage level held close to the $-V_{CC}$ supply. An indication of the change in output as the laser power is increased is given in figure 34(a). A sine wave input has been used, and the 'dark' response is shown in the first diagram, where $V_{CC} = \pm 8v$. When the laser power at T2 is increased, the d.c. output level begins to drop and clipping occurs when T15 saturates; for photocurrents larger than 32μA (calculated by assuming η = 70percent), T15 is permanently saturated for all input values. The magnitude of the photocurrent necessary to reach this final state has been found to be proportional to $\log_e(V_{CC})$ as expected, since the constant current supply to T2 and T1 varies as a function of the supply voltage in the same way[71].

The unity-gain drivers T7 and T9 also are very sensitive to the light probe: the effect of the beam positioned over the base-collector junction of T7 is also shown in figure 34. The output is first affected at low beam powers when T7 is conducting less than T9, i.e. the circuit input is negative, but as the injected photocurrent is increased, the output transistor T15 eventually saturates again. The buffer transistors T6 and T8 also produce a similar output response when optically probed, but more laser power is needed.

A small drop in the output potential is noted when T11 is illuminated, but this is the only site in the latter part of the circuit where the maximum photocurrent can approach the value of current which is normally flowing and alter the circuit operation.

5.2.2 The 741 op. amp.

The 741C is a more modern operational amplifier in which current sources are used as collector loads, and a 30pF frequency compensating capacitor and short-circuit protection are also included in the circuit, as shown in figure 35. Nine pnp transistors are used, of which T19 and T24 are substrate type, and pinch resistors are used to reduce the overall size of the device; the two stages produce an open-loop voltage gain of 100,000.



(a) Illumination of T2 base-collector

(b) Illumination of T9 base-collector

Figure 34: Laser probing of two transistors in the 709

The input stage uses the active load formed by T5, T6 and T7. The T1/T2 and T3/T4 combinations act as common emitter pnp devices, and the differential voltage swing appearing at their collectors is converted into a single-ended output, resulting in an improved common mode range compared with the 709. The stage gain is 60dB and feedback via T8 and T9 determines the operating point for the input transistors. A pnp current source (T12 and T13) is used as a load for the Darlington-configured transistors T15 and T16, and this pair drives a class B complementary amplifier. R5 together with T10 and T13 provides the correct bias, and short circuit protection is given by T20 and T21, which limit the maximum current flow to about 30mA.

The same colour code has been used to indicate the effect of the laser probe upon the circuit (see figure 35). To obtain these results, the op. amp. was used as a difference amplifier and adjusted so that a differential input of 2mV could be detected; the supply voltages were set to ± 10v and the maximum photocurrent for a quantum efficiency of 70percent was 400μA.

The differential input stage is obviously easily affected by the laser but some reaction has also been noted further on in the circuit. The strongest response to the laser illumination was found at the base--collector junction of transistor T9, where a power of only 26.5μW (just under 10μA) saturated the output voltage at +9.2v. A similar result was observed when the light was positioned over T1 (where a photocurrent of 18μA was needed), and also at T3(18μA) and T8(22μA); in these cases the base drive to the input transistors from T10 is reduced by the photocurrent in the common mode feedback circuit, so the output voltage is forced to rise.

When the input transistors T2 and T4 are illuminated, opposite polarity output voltage swings are produced, but the 0.6v change in d.c. level for a 35μA photocurrent is not as large as in the above examples because of the fixed base current drive.

The first stage output current, I_{O1}, is equal to $I_{C4} - I_{C6}$ (where I_{C4} is the collector current through T4 etc.), but since I_{C6} is identical to I_{C2} because of the action of the unity gain amplifier T7, I_{O1} is

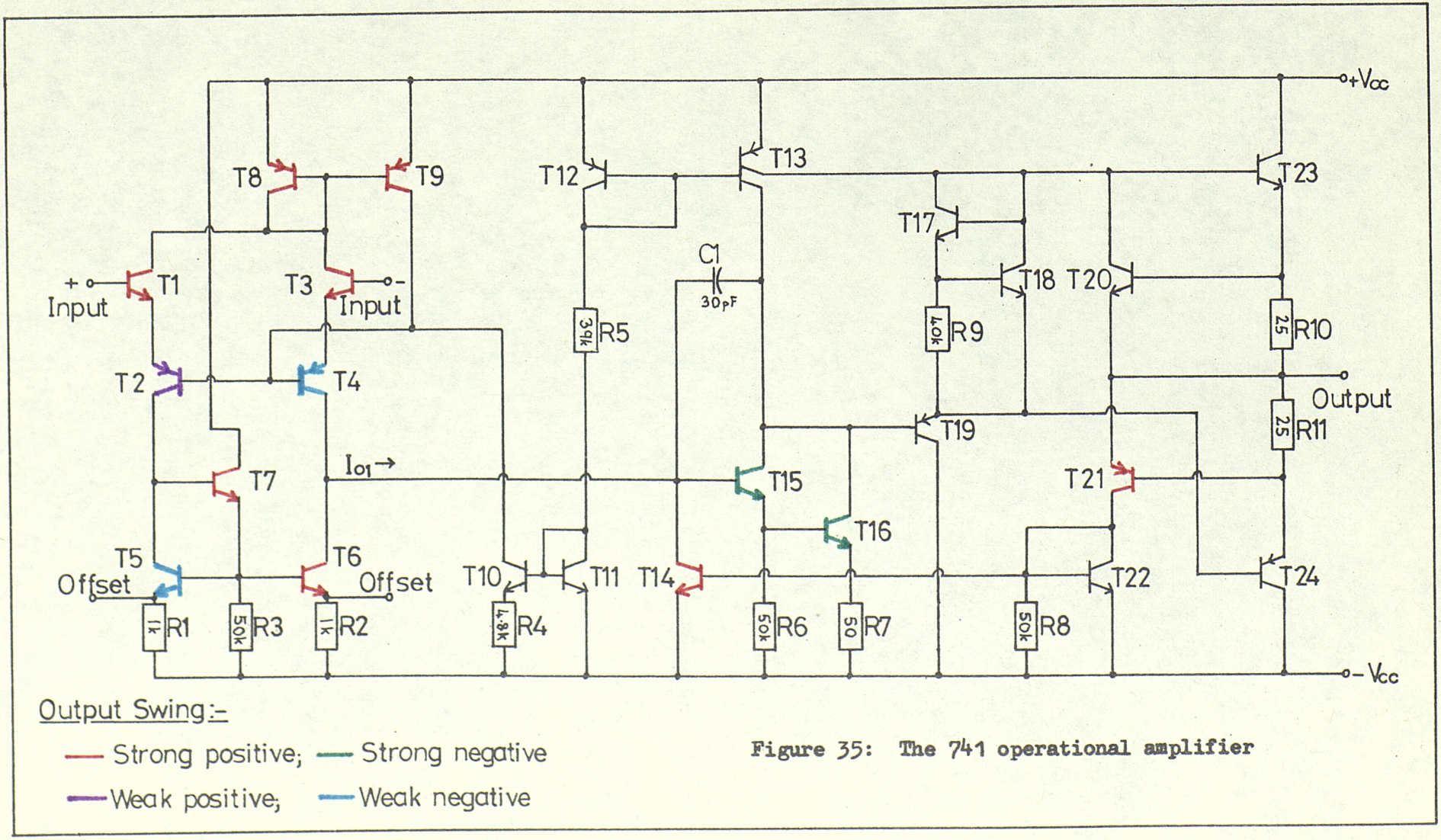


Figure 35: The 741 operational amplifier

simply the difference in the currents flowing through the T2 and T4 branches of the differential stage. Illumination of T7 and T6 will therefore tend to decrease the magnitude of I_{01} and produce a positive shift in the circuit output voltage, and in fact a 20μA photocurrent is sufficient to saturate the output; if the T5 collector current is incr--eased though, the drive for T6 is reduced and the output voltage drops.

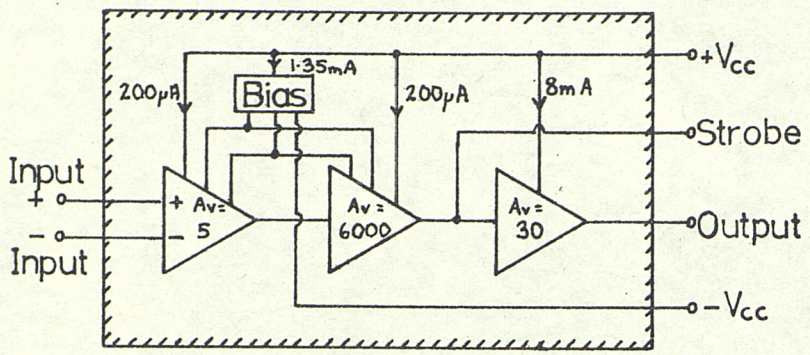
The current I_{01} is not very large when the op. amp. is operated as a difference amplifier (as demonstrated by the T6 result), so it would be expected that the laser could supply enough photocurrent to significantly alter the currents flowing in the Darlington pair T15 and T16. In practice, photocurrents of 18μA at T15 and 21μA at T16 were sufficient to produce a saturated output of -9.3v. Conversely, if the base-collector junction of T14 is probed by the laser, the base current for T15 is decreased and a + 9.2v output is obtained for an injected current of 16.5μA.

From these results, it can be seen that the first stage output current, I_{01}, needs only to vary over a 18 + 16.5 = 34.5μA range in order to produce the maximum possible output voltage swing. Hence the laser probe can be used to determine the magnitude of the currents flowing within the circuit, which are otherwise extremely difficult to measure, in order to check calculations or to diagnostically test faulty devices.

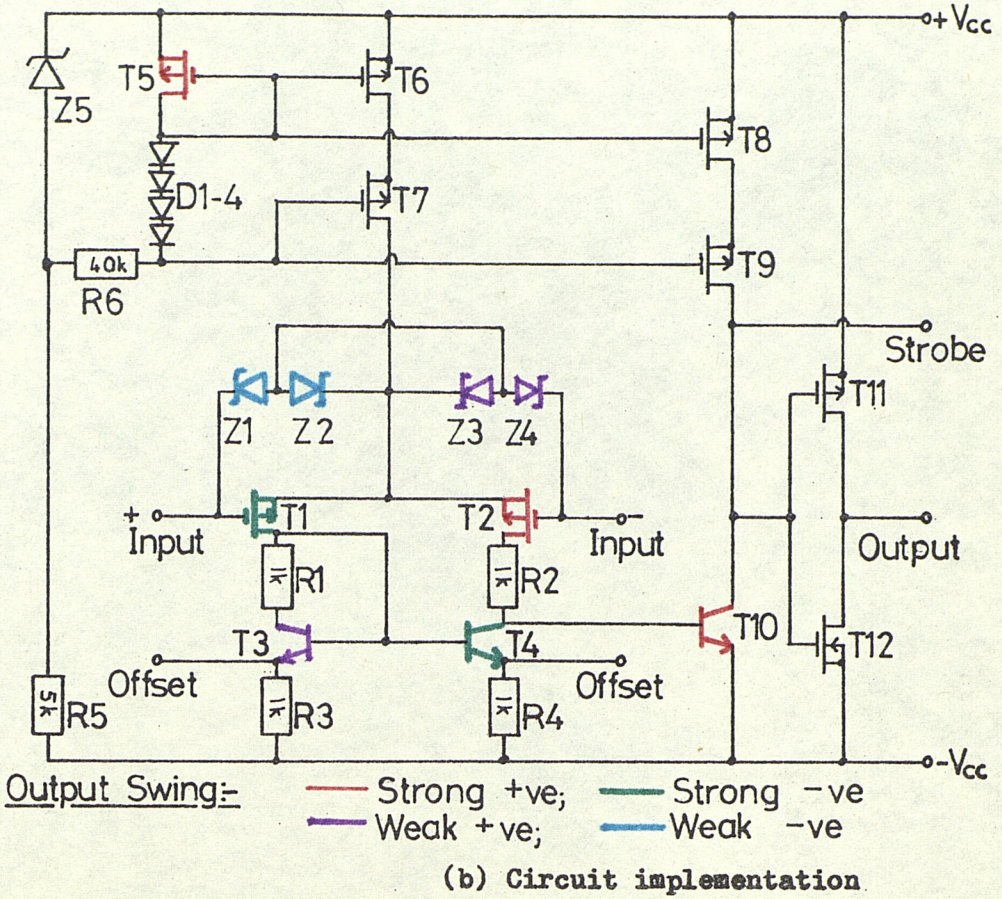
The relationship between the photocurrent magnitude (or laser power) and the current levels in the circuit is well demonstrated by a comparison of the output reactions observed for the laser probing of transistor T15, where a 0.05 mW beam power can produce a variation in output voltage of 9.3v, and transistors T23 or T24, when a 1mW beam can barely manage to alter the output by 10mV.

5.2.3 The CA3130 op. amp.

The CA3130 operational amplifier is another 3-stage device, but is implemented by using both M.O.S. and bipolar transistors. A block diagram of the op. amp., which shows the current levels and gain associated with each stage, and the detailed circuit diagram are given in figure 36. The T5 and T6 source supplies a constant current to the differential input transistor pair; an active load is formed by T3 and T4



(a) Block diagram



(b) Circuit implementation

Figure 36: The CA3130 operational amplifier

and the single-ended output is amplified by T10 and fed to the high input impedance C.M.O.S. output stage. A separate bias circuit is used and zener diode input protection is necessary because of the M.O.S. inputs.

This op. amp. has been probed with a 0.7mW (250μA) laser beam, and the results shown in colour on the circuit diagram were measured when it was operated in the inverting amplifier mode, with $V_{CC} = \pm 7.5v$. The input stage behaved similarly to the 741, but the polarity of the output changes was different. A minimum of 120μA photocurrent has been found to be necessary to drive the output to the $+V_{CC}$ level; this occurred when the beam was directed onto the drain of T5, in effect reducing the current supplies for T1, T2 and T10. For the beam positioned over T1, T2 or T4, photocurrents of 150μA are needed to produce the same result or its inverse, and this value shows reasonable agreement with the 100μA which is expected to flow in these branches of the circuit. Similarly, 200μA is the nominal supply for T10, and a measured laser power of 0.59mW (210μA) at this point produced an output voltage close to the $+V_{CC}$ supply. No change in the output was observed when T11 or T12 were illuminated, but the 8mA current flowing here is about sixty times larger than the photocurrent so this result was not unexpected.

This series of experiments on operational amplifiers has demonstrated that the laser can inject a photocurrent into both bipolar and M.O.S. structures in a predictable manner and that the effect of this extra current upon a circuit depends both upon the laser beam power and the currents already flowing in the portion of the circuit which is illuminated. These factors can all be quantified, so both fault detection and diagnosis, and circuit characterization can be enhanced by using the laser probe.

Analogue circuits offer only limited scope for laser testing though, so the majority of the work in this study has been concerned with digital i.c.'s. The same conclusions with regard to the action of the laser beam upon the circuit behaviour will still apply here but the optical probe can also be considered to be a moveable extra input, and used to great effect in changing the logical operation of a circuit.

5.3 Laser Probing of Shift Registers

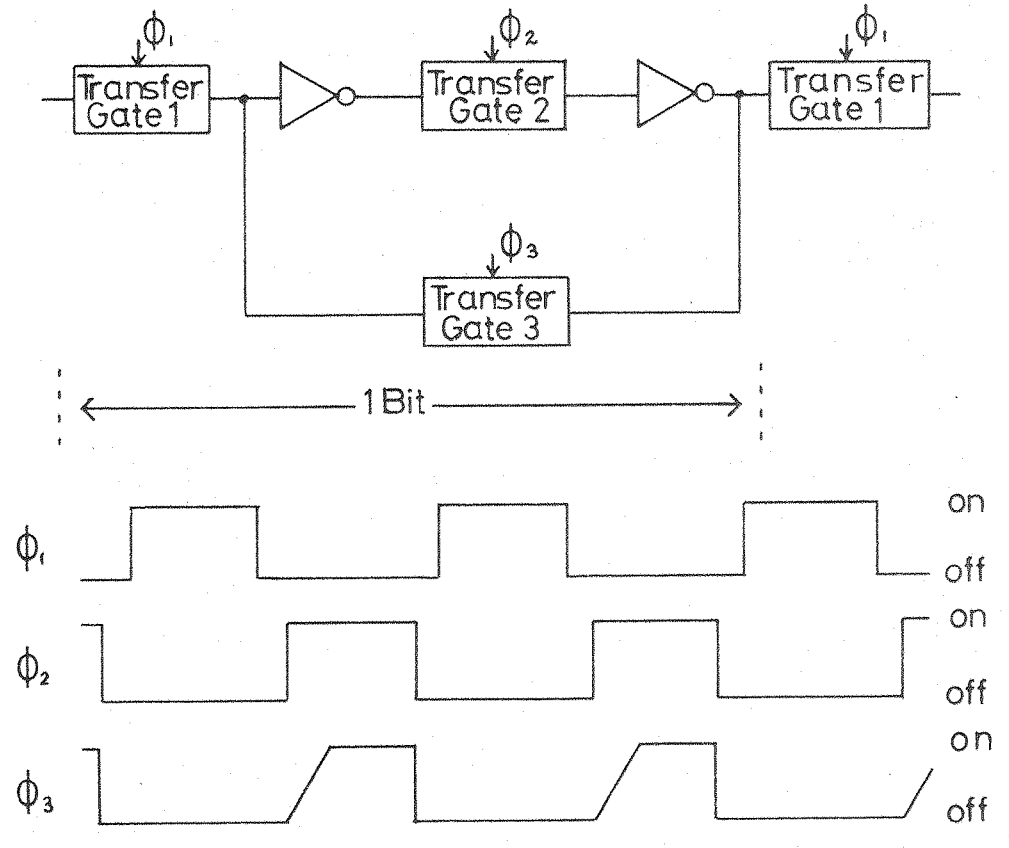
5.3.1 The shift register

The shift register is a relatively simple example of a digital circuit, and yet it is extremely hard to locate any faults which may occur in it; however, fault diagnosis is easy to perform using the laser probe, and since any output change can be readily recognised and related to the site of an optical input, the results obtained by using the register have been chosen to demonstrate the most important features of the the laser test method.

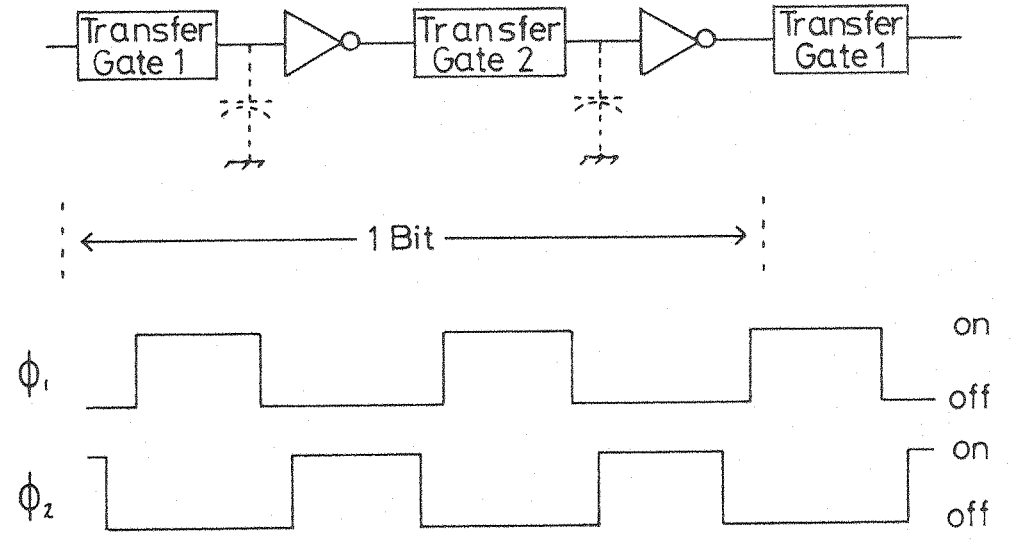
The shift register is shown in its basic form in figure 37: there are two inverters per each 'bit', and clock-controlled transfer gates are used to direct the flow of information. In the case of the static register (figure 37(a)), data are not lost when the clocks are stopped because of the feedback loop formed via Gate 3. However, the storage function is performed by the parasitic capacitances associated with each inverter in the dynamic shift register, so that this 'memory' branch is no longer needed; but since the charge on the capacitances leaks away, there is a minimum operating clock frequency associated with dynamic logic circuits. For each type of register, information transfer only takes place on the command of a clock signal, i.e. the operation is synchronous.

The M.O.S. implementation of the static shift register is shown in figure 38 together with its associated clock waveforms, and a photograph is shown in figure 41(a), where the laser probe (3μm diameter) is positioned over the diffusion indicated as node X. Each cell or bit consists of two cross-coupled inverters and four transfer gates which are governed by the internally-generated clocks ϕ_1, ϕ_2, ϕ_3 and ϕ_4. In the circuit shown, the M.O.S. transistors are p-channel enhancement type, so a negative gate voltage (logical '0') is needed to form a channel and turn a transistor ON.

The circuit operation is as follows:- if a '0' is clocked into the input (negative potential), this is inverted by Driver A to a '1' or 0v

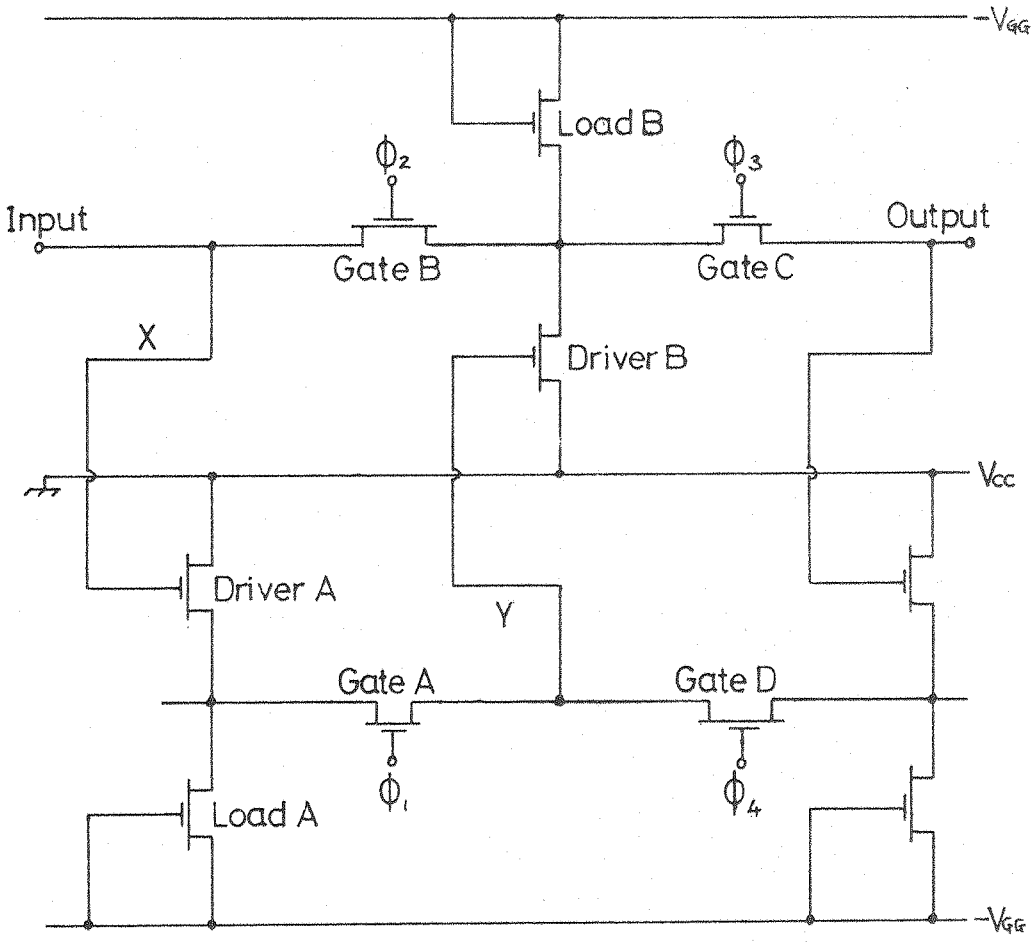


(a) The static shift register

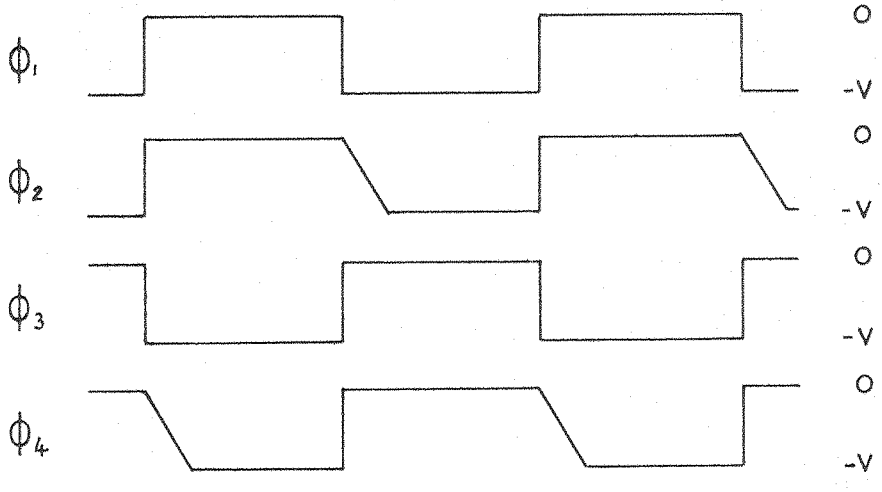


(b) The dynamic shift register

Figure 37: Basic structure of the shift register



(a) 1-bit of the register



(b) Internally-generated clock waveforms

Figure 38: The G.I. M.O.S. static shift register

at the source of Gate A. After clocks ϕ_3 and ϕ_4 return to ground level, ϕ_1 and ϕ_2 go negative and turn ON Gates A and B; the slower falling edge of ϕ_2 ensures that the '1' is transferred first to Driver B via Gate A and not through Gate B. This is inverted by Driver B, so a '0' is fed back to the input through Gate B, completing the loop. On the next clock transitions, Gates A and B turn OFF and then Gate C and finally Gate D turns ON, so that after one complete clock period, the '0' value reaches the output.

A different form of the static shift register is shown in figure 39 - this is an I^2L version of an edge-triggered D-type bistable. A photog--raph of one such flip-flop is shown in figure 41(b). When the clock is at level '1' (+5v), transistor T2 is ON with T4 and T5 OFF, so the output, which is determined by the cross-coupled NAND pair of T6 and T7, retains its previous state. Only during the clock '1 → 0' transition is this slave element connected to the master, and then the output is set equal to the input. Finally when the clock reaches the '0' level, the T5-T4 and T4-T1 branches of the circuit ensure that the slave is again isolated from the master. Thus information moves through the cell only on the clock falling edge, and by the time that it reaches the following bistable in the sequence, further movement is inhibited because the clock has reached ground potential.

The operation of the M.O.S. dynamic shift register shown in figure 40 is similar to that of the static logic circuit. The parasitic capacitances are indicated in the diagram and clocked loads are used to reduce the power dissipation. A '0' level (negative voltage) applied to Driver A will charge up the capacitance, and providing that the following Transfer Gate A turns ON whilst there is still sufficient charge present, a voltage close to ground ('1') will be presented to the gate of Driver B, discharging its associated capacitance. When Gate A has gone OFF and Gate B is turned ON, the output assumes a '0' value from the Loads B. A photograph of this particular circuit is given in figure 45(a).

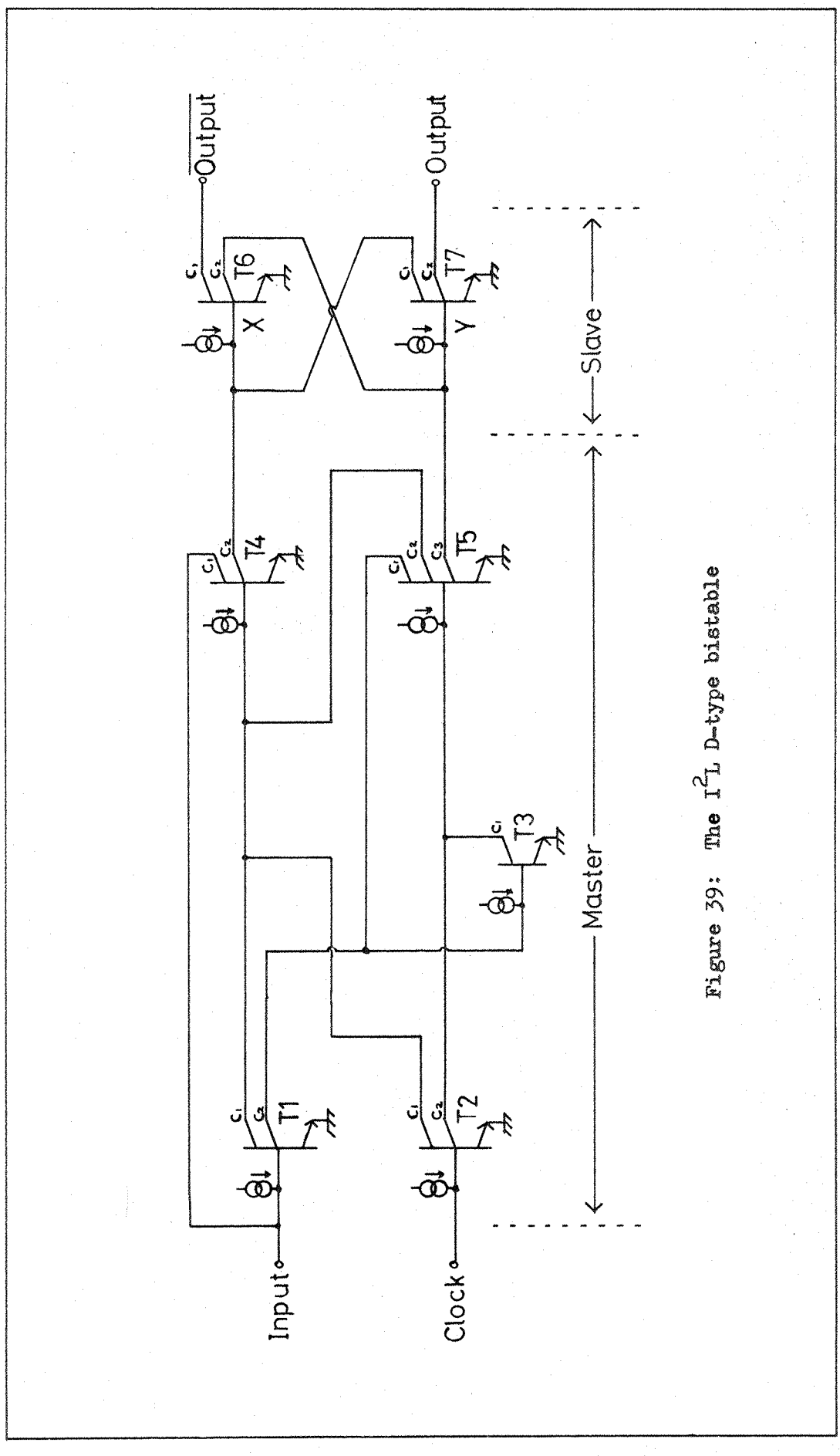
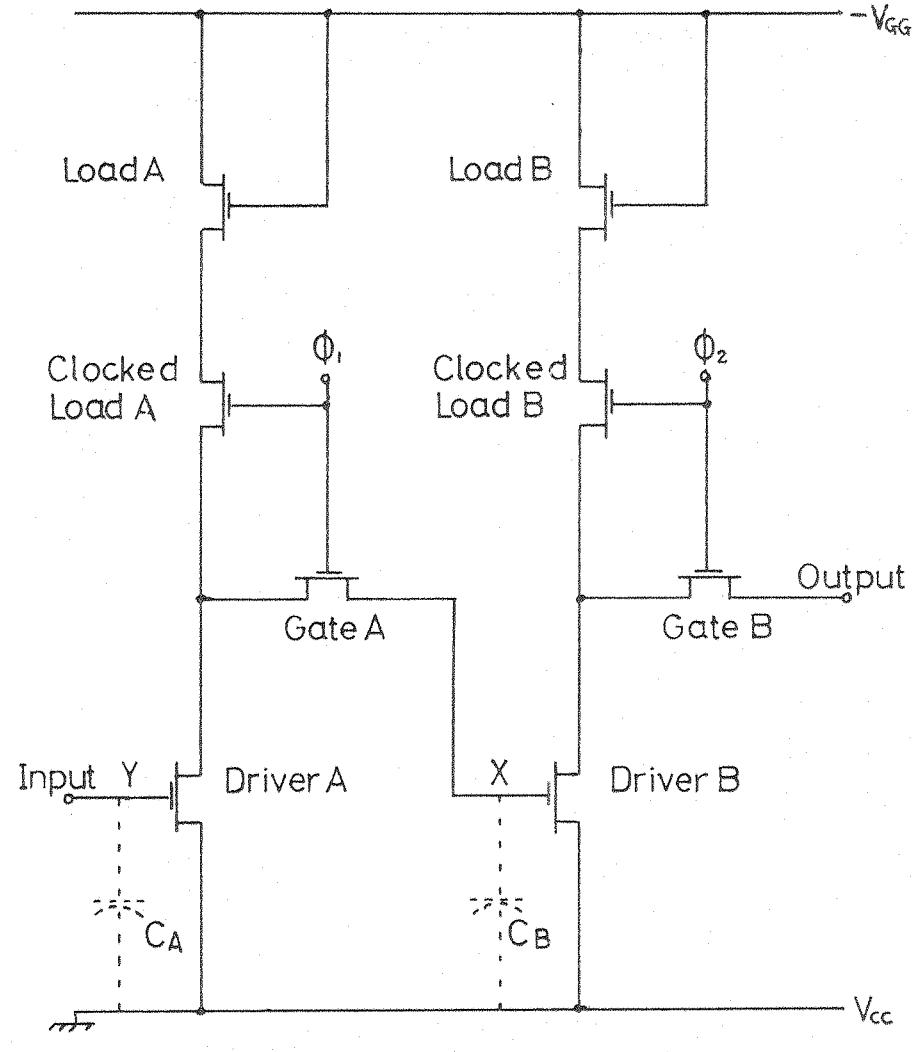
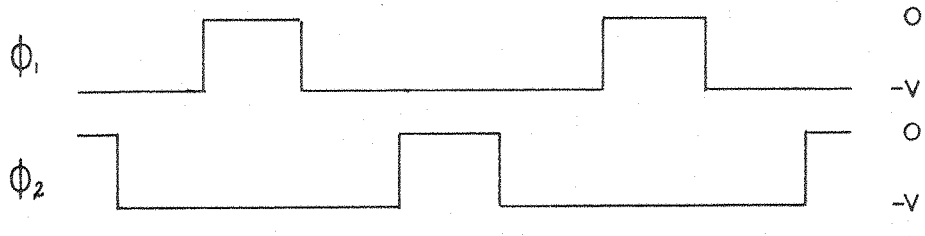


Figure 39: The I^2L D-type bistable



(a) 1-bit of the register



(b) Externally-generated clock waveforms

Figure 40: The DL-6-2128 dynamic shift register

5.3.2 Optical data insertion

Both a '0' and a '1' can be injected into every bit of each of the above shift registers using the focussed laser beam, overriding the data that were previously stored there.

An n-type substrate is used for the M.O.S. logic circuits, and this is held at the most positive potential in the circuit, i.e. V_{CC}, to ensure that the pn-junction which it forms with the p-type source and drain regions can never become forward biassed. If the light beam is directed at one such diffusion, the photocurrent will try to raise its potential to close to that of the substrate, i.e. logical '1'.

When the beam is positioned at node X in the static shift register circuit (see figure 38) and assuming that the laser power is sufficient to drive the potential high enough to be registered as a '1' level by the rest of the circuit, **node X can be driven high. As a result,** Driver A will turn OFF and Driver B ON, producing a stable state with the cell holding a '1' value, even if the laser is subsequently removed. Similarly, illumination of node Y will produce a '0' level at the cell output. The same result would be obtained if the laser probe was directed at the appropriate load-driver connections, but the minimum photocurrent necessary to change the information stored in the cell will be greater than in the previous case because of the ON-impedance of the transfer gates. The state of **the clocks governing data flow through these gates** will also influence the laser power requirements, and this is discussed in detail in section 5.5.2.

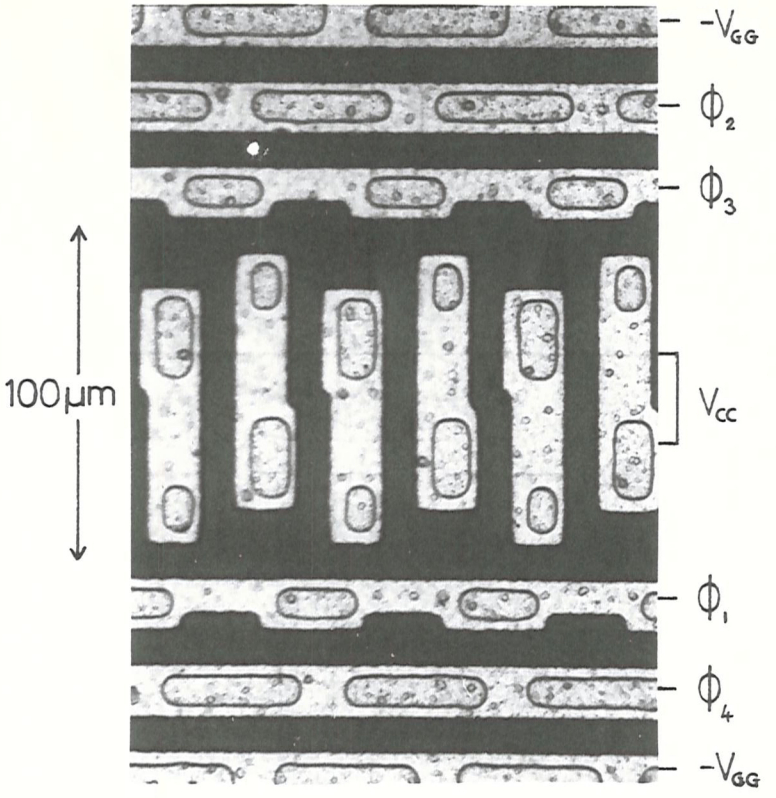
In an analogous way, both a logical '0' and '1' can be written into the M.O.S. dynamic shift register, but the laser beam powers needed are significantly smaller than for the static shift register, because the parasitic capacitance needs only to be discharged **to destroy the '0'** value previously held. In each 2-inverter cell, only one capacitance will be charged so the information stored in the bit can be inverted by directing the beam at the appropriate site; at node X, the laser can force the output to a '1', and vice versa for node Y.

In the I^2L D-bistable, the output can be changed by directing the laser probe at the base-collector junction of either T6 or T7 (see figure 39) depending upon the state of the previous output, but least beam power is needed when the clock is at the '1' level, i.e. when the cross-coupled output NAND-gates are isolated from the rest of the circuit. Again, illumination of node X produces a '1' output and a '0' results at node Y.

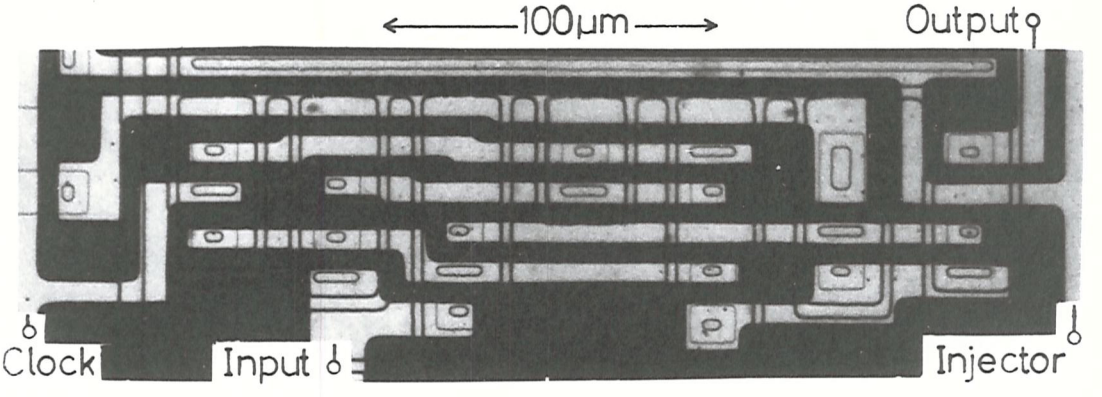
The electro-optic modulator has been used to vary the laser beam intensity, with the result as shown in figure 41(c). The beam was directed at a node X (where a '1' is optically inserted), when the register previously held '0''s in each bit. The clock was set at a 1MHz frequency and is shown as the bottom waveform. The laser 'input' is the upper trace, where the higher level is equivalent to the light-ON condition and the lower level indicates that no light reaches the register. The resulting register output is shown in the centre of the photograph: this can be seen to reproduce the light input sequence but is delayed by six clock periods, because the illuminated node X was in the sixth bit from the end of the register.

This experiment demonstrates two distinct features of the laser test method. First, data can be inserted at a chosen site in much the same way as if there was direct access to that point via a conventional input. Even though the laser light can only act as a photocurrent source and not also as a sink, both logic levels can be introduced into each cell simply by changing the input position (e.g. from node X to node Y in order to inject a '0' instead of a '1'). In all types of circuit tested to date, such complementary nodes have been available so it seems that the limitation of a'one-way' input will not be serious in practice; this aspect of the laser probe operation will be discussed further in section 6.3.

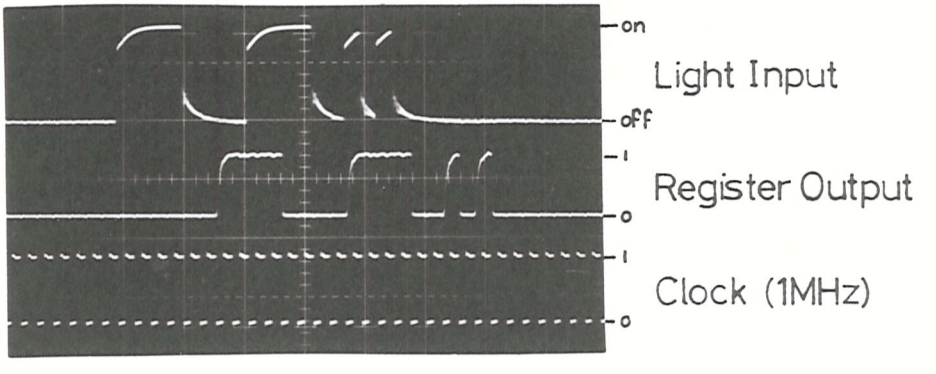
Second, the optical probe is non-contacting so it can be easily moved around the circuit, giving the tester access to many nodes. This facility is extremely useful in diagnostic testing, when precise fault location can be achieved by choosing input sites as close as possible to the faulty area of the device. For example, if there was a failure in the shift register, such as a simple stuck-at-'1' or a degraded frequency



(a) Laser spot over node X in the static M.O.S. register



(b) 1-bit of the I²L shift register (SP540)



(c) Register response to the light input

Figure 41: Laser probing of static shift registers

response, normal test methods would only discover that the register as a whole was faulty. A microprobe could then be used to locate the logical type of fault if the aluminium interconnections were reasonably large and the operator dexterous, but it is unlikely that the parametric failure mechanisms would be found. The only alternative would be to perform a critical examination of the whole register, which could be hundreds of bits long. If the laser probe was used though, the beam could be moved systematically along the register and the faulty cell would be found when the expected output response was not observed. For the parametric fault example, the register could be operated just above its cut-off frequency and then the same method of fault location would be used. If no fault was found in the chain of bits, the search would then be directed to the input/output circuitry and clock generators. In this way the fault can be isolated to one particular transistor or node (such as a faulty driver or 'slow' transfer gate), so a detailed examination can be performed to determine the precise cause of the failure.

The diagnostic testing aspect of the laser probe will only be discussed with reference to a few specific circuits in the remainder of this work, but detailed results of the laser powers needed to insert data into the shift registers and also a variety of other types of circuit will be given in the following section.

5.4 Laser Probing of Different I.C. Families

Modern integrated circuits are manufactured using a bewildering variety of technologies[72], therefore, in order to determine the feasibility of the laser method of i.c. testing, experiments ought to be performed on a representative sample of devices from each of the types which are now being produced. This would ensure that the laser power is strong enough to input data into a circuit and that the internal test sites were both accessible to the light beam and not too close to each other. However, only five different logic families have been studied in this fashion - p-channel M.O.S., I^2L, standard and low-power schottky T.T.L. and C.M.O.S.,

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but the results have shown that a reasonably accurate prediction of the criteria for successful laser probing can be made, so an analytical method has been used to determine the light beam power levels which will be necessary to optically test other types of circuitry.

5.4.1 p-Channel static M.O.S. logic

Five different i.c.'s in this class have been investigated:- these were three Al-gate shift registers from General Instruments, which also had a nitride layer over the gate oxide (the 1,1,2,4,8,16-bit SS-6-1032, 4 x 32-bit SL-6-4032 and 2 x 64-bit SL-6-2064), one poly--silicon gate 2 x 100-bit shift register from Mullards (type GYN111) and a Plessey Al-gate television touch tuner (ML232B). At least four of each of the metal-gate devices have been used, so 'average' results are given in this section although very little inter-device variation has actually been observed.

5.4.1.1 The M.O.S. static shift register

The effects of laser illumination upon the operation of the shift register have been outlined in qualitative terms in the previous section. With M.O.S. circuitry, the channel itself is not often optically acc--essible (because of the gate metal overlay) and neither is the driver-source or load-drain in an inverter circuit. The p-type diffusions linking the various transistors are usually metal-free though, and form suitable photodiodes which can be used for laser probing. The laser beam should be focussed onto the junction edge for maximum effect, but if it is incident upon the substrate or diffusion close by, the result will be the same although the laser power requirement will rise (see section 4.1). In the following measurements, the quoted beam powers refer to the power at the surface of the circuit under test when the beam is positioned over the junction edge, and so are the minimum levels which are necessary to produce a given change in the observable output. Conversion to an equivalent photocurrent can be easily made by reference to equation (4.1) and table 2 for values of quantum efficiency.

For the shift register circuits, the same minimum laser power is necessary to change the information stored in any cell to either a logical '0' or '1'. In the case of the SS-6-1032, a power of 52μW was required to change the output when the beam was positioned over the driver-load interconnection (see figure 38) but only 6.8μW at nodes X or Y produced an identical reaction if a continuous light intensity is maintained.

It is also possible to insert data into two adjacent cells simultaneously if the power is increased to 874μW, i.e. 130 times the minimum level. This result confirms the nodal isolation theory which was presented in section 4.3.4: from the photograph in figure 41(a), the distance between adjacent bits can be seen to be 67μm and the closest junction to the sensitive nodes X or Y, the driver-load diffusion, is only 24μm away (the diffusion length is 17.6μm). Without this disturbing influence, a 47-fold power increase above the minimum level would be needed to affect two node X's or Y's together, well below the ratio measured in practice.

The state of the transfer gates also has an effect upon the laser power requirements for data insertion, and it has been found that if a synchronised modulated beam is used so that light only reaches node X when **Transfer Gate** B is fully ON, then 21μW instead of the minimum 6.8μW is needed to drive the output high. The relationship between the transfer gate impedance and the laser power will be studied in detail in section 5.5.2. As expected for a static logic circuit, the clock frequency has very little influence upon the results, but close to the upper limit (1.2MHz in this case) it has been found that the feedback loop never has time to close; as a consequence, the device behaves as a dynamic register and some frequency dependence of the minimum laser power has been observed when this condition is reached.

Each of the three types of G.I. register tested had identical cell layout and driving circuitry, but even though the results obtained in every case were of a similar form, the magnitude of the necessary beam

power was dependent upon the length of the register, as shown in table 6. This relationship probably arises because the loading on the clock generation circuitry varies in proportion to the number of transfer gates, resulting in a degradation of switching speed for the longer registers. When the delay between one pair of gates turning OFF and the others coming ON increases, less photocurrent will be necessary to accomplish the change of state (see section 5.5.2) and so the minimum laser power will drop as the number of bits rises.

Device	No. of bits	Minimum laser power (μW)
SS-6-1032	16	6.8
SL-6-4032	32	3.4
SL-6-2064	64	1.2

Table 6: Data insertion into G.I. static shift registers

The polysilicon-gate GYN111 has a smaller cell geometry than the Al-gate registers, but here again a large increase in power (126 times) over the minimum level of 1.5μW is needed to input data into two bits simultaneously. The sensitive node X junction is partially obscured by metallization, but the laser beam can penetrate through the silicon gate to the channel in some cases. The light-probe power requirements of this circuit are comparable with those of the M.N.O.S. devices, and this is expected because the change in gate material will not greatly affect the current-handling characteristics of the similar-geometry transistors.

A detailed analysis of the Al-gate register cell has been made in order to relate the laser power requirements to the circuit parameters. The equations describing M.O.S. transistor operation are given in Appendix 6, and from these the steady-state currents and voltages at each point in the circuit have been calculated, with the results shown in figure 42 (the transistor w/l ratios are circled).

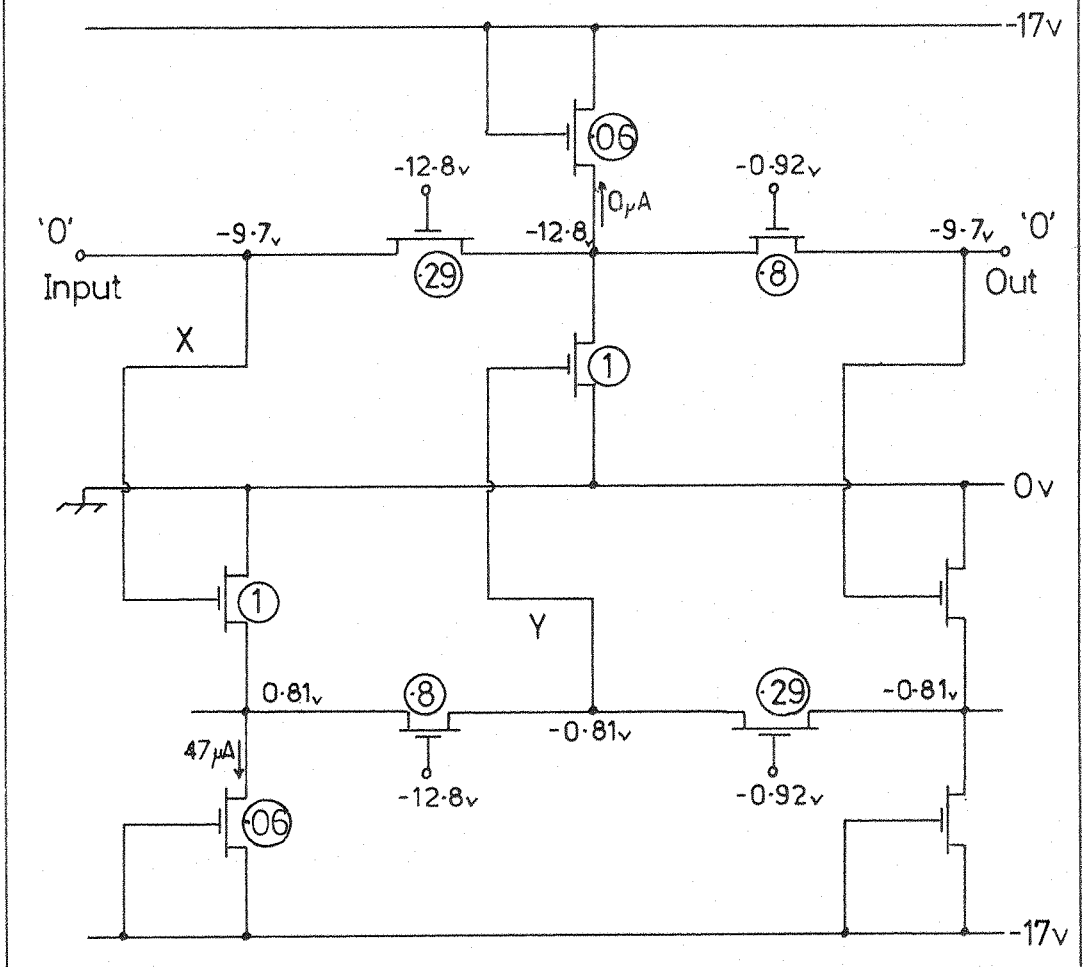


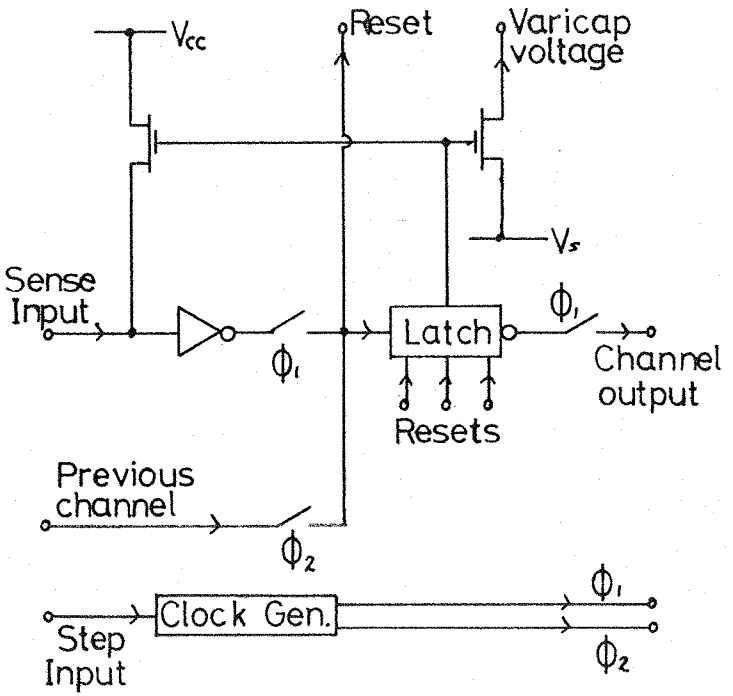
Figure 42: D.C. analysis of the SS-6-1032 shift register

When the laser beam is directed at the driver-drain diffusion which is initially at -12.8v, the photocurrent flowing from the substrate will try to raise its potential but at the same time the load impedance will alter. As shown by graphical analysis, a 'break-point' is reached when a current of 22.5μA is supplied by the load; with a higher current the output rises above -4.5v and a logical '1' state is reached. The measured 52μW laser power which was necessary to perform this task is equivalent to a photocurrent of 18.5μA, which shows good agreement with the calculation.

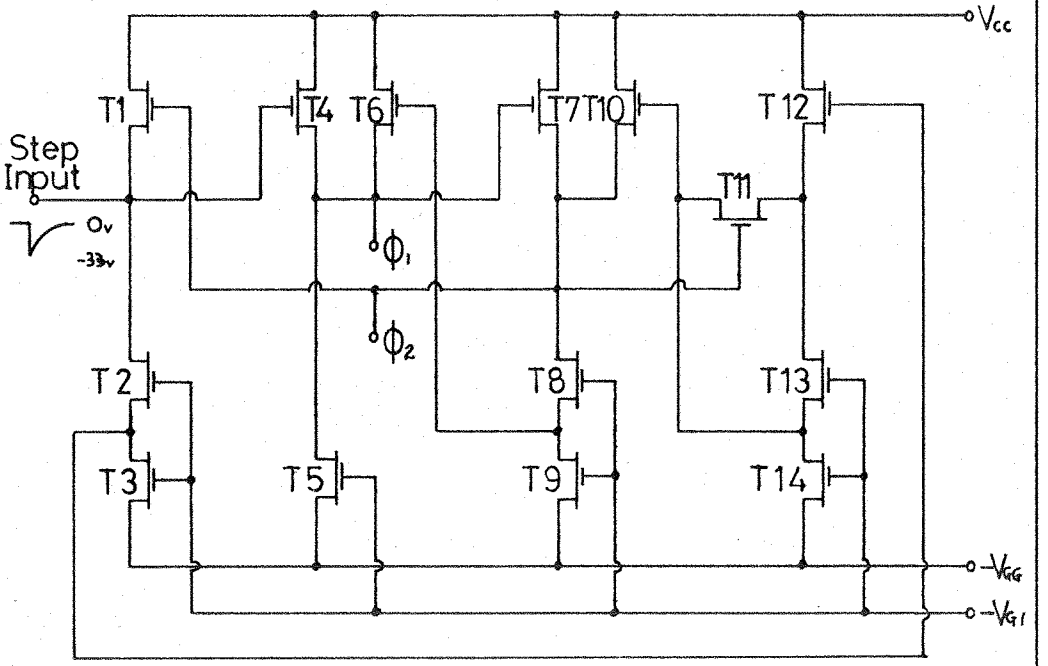
If one of the 'slow' Transfer Gates B or D was OFF when its partner (i.e. Gate A or C) was ON, the photocurrent would only have to discharge a parasitic capacitance in order to change the logic level at the input of each inverter, and this should be equivalent to the case for least laser power. In practice though, the minimum power level necessary for data insertion occurs at a time when one of the slow transfer gates is partially ON with the faster gate fully ON (section 5.5.2) so this approximation will lead to an underestimate of the minimum laser power required at nodes X or Y. The value of capacitance can be calculated to be 0.10μF from a knowledge of the voltage swings, transistor geometry and processing parameters (Appendix 6), and so a discharge current of 1.6μA for the SS-6-1032 is predicted, in which the time delay between the turn OFF of one transfer gate pair and the turn ON of the next slow gate has been found to be 330nsec (section 5.5.2). This would require a laser power of 4.4μW, which is slightly less than the 6.8μW measured for the reason described above.

5.4.1.2 The ML232B T.V. touch tuner

One channel out of the six in the Plessey ML232B touch tuner is shown schematically in figure 43(a). The circuit consists basically of a bistable whose state is determined by reset controls from each of the other channels so that only one is selected at a time, and either an input signal from a touch plate arrangement or the previous channel output, depending upon the clocks ϕ_1 and ϕ_2. Therefore both manual



(a) Block diagram of 1 channel



(b) Clock generation circuit

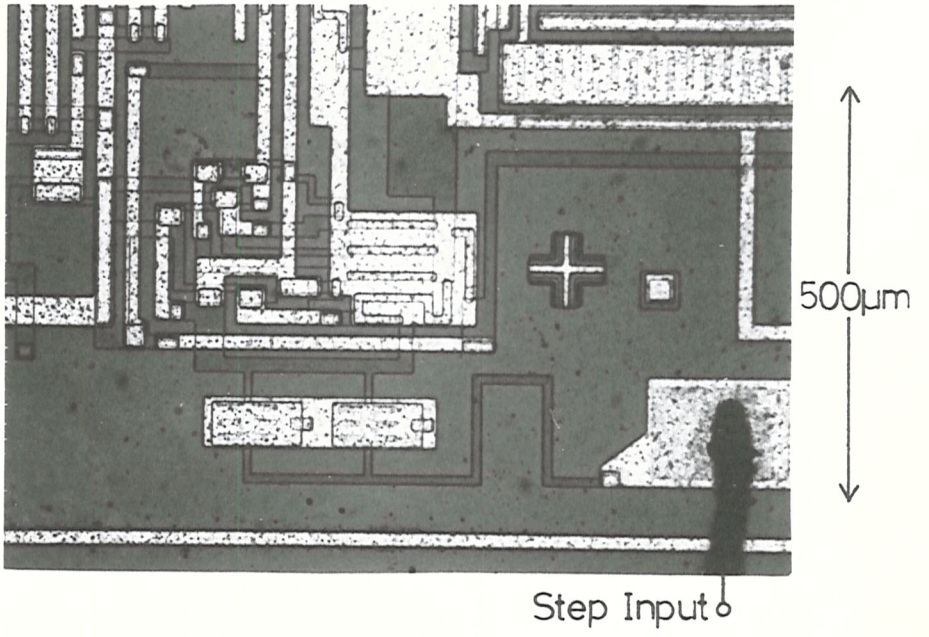
Figure 43: The Plessey ML232B touch tuner

and sequential channel selection can be used to control the voltage which is applied to an external varicap diode.

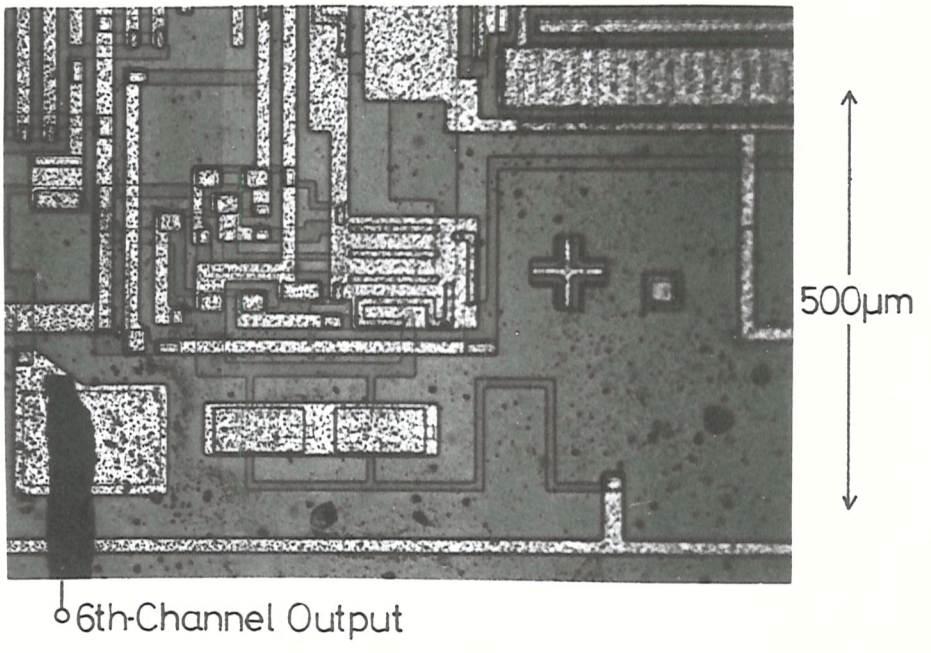
Again a low-powered laser beam was sufficient to modify the circuit behaviour: the state of the latch could be changed in both directions with a power of 20μW when the light spot was directed at the drain diffusion of an OFF transistor, the clock control circuitry could be overridden with under 70μW beam power, and at the sensitive sense inputs 8μW was enough to select one particular channel.

The clock generator is detailed in figure 43(b), and here also the laser probe can be used to alter the logical operation of the circuit, with an average power of 80μW. When the step-input diffusion is illuminated, its potential can be raised high enough to prevent T4 from turning ON, even when a negative input pulse is applied, thereby disabling the sequential channel selection function. Conversley, if the beam is directed at either the drain or source of T11 or T13, then $\emptyset_2$ is driven negative and simultaneously $\emptyset_1$ rises in potential and the action of a step input pulse is imitated. For a steady light beam at this position, control switches from channel to channel at a rate which is determined by the response time of the latch circuit, but if discrete light pulses of less than 60μsec duration are applied, then only the next channel in sequence is selected. Similarly, if 60-120μsec wide light pulses are used, the next-but-one channel is reached etc. At other photodiodes within the clock generation circuitry, either $\emptyset_1$ or $\emptyset_2$ individually can be forced to the '0' or '1' levels with the laser, and the effect upon the channel selection network is as expected for these conditions, which cannot occur during normal operation of the device.

Every one of the seven inputs to this circuit could be replaced by a laser beam, and this has been well demonstrated by one particular touch tuner in which the metallization pattern had been changed so that no access was provided to the step input (the spare contact pad was used as an observation or test point at the output of the sixth channel). This can be seen by comparing the two photographs in figure 44, where the conventional circuit shown above has its contact to the clock cir-cuit at the bottom right hand side. The modified circuit could be made to operate normally in every respect by using a pulsed light beam



(a) Normal ML232B touch tuner (clock circuit)



(b) ML232B with no step input connection

Figure 44: Conventional input simulation by the laser probe

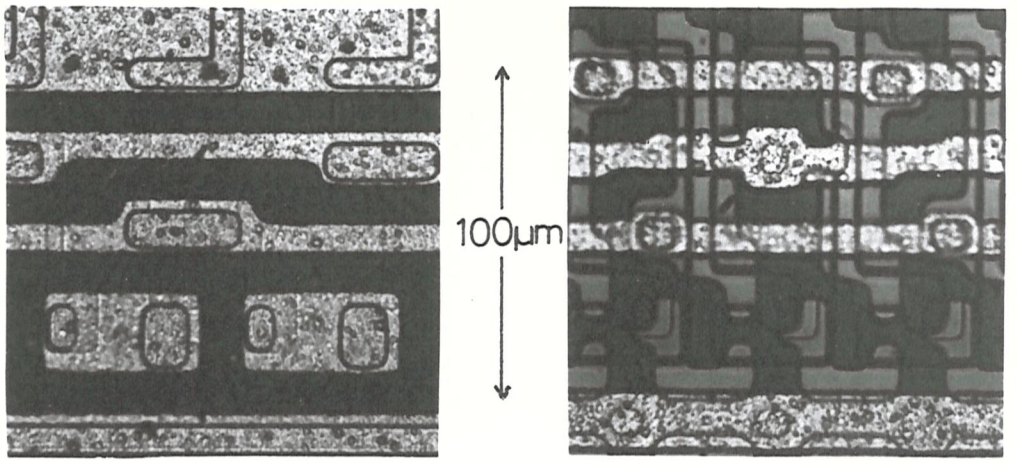
to simulate the step input, as described above.

In general, static M.O.S. logic dissipates about 1mW per bit [73], so laser powers in the 10-200μW range (4 - 70μA) should be adequate for data insertion. Any pseudo-dynamic operation (such as the case when the transfer gates are OFF in the shift register) could reduce the value by upto an order of magnitude.

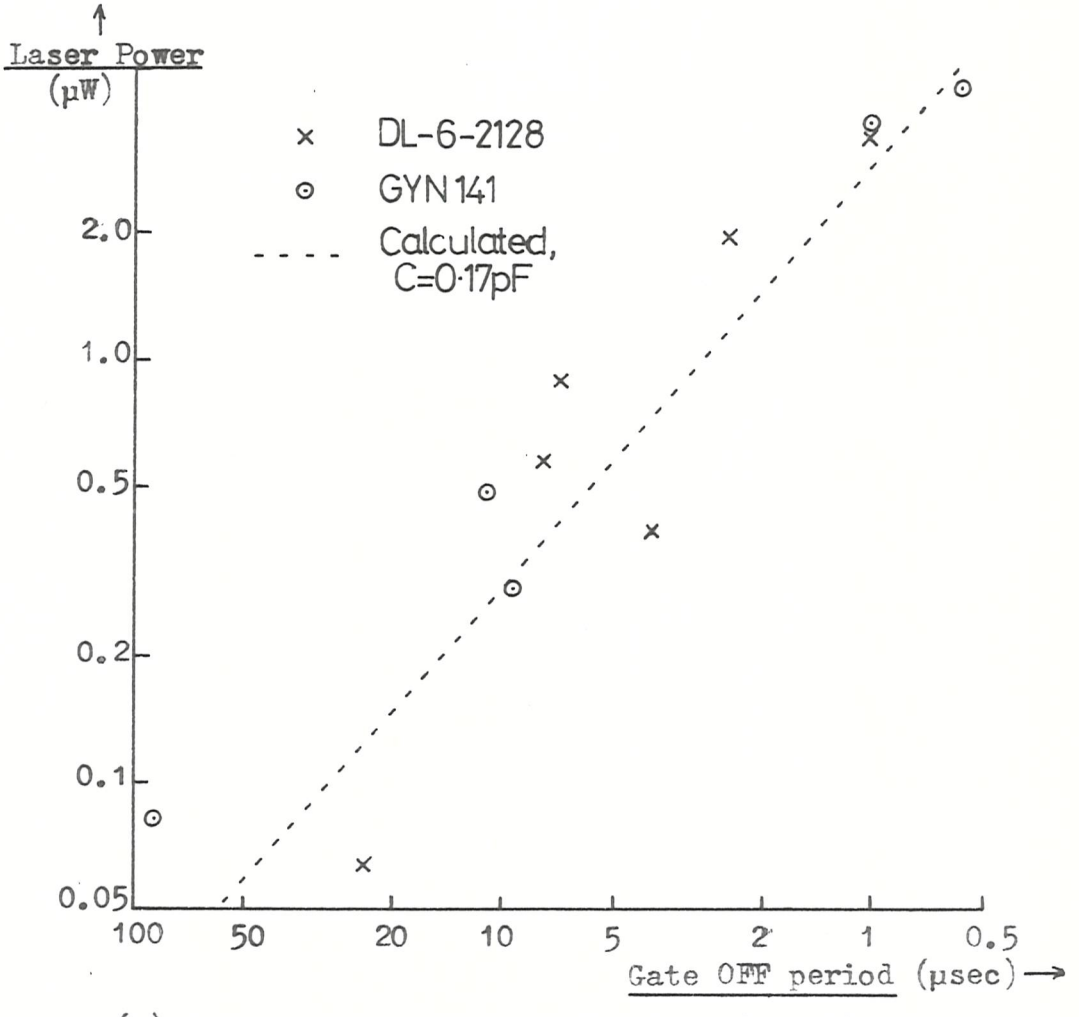
5.4.2 p-Channel dynamic M.O.S. logic

Two dynamic shift registers represent this device class: a 2 x 128-bit Al-gate from General Instruments (DL-6-2128) and a Mullard 4 x 256-bit Si-gate, type GYN141. In each case the lower frequency limit is 10kHz and the circuit configuration is similar except that the fixed Loads A and B (see figure 40) are omitted in the Si-gate device to reduce cell size and power dissipation. Photographs of both are shown in figure 45(a), and the area per bit can be seen to be approximately one third of that in the static registers.

Least laser power is needed to change the information held in each cell when the beam is directed at the diffusion between the transfer gate and following driver, i.e. nodes X and Y (figure 40). The power levels were in general less than the minimum required for the static logic circuits, but the value was dependent upon the clock frequency, or more precisely the time interval between one transfer gate turning OFF and the next coming ON; the two non-overlapping clock waveforms are externally generated, so this delay can be carefully controlled. If a long gap between successive clock pulses is allowed, then the parasitic capacitance will lose a significant porportion of its charge by leakage so that only a small photocurrent is needed to finally discharge it and the minimum laser power level will be low; as the gap decreases, the laser power requirement will rise correspondingly. The results of experiments performed on both registers to demonstrate this relationship are shown in figure 45(b). The laser probe has been positioned at node X or Y and the power required to force the output to a '1' or '0' when using a continuous light beam is shown as a function of the time delay between



(a) Photographs of the two dynamic registers



(b) Laser power necessary for data insertion

Figure 45: Dynamic p-channel M.O.S. shift register

successive clock pulses. When the registers are operated close to their lower frequency limits, light powers of less than 0.1μW affect the circuit output, but this level rises by nearly two orders of magnitude when the capacitance is allowed less than about 1μsec for its charge to leak away before the discharge is completed by the laser. The effective capacitance is calculated to be 0.17pF so an estimation of the necessary discharge current as a function of time delay can be made, and this has been included in the same figure.

The laser probe can also be used to drive the output high or low when it is positioned over the load-source or driver-drain diffusions, but a 50-80μW spot power (18-28μA) independent of the clock waveforms is needed; this is similar to the values measured for the static register. Obviously the latest dynamic circuit designs using four-phase ratioless logic for example (where the power dissipation is typically 0.1mW/bit or a tenth of value associated with the above circuits) will need proportionally less laser power if the photocurrent is used to match load currents; however, for the capacitance discharging function the main limitations will still be the initial time allowed for charge leakage and the size of the capacitance, so it is likely that a power in the range of 0.05-50μW should be adequate for testing dynamic logic M.O.S. circuitry over a 10kHz-5MHz range of operating frequency.

5.4.3 Integrated injection logic

Only one member of the I^2L logic family has been optically probed, but it has been possible to obtain some indications about the suitability of laser testing for this particular type of i.c. The circuit which has been studied is a pseudo-random binary sequence generator from Plessey (type SP540): this comprises of a string of 14 D-bistables, each separated by EOR-gates which are fed in bit-parallel format from a 13-bit shift register (see figure 46). The implementation of each D-bistable is identical, and has been described in section 5.3.1.

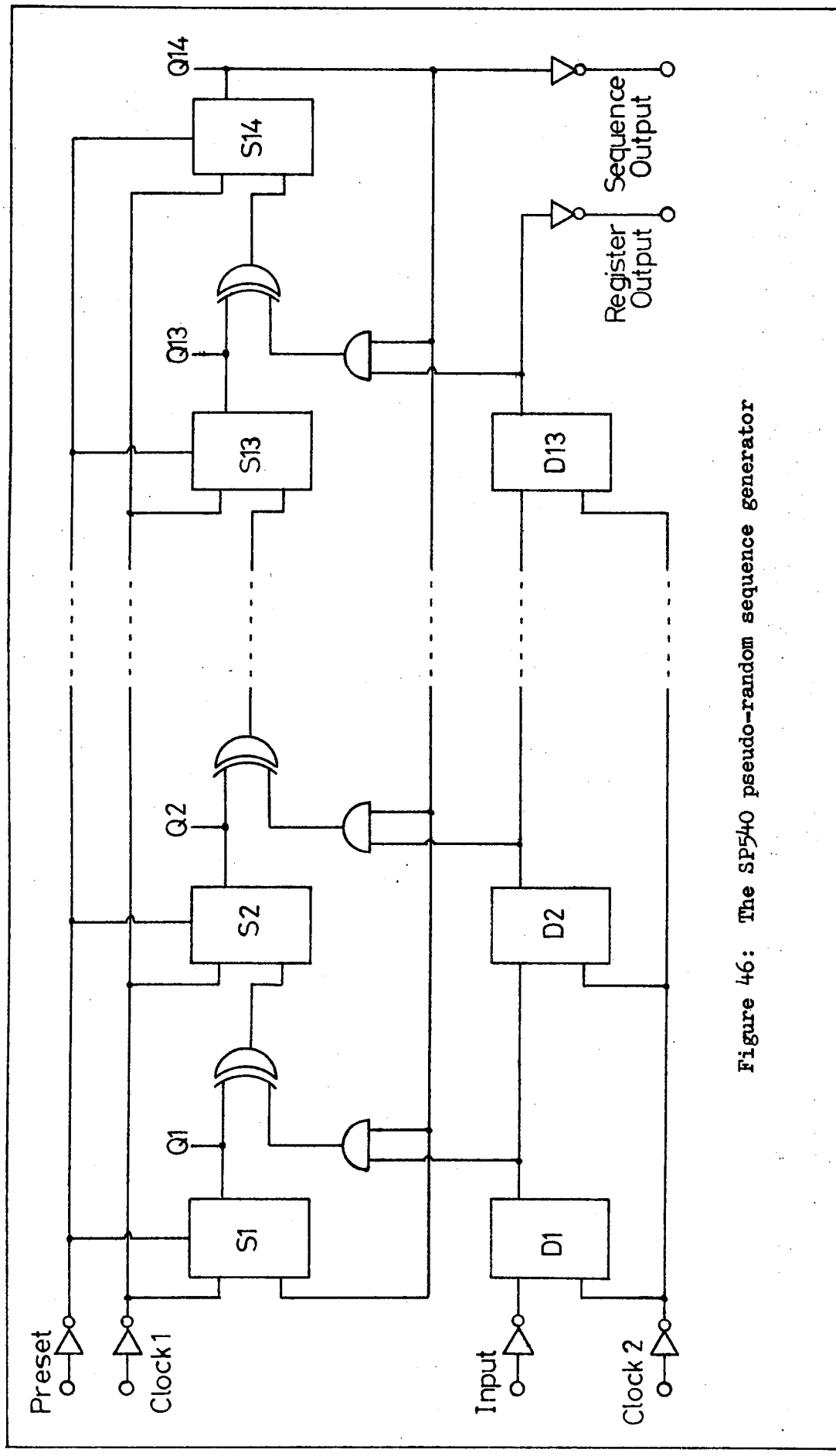


Figure 46: The SP540 pseudo-random sequence generator

At a clock frequency of 3kHz and with a total injection current of 50mA, a laser power of 300μW is sufficient to force the output of a bistable to a logical '1' and slightly less (230μW) can introduce a '0'. These results were measured when the base-collector junctions of the output transistors T6 and T7 (figure 39) were illuminated and the clock was at a high potential, i.e. the '1' level: in this case the photocurrent has only to match the current from the pnp injector which flows to ground through the ON transistor in the S-R bistable in order to change the state of the circuit, because the slave is isolated from the master; the disparity in the power levels needed to insert a '1' or '0' reflects the different driving requirements associated with the following stages via the output and $\overline{\text{output}}$ branches.

Details of the effect of the light beam upon the output when it is directed at other transistors are given in table 7, and the state of the clock when each output reaction is observed is also shown. All of the results can be explained by reference to the circuit action, and in addition it has been possible to estimate the beam powers needed for data insertion in each case: these are also listed and can be seen to show reasonable agreement with the measurements.

As an example, consider the situation when the laser is directed onto the junction between the base and collector-c2 of transistor T1. The photocurrent will tend to force T3 OFF by diverting away its base drive, so that when the clock is at '0' with T2 OFF, T5 will begin to conduct and the output rises to the '1' level. In the clock = '1' period, T5 is held OFF so illumination of T1 will be ineffective. By assuming that every lateral pnp current injector is identical, and that all the current they produce flows either to ground through the collector of a saturated npn transistor or provides the base current for the following npn common emitter driver[74], the number of units of 'base drive' which the photocurrent must overcome in order to produce the observed output change can quickly be found. The common base current gain has been assumed to be 0.7 and the common emitter gain as 15,[75] so for a total injection current of 50mA, each pnp transistor is calculated to supply a current of 0.12mA which could be equalled by a 345μW laser beam if η = 70percent. Thus the expected laser power

Transistor collector	Effect of light upon the output	Clock phase sensitivity	Laser probe power (μW)	Predicted power (μW)
T1 - c1	Forced to '1'	Clock = '0'	580	690
T1 - c2	Forced to '1'	Clock = '0'	470	690
T2 - c1	Held at '1'	-	1090	1035
T2 - c2	Held at '0'	-	970	1035
T3 - c1	Held at '0'	-	850	1035
T4 - c1	Forced to '0'	Clock = '1'	570	690
T4 - c2	Forced to '0'	Clock = '1'	550	690
T5 - c1	Forced to '1'	Clock = '0'	380	345
T5 - c2	Forced to '1'	Clock = '0'	1000	1035
T5 - c3	Forced to '1'	Clock = '0'	690	690
T6 - c1	Forced to '1'	Clock = '1'	850	690
T6 - c2	Forced to '1'	Clock = '1'	300	345
T7 - c1	Forced to '0'	Clock = '1'	650	690
T7 - c2	Forced to '0'	Clock = '1'	230	345

Table 7: Laser probing of the I^2L D-type bistable

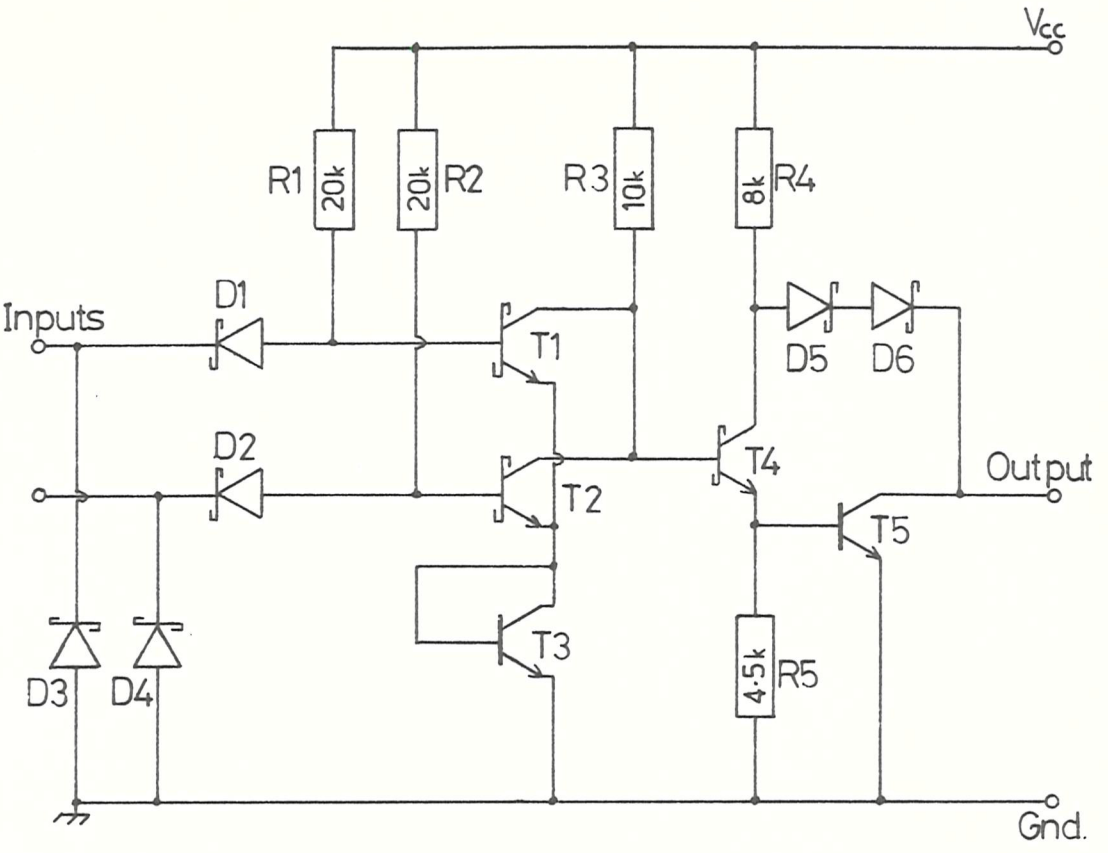
requirements at the various input sites will be multiples of 345μW, depending upon the propagation path of the laser-induced change of state. In the present example, both the T1 and T3 current supplies would have to be surmounted if the output is to be forced to the '1' level when T2 is OFF, so a light power of 690μW is predicted, rather higher than the 470μW which was measured. However in general, reasonable agreement between the estimates and practical results has been obtained, and this method can be used to calculate the laser power requirements for other circuits in this family.

The upper frequency limit of I^2L logic is inversely proportional to the injection current, so for high speed operation the laser power requirements will rise. For this circuit, the injection current range is 1-100mA for all frequencies up to 10MHz, so a laser power of 5μW-1mW should be satisfactory to cover the limits of operation and probably be adequate for optical testing of most standard I^2L m.s.i. and l.s.i. circuitry.

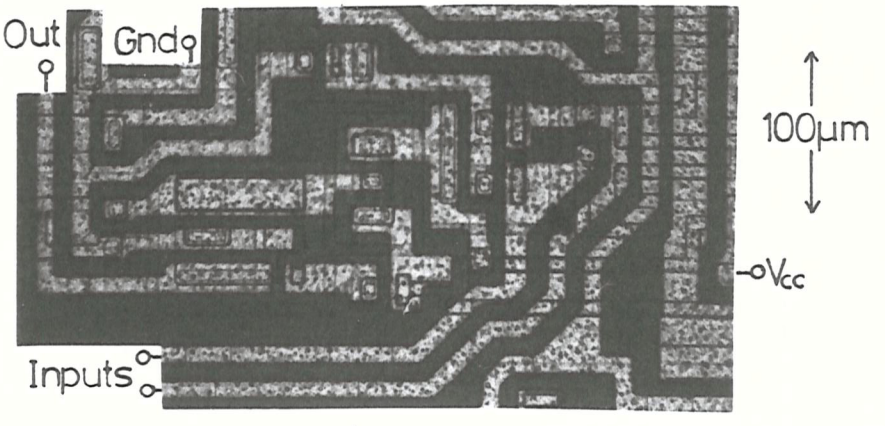
5.4.4 Low power schottky T.T.L.

The Texas Instruments SN54LS191 synchronous up/down counter has been chosen to represent the low power schottky T.T.L. logic family. A full description of this 58-gate m.s.i. device will be given in section 5.6, but the results obtained from the laser probing of two parts of the circuit, a 2-input OR-gate and a JK-bistable, will be detailed here in order to evaluate the power requirements for laser testing of L.S.T.T.L.

The simple OR-gate is shown with a photograph in figure 47. When the laser spot is directed at the base-collector junction of T1 or T2, the gate output voltage can be increased to reach the '1' level, and by changing the position of the beam to T5 the output can also be forced low. In practice, the output of the OR-gate cannot be observed directly, so any change of state can only be detected by its effect upon the rest of the circuit; thus the following values of light



(a) Circuit diagram



(b) Practical implementation

Figure 47: Low power schottky TTL OR-gate

power are those which are necessary to change the gate output potential sufficiently to overcome the noise immunity margins of successive gates.

To force the output to the '1' level, a laser power of 880μW at the base-collector junctions of T1 and T2 or 940μW at the T3 coll--ector was required, and to inject a '0', 775μW was needed at the base of T5 and 820μW at its collector. Assuming that both T4 and T5 are saturated and the values of resistance are as indicated, the base current for T4 will be 0.36mA, so a laser power of 1.01mW (η = 70 percent) should theoretically produce the high-level output. Similarly, for a V_{CE}(sat) of 0.3v for a schottky transistor, a photocurrent of 0.34mA (950μW) is predicted for '0' insertion at T5; both calculations are supported by the measured power levels.

The JK-bistable used in the 54LS191 is an interesting circuit which cannot be fully analysed at the logic level. The full diagram is given in figure 48: the top half comprises of a conventional cross--coupled NAND-gate pair with buffered output, and the 'master' element is formed by a four-transistor arrangement, in which the J and K inputs are wired together and the clock control only reaches the input transistors T1 and T2. The circuit is primed when J=K=C_p = '1'. When the clock voltage falls, either the set or reset potential drops to 0.5v (the emitters of T5 and T6) with the other node held at 0.9v: this forces the circuit output to toggle, with a 0.5v on the set line producing the low-level output and vice versa. Even though both T5 and T6 remain ON for the duration of the clock = '0' period, oscillation is prevented by diodes D1 and D2; at the same time a new J = K input is generated by other combinational logic and presented to the disabled input gate. The clock can then return to its high level in preparation for the next '1 → 0' transition when the slave will be connected to the master again. If J = K = '0' at this time, the output will retain its previous state.

The combination J = K: '1 → 0' when C_p = '1' cannot occur during normal circuit operation because of the relatively small propagation delays in the various combinational logic gates (maximum clock frequency

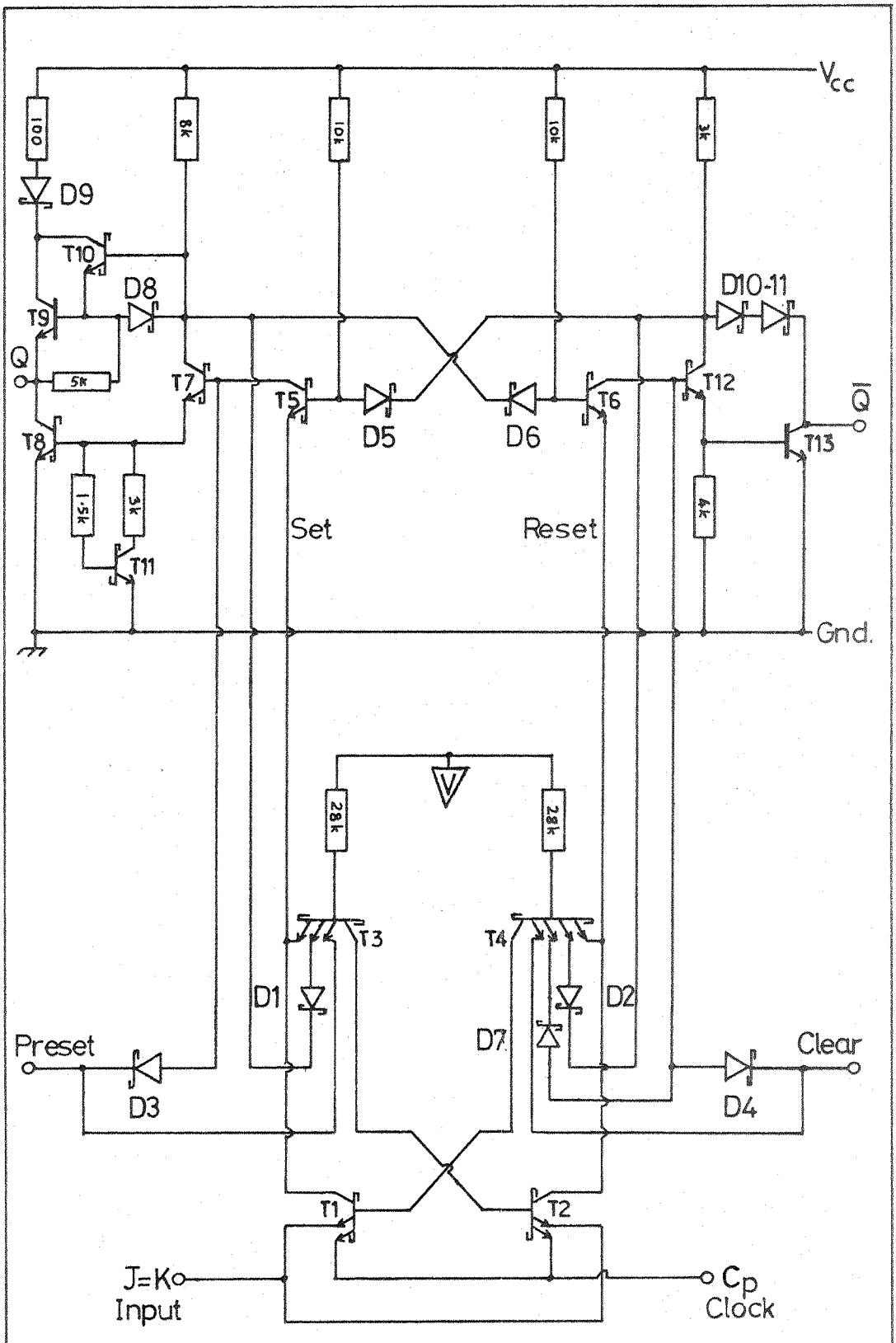


Figure 48: The JK-bistable (from the SN54LS191)

is 25MHz); however the J = K input can be driven low at any time by using the laser probe, producing some interesting consequences. For example, the output can be forced to toggle at double its normal speed with transitions occurring both on the clock '1 → 0' edge and when the J = K input is knocked from '1' to '0' by the laser, and and in this way the counting rate of the circuit can be artificially increased.

In a more conventional manner, the input gates can be overridden during any clock phase by directing the laser beam at T3 or T4 where the bistable output is immediately changed to a '1' or '0' respectively: illumination of T3 for example results in a drop in the potential of the reset, and when it reaches 0.9v, T12 will turn ON and T7 OFF, thereby producing the high-level output.

For other positions of the laser probe, the effect of the light is dependent upon the states of the inputs. In some cases though, it has been found that the power of the laser beam can also play an important part in determining the output reaction. Such a situation arises when the base-collector junction of T12 in the $\overline{\text{output}}$ branch of the circuit is chosen as the optical input site. Below a certain threshold light power level, the circuit operation is unaffected by the illumination, but as the power is increased, the buffered output can be forced to '0' when the clock is at a logical '1', but this change in state is not recognised by the combinational logic which uses the output level to determine the next-state inputs. When the beam power rises still further, the observable output is still forced to '0' only for the duration of the clock = '1' period but now this low-level output is used to determine the next-state inputs, and the counting sequence is disturbed. Finally with a much higher laser power, the output can be forced to '0' irrespective of the clock input control.

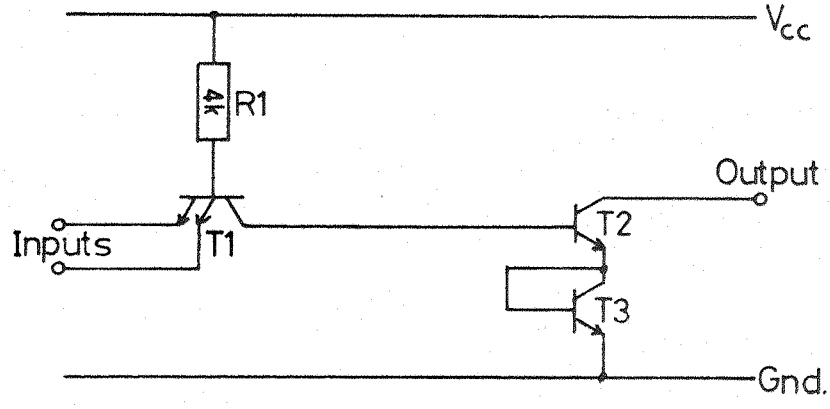
The versatility of the laser input is well demonstrated by these experiments, where not only have both '1' and '0''s been injected into a circuit (since complementary nodes have been available) but also a 'can't happen' condition has been introduced and an indication of the circuit operation has been obtained from the observations of the effect of different laser powers (or photocurrent levels). This latter facility is particularly useful for diagnostic testing purposes, and will be discussed further in section 5.5.1.

The laser powers necessary to influence the circuit behaviour of this particular m.s.i. low power schottky device have all been in a 200μW-1mW range, with the lowest values being recorded when the JK-bistable was illuminated (because of the T1-T4 latch and large 28kΩ resistors). From an inspection of other L.S.T.T.L. circuits[76], an estimate of the average power requirements for laser testing of the logic family can be formed: the size of the load resistance will play an important part in determining the current levels, and for m.s.i. and l.s.i. circuitry resistance values are similar to those in the internal gates of the 54LS191, but for buffered outputs or s.s.i. i.c.'s a slightly higher photocurrent will be needed. Thus a laser beam power of 0.2-2mW should be adequate for laser probing of low power schottky T.T.L. i.c.'s.

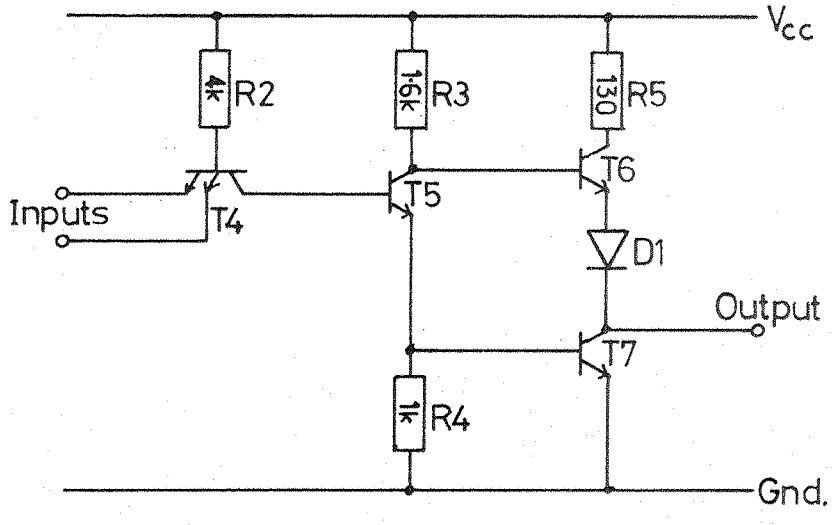
5.4.5 Standard T.T.L.

Standard T.T.L. circuits react in a similar way to the low power schottky version which has already been described when they are probed by a light beam, but the different values of circuit components will alter the laser power requirements for data insertion. Three devices of this type have been investigated: a simple NAND-gate (7400), a NAND-buffer (7440) and an edge-triggered D-bistable (7474). The bistable is formed from six NAND-gates, the first four of which are as shown in figure 49(a) and the output cross-coupled pair is comprised of buffered gates which are identical to the 7400 configuration (figure 49(b)).

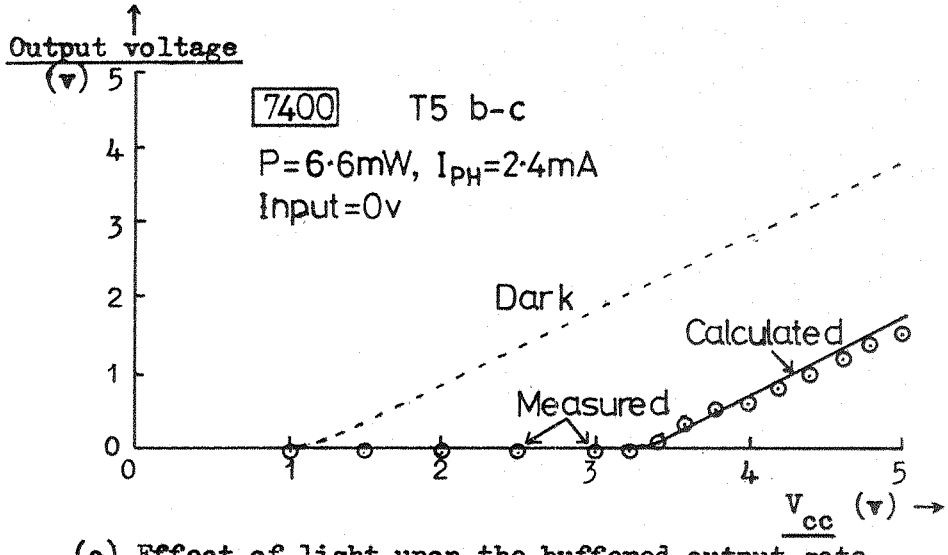
When the laser spot is directed at the base-collector junction of transistor T2 in the open-collector NAND-gate, the collector voltage will be reduced and a '0' level output can be reached. For this change of state to propagate through the rest of the circuit and so be registered at the bistable output where it can be observed, the base drive to the corresponding T2 in the following gate must be removed. If a quantum efficiency of 70percent is assumed, then a laser power of 3.8mW is calculated to be necessary to drive the gate output low, a value which is remarkably close to the 3.7mW measured in practice.



(a) Internal NAND-gate



(b) Buffered NAND-gate



(c) Effect of light upon the buffered output gate

Figure 49: The T.T.L. NAND-gates

When the collector of T1 is illuminated, its collector-to--emitter current will be increased and the T2 collector voltage can be forced high, even if the inputs are also high. Again a photocurrent of 1.34mA (or 3.8mW) is estimated for this case, and 3.6mW was the measured minimum beam power.

The NAND-gates with totem-pole outputs (figure 49(b)) have proved to require even more laser power to change the output state, and in fact the 7.5mW laser which is used for these experiments is often not strong enough. A photocurrent of 2.9mA, equivalent to a power at the focussed spot of 8.2mW, is the calculated value necessary to input a '0', but if the V_{CC} supply is lowered below the normal +5v though, the currents flowing within the circuit are correspondingly reduced and it is then possible to drive the output low with the present laser.

A plot of the output voltage as a function of the supply voltage for '0' level inputs is given in figure 49(c), and the effects of a 6.6mW beam of light (obtained when the laser was performing above its specifications) directed at the base-collector junction of transistor T5 are also shown, both with measured values (data points) and the calculated response (solid line). A '0' level of 0.8v is reached when V_{CC} falls below 4.2v, and a 0v output is produced for V_{CC} = 3.3v. If the usual 5v supply is used, extrapolation shows that a 7.9mW beam is necessary to force the output low: at least a 28mW laser would be required to provide this spot power if the modulator was included in the optical system.

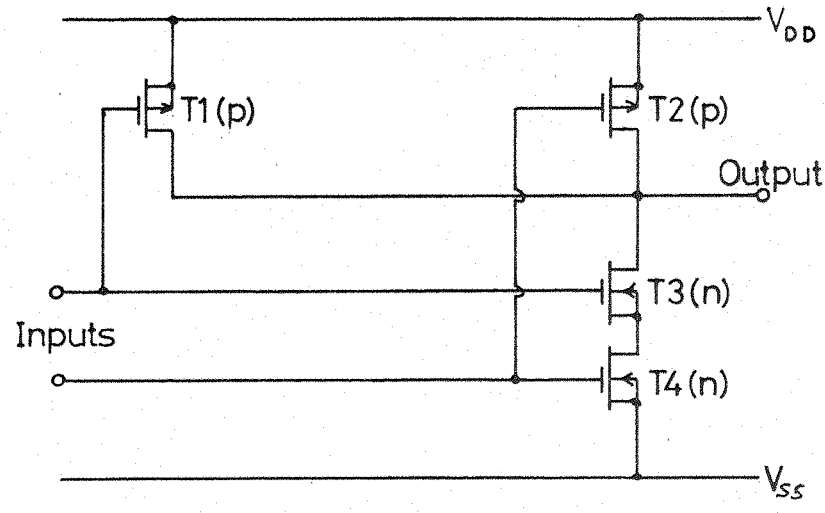
Standard T.T.L. will therefore not be suitable for testing with a small, cheap laser if all the gates are implemented in a similar form to the 7400; however in m.s.i. and l.s.i. circuitry only the output gates are buffered,with the simpler open-collector configurations used for the internal logic (where the driving requirements are less), so the power levels needed will not be as high. From a survey of the common T.T.L. i.c.'s[76,77] it seems probable that a 3-6mW focussed beam power will be adequate for laser testing purposes, with 8-10mW needed for the output stages when the conventional supply voltages are used.

5.4.6 Complementary M.O.S. logic

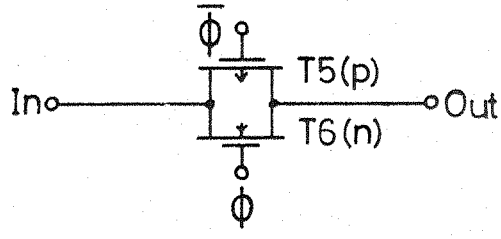
C.M.O.S. i.c.'s are characterized by very small power dissipation[78], so it would seem likely that low laser beam powers will be sufficient to inject information into the internal circuitry; in practice however, the reverse has proved to be the case. Five devices in the RCA CD4000 series have been studied:- three basic gates: CD4011 (NAND), CD4012 (NAND), CD4001 (NOR) and two bistables: CD4013 (D-type), CD4027 (JK). Acid etching has been used to remove the plastic encapsulation, but the electrical performance was not affected by this treatment so it has been assumed that the circuits did not suffer permanent damage.

The two gates shown in figure 50(a) and (b) are typical of those found in nearly all devices of this family: the first is a 2-input NAND-gate and the second is a complementary pair transfer gate, which in this example presents a low impedance (i.e. turns ON) when the clock potential goes positive. The output gates for the larger circuits are designed in the same form as the internal gates but they are made physically larger in order to increase their current-sinking capacity. A positive gate voltage ($+V_{DD}$) will turn ON the n-channel transistor and a '0' level or V_{SS} is needed to overcome the threshold for the p-channel device; the threshold voltage for both can range from 0.7v to 2.8v[79], so the 'average' value of V_T = 1.5v has been assumed in all calculations.

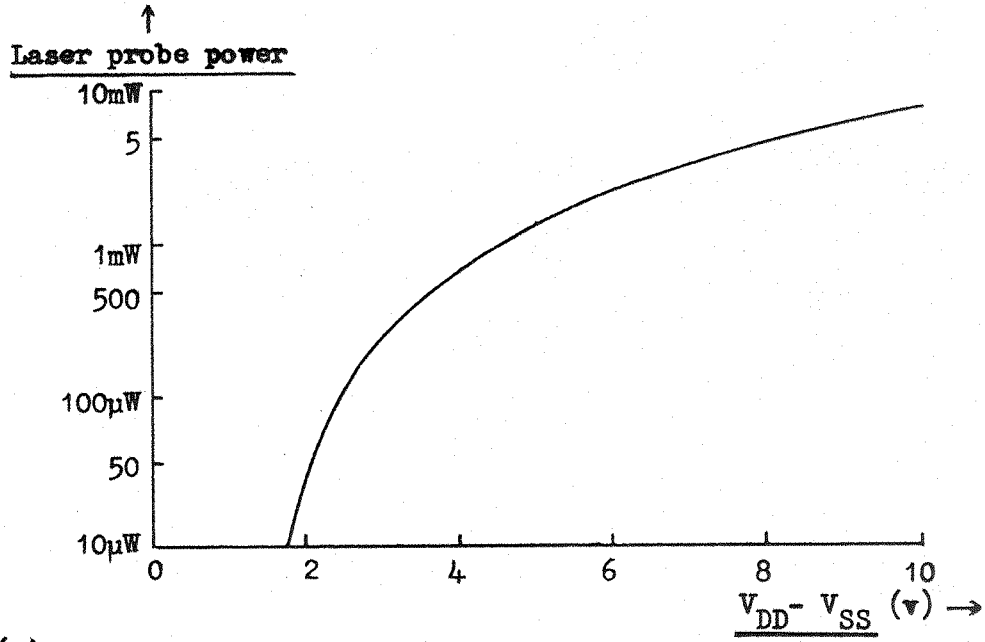
If the NAND-gate is illuminated, very little change in the output potential is noted when the $V_{DD} - V_{SS}$ supply is set to 10v, even if full laser power is used. The reason for this is that with every input combination, one transistor in each complementary pair is in the ON state and the other OFF; thus in order to change the output level by optical means, the injected photocurrent would have to at least equal the current which can be drawn through the ON device, and this can be quite large (typically 1-3mA), because the C.M.O.S. gate is designed to have a fast switching speed. Only by lowering the $V_{DD} - V_{SS}$ level and the input voltage is it possible to change the gate output using the present laser: the CD4000 family usually continues to function correctly down to a $V_{DD} - V_{SS}$ supply of 2v, but the frequency response is obviously impaired.



(a) 2-input NAND-gate



(b) Transfer gate



(c) Laser power necessary for data insertion into a NAND-gate

Figure 50: C.M.O.S. integrated circuits

When, for example, the laser was directed at the source of a p-channel transistor in an internal NAND-gate in one of the bistables, the output was forced to the '1' level with a 3.7μW beam power when $V_{IN} - V_{SS} = 1.7v$ and $V_{DD} - V_{SS} = 2.4v$; also by positioning the light spot over an n-channel device under the same conditions except that the input voltage (V_{IN}) was lowered to V_{SS}, a low-level output could be produced with a power of 97μW. If the factor β' (Appendix 6) is taken to be $20 \times 10^{-6} A/v^2$ for the n-channel and $10 \times 10^{-6} A/v^2$ for the p-channel transistors[80], the current-sinking capacity of the ON transistor can be calculated to be 1.6μA and 24.3μA respectively for the n- and p-devices under the above conditions. This corresponds to laser powers of 4.5μW and 68μW if $\eta = 70$percent, reasonably close to the measured values. The quantum efficiency will be less for the n-channel transistor because of the p-type 'well' diffusion, and this may account for the underestimate in the predicted beam power here.

A plot of the calculated laser power requirements for data insertion as a function of $V_{DD} - V_{SS}$ is shown in figure 50(c), where the input voltage is assumed to be either at the V_{DD} or V_{SS} level. It can be seen that for a 10v supply an 8mW beam is needed, but if the output transistors in the bistable circuits or the single-gate i.c.'s were optically probed, the larger dimensions would boost this minimum level to over 23mW!

The JK- and D-type bistables are constructed out of a series of simple gates (NAND, NOR etc.) which are separated by transfer gates. Under certain conditions it has been possible to change the circuit output in these cases with the laser, even when using the maximum $V_{DD} - V_{SS}$ operating voltage. Such a situation can arise when a coupling transfer gate is in its high impedance mode, so the following gate is easily 'switched' by the discharge of a parasitic capacitance at the input. The variation in the necessary laser power to input a '1' or '0' as the clock level changes is most marked: using near-minimum supply voltages for the CD4013, 107μW (38μA) is needed to override the data flow through one transfer gate when it is in the ON state, but only 0.083μW (30nA) will produce the same effect when the

clock changes state. Using the values of capacitance/unit area quoted by Athanas[80], a discharge current of 19nA is calculated for this case, showing reasonable agreement with the 30nA equivalent which was measured in practice.

Even though the bistables are comprised of a cascade of geometrically identical gates (except for the output inverters), some gradation in the minimum laser powers for data insertion has been noted when different parts of the circuit were probed. A typical set of results obtained when near-minimum voltage levels was used shows that 4μW was enough to 'switch' the input gate, about 30μW was needed in the intermediate stage and more than 300μW had to be supplied at the gate before the buffer inverter (which was not effected with a 1mW beam power). This increase is because the input to each successive stage after the first one is internally generated so the input voltages will move towards the V_{DD} and V_{SS} levels, whereas the primary input is adjusted to be close to the threshold. The steep increase in the laser power requirements resulting when the transistor gate voltage and supply rails are raised (as in figure 50(c)) is well illustrated by these measurements.

Assuming that the C.M.O.S. circuits will be tested with supply voltages in a 10v-15v range and operating up to about 5MHz[79,81], then minimum laser probe powers of 1mW for gates following OFF transfer gates, 6-20mW for internal logic independent of the clock level and 15-60mW for output transistors are expected to be necessary. Low voltage operation with an associated reduction in laser power will probably be essential for practical laser testing (see sections 5.4.7.4. and 6.2.2.) but this should still be useful for some dc and diagnostic testing.

5.4.7 Laser testing of other i.c.'s

I.C.'s of many varieties are being developed and produced at the present time, and some of the more common types are shown in figure 51; however there are often many subdivisions within each class and novel circuits seem to be appearing monthly. An estimate of the laser powers needed to input information into typical members of

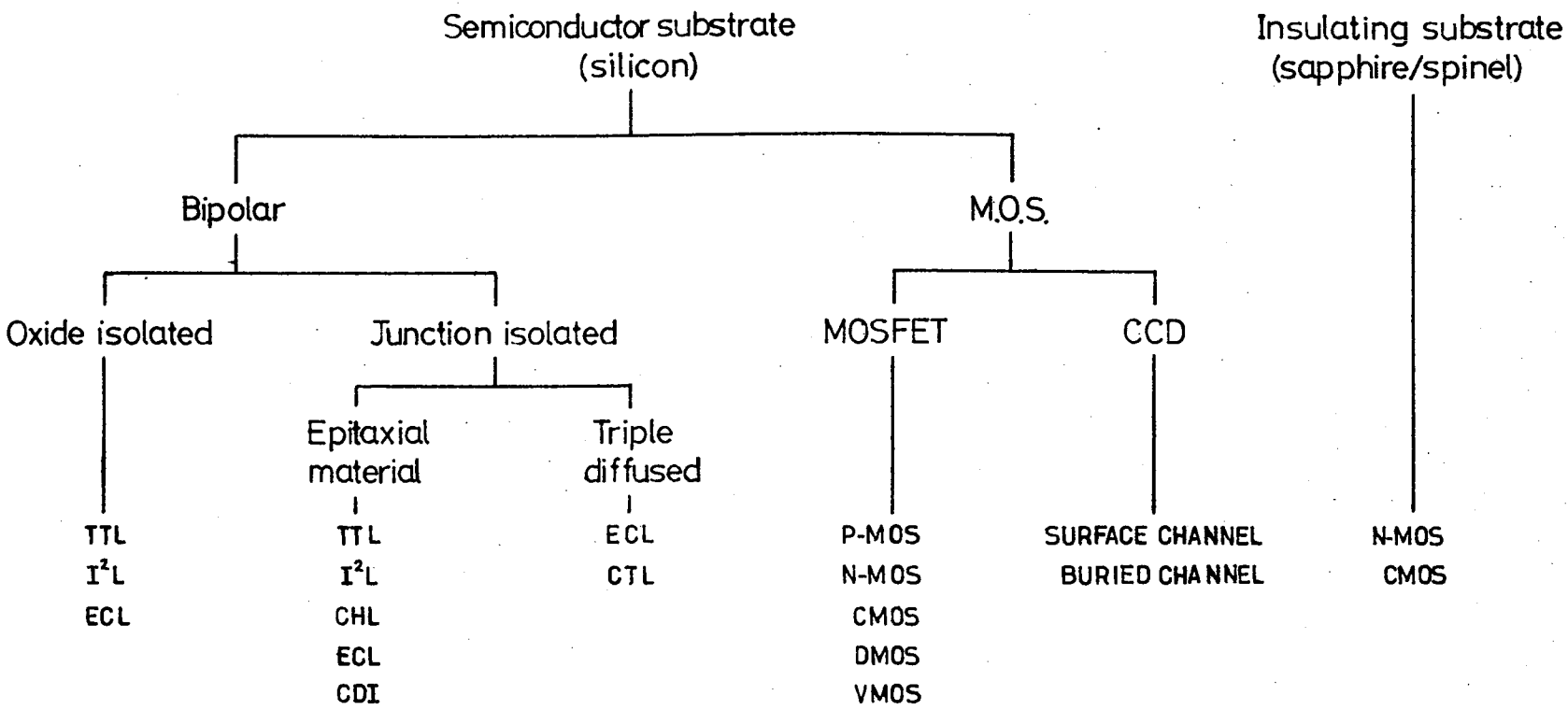


Figure 51: Common integrated circuit technologies

most of these device categories is presented in this section, but the power limits have been found from calculation alone and have not been confirmed by experiment. In every case, a quantum efficiency of 70percent is assumed.

5.4.7.1 M.O.S. circuits and insulating substrate devices

(a) n-Channel polysilicon-gate M.O.S.

The present trend in M.O.S. technology is towards the development of n-channel Si-gate i.c.'s which can reach higher speeds than their p-channel antecedents and also be operated from T.T.L.-compatible voltage supplies. The self-aligned silicon gate process allows very small interelement distances to be used and also reduces parasitic capacitance, and multi-level metallization is often utilized to increase the packing density still further[82]. If the operating voltages and capacitance were exactly the same as in an equivalent p-channel M.O.S. circuit, then the laser power would have to be increased by 2-3 times in order to produce the identical effect in the n-channel version (because of the electron-hole mobility ratio). However, the power dissipation per bit is steadily dropping in modern n-M.O.S. i.c.'s due to refinements in the circuit design and layout[73], so it is expected that rather less laser beam power will in fact be needed to optically input data, but it should still be of the order 1-100μW for static logic and 0.01-100μW for dynamic logic. The effect of the smaller circuit dimensions and increased possibility of a metal layer obscuring an important photodiode on the laser testing method will be considered in section 6.3.

(b) Depletion-load M.O.S. (D.M.O.S.)

In D.M.O.S. circuitry, a p-type diffusion is used to reduce the channel length to about 1μm so the aspect ratio will be significantly decreased, and also the basic inverter is formed with a higher conductance depletion-mode load[83]. More photocurrent will therefore have to be supplied in order to force the output potential to the substrate level so the laser power requirements will increase proportiona-lly: for example about 15mW would be needed for the device parameters quoted in reference 83.

(c) Vertical-channel M.O.S. (V.M.O.S.)

V.M.O.S. is another short channel version of M.O.S. which is characterized by a large current-carrying capacity[84]. Since however the M.O.S. transistor is in the vertical plane with the n^+ substrate typically 3μm below the surface and the etched V-groove is entirely covered by metal, there is little possibility of the laser having any effect upon the circuit operation.

(d) Silicon-on-sapphire(S.O.S., E.S.F.I., S.I.S. and S.O.S.L.)

The parasitic capacitance can be reduced and the operating speed increased if an insulating substrate, such as sapphire or spinel, is used for an i.c.[85]; C.M.O.S. - S.O.S. has been most widely used to date[78] but other forms of M.O.S. - S.O.S. have been produced. Thin layers of p- and n-type silicon, approximately 0.5-2μm in depth, are deposited on the insulator surface so there is no requirement for large isolation regions. The laser cannot produce a significant number of free carriers in the substrate material and the thin pn-junctions are all completely metal-covered, so unless the light is directed through the insulator from the back, this type of device cannot be optically probed.

5.4.7.2. Bipolar i.c.'s

Many different types of bipolar i.c.'s have been introduced in the past few years so in most of the following cases, only the meaning of the acronym, an estimate of the laser power for data insertion and a reference shall be given.

(a) T.T.L. derivatives

About eight varieties of transistor-transistor logic are presently in production: standard T.T.L.[76], low power (L.T.T.L.)[76], low power schottky (L.S.T.T.L.)[77], schottky (S.T.T.L.)[77], high power (H.T.T.L.)[76], complementary (C.T.T.L.)[86], direct coupled (D.C.T.T.L.)[87] and emitter function logic (E.F.L.)[88]. The predecessors of T.T.L.,

resistor or direct coupled transistor (R.T.L. or D.C.T.L.)[89], diode transistor (D.T.L.)[89] and complementary transistor logic (C.T.L.)[90], can also be included under this heading.

Most of the circuit details quoted in the literature are for i.c.'s of s.s.i. or m.s.i. complexity, so it is probable that the calculated minimum laser powers will be rather higher than those which will be necessary for testing l.s.i. devices. Improvements in circuit design may also result in a reduction of the beam power requirements, as is the case for the T.T.L. random access memory for example, where the power dissipation per bit has recently dropped from 5.8mW to 0.42mW[73] (which can be compared with 10mW for a typical s.s.i. gate).

The predictions for the laser beam power are summarised in table 8(a); the values have been normalised with respect to the results for standard T.T.L., where the minimum power range has previously been found to be 3-6mW for internal circuitry and 8-10mW for the output stages (see section 5.4.5). As shown in the table, most of the estimates have been made for an optical input site within an internal gate and these values have been determined from a study of a selection of m.s.i. circuits. The low power-consumption logic families need least laser power as expected, but C.T.T.L. and C.T.L. have very high requirements for the same reason as C.M.O.S., where one transistor is always ON and capable of sinking a large current.

(b) I^2L derivates and C.H.L.

The standard integrated injection or merged transistor logic implementation has given rise to a large number of circuit mutations which include schottky diodes for input and/or output isolation and schottky clamps on the driver transistor[72]. The most common of these are schottky I^2L[91], substrate fed logic (S.F.L.)[92], schottky transistor (S.T.L.)[93], complementary constant current (C^3L)[94] and isoplanar I^2L (I^3L)[95]. Current hogging injection logic (C.H.I.L.)[96] could also be considered to be a member of this class, but it is really a cross between I^2L and C.H.L. (current hogging logic). Most of these variations on the I^2L basic theme are used to improve the operating speed of the circuit and are not accompanied by a reduction in power dissipation.

Logic family	Laser power requirement (normalised to T.T.L.)	
	I	0
T.T.L.	100%	200%
L.T.T.L.	10%	-
L.S.T.T.L.	20%	-
S.T.T.L.	190%	-
H.T.T.L.	220%	-
C.T.T.L.	-	2000%
D.C.T.T.L.	95%	-
E.F.L.	20%	-
R.T.L.	-	500%
D.T.L.	270%	400%
C.T.L.	-	2000%

T.T.L.: 3 - 6mW

I=Internal gate (msi)

O=Output gate (ssi)

(a) T.T.L. derivatives

Logic family	Laser power requirement (normalised to I^2L)
I^2L	100%
Schottky I^2L	50%
S.F.L.	30%
S.T.L.	50%
C^3L	40%
I^3L	100%
C.H.I.L.	100%
C.H.L.	200%

I^2L: 5µW - 1mW

(f: 1kHz-100Mhz)

(I_{inj}: 1-100mA)

(b) I^2L derivatives

Table 8: Laser probing of T.T.L. and I^2L circuits

There is a slight difference in the laser power levels needed for data injection though, and these are shown in table 8(b). Again the power estimates are presented in a normalised form, this time with respect to the 5μW-1mW previously determined for I^2L operating in the 1kHz-10MHz frequency range (see section 5.4.3).

A current is used as the logic variable in C.H.L. circuits, where a control collector in a lateral pnp transistor is used to regulate the reinjection of carriers to a second collector[97]. The laser-generated photocurrent would emulate this reinjected current when the control collector is reverse-biassed with respect to the base, so a light probe power of 10μW - 3mW is calculated for an operating frequency between 1kHz and 1MHz.

(c) Emitter coupled logic (E.C.L.)

E.C.L.[98], in common with the related versions of base coupled (B.C.L.)[90] and current mode logic (C.M.L.)[99], is a high-speed/high-current circuit which will need a large photocurrent to influence its logical behaviour: typically 6mA flows in the output buffers[89] and 1-2mA in internal gates (where the voltage supply is also less)[100], so an overall laser power of 7-40mW at the i.c. surface will be needed.

(d) Collector diffusion isolation (C.D.I.)

The isolation region is used as the collector in C.D.I. integrated circuits[101]: this results in a smaller gate size than the conventional T.T.L. layout and also a high transistor inverse current gain. The C.D.I. equivalent to the 7400 (for which the laser power requirement was 7.9mW) would need about 6.5mW, but only about a tenth of this value should be adequate for the laser testing of internal gates.

(e) Triple-diffused, ion implantation and isoplanar technologies

Triple diffusion is used, particularly in association with E.C.L., to improve the current-carrying capacity of an i.c. but this

will not affect the laser power calculations unless the circuit itself was changed. Ion implantation techniques can give more control and flexibility in the fabrication process[102], and for example, it is possible to create depletion-mode M.O.S. loads which would result in a higher photocurrent requirement, but no general conclusions can be made about the effect of implantation upon laser testing of bipolar i.c.'s. Isoplanar devices[103] may prove difficult to probe optically because of the increased packing density arising from the use of oxide isolation, but the laser power should not be affected.

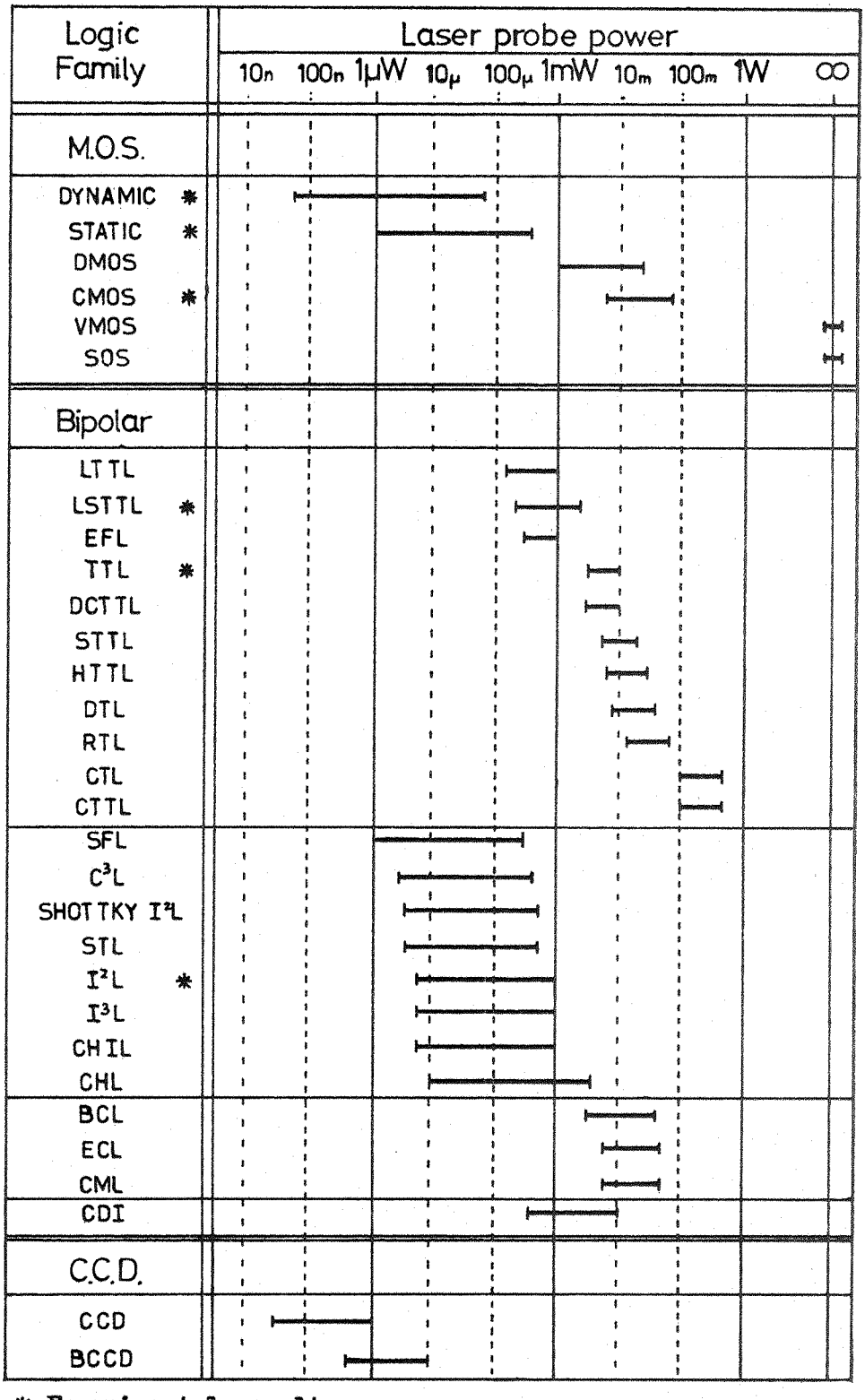
5.4.7.3. Charge coupled devices (C.C.D.)

The maximum number of charge carriers held under each electrode in a CCD is quite small, typically 3×10^6 electrons below a 10 x 10μm gate (1.4×10^{12} cm^{-3})[104], and a laser power of under 1μW should be able to create such a charge packet. For a buried channel device, approximately a six-fold power increase would be needed to fill the charge 'well' for a 4μm channel depth.

5.4.7.4. Summary

All the estimates of the laser probe power needed for data insertion into each of the logic families which have been studied are shown in figure 52; the feasibility of integrated circuit testing in these cases can therefore be determined, although it must be emphasised that only the results marked by an asterisk have been supported by experiments.

The maximum beam power at the surface of a circuit will only be about 20mW, even if the most powerful c.w. helium-neon laser available is used as the source, so in their present form, none of the C.M.O.S., V.M.O.S., S.O.S., C.T.L., C.T.T.L., D.T.L. and R.T.L. devices will be suitable for optical testing. It is also probable that a multiple-beam arrangement will have to be used for an economically-viable high-speed production (go/no-go) test system, therefore unless individual high-powered (very expensive) lasers are used, the E.C.L., B.C.L., S.T.T.L., and H.T.T.L. i.c.'s may also fall into the 'untestable by laser'



* Experimental results

Figure 52: Laser power requirements for i.c. testing

category. However, only a medium power laser beam is needed for standard T.T.L. and C.D.I., and a power of less than 2mW should be satisfactory for M.O.S. and I^2L circuits; together, these logic families form by far the greatest part of the total i.c. production at the present time, so the laser method of integrated circuit testing has a very promising future.

5.5 Measurement of the Internal Circuit Operation

5.5.1 Parametric testing with the laser probe

Functional and simple diagnostic testing can be performed satisfactorily by using the laser probe to insert '1''s or '0''s at various points within a circuit, but it is also possible to detect and isolate parametric-type faults and failure mechanisms. It is extremely difficult to monitor the behaviour of the internal circuitry under working conditions in an i.c. by using conventional methods, so an important application of the laser in the fields of circuit character--ization, full diagnostic and even ac testing is envisaged.

The effect of the laser input has been found to alter when the beam power was changed in some cases (see section 5.4.4.); this power--dependence arose because the laser-generated change of state in one part of a circuit could propagate along a number of paths, each of which had different current-sinking characteristics. A response of this type could be precomputed from an analysis of the circuit or determined experimentally by using one known fault-free device, so that by a comparison between the expected result and measurements performed on other devices, an indication of both the presence and cause of a fault can be obtained.

In a similar way, the laser power needed to produce a given change in output is often dependent upon the state of other circuitry, such as the impedance of a transfer gate: in many cases, the minimum laser power level can be measured as a function of clock voltage and the result may be used to determine both the transient behaviour of the

clock and transfer gate; two detailed examples of this procedure will be given in the following sections.

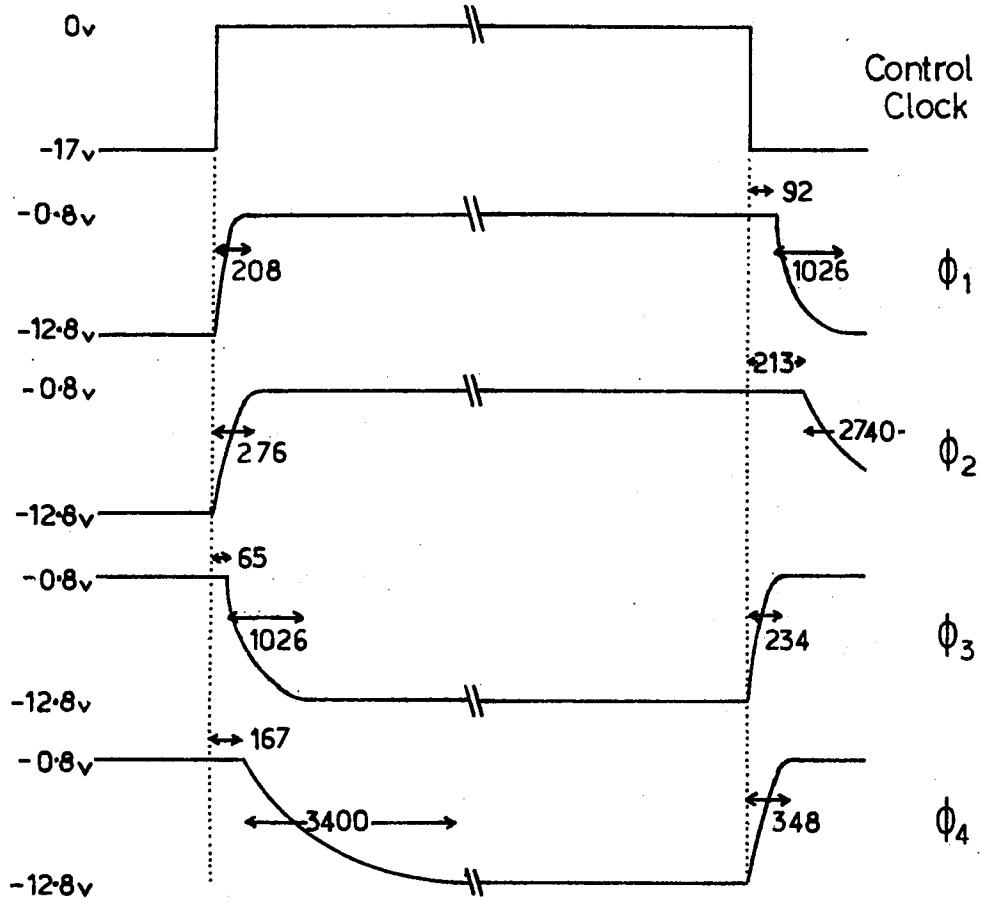
The optical input can be controlled in time and position, thus propagation delays from different parts of a circuit to the output can be easily measured. This ability will be particularly useful for asynchronous-circuit testing but should also find an application with some clocked devices, especially when operating frequencies close to the maximum are used.

In each of these cases, a detailed observation of the interaction between the circuit under test and the laser input can give information about the operation of the circuit which often cannot be obtained in any other way; microprobes for example tend to load internal circuitry and alter the parameters which are being measured. Thus the laser probe can be used to identify parametric faults, check circuit calculations or simply to improve fault resolution. An example of this technique is given in the following two sections, when the transient response of a transfer gate in both a static and dynamic shift register circuit is determined.

5.5.2 M.O.S. static shift register transfer gate response

The circuit diagram of the basic cell in a SS-6-1032 M.O.S. shift register is shown in figure 38. The four clocks ϕ_1 - ϕ_4 are generated from a single external clock control, and if this is assumed to be a step-input pulse, the method of transient analysis outlined in Appendix 6(b) can be used to calculate each internal clock waveform. These are shown in figure 53, where the 10-90percent rise and fall times are indicated in nsec and the equivalent exponential time constants are tabulated underneath.

The transfer gate response is almost entirely dependent upon the clock voltage because the parasitic capacitance of the following stage is only 0.1pF, so the time variation of the transfer gate impedance can be found directly from these waveforms (see Appendix 6(c)). The laser power necessary to insert data at nodes X and Y is dependent upon the



10-90% rise and fall times in nsec. (not to scale)

Exponential time constants (nsec):-

Internal clock	Rise time ('0'→'1')	Fall time ('1'→'0')
∅1	94	460
∅2	126	1246
∅3	106	460
∅4	158	1550

Figure 53: Calculated clock waveforms for the SS-6-1032

gate impedance, so this will also be a function of the clock potential. A series of measure--ments have been made to experimentally determine this relationship by using the method shown schematically in figure 54. A narrow light pulse (typically 500nsec in duration) was directed at node X during different phases of the external clock signal, and the power needed to force the cell output to '1' was measured as a function of the clock edge -light pulse delay, δt. A correction is made to allow for the 150nsec response time of the modulator (section 4.4.2) because it is the rising and falling edges of the light input which determine the laser power level; the pulse width itself is not important.

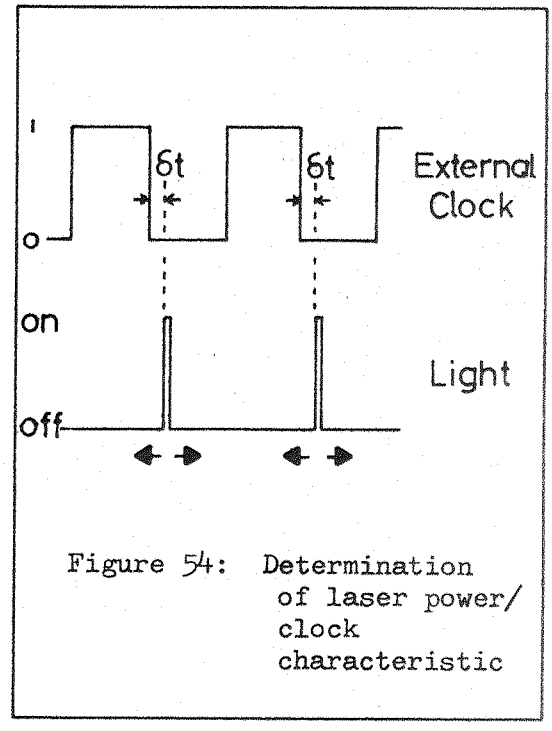


Figure 54: Determination of laser power/ clock characteristic

A typical set of results is shown in figure 55, where the laser power/clock phase characteristic has been measured with three positions of the laser beam relative to the sensitive node X . If carrier lifetime effects were significant, the exponential decay times would have changed as the light spot was moved away from the junction; in this case there is clearly very little alteration in the shape of the curves, indicating that the injected carrier lifetime (260nsec) is much less than the time constants being measured.

The multi-slope characteristic is produced because both Transfer Gates A and B (figure 38) have an effect upon the photocurrent needed to raise the potential of node X to a logical '1' value. At the time origin $\delta t = 0$ (when the external clock control drops to the '0' level), both Gates C and D in the cell before the one in which node X is illuminated are ON, or in the low-impedance condition, so a high laser power is needed to change the state because of the completed feedback loop. These two transfer gates quickly turn OFF after the clock transition (figure 53), and after a short time this is followed by the

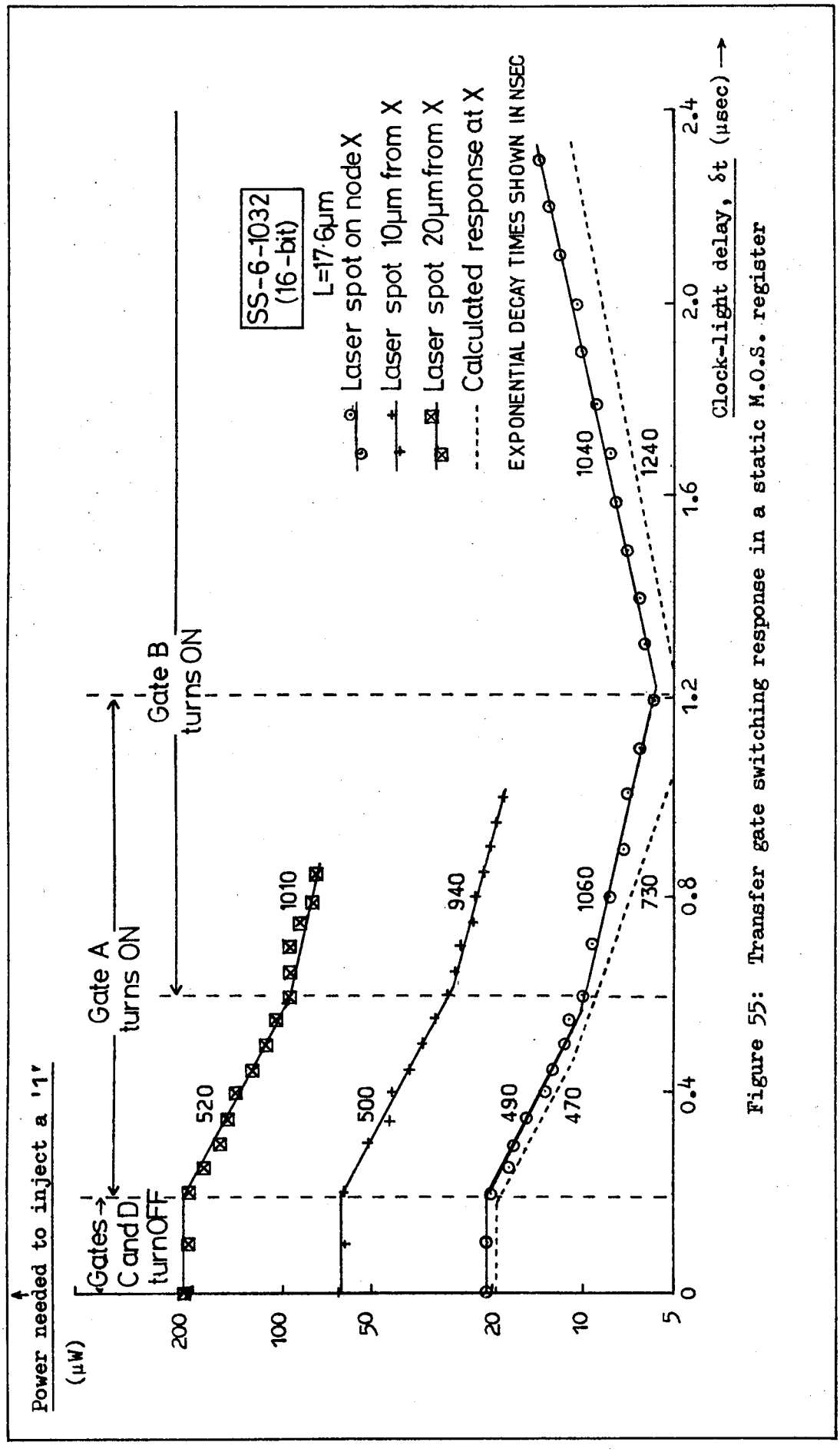


Figure 55: Transfer gate switching response in a static M.O.S. register

faster Gate (A) starting to turn ON. The rise in potential at node X due to the laser action in discharging the parasitic capacitance can then begin to reach Driver B because of the falling impedance of this transfer gate, and correspondingly less power is needed to force the cell output to '1'. At approximately δt = 0.6μsec, the ϕ_2 clock potential crosses the threshold and Gate B also begins to turn ON; the feedback from Load B to node X will produce an increase in the photo--current requirement again, but because the impedance of Gate A is dropping at a faster rate than that of the slower Gate B, the net effect is still a fall in the laser power, but at a reduced rate. Eventually ϕ_1 and Gate A reach their steady-state limits and at this point, δt = 1.2μsec, a minimum laser power is reached. When δt is further increased, Gate B is allowed to turn ON more and the power level rises again till the transfer gate is fully ON.

The exponential decay times of the measured response will there--fore be determined by the turning-ON characteristics of Gates A and B (or the fall times of ϕ_1 and ϕ_2). The 'expected' result obtained from the clock waveform calculations for the case of the beam positioned above node X and a quantum efficiency of 71percent is also shown in figure 55 (dashed line), and this agrees well with the readings. Hence it can be concluded that the Transfer Gates A and B and the ϕ_1 and ϕ_2 generation circuit are operating correctly.

If the external clock changed state at less than 0.6μsec intervals, the slow Transfer Gates B and D would not begin to turn ON and the feedback loops could never be completed. Providing that the inverter gain was large enough to overcome the higher impedance encountered because the faster gates would not be fully ON either, the shift register should then behave in the dynamic mode: this has in fact been noted for an external clock frequency in the 1 - 1.2MHz range (see section 5.4.1.1). An attempt to discover the reason for the upper frequency limit has been made by using the laser to inject a '1' or '0' into each cell when the clock frequency is just above the maximum; it has been found though that the cut-off is not caused by a malfunction of one

particular cell but rather data are not transferred to the next cells in sequence: the frequency limit therefore probably arises because of a failure of the clock lines or transfer gate impedance effects (the maximum operating frequency quoted for the SS-6-1032 is 1MHz). In a faulty circuit however, an investigation of this kind followed by a detailed measurement of transfer gate response times in any suspect cell should quickly lead to a precise determination of the cause of the fault.

5.5.3 M.O.S. dynamic shift register transfer gate response

The two clocks in the DL-6-2128 dynamic shift register (figure 40) are generated externally, so the transient analysis of the transfer gate response is much simpler. There is only one gate in each half bit (equivalent to the faster gate in the static register) and therefore a single decay slope is found when an experiment similar to that described in the previous section is performed. This is shown in figure 56, where the calculated response of the transfer gate impedance as a function of time is the dotted line; the similarity of the results obtained for different laser spot/collecting junction separations again indicates that the minority carrier lifetime (120nsec) can be ignored. The maximum frequency in this case is 2.2MHz, but as previously, the upper limit does not arise as a result of a failure of one particular cell.

5.6 Laser Testing of the SN54LS191

This low power schottky T.T.L. counter has been mentioned in section 5.4.4, in which detailed results obtained from the laser probing of an OR-gate and a JK-bistable were presented, but now the circuit as a whole will be considered and used to demonstrate the benefits which can be gained from use of the laser in an integrated circuit testing context.

A block diagram of the circuit is given in figure 57: the four bit synchronous up/down counter has a down/up mode control and counting can be stopped at any time by raising the potential of the enable input; in the counting mode, the J = K inputs to the bistables are

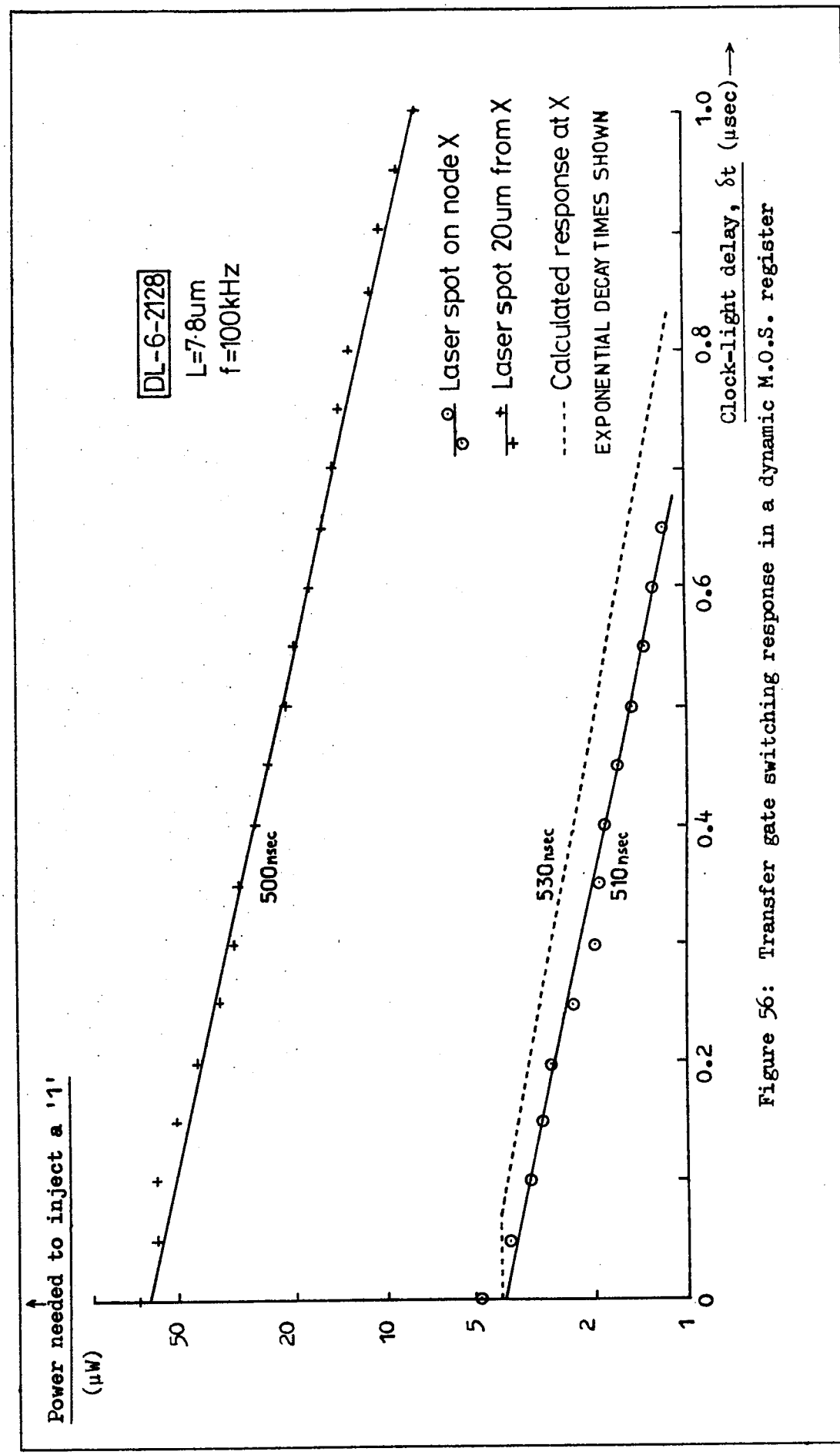


Figure 56: Transfer gate switching response in a dynamic M.O.S. register

determined by the values of the previous state outputs using simple combinational logic. Each bit is also fully programmable and can be set or reset by using the data inputs, independent of the clock level.

The laser can impose a '1' or '0' condition at all the sites indicated in red. A '0' can be inserted at the inverter gates, but if the input is allowed to float or is strapped to the positive rail by a large resistor ($R > 2k\Omega$), a '1' at the gate output can also be pr--oduced by shining the laser on the input diffusion. Both logic levels can be introduced directly in some other parts of the circuit where complementary nodes are available (such as at the OR-gates which are implemented in the form of a NOR-NOT combination), but even at positions where a '0' alone can be injected, illumination of a previous gate can be used to force the desired node to the '1' level. In fact the only gate outputs in the 58-gate device which cannot be altered by the laser are the central AND-gates, and this is because they are wire-AND'ed with no suitable pn-junction to illuminate.

This particular 8-input circuit could obviously be made to function correctly in every detail, even when none of the input pads were bonded up, by directing laser beams upon each of the input gates. In a large l.s.i. network, a counter module like this may form just one minor part of the whole system, and then it is probable that there will be no direct connection to any of the inputs, except the enable; in such a case very long input sequences will be needed to access the module, and so the ability to control the counter circuit with laser beams would be extremely useful. Even in its present m.s.i. form, the laser can be used to reduce the minimum comprehensive test sequence for the counter from 10 to 6 clock periods in length by overriding the J = K input circuitry; if the programmable counter output facility was not provided though, then a full functional test would last for 33 clock periods, whilst the circuit could still be tested in 6 by using the laser method. In a complex l.s.i. system, this 6-clock period test may be comparable with one which is thousands or even millions of times longer.

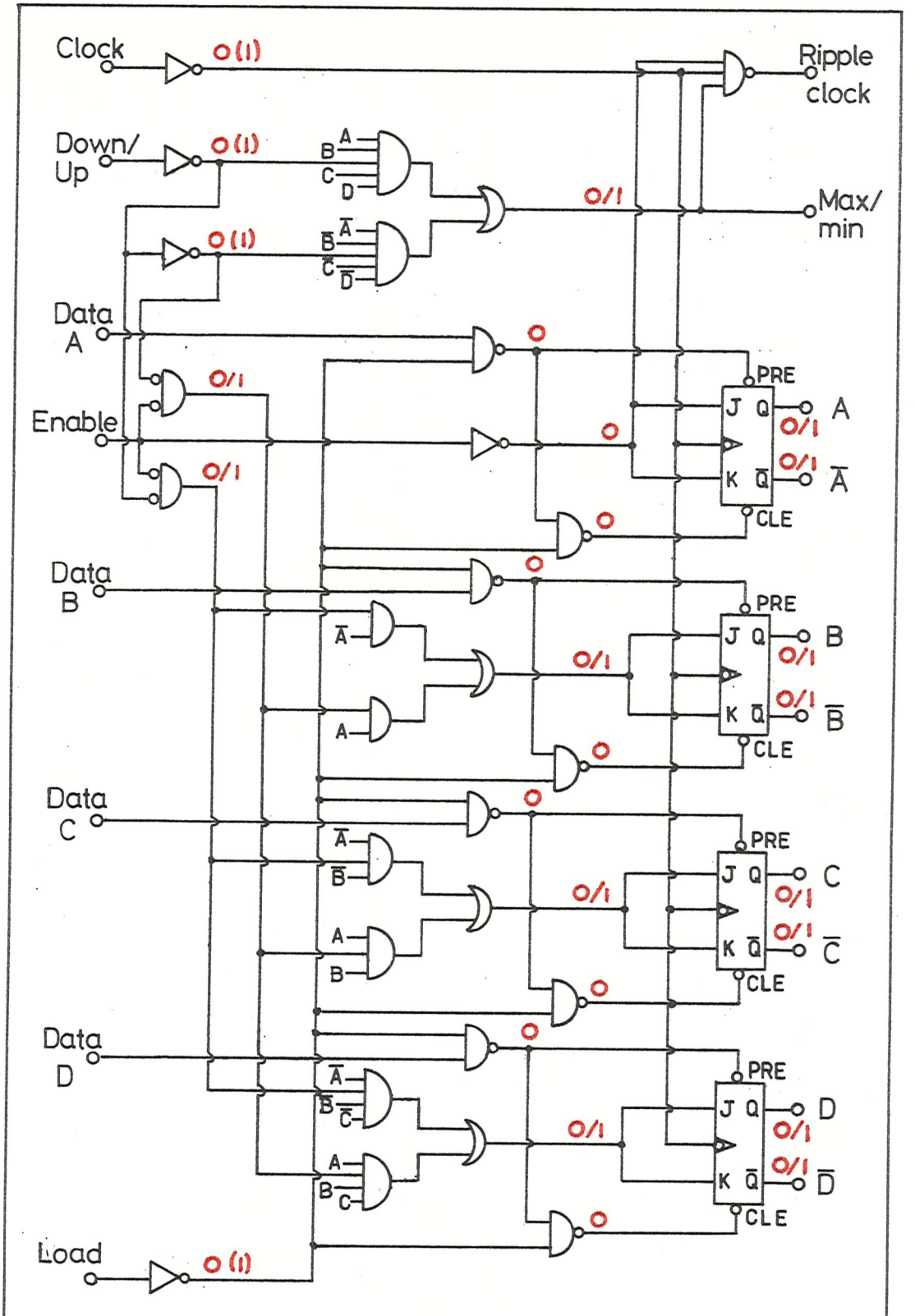
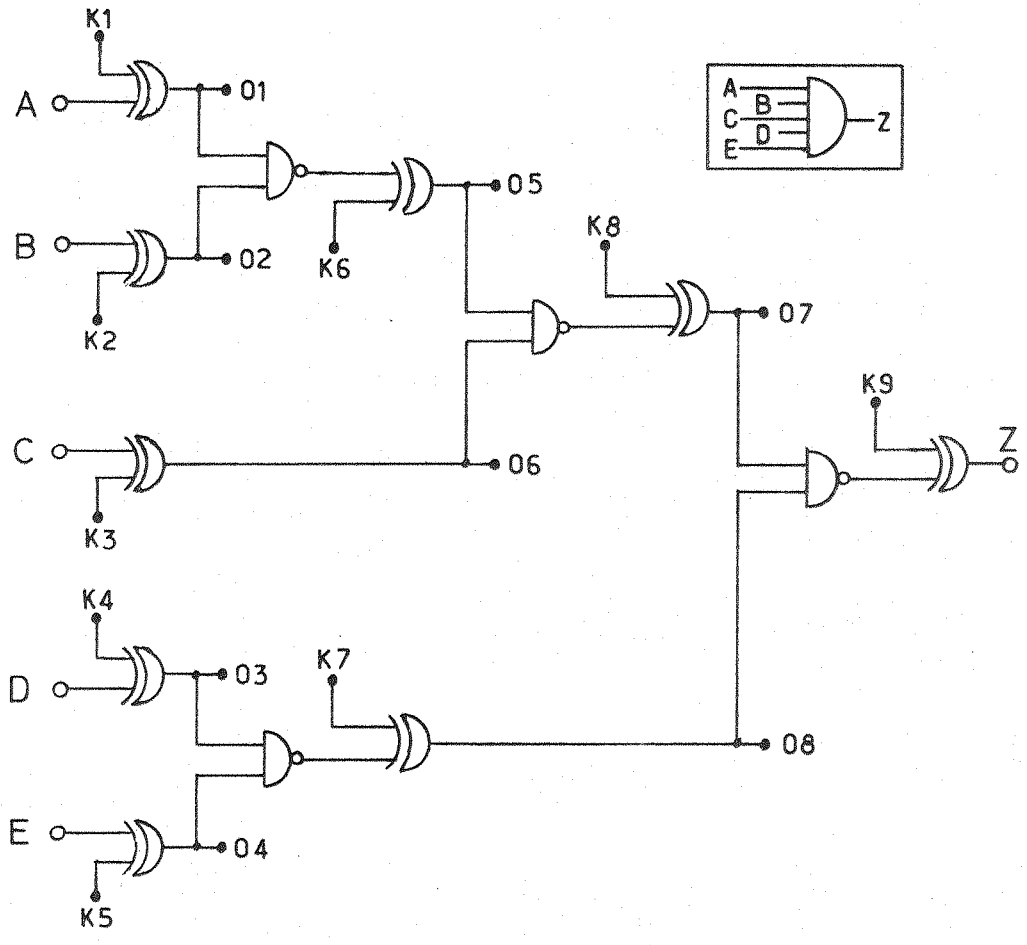


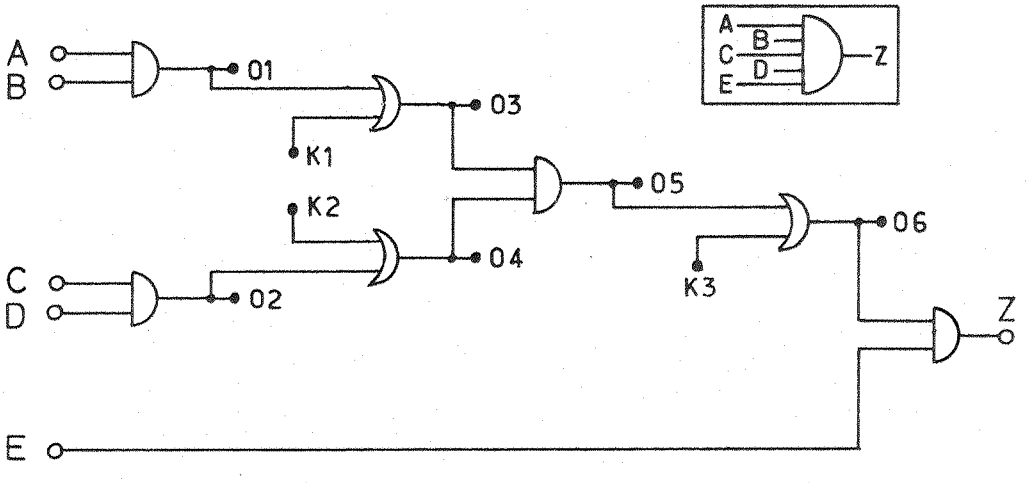
Figure 57: Block diagram of the 54LS191

The advantages that laser testing would bring in terms of a reduction in the comprehensive testing time cannot be demonstrated effectively on a small circuit in isolation, but the benefits from a diagnostic testing point of view can be seen more clearly. Considering only single stuck-at faults (i.e. logical-type) at the gate level for each interconnection, only 52 out of a possible 120 failure modes can be isolated by using tests applied at the normal inputs; however, with the laser probe all except 12 can be found (these are the wired- AND's). When multiple faults are postulated, the improvement in fault location gained by use of the moveable optical input is even larger, since 90percent of all possible failure mechanisms can be uniquely determined compared with 36percent by conventional means. In addition to this, the resolution of the laser fault finding method is much better because the light beam can probe within the gate itself, and some parametric faults can even be detected and diagnosed (see section 5.5.1).

Laser testing also compares favourably with two techniques of circuit design which have been proposed to improve testability. The 54LS191 has been redesigned according to the guidelines given by Hayes[13], where the circuit function is implemented by using only 2-input NAND-and EOR-gates, and by Saluja and Reddy[14], in which 2-input gates are used to allow the whole device to be comprehensively tested with a 3-test sequence. The five-input NAND-gate is shown in its redesigned forms in figure 58: the k inputs are extra controls and a large number of observation points (outputs) are also needed. These additional inputs and outputs have to be routed to contact pads, so the net result is a large increase in the chip and package size, failure rate, propagation delay and overall cost[15]. A summary of these properties for the case of the redesigned 54LS191 is given in table 9, in which they have been compared with the i.c. in its present form; the improvement in the testability which arises from the use of these two theoretical methods can be seen, but they are obviously impracticable. The laser test method can of course be used to reduce the test sequence and improve the 'diagnostibility' of the circuit without any modification. When the laser is used in conjunction with l.s.i. or v.l.s.i. circuits, the savings in test time and benefits which it will bring in diagnostic testing will clearly be highly significant.



(a) Hayes technique[13]



(b) Saluja and Reddy technique[14]

Figure 58: 'Testable' implementations of a 5-input AND-gate

	Conventional circuit	Laser testing	Hayes method[13]	Saluja+Reddy method[14]
Number of pins (increase)	16 (100%)	16 (100%)	125 (680%)	186 (1060%)
Chip size (increase)	$1.9\times2.3mm^2$ (100%)	$1.9\times2.3mm^2$ (100%)	$6.5\times6.5mm^2$ (750%)	$4.8\times4.8mm^2$ (370%)
Propagation delay (increase)	20nsec (100%)	20nsec (100%)	128nsec (540%)	52nsec (160%)
Number of gates (increase)	58 (100%)	58 (100%)	516 (790%)	170 (193%)
Approximate cost (increase)	£3.00 (100%)	£3.00 (100%)	£13.50 (450%)	£14.40 (480%)
Number of tests (decrease)	10 (100%)	6 (60%)	5 (50%)	3 (30%)
Diagnostibility: single/multiple logical faults	43%/ 36%	90%/ 90%	100%/ 100%	100%/ 100%
Fault isolation	Gate level	Transistor level	Gate level	Gate level

Table 9: Testing strategies for the 54LS191

CHAPTER 6

DEVELOPMENT OF A COMMERCIAL LASER I.C. TEST SYSTEM

- Test strategy using the laser probe
- Practical i.c. testing using a laser
- Design of laser-testable circuits
- Future possibilities

6. DEVELOPMENT OF A COMMERCIAL LASER I.C. TEST SYSTEM

In each of the experiments described in sections 4 and 5, only a single laser beam was used to probe the integrated circuits, and its position was manually adjusted. High-speed modulation was achieved by using the electro-optic modulator, but in its present form the system may not be suitable for use as a practical i.c. tester, particularly in the application of production testing. The improvements and modifications which may be necessary in order to use the laser method in a commercial testing environment will be outlined in section 6.2, but initially the manner in which the laser can be used to test a circuit and the limitations of the present system in this context must be investigated.

6.1 Test Strategy using the Laser Probe

6.1.1 Laser probing at the transistor level

Logical faults are usually simulated by using the 'stuck-at' fault model, in which every possible failure mechanism in a network, which could be a simple gate (AND, OR, NAND, NOR, NOT, EOR), bistable (JK, D, RS etc.) or m.s.i. element (shift register, counter, multi-plexer etc.), is assumed to occur in isolation and to result in either the input or output of the network behaving as if it was stuck-at-'1' (s-a-1) or s-a-0. This model evolved from work on p.c.b. testing and was subsequently applied to i.c.'s, even though many fault mechanisms are not covered by the basic stuck-at approximation[1]. Faults occurring in logically redundant branches of a circuit for example often cannot be detected, failures arising from bridging-faults are also not always included in the simulation[105] and even open- and short-circuits in voltage-operated logic families such as C.M.O.S. may not behave as simple logical faults. Multiple and intermittent faults can however be detected by a repeated application of the test sequences based upon the single 'solid' fault approximation[106], and since the simple stuck-at model is found to cover the majority of commonly-occurring faults, it is still frequently used as the basis of the test pattern generation procedure.

Essentially the laser creates a stuck-at condition when it drives the potential of a node towards the substrate level, but unlike the normal case where a gate or bistable is assumed to be the basic circuit unit, the laser probes the component parts of the gate; the validity of the conventional gate-level model must therefore be investigated under these conditions to determine whether standard testing routines can still be used (treating the laser input as just another test point) or if completely new test pattern generation procedures will have to be employed. For example, a 2-input NAND-gate is fully tested in three tests with input sequences of (01, 10, 11) according to the stuck-at fault model, because the fourth input comb--ination of (00) could not indicate any of the six possible failure modes that had not previously been identified by the other tests; if the laser, by probing within the gate, could create a situation where the first three tests gave an error-free output and yet a (00) input still gave a '0' at the output then obviously the test strategy would have to be changed. In a T.T.L. 2-input NAND-gate there are 28 possibilities of single logical faults within the gate, but by analysing the effect of the laser in each case it has been found that the gate--level test sequences still hold. In a similar way, each of the six basic gates implemented using a variety of technologies have been studied with the same result. Therefore at the transistor-level, standard fault-propagation theory will still apply and the laser input position will not be restricted to the gate inputs or outputs, thereby enabling fault isolation within the gate itself to be performed with the laser probe.

6.1.2 Fault diagnosis

Isolation of a fault in a large i.c. is frequently achieved by initially using either sensitive path, boolean difference or simulation methods[107] to locate the faulty area (to the gate or bistable etc.), and then visually inspecting this suspect region in order to determine the exact cause of the failure. This process may

require the use of microprobes and possibly may also involve some metal and semiconductor etching in order to complete the diagnosis.

The more efficient intersecting-path technique illustrated in figure 59 could be used to isolate a fault if the extra input provided by the laser beam was used. This method is not generally used at the present time for economic reasons, because the limited access to the circuit makes it difficult to prod--uce the desired sensitive path without being obscured by many others. By using a fault dictionary, the optimum site for the next test input can be found and the laser repositioned accordingly, so that after successive applications of test sequences the position of the fault can be quickly refined.

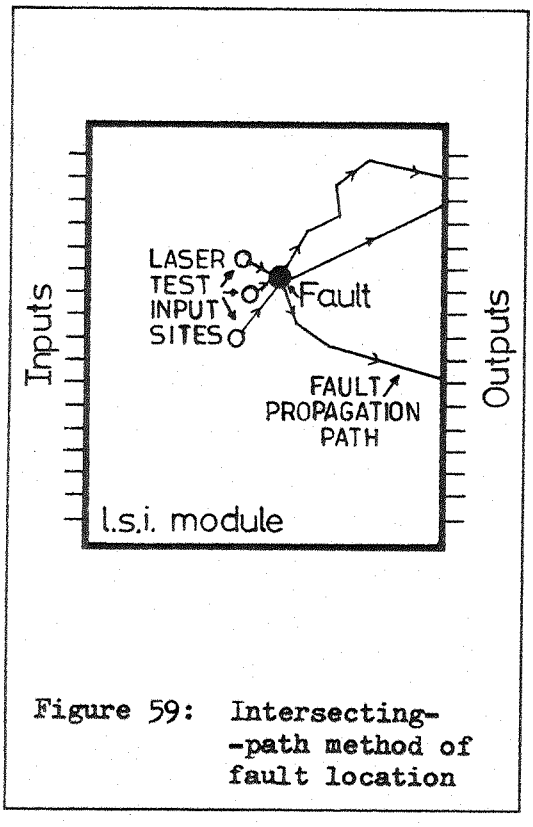


Figure 59: Intersecting--path method of fault location

The laser probe can also be used to break into indistinguishable fault sets and to generate 'can't happen' or 'don't care' situations which are not normally available to the diagnostic tester and can be used to simplify the testing problem. Furthermore, some parametric faults can also be detected and located (see section 5.5) by carefully controlling the laser beam power and studying the interaction between the light input and circuit under test.

6.1.3 High-speed fault detection

Fault detection is achieved in two ways in practice: a functional test can be used, in which the circuit is treated as a 'black box' and long input sequences are applied with the output checked against

the state table or a known good device, or alternatively a knowledge of the circuit structure is used to generate test patterns based upon the effect of a postulated fault upon the circuit operation. Detailed information about the physical layout of the circuit under test will be needed for laser testing purposes in order to locate the optical input sites, so the structural test approach will probably be most suitable for use with the laser.

The position of the additional inputs will be an important factor in determining the reduction of the overall testing time, but this will be highly dependent upon the circuit configuration and difficult to quantify in general terms. Intuitively it would be desirable to have as many inputs (i.e. laser beams) available simultaneously as possible, and to use these to gain access to the connections between different circuit blocks or to break feedback loops or counter chains etc. (see section 2.5), but it is hoped to co-ordinate work with a research group studying the theoretical aspects of digital network testing in order to produce a more satisfactory solution to the test input siting problem.

6.2 Practical I.C. Testing using a Laser

6.2.1 Diagnostic testing

Fault diagnosis is usually performed throughout the initial stages of the production of a new circuit and on a sample of the devices which fail the main go/no-go detection tests, but occasionally customer returns are also inspected for reliability studies. The number of circuits which are given a full diagnostic test is therefore relatively small compared with the total manufactured, so the speed of testing is not as important as is the case for fault detection work where every single device must be checked. From the point of view of laser testing, this implies that a single optical probe will probably be adequate for use in a diagnostic test system; another two or three beams could make the task of fault isolation quicker and easier by enabling some of the alternative paths for data flow to be blocked off for example, but the additional expense involved in their provision would probably outweigh the benefits gained by their use.

The single-wavelength HeNe laser has proved to be very suitable for work with silicon i.c.'s, but the power output should be chosen with respect to the types of circuit which are to be tested because the cost of the laser rises steeply as the power output increases (see Appendix 7). One of the largest available c.w. HeNe lasers produces a beam power of 50mW, so it may be necessary to use pulsed light if larger powers are required (for example with C.M.O.S. integrated circuits).

The penetration depth in the semiconductor would be altered if the wavelength of the incident illumination was changed, and this could be used to obtain information about surface effects or buried inhomogen--eities for example. Two laser systems suitable for this application are detailed in Appendix 7, and these would enable the use of a number of wavelengths in the range 4600-11000Å, but apart from very specialised work it is unlikely that such a versatile light source will be required for diagnostic testing.

A good quality pockel cell is essential for accurate measurements of carrier lifetime and for the determination of parametric faults, especially in circuits with a high operating frequency and small propagation delays, and if necessary the 150nsec 10-90 percent response time obtained with the present modulator could be improved to less than 1nsec by the use of a better cell [108].

A large working-distance focussing lens will be needed if the tests are to be performed at the wafer stage of the device fabrication, and a clearance of at least 15mm will have to be maintained between the circuit surface and lens if conventional probing systems are used. This lens should also be of a good quality and have a large numerical aperture in order to produce a small undistorted spot. The step-and-repeat camera lens described in section 3 should be satisfactory, but larger lenses can be obtained, although usually with a sacrifice of quality: an example of a lens with working distance of 289mm is given in Appendix 7 - the spot size would then be about 5-10μm but this should be adequate for optical probing the present generation of i.c.'s. Laser testing of

decapped packaged devices should not pose a problem since the chip is unlikely to be recessed by more than 5mm below the upper surface. The position of the beam on the circuit can be altered manually (as at present) or automatically by beam deflection or movement of the wafer prober: speed is not important, so a cheap mirror deflection arrangement will probably be the most suitable system (also see section 6.2.2.2).

A full diagnostic test system capable of performing logical and parametric fault analysis on i.c.'s ranging from M.O.S. through I^2L and T.T.L. to E.C.L. could therefore consist of a single 50mW HeNe laser, electro-optic modulator, focussing optics and wafer prober; the total cost would be approximately £7,000 excluding normal drivers and power supplies etc. (a detailed breakdown of the cost is given in Appendix 7). This system would enable the tester to access nearly all parts of the circuit under test by using a small easily-moveable probe which does not load down the internal circuitry and cannot damage the surface. Fault isolation can be carried out to the transistor level and in addition, the transient as well as steady-state operation of the circuit can be checked.

6.2.2 Production (go/no-go) testing

The laser probe can be used to provide greater access to a circuit through the ability to insert data at various input sites. The laser test system will therefore not be used to replace conventional automatic test equipment (ATE) but rather to complement it; consequently the laser, focussing optics and control electronics should be designed so that they are compatible with existing i.c. testers, both physically and in terms of speed and synchronization. Only the large computer-controlled general purpose ATE (of the type described in section 2.3) will be considered in this respect, and it shall also be assumed that the hardware and software used by the conventional tester can handle the additional demands of the laser system.

Testing must be performed as fast as possible, so automatic handling and beam alignment, and possibly multiplexing of facilities, will be essential. The saving in test time resulting from the use of the extra inputs will be greatest if a large number can be accessed simultaneously since in complex circuits there may be many feedback loops and multiple branches, all of which contribute to the test sequence length. A multi-laser beam system in which each focussed beam is controllable in position and intensity is difficult and expensive to build though, so a compromise will have to be reached in order to derive the maximum benefit from the laser test method.

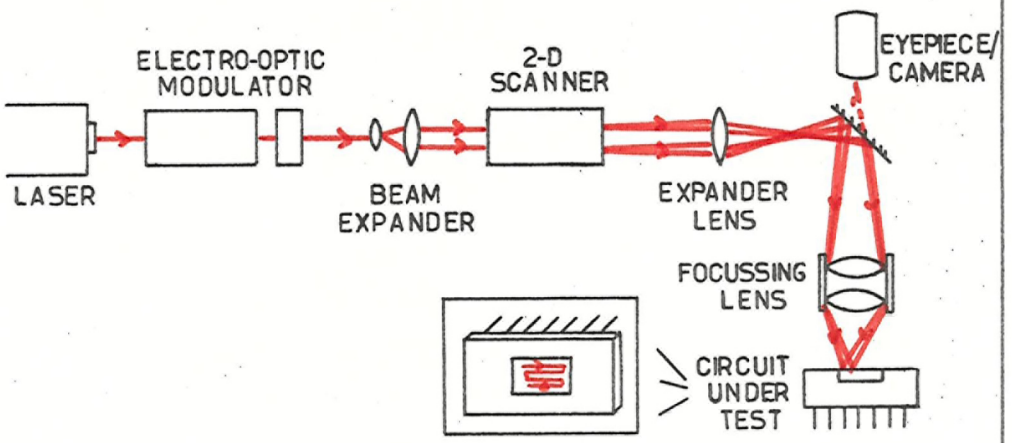
6.2.2.1 Provision of multiple inputs

Two solutions to the practical problem of providing a multiple laser beam facility have been proposed: a single beam could be moved rapidly over the i.c. surface to cover all input sites sequentially or a group of individual beams could be used, each of which was independ--ently positioned and modulated.

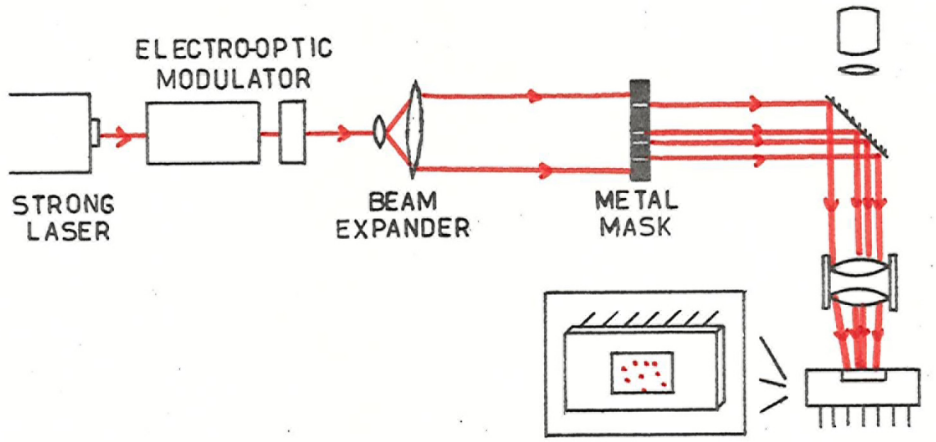
(a) Single beam systems

If a single laser spot was scanned in raster fashion or in discrete steps over the surface of an i.c., access to any particular input site could be gained by synchronizing the modulator with the beam movement to provide a burst of light when the probe passed over the target (see figure 60(a)). Obviously the input will only be available for a small period of time during each scan, so a continual data stream could not be injected at one point unless the beam movement was halted; neither can the light be used to disable feedback loops or partition the circuit and test other parts of the device at the same time.

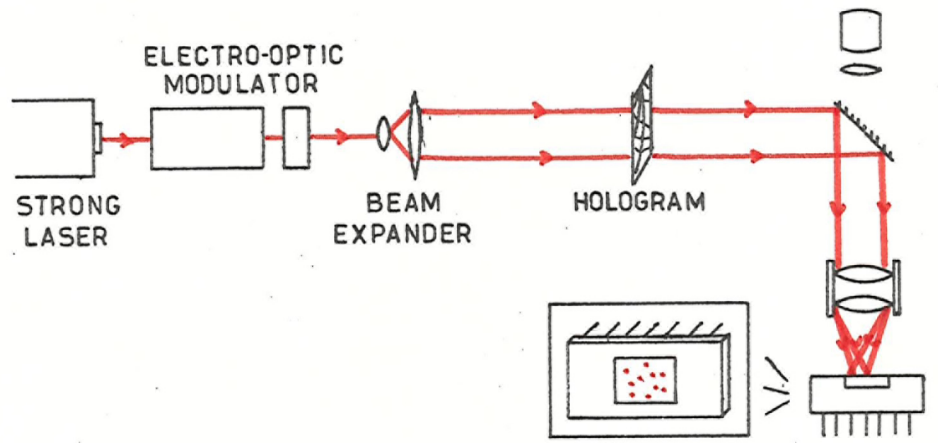
Depending upon the area of the chip, the total time taken to complete one sweep of the surface with the laser spot will be large, even if high-speed deflection systems are used: for example, the deflector described in the next section would take approximately 4msec to cover a 4mm x 4mm area, and mechanical methods using torsion bars or mirror



(a) Beam scanning



(b) Flood beam with mask



(c) Multiple-beam production from a hologram

Figure 60: Multiple-input provision from a single beam

systems would be orders of magnitude slower. Thus it will only be possible to set or reset certain key nodes and maintain these states till the next beam scan if photosensitive bistables are incorporated into the circuit design (this aspect will be considered further in section 6.3).

Variations of the single-beam method include the possibility of using a powerful 'flood' beam with an appropriate metal mask held over the circuit under test to direct the laser probes to the correct input sites (figure 60(b)), where the mask would either have to be of the same size as the chip and positioned over the surface or be larger and placed in a near-parallel expanded beam in order to prevent the focussed spot size from becoming too large; also a novel technique of using a hologram to produce the desired pattern of light spots has been proposed by Bryngdahl and Lee[109] (figure 60(c)). In each case though, the individual inputs cannot be separately modulated so these methods would only be suitable for illuminating the test nodes in a pseudo--static fashion or for providing a general reset.

(b) Multiple beam systems

Either a cluster of lasers or a single high-powered model with beam splitting system can be used to produce a group of optical probes which are capable of being individually controlled. The physical size of such an arrangement will probably limit the maximum number of laser inputs to 9 or 16, and each would need its own modulator, deflector and control electronics. Small semiconductor lasers[110] would be more appropriate for this purpose, but at present the only types available which operate in the c.w. mode with relatively moderate threshold currents (typically amps) give an output wavelength of 0.85μm or greater. A 20mW output power from these double heterostructure devices has been obtained (see Appendix 7) but at this wavelength the penetration depth is ~ 13μm in silicon (figure 4(b)), so only 20 percent of the incident light is absorbed in the top 3μm of the i.c. The focussed spot would also be slightly bigger and invisible to the eye, but image intensifiers could be used to determine its position. The focussed light collected

from modern high-radiance LED's of a suitable wavelength is at most $100mW/cm^2$ [111], which is still about a hundred times too low for testing of M.O.S. circuitry. However future improvements in the power output may result in these smaller and cheaper solid-state light sources becoming suitable for laser testing (see also section 6.4).

6.2.2.2 Automatic beam deflection

Automatic beam positioning will be necessary if the laser method is to be used in conjunction with high-speed production testing of integrated circuits. The focussed spot size will be about 1-5μm, and it should lie not more than 5-10μm away from the pn-junction which forms the input site so that other junctions will not also be accessed at the same time. The active chip area may be 6mm x 6mm or more, so the deflection system must have a positional accuracy of at least 0.15percent if a single beam is used.

(a) Acousto-optic deflection

High-speed deflection is possible by using acousto-optic or electro-optic deflectors, when on average the beam can be repositioned to any point within the range of movement in about 1-10μsec. The total number of resolvable spots, N, is a limiting factor and its value can be calculated from the formula

$$N \simeq \frac{\delta\theta}{2\phi} \qquad \ldots (6.1)$$

where $\delta\theta$ is the deflection angle and ϕ is the laser beam divergence. The minimum value of ϕ is determined by the dimensions of the active crystal in the deflector (see Appendix 1), so the number of resolvable spots is theoretically dependent upon the choice of deflector and laser.

For an acousto-optic deflector[40] (which in general has a larger deflection angle than electro-optic versions),

$$\delta\theta = \frac{\lambda}{v_s} \cdot \delta\nu_s \qquad \ldots (6.2)$$

where $\delta\nu_s$ is the bandwidth and v_s is the velocity of sound in the material. For a typical commercial device with $\delta\theta = 2.9^\circ$, there are 400 resolvable spots in both the x and y planes (for details see Appendix 7), so if each was 5μm apart on the circuit surface, the total area covered by the 2-D scan would only be 2mm square. Thus nine such beams and deflectors would be needed to cover a 6mm x 6mm chip.

Some magnification will be required if small angular deflections are to produce a spot movement of 2mm after focussing on the i.c. surface. Three different lens arrangements have been modelled on the computer in order to determine which system results in the smallest focussed spot size and largest deflection: the fixed parameters were the laser beam divergence and beam waist which apply to the present 7.5mW laser, a 2.9° angular deflection and the focal lengths of the Ultra-Micro Nikkor focussing lens. Various combinations of expander lenses and inter--element spacings have been simulated, and a composite plot of the results obtained is given in figure 61: the deflection and diameter of the focussed beam are shown as a function of the focal lengths of the expander lenses, and in each case optimum distances between the various lenses and deflector have been used. The three groups of results correspond to the cases of a single convex expander lens, a single concave expander lens and a two lens beam expansion arrangement, as shown. The latter method can be seen to produce a large deflection with small spot size, and one possible configuration which is calculated to give a probe diameter of 3.4μm, deflection of 2mm and depth of focus 4.6μm is shown in figure 62(a).

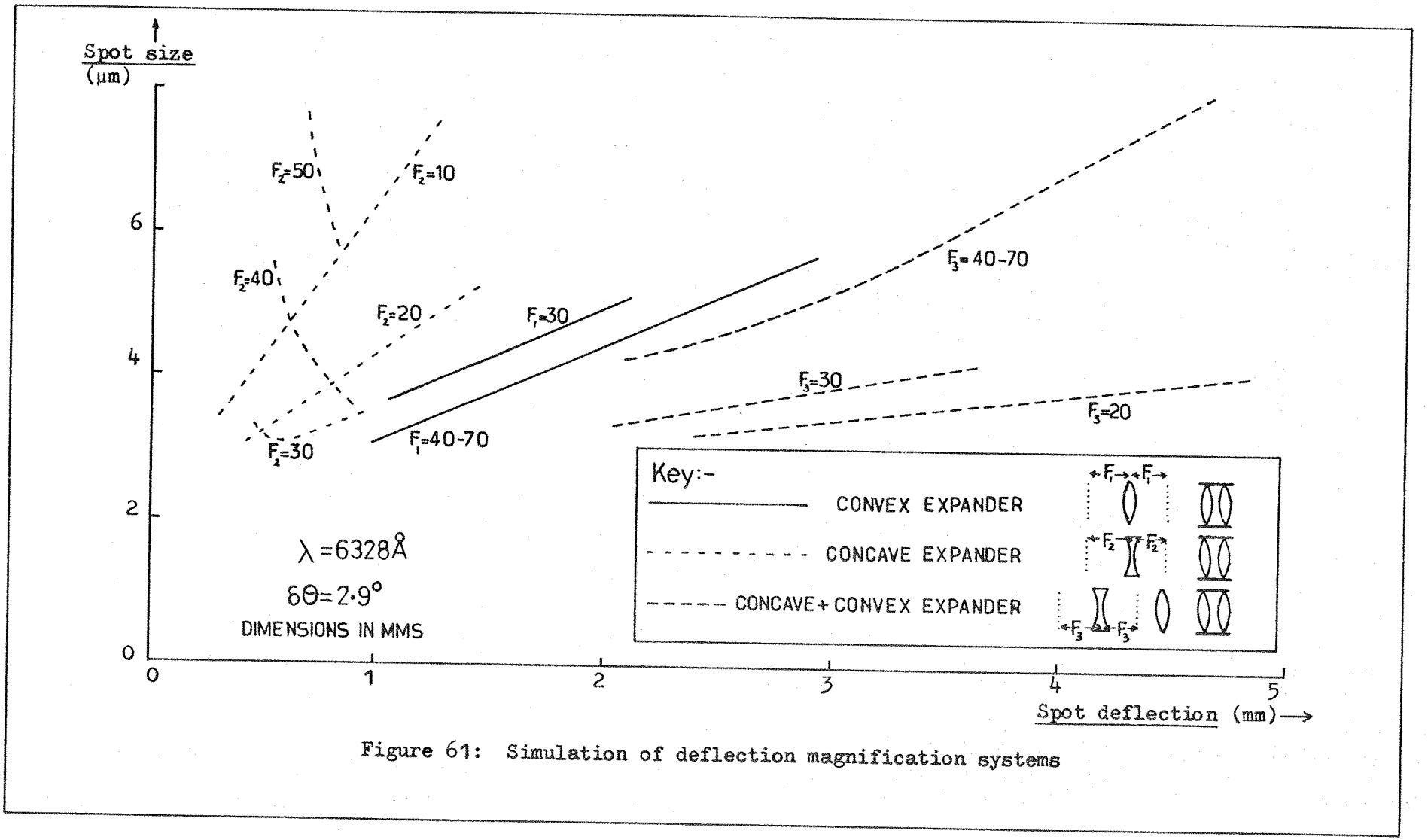


Figure 61: Simulation of deflection magnification systems

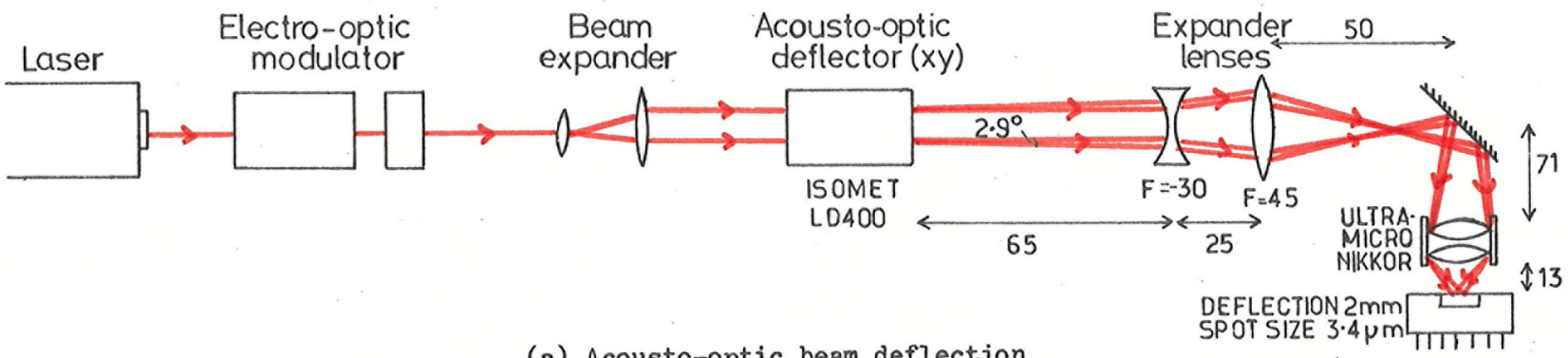
(b) Mechanical deflection

Mirror deflection systems are much cheaper than acousto-optic or electro-optic versions and are also capable of high resolution and accuracy. However the speed of operation is relatively low, with beam repositioning possibly taking longer than 1msec and a full scan of a chip lasting about a minute. There is no serious limitation to the number of resolvable spots for the mechanical deflectors though, so a single beam could be used to sweep across a 6mm square area with a repeatability of 1.5μm and resolution of 0.25μm for example with the system detailed in Appendix 7.

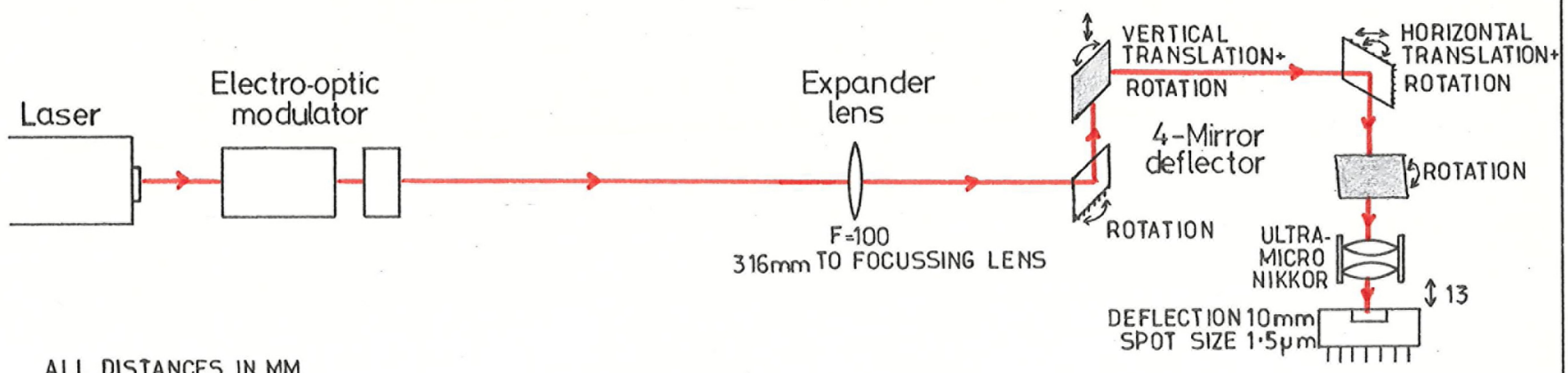
The deflection of the unfocussed laser beam can be related to movement of the light probe upon the circuit surface if the radius of curvature, aperture and magnification of the focussing lens are known. The spot movement over about a 2mm distance for the Ultra-Micro Nikkor lens is a linear function of the unfocussed beam displacement if the in--cident beam is close to the centre of the focussing lens, but when the incoming beam is rotated, the laser spot can be made to move over much larger distances and is limited only by the aperture of the lens. The simple four-mirror system illustrated in figure 62(b) is capable of moving the probe over a 10mm x 10mm area; the rotary movement of the incident beam is used for course beam adjustment and the translational movement in the vertical or horizontal planes is performed with micrometers, giving repeatable positioning on the chip surface to within 1μm. A motorised version of this arrangement would take up to 0.5secs to locate the laser spot at any site in the 10mm square, but alternatives such as a ready-built galvanometer-controlled system designed primarily for laser trimming applications (Appendix 7) could perhaps be adapted to perform this task.

(c) Multiple beam provision

If multiple beams are to be provided, each must have its own deflection system. The mirror configurations tend to be quite bulky, so in order to accommodate a number of these, the prototype arrangement illustrated in figure 62(b) will have to be modified so that the mirrors were positioned before the expander lens, which would need to have a



(a) Acousto-optic beam deflection



ALL DISTANCES IN MM

(b) 4-mirror beam deflection

Figure 62: Alternative beam deflection systems

large aperture stop. The solid-state deflectors are only up to 50mm wide, so there should be no problem in grouping these together.

It is probable that some of the laser inputs to an i.c. will remain stationary for relatively long periods (for example when used to disable feedback loops or to partition the circuit) so not all the beams will need to be quickly moved whilst others are used to inject the data sequences. The cheaper slow mirror deflection methods will therefore be suitable for most of the laser probes, and only a few will require the ability to be repositioned at high speed; as a consequence, a multi-laser deflection system may be comprised of a mixture of acousto--optic and mirror deflectors. The faster-moving light inputs with their limited range of movement will probably have to be located close to the centre of the circuit under test to be most effective, and possible configurations are a 9-beam system with one under the control of an acousto-optic deflector and the remainder using mirror deflection, or 16-beams with four capable of high-speed movement.

6.2.2.3 Beam alignment

The laser probe will need to be positioned to within 10μm of a selected pn-junction, but normal automatic wafer handlers usually allow tolerances of 20μm or more because of the large contact pad targets. The whole prober could be mounted on a specially designed xyθ stage in order to align the beam co-ordinate system and the slice, using positional feedback if the absolute location of two or three reference points on the chip surface can be determined, or alternatively these values could be used to recalculate the co-ordinates of the input sites. These initial points could be found by measuring the photocurrent collected by a junction and noting the position where the laser input was blocked by a metal interconnection, or where the beam passed through small holes which were included in the metallization around the circuit periphery.

If metal masks or holograms are used in conjunction with a 'flood' beam or to ease the task of the deflection system, these will also have to be carefully aligned. A similar approach to this problem

would have to be adopted, with the mask mounted upon a translation and rotation stage and a few reference points used to determine its relative position with respect to the i.c. surface. In each case, this alignment should not take more than a second.

6.2.2.4 Integration with a conventional i.c. tester

DC tests can be performed at the wafer stage with clock rates up to about 5-10MHz, but for higher speeds and some parametric tests it is often necessary to package the device before testing, because of the capacitive loading of the probes and crosstalk problems. In fact some manufacturers prefer to perform the whole test sequence on a packaged circuit, even though the cost of the pack and the bonding constitute a sizeable proportion of the final price of each i.c. This particular test strategy will not be suitable for use with the laser.

The test head and electronics are situated as close as possible to the probes in order to prevent pulse distortion and crosstalk, so some redesign may be required in order to allow optical access to the circuit under test. If satellite test stations are used, each will require its own laser, modulation and deflection apparatus: however it is probable that the use of the laser for production testing will only be economically viable on large complex i.c.'s which normally take a very long time to test (i.e. more than about a second); thus the slow speed of the automatic handling facilities and alignment system would not be too important and multiplexing may not be necessary.

One possible integrated circuit test configuration is shown schematically in figure 63. This uses 9 laser inputs, of which only one tier of three has been illustrated, and a single 50mW laser is used as the light source. The optical transmission through each branch will be approximately 50percent, so a focussed beam power of more than 2mW for each probe will be produced, adequate for M.O.S. and I^2L testing. Only one beam can be deflected at high-speed, but all are individually

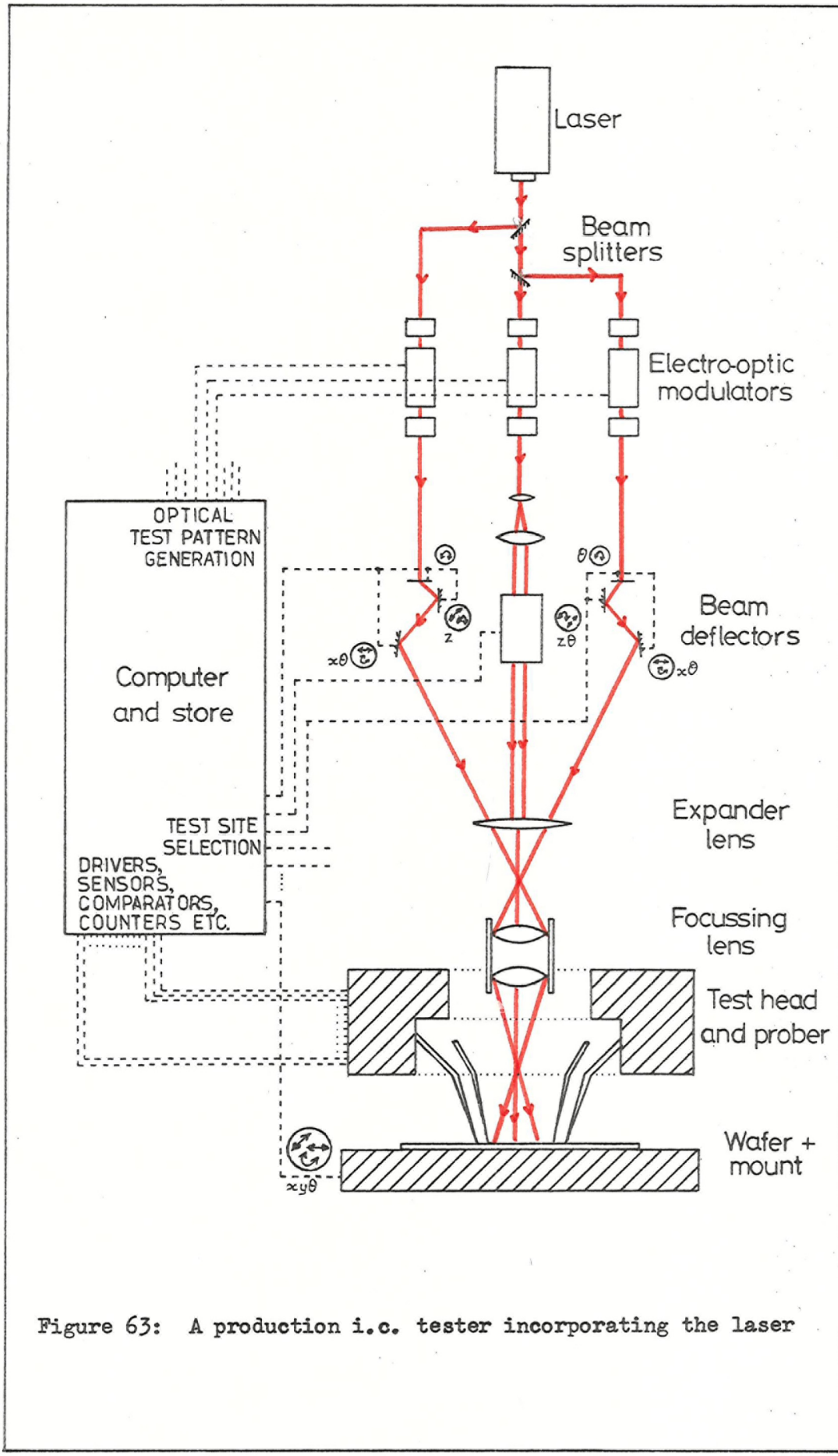


Figure 63: A production i.c. tester incorporating the laser

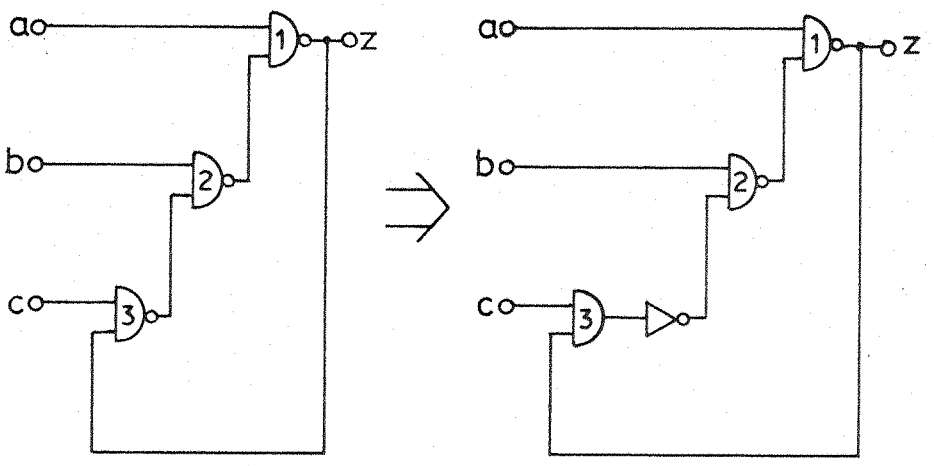
modulated with pockel cells which are capable of operating faster than the maximum clock rate of the tester. The total cost of the add--itional laser, optics and deflection system would be about £35,000 (see Appendix 7), but if separate 50mW lasers are used to enable laser testing of T.T.L., E.C.L., and C.D.I. etc., this would increase to nearly £75,000. This is still well below the price of conventional A.T.E. though, which at the present time is in the range £100,000-£250,000.

High-speed go/no-go testing using multiple laser inputs would therefore be costly, but this capital expenditure could be quickly repaid if the testing time per device was significantly reduced, because the volume of i.c. production is so great and the testing time accounts for a large proportion of the final price of each device (section 2.4). Indeed, use of the laser for production testing may even allow hitherto 'untestable' circuits to be manufactured and tested in a reasonable time.

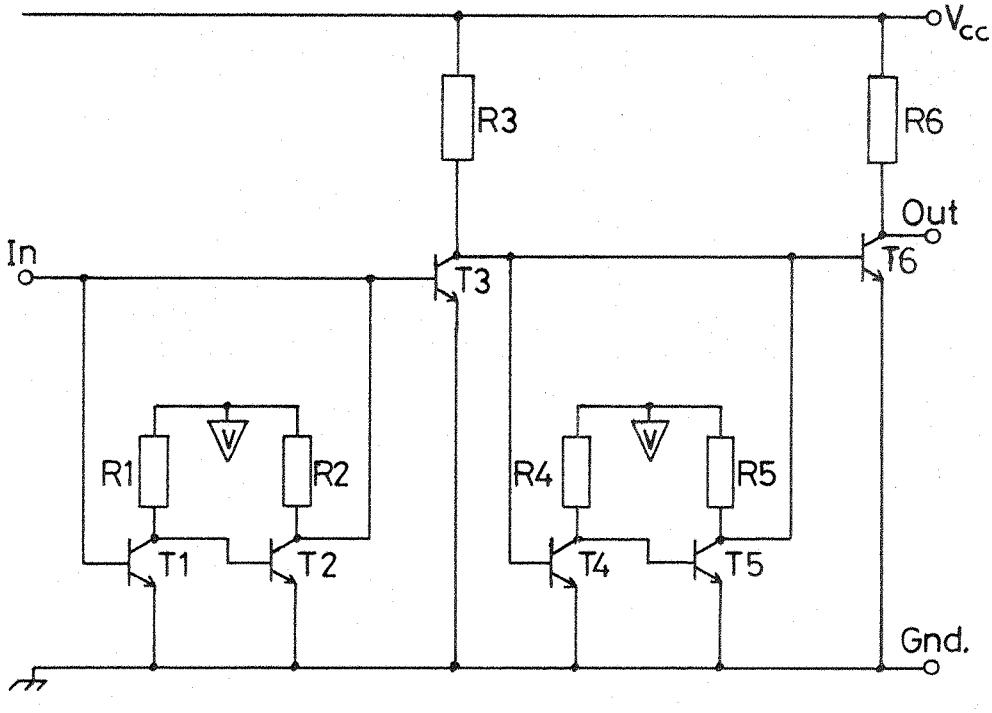
6.3 Design of Laser-Testable Circuits

One of the most important features of the laser method of i.c. testing is that it can be used on any conventionally-designed device. Manufacturers are very reluctant to incorporate even small modifications into the circuit design for testing purposes alone, but in some cases this has proved to be necessary, as for example in a recent nine-decade counter which had to be divided into three blocks with accessible test points in order to reduce the testing time to three hours. However, greater reductions in the test time and less stringent requirements for beam control could result if circuits were designed with laser testing in mind.

Complementary nodes have been found in nearly all the i.c.'s investigated (see section 5.3.2) but it is possible that in some cases the inability to inject both a logical '1' and '0' at a certain node could limit the usefulness of the laser input. For example, in the simple circuit illustrated in figure 64(a), the secondary input to gate 2 is a function of the output level and could be disabled if it was held at



(a) Provision of complementary nodes



(b) Photosensitive bistable

Figure 64: Circuit redesign to enhance laser testing

'1'. For T.T.L. NAND-gates though, the laser can only force the output to ground or the '0' level; but if gate 3 was implemented in the form of an AND-NOT combination as shown in the second diagram, this problem could be solved. In general, the inclusion of a two-inverter stage to any circuit branch would ensure that a complementary node was available.

High laser powers have been found to be necessary to inject data into some types of i.c., thereby making laser testing impractical. However by using specially introduced transfer gates under the control of an externally applied signal, the laser power requirement could be reduced by orders of magnitude: also in C.M.O.S. circuits a few p-M.O.S. or n-M.O.S. gates could be implemented with the same effect; this would result in a rise in the power dissipation and probably a degradation of the frequency response, but if the number of these gates was kept low, this problem may not be too severe. Photosensitive bistables could be built into the circuit to enable certain nodes to be held at a fixed level even if the laser beam is subsequently removed. The arrangement shown in figure 64(b) could perform this task, holding the output at either '0' or '1' when the beam is directed at T2 or T5 respectively; if it is only necessary to inject a '1' at a particular site then a single flip-flop and inverter would be required. Large value resistors could be used to limit the laser power requirements, and similar circuit configurations could be used for other logic families.

The accuracy constraints imposed upon the deflection system and the mean time taken to reposition the laser beams could be reduced if the optical input sites were enlarged and located reasonably close to each other in a certain portion of the i.c. surface. It may be necessary to adopt measures such as these when minute-geometry circuits come into production because sub-micron layout tolerances may then be used. Careful design of the chip would also ensure that important junctions were not placed too close to each other, in order to maintain nodal isolation, and that no metallization layers covered the test sites.

6.4 Future Possibilities

Advances in semiconductor laser or LED technology could mean that in the future either or both of these light sources would be sufficiently powerful and of a suitable wavelength to be utilized as an alternative to the gas laser. Their use would result in a much more compact and cheaper optical system,and may even enable large numbers of beams to be provided; if there were enough individual beams, each could be fixed in position over a certain input site but only a few need be used at any one time for test purposes,thereby eliminating the necessity for deflection apparatus. A further possibility is that LED sources could be built into the i.c. during manufacture and positioned over selected photodiodes, obviating all alignment and focussing problems.

Only the concept of optical inputs has been considered in this study, but it is also possible to sense the state of internal sites using a laser probe[112]. At present this is achieved by monitoring the power supply current variations as the laser is scanned across the circuit surface, and so is not suitable for clock frequencies over about 1kHz; if such methods were improved to enable the laser to be used as an extra output as well as an extra input, the potentiality for a reduction of the test time in complex i.c.'s would be very large and fault diagnosis would be greatly eased.

CHAPTER 7

CONCLUSION

7. CONCLUSION

A new method of integrated circuit testing has been presented in this thesis, and the results which have been obtained indicate that by using a focussed laser beam, the time taken for production testing can be reduced and improvements in the ease and resolution of diagnostic testing can be gained.

The laser produces a current within an i.c. and so the light beam can act as a very small, non-contacting probe. In the present arrange-ment, the laser probe is typically 2μm in diameter and a photocurrent of 0.75mA can be generated in the silicon semiconductor. An electro-optic modulator has been used to control the light beam intensity, thereby enabling data input sequences to be optically injected into the i.c. under test at rates up to 7MHz.

The target for the laser probe in the integrated circuit interior is a pn-junction. The photocurrent crossing the junction reaches a maximum when the beam is positioned on the junction edge, but if it is displaced to one side the photocurrent drops as a function of the distance and carrier diffusion length, causing a proportional increase in the laser power requirement. When two junctions are close to each other it has been shown that there is some mutual isolation and relatively large laser powers are necessary to inject information at both sites simultaneously, and this can be more than an order of magnitude greater than the power needed to access one input only: thus a beam misalignment of about 5-10μm can be tolerated in all circuits tested to date.

Even though the laser beam generates a current which adds to and does not annihilate those already flowing in a circuit (so that a logical '0' or '1' and not both together can be inserted at any particular site), this has not proved to be a serious limitation in practice because complementary nodes have been available to the laser probe, and data of the opposite logical type can be injected by changing the beam position.

The laser power requirements for testing different kinds of integrated circuit have been determined both experimentally and analytically, and it has been shown that these power levels are closely related to the circuit implementation. M.O.S., I^2L and C.C.D.'s need a relatively low laser probe power of under 1mW which could be provided by a small cheap laser, but other logic families such as T.T.L., E.C.L., and C.D.I. will need laser powers of up to an order of magnitude more. C.M.O.S. i.c.'s require such a large photocurrent to input data optically that it is probable that laser testing in this case will not be economically feasible. Some linear circuits have also been probed by the laser and here the results have provided some useful details about the currents which flow in the circuit under normal operating conditions, but in general the photocurrent has a significant effect only in the input stages of these devices, when it is greater than or comparable to the circuit current levels.

By observing in detail the interaction between the laser input and the circuit under test, some features of the internal circuit operation (such as transient responses and propagation delays) can be measured; furthermore the diffusion length and lifetime of minority carriers in the semiconductor substrate can be easily determined by recording the photocurrent collected by one accessible pn-junction as the probe is moved away from it or when the laser light is removed.

In the field of i.c. testing, the laser input can be used in two roles: as a diagnostic tool and as an aid to production (go/no-go) testing. Diagnostic testing involves both the detection and isolation of a fault so that the failure mechanism can be identified. The use of a single laser beam in this context would bring several advantages over the methods presently employed: the position of the additional input can be easily moved around the circuit but unlike microprobes which can be up to ten times larger, the laser probe will not damage the device or load internal nodes. Any fault can therefore be quickly located to the pn-junction where it first becomes effective, i.e. the resolution

achieved is often one stage better than that obtained with conventional methods where failures are isolated to the gate or module level. In some cases, faults of a parametric nature can be found and their cause determined because certain internal transient responses can be accurately measured; also an indication of the processing conditions can be obtained by determining the injected carrier diffusion length and lifetime at various stages during the device fabrication. The simple non-destructive laser technique also gives a limited ability to measure spatial variations in these two parameters and can be used to identify failure mechanisms in the bulk semiconductor.

Speed is essential in production testing, but even with test rates of 10MHz it can still take minutes or hours to comprehensively test l.s.i. and v.l.s.i. The ability to access more of a circuit via laser probes can be used to cut down test sequence length and so reduce the total testing time: clearly a large number of test inputs are needed to simplify and shorten the test programmes to a maximum extent, but the cost and complexity of a multi-laser beam system will restrict its use to manufacturers and testers who already need extremely expensive computer-controlled automatic test equipment. Highly significant savings in the test time will be gained when the laser method is used in conjunction with conventional methods of production testing though, so the initial capital outlay should be quickly regained.

A summary of the major applications for the technique of probing integrated circuits by a laser is presented in figure 65. Use of the laser beam as an extra circuit input will considerably ease the task of testing the modern generations of l.s.i. and v.l.s.i., and also improve the chances of quickly locating the cause of any faults which do occur; it is even possible that device cost may be reduced as a result and that laser testing may enable the semiconductor industry to extend its limits still further and develop a new class of testable e.l.s.i. (extremely large scale integrated circuits).

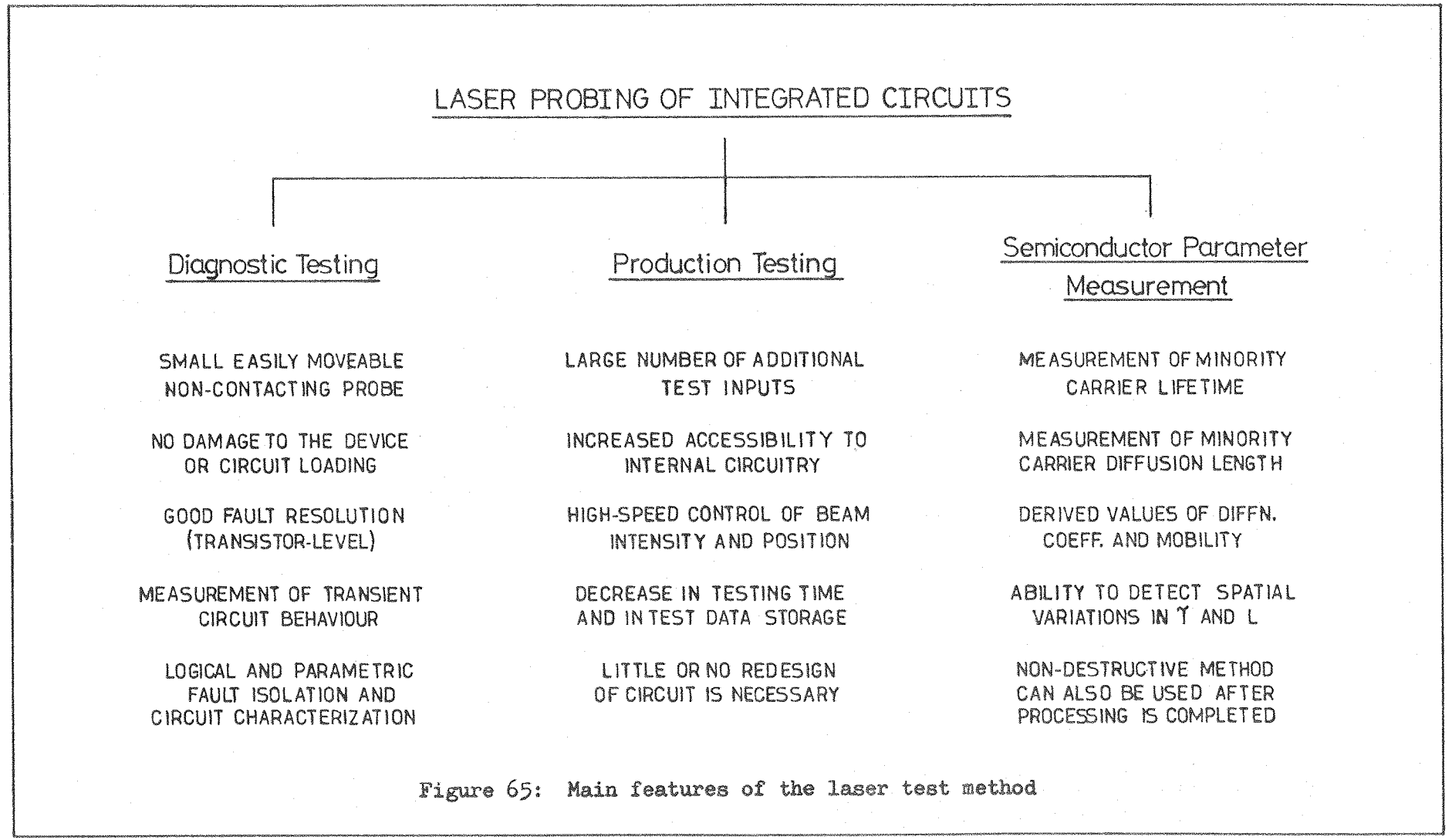


Figure 65: Main features of the laser test method

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APPENDICES

- Gaussian beams
- Reflection and interference
- Injection levels and excess carrier distribution
- Computer simulation of excess carrier distribution
- Nodal isolation
- M.O.S. circuit analysis
- Laser i.c. test equipment
- Published paper

APPENDIX 1. GAUSSIAN BEAMS

A gaussian beam has an intensity distribution which is described by the equation:

$$I(r) = I_o \cdot \exp(-2r^2/w^2) \qquad \ldots (A1.1)$$

where I_o is the on-axis intensity and I is the intensity at a radius r away[40]. The beam width, w, is defined as the distance in the transverse direction over which the intensity drops to e^{-2} of its peak value (see figure A1(a)), and at any position z along the axis, w can be found from the equation:

$$w^2(z) = w_o^2 \cdot \left[1 + \left(\frac{\lambda . z}{\pi . w_o^2}\right)^2\right] \qquad \ldots (A1.2)$$

w_o is the beam waist located at the origin z=0, where the phase front of the propagating wave becomes plane; this function is illustrated in figure A1(b). For large values of z the beam expands in a linear manner, with the far-field divergence angle ϕ (for small angles) given by:

$$\tan\phi \simeq \phi = \lim_{z\to\infty} \frac{dw}{dz} = \frac{\lambda}{\pi . w_o} \qquad \ldots (A1.3)$$

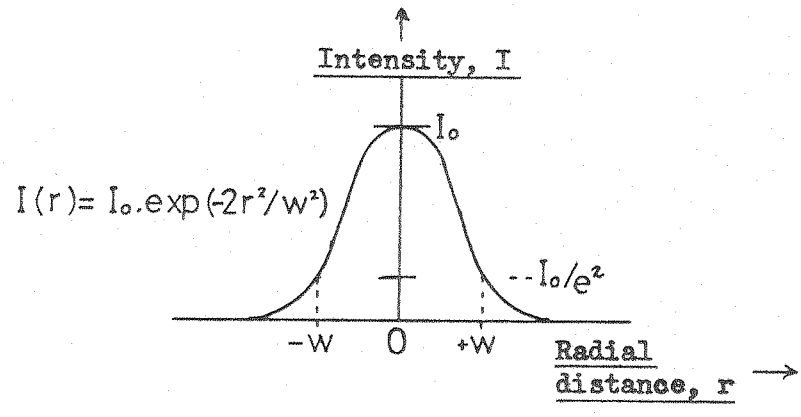
The total power of the beam, P, is related to the peak intensity I_o by:

$$P = \int_o^\infty I(r) . 2\pi r . dr = I_o \cdot \frac{\pi w_o^2}{2} \qquad \ldots (A1.4)$$

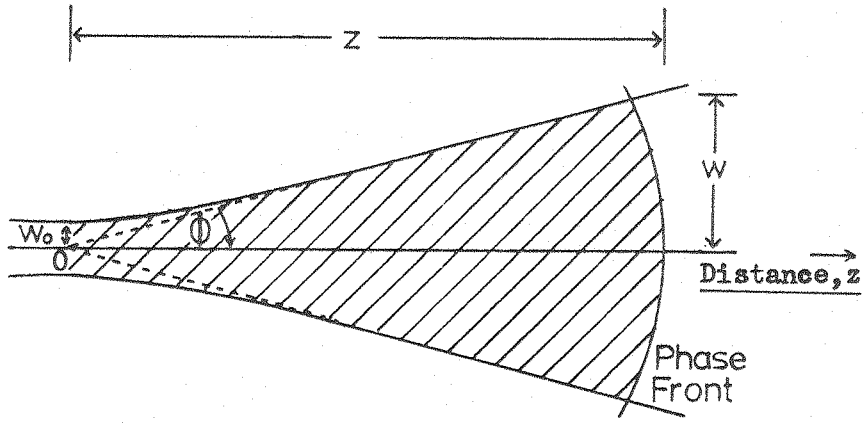
When a gaussian beam passes through an ideal lens, a new beam waist is formed, as shown in figure A1(c): the incident beam has a waist w_1 located at a distance d_1 from the lens and this is transformed to produce the new waist w_2 at a position d_2 away. These parameters can be calculated from the following relationships:

$$\frac{1}{w_2^2} = \frac{1}{w_1^2} \cdot \left(1 - \frac{d_1}{f_2}\right)^2 + \frac{1}{f_2^2} \cdot \left(\frac{\pi w_1}{\lambda}\right)^2 \qquad \ldots (A1.5)$$

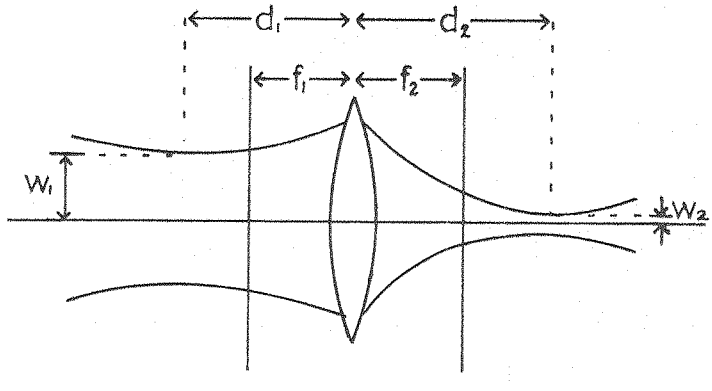
$$d_2 = f_2 + \frac{(d_1 - f_2) . f_2^2}{(d_1 - f_2)^2 + \left(\frac{\pi w_1^2}{\lambda}\right)^2} \qquad \ldots (A1.6)$$



(a) Gaussian intensity distribution



(b) Propagation from a waist w_o



(c) Transformation by a lens

Figure A1: Gaussian beams

If the divergence angle ϕ is small, then the width of the beam at the lens surface will be approximately equal to the waist w_1. Additionally, if the term $\frac{1}{w_1^2}\cdot\left(1-\frac{d_1}{f_2}\right)^2$ contributes little to the value of w_2:

$$d_2 \simeq f_2 \qquad \ldots (A1.7)$$

and $$w_2 \simeq \frac{f_2.\lambda}{\pi.w_1} \simeq f_2.\phi \qquad \ldots (A1.8)$$

i.e. the radius of the focussed spot is directly proportional to the ratio of the focal length of the lens and the untransformed waist w_1; thus the smallest spot size for a given wavelength of light can be obtained by minimising the f/number of the lens. The maximum value of w_1 is limited by the lens aperture, therefore the minimum spot diameter is:

$$d_g = \frac{2.f_2.\lambda}{\pi.\left(\frac{\text{aperture}}{2}\right)} \simeq \frac{2.\lambda}{\pi.NA} \qquad \ldots (A1.9)$$

where NA is the numerical aperture of the lens. The value of d_g is smaller than the diffraction-limited spot size obtained for a uniform intensity beam and lens of circular exit pupil, where the diameter of the bright central disc in the diffraction pattern (the Airy disc) is[113]:

$$d_A = \frac{1{\cdot}22.\lambda}{NA} \qquad \ldots (A1.10)$$

If specific limits are imposed upon the width variation, equation (A1.2) can be used to find the depth of focus, z_d. For an increase in the focussed spot radius of 5percent in an axial distance z_d, then

$$z_d = \pm\frac{0{\cdot}32.\pi.w_2^2}{\lambda} \qquad \ldots (A1.11)$$

The values of the minimum spot size and depth of focus theoretically attainable with the focussing lenses detailed in section 3.4.1 are given in table A1 below (λ = 6328Å).

	x5 Objective	x10 Objective	x20 Objective	x40 Objective	Ultra-Micro Nikkor lens
Spot size (μm)	2.69	1.61	0.81	0.62	1.44
Depth of focus (μm)	2.87	1.03	0.26	0.15	0.82

Table A1: Spot size and depth of focus for focussing lenses

APPENDIX 2. REFLECTION AND INTERFERENCE

(a) Reflection at a boundary

The intensity reflectance, R, for polarized monochromatic light incident at a boundary between two ideal dielectrics of refractive indices n_1 and n_2 $(n_2 > n_1)$ is described by the Fresnel equations[114]:

$$R_{\parallel} = \left(\frac{n_2 \cos\theta_i - n_1 \cos\theta_t}{n_2 \cos\theta_i + n_1 \cos\theta_t} \right)^2 \qquad \ldots (A2.1)$$

and

$$R_{\perp} = \left(\frac{n_1 \cos\theta_i - n_2 \cos\theta_t}{n_1 \cos\theta_i + n_2 \cos\theta_t} \right)^2 \qquad \ldots (A2.2)$$

where θ_i and θ_t are the angles of incidence and transmission (see figure A2) and the subscripts '$\parallel$' and '$\perp$' refer to the cases of light polarization parallel and perpendicular to the plane of incidence respectively.

The numerator of equation (A2.1) becomes zero when $\cos\theta_i = \frac{n_1}{n_2}.\cos\theta_t$, whereas the numerator in the equation for $R_{\perp}$ can never be zero in the case under consideration $(n_2 > n_1)$. Thus for a certain angle of incidence, $\theta = \tan^{-1}\left(\frac{n_2}{n_1}\right)$, called the Brewster angle, the reflectance of polarized light vibrating parallel to the plane of incidence drops towards zero for increasing values of the angle of incidence, then rises steeply after the Brewster angle has been reached.

(b) Interference in a thin layer

In a three-medium system with $n_1 < n_2 < n_3$, the simple Fresnel relationships do not hold, but although zero reflectance is never attainable in the $R_{\parallel}$ characteristic, there is still a pronounced minimum in the response at the Brewster angle for the first and second layers[24]. A schematic representation of the light propagation through such an arrangement is shown in figure A2. Phase changes are introduced, so the amplitude reflectance (r) and transmittance (t) are used. The intensity reflectance and transmittance are related to r and t through the identities

$$R = r.r^* \qquad T = t.t^* \qquad \ldots (A2.3)$$

where r^* is the complex conjugate of r etc. γ is the phase change

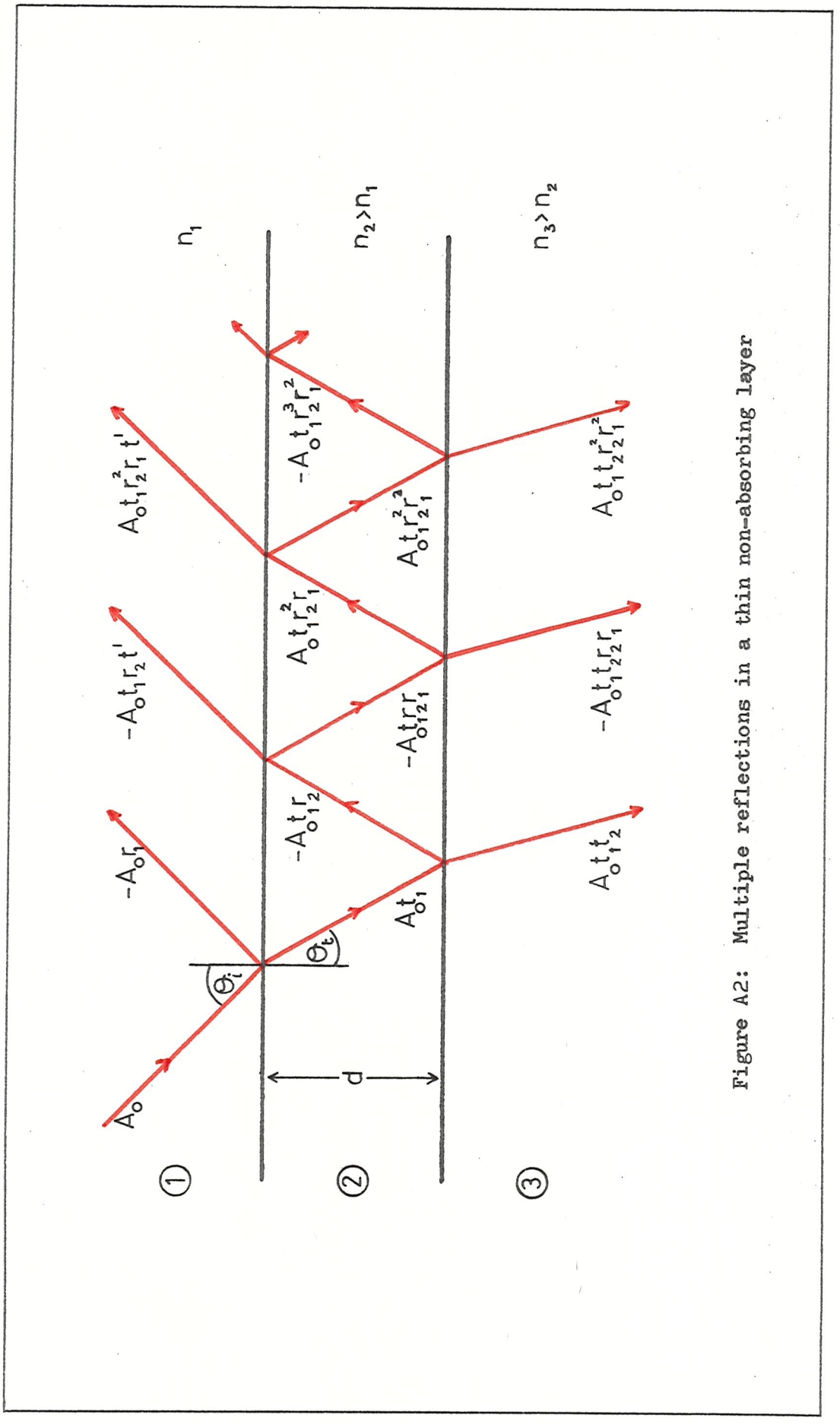


Figure A2: Multiple reflections in a thin non-absorbing layer

introduced during one transversal of the central layer, thickness d, so

$$\gamma = \frac{2.\pi.n_2.d}{\lambda}.\cos\theta_t \qquad \ldots (A2.4)$$

The total reflectance r_{tot} can be seen to be composed of many terms with multiple reflections occurring in layer ②, i.e.

$$A_o r_{tot} = -A_o r_1 - A_o t_1 r_2 t' e^{-2i\gamma} + A_o t_1 r_2^2 r_1 t' e^{-4i\gamma} \ldots \qquad \ldots (A2.5)$$

$$\therefore\ r_{tot} = -r_1 - \frac{t_1 t' r_2 e^{-2i\gamma}}{1 + r_1 r_2 e^{-2i\gamma}} \qquad \ldots (A2.6)$$

where A_o is the incident light amplitude, r_1 and r_2 are the reflections at the upper and lower boundaries respectively, t_1 is the amplitude transmission from medium ① to medium ②, t' is the transmission from ② to ① and t_2 is the transmission into layer ③ from layer ②.

If absorption is assumed to be negligible in layer ②, then the total intensity reflectance and transmittance can be found from equations (A2.3) and (A2.6):

$$R_{tot} = \frac{r_1^2 + r_2^2 + 2r_1 r_2.(1 - 2\sin^2\gamma)}{(1 + r_1 r_2)^2 - 4r_1 r_2 \sin^2\gamma} \qquad \ldots (A2.7)$$

$$T_{tot} = \frac{(1 - r_1^2).(1 - r_2^2)}{(1 + r_1 r_2)^2 - 4r_1 r_2 \sin^2\gamma} \qquad \ldots (A2.8)$$

The light intensity transmitted into the third medium is therefore strongly dependent upon the thickness of the central layer, d, because of the $\sin^2$ term. For an air-SiO_2-Si system, r_1 and r_2 can be calculated to be 0.19 and 0.44 respectively for a zero angle of incidence light beam, since at the HeNe laser wavelength, $n_2 \equiv n_{SiO_2} = 1.46$ [115] and $n_3 \equiv n_{Si} = 3.8$ [116] so

$$T = \frac{1}{1{\cdot}51 - 0{\cdot}43 \sin^2(4{\cdot}6.\pi.d)} \qquad \ldots (A2.9)$$

where d is in microns. Under these conditions, the transmittance shows a periodic variation from 92.5% to 66.2% with changing oxide thickness.

APPENDIX 3. INJECTION LEVELS AND EXCESS CARRIER DISTRIBUTION

(a) Semiconductor parameter variation with injection level

The value of the effective diffusion coefficient, D, in common with most of the other semiconductor parameters is dependent upon the carrier injection level. If δn and δp are the excess concentrations of electrons and holes, and n_o and p_o are the carrier concentrations in thermal equilibrium, then[45]

$$D = \frac{n_o + \delta n + p_o + \delta p}{\frac{n_o + \delta n}{D_p} + \frac{p_o + \delta p}{D_n}} \qquad \ldots (A3.1)$$

where D_p and D_n are the diffusion coefficients for holes in n-type and electrons in p-type material respectively. In n-doped material, $p_o \ll n_o$ so that in neutral regions when $\delta n = \delta p$ and under low injection conditions where $\delta n \ll n_o$,

$$D = D_l = D_p \qquad \ldots (A3.2)$$

and for high injection with $\delta n \gg n_o$,

$$D = D_h = \frac{2.D_p.D_n}{D_p + D_n} \qquad \ldots (A3.3)$$

where the subscripts 'l' and 'h' refer to low and high level injection respectively.

The effective carrier lifetime, τ, is given by:

$$\tau = \tau_p \cdot \frac{n_o + \delta n + n_1}{n_o + \delta n + p_o} + \tau_n \cdot \frac{p_o + \delta p + p_1}{n_o + \delta p + p_o} \qquad \ldots (A3.4)$$

at room temperature, where τ_p and τ_n are the minority carrier lifetimes of holes in highly doped n-material and electrons in highly doped p-type, and p_1 and n_1 are the concentrations of holes and electrons which would exist if the fermi level lay at the same energy level as the recombination centres. Therefore for n-type material with $\delta n = \delta p$, the fermi level above the trap level and low level injection,

$$\tau = \tau_l = \tau_p \qquad \ldots (A3.5)$$

and for high injection,

$$\tau = \tau_h = \tau_p + \tau_n \qquad \ldots (A3.6)$$

Between these two limits, which in practice are found to be approximately $\delta n \leq 0.1 \times n_o$ for low injection and $\delta n \geq 10 \times n_o$ for high injection[46,117], τ varies as a function of $\delta n/n_o$.

The diffusion length, L, is related to the diffusion coefficient and lifetime through the expression

$$L = \sqrt{D.\tau} \qquad \ldots (A3.7)$$

thus $$L_l = \sqrt{D_p.\tau_p} \qquad \ldots (A3.8)$$

and $$L_h = \sqrt{\frac{2.D_p.D_n.(\tau_n + \tau_p)}{D_p + D_n}} \qquad \ldots (A3.9)$$

again for n-type material.

(b) 3-D excess carrier distribution

When a laser beam hits the surface of a uniformly doped n-type semiconductor, the excess hole distribution can be considered to be constant at a maximum level of δp_{max} within a finite volume (the source) whose dimensions are determined by the properties of the incident light beam and penetration depth within the semiconductor; away from this region the hole concentration decays as a function of distance and diffusion length. The continuity equation cannot be solved directly under these conditions, so in order to determine the carrier distribution in 3-D analytically, a simple approximation to the finite carrier generation source has had to be made, and a method of superposition has been used to extend the solution to a rectangular co-ordinate system.

For a laser beam of width w incident upon a material of absorption coefficient α, the distribution of the light intensity I can be found from Appendix 1 and section 3.1.1,

$$I(x,y,z) = I_o \cdot \exp\left(\frac{-2(x^2 + y^2)}{w^2}\right) \cdot \exp(-\alpha z) \qquad \ldots (A3.10)$$

where I_o is the maximum intensity, at a position $x = y = z = 0$.

If g is the carrier generation rate per unit volume, the total generation rate G is given by the volume integral:

$$G = \oint_V g(x,y,z).dV = \int_{x=0}^{\infty}\int_{y=0}^{\infty}\int_{z=0}^{\infty} g.\exp\left(\frac{-2(x^2+y^2)}{w^2}\right).\exp(-\alpha z).dxdydz \qquad \ldots (A3.11)$$

$$\therefore G = \frac{w^2.\pi.g}{8\alpha} \qquad \ldots (A3.12)$$

for a semi-infinite semiconductor. The 'centre of gravity', h, of the generation volume is equal to

$$h = \frac{\oint_V z.g(x,y,z).dV}{\oint_V g(x,y,z).dV} = 1/\alpha \qquad \ldots (A3.13)$$

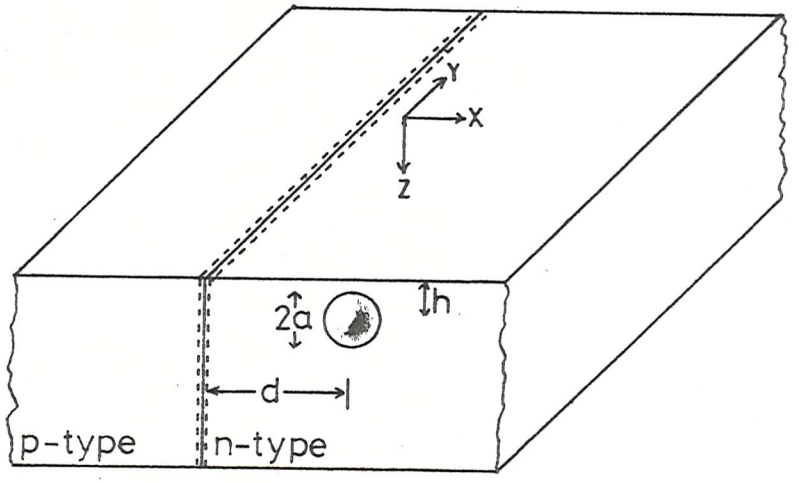
From equation (A3.10) it can be seen that the light intensity decays as an exponential function of distance in all directions and only reaches zero at infinity, so an arbitrary boundary of the generation region is chosen: this is the distance at which the intensity falls to $1/e^2$ of its peak value. The resulting volume is a distorted cone, with a base of radius w on the surface of the semiconductor and apex at a depth $2/\alpha$ below, as shown in figure A3(b). Three approximations to this shape have been proposed to simplify the analysis, and in each case the volumes are adjusted so that they are equal. The models are a hemisphere with radius a and centre at a depth h below the surface, a sphere of radius a and centre at depth h and thirdly a cylinder of length 2h and radius a. The values of radius a in terms of w and α are shown in table A2.

For each of the three generation volumes, the injected carrier density at a distance r from the centre, $\delta p(r)$, can be calculated by analogy with the electrostatics case of the potential variation at r from a body with a distributed internal charge. By using a concept of generation or recombination centre images, the three-dimensional carrier distribution can be found by superposition after each source or sink has been separately considered (see figure A4(a)). A pn-junction situated at a distance d away acts as a region of infinite recombination velocity, and for zero surface recombination velocity the surface acts as a mirror, so

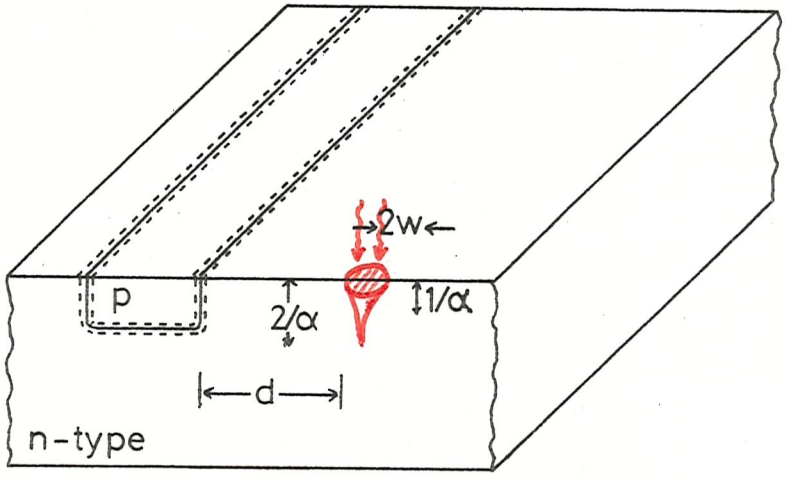
$$\underline{s=0} \quad \delta p(x,y,z) = \delta p(r) + \delta p(r') - \delta p(r_1) - \delta p(r_1') \qquad \ldots (A3.14)$$

but for infinite surface recombination velocity,

$$\underline{s=\infty} \quad \delta p(x,y,z) = \delta p(r) - \delta p(r') - \delta p(r_1) + \delta p(r_1') \qquad \ldots (A3.15)$$



(a) Spherical approximation for carrier source

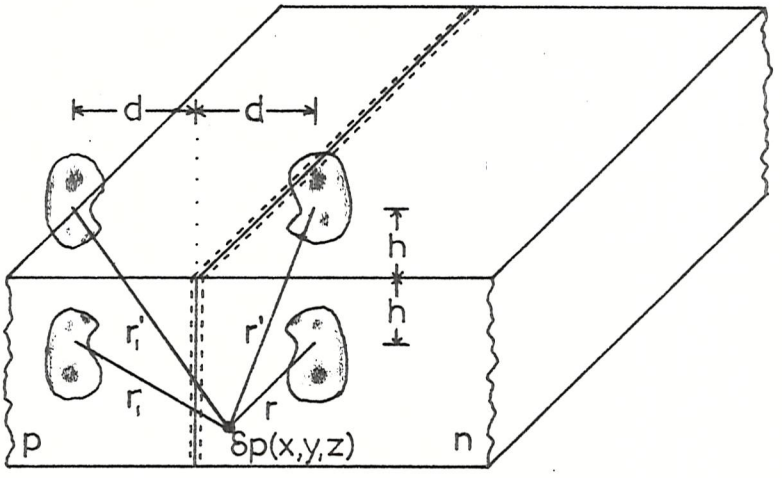


(b) Laser generation of excess carriers

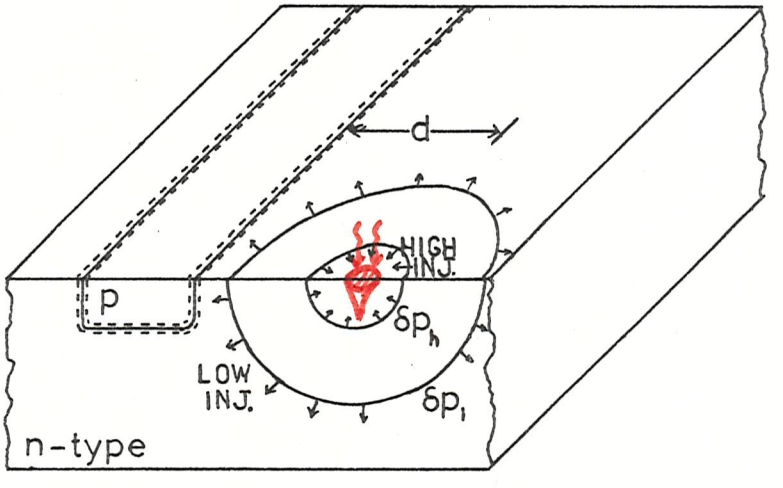
Figure A3: Models of the generation volume

		Hemisphere	Sphere	Cylinder
Radius a		$0{\cdot}53 \cdot \sqrt[3]{\frac{w^2}{\alpha}}$	$0{\cdot}42 \cdot \sqrt[3]{\frac{w^2}{\alpha}}$	$0{\cdot}31 \cdot w$
$\delta_p(r)$	$r \leqslant a$	$\frac{G}{4\pi Da} \cdot \left(3 - \frac{r^2}{a^2}\right)$	$\frac{G}{8\pi Da} \cdot \left(3 - \frac{r^2}{a^2}\right)$	$\frac{G \cdot \left(1 - \frac{r^2}{a^2} + 2.\log_e\left(\frac{1}{a}\right)\right)}{8\pi Dh}$
	$r > a$	$\frac{G \cdot \exp(-r/L)}{2\pi Dr}$	$\frac{G \cdot \exp(-r/L)}{4\pi Dr}$	$\frac{G \cdot \exp(-r/L) \cdot \log_e\left(\frac{1}{r}\right)}{4\pi Dh}$
δp_{max}	$s=0$	$\frac{G}{4\pi D} \cdot \left(\frac{3}{a} + \frac{1}{h}\right)$	$\frac{G}{8\pi D} \cdot \left(\frac{3}{a} + \frac{1}{h}\right)$	$\frac{G}{8\pi Dh} \cdot \left(1.5 + 3.\log_e\left(\frac{1}{a}\right)\right)$
	$s=\infty$	$\frac{G}{4\pi D} \cdot \left(\frac{3}{a} - \frac{1}{h}\right)$	$\frac{G}{8\pi D} \cdot \left(\frac{3}{a} - \frac{1}{h}\right)$	$\frac{G}{8\pi Dh} \cdot \left(0.5 + \log_e\left(\frac{1}{a}\right)\right)$

Table A2: Simple approximations to the generation volume



(a) Concept of carrier source images



(b) Limits of the high and low injection regions

Figure A4: 3-D carrier distribution

where the r, r', r_1, r_1' distances are defined in figure A4(a). The junction depth can be assumed to be infinite for all except very small values of d ($d \ll L$). A schematic representation of the approximation for a spherical generation source is shown in figure A3(a), where it may be compared with the more realistic case shown below. In each of the three models, the maximum excess carrier concentration δp_{max} occurs when $r = 0$ and $r' = 2h$ (assuming that $a,h < L$ and $r_1, r_1' > L$), and these values are also listed in table A2.

The relative merit of these three solutions has been determined by a comparison with a measured value of the peak carrier concentration generated by a laser spot power of 1mW and width w of 5μm. This result was taken on a 166 JGSJCW circuit, for which the diffusion length, lifetime and quantum efficiency are known, using an infra-red technique[36]. δp_{max} was found to be $2.2 \pm 0.3 \times 10^{16}$ cm^{-3} ($n_o = 5 \times 10^{15}$ cm^{-3}). For a 1mW laser, the total generation rate, G, is 1.12×10^{15} sec^{-1} so the following results are predicted from the formulae given in table A2:

(i) Hemisphere	s=0	$\delta p_{max} = 9.7 \times 10^{16}$ cm^{-3}
	s=∞	$\delta p_{max} = 5.4 \times 10^{16}$ cm^{-3}
(ii) Sphere	s=0	$\delta p_{max} = 5.9 \times 10^{16}$ cm^{-3}
	s=∞	$\delta p_{max} = 3.7 \times 10^{16}$ cm^{-3}
(iii) Cylinder	s=0	$\delta p_{max} = 6.1 \times 10^{17}$ cm^{-3}
	s=∞	$\delta p_{max} = 2.0 \times 10^{17}$ cm^{-3}

The value of surface recombination velocity is expected to be close to zero (see section 4.2), so it can be seen that all three models give an overestimate of the true value of δp_{max}, but the spherical approximation yields the closest agreement. Thus the carriers will be assumed to be generated within a sphere of radius $a = 0.42\sqrt[3]{\frac{w^2}{\alpha}}$ with a centre $h = 1/\alpha$ below the surface (figure A3(a)).

(c) Injection levels

The value of δp_{max} is above the substrate doping concentration for the case previously considered with a 1mW laser beam, but at a certain distance away from the generation point, the excess carrier concentration $\delta p_{max}(x,y,z)$ will fall below n_o. As shown in figure A4(b), the boundaries

of the regions over which high and low injection conditions prevail are defined as the position at which the injected carrier concentration is δp_h and δp_l respectively.

δp_h is chosen to be the value of hole concentration on the contour within which 75% or 90% of the total current flows (denoted $\delta p_h(75\%)$ and $\delta p_h(90\%)$ respectively). Inside this region, the variation in current density with distance d is the same as if the whole of the n-type semiconductor is under high injection. This method of defining the injection level boundaries has been taken from a publication by Berz and Kuiken[47], in which are given the constants of proportionality needed to calculate δp_h. In a similar way, low-level injection conditions hold when $\delta p_l < n_o$. This boundary is arbitrarily assumed to be reached when the total contributions of $\delta p(r_1)$ and $\delta p(r_1')$ to the value of $\delta p(x,y,z)$ (equations (A3.14), (A3.15) and figure A4(a)) is less than 10%. This roughly corresponds to a hemispherical excess carrier distribution.

(d) Diffusion length

The following analysis also is based upon the work of Berz and Kuiken[47]. In the steady-state, the continuity equation is[50]:

$$D.\nabla^2(\delta p) - \frac{\delta p}{\tau} + g = 0 \qquad \ldots (A3.16)$$

The current density, J, crossing an infinitely deep pn-junction positioned at $x = 0$ and semi-infinite in the y-direction is given by:

$$J = q.D_1.\int_{y=0}^{\infty}\int_{z=0}^{\infty} \frac{\partial(\delta p)}{\partial x}\,.dydz \qquad \ldots (A3.17)$$

where D_1 is an effective diffusion coefficient whose value is D_p for low injection and $2D_p$ for high injection. The value of δp is found from equations (A3.14) and (A3.15), therefore if $a \ll L$ with the carrier source situated at a distance $x = d$ in the n-type material,

$$\underline{s=0} \quad J = \frac{D_1}{D}.q.G.\exp(-d/L) \qquad \ldots (A3.18)$$

$$\underline{s=\infty} \quad J = \frac{2D_1}{\pi D}.q.G.\frac{h}{L}.K_1(d/L) \qquad \ldots (A3.19)$$

where K_1 is the modified Bessel function of the second kind. For a finite

value of s, the surface recombination velocity,

$$J = \frac{2.D_1}{\pi.D} \cdot q.G.\frac{d}{L}.\left(1 + \frac{hs}{D}\right).\int_{z=0}^{\infty} \frac{\exp\left(-s.\sqrt{\frac{\tau}{D}}.\frac{z}{L}\right).\ K_1\left(\frac{\sqrt{d^2+z^2}}{L}\right)}{\sqrt{d^2+z^2}}.\ dz \qquad \ldots (A3.20)$$

When there is no change of the injection conditions throughout the range of d, these expressions reduce to:

$$\underline{s=0} \quad I_{ph}(d) = I_{sc} \cdot \exp(-d/L) \qquad \ldots (A3.21)$$

$$\underline{s=\sqrt{\frac{D}{\tau}}} \quad I_{ph}(d) = I_{sc} \cdot \frac{\int_{z=0}^{\infty} \exp(-z/L).\frac{K_1\left(\frac{\sqrt{d^2+z^2}}{L}\right)}{\sqrt{d^2+z^2}}.dz}{\int_{z=0}^{\infty} \exp(-z/L).\frac{K_1\left(\frac{z}{L}\right)}{z}.dz} \qquad \ldots (A3.22)$$

$$\underline{s=\infty} \quad I_{ph}(d) \simeq I_{sc} \cdot K_1\left(\frac{d}{L}\right) \qquad \ldots (A3.23)$$

where I_{sc} is the maximum current collected by the reverse biassed pn-junction when the light spot is positioned directly over it (at $x = d = 0$) and I_{ph} is the photocurrent measured when the carrier generation region (i.e. laser spot) is at a distance d away. A computer plot of these three functions is presented in section 4.3.3, figure 18(a).

(e) Lifetime

The method used by Berz and Kuiken to determine the 3-D carrier distribution has also been adopted to predict the time-dependent case when the source of the excess carriers is removed[56], and the steady-state solution outlined above is taken as the initial condition. To simplify the analysis, it has been assumed that $d \gg a$, so the generation volume becomes a point source whose co-ordinates are (d,0,h). Thus from table A2

$$\delta p(r) = \frac{G.\exp(-r/L)}{4\pi Dr} \qquad \ldots (A3.24)$$

for all r, and this can be used in equations (A3.14) and (A3.15) to determine $\delta p(x,y,z)$.

After the generation source is removed, the continuity equation is

$$\frac{\partial \delta p}{\partial t} = D.\nabla^2(\delta p) - \frac{\delta p}{\gamma} \qquad \ldots (A3.25)$$

This can be solved to give the current density as a function of time, so using equation (A3.17):

$$\underline{s=0} \qquad J = 2.\sqrt{\pi}.\frac{d}{L}.\int_{u=t/\gamma}^{\infty} u^{-3/2}.\ \exp\left(-u - \frac{d^2}{4.L^2.u}\right).\ du \qquad \ldots (A3.26)$$

$$\underline{s=\infty} \qquad J \simeq \frac{2.d.h}{L^2}.\int_{u=t/\gamma}^{\infty} u^{-2}.\ \exp\left(-u - \frac{d^2}{4.L^2.u}\right).\ du \qquad \ldots (A3.27)$$

where u is a dummy variable. Again these solutions can be simplified if the range of d is chosen so that the same injection level prevails throughout. Hence,

$$\underline{s=0} \qquad I_{ph}(d,t) = I_{sc}.\frac{\displaystyle\int_{u=t/\gamma}^{\infty} u^{-3/2}.\ \exp\left(-u - \frac{d^2}{4.L^2.u}\right).\ du}{\displaystyle\int_{u=0}^{\infty} u^{-3/2}.\ \exp\left(-u - \frac{d^2}{4.L^2.u}\right).\ du} \qquad \ldots (A3.28)$$

$$\underline{s=\infty} \qquad I_{ph}(d,t) = I_{sc}.\frac{\displaystyle\int_{u=t/\gamma}^{\infty} u^{-2}.\ \exp\left(-u - \frac{d^2}{4.L^2.u}\right).\ du}{\displaystyle\int_{u=0}^{\infty} u^{-2}.\ \exp\left(-u - \frac{d^2}{4.L^2.u}\right).\ du} \qquad \ldots (A3.29)$$

A computer plot of these solutions is given in section 4.4.3, figure 26(a).

APPENDIX 4. COMPUTER SIMULATION OF EXCESS CARRIER DISTRIBUTION

A numerical solution of the continuity equation in two dimensions using a computer has been attempted, in which the finite carrier generation area and long pn-junction at various distances away have been included as boundary conditions. The junction itself has been modelled as a region of infinite recombination velocity, but the semiconductor surface is assumed to have zero surface recombination velocity and act as a carrier mirror; thus the two dimensions used in the simulation are chosen to be in the plane of the surface, and the vertical component of carrier motion is ignored. The current-collecting junction is quite shallow (2-3 μm) so the horizontal carrier diffusion will contribute most to the current flowing across the junction, and the results obtained with the 2-D restriction can be expected to be similar in form to those which would be found if a more rigorous solution was attempted (see section 4.3.3): excessive computer time and storage requirements prevented the use of a full simulation.

The surface of the semiconductor has been modelled as a grid of 2,500 blocks of 2μm square; a diffusion length of 15μm has been assumed, so the total area covered is 100 x 100μm or over six diffusion lengths in each direction. A 4μm square laser 'spot' is positioned in the centre of the grid and a 100μm long, 4μm wide carrier sink, i.e. the junction, was located at a distance d in the x-direction from the generation region (see figure A5). The limits of the grid have been considered to be at infinity, with zero excess carrier concentration, whereas in fact the boundaries are 3.3 x L; however the error introduced from this assumption will be less than 5%.

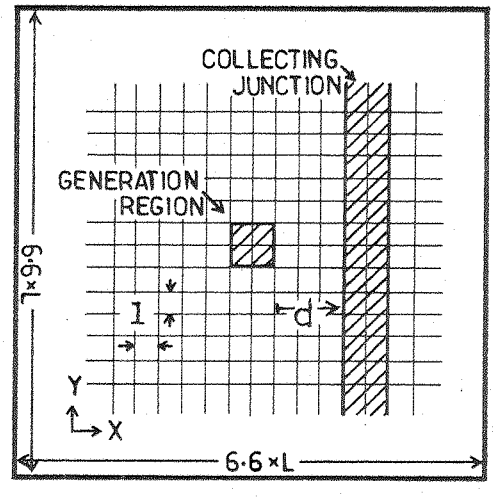


Figure A5: Simulation of the i.c. surface

(a) Steady-state

In the steady-state and with no applied field, the continuity equation for holes in two-dimensions in n-type material is[50]:

$$\frac{\partial^2 \delta p}{\partial x^2} + \frac{\partial^2 \delta p}{\partial y^2} = \frac{\delta p}{L^2} - \frac{g}{D} \qquad \ldots (A4.1)$$

where L is the diffusion length of minority carriers (low level injection conditions will be assumed to hold throughout, so $L \equiv L_p$), δp is the excess hole concentration and g is the generation rate per unit volume. A simple two-level explicit numerical approximation has been used to evaluate the second-order differential, i.e. at the node $x = m$ and $y = n$,

$$\left(\frac{\partial^2 f(x,y)}{\partial x^2}\right)_{m,n} = \frac{1}{l^2} \cdot \left(f(x,y)_{m-1,n} - 2.f(x,y)_{m,n} + f(x,y)_{m+1,n} \right) \qquad \ldots (A4.2)$$

where l is the internodal spacing: $(x)_{m+1} - (x)_m = l$. This algorithm is stable if $1/l^2 \leq \frac{1}{2}$ and the error is of the order $0(l^2)$[118].

The current collected by the junction positioned at $x = d$ is found from:

$$J = \text{Const} \cdot \int_{y=-\infty}^{\infty} \left(\frac{\partial(\delta p)}{\partial x}\right)_{x=d} dy \simeq \text{Const.} \sum_{y=1}^{y=501} \left(\frac{(\delta p)_{d,y} - (\delta p)_{d-1,y}}{l} \right) \qquad \ldots (A4.3)$$

After each iteration using equations (A4.1) and (A4.3), the value of J was inspected to ensure that the method was convergent; the solution was reached when the results of successive applications varied by less than 0.1%. In some cases 500 iterations have proved to be necessary to produce the answer. Suitable values must initially be assigned to each node in order to give rapid convergence of the algorithm, and a simple exponential decay of carrier concentration as a function of diffusion length in all directions from the generation region has proved satisfactory. After one steady-state distribution of carrier concentration has been established, this can be used as the initial condition for the next case, when the junction is moved to a different distance d.

This process has been repeated for values of d in the range of

4-50μm, and three typical results are shown in figure A6 for the values of excess carrier concentration in a 40 x 38 μm region around the central spot, which has been allocated the value of 999. Junction separations of d = 4,10,20μm have been used here, and the position of the junction can be seen where the concentration first reaches zero. The perturbing effect that it has upon the carrier distribution can clearly be seen by comparing the decay on both sides of the central generation region. A plot of the current collected by the junction as determined by equation (A4.3) is shown in figure 18(b), section 4.3.3.

A similar approach was used to simulate the influence of two junctions upon the carrier distribution. A second junction was positioned to the left of the generation region and the current collected by the first was again found as a function of distance d. The resulting steady-state nodal values of carrier concentration can be seen in figure A7, which shows the case for an inter-junction separation of 18μm and distances d of 4μm and 10μm.

(b) Transient case

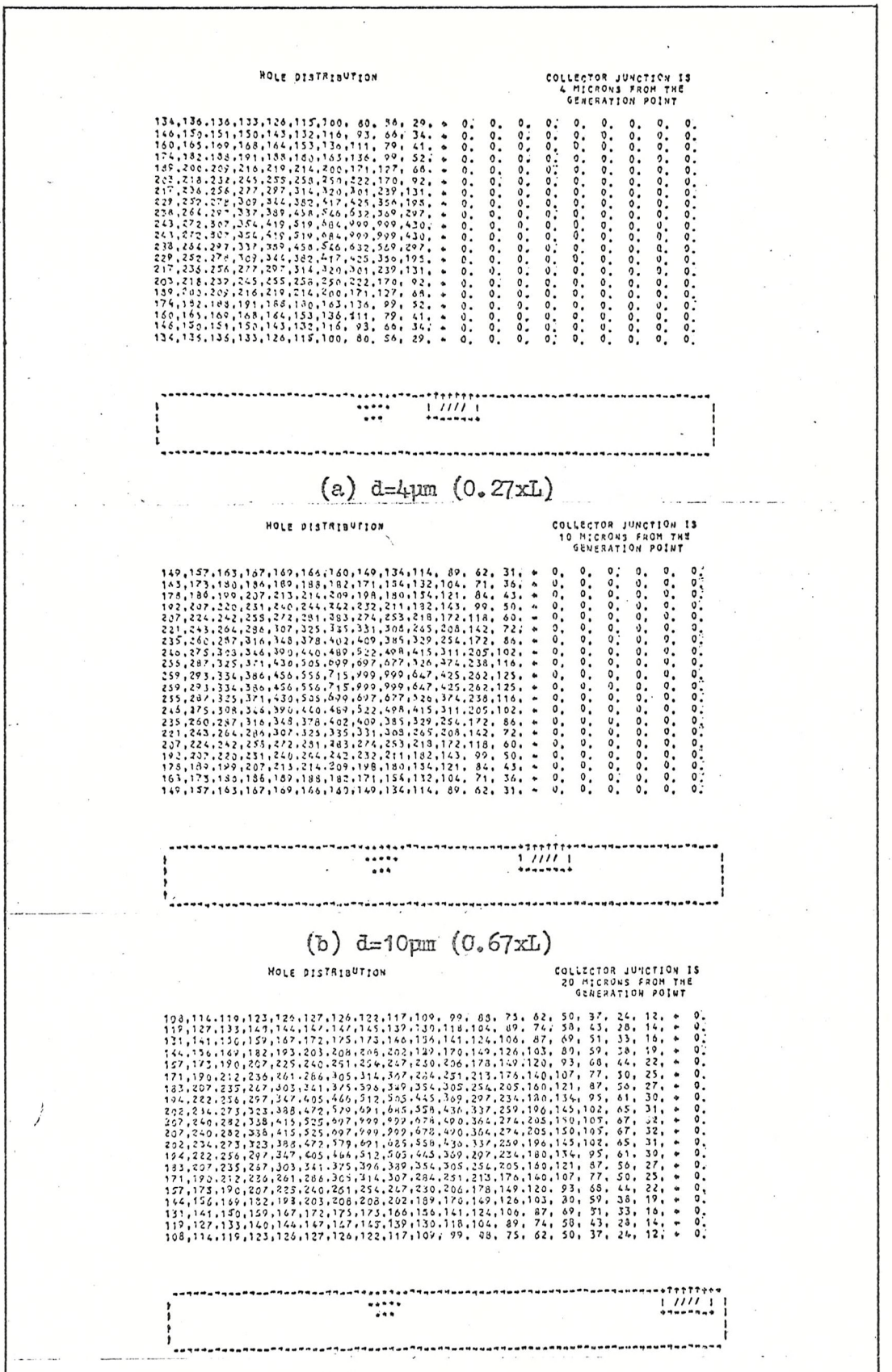
The stability criteria are much more stringent for the time-dependent numerical solution of the continuity equation, and the programme complexity is much increased, with the steady-state determination of the hole concentration described previously only forming the initial condition.

The 2-D field-free continuity equation for holes in n-type material is[50]:

$$\frac{\partial \delta p}{\partial t} = D \cdot \frac{\partial^2 \delta p}{\partial x^2} + D \cdot \frac{\partial^2 \delta p}{\partial y^2} - \frac{\delta p}{\tau} \qquad \ldots (A4.4)$$

where D is the diffusion coefficient and τ is the minority carrier lifetime (see section 4.3). The method used to solve this equation is based on the mid-point/trapezium rule predictor-corrector technique[119]. The open quadrature mid-point rule follows from Taylor's expansion and can be expressed in the form

$$\int_{t_t}^{t_{t+2}} \delta p(x,y,t).dt = 2.t'.\delta p(x,y,t_{t+1}) + \frac{(t')^3}{3}.\delta p''(\xi_t) \qquad \ldots (A4.5)$$



(a) d=4μm (0.27xL)

(b) d=10μm (0.67xL)

(c) d=20μm (1.33xL)

Figure A6: Computer-generated steady-state hole distribution

SINK JUNCTION 14 MICRONS FROM GENERATION POINT

GENERATED HOLE DISTRIBUTION

COLLECTOR JUNCTION IS 4 MICRONS FROM THE GENERATION POINT

0.	*	16,	31,	43,	52,	55,	53,	46,	34,	18,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	20,	38,	52,	63,	68,	66,	58,	43,	23,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	24,	45,	64,	78,	84,	83,	73,	55,	29,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	29,	55,	79,	97,	107,	107,	96,	73,	39,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	35,	68,	97,	122,	138,	142,	130,	101,	55,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	42,	82,	120,	154,	179,	191,	182,	144,	80,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	49,	98,	147,	193,	234,	262,	262,	215,	120,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	57,	115,	175,	238,	303,	362,	391,	336,	186,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	63,	129,	201,	283,	381,	497,	608,	556,	291,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	67,	137,	217,	314,	444,	643,	999,	999,	428,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	67,	137,	217,	314,	444,	643,	999,	999,	428,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	63,	129,	201,	283,	381,	497,	608,	556,	291,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	57,	115,	175,	238,	303,	362,	391,	336,	186,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	49,	98,	147,	193,	234,	262,	262,	215,	120,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	42,	82,	120,	154,	179,	191,	182,	144,	80,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	35,	68,	97,	122,	138,	142,	130,	101,	55,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	29,	55,	79,	97,	107,	107,	96,	73,	39,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	24,	45,	64,	78,	84,	83,	73,	55,	29,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	20,	38,	52,	63,	68,	66,	58,	43,	23,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	*	16,	31,	43,	52,	55,	53,	46,	34,	18,	*	0.	0.	0.	0.	0.	0.	0.	0.	0.

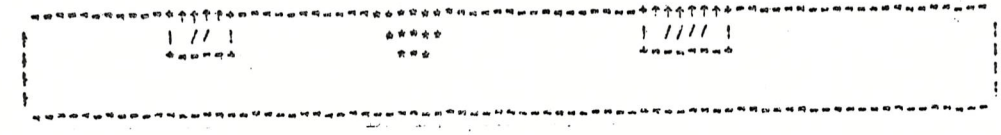
(a) d=4μm (0.27xL)

SINK JUNCTION 8 MICRONS FROM GENERATION POINT

GENERATED HOLE DISTRIBUTION

COLLECTOR JUNCTION IS 10 MICRONS FROM THE GENERATION POINT

0.	0.	0.	0.	*	11,	21,	29,	34,	35,	33,	28,	20,	11,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	16,	29,	40,	47,	49,	46,	39,	28,	15,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	22,	42,	57,	67,	70,	65,	55,	39,	20,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	31,	59,	81,	95,	98,	92,	76,	54,	28,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	44,	83,	115,	135,	140,	129,	106,	74,	38,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	61,	117,	164,	193,	199,	181,	146,	101,	51,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	83,	163,	233,	279,	286,	253,	198,	134,	67,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	111,	222,	329,	409,	417,	353,	264,	173,	85,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	140,	291,	457,	620,	627,	463,	338,	212,	102,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	162,	348,	598,	999,	999,	623,	398,	240,	113,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	162,	348,	598,	999,	999,	623,	398,	240,	113,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	140,	291,	457,	620,	627,	463,	338,	212,	102,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	111,	222,	329,	409,	417,	353,	264,	173,	85,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	83,	163,	233,	279,	286,	253,	198,	134,	67,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	61,	117,	164,	193,	199,	181,	146,	101,	51,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	44,	83,	115,	135,	140,	129,	106,	74,	38,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	31,	59,	81,	95,	98,	92,	76,	54,	28,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	22,	42,	57,	67,	70,	65,	55,	39,	20,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	16,	29,	40,	47,	49,	46,	39,	28,	15,	*	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	*	11,	21,	29,	34,	35,	33,	28,	20,	11,	*	0.	0.	0.	0.	0.	0.



(b) d=10μm (0.67xL)

Figure A7: Hole distribution for two pn-junctions 18μm apart

where $\xi_t \in (t_{t+1}, t_t)$, t' is the time interval between successive evaluations and $\delta p''$ is the second order differential of δp with respect to time. The closed interval trapezium rule in similar format is:

$$\int_{t_t}^{t_{t+1}} \delta p(x,y,t).dt = \frac{t'}{2}.\left(\delta p(x,y,t_{t+1}) + \delta p(x,y,t_t)\right) - \frac{(t')^3}{12}.\delta p''(\xi_t) \quad \ldots (A4.6)$$

The mid-point rule can be used to predict a solution, then an iterative procedure is used with the trapezium rule corrector to reach a more accurate answer, i.e. to find $\delta p(x,y,t_{t+1})$:

$$\text{Predictor: } \overset{(0)}{\delta p}(x,y,t_{t+1}) = \delta p(x,y,t_{t-1}) + 2.\frac{\partial}{\partial t}(\delta p(x,y,t_t))$$

$$\text{Corrector: } \overset{(k+1)}{\delta p}(x,y,t_{t+1}) = \delta p(x,y,t_t) + \quad \ldots (A4.7)$$

$$+ \frac{t'}{2}.\left(\frac{\partial}{\partial t}(\overset{(k)}{\delta p}(x,y,t_{t+1})) + \frac{\partial}{\partial t}(\delta p(x,y,t_t))\right)$$

where $k = 0,1,2$ etc. and $\overset{(k+1)}{\delta p}(x,y,t_{t+1})$ is the $(k+1)$'th estimate of $\delta p(x,y)$ at a time t_{t+1}. The error inherent in this procedure is $O(t'^3)$, but the initial values of $\delta p(x,y,t_{t-1})$ and $\delta p(x,y,t_t)$ must be found before the predictor can be applied. Euler's rule has been used to determine the value of $\delta p(x,y,1)$, with the steady-state solution providing $\delta p(x,y,0)$,

$$\frac{\delta p(x,y,1) - \delta p(x,y,0)}{t'} \simeq \frac{\partial}{\partial t}(\delta p(x,y,0)) \quad \ldots (A4.8)$$

and to improve convergence, a special step has been included between the predictor and first corrector:

$$\overset{(0*)}{\delta p}(x,y,t_{t+1}) = \overset{(0)}{\delta p}(x,y,t_{t+1}) + \frac{4}{5}.\left(\overset{(final)}{\delta p}(x,y,t_t) - \overset{(0)}{\delta p}(x,y,t_t)\right) \quad \ldots (A4.9)$$

A full flow-chart of the computer programme is shown in figure A8.

It has been found that the method is only stable if $t' < 0.0025 \times \Upsilon$, so a very large number of iterations has had to be performed (the total time range is usually chosen to be from 0 to about $2 \times \Upsilon$). The results of the current crossing the junction for three junction-generation area separations (d) of 8,20,40μm are shown in figure 27(a), section 4.4.3.

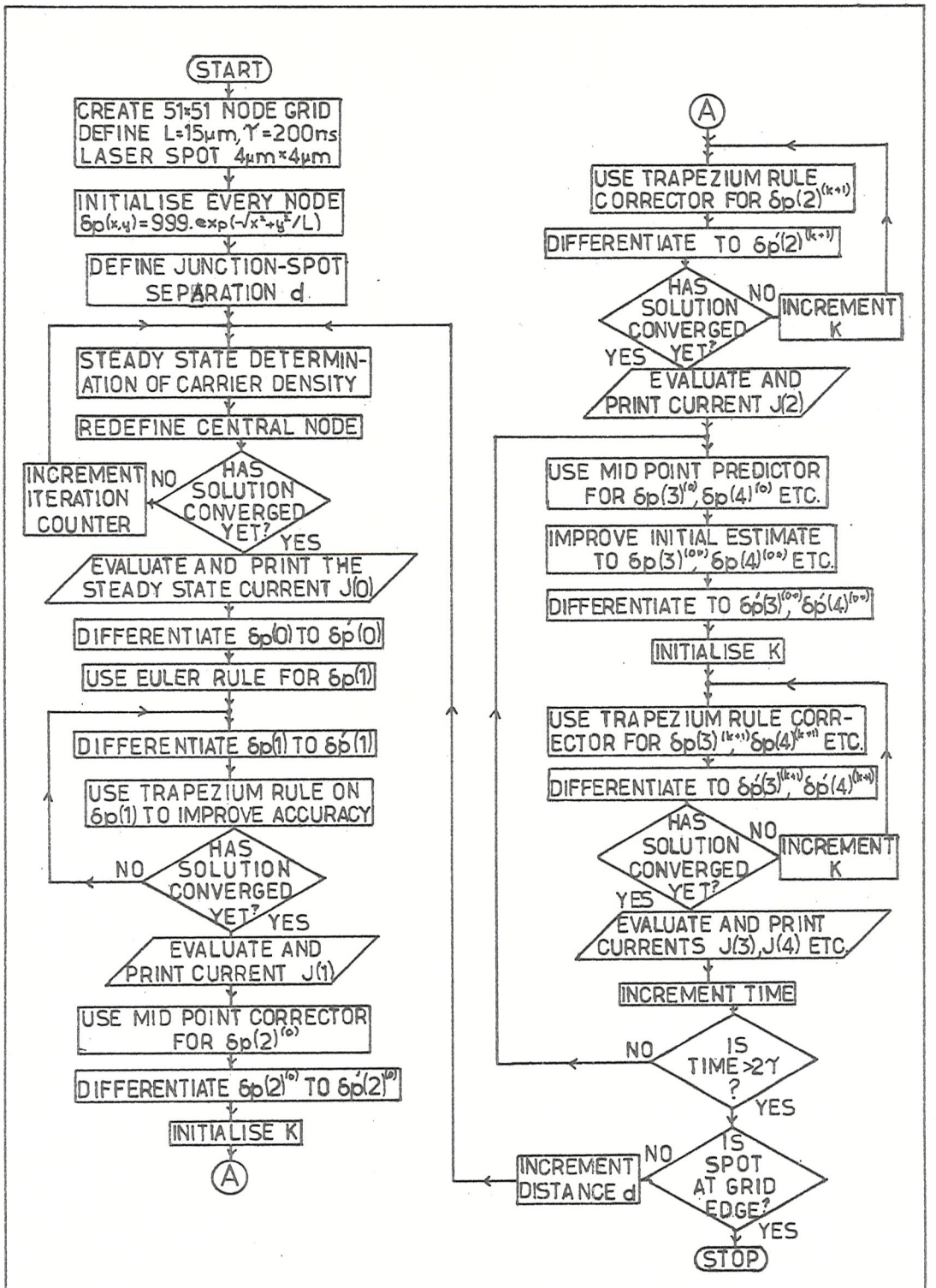


Figure A8: Numerical solution of 2-D continuity equation

APPENDIX 5. NODAL ISOLATION

In one dimension, the excess carrier concentration will be of the form shown in figure A 9 if the generation region is placed at a distance d from junction 1, and $(d_o - d)$ from a second junction, junction 2. In n-type material with a hole diffusion length of L^{50},

$$\delta p(x) = A.\exp(x/L) + B.\exp(-x/L) \qquad \ldots (A5.1)$$

where $\delta p(x)$ is the hole concentration at a distance x from junction 1 and A and B are constants. δp will be zero at the edges of both junctions ($x = 0$ and $x = d_o$) and a maximum of δp_{max} when $x = d$, therefore

$$A + B = 0$$

and $$\delta p_{max} = A.\exp(d/L) + B.\exp(-d/L)$$

$$\therefore A = -B = \frac{\delta p_{max}}{2.\sinh(d/L)} \qquad \ldots (A5.2)$$

The current density crossing junction 1 is

$$J_1 = -q.D.\left(\frac{d\delta p}{dx}\right)_{x=0} = \frac{-q.D}{L}.(A - B) = \frac{-q.D.\delta p_{max}}{L.\sinh(d/L)} \qquad \ldots (A5.3)$$

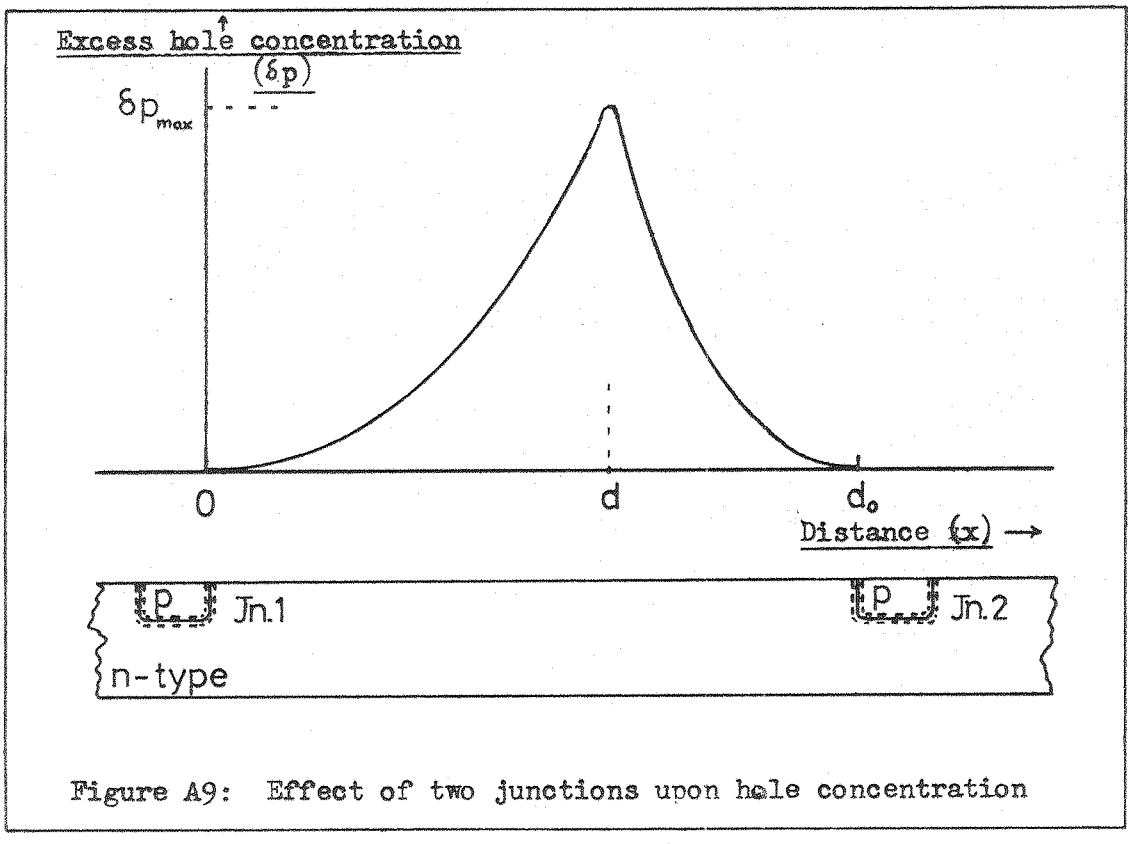


Figure A9: Effect of two junctions upon hole concentration

At the carrier source, the total current density J_g is given by:

$$J_g = -q.D.\left(\frac{d\delta p}{dx}\right)_{x=d} = \frac{-q.D.\delta p_{max}}{L.\tanh\left(\frac{d}{L}\right)} + \frac{-q.D.\delta p_{max}}{L.\tanh\left(\frac{d_o - d}{L}\right)} \quad \ldots (A5.4)$$

so the proportion collected by junction 1 at a distance d away is

$$\frac{J_1}{J_g} = \frac{1}{\sinh\left(\frac{d}{L}\right).\left(\coth\left(\frac{d}{L}\right) + \coth\left(\frac{d_o - d}{L}\right)\right)} \quad \ldots (A5.5)$$

But $\coth\left(\frac{d_o - d}{L}\right) = \frac{\coth(d_o/L).\coth(d/L) - 1}{\coth(d/L) - \coth(d_o/L)}$

and $\cosh^2(d/L) = 1 + \sinh^2(d/L)$

$$\therefore \frac{J_1}{J_g} = \cosh(d/L) - \frac{\sinh(d/L)}{\tanh(d_o/L)} \quad \ldots (A5.6)$$

APPENDIX 6. M.O.S. CIRCUIT ANALYSIS

The output characteristic of a p-channel enhancement-mode M.O.S. transistor is shown in figure A10(a). There are three regions of device operation:-

(i) a cut-off region where the voltage across the gate oxide is always less than the threshold, V_T, and the channel current is zero

(ii) a saturated or pinched-off region where an inversion layer is not formed under part of the gate (resulting in the drain current tending to saturate at a constant value) and

(iii) a non-saturated (triode) region where a well-formed channel exists at all points under the gate.

These three regions can be described in terms of gate and drain voltages V_G and V_D as follows:

(i) Cut-off $\quad |V_G| < |V_T| \quad \ldots$ (A6.1)

(ii) Saturation $\quad |V_T| \leq |V_G| \leq |V_D + V_T| \quad \ldots$ (A6.2)

(iii) Non-saturation $\quad |V_G| > |V_D + V_T| \quad \ldots$ (A6.3)

(a) Steady-state analysis

In a simplified form, the drain current I_{DS} is given by[120]:

(i) Cut-off $\quad I_{DS} = 0 \quad \ldots$ (A6.4)

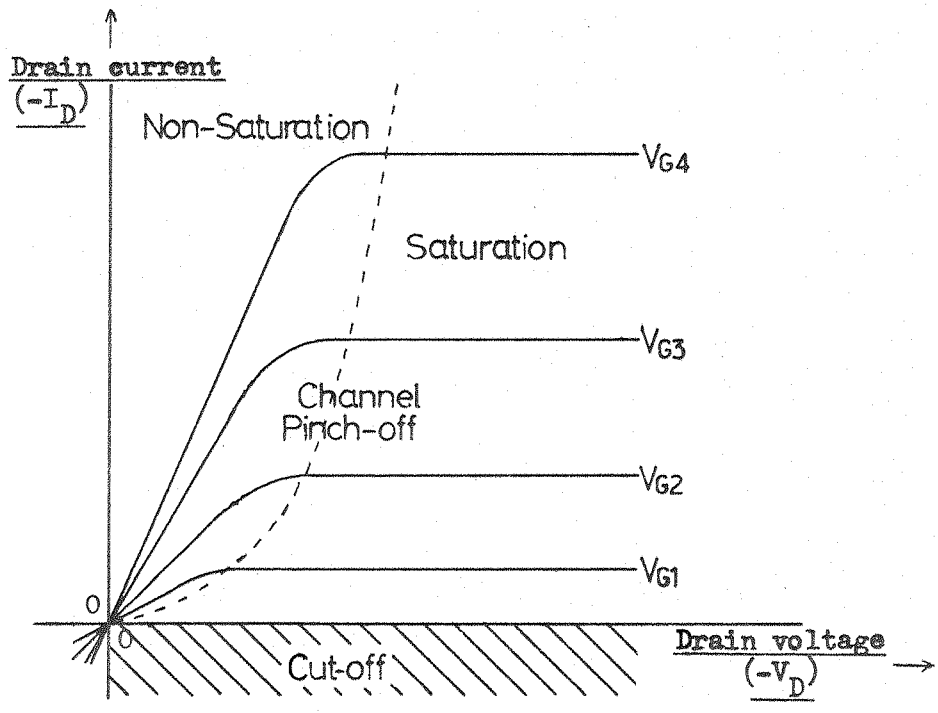
(ii) Saturation $\quad I_{DS} = \frac{1}{2} \cdot \beta' \cdot \frac{w}{l} \cdot (V_G - V_S - V_T)^2 \quad \ldots$ (A6.5)

(iii) Non-saturation $\quad I_{DS} = \beta' \cdot \frac{w}{l} \cdot ((V_G - V_S - V_T).(V_D - V_S) - \frac{1}{2} \cdot (V_D - V_S)^2) \quad \ldots$ (A6.6)

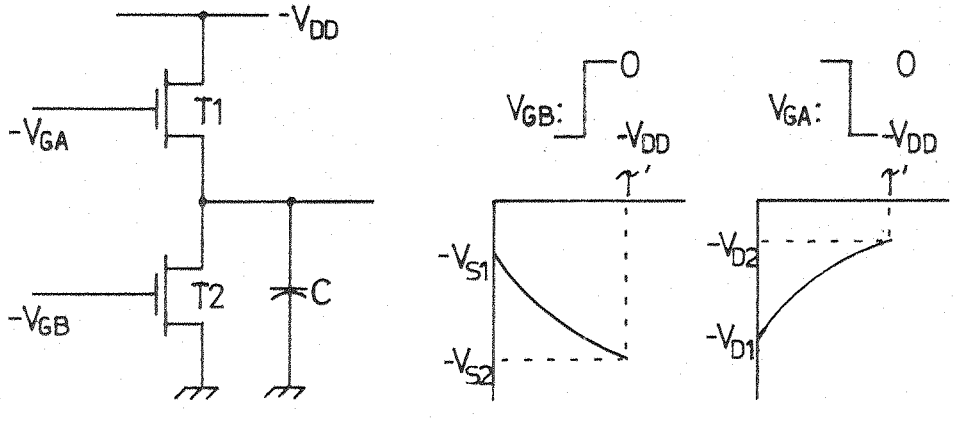
where V_S is the source potential, w is the channel width, l is the channel length and β' is a taken to be a constant whose value is:

$$\beta' = \frac{\mu_p \cdot \varepsilon_{ox}}{t_{ox}} \quad \ldots \text{(A6.7)}$$

with μ_p as the average mobility of the mobile charge, ε_{ox} the oxide



(a) Output characteristic of a M.O.S. transistor



(b) Transient response of a two-transistor circuit

Figure A10: M.O.S. transistor analysis

permittivity and t_{ox} is the gate oxide thickness.

In order to use these equations to evaluate the voltage and current levels associated with a particular circuit, the values of V_T, β' and w/l need to be known for each M.O.S. transistor. The application of this analysis has mainly been used with circuits manufactured by General Instruments, so a discrete transistor (type Q2-2) made by the same firm has been used to experimentally determine the first two of these factors, V_T and β', for devices in which their values were not known previously. The minority carrier diffusion length and quantum efficiency of both the G.I. static shift registers and the Q2-2 was similar in value, so it has been assumed that the other properties will also be the same. Results of $V_T = -2.0v$ for the substrate connected to the source and $\beta' = 8 \pm 1.3 \times 10^{-6} A/v^2$ have been experimentally obtained; the latter is rather higher than the quoted average value of $5 \times 10^{-6} A/v^2$ [121].

In a p-channel M.O.S. integrated circuit, the substrate is at the highest positive potential, so is not usually connected to the source. This means that the substrate will probably be reverse biassed with respect to the source and the gate potential needed to form a channel is increased because of the wider depletion region. The 'body effect' therefore results in a variation of the threshold voltage as a function of source potential V_S, with

$$V_T = V_{TO} + \Delta V_T(V_S) \qquad \ldots (A6.8)$$

where V_T is the effective threshold, V_{TO} is the threshold voltage for the substrate voltage equal to V_S and ΔV_T is the difference between these two terms. The measured relationship between ΔV_T and V_S which has been published by A.M.I.[82] agrees reasonably with the theory presented by Crawford[120] and has been used in all analyses.

(b) Transient Analysis

The transient response of an M.O.S. transistor can also be satisfactorily described by a set of equations. The following relationships have been derived for the case of the two-transistor inverter illustrated in figure A10(b), assuming that a step input is applied to each gate[121]. V_{GA} and V_{GB} are defined in the diagram, and the subscripts

'1' and '2' refer to the initial and final states respectively. τ' is the time taken for the capacitance C to charge from $-V_{S1}$ to $-V_{S2}$ in the case of the step input applied to the top transistor (T1) when T2 is cut-off, and similarly for C to discharge from $-V_{D1}$ to $-V_{D2}$ for the bottom transistor when T1 is cut-off.

T1: Saturated

$$\tau' = \frac{2.C}{\beta'} \cdot \frac{1}{w} \cdot \left(\frac{V_{S2} - V_{S1}}{(V_{GA}-V_T-V_{S1}).(V_{GA}-V_T-V_{S2})} \right) \quad \ldots (A6.9)$$

T2 cut-off

T1: Non-saturated

$$\tau' = \frac{C}{\beta'.(V_T-V_{GA}+V_{DD})} \cdot \frac{1}{w} \cdot \quad \ldots (A6.10)$$

$$\times \log_e \left(\frac{(V_{S2}-V_{DD}).(V_{S1}+2V_T-2V_{GA}+V_{DD})}{(V_{S1}-V_{DD}).(V_{S2}+2V_T-2V_{GA}+V_{DD})} \right)$$

T2: Saturated

$$\tau' = \frac{2.C}{\beta'} \cdot \frac{1}{w} \cdot \left(\frac{(V_{D1} - V_{D2})}{(V_{GB} - V_T)^2} \right) \quad \ldots (A6.11)$$

T1 cut-off

T2: Non-saturated

$$\tau' = \frac{C}{\beta'.(V_{GB}-V_T)} \cdot \frac{1}{w} \cdot \quad \ldots (A6.12)$$

$$\times \log_e \left(\frac{(2.(V_{GB}-V_T) - V_{D2}).(V_{D1})}{(2.(V_{GB}-V_T) - V_{D1}).(V_{D2})} \right)$$

The capacitance, C, can be calculated from a knowledge of the physical transistor layout and processing parameters, but an allowance for the voltage changes (Miller Effect) must also be made. A schematic representation of these factors is shown in figure A11 and numerical values are given in table A3 overleaf[82,121,122]. The effective capacitance under changing voltage conditions can be related to the geometric capacitances which are determined in this way by using the identity:

$$C_e = C_{geom} \cdot \left| \frac{|V_{B2}-V_{A2}| \pm |V_{B1}-V_{A1}|}{|V_{A1} - V_{A2}|} \right| \quad \ldots (A6.13)$$

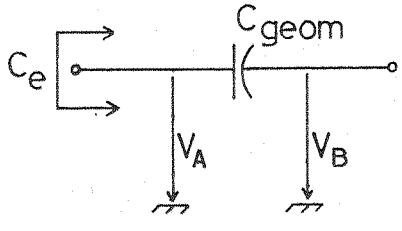
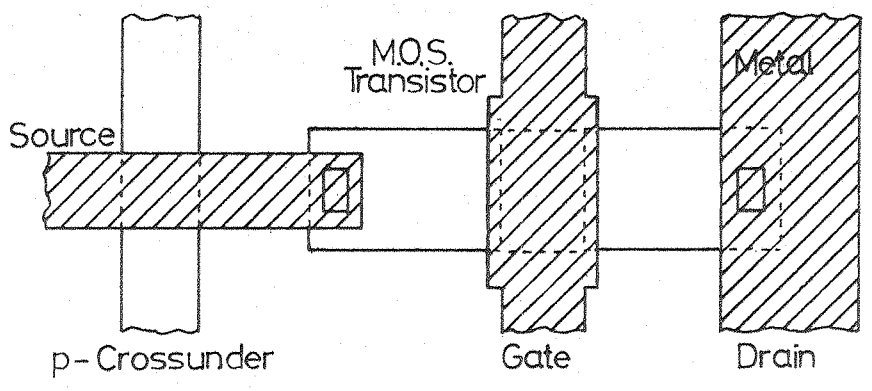
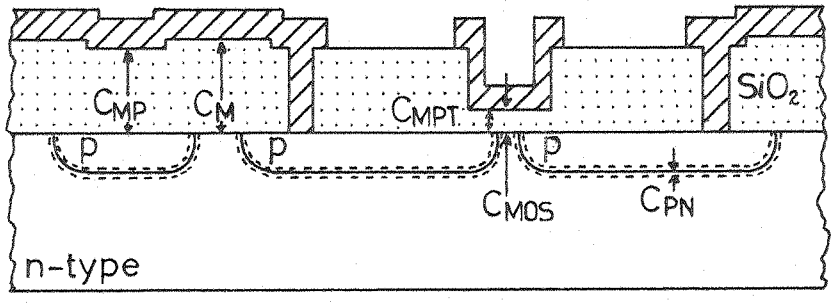


Figure A12: Effective Capacitance

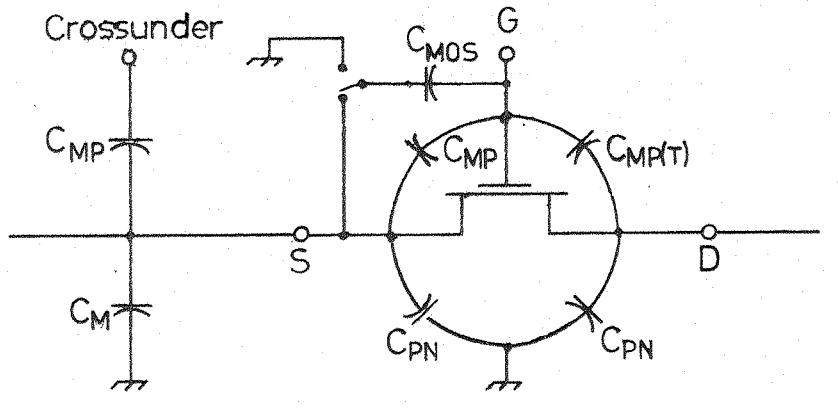
where the subscripts '1' and '2' are again the initial and final states, and V_A and V_B are as defined in figure A12. Therefore from a measurement of the



(a) Layout



(b) Cross-section



(c) Circuit equivalent

Figure A11: Parasitic capacitance

Symbol	Location	Capacitance / unit area ($fF/\mu m^2$)
C_{MOS}	Metal over thin oxide-substrate	0.20
C_{PN}	Junction capacitance p-region-substrate	0v bias 0.16 -10v bias 0.11
C_{M}	Metal over thick oxide-substrate	0.03
C_{MP}	Metal over thick oxide and p	0.05
C_{MPT}	Metal over thin oxide and p	0.30
C_{SP}	Poly-Si over thick oxide and p	0.023
C_{SPT}	Poly-Si over thin oxide and p	0.31

Table A3: Values of parasitic capacitance

dimensions of the integrated circuit transistors, the aspect ratios and the geometrical capacitances can be found; then after a steady-state analysis of the circuit operation has been performed, the effective capacitance can be calculated and the transient analysis completed.

(c) Propagation delay and transistor impedance

The total propagation delay, t_r, can be found from the individual response times t_1, t_2, t_3 etc. of each of the stages in a cascade of transistors or constituent parts of a subdivided network by using the relationship[123]:

$$t_r = \sqrt{t_1^2 + t_2^2 + t_3^2 + \ldots} \qquad \ldots (A6.14)$$

The dynamic ON resistance of an M.O.S. transistor operating in the unsaturated region is, from equation (A6.6),

$$r_{ON} = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{w} \cdot \frac{1}{\beta' \cdot (V_{GS} - V_T - V_{DS})} \qquad \ldots (A6.15)$$

and $$r_0 = \frac{1}{w} \cdot \frac{1}{\beta' \cdot (V_{GS} - V_T)} \qquad \ldots (A6.16)$$

at the origin where the output characteristic is linear.

APPENDIX 7. LASER I.C. TEST EQUIPMENT

In this appendix, brief details of possible component parts which could be used to make up a practical i.c. tester will be given, together with the approximate cost (at Spring 1977, including V.A.T. and 8.9% import duty where applicable). The examples cited are by no means the only ones suitable for this purpose, but they should serve to indicate the equipment which is presently available.

(a) Lasers

A helium-neon c.w. laser has been used throughout this study, and has proved to be very satisfactory from the point of view of laser testing. The cost of these lasers does rise steeply as the power output increases though, so the choice of laser should be made with respect to its intended use; e.g. for testing M.O.S. circuits alone, a 2mW laser would be suitable etc. Examples from the range by Spectra Physics Inc. are given in table A4.

Model No.	145P	142P	120	124B	125A
Power output	0.5mW	2mW	5mW	15mW	50mW
Cost	£125	£400	£930	£2500	£5700

Table A4: HeNe laser cost

If laser powers greater than 50mW are needed, pulsed sources will probably have to be used, and a Nd:YAG laser with a frequency doubler (λ = 5320Å) would be suitable; for example, GTE Sylvania produce lasers of this type with TEM_{oo} powers in the range 250mW - 200W.

Variable frequency lasers can also provide high powers over most of their output wavelengths. The Lexel Model 85 Argon ion laser (£6000) produces more than 25mW in each of the 10900,5287,5145,5017,4965,4880, 4765 and 4579Å lines, and their Model 95 (£8000) gives out more than 100mW over a similar range. Tunable dye lasers, such as the Chromatix CMX-4, cost much more than this but allow wavelength tuning:- with this instrument from 4350Å to 7300Å accompanied by average powers of over 30mW at 30pps.

Semiconductor lasers may soon be reduced in price to about £10, but as yet they are not suitable for use in a laser testing system. The

LBA 185A double heterostructure laser from ITT for example has an output wavelength of 8500Å with a 100 x 1 μm^2 emitting area and 150mW peak radiant power (5% duty cycle); the operating current is 1.5A at room temperature and the 20mW c.w. GaAlAs version from Laser Diode Laboratories also has λ = 8500Å and operates at room temperature.

(b) Optics

The focussing lens needs to be of a good quality, high numerical aperture and have a large working distance and aperture stop. The Ultra-Micro Nikkor step-and-repeat x10 reduction camera lens with working distance of 13.6mm and NA of 0.28 (£800) has proved satisfactory to date, but larger lenses can be obtained, although not usually of such high quality; for example a x2.2 reduction 380mm diameter lens from Tropel, F/3.3 with 289mm working distance which is designed for use in photocopiers could provide a large enough working distance for nearly any probing arrangement.

The expander lens will not need to be of such good quality, but the aperture may need to be large if a multi-beam system is used. Simple glass or Fresnel lenses of focal length greater than about 100mm should be suitable for this task (£5-20). Beam expansion would be necessary to obtain the best performance from acousto-optic deflectors or to produce a 'flood' beam, and a 46mm aperture ready-built system with x5-x20 expansion power from Oriel costs £250. Neutral density filters may be necessary for use in a single beam diagnostic tester, and can be obtained with density values of 0.1 to 4 (transmission 79.5% - 0.01%) at about £25 each, but continuously variable attenuators can cost up to £250.

(c) Modulation, deflection and alignment

The pockel cell and driver system from Electro-optic Developments used in the present study (type PC100 cell with VLA30 driver) gives an optical response time of 150nsec. (cost is £600). Faster modulators such as Coherent Associates' Model 3025 (DC-25MHz, 14nsec. rise and fall times, 500:1 extinction ratio, V_o = 660v, £6000) or model BC-4808 from Laser Precision Corp. (DC-20MHz, rise time <1nsec., 20:1 extinction ratio, V_o = 150v, £2000) are available if required.

Electro-optic deflectors such as the Coherent Associates' Model 10 with only a 0.14° deflection angle (£3000) are not as suitable as acousto-

optic versions for controlling the position of the laser input; one example of an A.O. deflector is the LD-400-XY from Isomet, which has 400 x 400 resolvable spots, deflection angle of 2.9° and transit time of 10.7μsec (£10,000).

Mechanical systems, such as torsion bar and spinning mirror choppers and scanners, may cost up to £400 but the upper frequency limit is only 1-5kHz. Motorized stages such as a xyθ movement control (models ATS302M and ATS301MR from Aerotech Inc. have 50mm range, 2.5μm accuracy, 1.5μm repeatability, 0.25μm resolution and 360° rotation with 3arcmin. accuracy, 0.2arcmin. repeatability and 0.25arcmin. resolution, all with a slew speed of 2000 steps/sec) will cost about £1500. Galvanometer-controlled beam deflection may also be possible, and a system similar to the one employed in the Teradyne W311 Dynamic Laser Adjust System[124] for beam control in laser trimming may be adapted for this purpose.

(d) Conventional i.c. testers

The cost of i.c. testers varies in accordance with the range of tests which can be performed[5]. Comparison testers, often programmed by plug-in cards, can cost up to £10,000, but to generate test data, provide dynamic testing, make accurate parametric tests etc., a computerized system is needed. The price then rises to above £50,000 and can even be as high as £300,000 for a really comprehensive tester which can perform functional, parametric and clock rate testing on a variety of types of integrated circuit; it is this kind of ATE which is envisaged for use with the laser test method. Some of the manufacturers in this field are Datatron, Fairchild, LSI Testing, Macrodata, Teradyne and Xintel.

The following published paper was included in the bound thesis. This has not been digitised due to copyright restrictions, but its doi is provided.

Smith, J.G. & Oldham, H.E., 1977. Laser testing of integrated circuits. IEEE Journal of Solid-State Circuits, 12(3), pp.247–252. Available at: http://dx.doi.org/10.1109/jssc.1977.1050886.