UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND APPLIED SCIENCE

ELECTRONICS

TRANSMISSION STUDIES RELATED TO SERIAL DATA HIGHWAYS

by

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Thesis submitted for the Degree of Doctor of Philosophy

- January 1980 -

To Mum, Dad, Merry and Christiana.

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

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This thesis is a comprehensive investigation of the transmission performance of both baseband and modulated carrier serial data highway systems. In particular the effects of the terminal loads on the system performance and the relative comparison of the two systems is considered.

Results of investigations of the properties and performance of the two bit-related baseband codes used for the highway signalling are presented.

Experimental tests carried out to identify the effects of loading on a baseband system are described. Two simple theories which attempt to predict the cumulative attenuation, and the overall frequency response of the loaded line are presented.

A model for computer simulation of the baseband system, which was developed to study the responses under various loading conditions is described. The results of investigations using this model are presented.

Tests carried out to verify the performance of an experimental modulated carrier system are reported. Design of the experimental system which uses a narrowband modulation technique is presented in detail. Procedures for the design of the coupling network required to meet specific highway loading conditions are outlined.

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LIST OF SYMBOLS

A = signal attenuation

A_c = tap coupling loss

A_I = tap insertion loss

A_L = transmission line loss

A_M = mismatch loss

A_R = tap return loss

A_T = total transmission loss

A_U = peak voltage of received signal

B_c = channel bandwidth

C = capacitance per unit length of line

C_L = load capacitance

C_s = number of basic time steps within input signal period

d_n = distance between loads

E = signal energy per bit

f_1 = 'mark' frequency

f_2 = 'space' frequency

f_b = data bit rate

f_c = carrier frequency

f_H = high cut-off frequency of transformer loads

f_L = low cut-off frequency of transformer loads

f_o = filter cut-off frequency

f_R = reference frequency (translation oscillator frequency)

f_s = sub-carrier frequency

g = conductance of elementary section of line

G = conductance per unit length of line

G_o = receiver amplifier power gain

G_v = voltage gain of noise amplifier

$i_{n,m}(k)$ = transmission line current variable at discrete time intervals (T_s)

$i(x,t)$ = current at point x along line at time t

$I(k)$ = input current samples at discrete time intervals (T_s)

K_s = total number of basic time steps for computation

l = transmission line length

L_K = transformer primary referred leakage inductance

L_p = transformer primary self inductance

m = message length

n	= coupling transformer tap ratio
N	= number of loads
N_0	= noise power spectral density
P_c	= carrier power
P_e	= data error probability
P_{ec}	= code error probability
P_{es}	= element error probability
P_{eu}	= undetectable error probability
P_m	= message error probability
P_{mue}	= message undetectable error probability
P_n	= noise power
P_{OB}	= out-of-band power
R	= resistance per unit length of line
r	= resistance of elementary section of line
R_2	= equivalent characteristics impedance of load capacitance
R_3	= equivalent characteristic impedance of load inductance
r_c	= load reflection coefficient
r_o	= resistive load transmission coefficient
R_L	= load resistance
R_o	= line characteristic impedance
R_s	= generator source resistance
$S(f)$	= power spectral density
S_n	= number of basic time steps within line section n.
S/N	= signal-to-noise power ratio
T	= data bit period
t_d	= duration of input current waveform
T_d	= delay of unit length of line
T_o	= transmission coefficient of load
T_s	= time delay of elementary section of line = basic time step for numerical computation
V	= pulse signal amplitude
$v_{n,m}(k)$	= transmission line voltage variable at discrete time intervals (T_s).
V_T	= r. m. s. sending end signal voltage
$v(x, t)$	= voltage at point x along line at time t.
Z_p	= H. F. tap load impedance

α = a positive real factor ≤ 1

β_1, β_2 = relative i. s. i. factors

β_c = coupling loss voltage ratio

β_i = insertion loss voltage ratio

β_r = return loss voltage ratio

γ = propagation constant of line

Δf = frequency deviation

ρ = filter output peak-signal-to-noise power ratio

σ = r. m. s. noise voltage

τ_c = capacitive time constant $(R_o C_L)$

τ_L = inductive time constant (L_L / R_o)

1. INTRODUCTION

1.1 Background

1.1.1 General

The work described in this thesis has been directed towards the design of a proposed local data communication network in a distributed computer system, suitable for shipborne applications.

The proposed network is to be implemented as a polled multidrop data highway with serial transmission over a single wire cable at Mb/s rates of relatively short messages (up to 256 bits) in a broadcast mode to all processor elements. Each processor is connected to the highway via a microprocessor controlled interface unit which also contains circuits for signal transmission/reception, modulation/coding, demodulation/decoding, and clock synchronisation in addition to providing the software functions of message formatting, message filtering, buffer storage and error detection. These interface units are hereafter referred to as "terminals".

The protocols and control procedures, and some aspects of the signal transmission design of the proposed serial highway had been considered in the preliminary studies reported in (1) - (4). In the author's studies effort has been concentrated on the transmission performance of both a baseband coded system and a modulation carrier system ; in particular the effects of loading the baseband highway with a large number of terminals and a comparative evaluation of the modulated carrier system. Both systems are based on a passive highway configuration i.e. there is no amplification or regeneration of the line signal at terminals.

1.1.2 Baseband Serial Highway Loading Problem

The main transmission problems associated with the passive ring configuration and which affect its performance are twofold :

(i) There is the inherent transmission line distortion appropriate to the total line length involved,

(ii) Connection of the intermediate terminals onto the line cause impedance discontinuities in the line which result in multiple reflections and cumulative transmission losses.

For reliable operation of the passive highway it is highly desirable that the above effects be taken into account in the overall system design. This requires both a qualitative understanding and a quantitative analysis of the problem.

The primary cause of the line loss is known to be skin-effect ; and the quantitative analysis of its effect on the transmission performance is well established in the relevant literature (5), (6).

An attempt to quantify and predict the mismatch loss caused by the connection of a number of loads onto the passive ring was first made by CCL (2) in the preliminary studies on the proposed highway. The assumption of purely resistive loads however limits the application of this theory to simple terminals loads which may be treated as purely resistive. Unfortunately such is not always the case in practice.

The proliferation of microcomputers in recent years and the potential benefits such as increased flexibility and improved reliability through dynamic allocation of resources, have stimulated a growing interest in distributed systems (7)-(9). This growing interest has, however, not been matched by the availability of adequate information pertaining to the associated transmission design problems.

In the most recent published material, which has a direct relevance to the present investigation (10), some indication is given about the limitations imposed by the terminal loadings on the transmission performance of a similar passive serial highway. However, as in other publications, much of the detailed design

and performance evaluation of the system is concentrated on the protocol and control procedures.

The lack of specific information on the transmission design, as discussed above, is a general deficiency in this growing area of distributed computer systems. Would-be designers with very little experience are thus confronted with this problem of the lack of adequate information.

1.1.3 Modulated Carrier Highway Systems

The modulated carrier serial highway system provides an alternative to the baseband system. The current practice in modulated carrier distributed computer system design has generally been the use of FDM techniques to increase the number of terminals and directional couplers for bussing onto the highway (11). However, considering the proposed passive highway situation, the above techniques suffer two main drawbacks :

(i) it does not provide positive message control,
(ii) it cannot typically operate in a broadcast mode.

A direct consequence of the above drawbacks is that high speed data transfer between terminals, which is a basic requirement of the proposed serial highway system, cannot be readily effected.

For the full realisation of the advantages of modulated carrier systems in the proposed highway, an alternative technique to the above is thus desired.

1.2 An Account of the Present Investigation

1.2.1 Scheme of Studies

Problems of connecting a large number of terminals onto the baseband serial highway and the need to evaluate the performance of

an equivalent modulated carrier system as a possible alternative to the baseband system as outlined above have stimulated the present work, which was conducted basically in three stages. The first stage was an investigation in depth of the properties and experimental performance of the baseband signalling code used. The second stage dealt with a searching study of the baseband loading problem on both an experimental and computer simulation models of the passive serial highway. The third stage was the design and performance evaluation of a modulated carrier passive serial highway system. A more detailed outline of this work is given in the sub-sections which follow.

1.2.2 The Properties and Performance of the Baseband Signalling Codes

An essential factor affecting the performance of any data transmission system is the line signalling code used. Two bit-related biphase and bifrequency codes have been considered as possible candidates for the proposed highway system in the initial studies. The basic properties of these codes are known, However, it became necessary to conduct further investigations to assess the relative performances of the two codes for the intended high speed transmission applications.

The procedures adopted and the results of these investigations are described in detail in Chapter 2. New findings on less well known theoretical and experimental performance of these codes are reported.

1.2.3 The Loading of Baseband Passive Serial Highways

The transmission line and the coupling circuit suggested for use in the proposed highway system during the initial studies were a balanced screened twisted pair and transformer coupling respectively. The desirable features of the balanced screened line in the proposed environment is that it provides an adequate measure of protection against interfering electromagnetic fields.

As well as being suitable for AC coupling on to the balanced line, a transformer can provide a substantial degree of electrical isolation in addition to common mode rejection which gives further protection against interfering noise signals on the line.

The above type of cable and the method of coupling are used in the experimental investigations carried out to identify the effect of loading the serial data highway with a large number of simulated terminals. The results of these tests is reported in Chapter 3.

Two computer simulation models of the highway used for further investigations into the effects of loading the passive ring, are completely described. The essential feature of both of the models is that they are not restricted to the analysis of any one particular method of coupling. One of the models provides the capability of the exact prediction of the transmitted signal waveform at any terminal along the highway under various loading conditions. The results of detailed analysis of the effects of the terminal loadings on the transmitted signal and the overall transmission performance of the highway is reported in Chapter 4.

1.2.4 Design and Performance Evaluation of the Modulated Carrier Serial Highway System

The main potential advantage of using modulated carrier signals with a relatively high carrier frequency (in V. H. F. band) are that the line signal spectrum can be placed outside the bands containing interference and where the shielding efficiency of coaxial cable is high enough to enable advantage to be taken of its inherently lower losses and in addition, the narrow fractional bandwidth implies that line losses will cause signal attenuation rather than distortion. It also opens up the possibility of increasing the data rate by using FDM techniques.

An essential factor considered in the design of the modulated carrier system which is described in Chapter 5 has been simplicity and the use of cost-effective alternative approaches to the design problems faced ; with the view to offset the cost disadvantage when a large number of such units are used.

The design of the coupling of the transmitter and receiver terminals to the highway has been based on the need for a broadcast mode of operation as well as the possible use of FDM. The coupling techniques used in this realisation is described. In particular, the design of the receiver coupling network, implemented as a broadband high impedance tap, is presented in detail.

Experimental performance evaluation of the demodulators, and loading tests to assess the suitability of the system for passive serial highway applications is outlined. The transmission medium used is a low loss coaxial cable.

2. BASEBAND DESIGN STUDIES

2.1 Introduction

In baseband digital line transmission it is highly desirable that the transmitted signal has the following properties :

(a) sufficient timing information which can be recovered at the end of the transmission section,

(b) negligible energy at or near DC in the power spectrum of a random sequence, so as to enable AC coupling of line to terminal units.

To satisfy the above transmission requirements some form of line coding is adopted. This code can be defined as an encoding procedure which converts a data sequence into another sequence satisfying the previous two requirements for baseband transmission.

In addition to the above properties, other essential features desired of such a code are :

(c) in-service error monitoring capability ; in other words, it must possess some built-in features that enable errors to be detected and monitored during system operation,

(d) narrow spectral bandwidth so as to minimise noise and intersymbol interference effects,

(e) sufficient simplicity for practical implementation.

In the preliminary studies on the data highway (1), two bilevel codes which have met the above properties together with other desirable features were suggested. These are defined as Phase Modulation (PM) and Frequency Modulation (FM) codes respectively ; these codes are also known by the names of

Biphase or Manchester code and Harvard code respectively.

The following sections of this chapter report on results of theoretical and experimental studies carried out to investigate further the properties and performance of the PM and FM codes(14). Error detection by code violation testing is examined and a simple theoretical treatment of the effectiveness of this technique is presented. Transmission line distortion effects on the coded data is given consideration by comparison of the error rate performance with typical received signal eye diagrams. The use of receiver input filtering to improve the signal-to-noise performance is considered and it is shown that in practice a filter bandwidth equal to the data bit rate can be used.

2.2 Theory of PM and FM Coding

2.2.1 Waveforms

PM Coded Data

This modulation scheme uses two complementary phases to represent the two states in the binary data to be transmitted. The two basic elements are shown in Figure 2.1(a) and the resulting line signal for an arbitrary data sequence is shown in Figure 2.2 (a).

It is seen that there is always a signal transition in the middle of each bit period and an additional transition at the beginning when the next symbol has the same state as the previous bit. The inherent large number of transitions provide the desired timing information for the decoding process.

FM Coded Data

The two binary states are represented by the presence or absence of a mid-bit transition respectively, as shown in Figure 2.1(b). Corresponding line signal for the same arbitrary data

sequence as PM is also shown in Figure 2.2(b).

In this case however, regular transitions occur at the beginning of each bit period and the additional transitions, subject to the same data condition for PM, occur in the middle of a bit period.

As for the FM case, the advantage of the large number of transitions in the waveform is evident.

Polarity Reversal Advantage

The FM waveforms of Figure 2.2(b) show that a mundane, but certainly not trivial advantage of this code is that the polarity of a coded waveform can be reversed without affecting the decoding process. This is an important advantage over PM coding especially as a balanced pair line, where it is often difficult to ensure correct polarity of all line connections, has been chosen as the medium of transmission for the proposed highway.

2.2.2 Spectra

The spectral density function for both codes, assuming equal a priori probabilities of ones and zeros in the original data (random) sequence, is the same in general when this condition is satisfied. Using the techniques described in Chapter 19 of (12), the two sided power spectral density can be shown to be :

$$S(f) = V^2 T \frac{\mathrm{Sin}^4(\pi f T/2)}{(\pi f T/2)^2} \qquad (2.1)$$

where V is the amplitude and T the data bit period.

A plot of the normalised function of Equation 2.1 is shown in Figure 2.3. The spectrum has low energy at low frequencies and no energy at zero frequency (DC) which satisfies the requirement for AC coupling to the highway.

Most of the power is concentrated in the band O.1 f_b to 1.6 f_b, where f_b is the bit rate. It has been found however that in practice (as will be explained in section 2.3) the transmission bandwidth can be much less than this.

2.2.3 Error Probabilities

Three types of bit errors can be defined with PM and FM codes. These are respectively given as :

(a) Data Errors
(b) Code Errors
and (c) Undetectable Errors.

Basically, data is detected by strobing the code elements and comparing the resultant states. Details of the decoding principles are described in section 2.3.1.

Data Error Probabilities

Data errors are caused by invalidation of the rules defined for data states '1' and '0' within a bit period. For FM, data bit error arises when either, but not both half-bit elements within a bit period are in error. But for PM, a data bit error occurs when only one $\frac{1}{2}$ bit element is in error. From the results of theoretical analysis given in Appendix A.1, the data bit error probability for PM and FM coded signals, assuming equal a priori probabilities of zeros and ones, is respectively given as :

$$P_e(PM) = \tfrac{1}{2}\left[1 - \operatorname{erf}\sqrt{\tfrac{1}{2}\,S/N}\right] \qquad (2.2)$$

and

$$P_e(FM) = 1 - \operatorname{erf}\sqrt{\tfrac{1}{2}\,S/N} \qquad (2.3)$$

Equations 2.2 and 2.3 show that, theoretically, data bit error rate for FM is twice that for PM.

Code Error Probabilities

The waveforms for both PM and FM codes show that regular transitions occur in the middle of each bit period for PM and at the beginning of each bit period in the case of FM. Violation of this coding rule in either case, which results in the absence of the expected regular transition, gives rise to what is termed a code error.

The probability of code error found in Appendix A.2 for both codes is given by :

$$P_{ec}(PM) = 2\,P_e\,(1 - P_e) \qquad (2.4)$$

and

$$P_{ec}(FM) = P_e \qquad (2.5)$$

where P_e is the respective data bit errors given by Equations 2.2 and 2.3. Equations 2.4 and 2.5 show that code error probability is twice the data bit error probability for PM and the same for FM ; i.e. it is the same for both codes. Thus if code error detection is being exploited PM loses its advantage of lower error probability.

Undetectable Error Probabilities

Undetectable errors are caused by element errors which give rise to data errors but not detected by code violation tests. It arises where the signal states are inverted in a pair (or pairs) of $\frac{1}{2}$ bits on either side of a regular transition since this results in apparently legal code characters at the decoder output.

For PM this error condition involves a single data bit but in FM coding a pair of consecutive data bits are involved, in which the two $\frac{1}{2}$ bit elements either side of the bit boundary are in error and the other two elements correct. Such a condition also results in two data bit errors. Thus for FM in particular, prediction of

undetectable errors on a single bit basis would be invalid. This problem is overcome by considering data messages and from the results obtained, the single bit undetectable error is extrapolated.

The theoretical analysis given in Appendix A. 3 show that the bit undetectable error for both PM and FM are respectively given by :

$$P_{eu}(PM) = P_e^2 \qquad (2.6)$$

$$P_{eu}(FM) = \frac{P_e^2}{2} \qquad (2.7)$$

where P_e is the respective data bit error probabilities given by Equations 2. 2 and 2. 3.

The corresponding message error probability (P_{mue}), from the results of theoretical analysis given in Appendix A. 4 become,

$$P_{mue}(PM) \simeq mP_e^2 \qquad (2.8)$$

$$P_{mue}(FM) \simeq m\,\frac{P_e^2}{2} \qquad (2.9)$$

Thus the slope of the graph of P_{mue} against m should give the respective bit undetectable error probability.

Experimental undetectable message error rate tests carried out to verify the above results are described in Section 2. 3. 3.

2. 3 Performance of PM and FM Coding

2. 3. 1 Detection and Decoding Techniques

Clock Extraction

Two fundamental methods of clock extraction from PM and FM coded signals, termed synchronous and asynchronous extraction are used. The former uses some form of phase locked

loop, whereas the latter is based on monostable timing elements.

Synchronous Method

The form of circuit schematic for this method of clock extraction is shown in Figure 2.4 (a). The PLL runs at twice the bit frequency (f_b) so that all edges are utilised for timing correction and so that the synchronisation time can be made as short as possible. A divide-by-two circuit at the output of the PLL provides the required extracted data bit clock. The frequency division however results in ambiguity of the output clock phase and selection of the correct phase is achieved by the Phase Select Logic shown.

Asynchronous Method

This form of clock extraction is shown in Figure 2.4(b). The regularly spaced pulses from the edge detector are selected by the circuit comprising the monostable and logic gate, thus eliminating the irregular half-bit transitions from the coded signal. This method of clock extraction however does not reduce jitter and it does not provide clock continuity in very noisy or loss of signal conditions but it is a simple circuit and it is easy to synchronise.

Decoding

Decoding of the PM and FM coded signals is done by the use of two methods namely, strobe and edge detection. The principles applied in both cases is explained below. Details of the circuits used are given in Appendix B.

Strobe Detection Decoder

In this type of decoder the coded signals are strobed at $\frac{1}{4}$ and $\frac{3}{4}$ bit positions and the resultant states compared. See Figure 2.5. For PM only one element sample is required to decode the signals, but for FM signals both element samples are necessary for the

differential comparison involved. This method of decoding is used with either type of clock extraction described above.

Edge Detection Decoder

This type of decoder incorporates an asynchronous clock extractor which detects all the signal state transitions. For PM coding, the decoded data is determined by the direction of the regular mid-bit transitions in the input signal but for FM coding, the presence and absence of the mid-bit edges is detected which indicates a zero or a one respectively.

2.3.2 Bit Error Rate Tests

The results of bit error rate tests are summarised in this section. The clock extraction and decoding techniques discussed above were used together with the screened twin axial cable in a point-to-point link operation for the tests.

Measurement System

Figure 2.6 shows a block diagram of the experimental set up. Noise is coupled into the line (close to the receiver) via a linear long-tailed pair amplifier which acts as a high impedance source of either differential or common-mode signals. Input data for the transmitter is generated using a Hewlett Packard data generator type 8006A. All tests are carried out with the generator in pseudo-random mode with register length of 15 which provides a sequence of length 32,767 bits.

Decoded data from the receiver is compared bit by bit with the transmitter input data sequence, suitably delayed in the bit error rate testing unit (BERT). The bit error rate is measured in these tests by feeding the RZ error output into the 'B' channel of a Hewlett Packard Counter/Timer type 5326A set to display

'frequency' and using the main clock as an external time-base. Used in this way, the reading in MHz divided by 10 gives the error rate normalised to the bit rate, i.e. the error probability. The main bit rate clock (CK) is supplied to the whole system by the BERT unit.

Details of Transmitter, Noise Generator and Amplifier, and BERT units are given in Appendices C, D and E respectively. The two types of Receivers used for the tests and based on the clock extraction and decoding principles of section 2.3.1 are given in Appendix B.

Test Procedures

For all the tests, the general procedure followed was to set up the clock frequency to a specific value, adjust the clock extraction monostables as appropriate (see Appendix B) and then for each cable length selected, set up the data delay and error strobe delay. Noise was applied differentially in all cases. The definition of the S/N ratio used was given as :

$$S/N = \frac{\text{signal power at the transmitter end}}{\text{noise power injected at the receiver end}}$$

Using the method described in Appendix F, the noise generator output voltage was set such that the S/N ratio was directly given by the attenuator setting.

Error rate measurements were made by selecting S/N ratios in appropriate steps and reading off the corresponding error probabilities on the HP counter.

Test Results

The experimental results are presented as graphs of $\log_{10} P_e$ against S/N in dB, where P_e is the measured bit error probability.

Comparison of Theoretical and Experimental Error Rates

In order to closely simulate the theoretical conditions required for comparison, the tests were carried out with a clock (ideal) from the transmitter, fed into the 'Ext CK' input of the strobe decoder. A very short length of cable was also connected between transmitter and receiver.

Figure 2.7 shows a plot of log P_e against S/N for both PM and FM codes. The experimental results are shown by the broken lines. It is seen that at lower S/N values there is good agreement between theoretical and experimental results, which confirms the factor 2 advantage in error rate for PM coding. At higher values of S/N, deviation between theoretical and experimental curves increases, giving about 1 dB difference in S/N at P_e of about 10^{-6}.

The theoretical analysis assumes a perfect gaussian noise p.d.f. However this ideal p.d.f. is difficult to achieve in practice and the noise generator used is no exception in this case, which explains the deviation between the two sets of curves.

Synchronous and Asynchronous Clock Extraction

Figure 2.8 shows graph of experimental results for FM coding at a bit frequency of 1 Mb/s, using strobe detection decoder. Details of the PLL circuits used is given in Appendix G.

The results show that 2nd order PLL gives virtually the same error rate as ideal clock and that the asynchronous clock extraction is only about 1 dB worse in S/N. Performance of the 1st order PLL is rather worse with S/N degradation of the order of 3 dB.

The apparent poor performance of the 1st order PLL is attributed to jitter effects since no loop filter was present in this case. This S/N degradation was however offset by the much faster

synchronisation time of 2 - 3 bits compared with 4 - 10 bits obtained for the 2nd order PLL, which had a loop filter. This result shows that if PLL clock extraction is used then faster synchronising time can be obtained only at the expense of some degradation in S/N.

Figure 2.9 shows similar set of curves for PM coding but excluding 1st order PLL. Again, the 2nd order PLL gives closer performance to the ideal clock. At high S/N the asynchronous clock degradation is only 0.5 dB compared with 1 dB for FM.

Generally performance of the asynchronous clock has been much better than expected since there is no jitter reduction with this method of clock extraction. However this comparative result is for a relatively short length of cable. For longer cable lengths and higher data rates it was noted that performance deteriorated considerably - the direct result of increased signal jitter. This method of clock extraction, together with its overall simplicity would therefore be suitable for use where the cable runs are short and data rates are relatively low ; in effect it is suitable for low distortion transmission systems.

On the other hand using the PLL clock the advantage of performance reliability and lower S/N in high jitter environment, such as a loaded highway system, far outweighs the problems of extra complexity and time to acquire synchronisation. The PLL clock is therefore recommended as the method of clock extraction.

Strobe and Edge Detection Decoders

Results of tests making a direct comparison of edge and strobe detection decoders with zero and 100m cable lengths and 1 Mb/s bit rate are shown in Figure 2.10 for PM and FM respectively. The curves show that there is only slight improvement in the performance of a strobe detection decoder over an edge detection

decoder for both PM and FM. This improvement however appears to be marginally greater for PM data than for FM. Compared with results of previous tests using strobe detection decoder, the above results also show an interesting difference between the two decoders ; the theoretical deduction that PM coded data gives lower error rates than FM data is not borne out in the case of edge detection decoder. In fact FM performs slightly better than PM.

In the case of strobe detection, decoded data is determined by the level of the incoming signal at the strobing points whereas for edge detection, the decoding is dependent on the positions of the transitions in the received coded signal. It is thus evident that the theoretical analysis for strobe detection (Appendix A), based on signal levels, does not apply in the case of edge detection decoder.

However, a practical explanation is that the poorer performance of edge detection decoder with PM may be due to the asynchronous clock extraction loop dropping out of synchronisation by half a bit period when receiving long strings of all 'ones' or all 'zeros'. For PM such a situation causes continuous data errors until synchronisation is regained at the end of the string, but for FM there would probably be only an error at each end of the string.

Certainly a possible future work would be a theoretical analysis of the edge detection decoder for comparison with the strobe detection decoder and also further investigation to see if the above proposed mechanism is solely responsible for PM performance degradation.

For comparative purposes, asynchronous clock extraction had been used in the strobe detection decoder for the above tests. Despite the fact that comparative results were obtained for both decoders, strobe detection decoder has the added advantage of the use of synchronous clock extraction which gives superior performance, as found in the results of the previous section. Thus for both PM and FM coding, the strobe detection decoder is much preferred.

Variation of Bit Rate

The curves of Figure 2.11 illustrate the effect of bit rate for a fixed length of cable.

Comparison of the two sets of curves show that :

(1) at the lower bit rates the performance of PM and FM are comparable, with only slight improvement of PM over FM;

(2) the improvement of PM over FM increases the higher the bit rate.

This increase in performance of PM over FM is explained in terms of line distortion using typical eye patterns obtained during the tests as shown in Figure 2.12.

Data is decoded by strobing at points T_1 and T_2, i.e. 25% and 75% of a bit period for FM data, but at T_2 only for PM data. At low bit rates the effect of intersymbol interference is minimal and an eye pattern such as Figure 2.12(a) is obtained. As the bit frequency increases intersymbol interference also increases, giving rise to an eye pattern such as Figure 2.12 (b). It is seen that at the lower frequencies eye openings at the strobing instant T_1 and T_2 are almost the same. However as the bit frequency increases the eye opening at T_1 becomes significantly less than at T_2. Since for FM data is decoded from decisions at both T_1 and T_2, data errors for FM tend to increase faster with increasing bit rate than for PM due to the faster rate of closure of the eye opening at T_1 as opposed to that at T_2.

Computer calculated eye patterns obtained for a 300 m length of cable at various bit rates are shown in Figure 2.13. They do illustrate the effects discussed above.

The graphs of Figure 2.14 are derived from Figure 2.11 to show the increase in S/N ratio required to maintain constant value of error rate (P_e) as bit rate increases. The increases of S/N are relative to the values for zero length of cable ; they are therefore related to the variation of line loss with frequency. The apparent increase in line loss for FM data as bit rate increases is clearly evident. The FM curve in particular shows a tendency to follow line loss curve at low bit rates but deviate more at higher bit rate where intersymbol interference becomes predominant.

Variation of Line Length

The effect of line length for a fixed bit rate is shown in Figure 2.15. The results are plotted for 3 M b/s data rate using ideal clock and PM and FM data. The graphs of Figure 2.16 are derived from Figure 2.15 to show the increase in S/N ratio required to maintain constant error rate as the cable length varies. Also shown is the corresponding line loss.

It is observed that, like the variation of bit rate, FM is more susceptible to line length increase than PM.

The poorer performance of FM is again explained by the faster rate of closure of the first half bit eye opening as the line distortion increases. Figure 2.17 shows the calculated eye patterns for a bit rate of 3 M b/s and various lengths to illustrate the eye closure phenomenon.

Generally, the results of tests on the effect of transmission line distortion confirms the dependence of the associated loss on both bit rate and cable length. It also shows that PM is less affected by line distortion.

2.3.3 Message Error Rate Tests

A summary of results obtained for tests carried out to determine the effectiveness of the code violation error detection scheme for both PM and FM codes is presented in this section. Bit undetectable errors is obtained by extrapolation of the message error rate curves and compared with theoretically predicted values.

Measurement System

A block diagram of the experimental set up is shown in Figure 2.18. The 'link' portion of the system is the same set up used for the bit error rate tests described in section 2.3.2. Pseudo-random data generated by the 'link' is effectively asynchronously subdivided into messages by the Message Error Rate Test (MERT) unit (see Appendix H for detailed description). During the message period which can be preset up to 16 bits long, any code error pulses produced by the decoder set a flip-flop and similarly data error pulses from the BERT unit set a second flip-flop. In the 3-bit interval between messages the flip-flop outputs are strobed to produce three possible pulse outputs indicating the following types of erroneous message :

(a) containing one or more code errors (MCE) ;
(b) containing one or more data errors (MDE) ;
(c) containing one or more data errors but no code error, i.e. an undetected message error (MUE).

Message error rate is measured by feeding the respective output (MCE or MDE or MUE) into the 'B' channel of a Hewlett Packard Counter/Timer type 5326A set up to display frequency. Using the 'enable' output as an external time base, the reading in MHz divided by 10 gives the error rate normalised to the message rate and the message error probability. The bit rate clock to the MERT circuit is supplied by the strobe pulse output from the BERT unit.

Test Procedures

The general procedure for the tests was to set up the 'link' as in section 2.3.2 for a particular frequency and signal-to-noise ratio to give constant data and code error rates. Message error rate measurements are made by selecting message lengths in appropriate steps and reading off the corresponding message error rates on the H.P. counter. A data bit rate of 250 Kb/s was used for all the tests.

Test Results

The experimental results are presented as graphs of P_m against m where P_m is the message error rate and m is the message length respectively.

Typical message error rate curves obtained using strobe detection decoder with an ideal clock extraction for PM and FM coded data are shown in Figure 2.19. The general trend of these curves tend to confirm the theoretical results of Appendix A.4 that message error rate varies linearly with message length. The approximate bit error rate P_e, obtained by finding the slopes of the P_m vrs m curves is summarised in Table 2.1. It shows the following general trend :

Comparison of data error rates and code error rates show the expected relationship as given in Appendix A.1 and A.2, that code error rates are equal for PM and FM and that data error rates are in the ratio 1 : 2 for PM and FM respectively.

The undetectable bit error rate for PM seem to confirm the results of the theoretical analysis as given in Appendix A.3.1 that for PM, undetectable error rates are equal to the square of the data bit error rate. This result is borne out by the closeness of the experimental results to the theoretical results shown in a magnified form in Figure 2.20.

BIT ERROR RATE	PM		FM	
	Theoretical	Expt.	Theoretical	Expt.
P_{bde}	P_e	P_e	P_e	P_e
P_{bce}	$2P_e$	$2P_e$	P_e	P_e
P_{bue}	P_e^2	$1.05P_e^2$	$\frac{1}{2}(P_e)^2$	$0.27P_e$

Table 2.1

Theoretical and Expt. Bit Error Rates

The undetectable error rate for FM, determined by the initial slope of the curve, on the other hand, is rather large and seems to give a value which is proportional to the data bit error rate rather than its square as predicted by the theory given in Appendix A. 3. 2. Figure 2.21 shows similar results for FM but for a larger value of data bit error rate (P_e = .0475). It is noted that the initial slope of this curve also gives a value of P_{eu} that is proportional to P_e. However as the message length is increased, the slope decreases and tends to give a value of P_{eu} that is proportional to P_e^2.

The above results seem to confirm an expected false undetectable error condition arising from a single half-bit element error in the first data bit of the message, and which would tend to give errors proportional to the data bit error rate. However it was expected that this false error condition would become less significant at a much lower message length than seem to be the case indicated by the results. It rather shows that a longer message length would be required in order to accurately predict the undetectable error rate.

Later experimental tests, using a logic analyser however confirmed that the occurrence of double half-bit element errors is in fact proportional to the square of the corresponding data bit error rate for both PM and FM codes.

The following general conclusions can be drawn from the message error rate tests :

(a) the undetectable errors associated with error detection schemes based on code violation testing is proportional to the square of the data bit error rate for both PM and FM codes.

(b) for PM the constant of proportionality is UNITY as predicted by theory ; however for FM, the theoretical

factor of 2 advantage over PM could not be confirmed because of the relatively short message lengths used for the tests. However the trend of the results obtained seems to suggest a constant of proportionality of less than UNITY, which is in line with the theory.

2.4 Receiver Input Filtering

The results of loading studies (reported in Chapter 3) showed that the overall frequency response of the coupling transformers change with number of connected loads. It thus became clear that to achieve a well defined receiver pass-band particularly at the upper end it would be necessary to insert a low-pass filter between each terminal receiver and its transformer. The objectives in the design of this were :

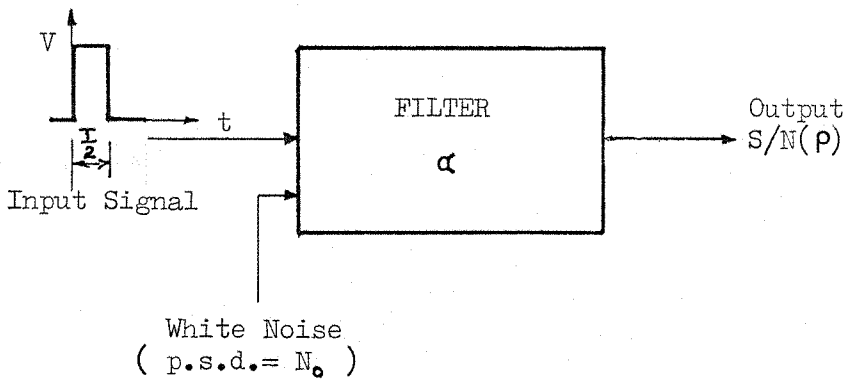
(a) to have a cut-off frequency independent of the number of terminals ,
(b) to present a constant and fairly high resistive input impedance over the whole pass band,
(c) to maximise the peak signal voltage to r. m. s. noise voltage ratio,
(d) to avoid excessive signal distortion and the consequent intersymbol interference.

Simple RC networks were rejected because they could not satisfy requirement (b). Of several other types of network which were studied or tested experimentally a 2nd order Butterworth RLC network was finally selected as offering the best all round performance without excessive complexity.

Results of theoretical and experimental work carried out to determine the performance of this filter when the input signal is PM or FM coded data is presented in this section.

2.4.1 Optimum Filter Cut-Off Frequency

To determine the value of the cut-off frequency f_o (at -3dB point) which would satisfy requirement (c), an analysis was made of the peak signal to r.m.s. noise voltage ratio at the filter output as a function of the product f_oT for a single rectangular pulse input of width T/2 accompanied by white Gaussian noise, following the treatment of sub-optimum filters given in (13). The input pulse represents a half-bit element of a PM or FM coded data signal of bit period T. See Figure below.



The output peak signal to noise ratio can be expressed in the form :

$$\rho = \alpha\sqrt{\frac{2E}{N_o}} \qquad (2.10)$$

where E is the energy of the input pulse ($= \frac{V^2T}{2}$) and α is a positive real factor ≤ 1. The equality applying only for a matched filter. A graph of α in dB vrs f_oT is given in Figure 2.22 (a) which shows that the maximum value of α occurs for f_oT just less than 1.

Experimental tests of error rate vrs f_oT for FM coded data over zero line length at constant signal-to-noise ratio confirmed that the optimum value of f_oT was just less than 1. Typical experimental results are shown in Figure 2.22 (b).

The theoretical curve of P_e vrs $f_o T$ shown in Figure 2.22 (b) for comparison was derived by using the calculated peak signal to noise ratio ρ in the theoretical equation for P_e derived in Appendix A. i.e. for FM coding :

$$P_e = \text{erfc}\left(\sqrt{\frac{1}{2}\frac{S}{N}}\right) \qquad (2.11)$$

$$= \text{erfc}\left(\frac{\rho}{\sqrt{2}}\right)$$

Now from Equation 2.10

$$\rho^2 = \alpha^2 \frac{2E}{N_o} = \alpha^2 \frac{V^2 T}{N_o}$$

The input noise p.s.d. from the experimental noise generator giving a noise power P_n over a band of B_c is assumed to be given by :

$$N_o = \frac{P_n}{B_c} \qquad \text{where } B_c \gg f_o$$

Thus

$$\rho^2 = \frac{V^2}{P_n} B_c T \alpha^2$$

$$= \left(\frac{S}{N}\right)_{in} B_c T \alpha^2 \qquad (2.12)$$

where $\left(\frac{S}{N}\right)$ is the measured input signal to noise ratio for zero line length and α^2 as a factor of $f_o T$ is taken from Figure 2.22 (a).

For comparison with the experimental results the following values were taken :

$$(S/N)_{in} = 8 \text{ dB}$$

$$B_c = 8 \text{ MHz}$$

$$T = 0.33 \,\mu\text{s}$$

which yielded an optimum value of $f_o \simeq 2.7$ MHz

2.4.2 Intersymbol Interference

Figure 2.23 shows calculated responses of FM and PM codes at the filter output for $f_o T = 1$. They are shown for :

(a) single $\frac{1}{2}$ bit element,
(b) two similar polarity elements (FM "1")
(c) two opposite polarity elements (FM "0")

All the waveforms show that intersymbol interference effects are minimal.

An analysis of the intersymbol interference (ISI) from a single element, shown in Figure 2.23 (a), as a function of $f_o T$ was carried out and the results are presented in Figure 2.24. The two relative ISI factors are defined as

$$\beta_1 = \frac{y(T)}{y(T/2)}$$

and

$$\beta_2 = \frac{y(3T/2)}{y(T/2)}$$

where y(t) is the filter output waveform. β_1 is a measure of the ISI at the neighbouring $\frac{1}{2}$ bit sampling point and β_2 is a measure of the ISI carried into the second element. It will be seen from the two curves that $\beta_1 = \beta_2$ at $f_o T \simeq 1.1$. This is clear by the optimum point in the vicinity of $f_o T = 1$ since it would tend to minimise the overall effect of the ISI.

Eye Patterns

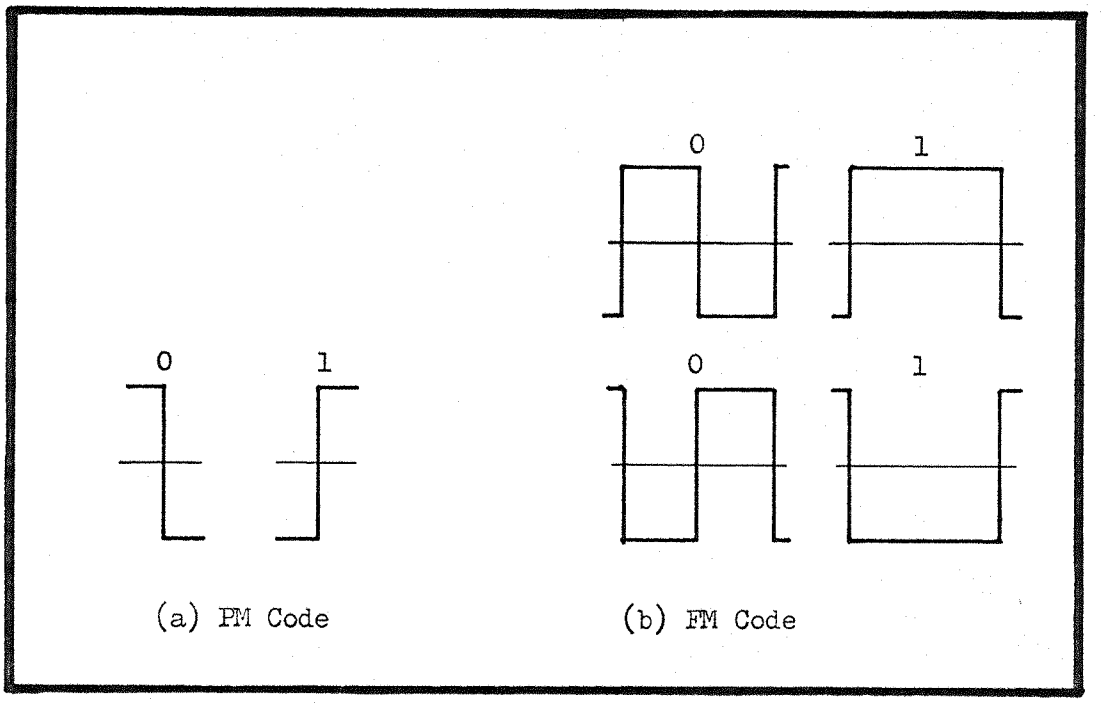
Observation of the eye pattern of coded data also showed that intersymbol interference effects were locally minimised at $f_o T \simeq 1$. This is illustrated by the two sets of photographs shown in Figure 2.25. The first set is for a data rate of 6M b/s and the

second set for 3 M b/s. It is interesting to note that the line distortion effect which causes unequal eye opening of the received signal is eliminated at the filter output ; with peaks of the $\frac{1}{2}$ bit elements occurring at the desired $\frac{1}{4}T$ and $\frac{3}{4}T$ sampling points.

From the above results of tests and studies on receiver input filtering of PM and FM coded data, the following conclusions can be drawn ;

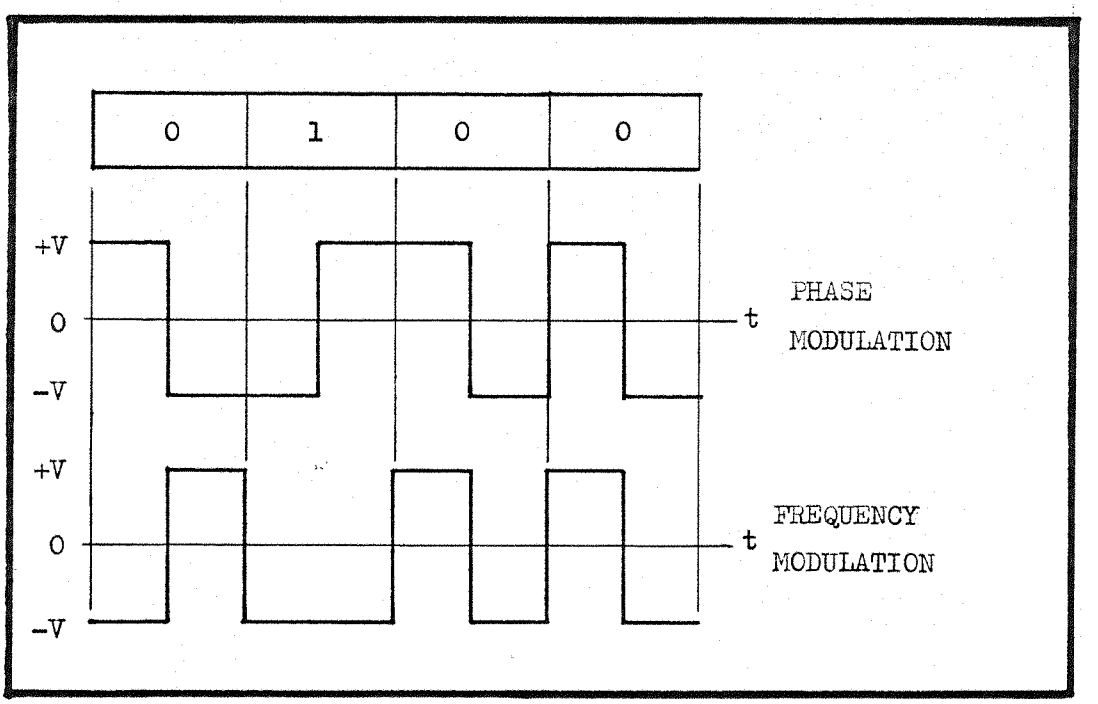
(1) It is possible to use a much lower cut-off frequency than had been previously thought possible,

(2) operation close to the optimum for both peak signal to noise ratio and intersymbol interference is possible for a cut-off (-3 dB) frequency equal to the bit rate.



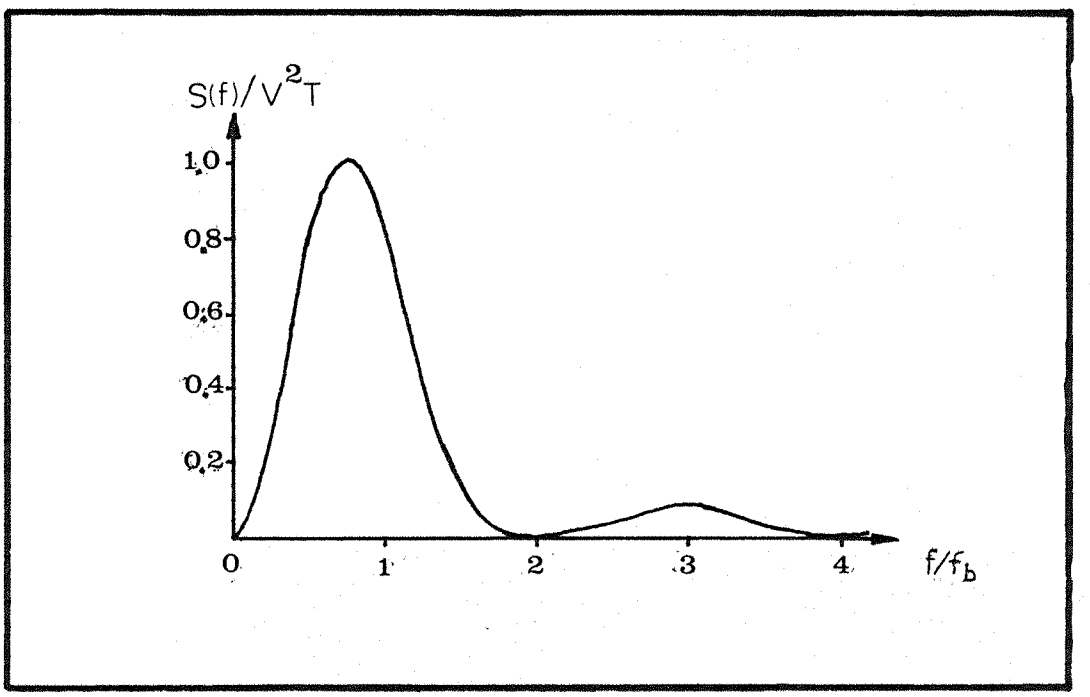
Basic Elements of PM and FM Codes

FIG 2.1



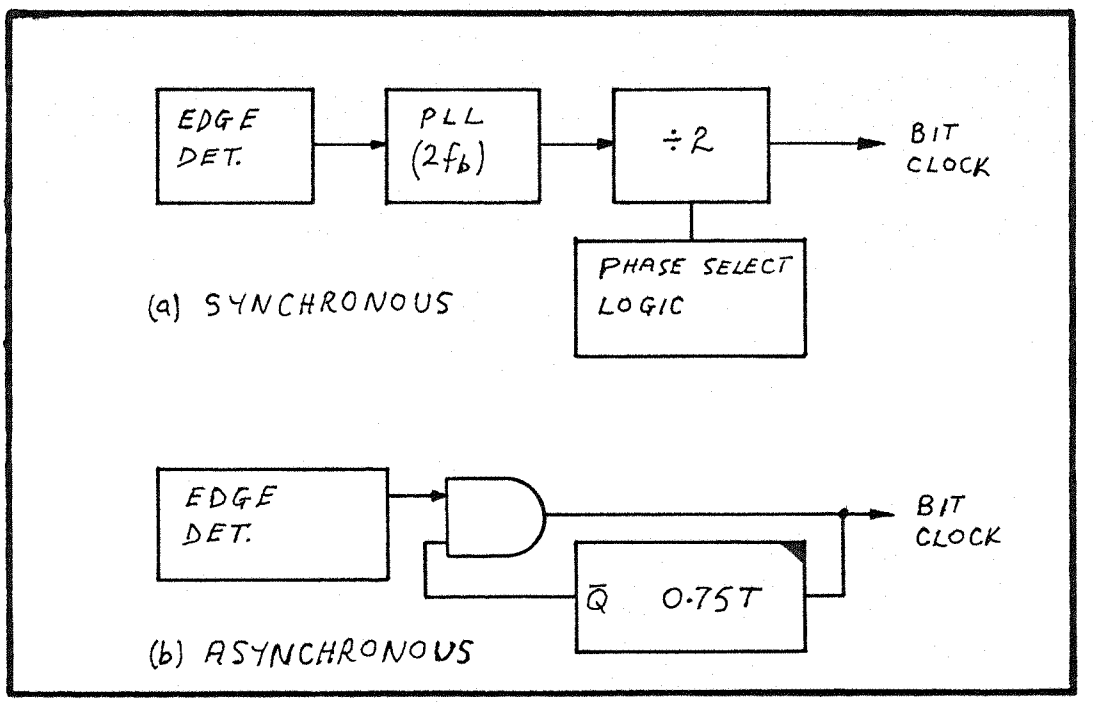
PM and FM Coded Signal Waveforms

FIG 2.2



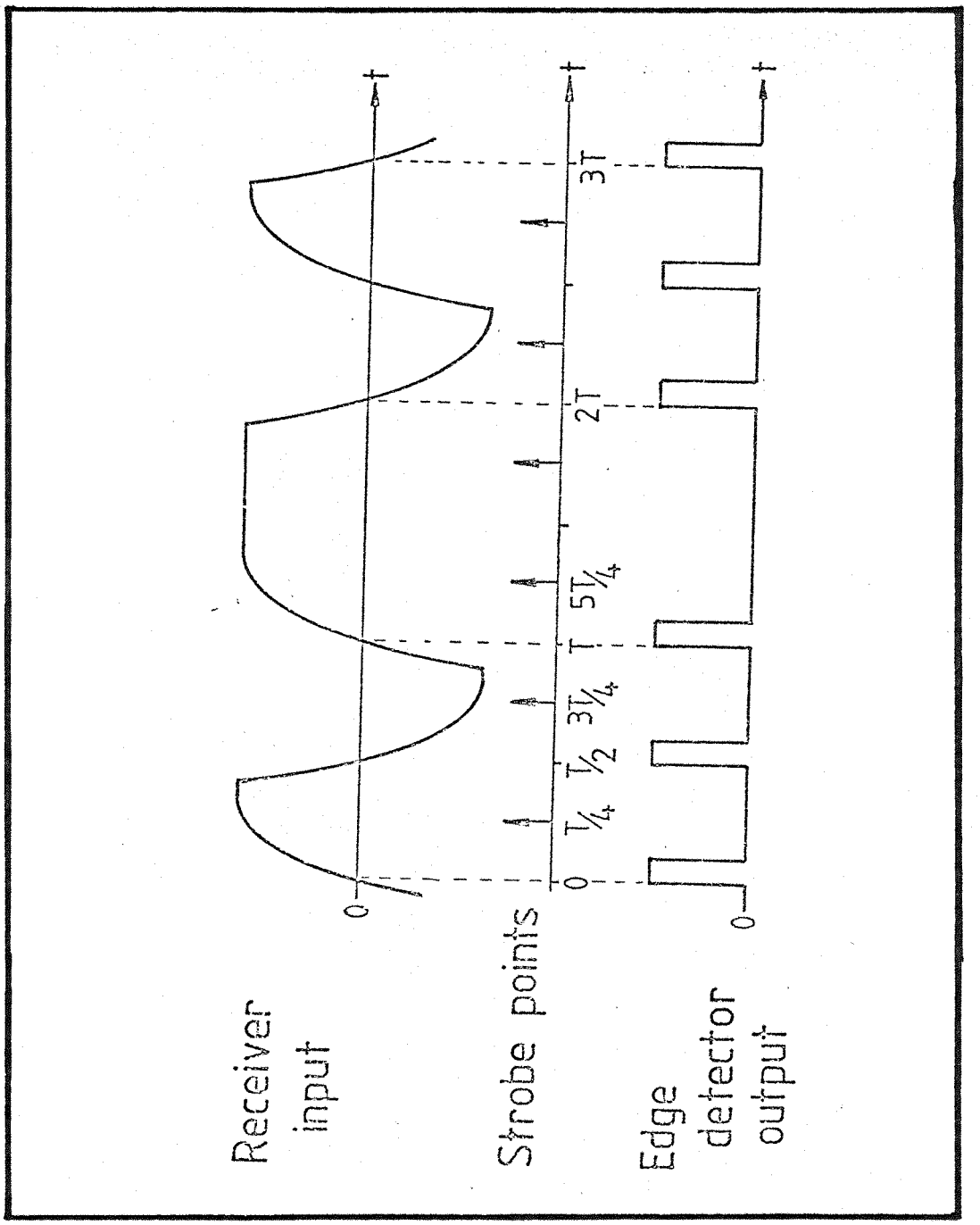
Power Spectrum of Coded Random Sequence

FIG 2.3



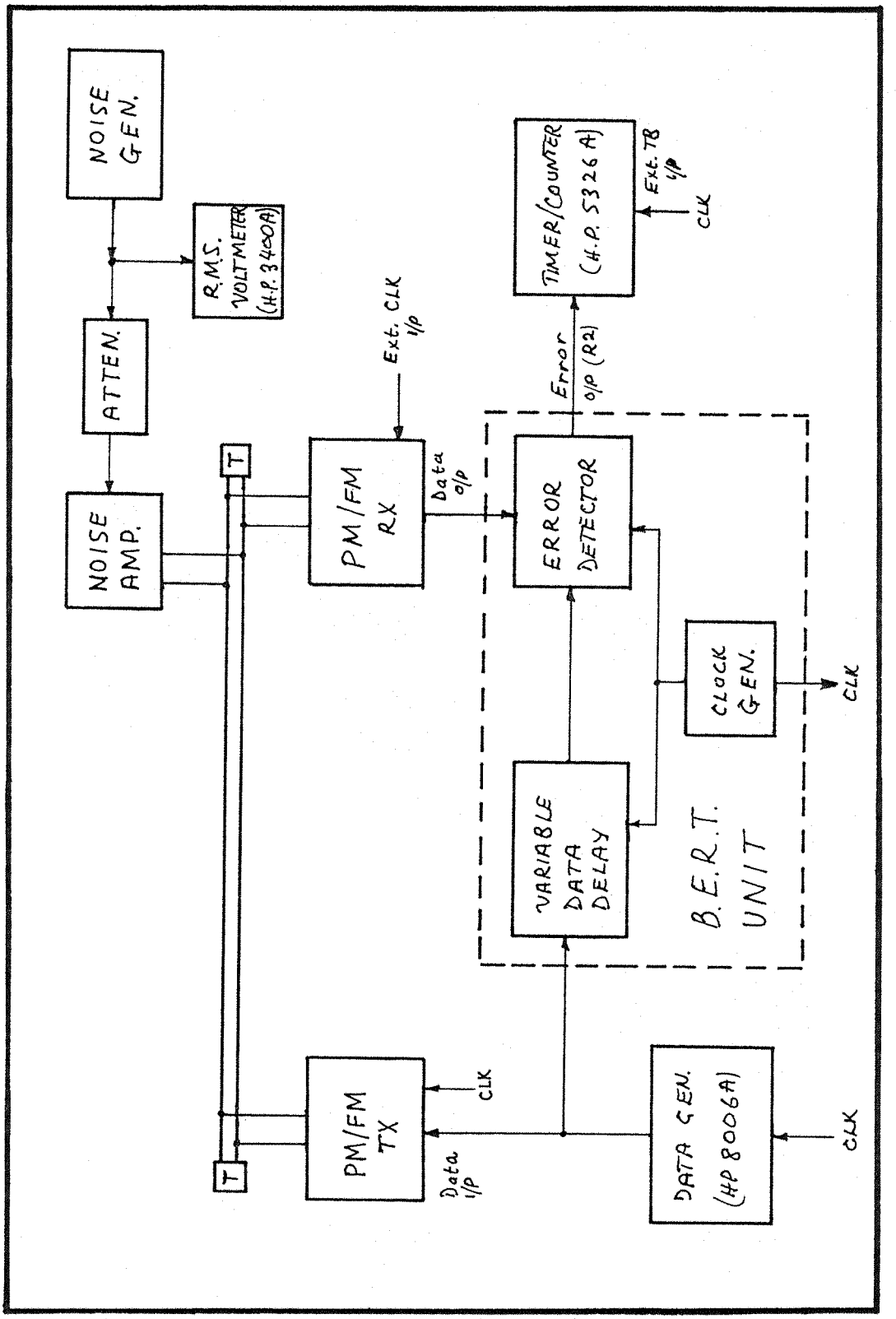
Methods of Clock Extraction from PM and FM Codes.

FIG 2.4



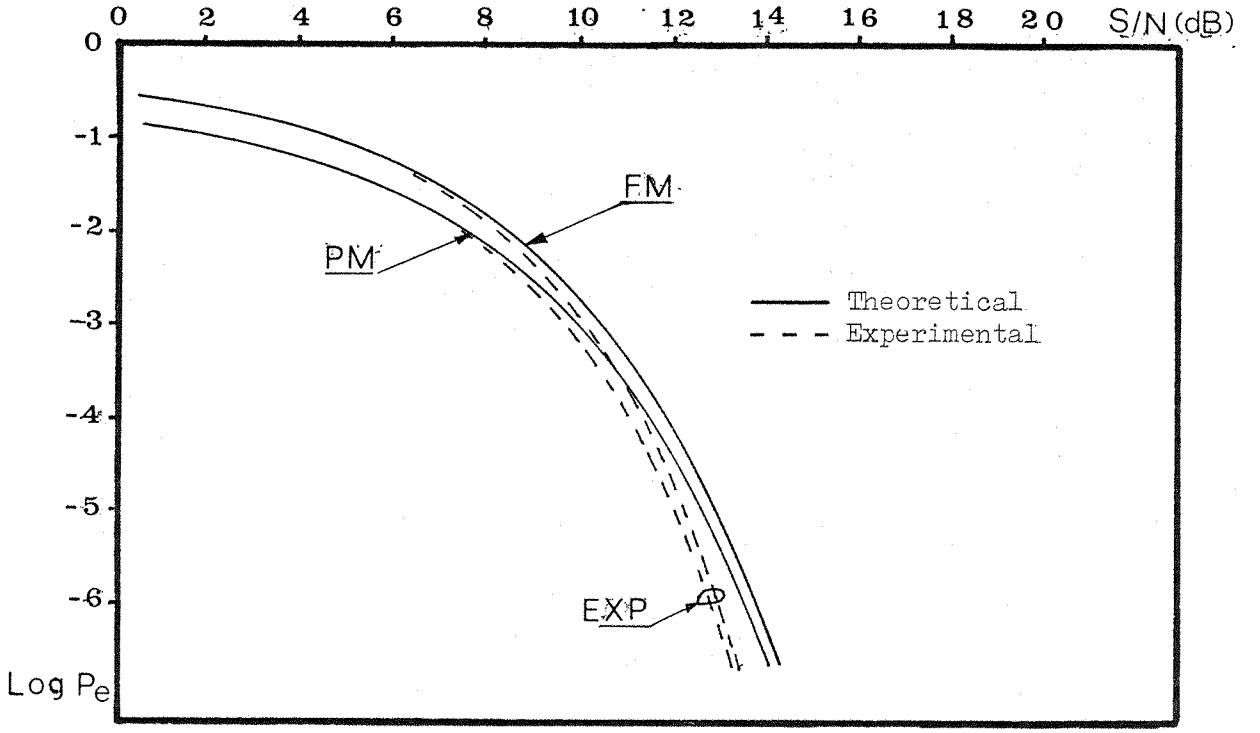
Principles of PM and FM Decoding

FIG 2.5



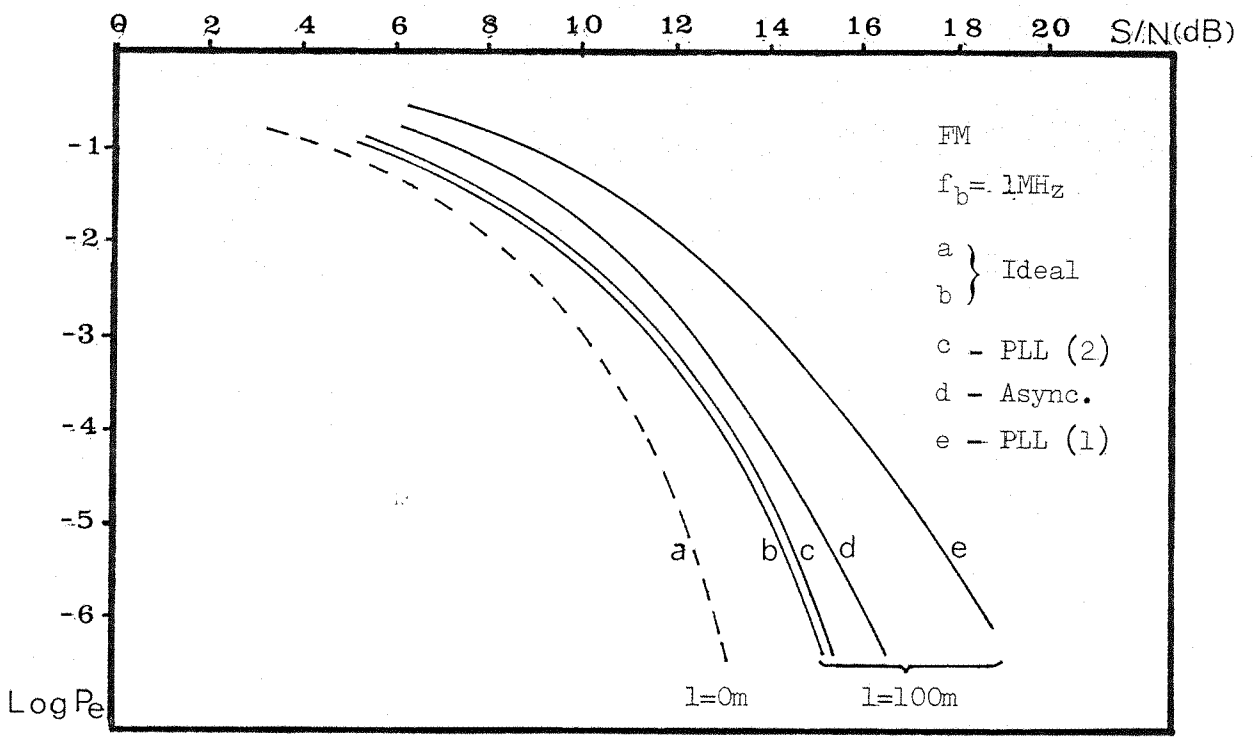
Bit Error Rate Measurement System

FIG 2.6



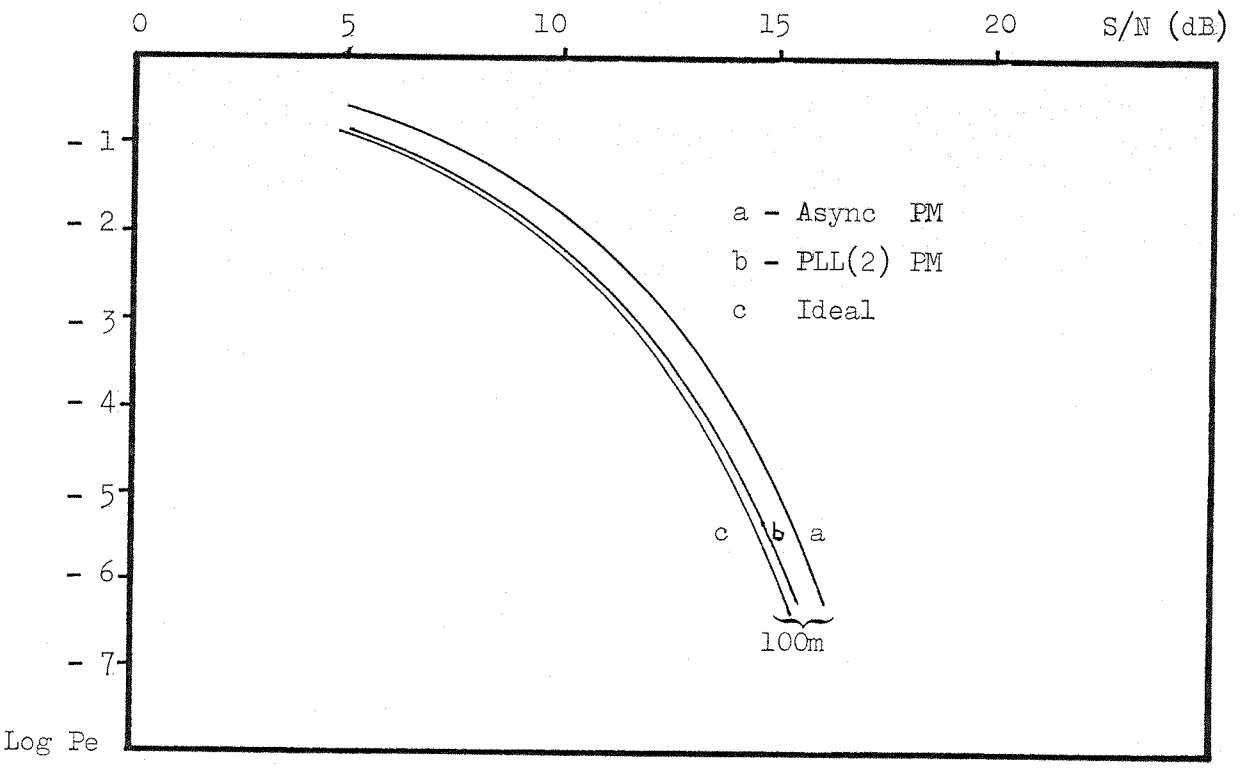
ERROR RATE:- Theoretical & Experimental

FIG 2.7



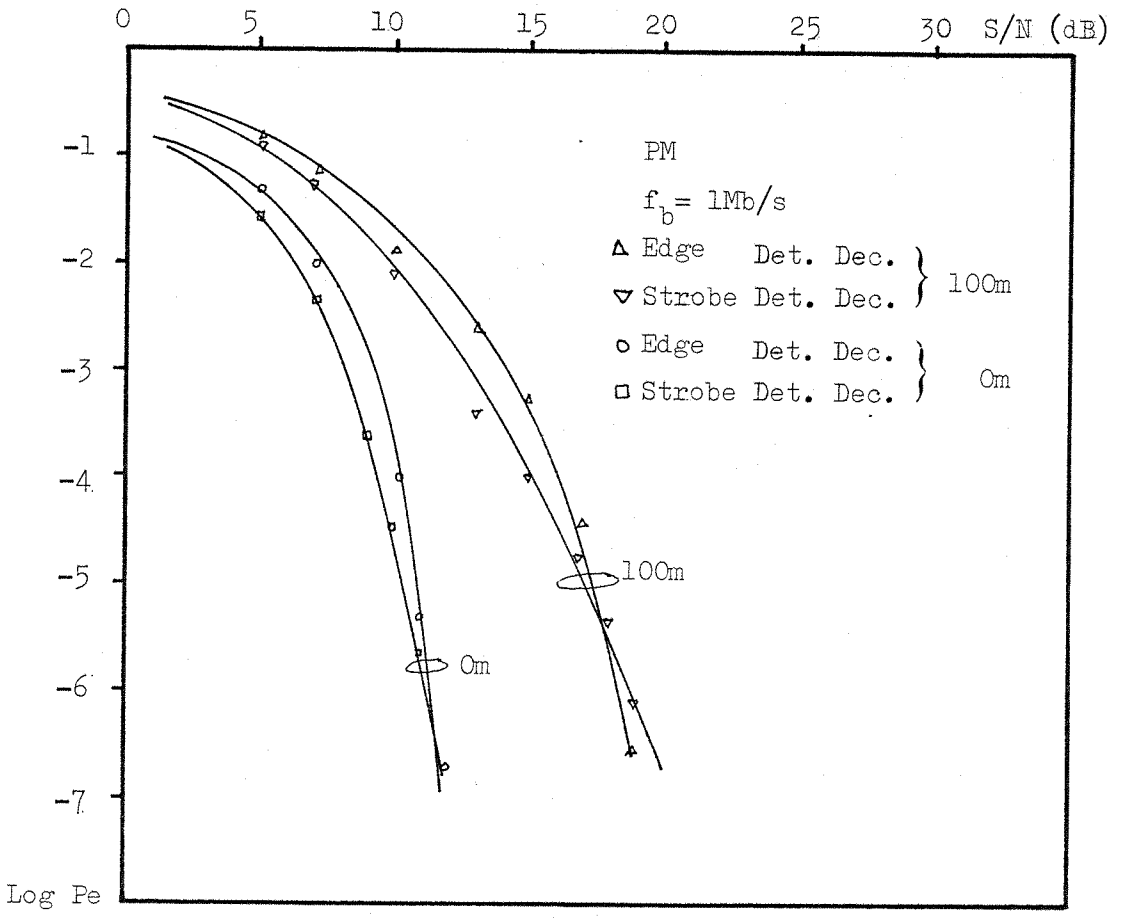
ERROR RATE:- Synchronous and Asychronous Clocks

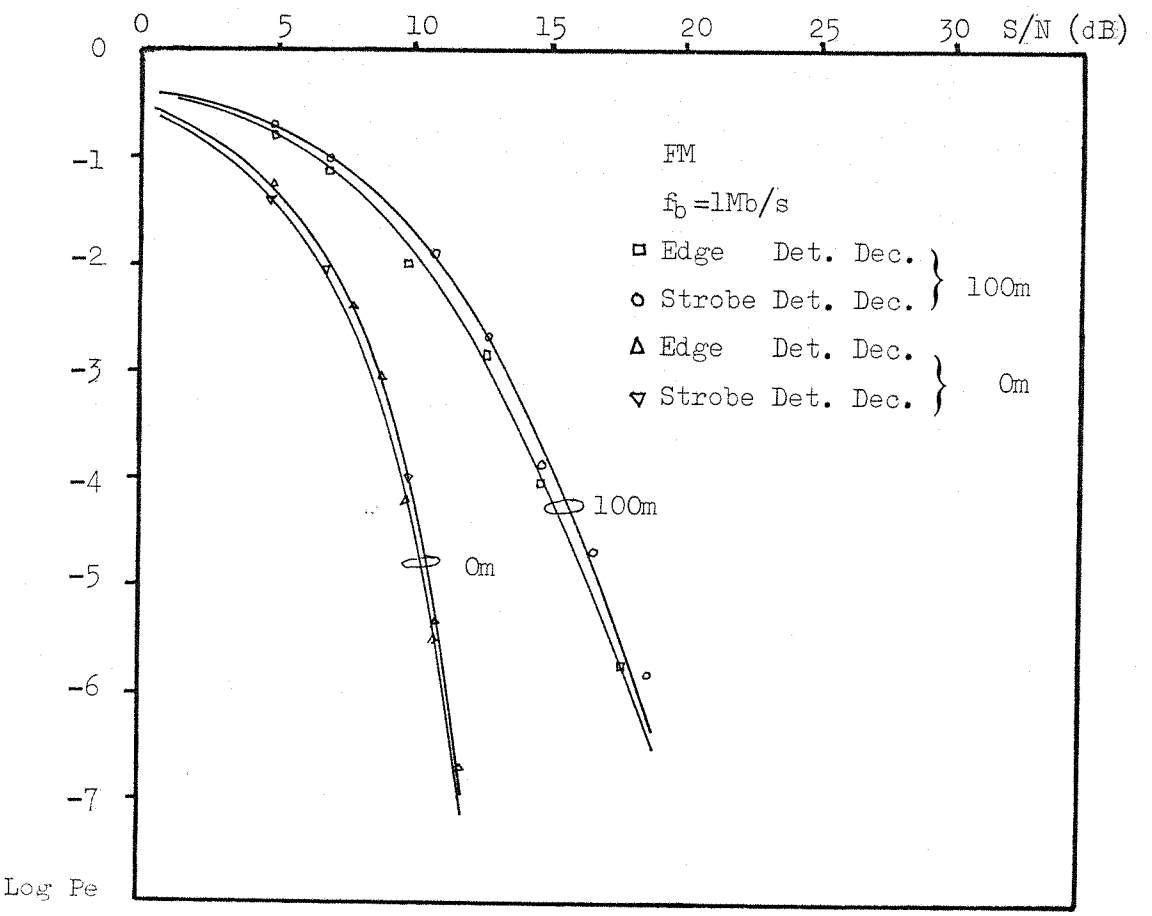
FIG 2.8



ERROR RATE:- Synchronous and Asynchronous Clocks

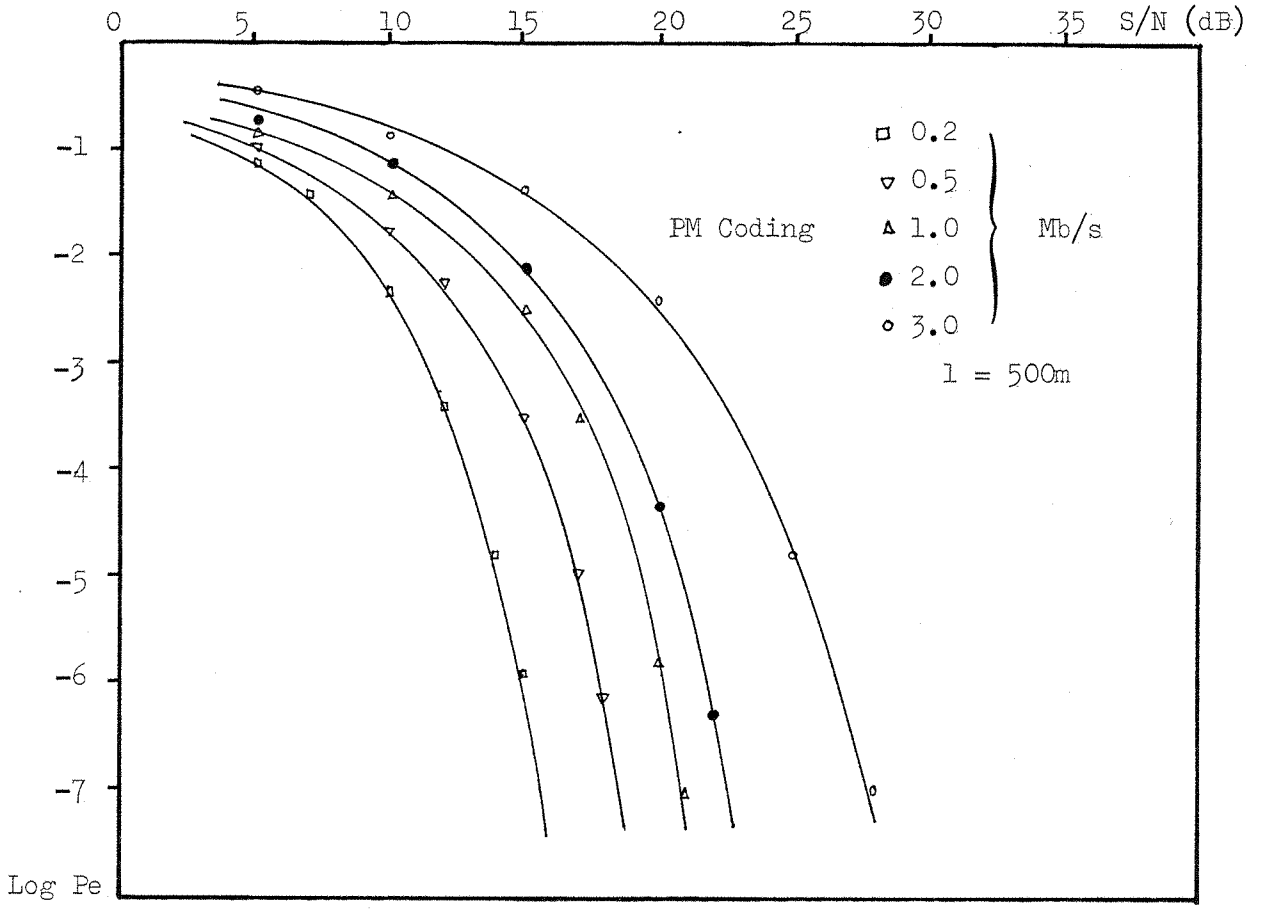
FIG 2.9

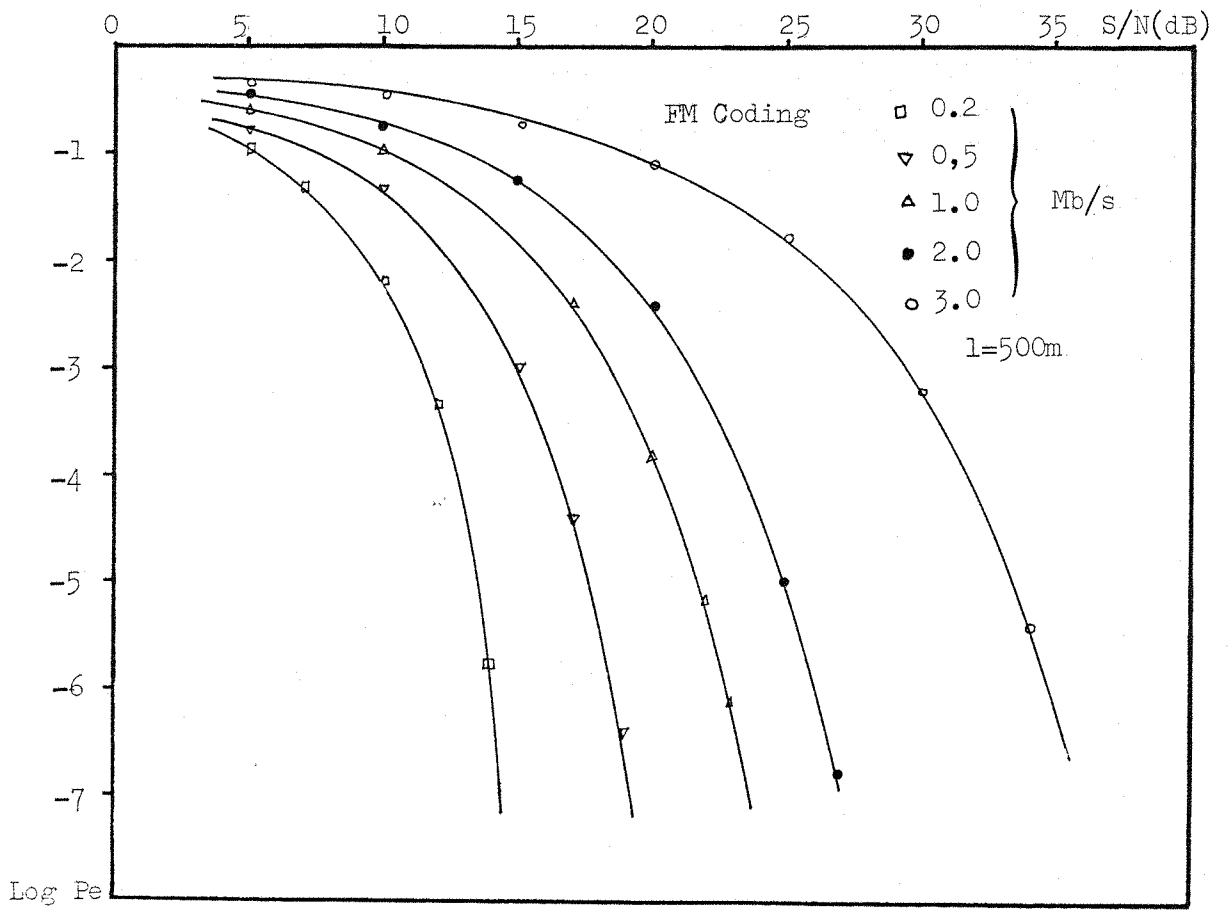




ERROR RATE:- Strobe and Edge Det. Decoders

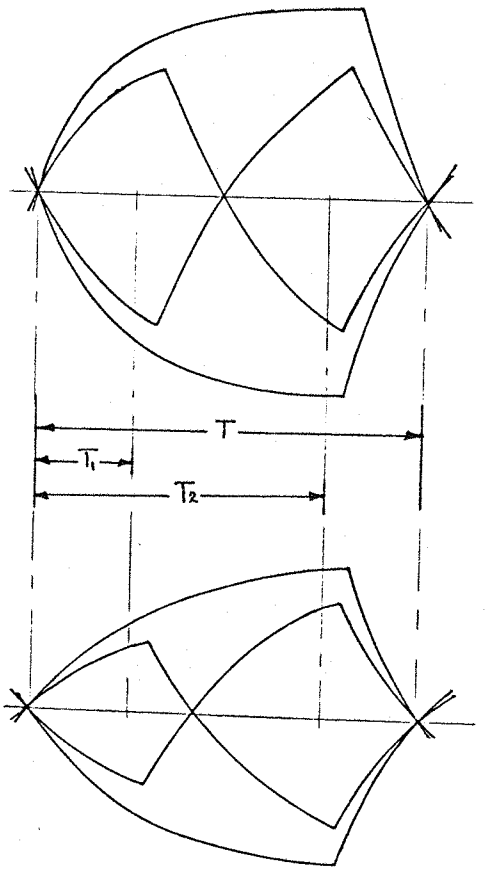
FIG 2.10





- ERROR RATE:- Variation of Bit Rate

FIG 2.11

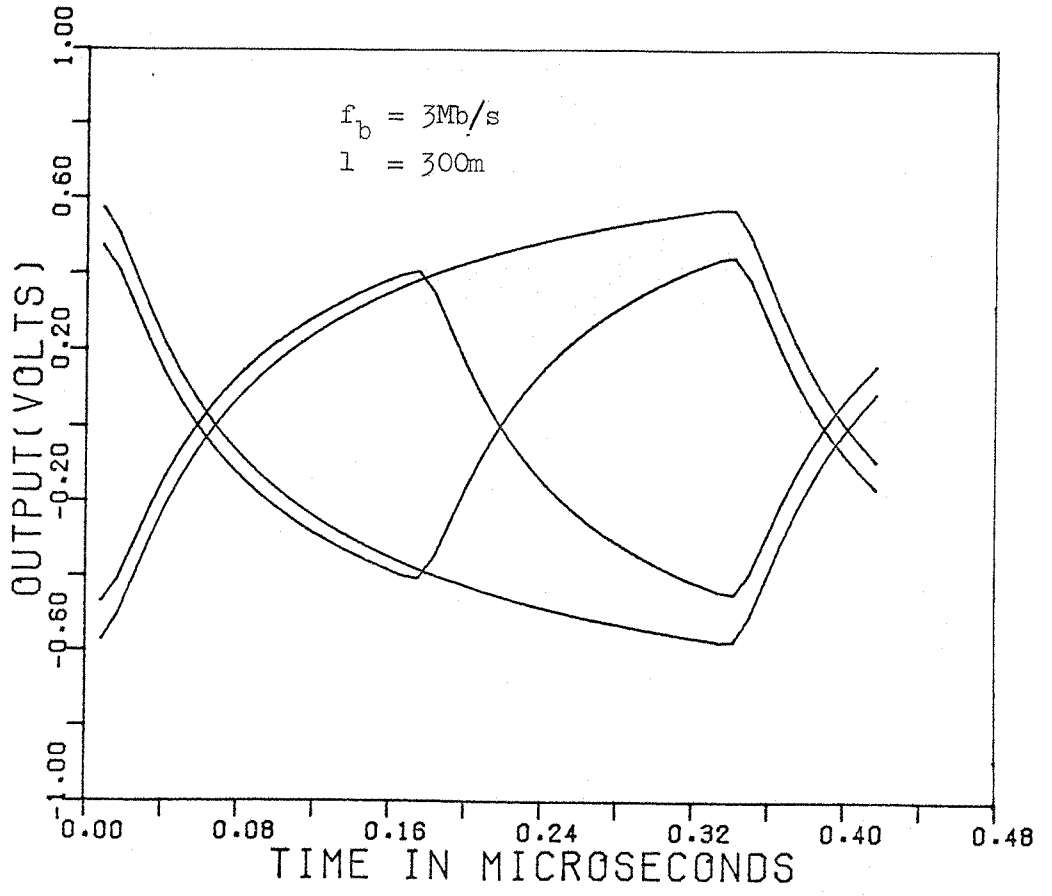


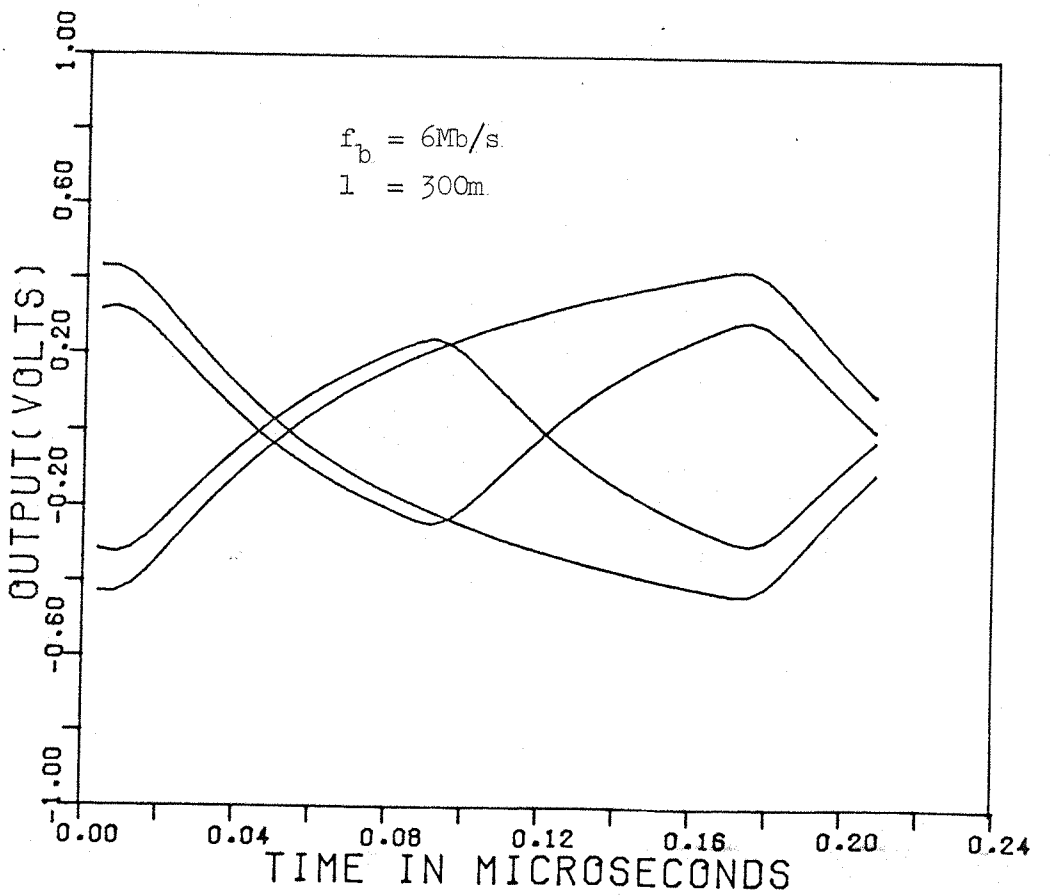
LOW BIT RATE (a)

HIGH BIT RATE (b)

EYE PATTERNS:- Variation of Bit Rate

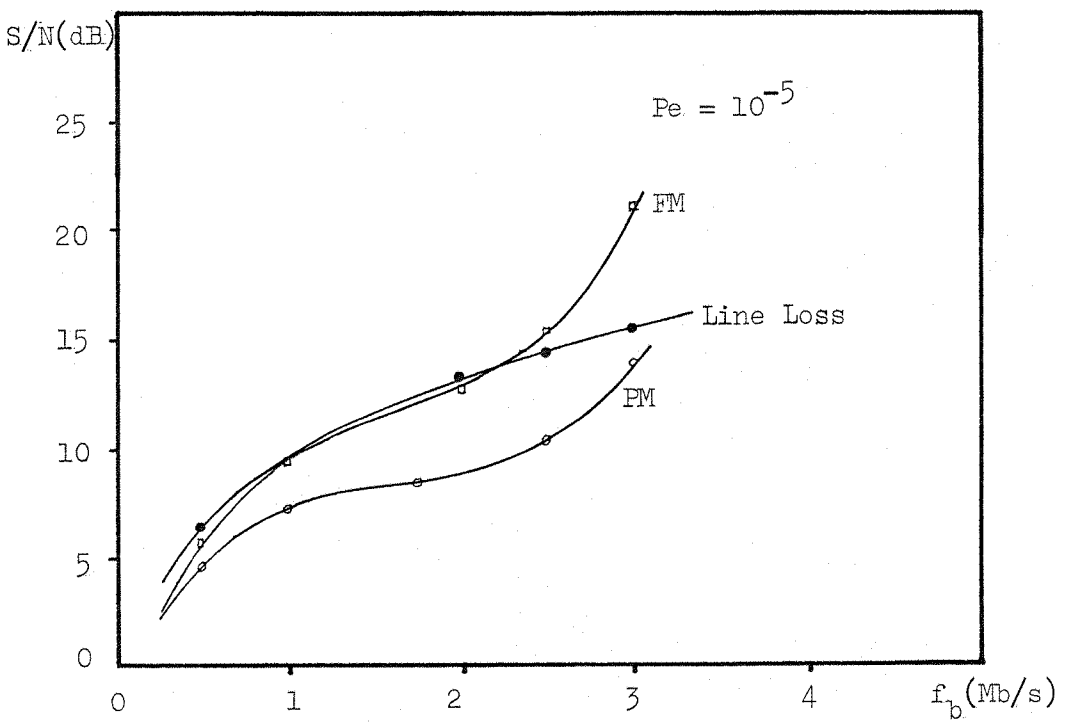
FIG 2.12





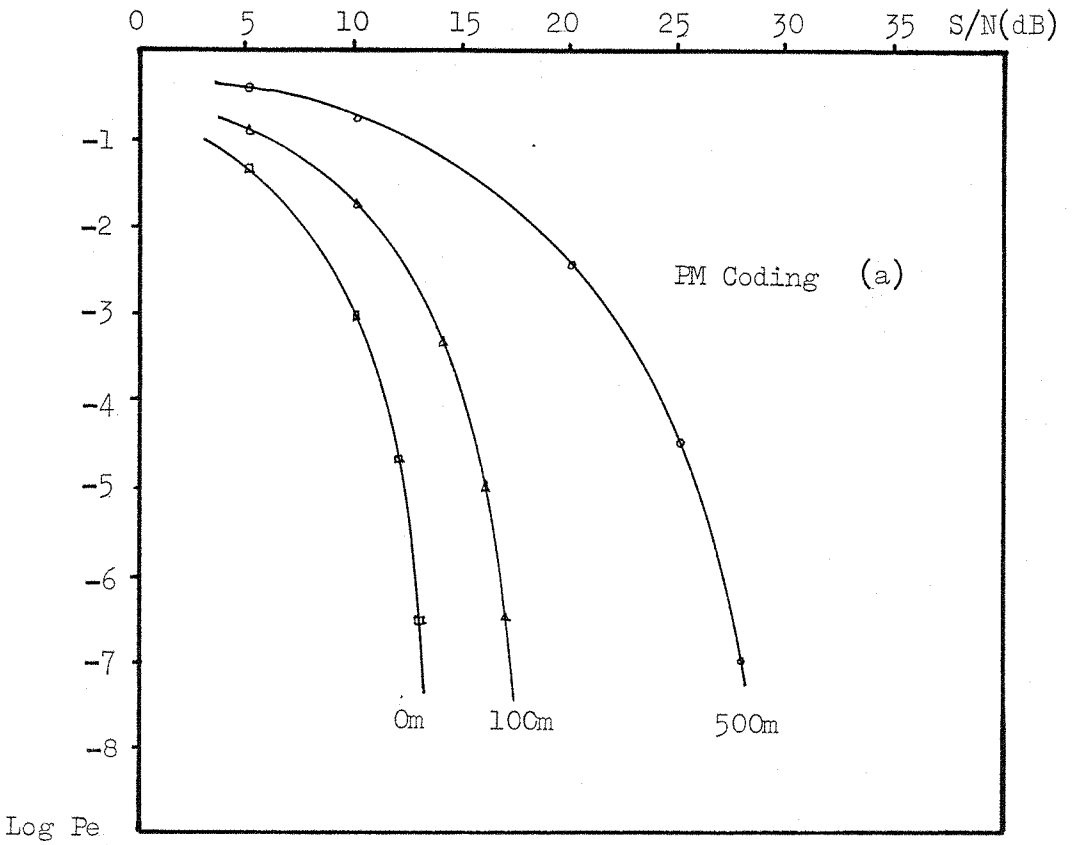
EYE PATTERNS:- Variation of Bit Rate

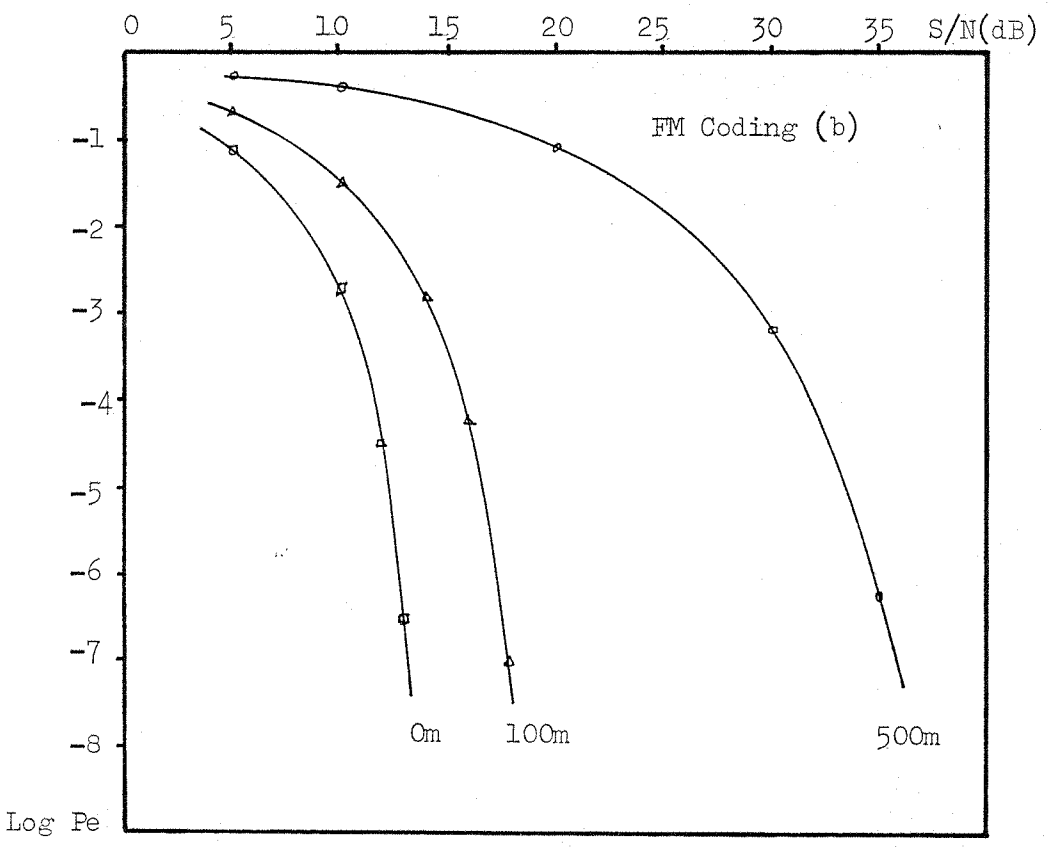
FIG 2.13



Increase In S/N Relative to Om

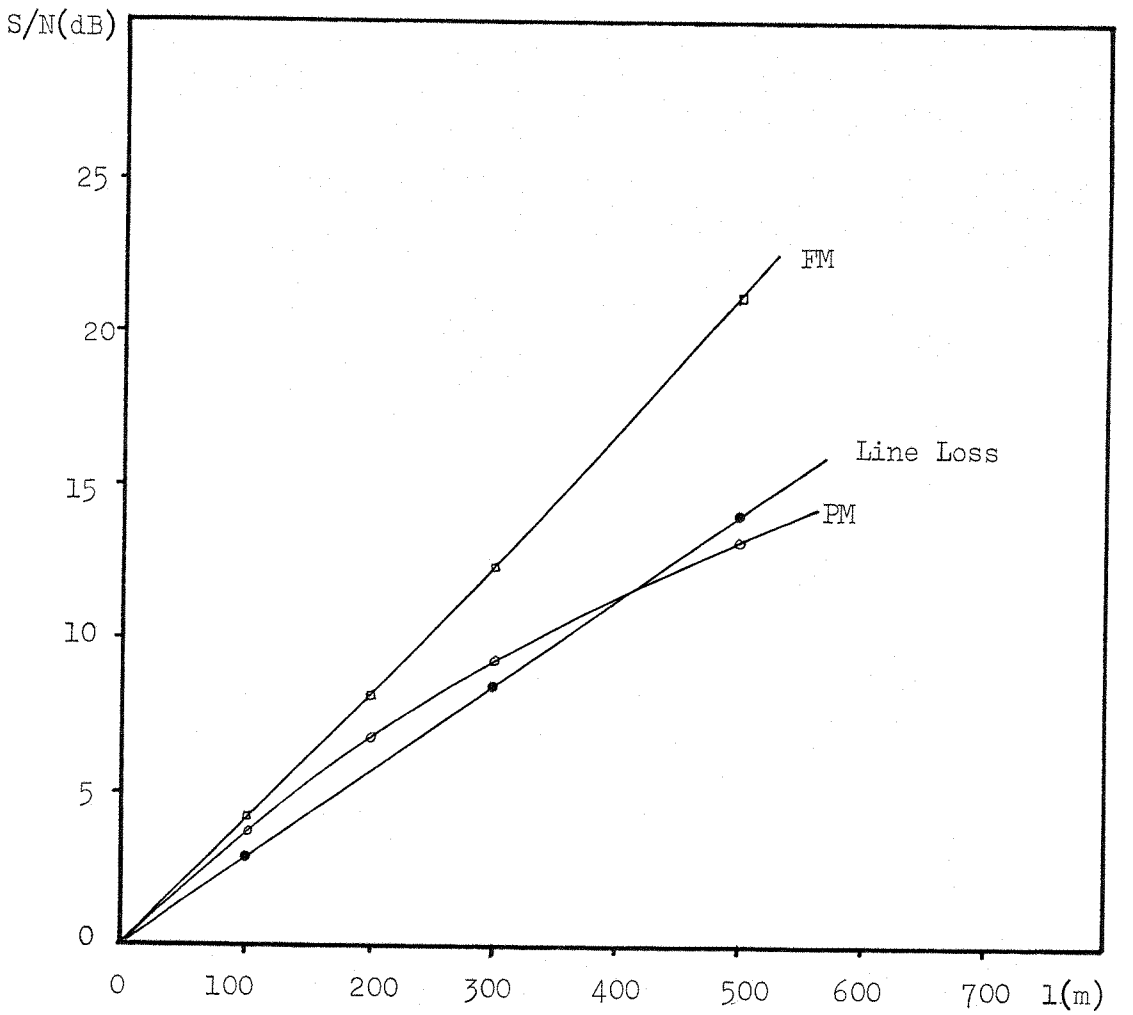
FIG 2.14





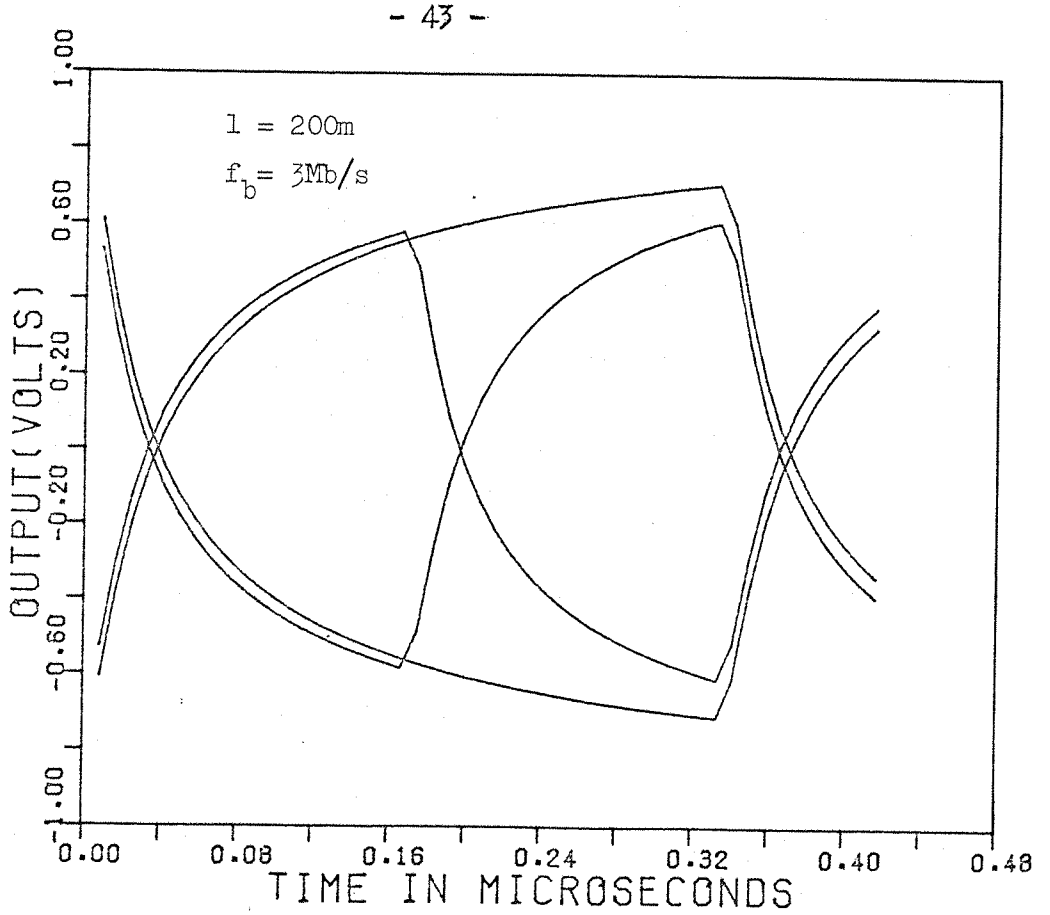
ERROR RATE:- Variation of Line Length

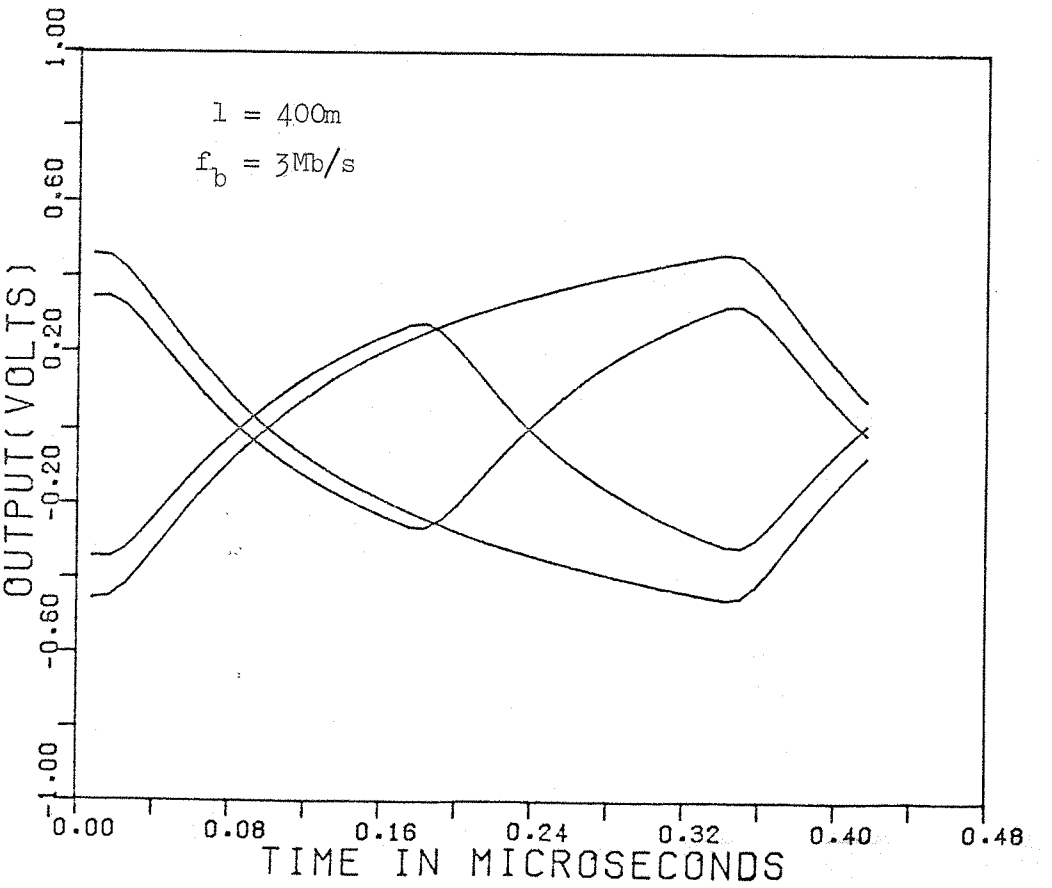
FIG 2.15



Increase In S/N Relative to Om

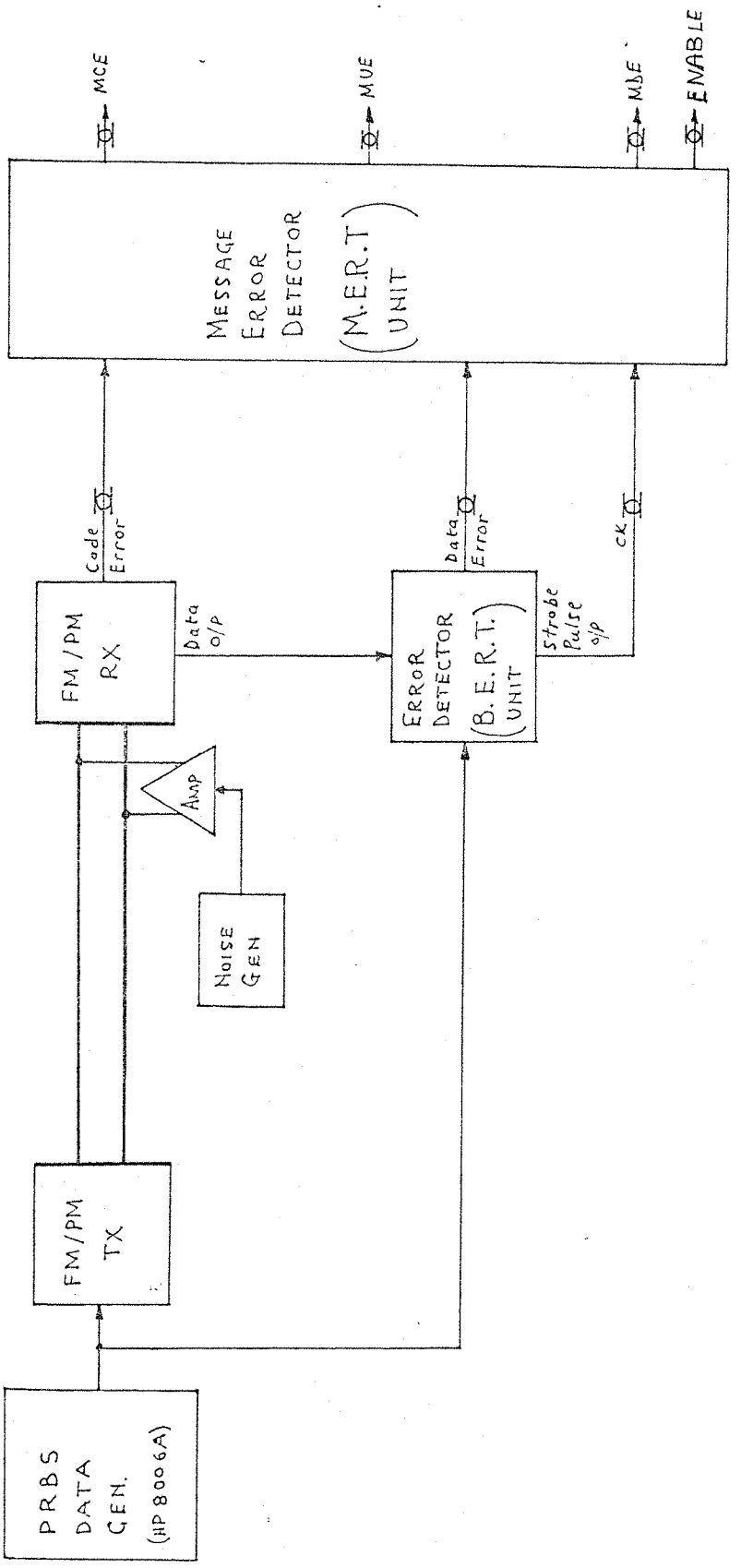
FIG 2.16



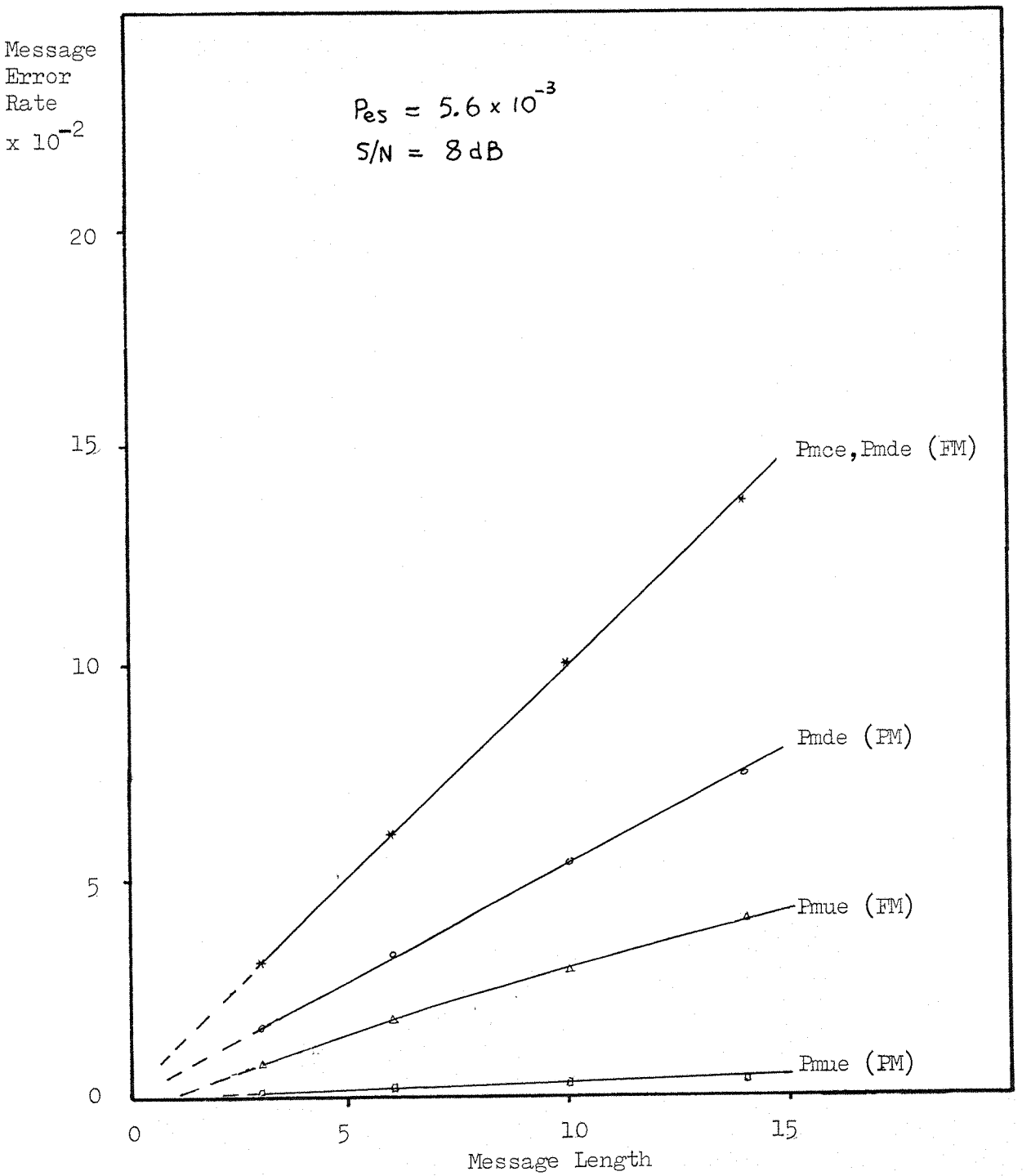


EYE PATTERN:- Variation of Line Length

FIG 2.17

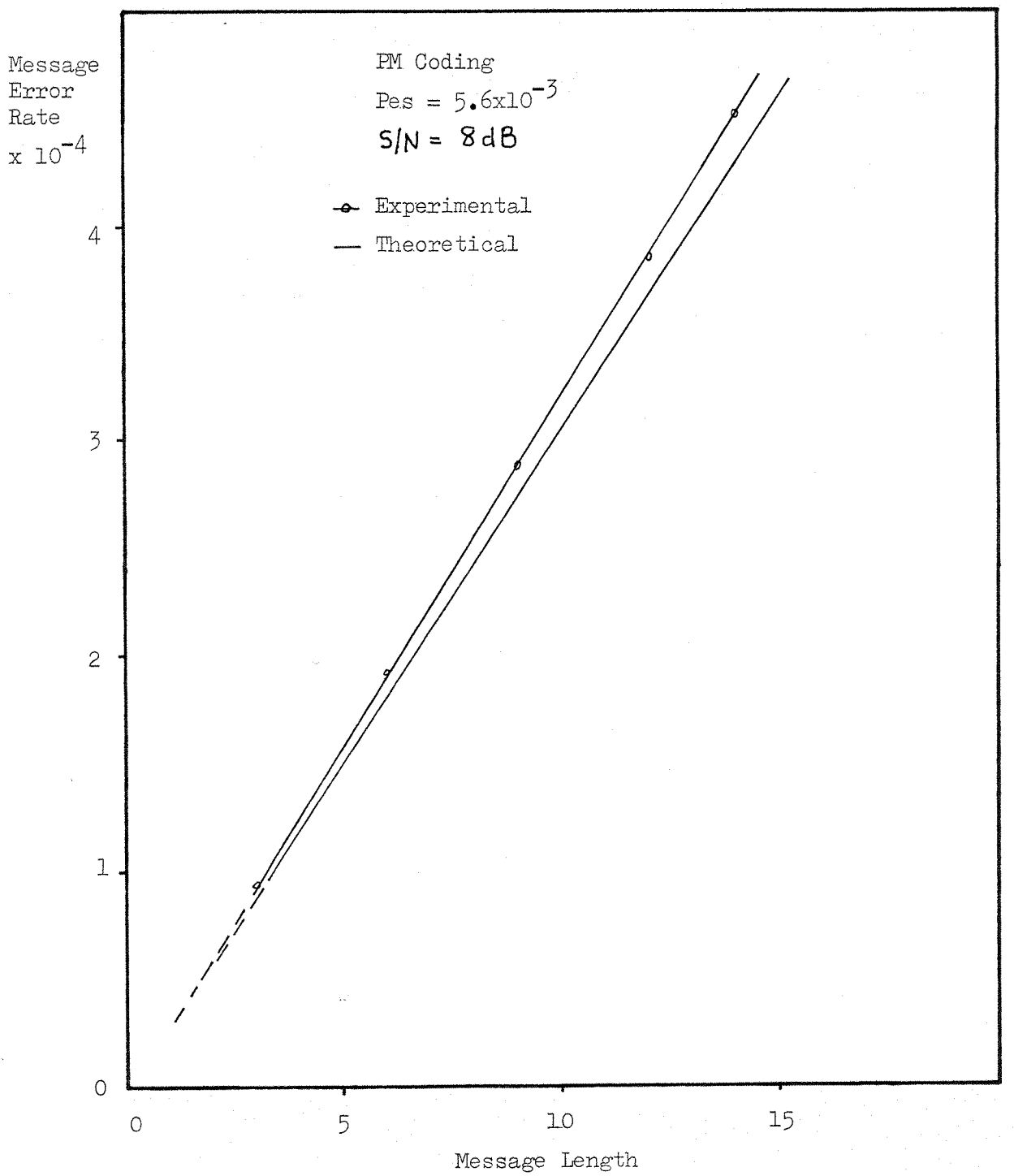


MESSAGE ERROR RATE MEASUREMENT SYSTEM FIG 2.18



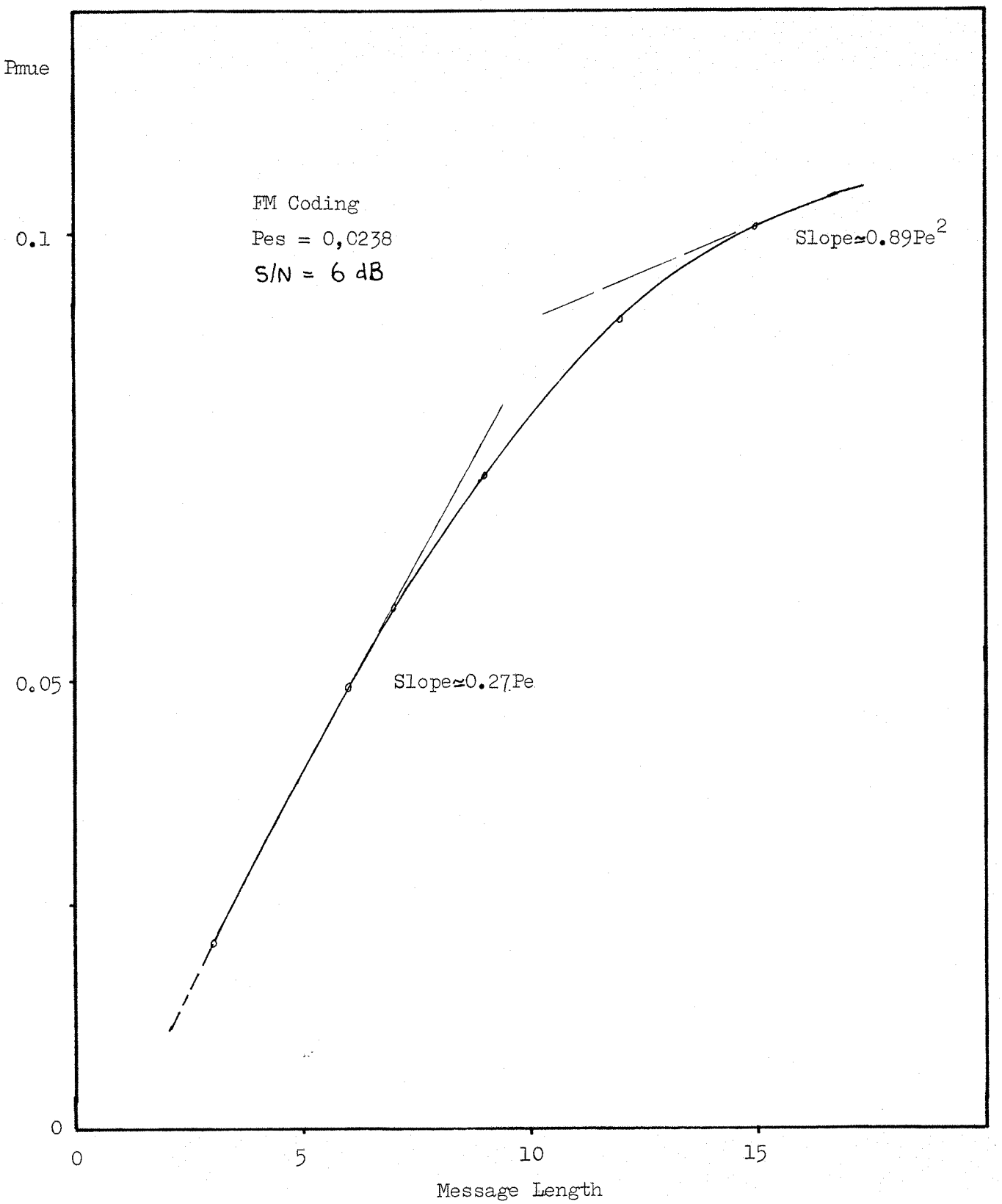
Message Error Rate In PM and FM Codes

FIG 2,19



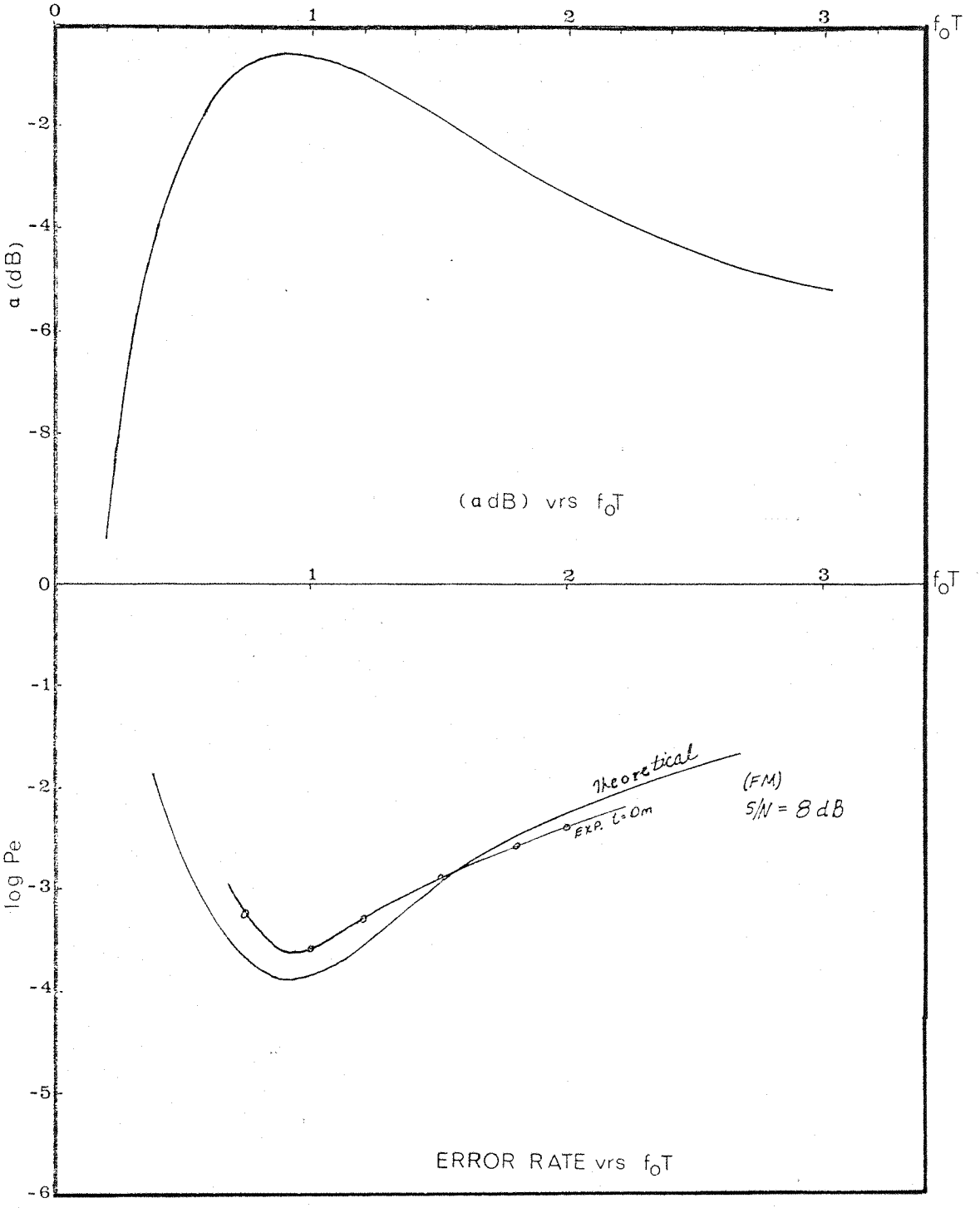
Message Undetectable Error Rate

FIG 2.20



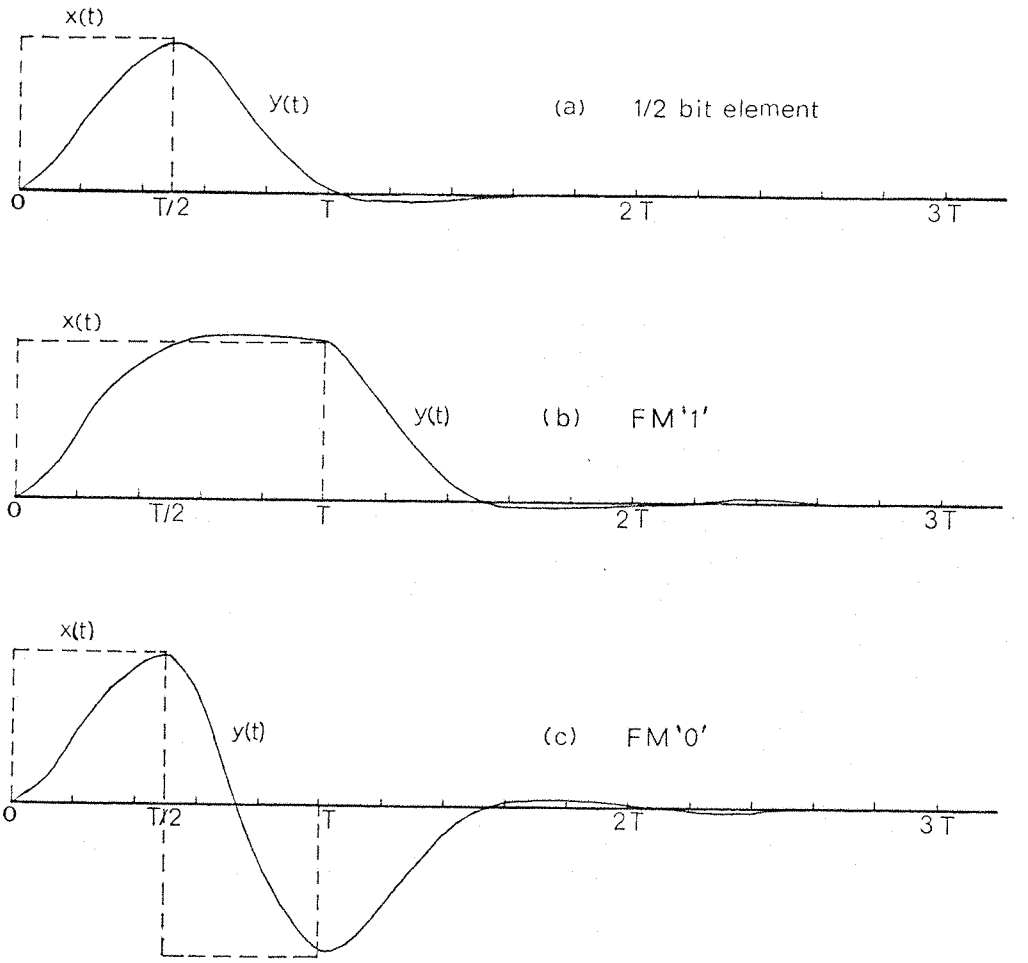
Message Undetectable Error Rate In FM Code

FIG 2.21



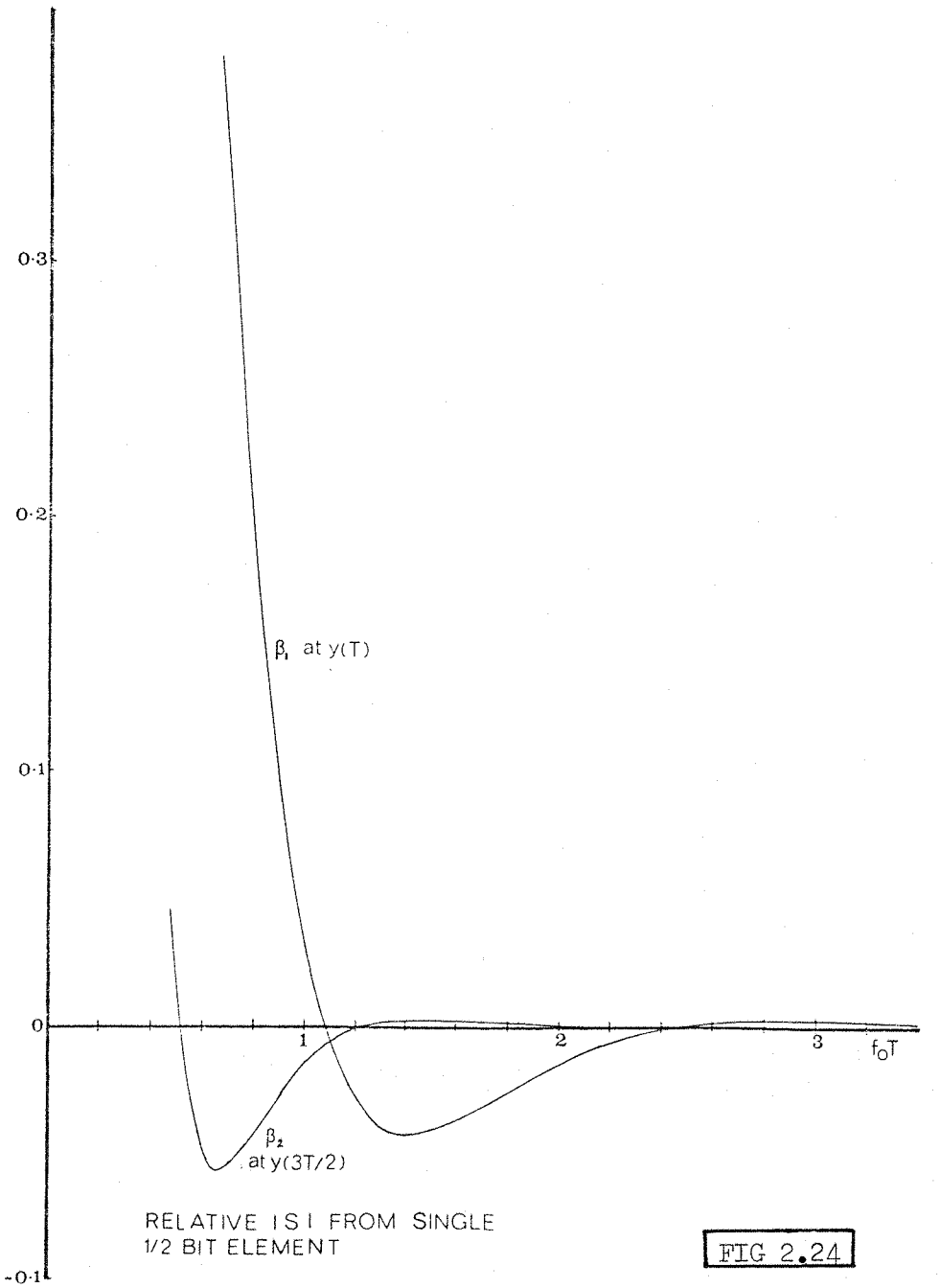
Variation of Filter Cut-Off Frequency

FIG 2.22



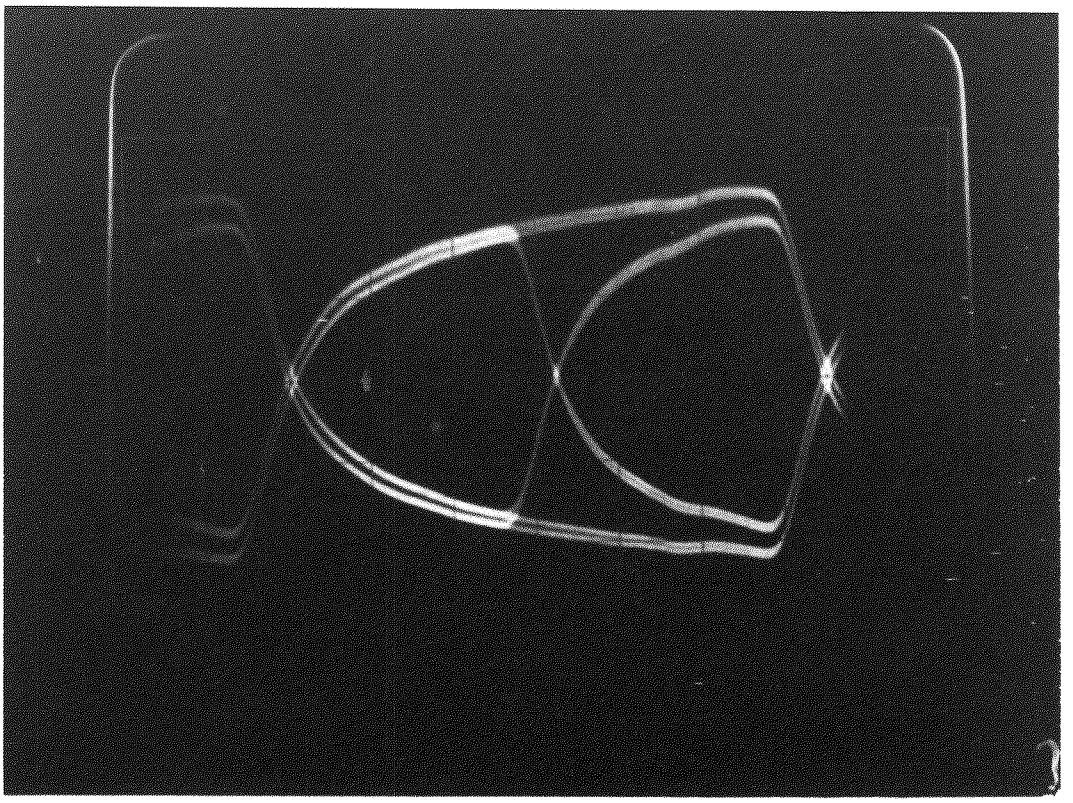
CALCULATED FILTER OUTPUT WAVEFORMS FOR $f_0T=1$

FIG 2.23



RELATIVE I S I FROM SINGLE 1/2 BIT ELEMENT

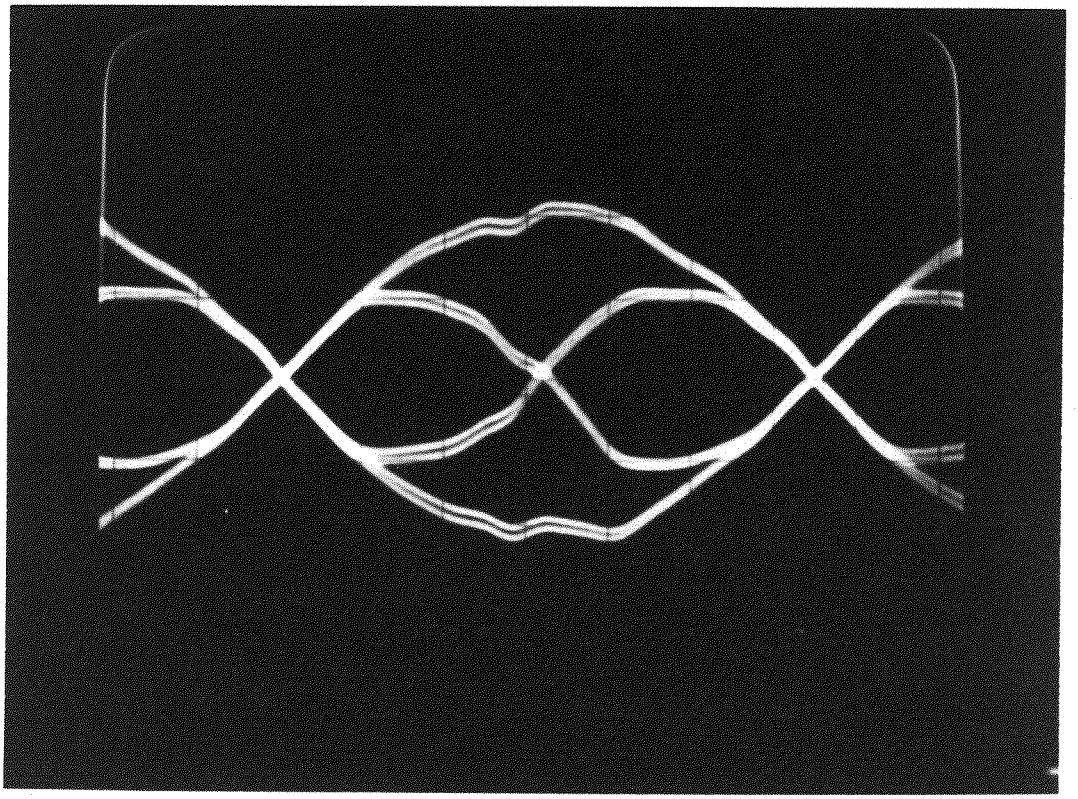
FIG 2.24



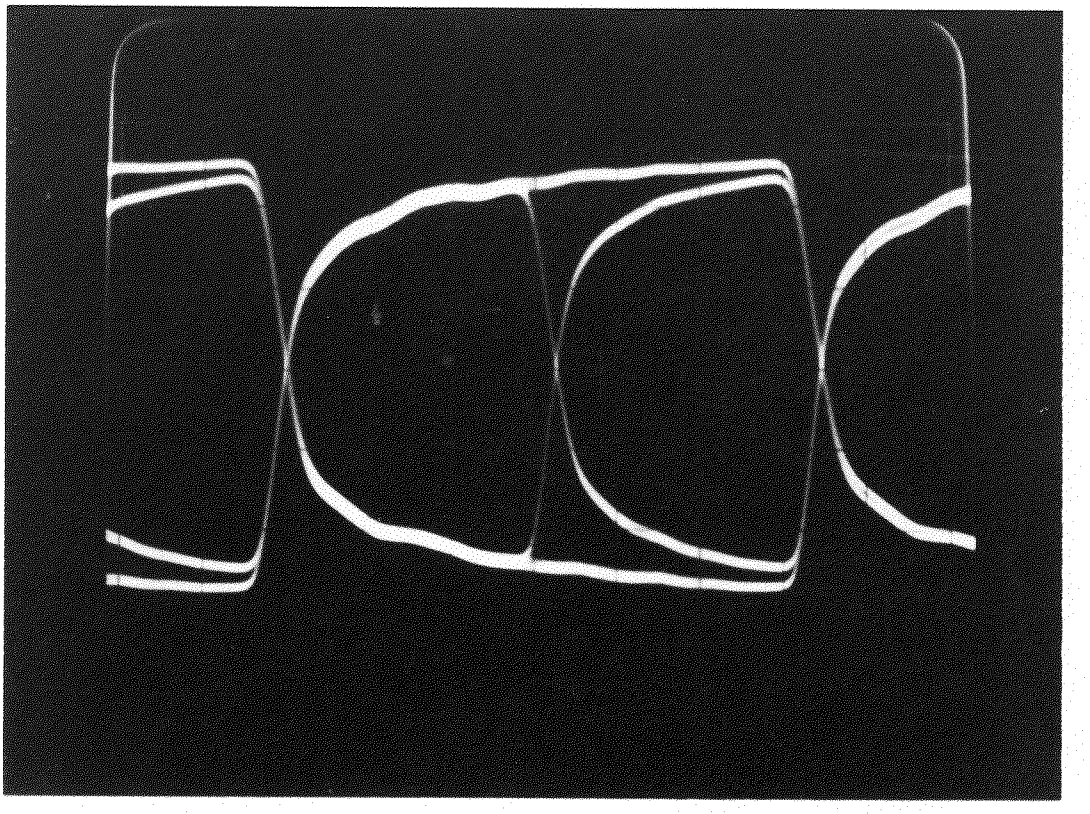
Filter Input

Filter Input and Output Eye Patterns for $f_o T=1$, at 6Mb/s

FIG 2.25(a)



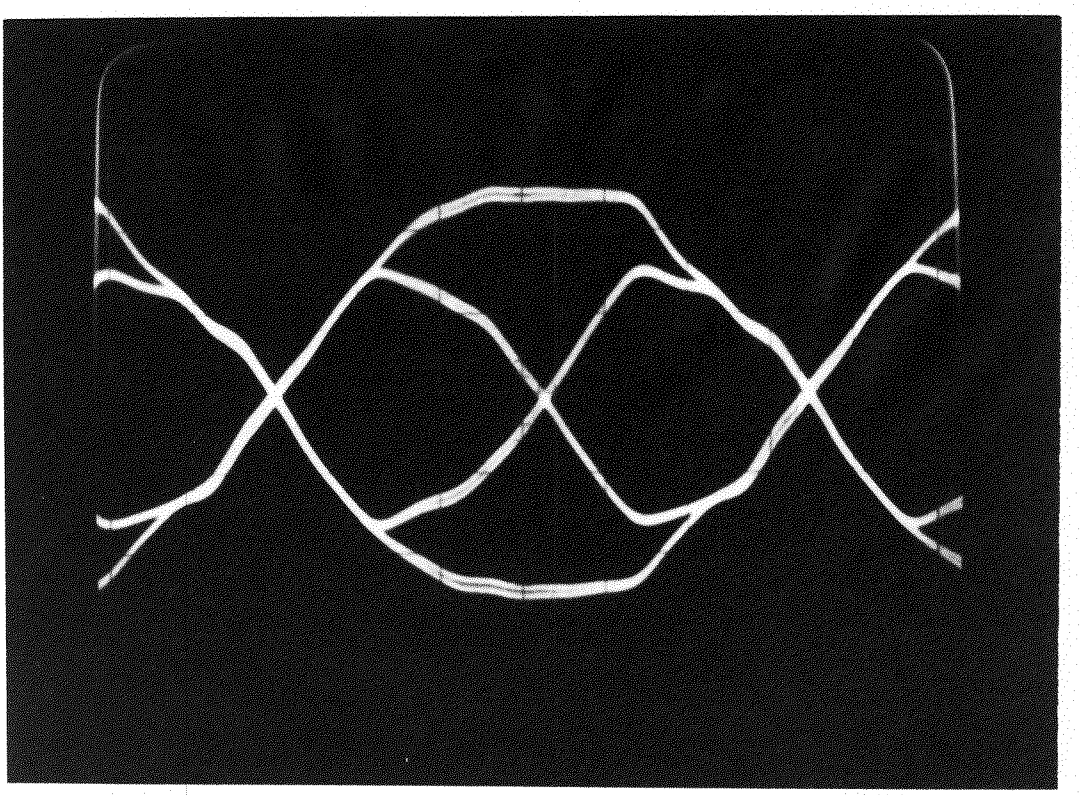
Filter Output



Filter Input

Filter Input and Output Eye Patterns for $f_o T=1$, at 3Mb/s

FIG 2.25(b)



Filter Output

3. EXPERIMENTAL LOADING STUDIES

3.1 Introduction

Studies carried out during the initial phase to identify the effects of loading a length of transmission line (100m of DRM 68 twin axial cable) with a relatively large number (greater than ten) of high impedance loads representing terminals on a passive highway system and carrying baseband signal with FM or PM coding are described in this chapter. In particular how transformer coupling of receiving terminals affect performance is investigated.

Two simple theories which attempt to predict cumulative attenuation caused by mismatching of the line at the load points and also the overall frequency response in the transformer coupled case are presented. The shortcomings of these simplified models of the highway, used for the initial design and performance prediction is outlined.

3.2 Theory

3.2.1 Mismatch Attenuation

The mismatch attenuation caused by resistive loads is taken into account by the cumulative mismatch theory presented in (2). This simple theory neglects any interference effects caused by multiple reflection and gives the total mismatch attenuation (in dB) of N resistive loads as

$$A_N = 20N \log \left(1 + \frac{R_o}{2R_L}\right) \qquad (3.1)$$

where

R_o = line characteristic impedance

R_L = load resistance.

A derivation of equation 3.1 is given in Appendix I.

In addition to the mismatch attenuation there is, of course, the line loss A_L (in dB) which depends on the type of cable, the line length and the data bit rate. Thus the total attenuation (A_T) is given by

$$A_T = A_L + 2ON \log \left(1 + \frac{R_o}{2R_L}\right) \tag{3.2}$$

3.2.2 Frequency Response

The effect of the inductive component of the transformer load, neglected by the above mismatch theory, was taken into account by an approximation of the highway which assumes the transformer loads to be effectively connected in parallel across a single finite impedance source. The effect of interwinding and stray capacities of the load are assumed negligible.

The low and high cut-off frequencies of a number of identical transformers connected in such an arrangement have been found to be given by :

$$f_L = \frac{R_L}{2\pi L_p} \left(\frac{1}{1 + \frac{R_L}{NR_o}}\right) \tag{3.3}$$

$$f_H = \frac{R_L}{2\pi L_K} \left(1 + \frac{NR_o}{R_L}\right) \tag{3.4}$$

where

L_p = primary self-inductance
L_K = primary referred leakage-inductance

Derivations of Equation 3.3 and 3.4 are given in Appendix (J).

It will be seen that both cut-off frequencies increase with N but for the low frequency there is an upper bound, i.e.

$$\lim_{N \to \infty} f_L = \frac{R_L}{2\pi L_p}$$

Interpretation of Results

The above results show that in the passive highway arrangement the individual frequency responses of the transformer loads interact to produce an overall response that is different from that of the single load. Further degradation of the transmitted signal thus results, in addition to that caused by transmission line effects.

It has been found that in practice it is the low cut-off frequency relationship which is more important. This is because the stray and interwinding capacities (neglected in the analysis) and to a greater degree the transmission line, limit the high cut-off frequency.

Experimental simulation of the transformer loading effect using a variable single-pole high-pass filter network showed that for PM and FM transmitted data, a maximum low cut-off frequency of not more than 10% of the data bit rate is tolerable.

3.2.3 Calculations

The following parameters were used to find the minimum permissible values of transformer load resistance (R_L) and primary self-inductance (L_p) for the initial tests. A 100m length of DRM 68 cable at a data bit rate (f_b) of 3M b/s was to be used.

$N = 50$

$R_o = 100$

$A_L = 2.5$ dB

$A_T = 6$ dB

$f_L = 90$ kHz (i.e. 3% of f_b)

The value of A_T is arbitrary and based on the transmitted voltage and a minimum receiver input voltage which must be far greater than the receiver threshold voltage.

Substituting the above set of values into Equations 3.1 and 3.3 gives

$$L_p = 4.671 \text{ mH}$$

$$R_L = 5.404 \text{k}\Omega$$

For convenience the nearest preferred value of 5.6 kΩwas used for R_L.

3.3 Experimental Tests

3.3.1 General

The procedures and results of initial tests carried out on a 100m length of DRM 68 cable to evaluate link performance with the connection of various numbers of either resistive and transformer coupled loads are described in this section.

Figure 3.1 shows the resistive and transformer coupled loads used for the tests. These have been designed using the results of Section 3.2.3. The filter was designed to give $f_o T$ of unity as explained in Chapter 2.4.1.

3.3.2 Measurement System

The measurement system for all the tests comprised the basic link set up described in Chapter 2.3.2 (see Figure 2.6), for error rate measurements. Minor modifications were however made to cater for the attenuation and low frequency response measurements.

The line was also broken up into random sections with 5m minimum length between sections for connection to the terminal loads.

Low Frequency Response

Figure 3.2 shows a block diagram of the set up for low frequency response tests of the transformer coupled loads. Sinewave signals from a video oscillator were differentially coupled onto one end of the line via the noise amplifier described in Appendix D. An oscilloscope was connected to the receiving end of the line to monitor the received differential signals, using the algebraic add facility.

3.3.3 Test Procedures

All tests were carried out with the loads distributed on the 100m cable in all three modes namely uniform, random, and clustered, as shown in Figure 3.3.

Error Rate

Error tests were carried out as described in Chapter 2.3.2 using strobe detection decoder in the ideal clock mode and with a pseudo random data sequence at a rate of 3M b/s. The definition of the S/N ratio used is as given in Chapter 2.3.2.

For each number of loads connected, error rate measurements were made by selecting S/N ratios in appropriate steps and noting the corresponding error probability on the counter.

Attenuation

For the attenuation tests the data sequence was set to all zeros and was FM coded to give worst case line signal, i.e. a 3 MHz square wave.

The peak-to-peak transmitting end and receiving end voltages were monitored with an oscilloscope for each set of loads connected to the line. The total attenuation in dB was found by using the equation

$$A = 20 \log \frac{V_T}{V_R} \text{ dB}$$

where

V_R = pk-pk receiving end voltage

V_T = pk-pk transmitting end voltage

Low Frequency Response

In these tests for each number of transformer coupled loads connected the frequency of the sinewave signal was varied to find the constant mid-band response which was then noted on the oscilloscope at the receiving end. The frequency was then reduced until the displayed voltage was $1/\sqrt{2}$ of the mid-band value (i.e. -3dB). This value of cut-off frequency was noted from the oscillator setting.

3.3.4 Results

Loading Mode - Effect on Transmitted Signal

Results of the initial tests carried out with resistive loads showed that the link performance in terms of attenuation and waveform

distortion at the far end of the line is independent of the mode of loading, i.e. uniform, random or clustered. At intermediate points along the line however, reflections become apparent. The severity in this case is dependent on the mode of loading. Clustered load gives the worst distortion, followed by random and uniform loading respectively. Reduction in the severity of waveform distortion was realised with higher value of load resistance as expected.

Resistive Loading

Test results for attenuation and increase in S/N for a constant P_e are presented in the graphs of Figure 3.4 from which the following is observed :

(a) the experimental attenuation curve shows a linear relationship with number of loads which confirms the theoretical predictions of section 3.2.1; (also shown in Figure 3.4).

The deviation in gradient from the theoretical curve can be accounted for if a value of 110Ω is used for the line characteristic impedance instead of the nominal value of 100Ω assumed in Section 3.2.3. Previous measurements of various samples of DRM68 cable showed a variation between 100Ω and 120Ω so that 110Ω is quite likely. The difference in intercept between the theoretical and experimental results is explained by superimposed noise on the signal waveform, observed during the measurements and which introduced uncertainties in the estimation of the correct peak-to-peak signal voltage on the oscilloscope. The difference of about 0.3dB between the two intercepts, corresponding to a spread of about 3.5%, agrees with the observed superimposed noise excursions. It is thus probable that the measure of peak-to-peak voltage values during the resistive attenuation tests were optimistically estimated compared to the corresponding value used in the theoretical attenuation equation.

(b) comparison of the increase in S/N curves with the attenuation curve show that :

(i) there is also a linear relationship with N

(ii) gradients are very similar but

(iii) the intercepts are about 1 dB greater.

The difference in intercept was found to be due to intersymbol interference arising from the line distortion effect on the pseudo-

random PM and FM coded data signals.

Figure 3.5 shows the error rate P_e vrs S/N graphs for PM and FM coding, from which the increase in S/N curves were derived.

Transformer Coupled Filter Loads

Error rate vrs S/N curves for transformer coupled filter loading are shown in Figure 3.6. for PM and FM coding. Derived curves of increase of S/N for constant P_e are included in Figure 3.4. Figure 3.7 shows results for the low cut-off frequency response. It is observed from these graphs that :

(a) the curves of increase of S/N vrs number of loads are linear but with a larger slope and rather more scatter than the results for resistive loads ;

(b) the intercepts are about 1 dB down on the corresponding resistive loading results

(c) the experimental points for the low frequency response lie close to the theoretical curve which confirms the theoretical predictions of section 3.2.2.

In case (a) the greater scatter can be accounted for by the more variable nature of the transformer input impedance of approximately 5.6 KΩ(mainly resistive) at the filter mid-band. The larger slope of the curve has been found to be due to intersymbol interference effects of the transformer reactive components which had not been accounted for by the simple parallel-transformer theory.

The result of (b) accounts for the S/N improvement obtained at the filter output. Referring to the typical eye patterns at the output of the filter, as shown in Figure 2.25, it would appear that the reduction in the signal eye opening would give poorer S/N performance ; however the corresponding noise power reduction at

the filter output explains the result above.

In case (c) it is interesting to note that although the theory assumed all the transformers to be connected in parallel at the same point on the line, the experimental results were independent of the points of connection along the line.

The results presented graphically in Figure 3.4 are conveniently summarised in Table 3.1 below.

Curve	Intercept (dB)	Gradient (dB/load)	Attenuation or Incr. of S/N for 50 loads (dB)
Attenuation Exp	2.8	0.085	7.05
Th R_o = 100	2.5	0.077	6.35
Th R_o = 110	2.5	0.085	6.75
Incr of S/N			
Resistive FM	3.8	0.083	7.95
PM	3.7	0.083	7.85
Transformer FM	2.6	0.107	8.0
PM	2.4	0.107	7.5

Summary of Experimental Results TABLE 3.1

3.4 Conclusions

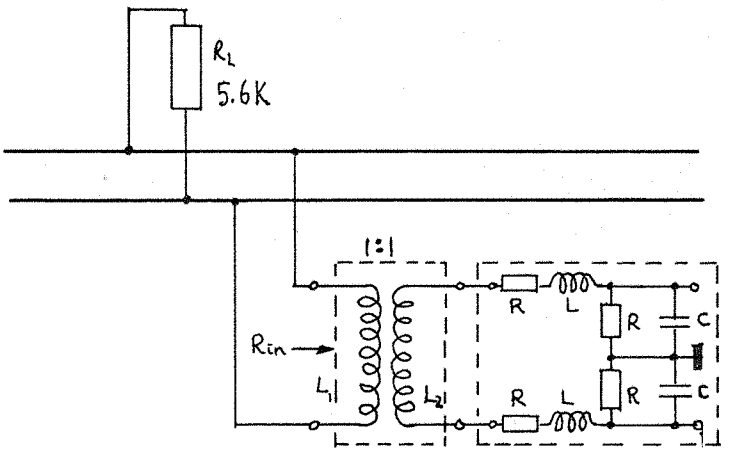
The simple theory proposed by CCL for the cumulative attenuation caused by multiple identical resistive loads has been shown to give quite accurate predictions for resistive loads.

The worst case attenuation is between the extreme terminals on a loaded line and has been found to be independent of the distribution of the intervening terminals.

The increase of low cut-off frequency with the number of loads behaved as predicted. This means that as the number of terminals on a passive highway is increased the primary inductance has to be increased.

For transformer loads it is found that the rate of increase of loss with number of loads is greater than predicted. This result identifies the main defect in the design and prediction of performance of transformer loads using the above simple theories.

Computer simulation studies carried out to investigate further the effect of transformer loads on the performance of the highway are described in the next chapter.



TRANSFORMER

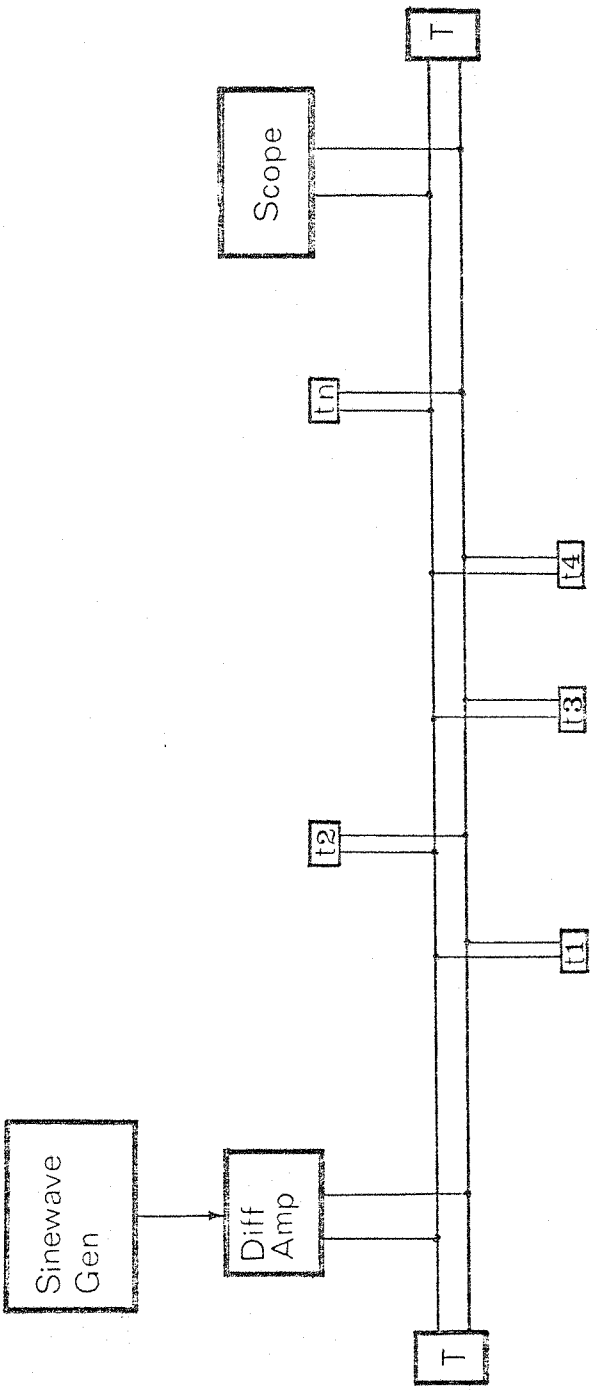
POT CORE TYPE: T38
$N_1 = N_2 = 30T$
$L_1 = L_2 = 4.77mH$
$R_{in} \triangleq 5.6K\Omega$ (Nominal with Filter)

FILTER

TYPE: 2ND ORDER BUTTERWORTH
$f_o = 3MHz$
$R = 2.2K\Omega$
$L = 0.165\ mH$
$C = 34.1\ pF$

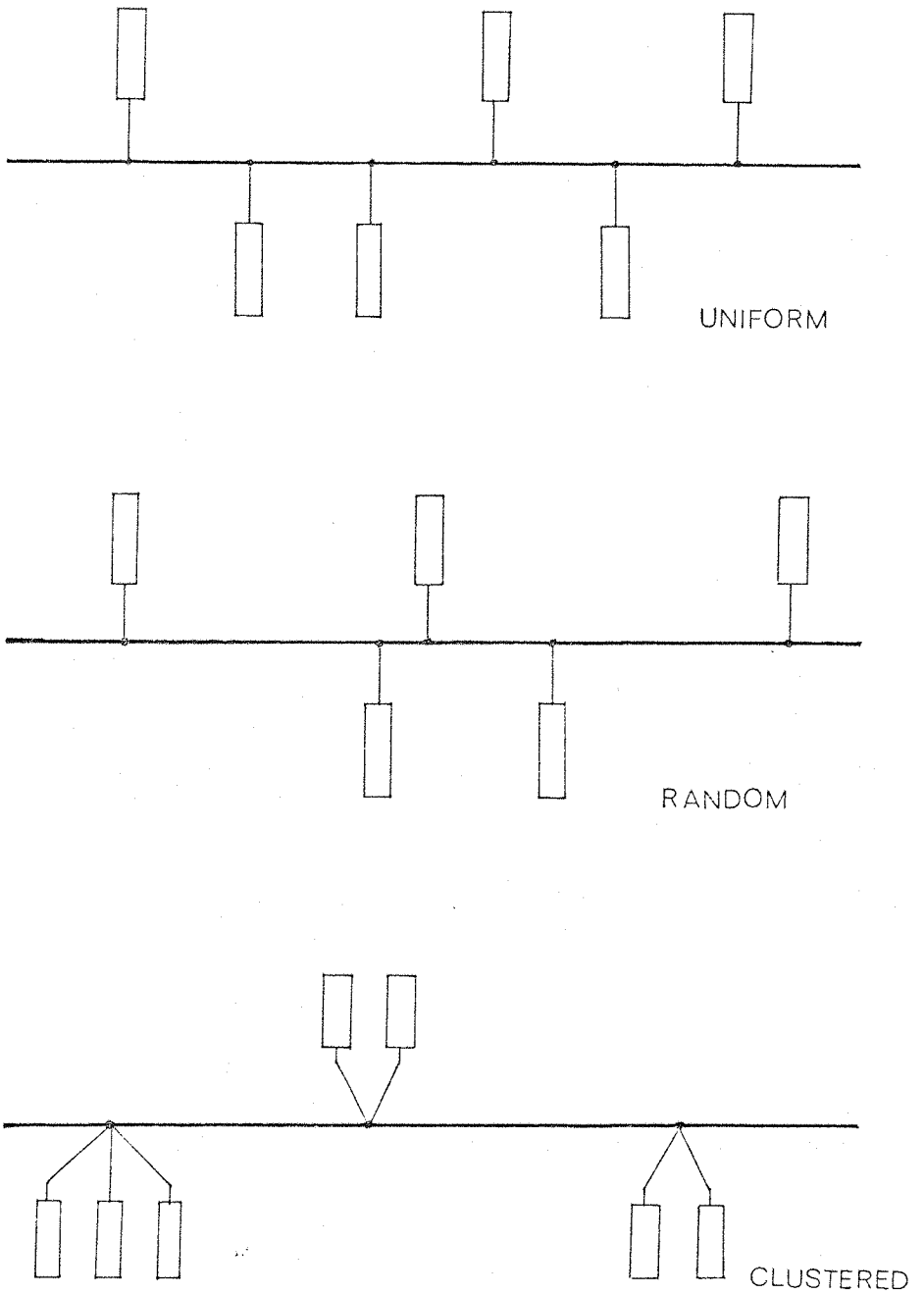
Resistive and Transformer Coupled Loads

FIG 3.1



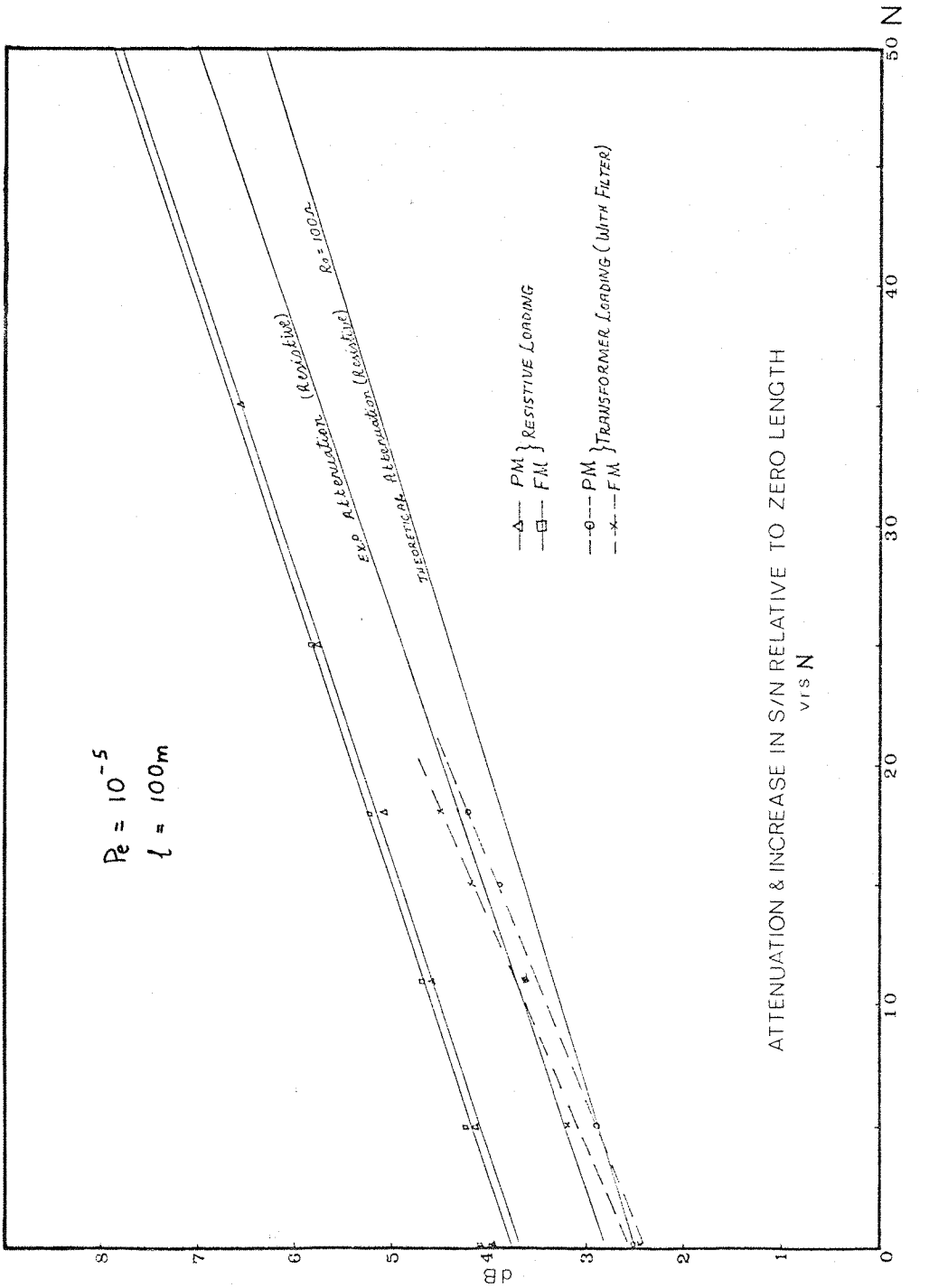
LOW FREQUENCY RESPONSE MEASUREMENT

FIG 3.2



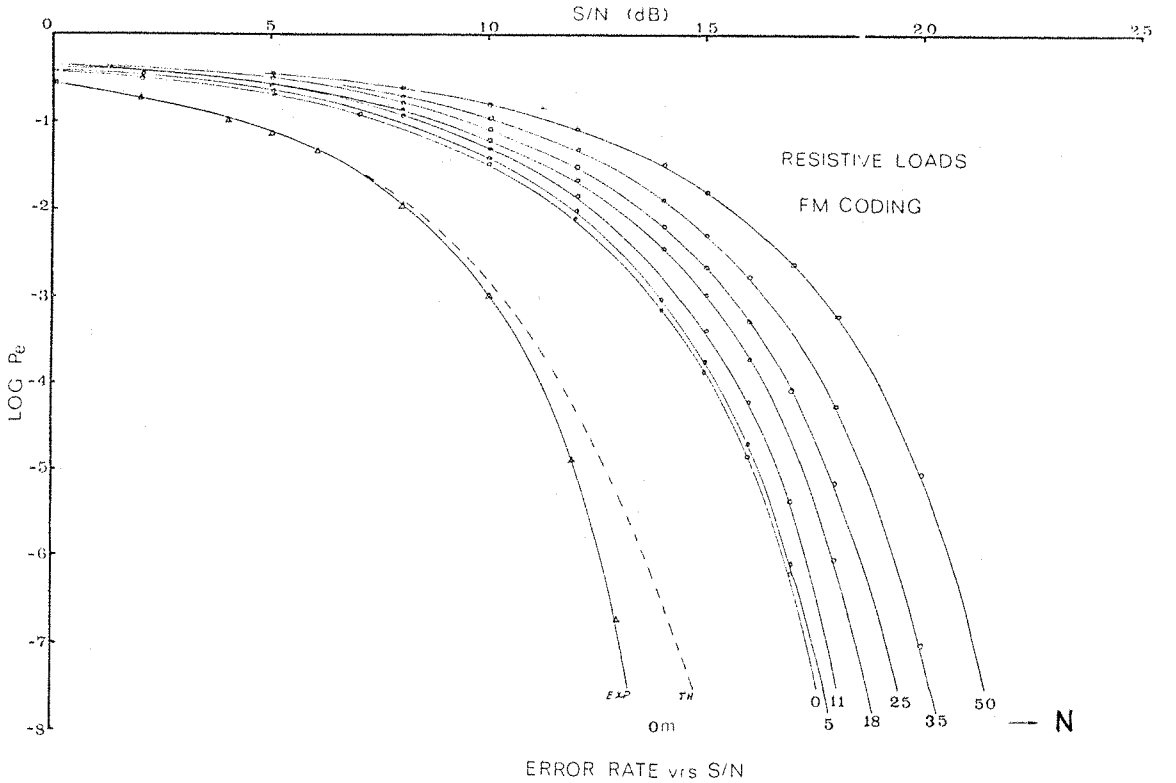
LINE LOADING MODES

FIG 3.3

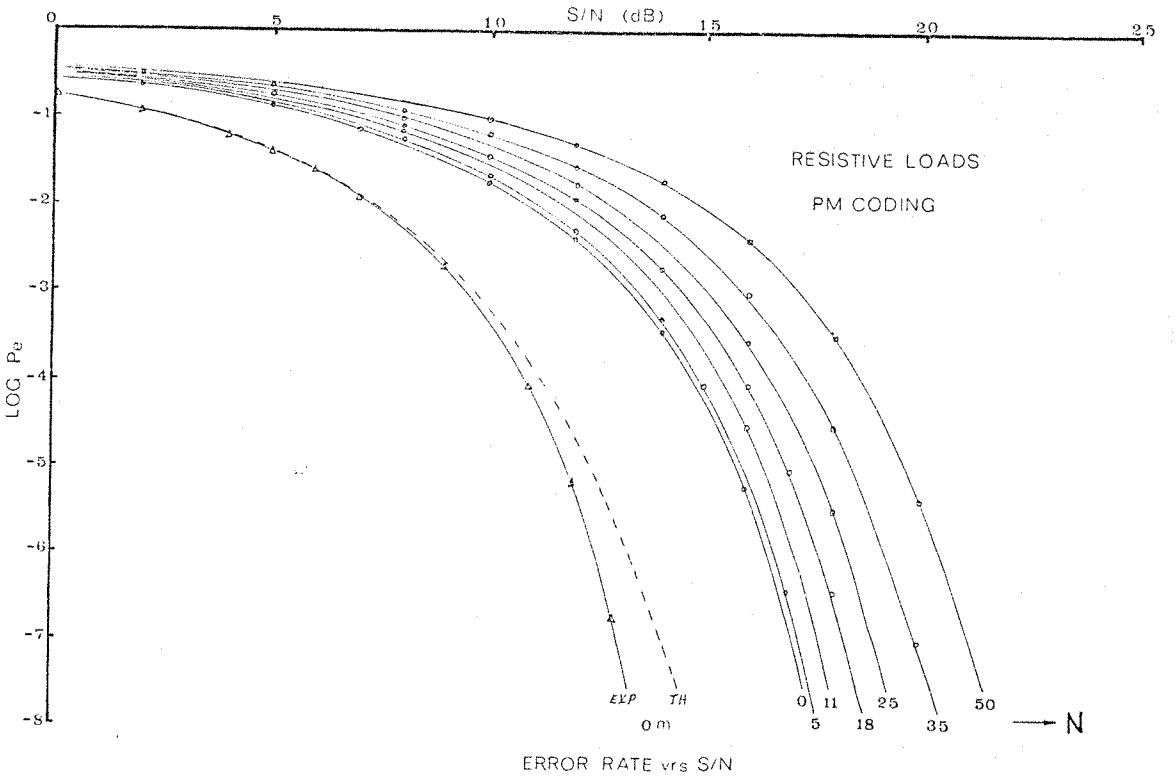


Attenuation & Increase In S/N Relative to Om

FIG 3.4



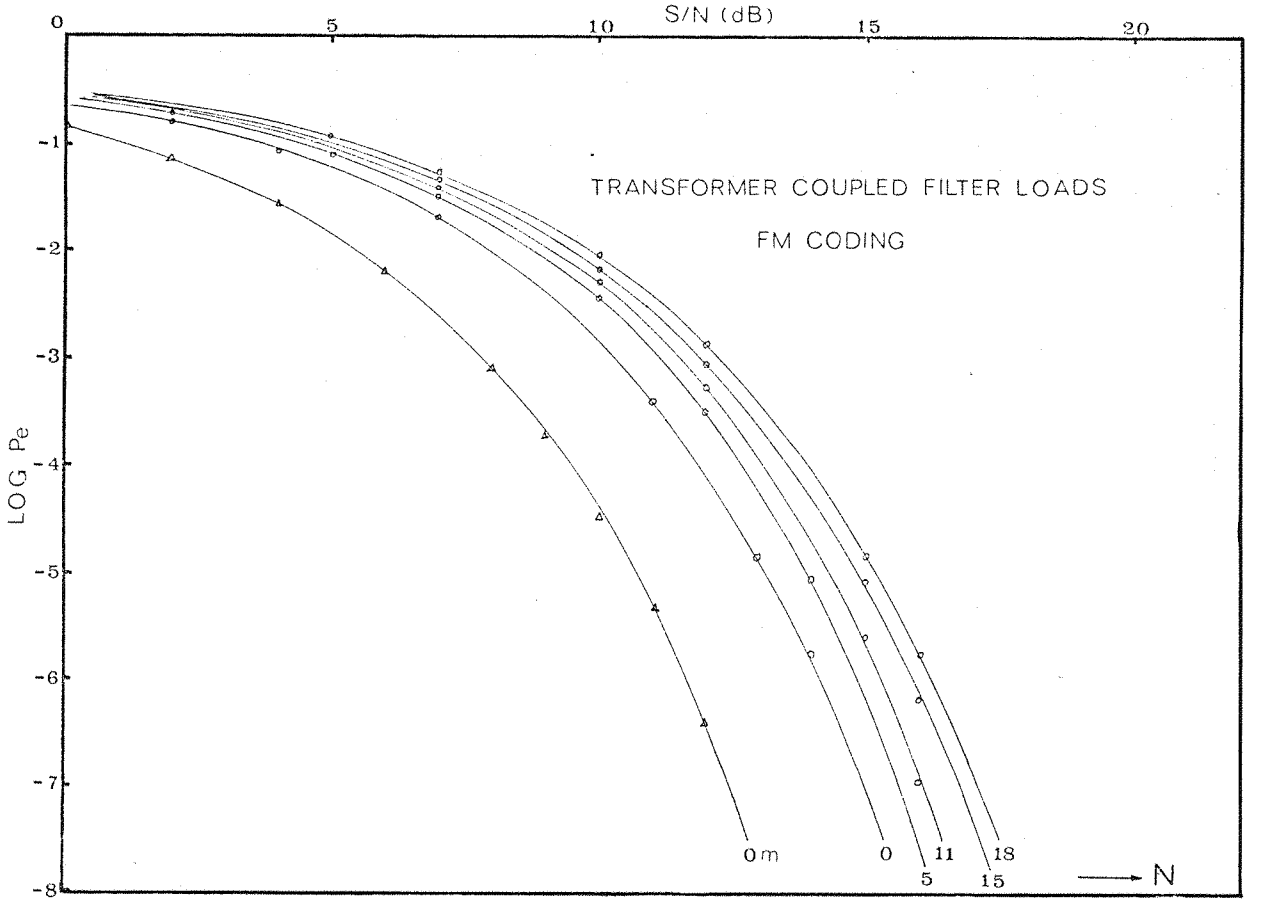
ERROR RATE vrs S/N

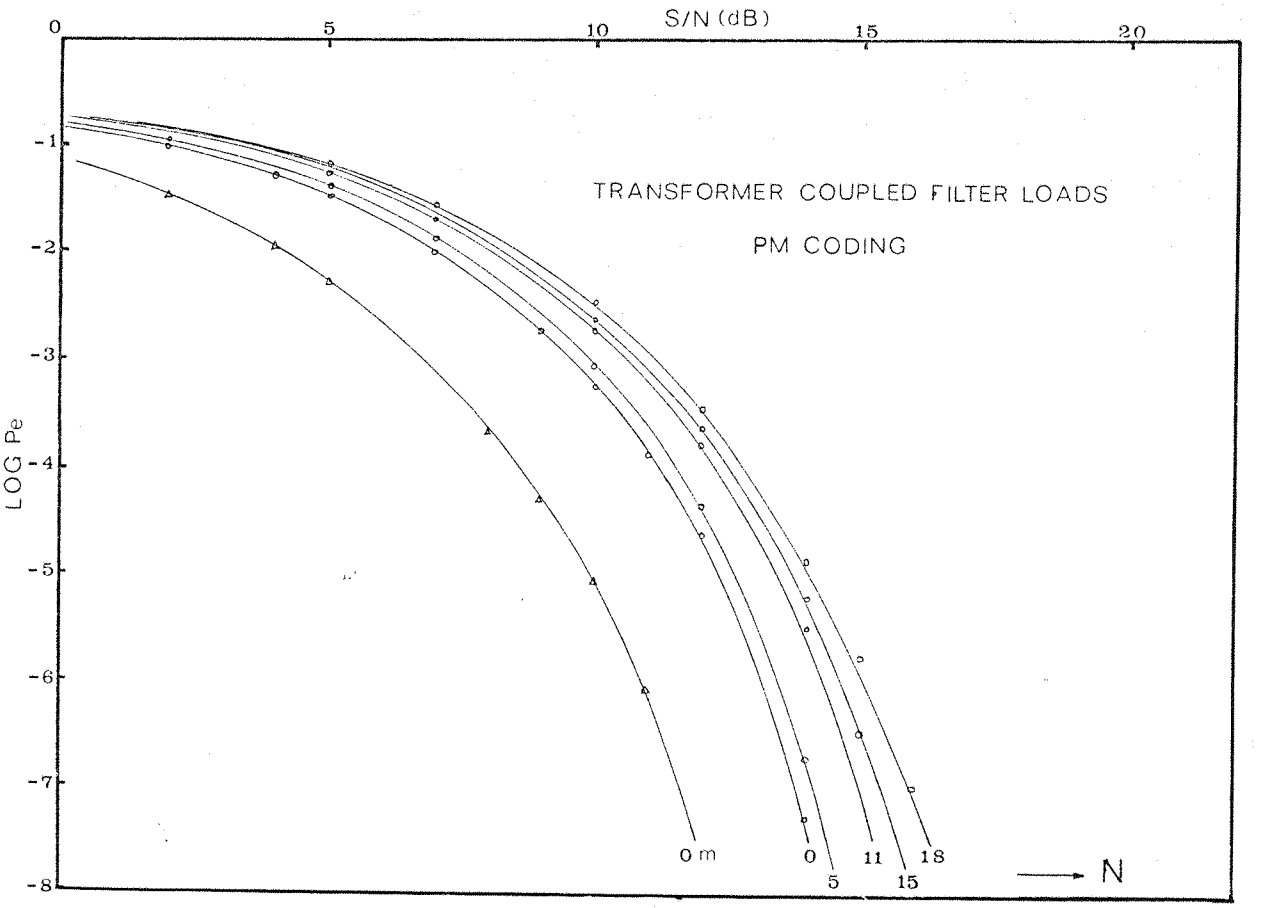


ERROR RATE vrs S/N

ERROR RATE:- Resistive Loads

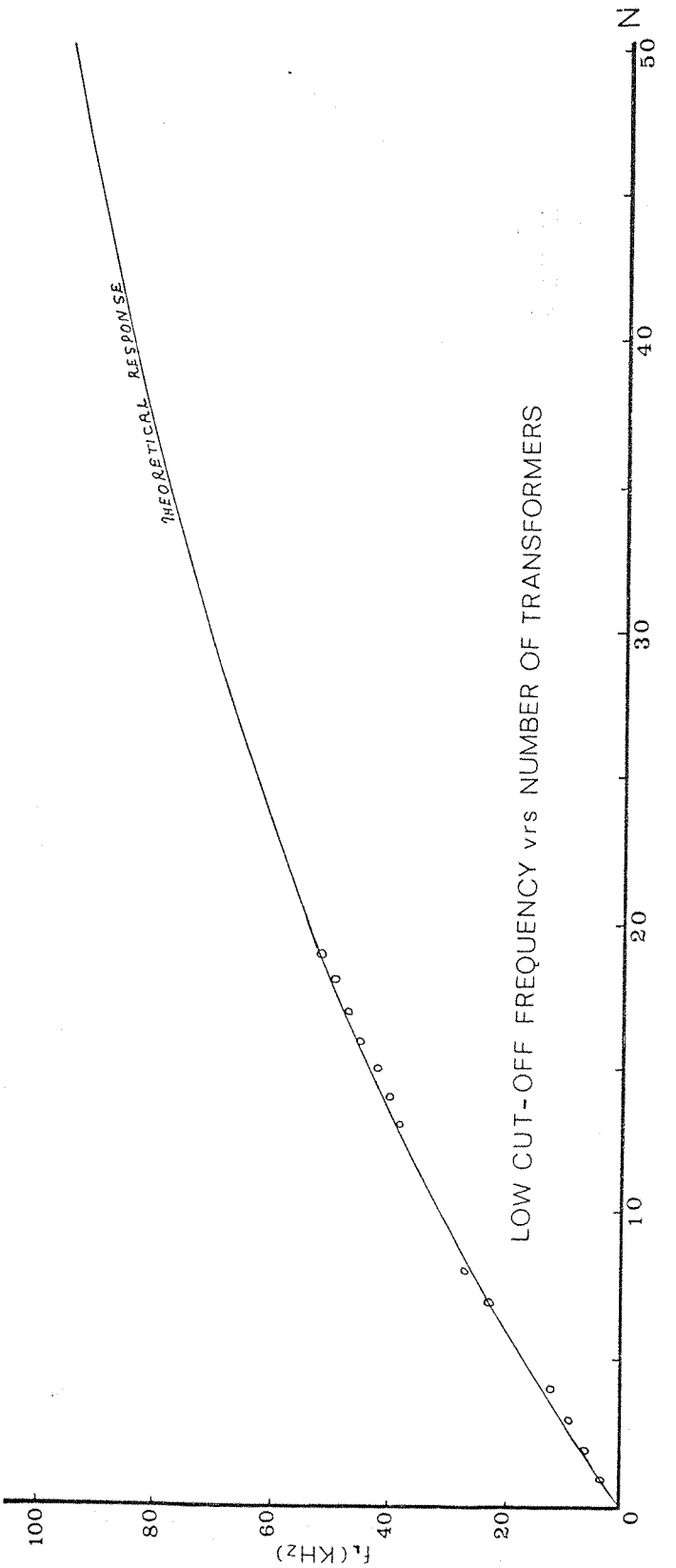
FIG 3.5





ERROR RATE:- Transformer Loads

FIG 3.6



Low Frequency Response of Transformer Loads

FIG 3.7

4. COMPUTER SIMULATION STUDIES

4.1 Introduction

The results obtained in Chapter 3 have shown that the connection of transformer coupled loads in the multiterminal passive highway environment degrades a transmitted signal more than has generally been thought possible. The ideal situation for identifying the causes of such degradation would be the physical system itself. However it would be appreciated that such an approach would require a great deal of physical effort, in addition to the lack of control over the load parameters for such investigations. It is in the light of these practical difficulties that a computer solution to the problem has been sought , through the study of the responses of the highway under various conditions of loading.

4.1.1 Review of existing methods

The passive highway arrangement is, in effect, a single transmission line with an arbitrary number of discontinuities at various points of the line. Theoretical prediction of received signal waveform for such an arrangement has been considered by Yao (15) and Polk (16), using Laplace transform methods. The analysis presented by both authors are however limited to lossless lines with RC discontinuities. These limitations arise because, when applied to the lossy line case, the Laplace transform method greatly increases the complexity of solution ; this complexity of solution is borne out in the analysis of lossy lines presented by Dvorak in (17).

4.1.2 Method of solution used

The method of solution used for the present investigation has been largely inspired by the numerical method first suggested by Dvorak (18). For this method the LC elements of the highway loads

are simulated by transmission lines with very small propagation delay T_s. The main transmission line is approximated by a cascade of small discrete sections such that their propagation delays are integer multiples of T_s. The transient behaviour of the resulting transmission line network is then described in the discrete time domain in terms of difference equations which are then solved using a digital computer. This method of solution is applicable to both lossy and lossless lines and also not limited by the type of load. Detailed explanation of the discrete modelling method is given in section 4.3.1.

For the purpose of comparison, the Laplace transform method considered by Yao (15) for capacitive discontinuities has also been used but extended to cover the more complex case of transformer coupled discontinuities.

Line Configuration

Figure 4.1 shows the loaded line configuration studied. The transmitter is positioned at one end of the line and the loads are tapped along the line. It was found experimentally (see Chapter 3) that this arrangement, with the receiver at the far end of the line, is the worst case condition.

Load Representation

The transformer coupled load is represented in the continuous time domain by an equivalent parallel RLC network. This representation of the transformer load makes possible the isolation of the individual contributions of the load components to the overall signal degradation.

Line Signal

All the studies have been carried out assuming a unit voltage

pulse of duration T/2, which represents a half-bit element of the PM and FM coded signals.

4.2 Laplace Transform Method

Let V = transmitted voltage
V_{rn} = received voltage at nth load
r_c = load reflection coefficient
T_o = load transmission coefficient
N = total number of loads
d_n = distance between loads n-1 and n
γ = propagation constant of line

Now assume all $d_n = d$,
(i.e. uniform loading situation).
Then, the received voltage at the nth load, neglecting reflections of second order has been found to be given by :

$$V_{rn}(s) = V(s)T_o(s)^n e^{-nd\gamma(s)} \left[1 + r_c(s) \sum_{k=1}^{N-n} T_o(s)^{2(k-1)} e^{2kd\gamma(s)}\right] \quad (4.1)$$

for $n < N$

At the Nth terminal i.e. the "far end" receiver,

$$V_{rN}(s) = V(s)\, T_o(s)^N e^{-Nd\gamma(s)} \quad (4.2)$$

4.2.1 Time Response

The time response at the "far end" receiver to the transmitted half-bit element pulse, assuming a lossless line, becomes :

$$\frac{V_{rN}(t)}{(2\tau_L)^N} = \sum_{k=O}^{N-1} \left[\frac{C_{N-k}}{\tau_1 (N-k-1)!} \left(\frac{t}{\tau_1}\right)^{N-k-1} e^{-\frac{t}{\tau_1}} + \frac{D_{N-k}}{\tau_2 (N-k-1)!} \left(\frac{t}{\tau_2}\right)^{N-k-1} e^{-\frac{t}{\tau_2}} \right] \quad (4.3)$$

$$- \sum_{k=O}^{N-1} \left[\frac{C_{N-k}}{\tau_1 (N-k-1)!} \left(\frac{t-T/2}{\tau_1}\right)^{N-k-1} e^{-\frac{t-T/2}{\tau_1}} + \frac{D_{N-k}}{\tau_2 (N-k-1)!} \left(\frac{t-T/2}{\tau_2}\right) e^{-\frac{t-T/2}{\tau_2}} \right]$$

where,

$$C_{N-k} = (-1)^{N+k-1} \frac{\tau_1}{(\tau_1 - \tau_2)^N} \sum_{p=0}^{k} \binom{N-1}{k-p} \binom{N+p-1}{p} \frac{\tau_2^{\,p}}{(\tau_1 - \tau_2)^p} \qquad (4.4)$$

$$D_{N-k} = (-1)^{N+k-1} \frac{\tau_2}{(\tau_2 - \tau_1)^N} \sum_{p=0}^{k} \binom{N-1}{k-p} \binom{N+p-1}{p} \frac{\tau_1^{\,p}}{(\tau_2 - \tau_1)^p} \qquad (4.5)$$

and,

$$\tau_1, \tau_2 = \frac{\tau_L}{r_o} \left[1 \pm (1 - r_o^{\,2} \frac{\tau_c}{\tau_L}) ^{\frac{1}{2}} \right] \qquad (4.6)$$

given that,

$$\tau_L = \frac{L_L}{R_o}$$

$$\tau_c = R_o C_L \qquad (4.7)$$

$$r_o = \frac{1}{1 + \frac{R_o}{2R_L}}$$

Equations 4.3 through 4.7 have been programmed in FORTRAN language for the ICL 2970 computer.

Results of loading studies using this program is presented in section 4.4. The storage and run times required for a maximum of 19 loads are 20 K byte and 75 s respectively.

Limitations

In theory, any number of loads and combinations of the R_L, L_L, and C_L values of the load may be analysed. However, it was found out that this was not generally the case ; because of the problem

of "overflow", when τ_1 or τ_2 is very small. It was thus found necessary to include some "checks" in the program to minimise the frequency of occurrence. The number of loads and choice of load values was thus limited by the stability problem associated with this method of solution.

4.3 Numerical Method

4.3.1 Principles

The theoretical principles of the numerical method used for simulation of the loaded highway is described in this section.

Transmission Line Modelling

Consider a lossy uniform line with its resistance, inductance capacitance and conductance per-unit-length designated as R, L, C and G, respectively. The partial differential equations for such a line is known to be given as (19)

$$L \frac{\partial i}{\partial t} + Ri + \frac{\partial v}{\partial x} = O \qquad (4.8)$$

$$C \frac{\partial v}{\partial t} + Gv + \frac{\partial i}{\partial x} = O \qquad (4.9)$$

where $v(x, t)$ and $i(x, t)$ are the voltage and current respectively at each point x along the line and at each instant of time t. The method of solving these equations, known as the method of characteristic in the literature (20), is based on a transformation in the x-t plane which accomplishes the conversion of Equations 4.8 and 4.9 into a pair of ordinary differential equations, which define the forward or incident wave and the backward or reflected wave, respectively.

The transformation uses the equations

$$\frac{dx}{dt} = \frac{1}{\sqrt{LC}} \qquad (4.10)$$

$$\frac{dx}{dt} = -\frac{1}{\sqrt{LC}} \qquad (4.11)$$

where $1/\sqrt{LC}$ is the phase velocity of the travelling wave.

The relationship between the partial derivatives of Equations 4.8 and 4.9 and the corresponding ordinary derivatives is given by

$$\frac{dv}{dt} = \frac{\partial v}{\partial t} + \frac{\partial v}{\partial x}\frac{dx}{dt} \qquad (4.12)$$

$$\frac{di}{dt} = \frac{\partial i}{\partial t} + \frac{\partial i}{\partial x}\frac{dx}{dt} \qquad (4.13)$$

See chapter 15 of (21).

By appropriately combining equations 4.10 through 4.13 with Equations 4.8 and 4.9, the following ordinary differential equations are obtained :

$$\frac{d}{dt}\left[v(x,t) + \sqrt{\frac{L}{C}}\, i(x,t)\right] = -\left[\frac{G}{C}\, v(x,t) + \frac{R}{\sqrt{LC}}\, i(x,t)\right] \qquad (4.14)$$

$$\text{for } \frac{dx}{dt} = 1/\sqrt{LC}$$

$$\frac{d}{dt}\left[v(x,t) - \sqrt{\frac{L}{C}}\, i(x,t)\right] = -\left[\frac{G}{C}\, v(x,t) - \frac{R}{\sqrt{LC}}\, i(x,t)\right] \qquad (4.15)$$

$$\text{for } \frac{dx}{dt} = -1/\sqrt{LC}$$

Equations 4.14 and 4.15 represent the transformed differential equations of the line, in the continuous time domain, for the incident and reflected waves respectively.

Discrete Solution

Let d = an incremental distance travelled by the wave
T_s = corresponding incremental time

See Figure 4.2 (a). The two heavy lines represent the forward

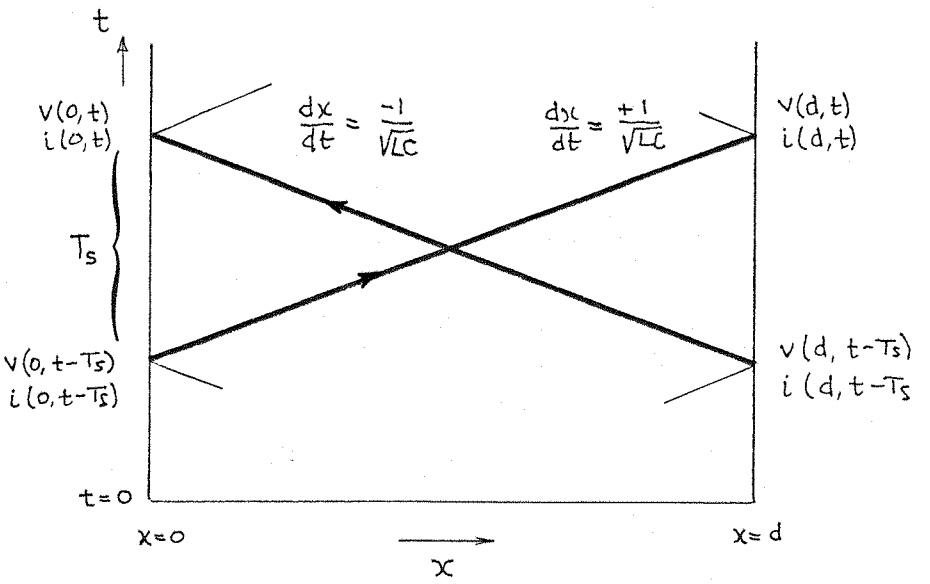


Fig 4.2a

Characteristic Curves for a Uniform Line

and backward characteristics of the travelling wave along the line. Since d and T_s are small we may write,

$$dv = \Delta v, \quad di = \Delta i, \quad dt = T_s$$

where, Δv = difference between the voltages at the end points on a given characteristic,

Δi = corresponding difference between the currents at the same two points,

and T_s = the incremental time.

Consider the wave travelling along characteristic $1/\sqrt{LC}$, then

$$\Delta v\,(t) = v(d, t) - v(O,\ t-T_s)$$

$$\Delta i(t) = i(d, t) - i(O, t-T_s) \qquad (4.16)$$

Similarly, for the wave travelling along characteristic $-1/\sqrt{LC}$, we have

$$\Delta v(t) = v(O,t) - v(d, t-T_s)$$
$$\Delta i(t) = i(O,t) - i(d, t-T_s) \qquad (4.17)$$

Substituting equations 4.16 and 4.17 into Equations 4.14 and 4.15 respectively and putting $dt = T_s$, we obtain after some rearrangements,

$$v(d,t) + \sqrt{\frac{L}{C}}\, i(d,t) = v(O, t-T_s)\left[1 - \frac{G}{C}T_s\right] + i(O, t-T_s)\left[\sqrt{\frac{L}{C}} - \frac{RT_s}{\sqrt{LC}}\right] \qquad (4.18)$$
$$v(O,t) - \sqrt{\frac{L}{C}}\, i(O,t) = v(d, t-T_s)\left[1 - \frac{GT_s}{C}\right] - i(d, t-T_s)\left[\sqrt{\frac{L}{C}} - \frac{RT_s}{\sqrt{LC}}\right]$$

Difference Equations

If the uniform line of length ℓ, is divided into a discrete number of M small sections such that the length and propagation delay of each small section is d and T_s respectively ; and if the corresponding nodes between sections are denoted by the integers 1, 2, ..., m, m+1, ...M. Then we may rewrite Equations 4.18 as

$$v_{m+1}(t) + \sqrt{\frac{L}{C}}\, i_{m+1}(t) = v_m(t-T_s)\left[1 - \frac{G}{C}T_s\right] + i_m(t-T_s)\left[\sqrt{\frac{L}{C}} - \frac{RT_s}{\sqrt{LC}}\right]$$
$$v_m(t) - \sqrt{\frac{L}{C}}\, i_m(t) = v_{m+1}(t-T_s)\left[1 - \frac{GT_s}{C}\right] - i_{m+1}(t-T_s)\left[\sqrt{\frac{L}{C}} - \frac{RT_s}{\sqrt{LC}}\right] \qquad (4.19)$$

Let r = resistance of each small line section
g = conductance of each small line section
and R_o = line characteristics impedance (for a lossless line)

Then we can write,

$$r = \frac{RT_s}{\sqrt{LC}}, \quad g = \frac{G\,T_s}{\sqrt{LC}}, \quad R_o = \sqrt{\frac{L}{C}}$$

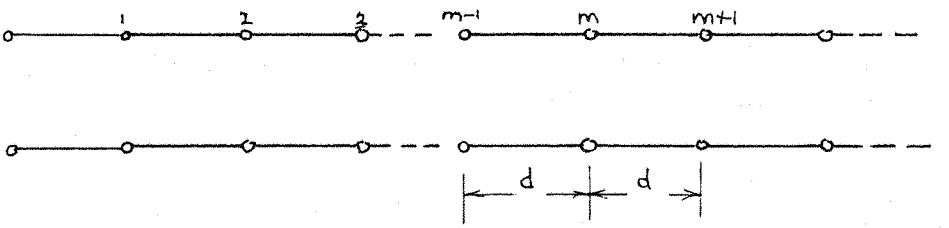
Substituting the above equations into Equation 4.19 we obtain,

$$v_{m+1}(t) + R_o i_{m+1}(t) = (1 - gR_o)v_m(t-T_s)+(R_o-r)i_m(t-T_s)$$
$$v_m(t) - R_o i_m(t) = (1-gR_o)\, v_{m+1}(t-T_s)-(R_o-r)i_{m+1}(t-T_s) \qquad (4.20)$$

Equation 4.20 is the set of difference equations of a very short lossy line in the time domain. It describes the forward and backward travelling waves respectively between the two nodes m and m+1 of the short line section.

Solution of Line Voltages and Currents

Consider the node m along the line (see Figure 4.2 (b)). Then the difference equations describing the forward and backward waves travelling between node m and node m+1 are as given by equation 4.20.



Discrete Line Sections

Fig 4.2b

Similarly we can describe the forward and backward travelling waves between node m-1 and node m by the set of difference equations given by :

$$v_m(t) + R_o\, i_m(t) = (1-gR_o)v_{m-1}(t-T_s) + (R_o - r)i_{m-1}(t-T_s)$$

$$v_{m-1}(t) - R_o\, i_{m-1}(t) = (1-gR_o)v_m(t-T_s)-(R_o-r)i_m(t-T_s) \qquad (4.21)$$

The equations 4.20 and 4.21 are simultaneously solved for $v_m(t)$ and $i_m(t)$. The v, i values so calculated at node m at time t are used as initial values in calculating the v, i values at the next node m+1.

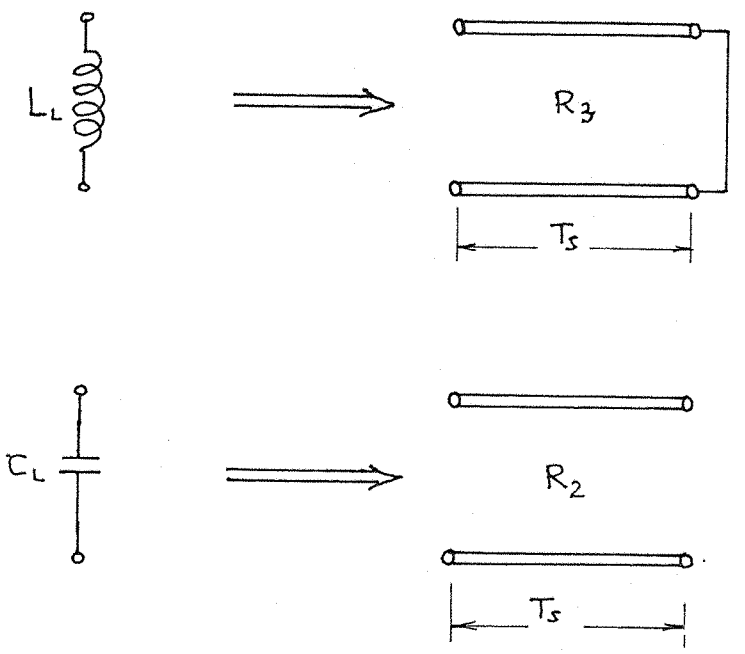
The initial conditions are stored in memory before starting solution.

Lumped Network Simulation

The lumped quantities L_L and C_L of any network can be approximated by distributed quantities in the form of lossless transmission lines provided that the total delay T_s of these lines is small enough (18). When this condition is satisfied, the equivalent characteristic impedances of the lumped L_L and C_L quantities are respectively given by

$$R_2 = T_s/C_L \qquad R_3 = L_L/T_s$$

See Figure 4.2 (c).



Transmission Line Model of Lumped L and C

Fig. 4.2c

The additional error capacitance and inductance introduced by the model is given by

$$C' = T_s^2/L_L \qquad L' = T_s^2/C_L$$

Thus for small T_s these additional elements become negligible. The equivalent transmission lines can thus be described by similar difference equations as given by Equations 4.20 and 4.21, but in this case, for the loss less line.

Application of the discrete transmission line models to the loaded highway situation is described in the following sections.

4.3.2 Model Description

Figure 4.3 illustrates the discrete-transmission line model of the basic highway configuration shown in Figure 4.1. Using

the principles described above, the length of each section of line connecting the loads is divided into an integral number of elementary sections of the same delay T_s. The parallel capacitance C_L is replaced by the equivalent lossless open-circuited transmission line in series with the main line and the paralled inductive load L_L is replaced by an equivalent lossless short-circuited line connected across the main line.

The equivalent characteristic impedances of the capacitive and inductive loads are respectively defined as

$$R_2 = \frac{T_s}{C_L} \tag{4.22}$$

and

$$R_3 = \frac{L_L}{T_s} \tag{4.23}$$

4.3.3 Model Solution Techniques

The model of Figure 4.3 is divided into four blocks which define sections of similar configurations. These blocks comprise the sending-end, transmission line, loads, and the termination as shown in Figure 4.4.

Six sets of difference equations, derived from the points labelled A to F, are used to completely describe the highway model.

Nodal Assignments

The nodes of elementary sections of the cascaded transmission lines (each of delay T_s), in each line-block are assigned values from 1 to M + 1, where M is the total number of elementary sections within the line-block. See Figure 4.5. Each load position is defined by the last node of the preceding block and the first node of the next block.

The first node of line-block 1 defines the input terminal point and the last node of line-block (N+1) defines the position of the line termination.

Variable Definitions

Three dummy variables (n, m, t) uniquely define the voltage (v) and current (i) at each node of the basic segments of transmission line making up the model :

n = block number
m = node number within block
t = time variable

General Line Variable

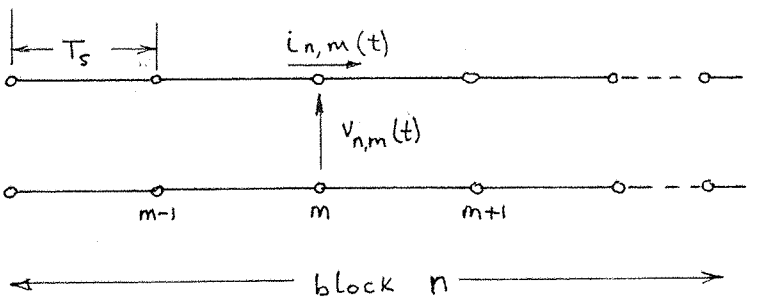
The voltage and current at a node m within block n at the time instant t thus becomes

$$v_{n,\,m}(t)$$

and

$$i_{n,\,m}(t)$$

respectively. See Figure 4.6.



Voltage and Current Variables at a Node Fig. 4.6.

For convenience of the numerical solution, t is represented by

$$t = k . T_s$$

where k is an integer and T_s is the basic time delay between nodes. Defined this way, the fixed quantity T_s may be dropped so that the voltage and current definitions become

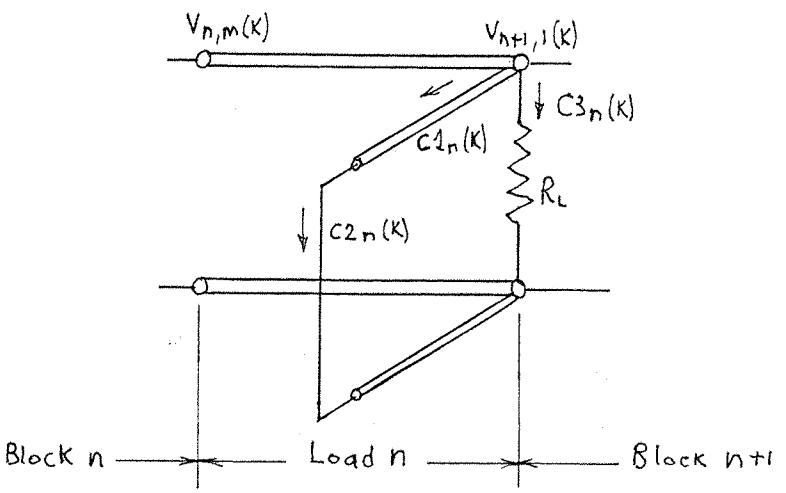
$$v_{n,m}(k)$$

and

$$i_{n,m}(k).$$

Load Variables

At the load points three additional variables (C1, C2, C3) define the currents due to the parallel branches formed by the resistive and inductive components of the load. In this case only the two dummy variables n and k are required to uniquely define the position of the loads. See Figure 4.7.



Voltage and Current Variables at a Load

Fig. 4.7.

$C1_n(k)$ = branch current into inductive load

$C2_n(k)$ = short circuit current in inductive load

$C3_n(k)$ = branch current into resistive load

Input Current

The input current is defined by the values of its amplitude at discrete time instants given by T_s, $2T_s$, ..., KT_s, ... T ; where T is the bit period, i. e.

$$I(k)$$

4.3.4. Algorithm

From the voltage and current definitions given in section 4.3.3, the six difference equations describing the complete highway model (see section 4.3.2) are determined from the points labelled A through F in figure 4.4 respectively. The respective definitions assigned to these equations are given as :

$v_{1,1}(k)$, $i_{1,1}(k)$ = input boundary equations

$v_{n+1}(k)$, $i_{n+1,1}(k)$ = first node of line equations

$v_{n,m}(k)$, $i_{n,m}(k)$= general line equations

$v_{n,M+1}(k)$, $i_{n,m+1}(k)$ = last node of line equations

$C1_n(k)$, $C2_n(k)$, $C3_n(k)$ = load terminal equations

$v_{N+1,M+1}(k)$, $i_{N+1,M+1}(k)$ = output boundary equations

Derivation of the general line equation given by $v_{n,m}(k)$, $i_{n,m}(k)$ is given in Appendix K to illustrate the general principles involved. Details of all six equations are given in Appendix L.

Figure 4.8 describes the algorithm flow chart used. Details of

the input parameters required for the main program are described in Appendix M. The calculated voltage and current values are stored as $C1_n(k)$, $C2_n(k)$, $C3_n(k)$, $v_{n,m}(k)$ and $i_{n,m}(k)$.

4.3.5 Computer Program

A FORTRAN program based on the above algorithm has been written for the ICL 297 O computer. Signal attenuation and relative intersymbol interference (ISI), defined in Section 4.4, are calculated by subprograms using the results from the main program.

Limitations

The primary limitation of the program is the relatively large storage size required to store the voltage and current values at each node of the basic line section. The corresponding minimum array size required, found from the variable definitions given in section 4.3.4. is given by

$$ARRAY = N(3 + 2M)K_S$$

where

N = total number of loads

M = total number of elementary sections within a block

K_S = total number of basic time steps for computation

(Calculation of K_S is given in Appendix M).

The above array size thus sets a limit to the number of loads and the length of transmission line that may be analysed.

In the present investigation, using a maximum of 19 loads, the required storage and run time of the computer are 1.4 M byte and 173 s respectively.

4.4 Simulation Results

This section describes the results of investigations carried out using both the transform and numerical methods of solution.

The performance criteria are based on the relative intersymbol interference factors of received signal waveform defined as

$$\beta_1 = \frac{v_r(T)}{v_r(T/2)}$$

$$\beta_2 = \frac{v_r(3T/2)}{v_r(T/2)}$$

and the signal attenuation at the half-bit sampling interval defined as

$$A = 20 \log_{10} v_r(T/2)$$

where,

$v_r(t)$ = received signal voltage at time t

T = the bit period.

Test Parameters

The following parameters were used for the test results described in this section :

Cable : 100m length of DRM 68 having the following characteristics :

$R = 0.35 \Omega/m$

$L = 0.60 \mu H/m$

$C = 60.0 pF/m$

$G = 0.019 m\mho/m$

above parameters were obtained from open-circuit and short circuit tests on the cable.

Input Current (I) : 20mA square pulse of width 1/6μS, which corresponds to a no-load input voltage pulse amplitude equal to UNITY and representing a half-bit element of PM and FM coded data at 3Mb/s.

Basic time step (T_s): 1.0 nS, which gives a total number of basic line sections of 600. i.e. $100\sqrt{LC}/T_s$.

Test Cases

Laplace : all the test results assume a lossless line.
Numerical : both the lossless and lossy line cases are considered.

4.4.1 Resistive Loading

Waveforms

Figure 4.9 shows received signal waveforms for various loads using the Laplace method and a lossless line. It is seen that, as expected, the signal amplitude reduces as the number of loads is increased, however no distortion is observed because second order effects are neglected.

Figure 4.10 shows similar waveform for the lossless line, using the discrete model. Distortion of the received signal due to multiple reflections is clearly evident in this case. This result is expected since the numerical solution, unlike the Laplace method, is exact and takes all reflections into account.

Attenuation

Received signal attenuation as number of loads is increased for various values of resistance is shown in Figure 4.11. All three cases using the cumulative theory, the Laplace method and the discrete model are compared. It is seen that there is close

agreement in all cases ; however the spread in the case of the discrete model is slightly greater. This is explained by the effect of multiple reflections as noted above.

The results of Figure 4.12 are derived from Figure 4.11 and emphasise the significance of load resistance value on the received signal attenuation. It shows that the signal attenuation and its rate of change increase sharply for low values of load resistance. The latter effect is important in considering the ability of a receiving terminal to accommodate load resistance variations (such as core loss resistance of transformer) without significant performance degradation.

Analysis of further simulation results, together with the use of the cumulative theory has shown that for a given number of loads N, the rate of change of attenuation w.r.t. load resistance, referred to as Resistance Spread Attenuation (RSA) by the author is given by :

$$RSA \simeq -4.343 \frac{NR_o}{R_L^2} \quad dB/\Omega \qquad (4.24)$$

R_o = line characteristic impedance

R_L = load resistance

In practice, it would be desired to keep the RSA small. The RSA value has in general been found to apply in the case of the RLC load as well.

4.4.2 Inductive Loading

Waveform

Figure 4.13 shows the effect of inductance on signal response for various loads using the Laplace method and assuming a lossless line. A resistance of 1KΩ is assumed in parallel with the inductive load. The result shows that increasing the number of loads has the effect of increasing the droop of the signal response. This is equivalent to decreasing the net inductance of the line with subsequent

increase in its overall low frequency cut-off. This is in line with the results of section 3.2.2 which assumed the loads to be effectively connected in parallel across a single signal source.

In Figure 4.14 similar response is obtained using the discrete model but, as for the resistive loading case, reflections caused by load mismatches is observed. It will be noted that there is no significant effect of inductance on the reflections.

Intersymbol Interference

A measure of the degree of waveform distortion caused by increasing number of loads is shown in Figures 4.15 and 4.16 for various inductance values ; using the Laplace method. There was no significant difference in similar results using the discrete model. Both results emphasise the significant effect of load inductance on signal intersymbol interference. At low values of inductance β_1 increases sharply with number of loads ; on the other hand, β_2 is generally smaller than β_1 and also tends to a maximum value as the load is increased. Comparable results are however obtained at higher values of inductance for both β_1 and β_2. The effects noted above will tend to reduce the noise margin of a transmitted signal further, in addition to that caused by resistive load mismatches. The maximum-value effect noted in Figure 4.16 for β_2 is explained by the waveforms of Figure 4.13 where it is noted that, for the higher load values the tail end of the curves tend to decrease faster.

Figures 4.17 and 4.18 are derived from Figures 4.15 and 4.16 respectively, and show that for high inductance values variation of loads does not significantly affect signal intersymbol interference.

The results of Figures 4.19 and 4.20 show the effect of variation of load resistance on signal intersymbol interference. It is noted that the effect for all values considered is insignificant even at low values of inductance. This result is expected and confirms that the resistive load affects signal attenuation only.

Attenuation

Figure 4.21 shows graphs of attenuation for various time constants as number of loads is increased ; using the Laplace method for the lossless line. Similar results were obtained using the discrete model. Corresponding results for the purely resistive load case is shown in the round dots . Comparison of the two sets of results show that the gradient of the inductive load curves is greater in all cases. Also for a given N the increase in attenuation of the inductive load results over the purely resistive load results is almost the same for all values of R_L. This observation again confirms the minimum dependence of signal intersymbol interference on the load resistance value. The difference between the resistive and inductive load results represent the attenuation due to signal distortion caused by the inductive loads. Figure 4.22 shows variation of the distortion loss with load inductance, derived by subtracting the results of Figure 4.21. It is seen that for low values of inductance the distortion loss increases sharply, which demonstrates yet again the significant effect of the inductance value on signal degradation. The effect of variation of load resistance is observed to be insignificant as noted earlier.

4.4.3 Capacitive Loading

Figure 4.23 shows signal response results for various loads using the Laplace method. A similar result for a single loading condition using the discrete model is shown in Figure 4.24 ; a lossy line is used. Three significant effects of capacitive loads on the signal waveform are generally observed, namely ; rise time, delay and multiple reflections. The delay in the case of the discrete model is not evident because in this case the program was organised to output non-zero results only.

Risetime and Delay

It is seen from Figure 4.23 that both the signal risetime and delay increase with number of capacitive loads even though the time constant for each load remains the same. Equally, it has

been found that for a fixed number of loads the signal risetime and delay also increase as the load time constants are increased. The increase in risetime show that, like the inductive case, the connection of a number of capacitive loads affects the overall frequency response of the line in the form of a reduction of the high cut-off frequency.

The capacitive load time constant is given by

$$\tau_R = \frac{C_L R_o}{2} \cdot \frac{1}{1 + \frac{R_o}{2R_L}} \qquad (4.25)$$

where

C_L = load capacitance

R_L = load resistance

Figure 4.25 shows typical results of variation of risetime and delay with number of loads. It is observed that the signal delay seems to increase linearly with number of loads whereas the risetime exhibits an exponential increase.

Both effects have been found to be dependent also on the load distribution. For a given number of loads the delay is found to be minimum for clustered loading and maximum for uniform loading ; however the increase over the minimum case is not very large and does not appear to be worthy of consideration in design. The signal risetime, on the other hand, is found to be minimum for uniform loading and maximum for clustered loading ; this is because concentration of the loads tend to increase the effective time constant of the loads.

Multiple Reflections

From Figure 4.24 it is seen that, unlike the inductive case, the capacitive loads tend to exaggerate the purely resistive load

reflections in the form of oscillations. The severity of oscillations, in terms of number, has been found to be dependent only on the load distribution ; the shorter the load spacing (this is directly equivalent to increasing number of loads for the uniformly distributed case), the more the number of oscillations. This is explained by the increase in the number of times the reflected signal travels between the closely spaced loads.

It is also seen from Figure 4.24 that the worst case reflection (i.e. the maximum negative deviation from the wave without reflections), occurs at the negative half cycle of the first oscillation. This is again demonstrated by the results of Figures 4.26 and 4.27. The latter is a photograph of the physical situation for comparison with the computer simulation results of Figure 4.26. The similarity of the computer and experimental results is clear ; the differences that are apparent are the smaller amplitude of oscillation of the physical case. This difference is explained by the fact that skin-effect resistance of the line, which would tend to limit the cable frequency response, was not completely taken into account in the model solution : the loss resistance used was taken at 3 MHz. It has been found that the worst case reflection is dependent on both the spacing and time constant of the loads. Generally it would be expected that as the load spacing decreases (i.e. number of loads increase), the worst case reflection would increase since the reflected wave would travel shorter distances and thus give rise to severe reflections. On the contrary, results obtained indicate that for a given load time constant, the worst case reflection decreases with increasing number of loads. This is explained by the increase of signal attenuation due to the resistive load component mismatches as the number of loads increases. See section 4.4.1. Figure 4.28 shows the variation of percent worst case reflection with number of loads for various time constants. The decrease with number of loads noted above is clear. It is seen however that for a given number of loads, an increase in the time constant of the single load has the effect of increasing the percent worst case reflection.

4.4.4 Transformer Load

The combined effect of the load components comprising the resistance, inductance and capacitance on signal response is demonstrated in Figures 4.29 and 4.30. All the effects noted in the previous sections, namely resistive load attenuation, inductive load droop and capacitive load delay and multiple reflections are evident. This result shows that in fact the individual effects in terms of degradation of signal noise margin may be treated separately and their effects added together. This is confirmed by the physical system tests presented in the next section of this chapter.

Mismatch Attenuation Prediction

The total mismatch attenuation of the RLC load, assuming negligible capacitance effects, has been found to be given by the following approximate relationship ;

$$A_M(dB) \simeq 20N\log(r_o) + [20(N-1)\log(1-\eta) - 8.686\eta] \qquad (4.26)$$

Given that,

$$r_o = \frac{1}{1 + \frac{R_o}{2R_L}}$$

$$\tau_L = \frac{L_L}{R_o}$$

then,

$$\eta = \frac{T}{4\tau_L r_o}$$

where,

T = the bit period.

The above equation is derived from the time response equation for the Laplace method given by Equation 4.3 ; by neglecting the capacitance terms i.e. $\tau_c = O$ in Equation 4.6.

It will be noted from Equation 4.26 that the first term is in fact the resistive mismatch loss predicted in the theory given in Section 3.2. The other terms account for the inductive distortion loss neglected in the previous theory.

This equation has been found to closely predict the physical situation, as will be noted in the next section.

4.5 Computer Solution and Physical System Examples

In this section experimental tests carried out to verify the discrete model simulation results is presented. Results of attenuation predictions using the resistive mismatch theory and the theoretical loss given by Equation 4.26 are included for comparison.

All the tests were carried out using a 100m length of DRM68 cable and a data bit rate of 3 Mb/s. The simulation tests however assume a $\frac{1}{2}$ bit element pulse of duration T/2. Measurements of signal to noise ratio and error rate were carried out following the procedures presented in Chapter 3.

4.5.1 Test Examples

Example 1

The RLC load components used were respectively ;

$$R = 1K$$
$$L = 1.3 \text{ mH}$$
and $$C = 47 \text{ pF}$$

Example 2

This test example used the same transformer designed for the tests described in section 3.2.3. The measured parallel RLC equivalent parameters were :

$R = 5.6\ K$

$L = 4.7\ mH$

and $C = 20\ pF$

4.5.2 Results

Figure 4.31 shows results of tests for the parallel RLC load of Example 1. The closeness of the experimental and simulation results is rather encouraging and confirms the validity of the discrete model used. It is observed that the attenuation variation tend to fluctuate about a mean value ; this fluctuation is in fact due to multiple reflections and represents a measure of its effect. The theoretical result given by Equation (4.26) also follows the experimental result closely but as the number of loads increases it begins to deviate. This is expected because it is only an approximation to the physical situation since the effects of line distortion and capacitve load reflections is not taken into account by this theory. However the result show that for small load capacitance and number of loads Equation (4.26) fairly accurately predicts the total mismatch attenuation. The improved prediction over the resistive mismatch theory is clearly demonstrated by the over-optimistic results shown by the heavy curve.

The results of tests for Example 2, using the transformer coupled loads is shown in Figure 4.32. Again as in the previous results, there is close agreement of the experimental and simulation results. The theoretical prediction using Equation (4.26) also gives an improved result over the resistive mismatch theory.

4.6 Conclusions

The use of the two simulated models of the highway have enabled precise identification of the effects of the LCR components of the transformer load on the performance of the baseband system.

It has been shown that the discrete transmission line method provides an exact solution of the highway model for both lossy and lossless line cases, without the additional complexities identified with the more conventional Laplace method of solution.

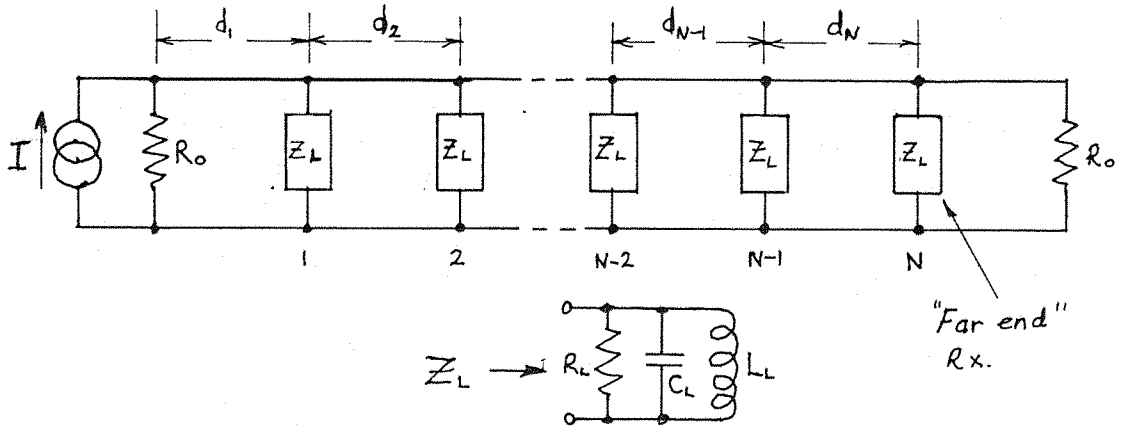
The studies carried out on the two highway models have shown that :

(a) The core loss resistance of the transformer load largely accounts for the transmitted signal attenuation.

(b) The additional signal loss of the transformer coupled loading tests, noted in Chapter 3, is due to the signal distortion caused by the primary self inductance of the transformer load.

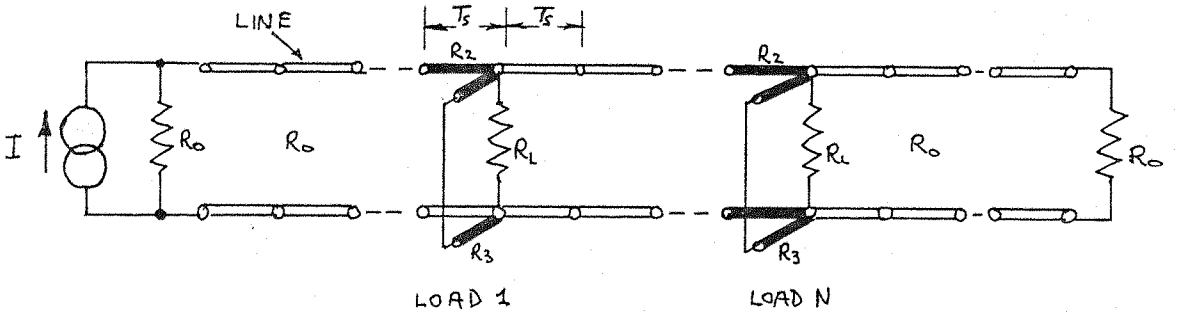
(c) The stray and interwinding capacitances of the transformer load account for the signal delay, risetime degradation, and multiple reflections.

The severity of the above effects on the signal have been found to increase as the number of loads is increased ; however, contrary to expectations, it has been found that the severity of the worst case reflections tend to decrease as the number of loads is increased. This is explained by the fact that as the number of loads is increased the corresponding increase of the resistive load mismatch loss, limits the amplitude of the reflections.



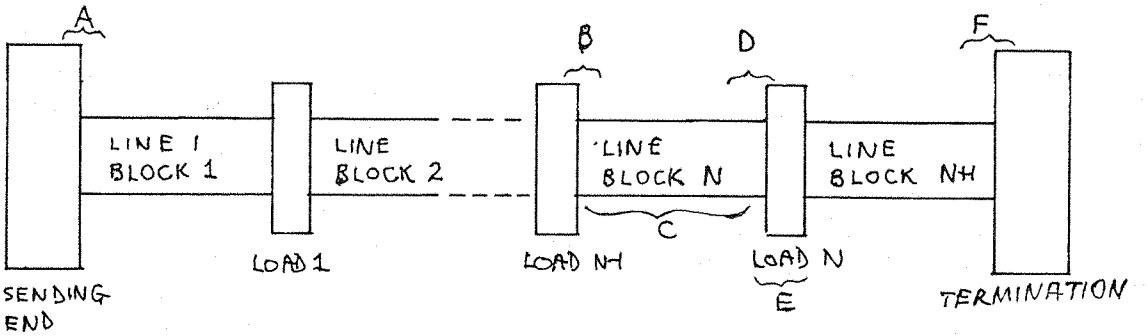
Passive Highway Arrangement

FIG 4.1



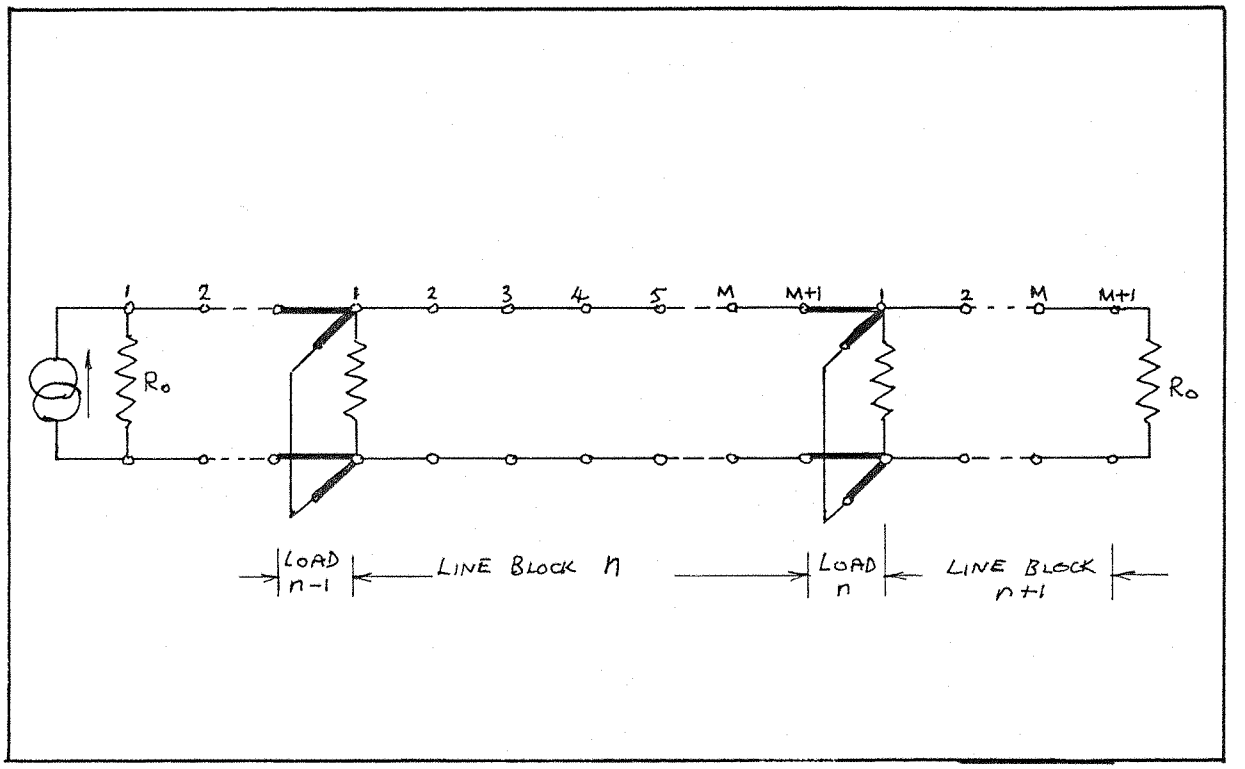
Discrete Transmission Line Model

FIG 4.3



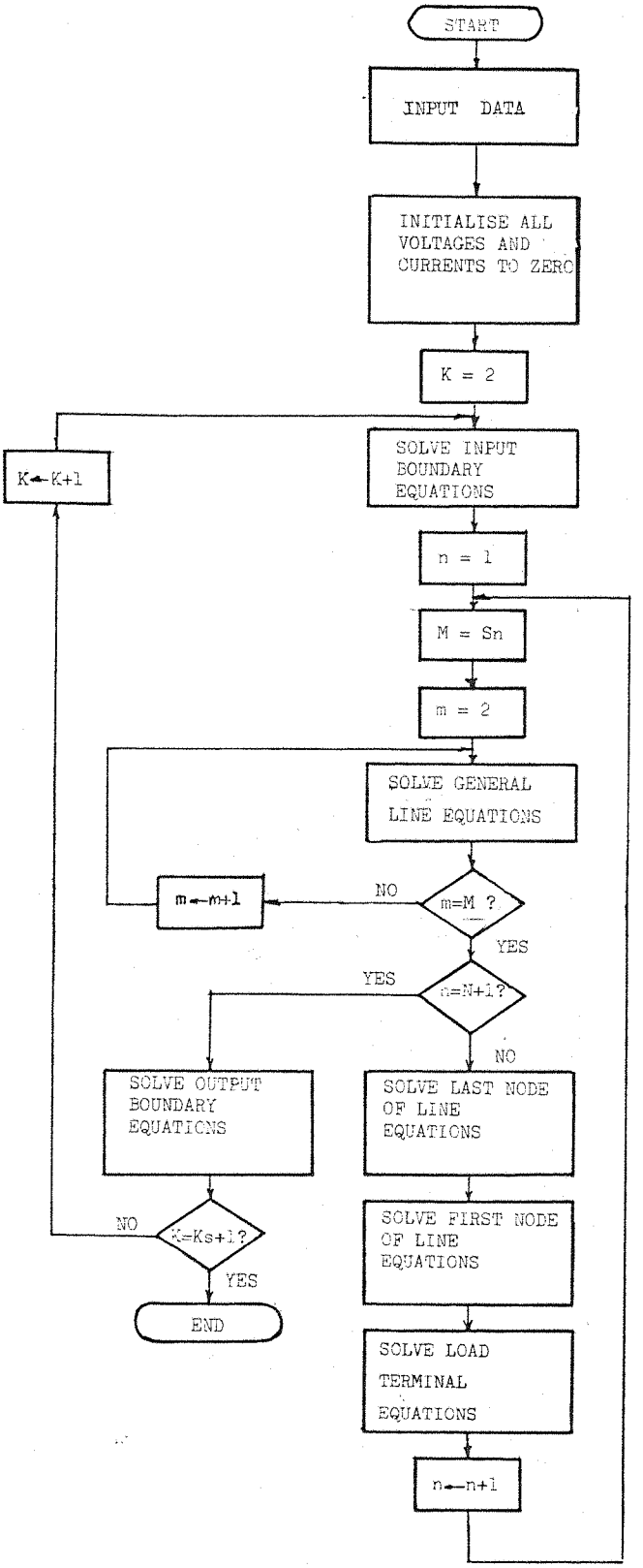
Block Diagram for Discrete Model Solution

FIG 4.4



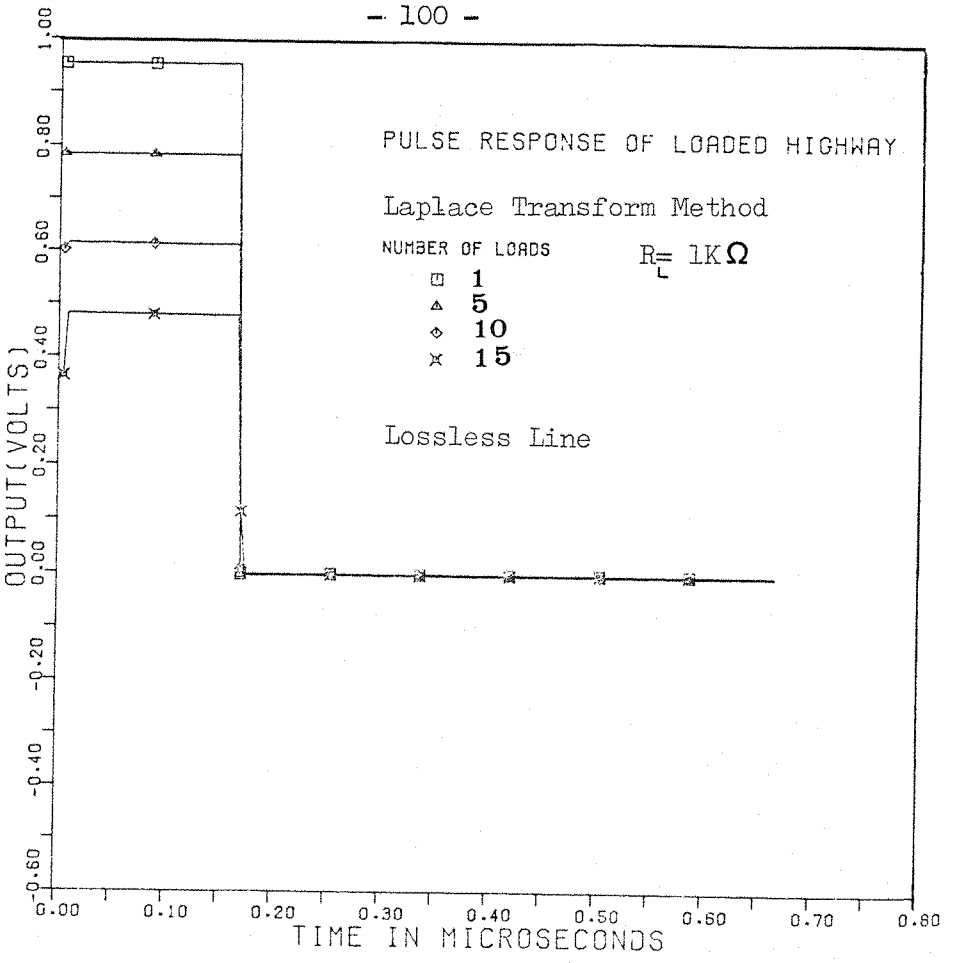
Nodal Assignments

FIG 4.5



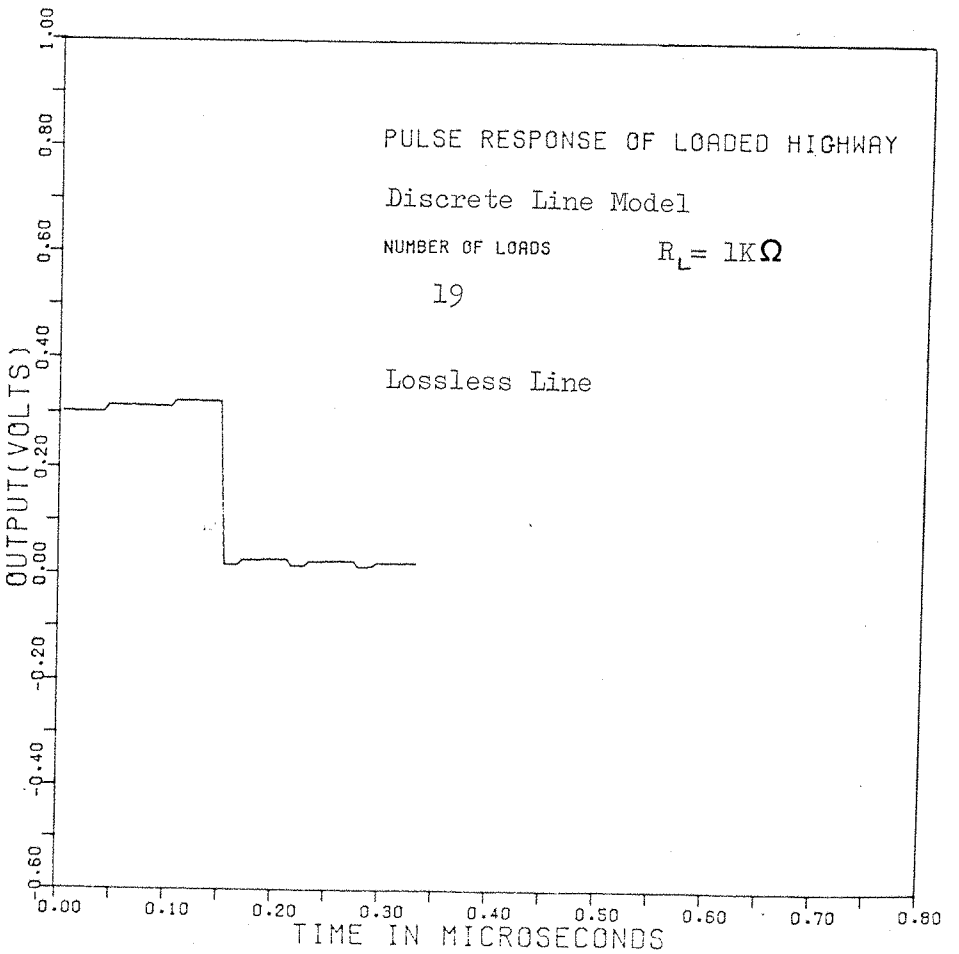
Algorithm Flowchart for Numerical Solution

FIG 4.8



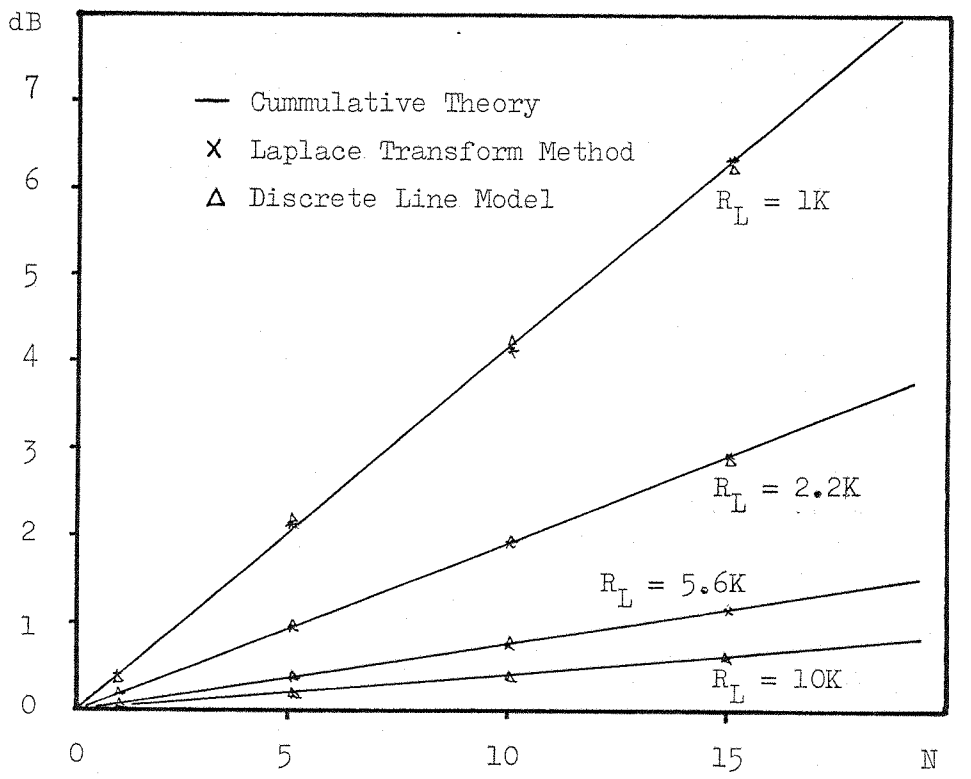
Signal Response for Various Number of Resistive Loads

FIG 4.9



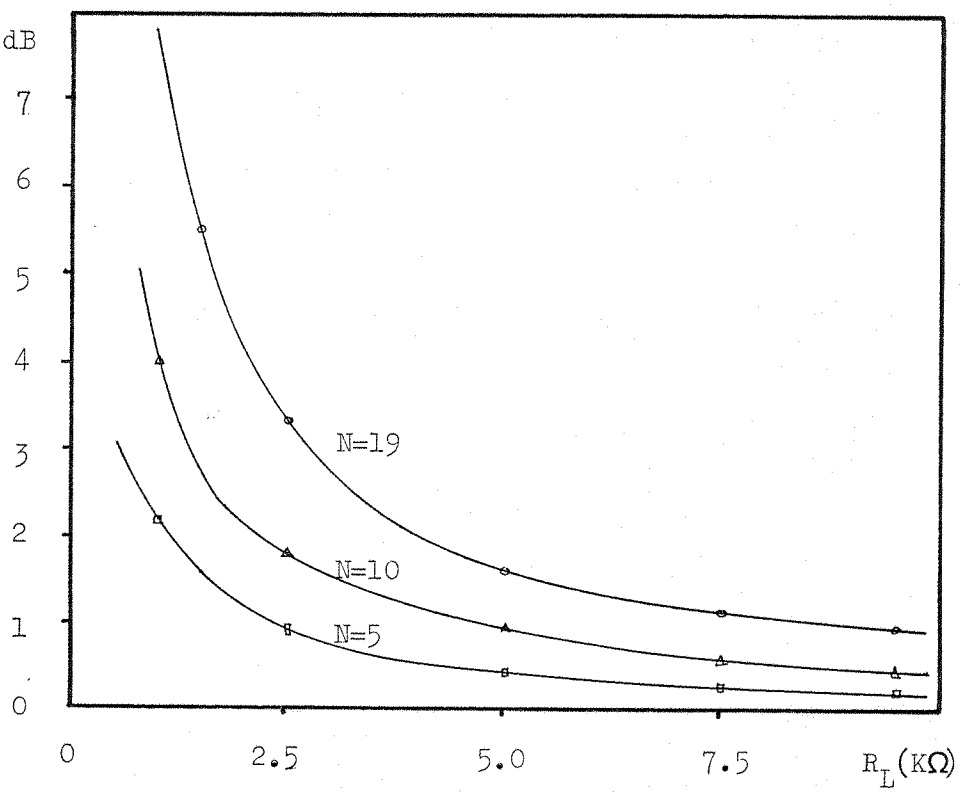
Multiple Reflections Caused by Resistive Load Mismatches

FIG 4.10



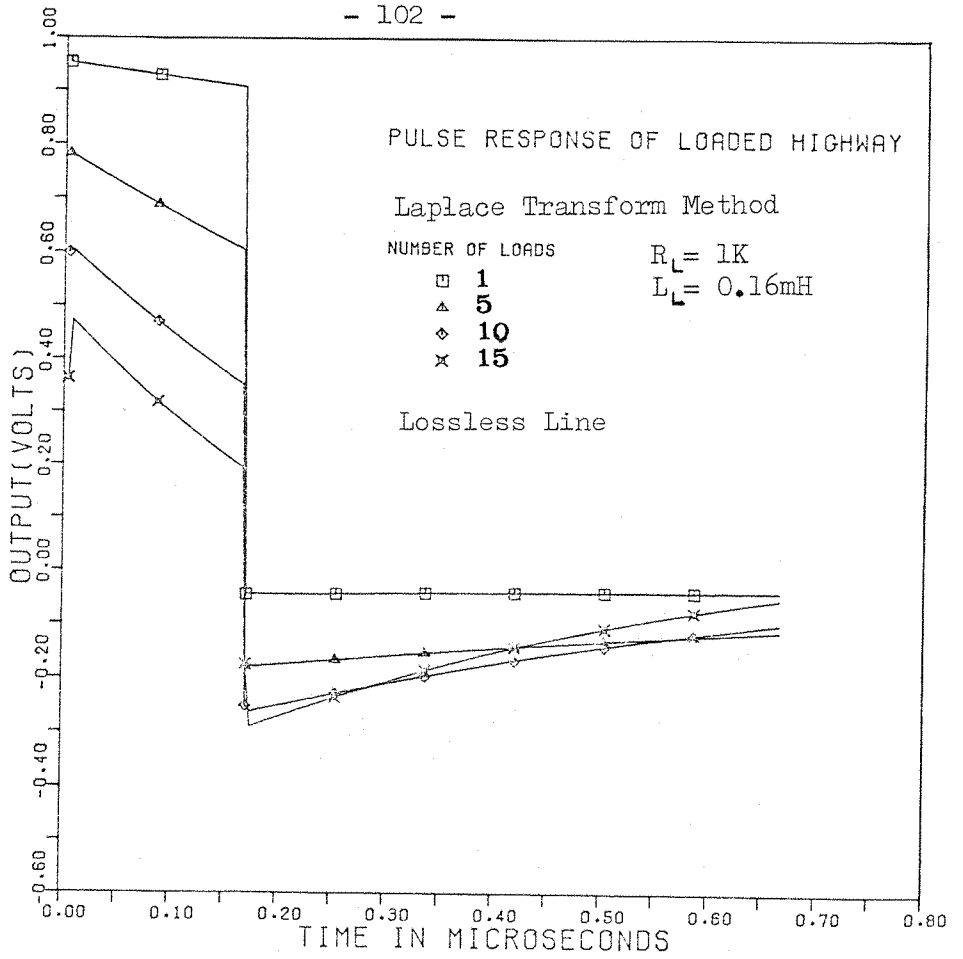
Signal Attenuation for Various Resisitive Loads

FIG 4.11



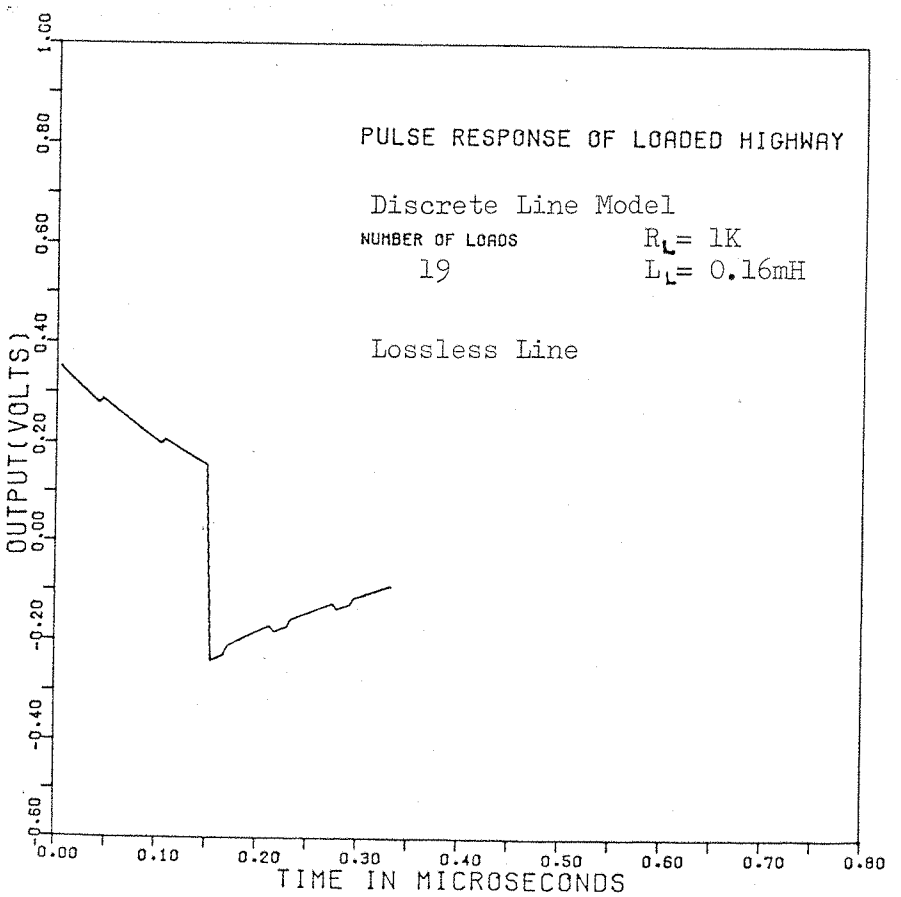
Effect of Resistance Value on Signal Attenuation

FIG 4.12



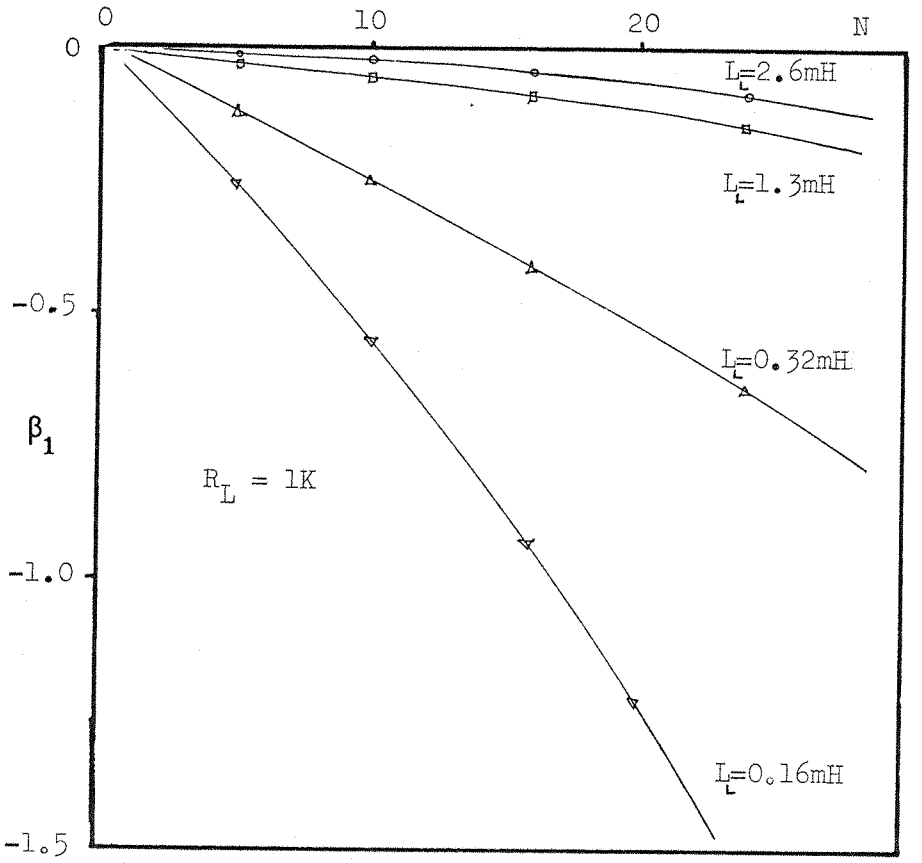
Signal Response for Various Number of Inductive Loads

FIG 4.13



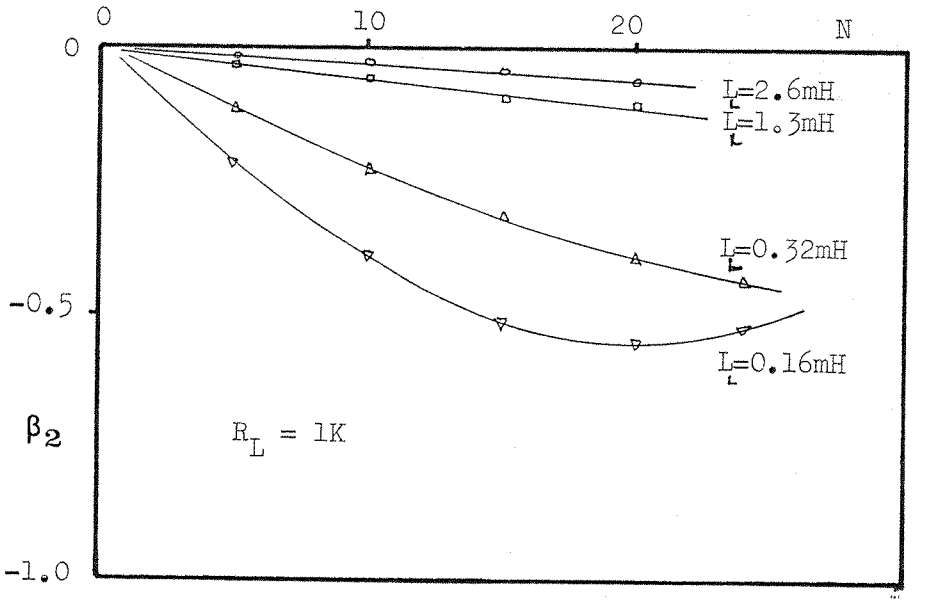
Effect of Inductive Loads on Signal Response

FIG 4.14



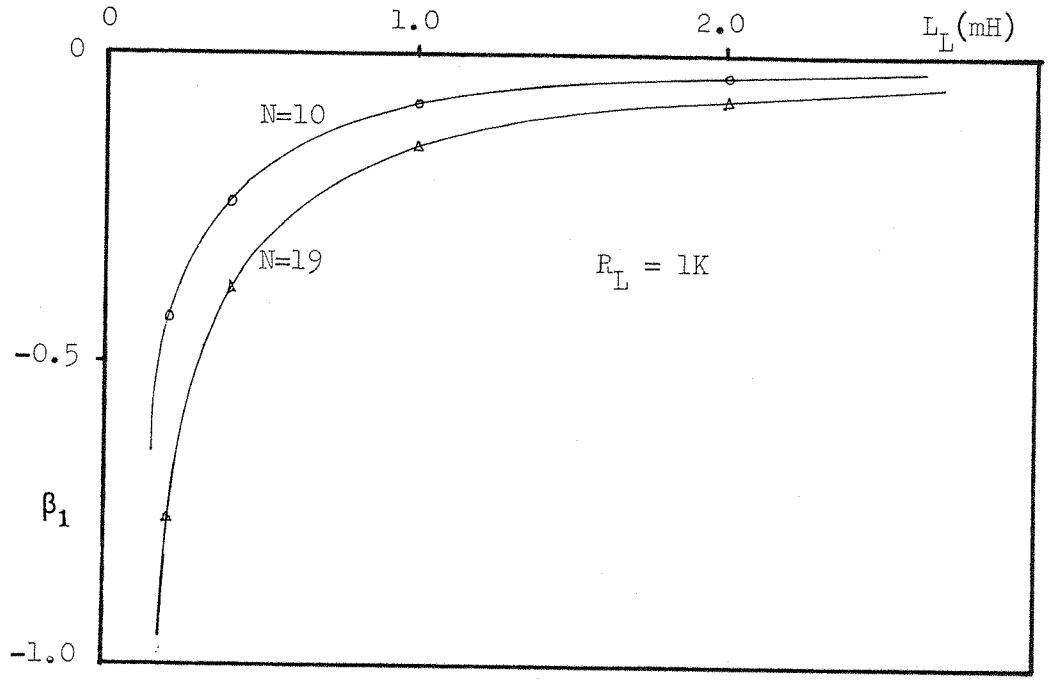
β_1:- Effect of Variation of Inductive Loads

FIG 4.15

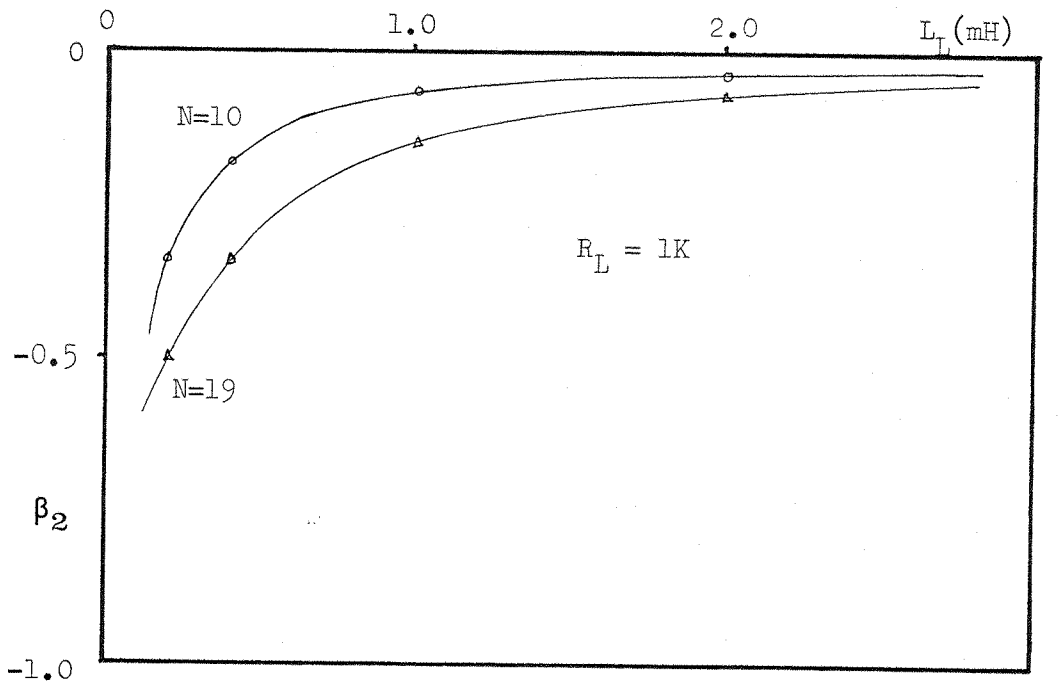


β_2:- Effect of Variation of Inductive Loads

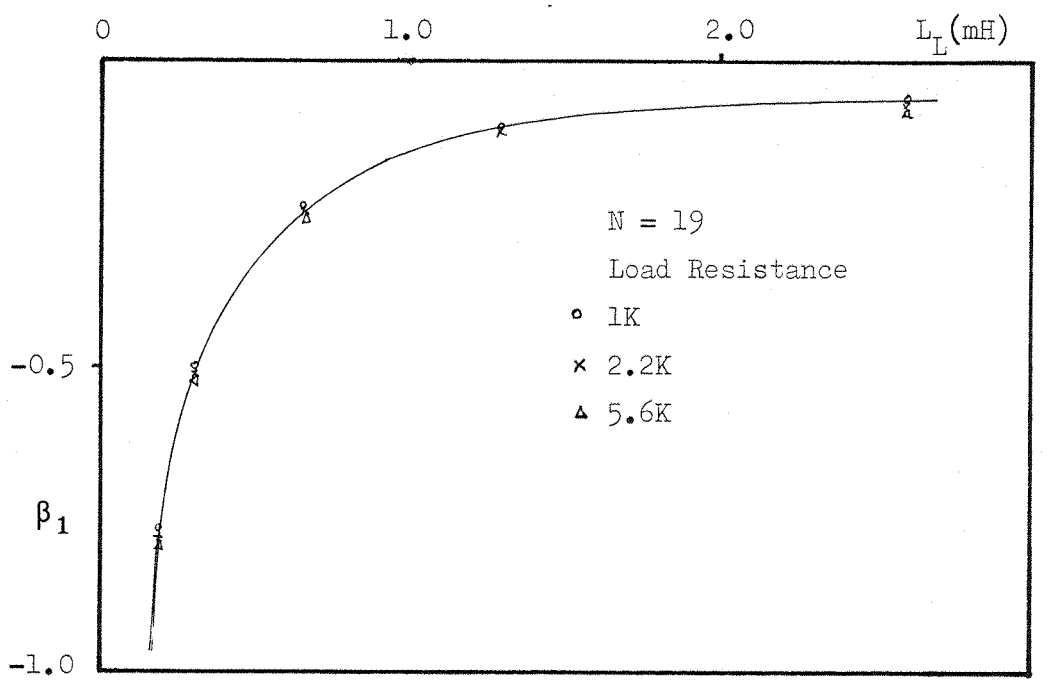
FIG 4.16



β_1 :- Effect of Variation of Number of Loads FIG 4.17

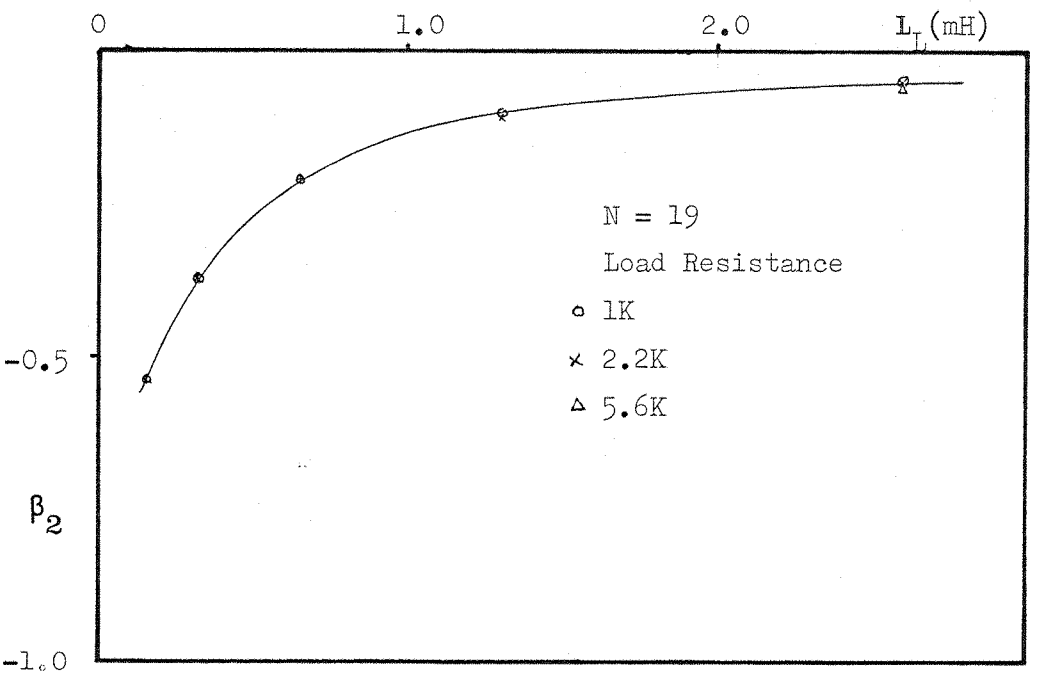


β_2 :- Effect of Variation of Number of Loads FIG 4.18



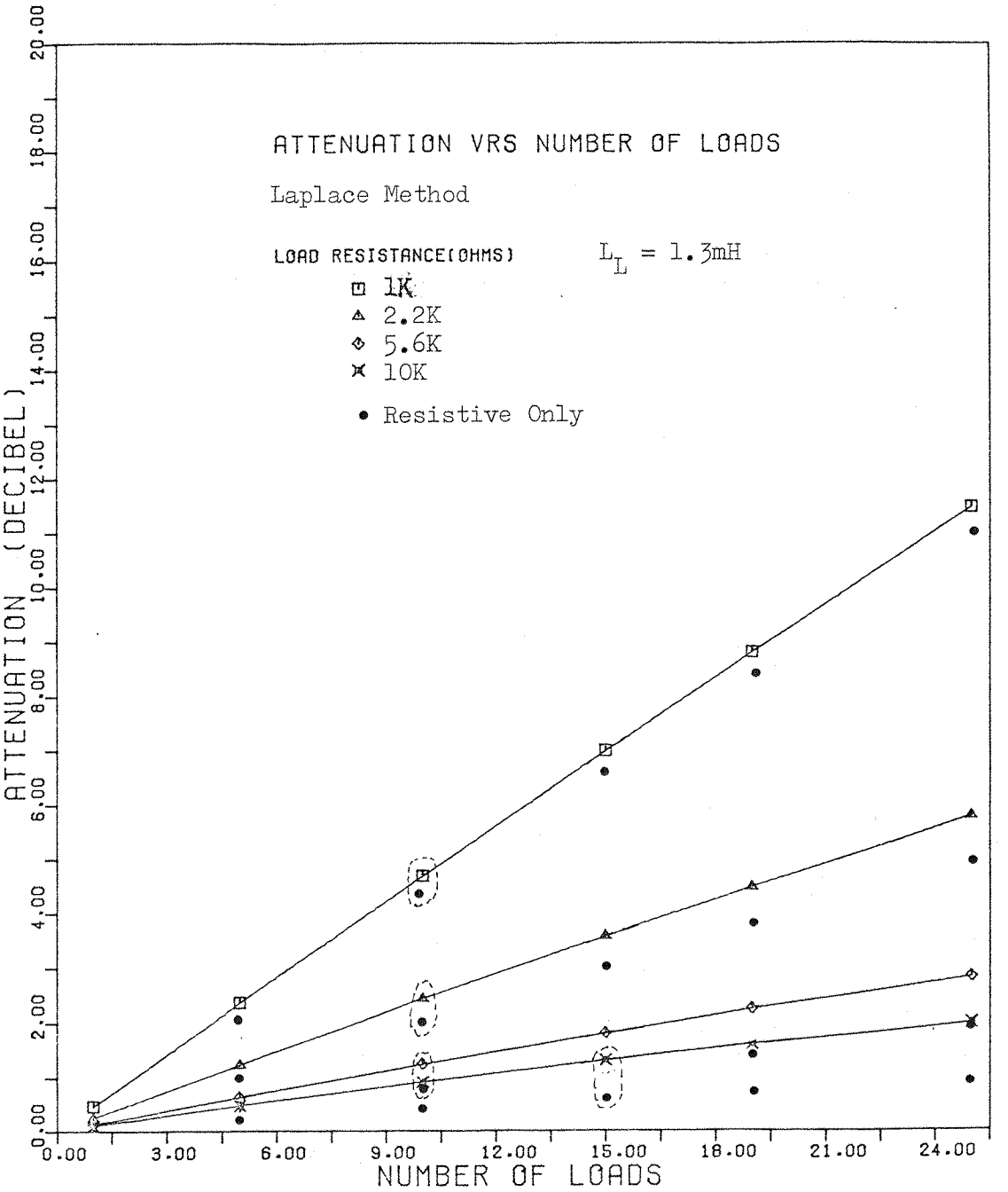
β_1:- Effect of Variation of Load Resistance

FIG 4.19



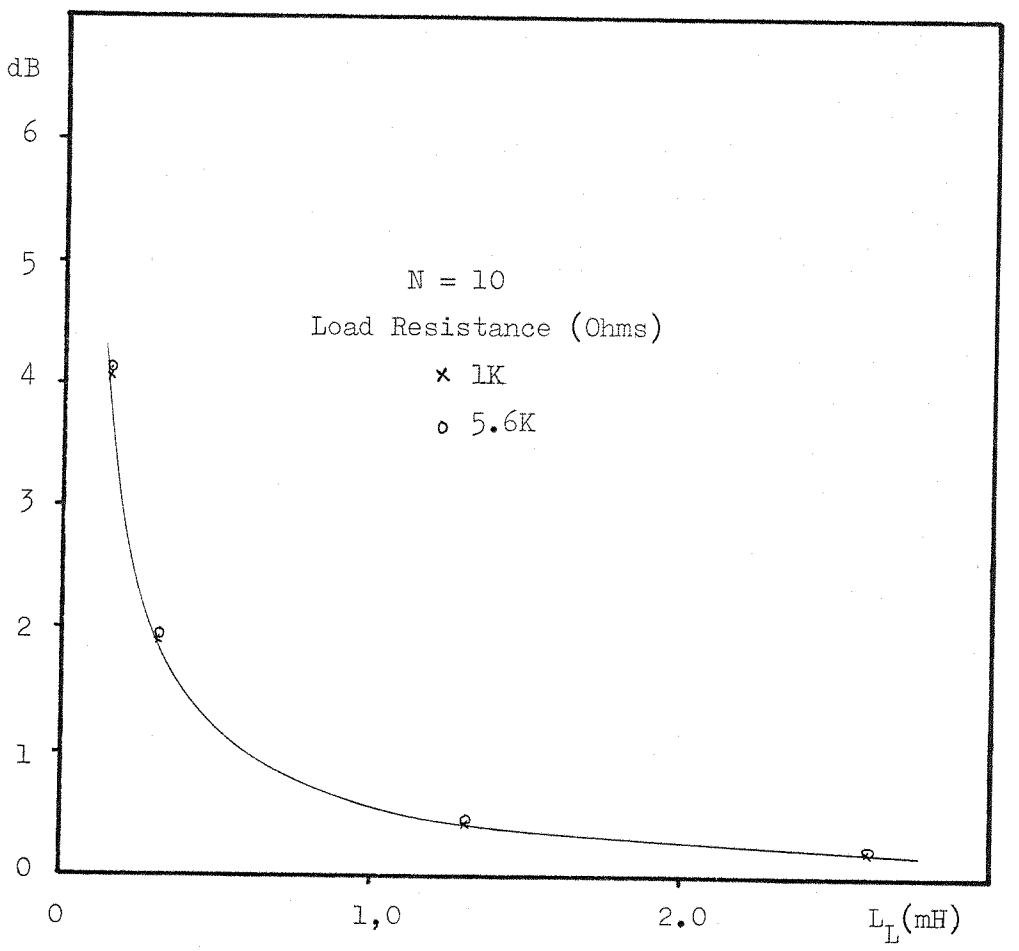
β_2:- Effect of Variation of Load Resistance

FIG 4.20



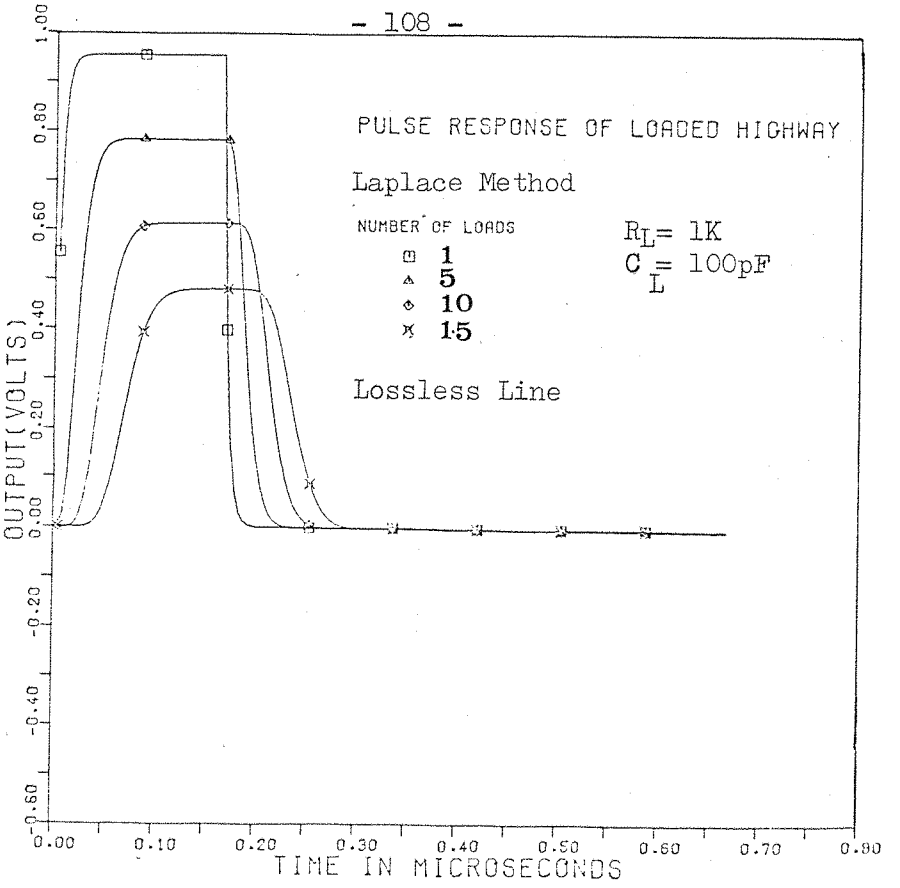
Variation of Inductive Load Time Constant

FIG 4.21



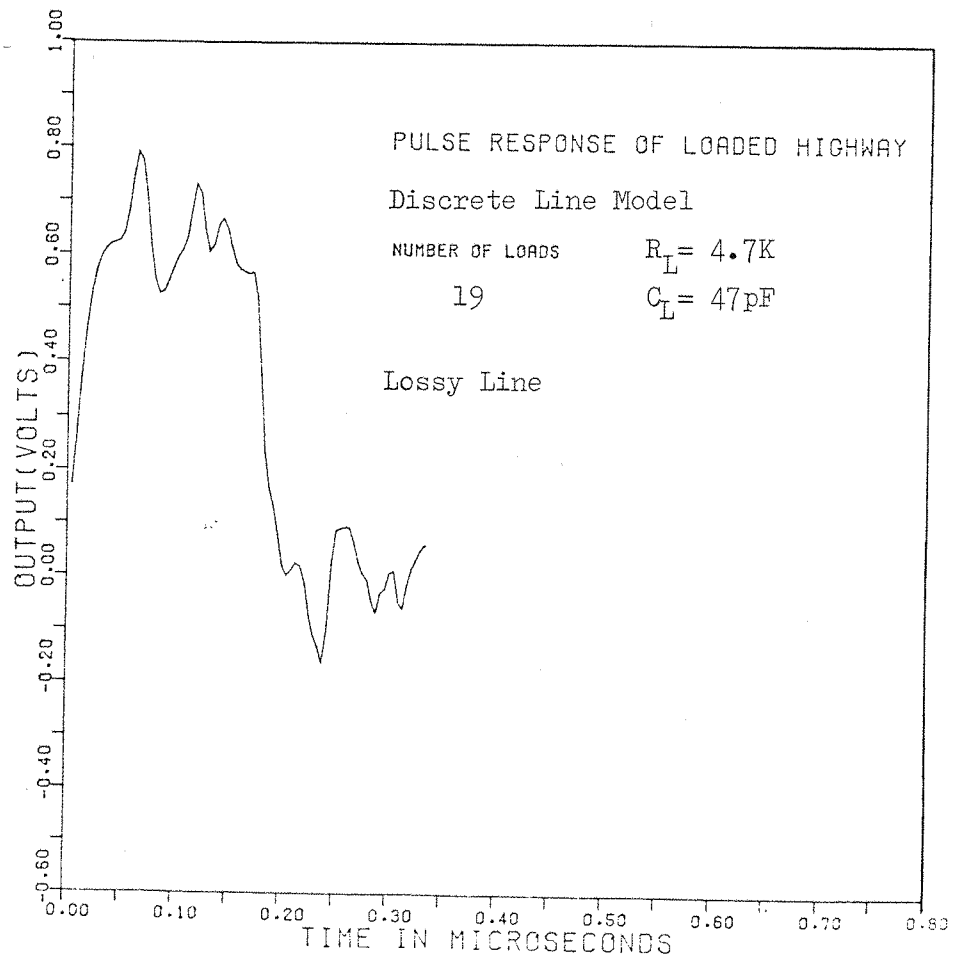
Inductive Load:- Variation of Distortion Loss with Load Inductance.

FIG 4.22



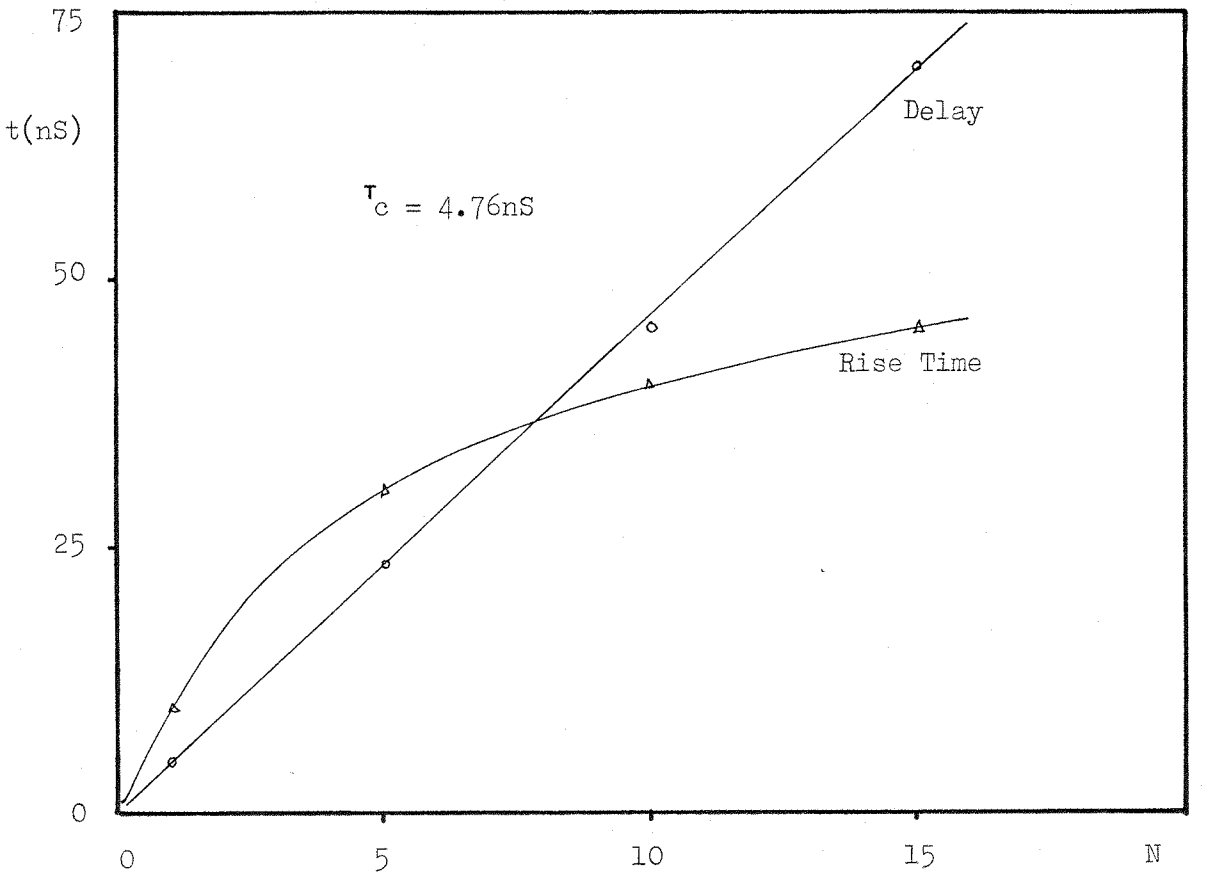
RC Load:- Effect of Variation of Number of Loads

FIG 4.23



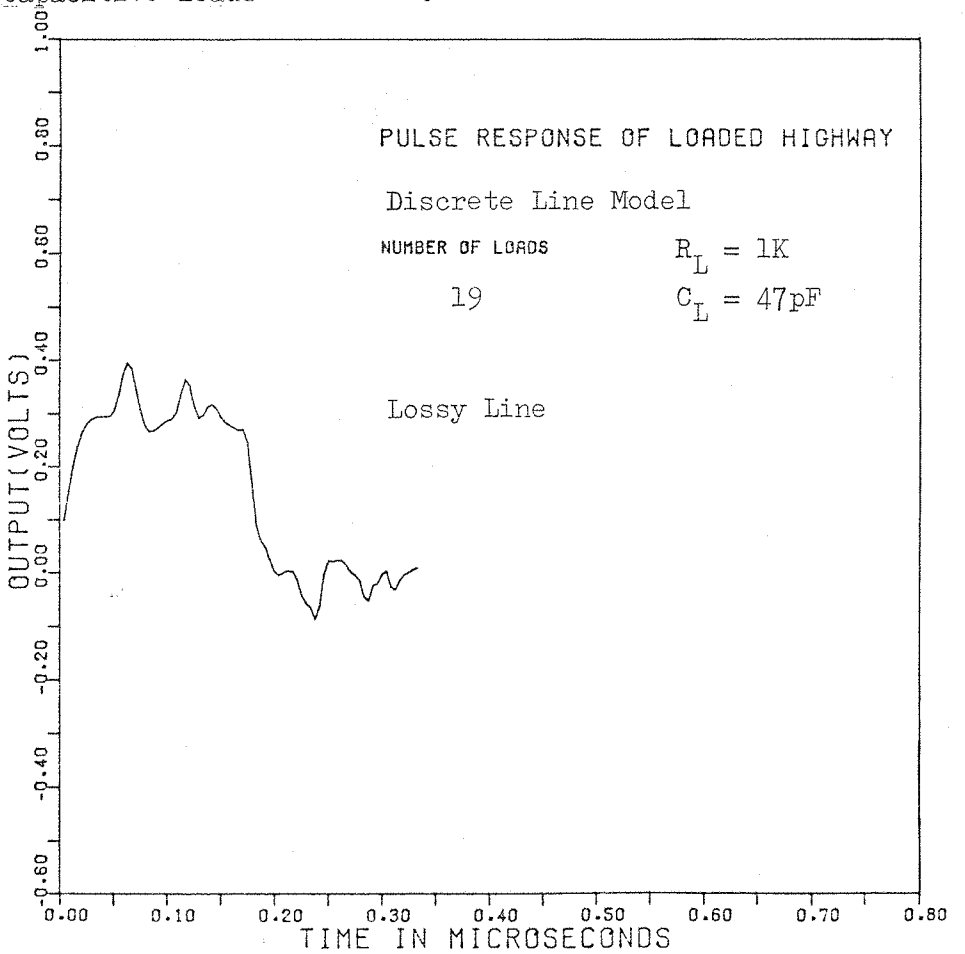
Multiple Reflections of Capacitive Loaded Line

FIG 4.24



Variation of Risetime and Delay with Number of Capacitive Loads

FIG 4.25



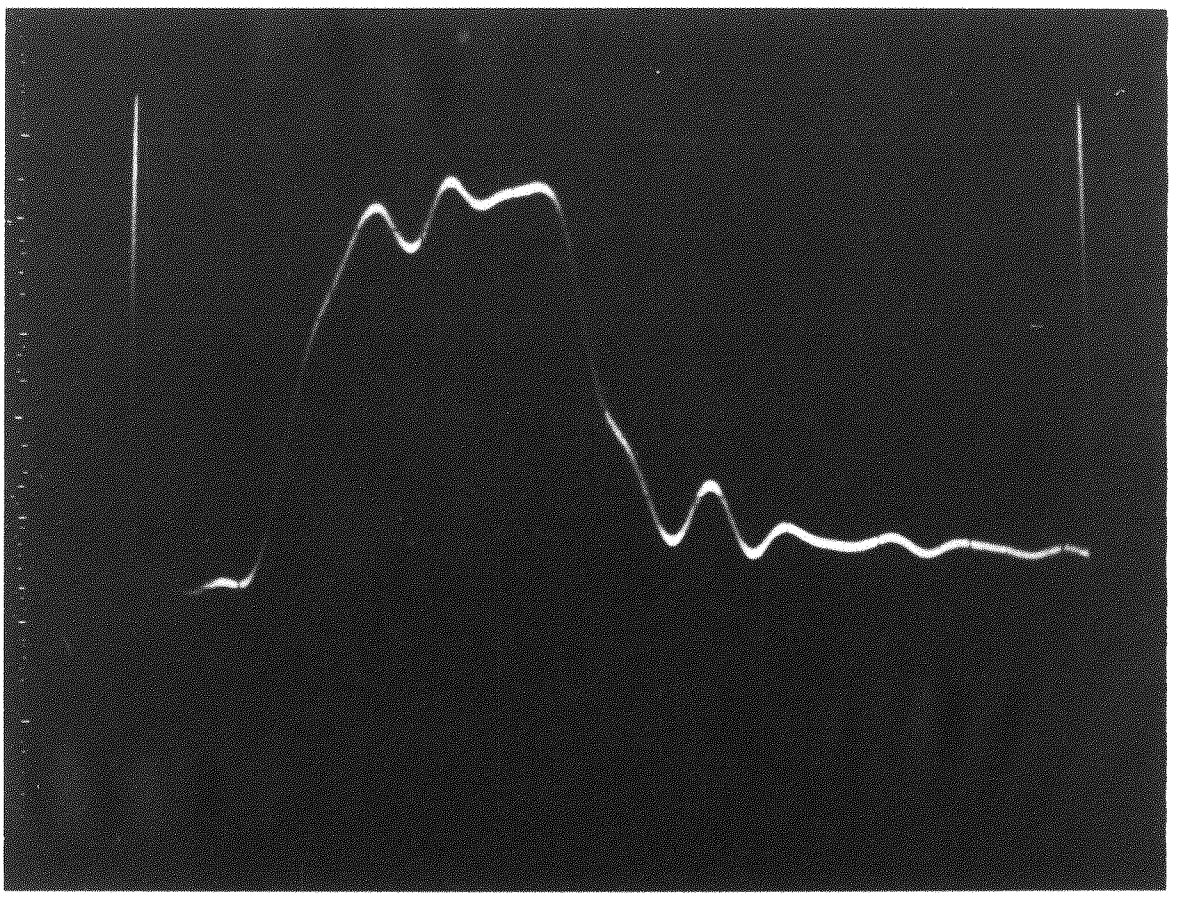
Multiple Reflections of Capacitive Loaded Line

FIG 4.26

N = 19

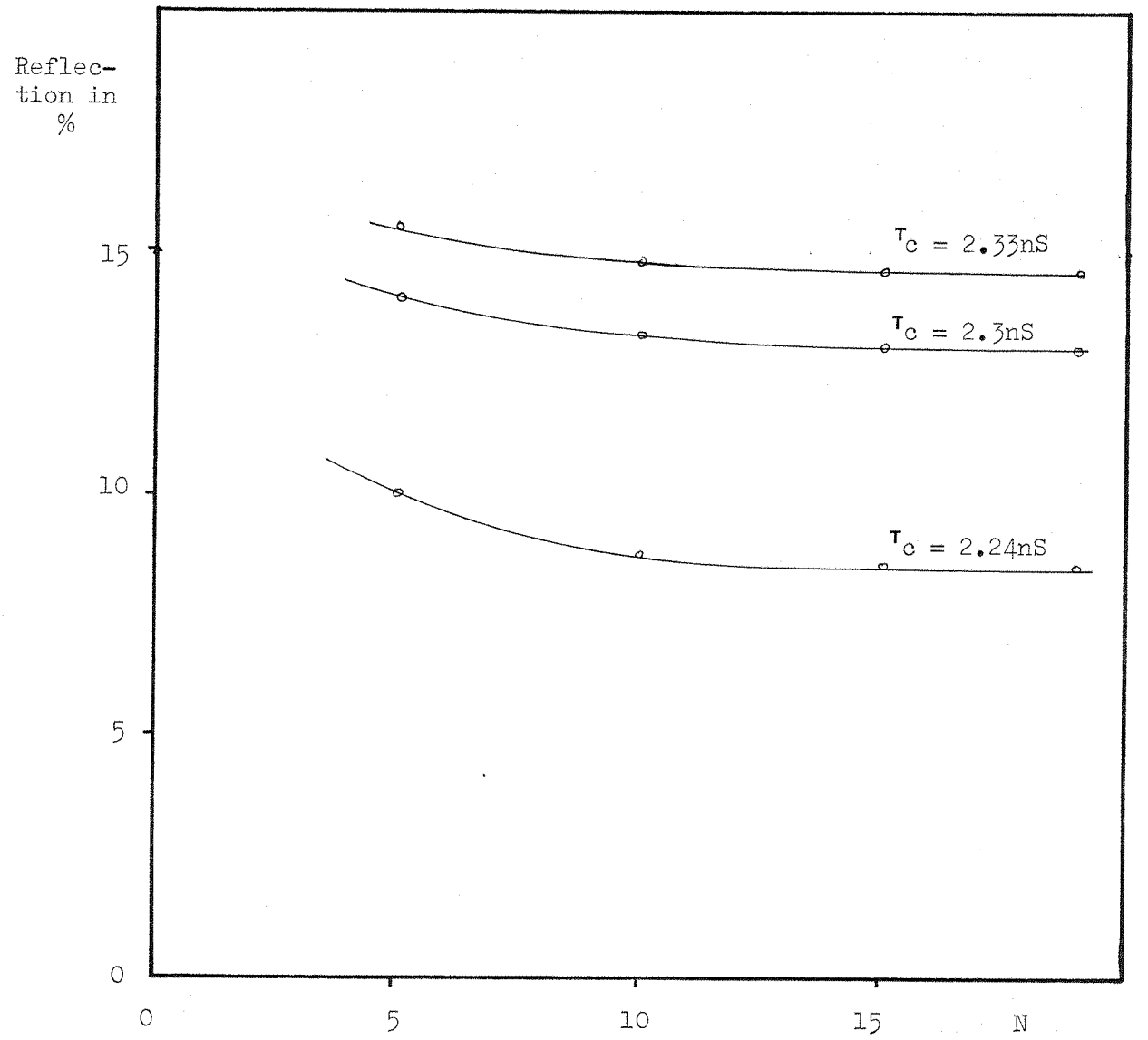
R_L = 1K

C_L = 47pF



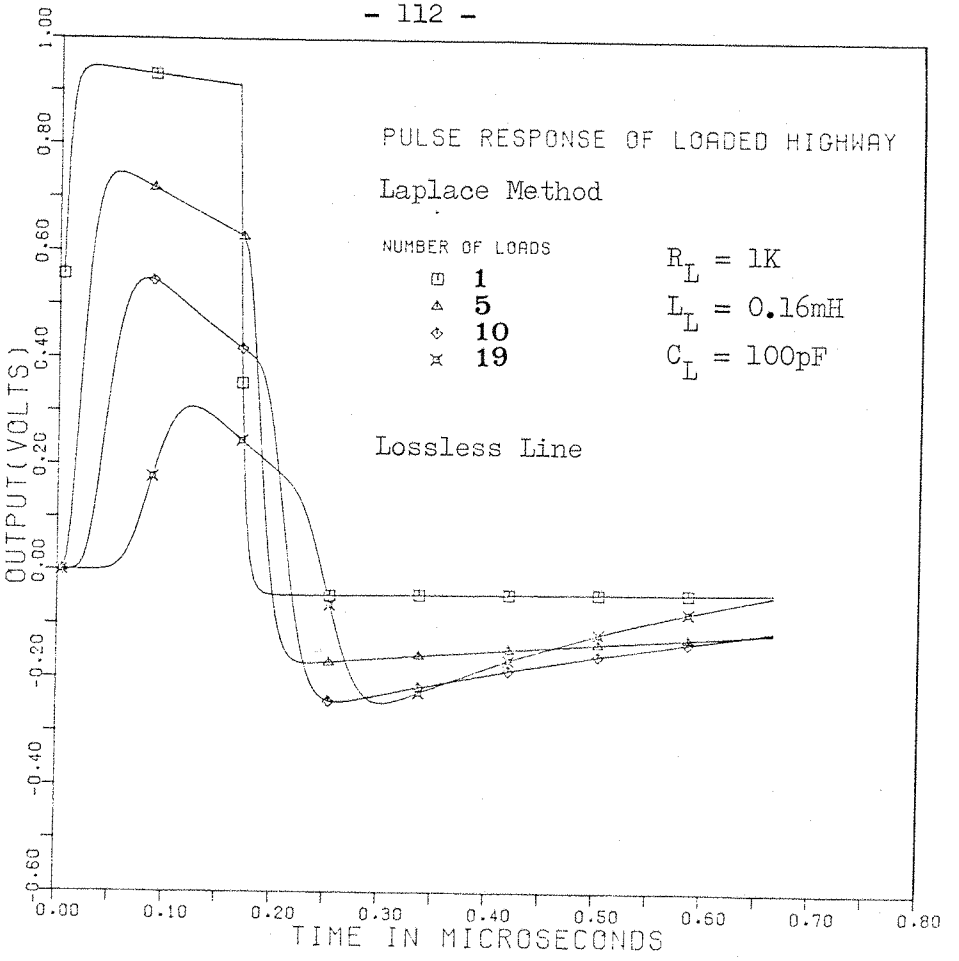
Experimental Result Showing Multiple Reflections of an RC Loaded Line.

FIG 4.27



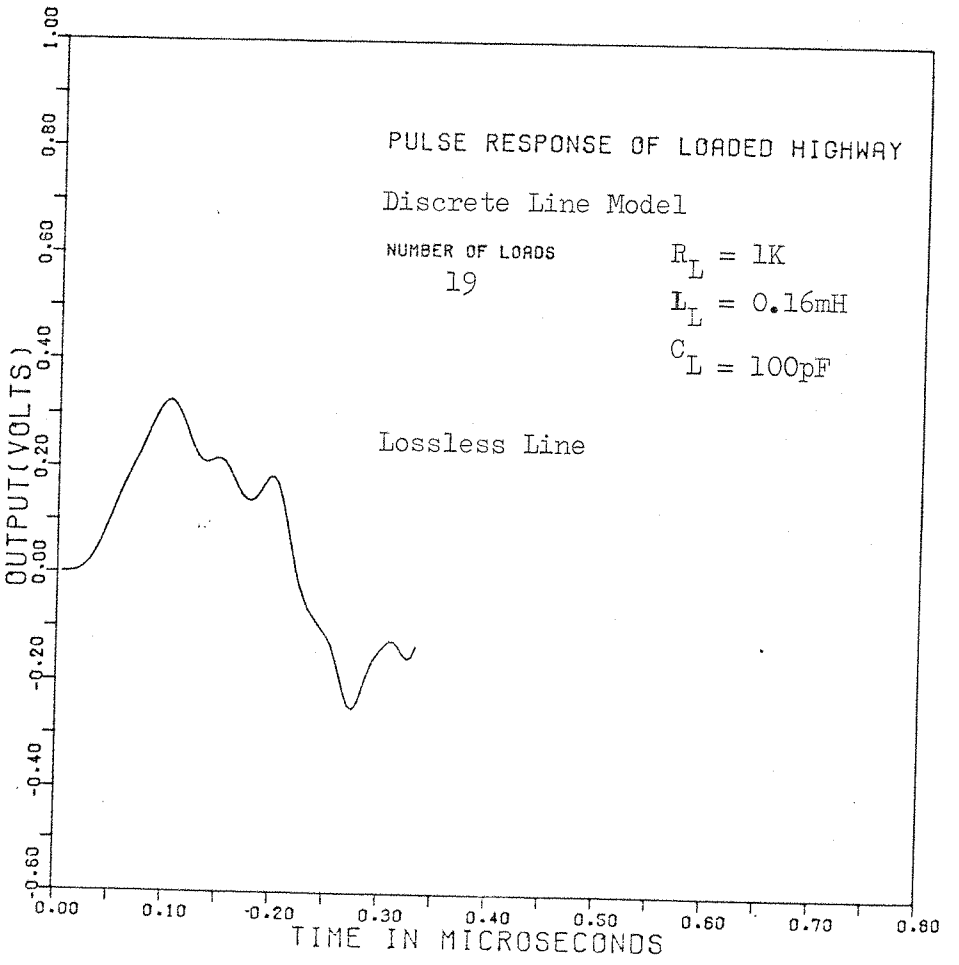
Variation of Worst Case Reflections with Number of Loads.

FIG 4.28



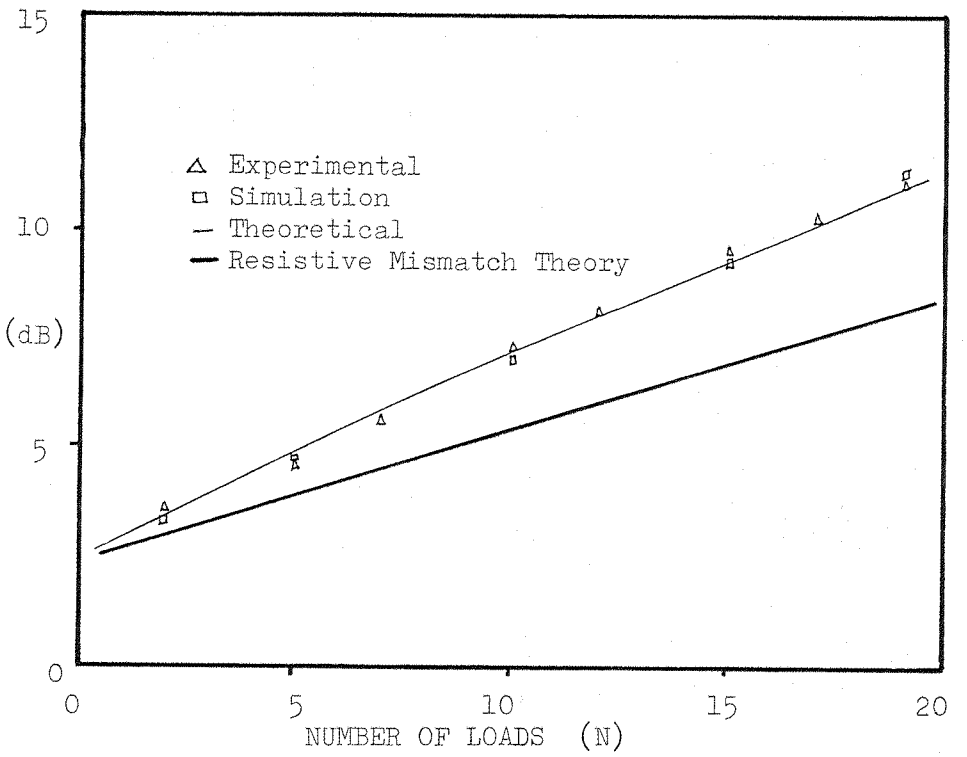
RLC Load:- Effect of Increasing Number of Loads.

FIG 4.29



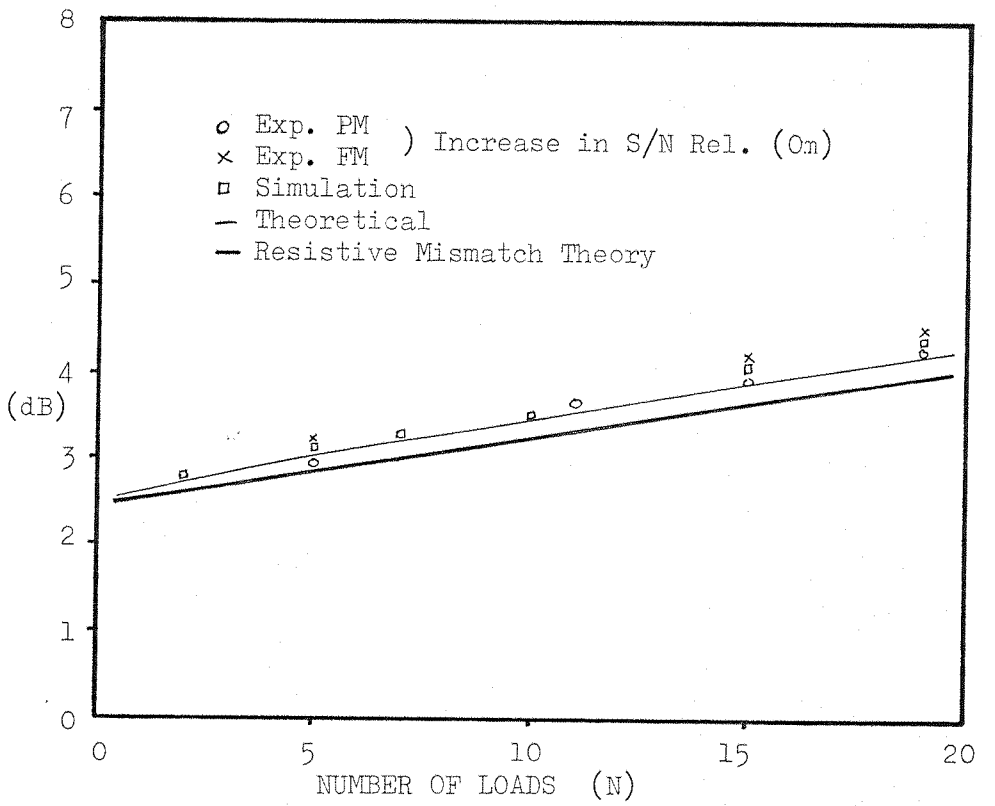
RLC Load:- Effect of Multiple Reflections

FIG 4.30



Comparison of Experimental, Theoretical and Simulation Mismatch Attenuation of an RLC Loaded Line.

FIG 4.31



Comparison of Experimental, Theoretical and Simulation Results for Transformer Coupled Loads

FIG 4.32

5. MODULATED CARRIER SYSTEMS

5.1 Introduction

The results of studies carried out in the previous chapters have shown that the baseband system suffers from both line distortion and loading effects which set limits to the total line length and to the acceptable number of terminals for reliable operation.

A more flexible means of increasing the number of terminals would be the use of multiplexing techniques with high frequency modulated carrier signals. If the signal is narrowband, with most of its energy in the vicinity of the carrier, then the effect of line distortion would also be minimised ; thus raising further, the threshold for reliable system operation. In addition to the above, the system noise threshold and hence the maximum tolerable number of loads can be increased by using lower loss coaxial cable with no common mode interference and no EMI radiation.

This chapter reports on the design of an experimental carrier modulated system and the results of tests carried out to verify its performance. The minimum shift keyed modulation (MSK), which is becoming an increasingly popular technique, (22), (23), (24), has been used because of its narrowband properties. The cable used for the tests is the low loss coax(Andrew flex $\frac{1}{2}$" type LDF 4/50).

Two sub-optimum types of demodulators for the MSK signal have been investigated, namely :

(a) correlation demodulator, and
(b) differential strobe demodulator ; also called filter threshold demodulator by French (25).

In principle bit clock can be recovered in the demodulation process thus no additional baseband coding is necessary.

Particular attention was given to the design of coupling networks for the transmitter and receiver circuits during the initial stages; it was required that the network should be more efficient because of the narrowband transmitted signal. Two approaches studied in the realisation of the above were ;

(a) impedance matching of input and output ports to the line,
(b) high input impedance parallel connections as in the baseband system.

The high impedance method of coupling was found to be the more suitable for bidirectional transmission on the line which is inherent in a passive highway.

5.2 Theory of MSK

Definition

Minimum shift keying (MSK) is a type of digital modulation which can be viewed as a form of coherent frequency-shift-keyed (FSK) modulation having the following properties :

(a) The frequency shift Δf is exactly $\frac{1}{2} f_b$;
(b) There is phase continuity of the modulated RF carrier at the interbit switching instants ;
(c) Relative to the carrier, the RF phase varies linearly during each bit period $T = 1/f_b$ with total changes of $\pm 90^o$;
(d) In general f_1 and f_2 are consecutive multiples of $1/2\ f_b$; e.g. $f_1 = 2k\ f_b/2$, $f_2 = (2k+1) f_b/2$. $k = 1, 2, \ldots$

Waveform

The MSK signal can be expressed as

$$u(t) = \cos\left[2\pi f_c t + \Phi(t) \right] \qquad (5.1)$$

$$O \leq t \leq T$$

where,

$$f_c = (f_1 + f_2)/2$$

and the continuous phase function

$$\Phi(t) = \Phi(O) \pm \pi t/2T$$

A typical MSK signal for $f_1 = 2f_b$ and $f_2 = 2\frac{1}{2} f_b$ is shown in Figure 5.1 (a). Figure 5.1 (b) is a special case MSK signal and represents the minimum possible keying frequencies, i.e. $f_1 = \frac{1}{2} f_b$ and $f_2 = f_b$. It will be noted that this waveform is similar to the bifrequency baseband coding (FM), using sine rather than square waves. See Figure 2.2.

Spectra

When modulated by a random binary data having equal probabilities of 1's and O's, the single sided power spectral density is given by (26)

$$S(f) = 8\pi^2 P_c T \frac{\left[1 + \cos 2T(\omega - \omega_c)\right]}{\left[\pi^2 - 4T^2(\omega - \omega_c)^2\right]^2} \quad W/Hz \qquad (5.2)$$

where P_c = carrier power

$$\omega \geq O$$

The above expression is plotted in Figure 5.2. It is noted that most of the signal power is concentrated within a bandwidth of about 1.5 f_b.

In connection with an FDM situation the total power lying outside an allocated channel passband of $f_c \pm B_c/2$ is given by

$$P_{oB} = 1 - \int_{f_c - B_c/2}^{f_c + B_c/2} S(f)\, df \qquad (5.3)$$

which is plotted in Figure 5.3.

The area under the total power = UNITY. It is illustrated that

99 percent of the power of a non-filtered MSK signal is contained within a channel bandwidth of 1.15 f_b. This result shows that MSK requires less post modulation filtering because of the absence of significant amounts of energy outside this bandwidth. High data rates are thus possible in principle since the relatively narrow occupied bandwidth enables channels to be closely spaced without requiring critical filtering.

Error Probability

The optimum error performance of the MSK modulation has been found to be given by (27);

$$P_e \simeq \text{erfc}\sqrt{\frac{E}{N_o}} \qquad (5.4)$$

where,

E = input signal energy per bit

N_o = noise spectral density

5.3 Transmitter Design

5.3.1 General

A block diagram of the transmitter arrangement is shown in Figure 5.4. The MSK signal at the output of the modulator is translated from the IF subcarrier frequency f_s to the RF carrier

frequency f_c in the mixer. (The translation frequency f_R is henceforth referred to as the Reference Carrier). The output of the zonal band-pass filter, centred at the carrier frequency $f_c = f_R + f_s$, gives the desired RF modulated MSK signal which is subsequently amplified and transmitted.

The modulator design is based on the visualisation of MSK as a form of coherent FSK modulation which gives the signal properties noted in Section 5.2.1.

The post modulation filter is a tuned circuit designed to pass the MSK signal and suppress the reference carrier (f_R). The reduced reference carrier component is regenerated at the receiver for the detection process as explained in Section 5.4.1.

5.3.2 Modulator

A block diagram of the modulator is shown in Figure 5.5. The basic operation of the modulator is such that during any keying interval of duration T, one of two square waves at either $2f_1$ or $2f_2$ is gated to the output of a flip-flop which divides down to f_1 and f_2. This arrangement ensures the required phase continuity.

$$2f_1 = kf_b$$
$$2f_2 = (k+1)f_b \qquad (5.5)$$
$$k = 1, 2, \ldots$$

i.e. $\Delta f = f_2 - f_1 = \frac{1}{2}f_b$

The resulting spectrum is centred on the apparent subcarrier frequency

$$f_s = \frac{f_1 + f_2}{2} = \frac{(2k+1)}{4} f_b \qquad (5.6)$$

A complete description of the modulator circuit, digitally implemented for k = 4, is given in Appendix N.

It is obvious that other values of k are possible, however the

value k = 4 represents the minimum possible for the method of digital generation used.

The modulator is designed to accept a bit rate of f_b = 3M b/s.

5.3.3 Circuit Diagram

The complete circuit diagram of the transmitter, implemented with the Motorola ECL 10,000 logic family is shown in Figure 5.6. Details of some basic characteristics of the ECL logic family, relevant to the present application, are given in Appendix R.

The binary data input signal at the TTL logic level is translated to ECL logic level by U8/1 externally, and transmitted via balanced twisted pair to the transmitter. This isolates the ECL logic from the noisy TTL environment. The 120Ω resistor at the input of the receiver U1 /2, which is the typical characteristic impedance (Z_o) of the twisted pair, is necessary to minimise reflections at the receiver.

The modulator circuit is as described in Appendix N.

Oscillator

The oscillator uses an adjustable LC tuned circuit to select the 3rd harmonic of the crystal. The circuit is based on suggested designs in the ECL application notes given in (28). U1/1 is essentially a very high speed linear differential amplifier with standard ECL outputs. See Appendix R.2 for details of the differential amplifier. and Appendix R. 3 for the oscillator circuit.

Specifications

Crystal type : 1260 (60 MHz)
Amplifier gain : 14 dB
Amplifier, input impedance : 50 KΩ
Output frequency : 60 MHz

Filter

The output filter of the transmitter is shown as the single-stage LCR tuned circuit at the input of the differential amplifier U10/1.

Specifications

Amplifier gain	:	14 dB
Amplifier input impedance	:	50 kΩ
Centre frequency	:	66.75 MHz
Bandwidth	:	3 MHz

Measured Performance

The measured frequency response at the output of the amplifier is shown in Figure 5.7.

Driver

The transmitter output driver, shown in the circuit diagram, employs two differential amplifiers connected in parallel as shown. This arrangement is possible because of the open emitter follower outputs provided. See Appendix R.2. The need for the parallel connection was to obtain the required output signal power.

Transmitter Construction

The complete transmitter circuit has been built on a double sided epoxy glass PCB with an earth back plane, with particular attention paid to the layout guidelines suggested in the manufacturers

application notes (28). Basically the line lengths were kept as short as possible in order to minimise line reflections. Details of these guidelines are given in Appendix R. 4.

Transmitter Specifications

Data bit rate : 3 Mb/s
Carrier frequency : 66.75 MHz
Output signal power: 7 mW
Output carrier power: 3 mW
Off impedance : 240 Ω

5.4 Receiver Design

5.4.1 General

Figure 5.8 shows a block diagram of the receiver arrangement. The MSK signal at the IF sub-carrier frequency f_s is recovered from the incoming RF signal by the frequency down converter. The baseband clock and the reference signals required for the demodulation process are subsequently regenerated by the reference and clock recovery circuits.

Frequency Down Conversion

A block diagram of the converter is shown in Figure 5.9. The reduced reference carrier component f_R at the receiver input is detected by a high-Q tuned filter and amplified to restore the original power level. The regenerated reference carrier signal is correlated with the received signal in the mixer to obtain the desired IF sub-carrier signal.

The ECL implementation of this circuit is shown labelled in the receiver circuit of Figure 5.14.

Clock and Reference Signal Recovery

Figure 5.10 shows a block diagram of the arrangement used for the clock and reference signal recovery. The IF signal input

is doubled in frequency which results in an FSK signal having spectral lines at $2f_1$ and $2f_2$ (29). These components are extracted by the two phase-lock loop circuits to produce the two mark and space reference signals. The output of the mixer produces the frequencies $2f_1 + 2f_2$ and $2f_2 - 2f_1$, but from the properties of the MSK signal noted in Equation 5.5, $f_2 - f_1 = \frac{1}{2} f_b$. Thus the output of the low-pass filter gives the regenerated baseband clock signal $2 (f_2 - f_1) = f_b$. Figure 5.11 shows a photograph of the spectrum of the doubled MSK signal. The spectral lines referred to can be clearly seen.

The clock and reference recovery circuits are also implemented in ECL logic except for the phase-lock loops which are signetics NE561 ICs. The circuits are similarly shown labelled in Figure 5.14.

5.4.2 Demodulators

(a) Sub-optimum Correlation Demodulator

Figure 5.12 shows a block diagram of this demodulator. The principle is based on the well known two path correlation receiver for FSK signals (27). The regenerated mark and space frequency $2f_1$ and $2f_2$ are used as the coherent reference signals for the detection process. The demodulation process is based on a single bit-period and also the phase information contained in the MSK signal given by Equation 5.1 is not fully exploited ; it therefore has a lower performance than the optimum demodulator.

A complete description of the demodulator is given in Appendix P.

S/N Performance

Let T = bit period

E = signal energy per bit

N_o = noise power spectral density

f_o = filter cut-off frequency

Then, the error rate performance (P_e) of the demodulator has been found to be given by ;

$$P_e = \tfrac{1}{2}\,\mathrm{erfc}\sqrt{\frac{E}{N_o}\cdot\frac{1}{2f_oT}} \qquad (5.7)$$

The derivation of Equation 5.7 is given in Appendix P.

Circuit Diagram

The demodulator circuit is shown labelled in the receiver circuit of Figure 5.14. The filter cut-off frequency is set at 3 MHz, which gives $f_oT = 1$ in Equation 5.7. The design of this filter, which is a second-order Butterworth type, is given in Appendix S.

(b) Differential Strobe Demodulator

Principles

The MSK signal waveform for an arbitrary data sequence is shown in Figure 5.13 (a). It is observed from this waveform that within a bit period T, f_1 contains an even number of half-cycles and f_2 an odd number ; the polarity of the shaded $\frac{1}{2}$ cycle of f_1 is thus the same as the corresponding half-cycle in the previous bit but in the case of f_2 the shaded half-cycle element is opposite to the corresponding element in the previous bit. Thus the symbol value of a current transmitted data can be uniquely determined by comparing the polarity of the current half-cycle element with the previous one.

Circuit Diagram

Figure 5.13 (b) shows the circuit diagram of the demodulator which implements the above principle. The demodulator compares each polarity decision with the previous one at time t = 8T/9 when

the maximum signal is available (see Figure 5.13 (c)), in an effectively differential decoding process. A 'mark' is detected if the polarities are the same and a 'space' if opposite.

S/N Performance

The filter limits the additive noise into the demodulator and hence determines its S/N performance. In the present investigation, a low pass filter with a cut-off frequency $f_o = 3f_b$ has been used ; this passes the signal contained in the band to the first upper minimum of the MSK spectra. Ideally, a bandpass filter with bandwidth $B_c \simeq f_b$ could be used since, as noted in the properties of MSK given in Section 5.2, about 99% of the signal energy is contained within this band. Such a filter has been built however experimental tests using this band pass filter had not been carried out at the time of writing this report.

The theoretical error rate performance of this demodulator for $f_o = 3f_b$ is given by:

$$P_e = \text{erfc}\sqrt{0.323\ (\frac{E}{N_o})} \quad - \quad \text{erfc}^2\sqrt{0.323\ (\frac{E}{N_o})} \qquad (5.8)$$

Derivation of Equation 5.8 is given in Appendix Q.

5.4.3 Circuit Diagram

Figure 5.14 shows the complete receiver circuit diagram, using both the correlation demodulator and the differential strobe demodulator. The various units of the receiver system, described earlier are shown labelled in the diagram. Design of the low pass Butterworth filters are given in Appendix S. The principles of the frequency doubling circuit, labelled 'X2' in the circuit diagram is described below:

Frequency Doubling Circuit

The waveforms of Figure 5.15 illustrate the frequency doubling principle. The frequencies of the waveforms A and B are the same, however with B delayed from A as shown, a modulo-2 addition of the two waveforms results in a signal waveform at twice the frequency. The pulse width of the doubled signal is determined by the delay between A and B.

The circuit formed by U3/2, U3/3 and U2/2, shown in Figure 5.14, implement the above principle. U3/2 and U3/3 and the two respective feedback resistors make up a Schmitt trigger which speeds up the edges of the incoming MSK signal to obtain the square waves as shown in Figure 5.15. The Exclusive-OR gate provides modulo-2 addition to obtain the doubled frequency output. Thus the input signal sequence comprising f_1 and f_2 is doubled to obtain a sequence of $2f_1$ and $2f_2$ at the output of U2 /2. The delay is set to give $t_d = 1/(4f_1) = 0.1T$.

Receiver Construction

The complete receiver circuit has been constructed on a similar double sided PCB as the transmitter, and following the same layout guidelines as given in Appendix R.4.

5.4.4 Measured Performance

Measurements were made to verify the theoretical results for the correlation demodulator and the filter threshold demodulators. All measurements were made using the regenerated clock signal. The measurement system is fully described in Section 5.6. The minimum receiver input signal power for satisfactory operation of the correlation demodulator was measured as 0.25mW, which corresponds to a transmitted signal degradation of about 15 dB.

Figure 5.16 (a) shows the theoretical curves given by Equations 5.7 and 5.8 for the two demodulators respectively. The optimum detector case is also shown for comparison. Experimental results for Om and 100m cable lengths are shown in Figure 5.16 (b). It is seen that the results for Om in both cases closely agree with the corresponding theoretical values. Compared with the optimum results however, it is seen that the correlation demodulator gives about 3 dB performance degradation and the differential strobe about 5 dB degradation. The experimental results for the 100m cable length show that the increase in S/N relative to Om is greater for the differential strobe demodulator than the correlation demodulator. The S/N increase for the correlation demodulator is accounted for by the cable loss which is 2.4 dB at the operating frequency of 66.75 MHz. The differential strobe demodulator gives an increase of about 3.5 dB : the additional loss is explained by the poor jitter performance of this demodulator caused by the relatively critical peak sampling interval as shown in the signal eye diagram of Figure 5.13 (c). The result is that deviations from the sampling instant reduce the noise margin and hence a degradation of the S/N performance.

5.5 Line Coupling Design

5.5.1 Receiver Coupling

Figure 5.17 shows the network used for coupling the receivers to the transmission line.

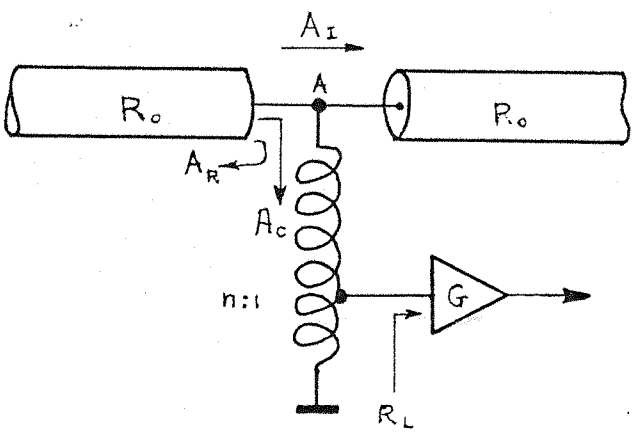


Fig. 5.17

Receiver Coupling Network

It comprises a simple unmatched transformer with a variable tap ratio to give the required tap losses. It is treated as a high impedance broadband device without selective tuning.

Tap Losses

Three kinds of losses are defined which relate the mismatch effect of the device on the transmission line. These are respectively, the coupling loss (A_c), insertion loss (A_I) and return loss (A_R). See Figure 5.18.

The voltage ratios associated with these losses are respectively defined as ;

coupling loss ratio β_c = transmitted voltage ratio x received load voltage ratio

insertion loss ratio β_i = $\frac{\text{voltage transmitted from point A}}{\text{voltage incident at point A}}$

return loss ratio β_r = $\frac{\text{voltage reflected from point A}}{\text{voltage incident at point A}}$

From the above definitions it is seen that

$\beta_i = T_o$ = transmission coefficient at A

$\beta_r = r_c$ = reflection coefficient at A

A diagram of the tap showing the various losses is shown in Figure 5.18.

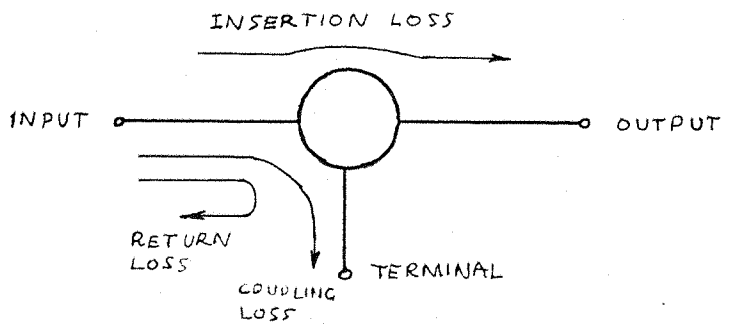


Fig. 5.18.

Tap Losses

In terms of the parameters given in Figure 5.17, the respective voltage ratios are given by ;

$$\beta_c = \frac{2nR_L}{R_o+2n^2R_L} \qquad (5.9)$$

$$\beta_i = \frac{2n^2R_L}{R_o+2n^2R_L} \qquad (5.10)$$

$$\beta_r = \frac{-R_o}{R_o+2n^2R_L} \qquad (5.11)$$

The derivations of the above equations are given in Appendix T.

A plot of the tap loss A_c, A_I and A_R as a function of tap ratio n, for $R_o = 50\,\Omega$ and $R_L = 100\,\Omega$ is shown in Figure 5.20. The expanded insertion loss curve is shown in Figure 5.21.

It is observed from the above graphs that as n increases, A_c increases but A_I decreases. A_R, which is a measure of the tap reflections is seen to increase rapidly with n. Generally a higher value of A_R is desired to keep reflections to a minimum.

Total Transmission Loss

Considering the passive highway arrangement with N such taps connected as shown in Figure 5.19, the total signal loss (in dB) to the output of the Nth terminal is given by

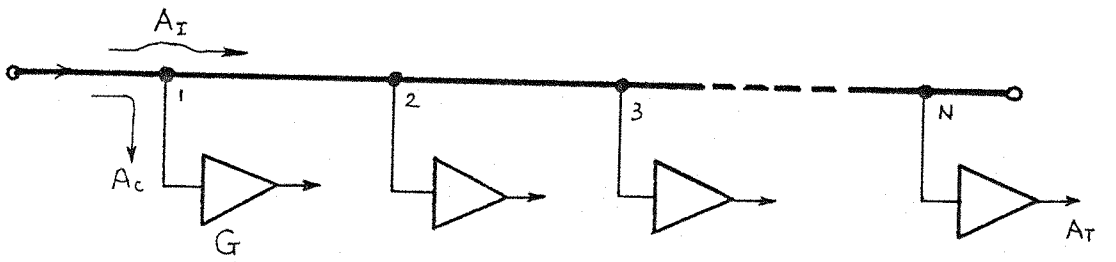
$$A_T = \left[(N-1)A_I + A_c + A_L\right] - G \qquad (5.12)$$

$$= A_M + A_L - G$$

where A_M is the total mismatch loss given by

$$A_M = (N-1)A_I + A_c \qquad (5.13)$$

In practice it would be desired to keep A_M low.



Tapped Transmission Line

Fig. 5.19

Tap Design

It is seen from Equations 5.9, 5.10 and 5.13 that the total mismatch loss A_M is dependent on both the total number of loads and the tap ratio n. For a given total number of loads, the tap ratio n required to give the minimum possible total mismatch loss is found to be given by

$$n = \sqrt{(2N-1)R_o/2R_L} \qquad (5.14)$$

The above expression is found by making $dA_M/d_n = O$.

The parameters used to find n were ;

$N = 50$

$R_o = 50\,\Omega$

$A_L = 2.4$ dB at 66.75 MHz

$R_L = 100\,\Omega$

$G = 14$ dB

Note. The relatively small value of R_L is because of the ECL amplifier configuration used, which requires a low value of resistance at the input to provide the signal and bias voltage at both of its complementary inputs. See Appendix R. 3.

Using the above parameters and equations, the following were obtained ;

$n = 4.97$ (a value of $n = 5$ was used for convenience)

$A_I = 0.09$ dB

$A_C = 14.0$ dB

$A_R = 40.0$dB

See Appendix V for details of Tap.

From equation 5.12 the total transmission loss equation thus becomes ;

$$A_T(dB) = 0.09\ (N-1) + 2.4 \qquad (5.15)$$

Measured Performance

Measurements of the tap losses to verify the predicted performance were carried out using the HP Vector Voltmeter Type No. 8405A.

Figures 5.22 and 5.23 show results of coupling loss and insertion loss measurements of the tap as a function of frequency. In both cases the results give the predicted values at the operating frequency of 66.75 MHz. The increase of insertion loss as the frequency decreases is expected since the effective inductive reactance of the tap is decreased . The coupling loss however tends to remain fairly constant over the range of frequencies considered.

The results obtained confirm the theory but suggests that it is not valid at the low frequencies where the shunt inductance tends to load the line.

5.5.2 Transmitter Coupling

The transmitter coupling network is shown in Figure 5.24. The principle of operation of the arrangement is such that when a transmission is requested, the control signal switches on the constant current generators which drive sufficient current to forward bias the PIN diodes. The low forward bias resistance of the diodes allow the RF signal from the amplifier to be transmitted through the wide-band transformer to the line. At the end of the transmission the current sources are turned off by the control signal to reverse bias the diodes. A very high impedance load is presented to the line in this state, thus overcoming the problem of the low off-state output impedance of the transmitter.

PIN Diode Characteristic

Figure 5.25 shows a typical characteristic curve of the PIN diode. It is seen that for a change of current from 1μA to 100 mA the diode resistance will change from over 10K to about 1Ω.

Current Generator

A circuit diagram of the current generator is shown in Figure 5.24 (b). It is biased such that the off-state current is less than 1μA and the on-state current is 100mA. The generator is ON when the control voltage (V_c) is low and OFF when V_c is high.

Output Transformer

Figure 5.26 shows the circuit and wiring diagrams and coil data of the balun transformer used. It consists of a single twisted pair winding with an extra length of winding added to complete the magnetising current path. Design of the transformer was carried out experimentally based on the guidelines given in (30). The main requirement was to obtain a flat response over the frequency band formed by the main signal lobe, i.e. 65.5 MHz

to 70.0 MHz. Twisted pair wires were used to improve the high frequency response of the transformer by ensuring close coupling between primary and secondary windings to reduce interwinding capacity.

Measured Performance

The measured characteristics of the overall coupling network is given below ;

low frequency cut-off f_L = 20.5 MHz
high frequency cut-off f_H = 95.5 MHz
off-state impedance presented to the line = 45.5 kΩ
insertion loss of PIN diode = 1.0 dB

5.6 Experimental Loading Tests

5.6.1 General

This section describes the procedures and tests carried out on a 105m length of coaxial cable (Andrew flex $\frac{1}{2}$" type LDF4/50) to evaluate the modulated carrier link performance with the connection of several transformer tap loads. The transformer loads are described in Section 5.5. Because of the relatively high impedance and low insertion loss of the transmitter coupling, in comparison with the receiver tap insertion loss, the measurements described in this section assumed their effect on the overall line loading to be negligible, thus only the receiver coupling is used.

All tests were carried out with a continuous pseudorandom binary data sequence at a rate of 3 Mb/s.

The results are presented as error rate against S/N between a transmitter at one end of the line and a receiver at the other end.

5.6.2 Measurement System

The measurement system, which is similar to that used in the baseband tests, is shown in Figure 5.27. Noise is coupled into the receiver via a wide band transformer, having similar characteristics as the transmitter coupling transformer. The cable was in short sections of 10m, 15 m and 20m lengths and connected via PCB modules each of which provided a through connection in 50Ω stripline form to match the cable. These boards were used as the tapping points for simulated terminal loads. Details of the performance of the noise generator and the PCB modules are given below ;

Noise Generator

Noise bandwidth : 50 MHz
Centre frequency : 60 MHz
Maximum output power into 50Ω: 25 mW

PCB Module

Insertion loss : 0.01 dB

A complete description of the noise generator and amplifier circuits is given in Appendix U. Further details of the PCB module are given in Appendix V.

5.6.3 Test Procedures

Calibration

Before commencing the error rate measurements, the set up was calibrated for 0 dB S/N ratio. The definition of S/N ratio used is that used in the previous baseband tests ;

$$\frac{S}{N} = \frac{\text{signal power at the transmitter end}}{\text{Noise power injected at the receiver}}$$

Referring to the link diagram of Figure 5.27, the following procedures were followed :

1. cable is replaced by a very short length of line (Om) ;
2. signal power at the transmitter end A is measured ;
3. with the noise source cut off, the signal power at the receiver input is measured and noted ;
4. the transmitted signal is cut off and the noise source gain and attenuation settings are adjusted to give the same power at receiver input B as recorded in (3). This setting then corresponds to the O dB S/N ratio condition.

S/N Ratio Measurement

With the Om line replaced by the test cable, the general procedure followed was to connect the required number of loads in increasing steps and for each number of loads, measure the error rate by selecting S/N ratios in appropriate steps with the attenuator.

5.6.4 Results

Figures 5.28 and 5.29 show the results of error rate tests for various loads using the correlation demodulator and the differential strobe demodulator respectively. The general trend of the two sets of results is evident ; that is as the number of loads is increased, the S/N degradation increases.

The relative increase in S/N w.r.t. Om to give a constant error rate of $P_e = 10^{-5}$ for both demodulators is shown in Figure 5.30. These results are derived from the respective curves of Figures 5.28 and 5.29. The theoretical total signal loss as the number of loads is increased, given by Equation 5.15, is also shown for comparison. It is seen that the results for the correlation demodulator closely agree with the theory, which

confirms that signal degradation due to loading is mainly caused by the insertion loss of the taps. The results for the filter threshold demodulator however show that the total loss as the number of loads is increased is not accounted for by the tap insertion loss only. As noted in Section 5.4.6., this additional loss is accounted for by the poor jitter performance of this demodulator. This assertion is further confirmed by the larger gradient of the results because the effect of jitter would increase as the number of loads is increased. The results show that on average there is an additional S/N degradation of about O.O3 dB for each additional load connected, in addition to that due to the line and tap insertion loss.

5.7 Conclusions

The sub-optimum correlation demodulator has been shown to give superior performance over the differential strobe demodulator. The additional degradation of the latter has been found to be due to its susceptibility to the effects of jitter and it increases with number of loads.

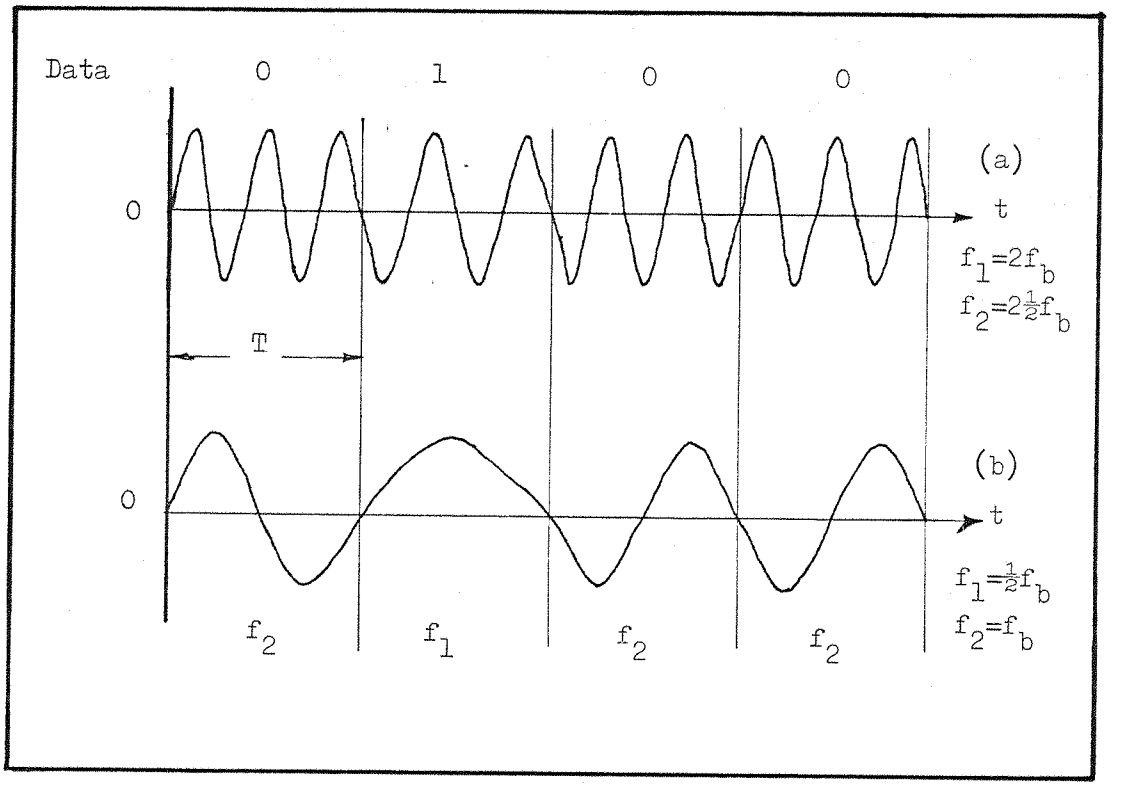
Results of the loading tests have shown that for the correlation demodulator, the S/N increase due to loading is accounted for by the respective insertion loss of the loads which agrees with the theoretical prediction. This result is rather encouraging for it validates the main predicted behaviour of the modulated carrier system ; i.e. the minimisation of signal loss due to line distortion effects by the use of narrow band signalling.

The tapped transformer network used has proved to be a simple and effective method of coupling the line to the receivers. The added advantage of its predictable behaviour shows that it is a viable alternative to the more sophisticated commercial couplers.

The simple PIN diode arrangement has facilitated the direct coupling of the transmitter to the line, with a transmitted signal loss of only 1 dB when active, and negligible disturbance to the line when in the off-state. The additional cost of the transformer and control circuitry required is however offset by the apparent power gain of about 14 dB which represents the additional power that would be required to overcome the coupling loss, if the same technique as for the receiver coupling had been used.

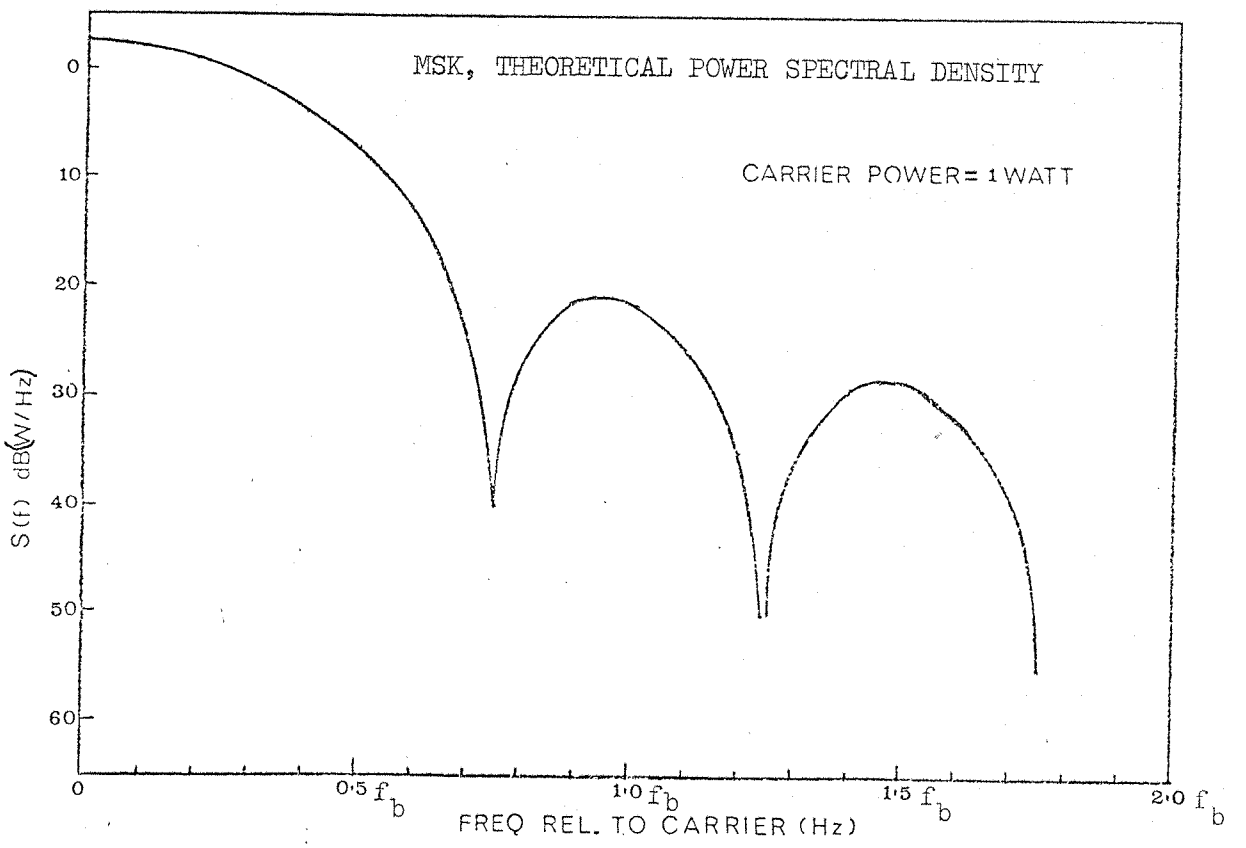
The measured tolerable total transmission loss of about 15 dB and the tap loss of O.1 dB, shows that up to 100 terminals can be readily accommodated on a transmission line length of 200m. This compares with the baseband system of Chapter 3, which shows that a similar number of transformer coupled terminals can be accommodated with a total loss of about 15 dB. (See Table 3.1). However, the above results of this chapter show that potentially, a modulated carrier system can be designed to accommodate more terminals on the highway than the baseband system, because of the added advantage of reduced signal distortion effects and the predictable performance.

One important outcome of this study has been the successful implementation of the complete transmitter and receiver system in an all digital form using ECL logic. It is appreciated, however, that implementation of the filters and amplifiers has been possible because of the less stringent band width and power requirements of the experimental system. In a practical system however the use of conventional filters and amplifiers would be recommended.



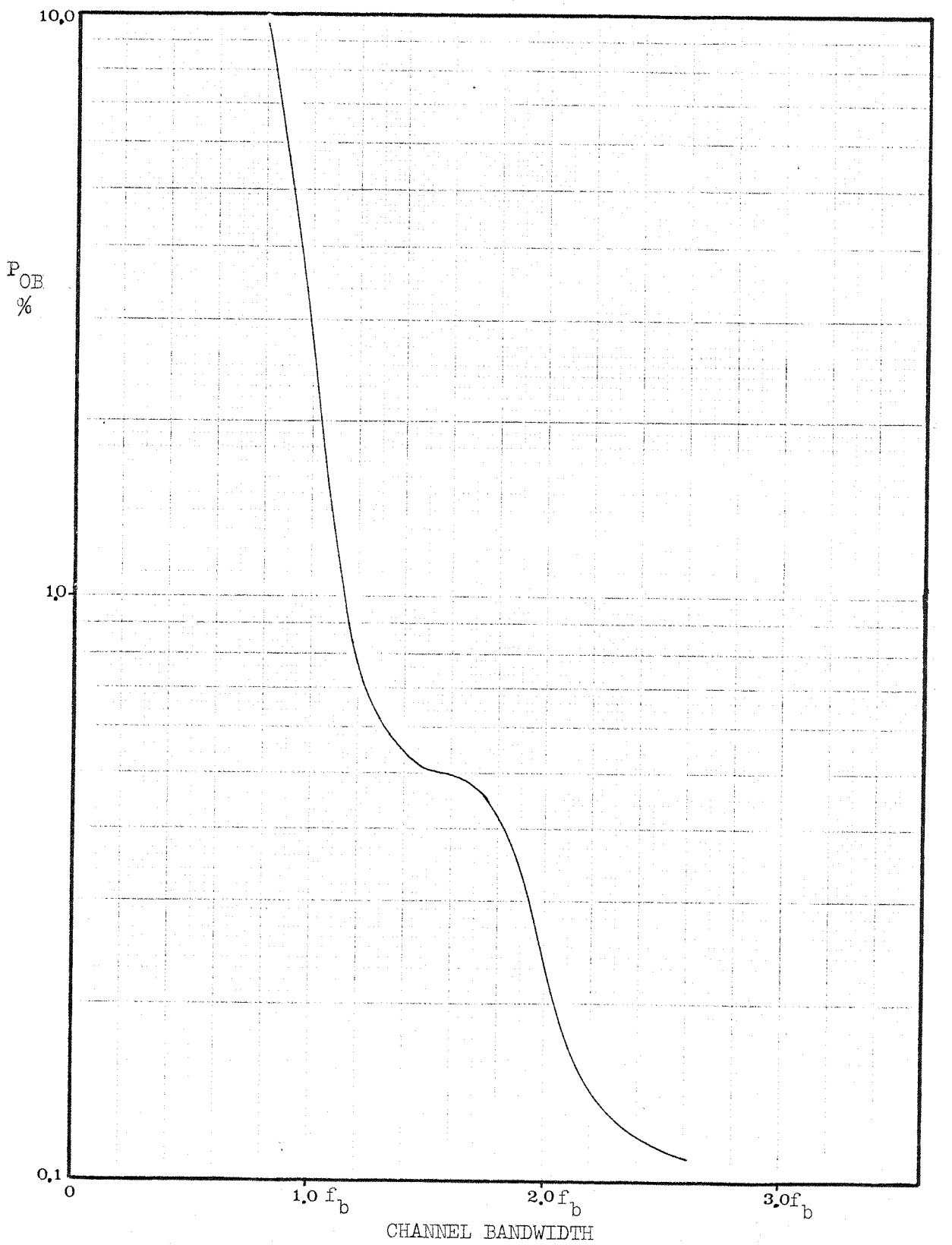
MSK Signal Waveforms

FIG 5.1



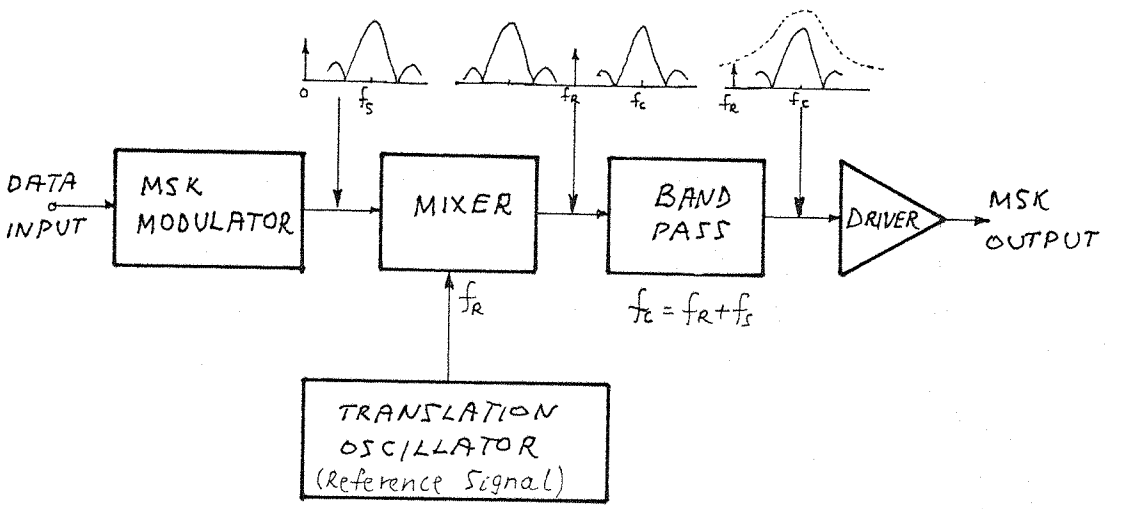
MSK Spetral Density

FIG 5.2



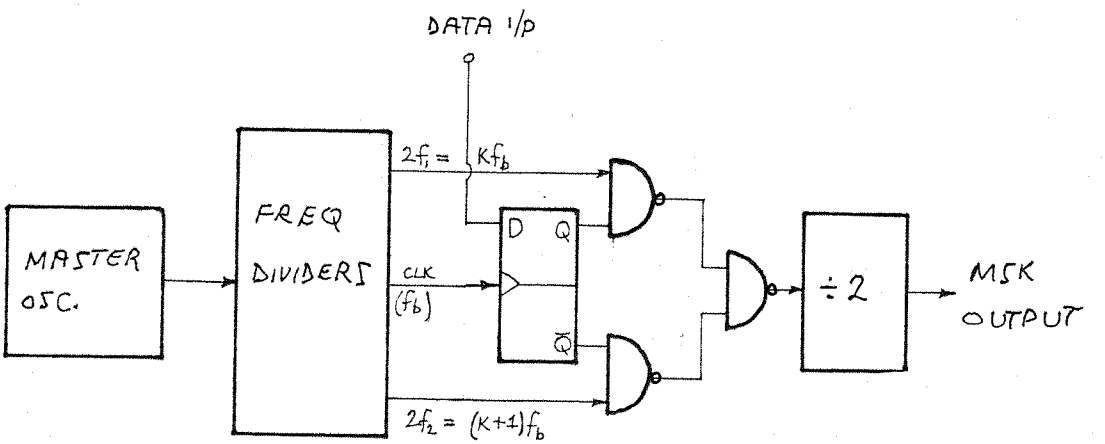
% Power Outside of Channel Bandwidth for MSK Signal

FIG 5.3



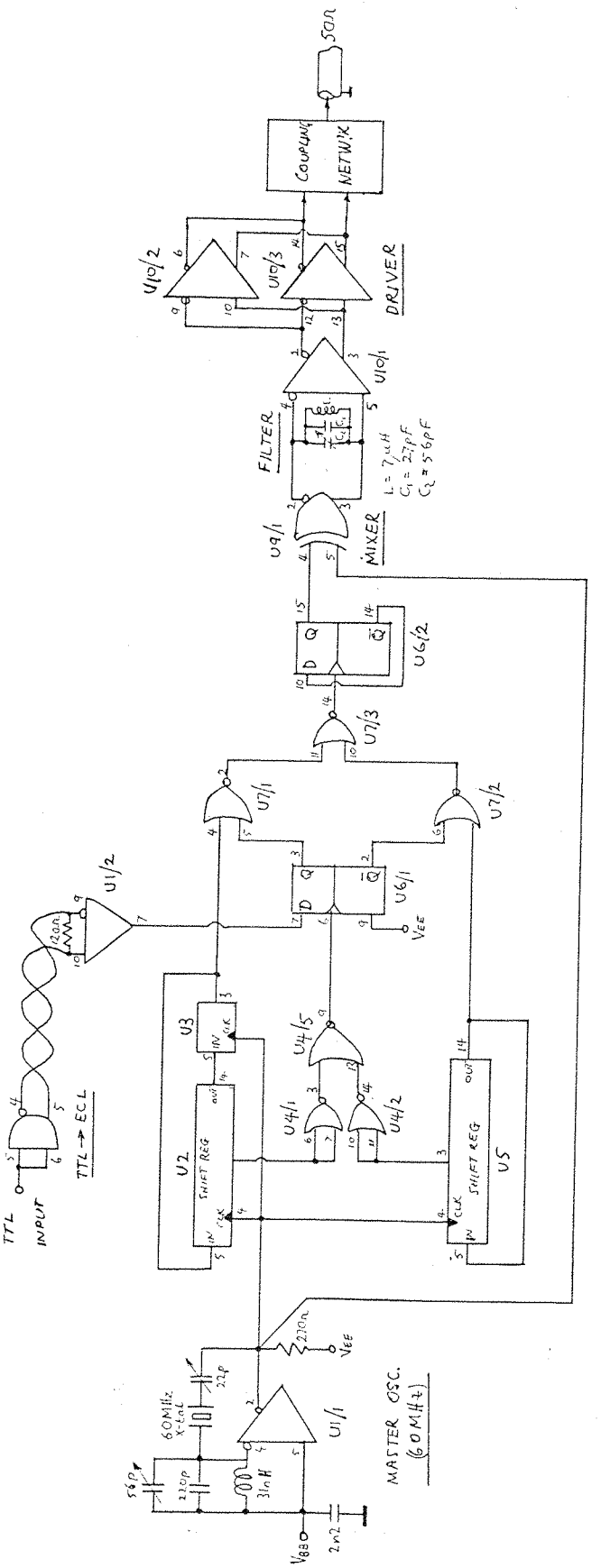
Transmitter Block Diagram

FIG 5.4



Modulator Block Diagram

FIG 5.5



IC'S

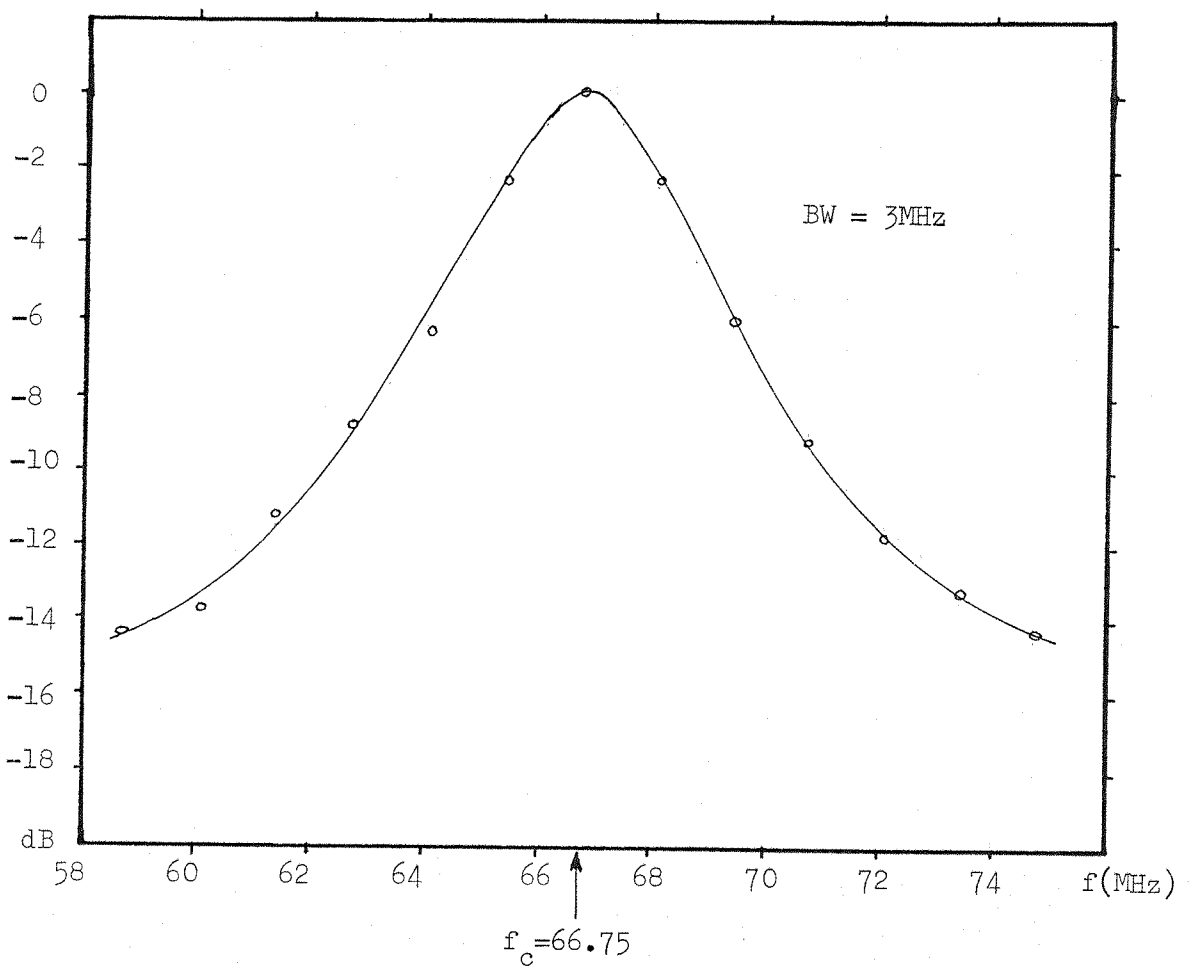
U1 - 10116	U6 - 10131
U2 - 10141	U7 - 10102
U3 - 10141	U8 - 10124
U4 - 10102	U9 - 10107
U5 - 10141	U10 - 10116

NOTE: All Outputs are Connected through a 470Ω resistor to V_{EE}, Except ~~, indicated otherwise.

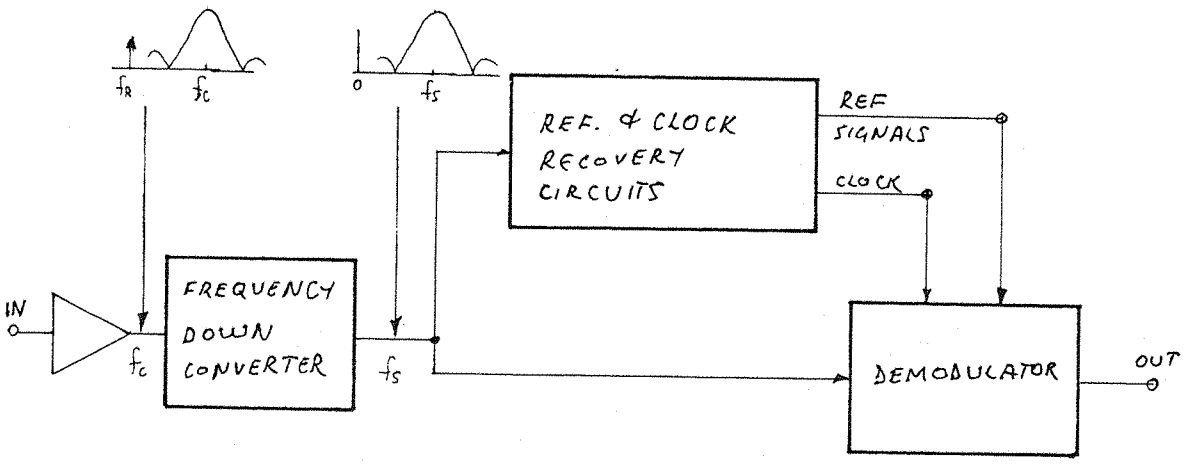
$V_{EE} = -5.2V$
$V_{BB} = -1.3V$

MSK Transmitter

FIG 5.6

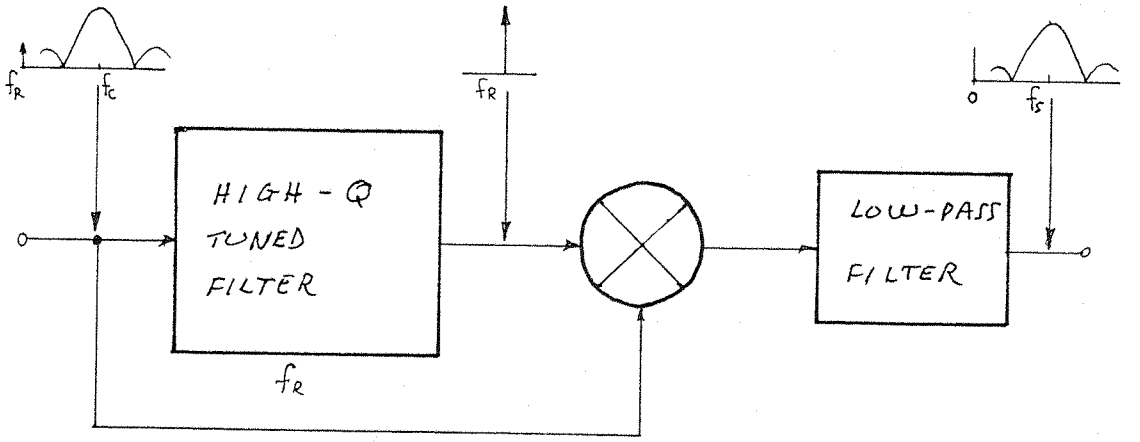


Measured Frequency Response of Transmitter O/P Filter FIG 5.7



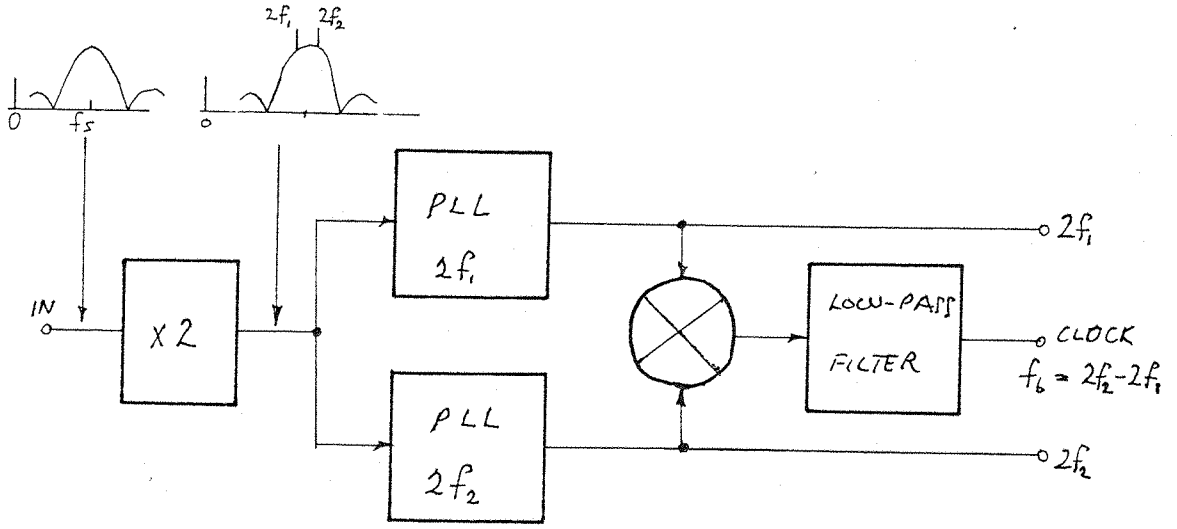
Receiver Block Diagram

FIG 5.8



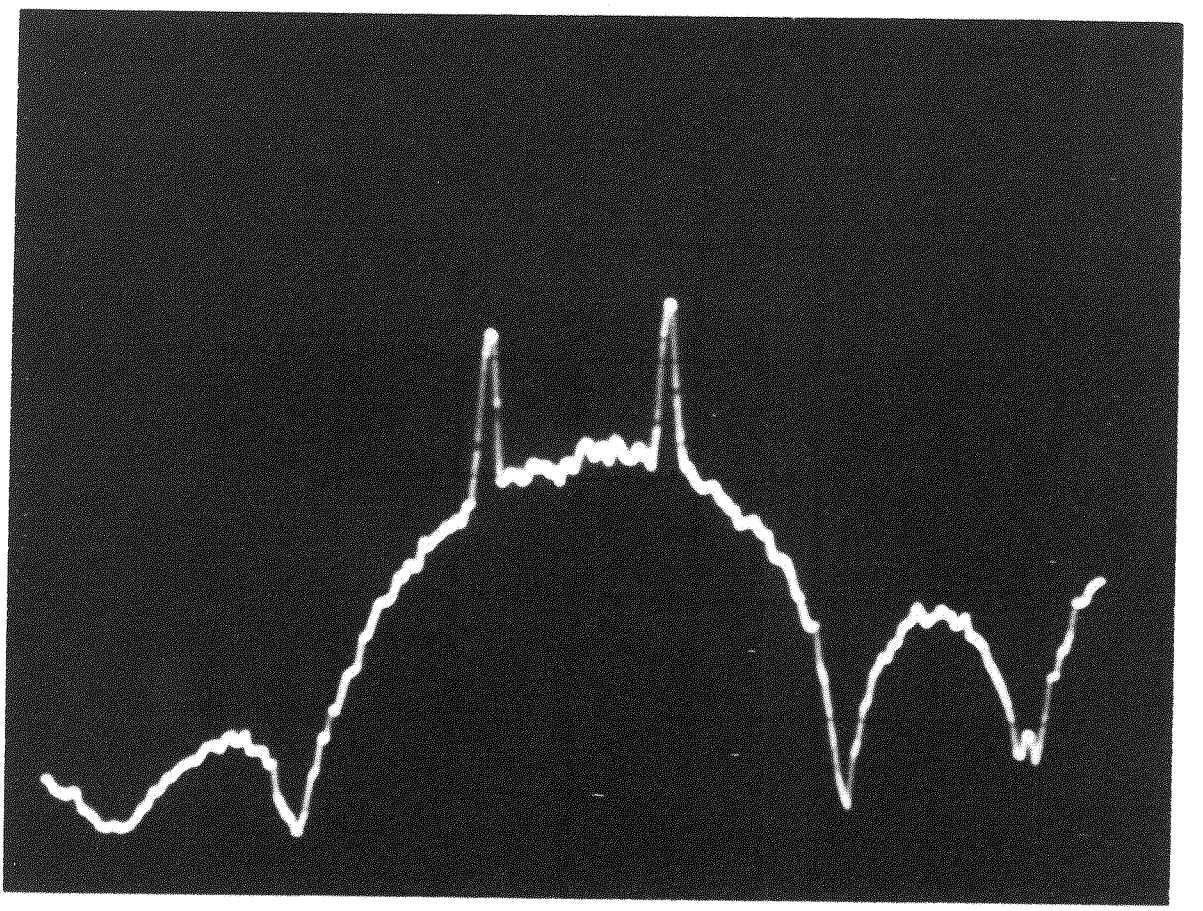
Frequency Down Conversion

FIG 5.9



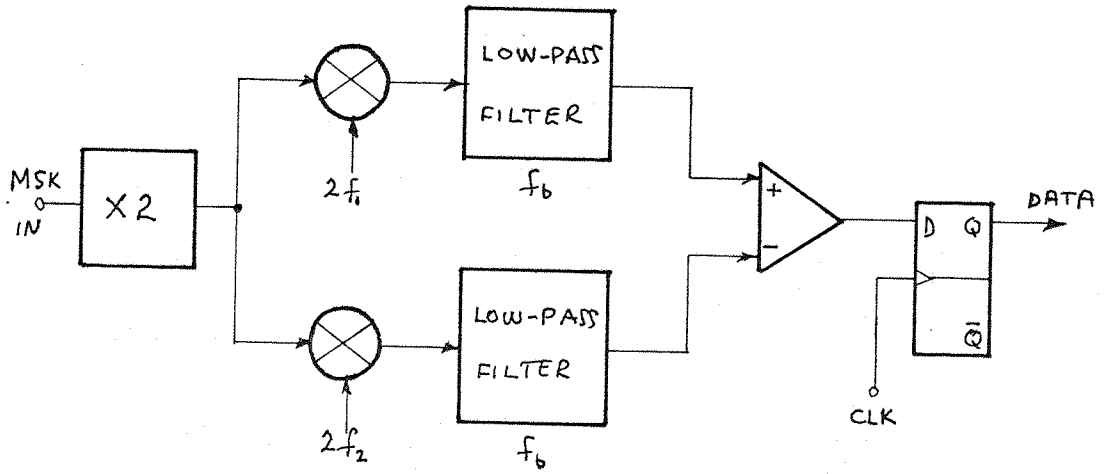
Clock and Reference-Signal Recovery

FIG 5.10



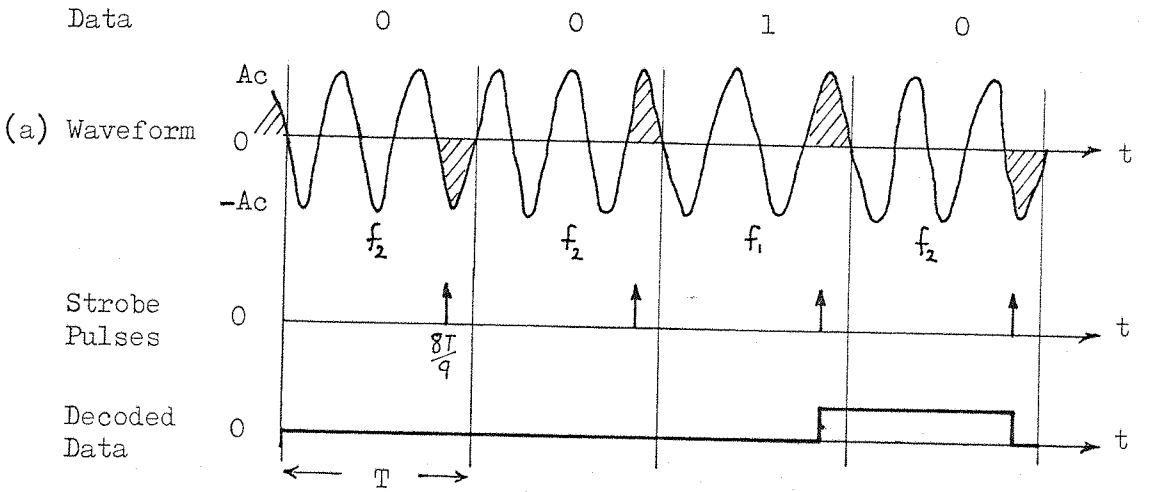
FSK Signal ($f=f_b$) Showing Spectral Lines at $2f_1$ and $2f_2$.

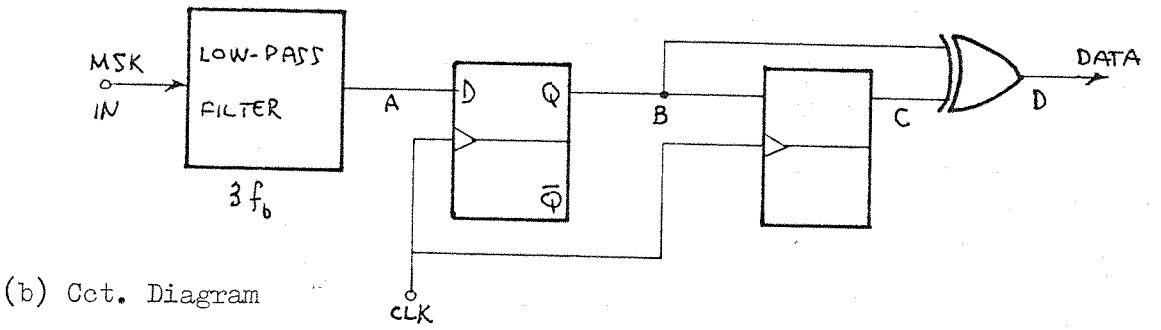
FIG 5.11

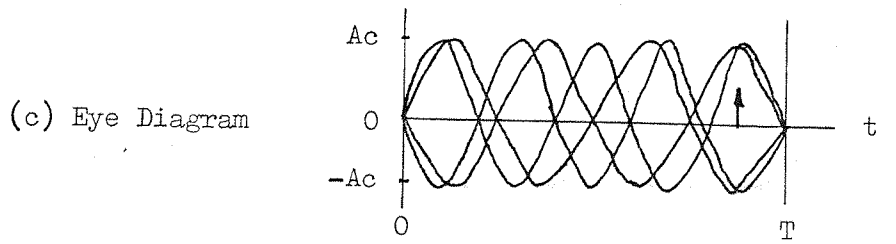


Correlation Demodulator

FIG 5.12

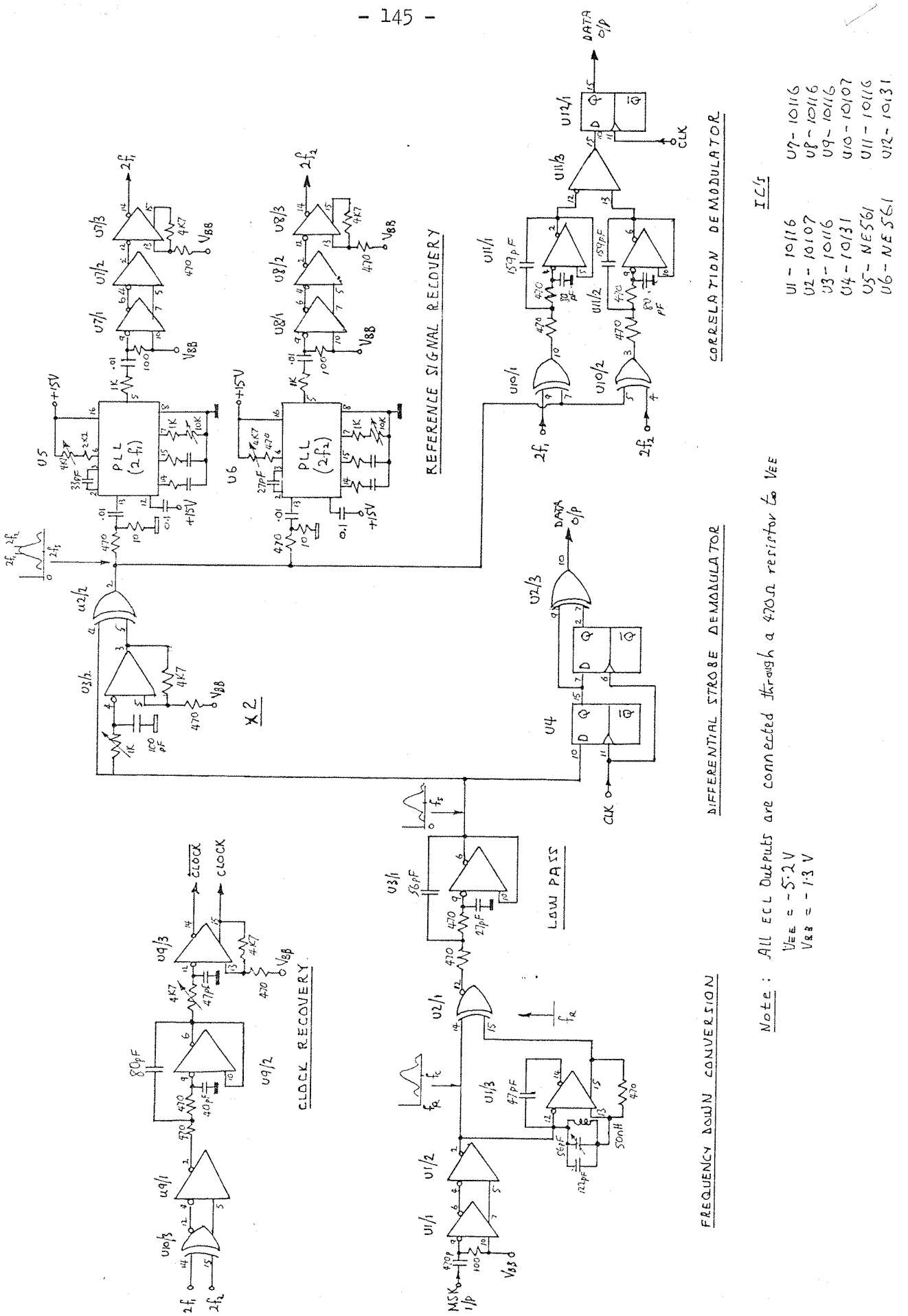






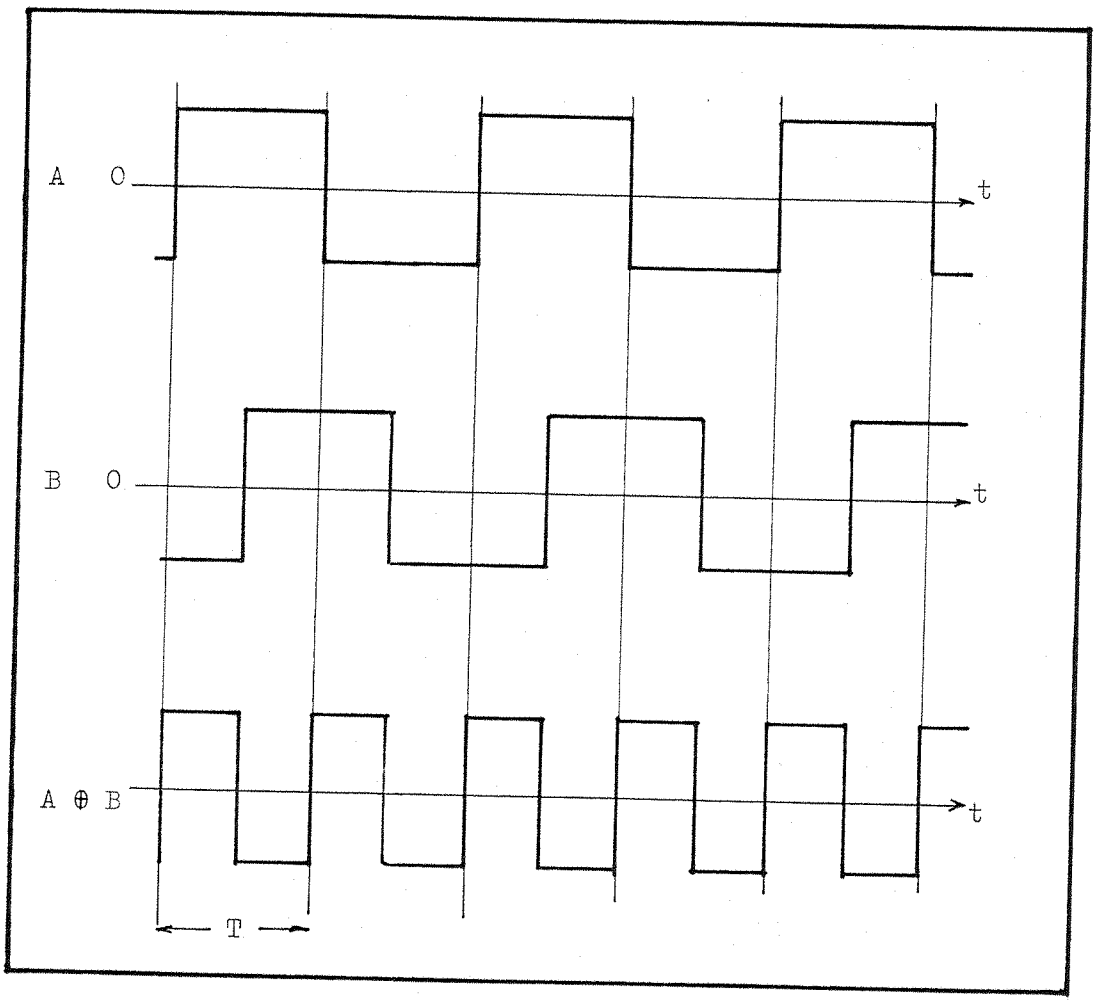
Principles of Differential Strobe Demodulator

FIG 5.13



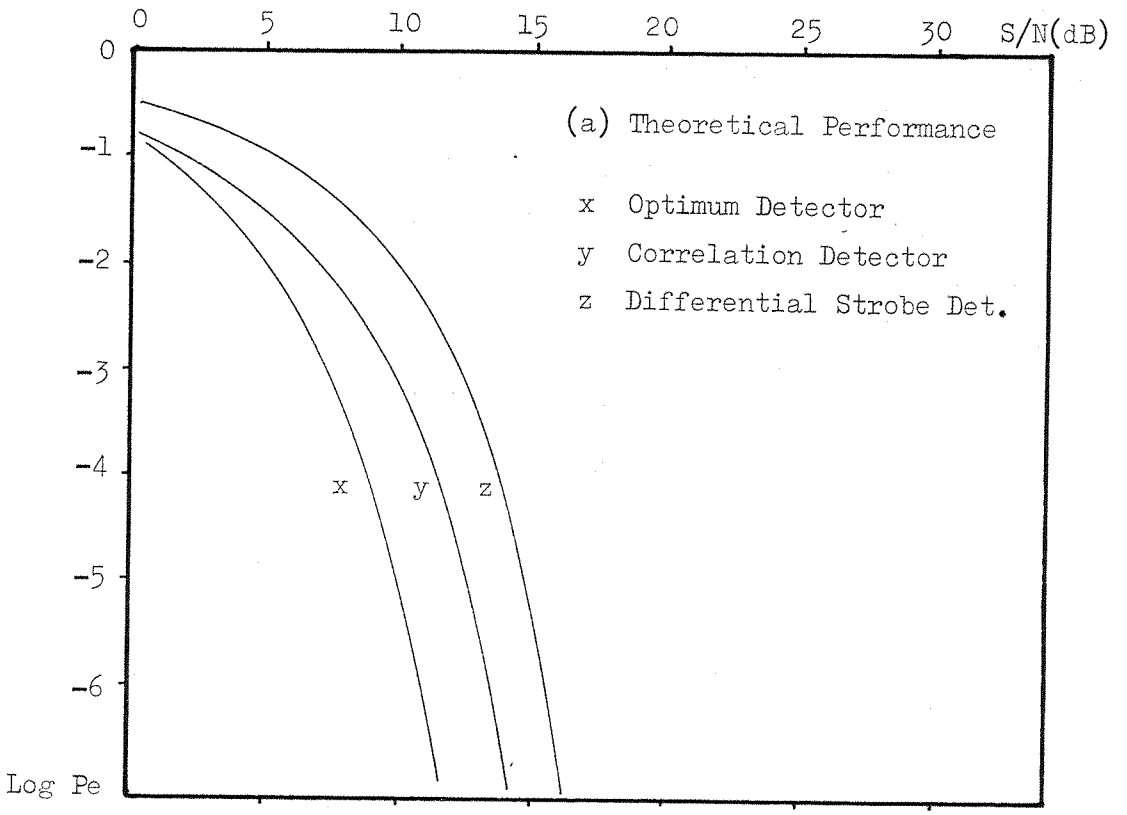
MSK Receiver

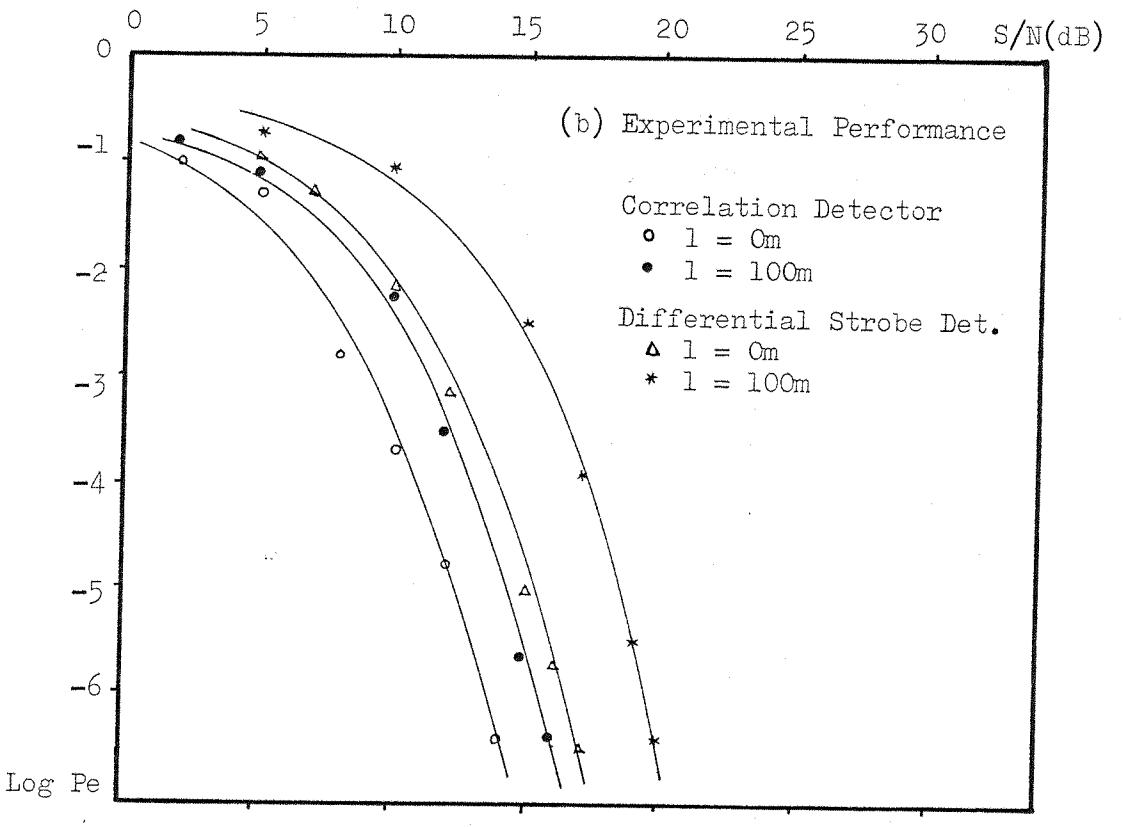
FIG 5.14



Frequency Doubling Principle

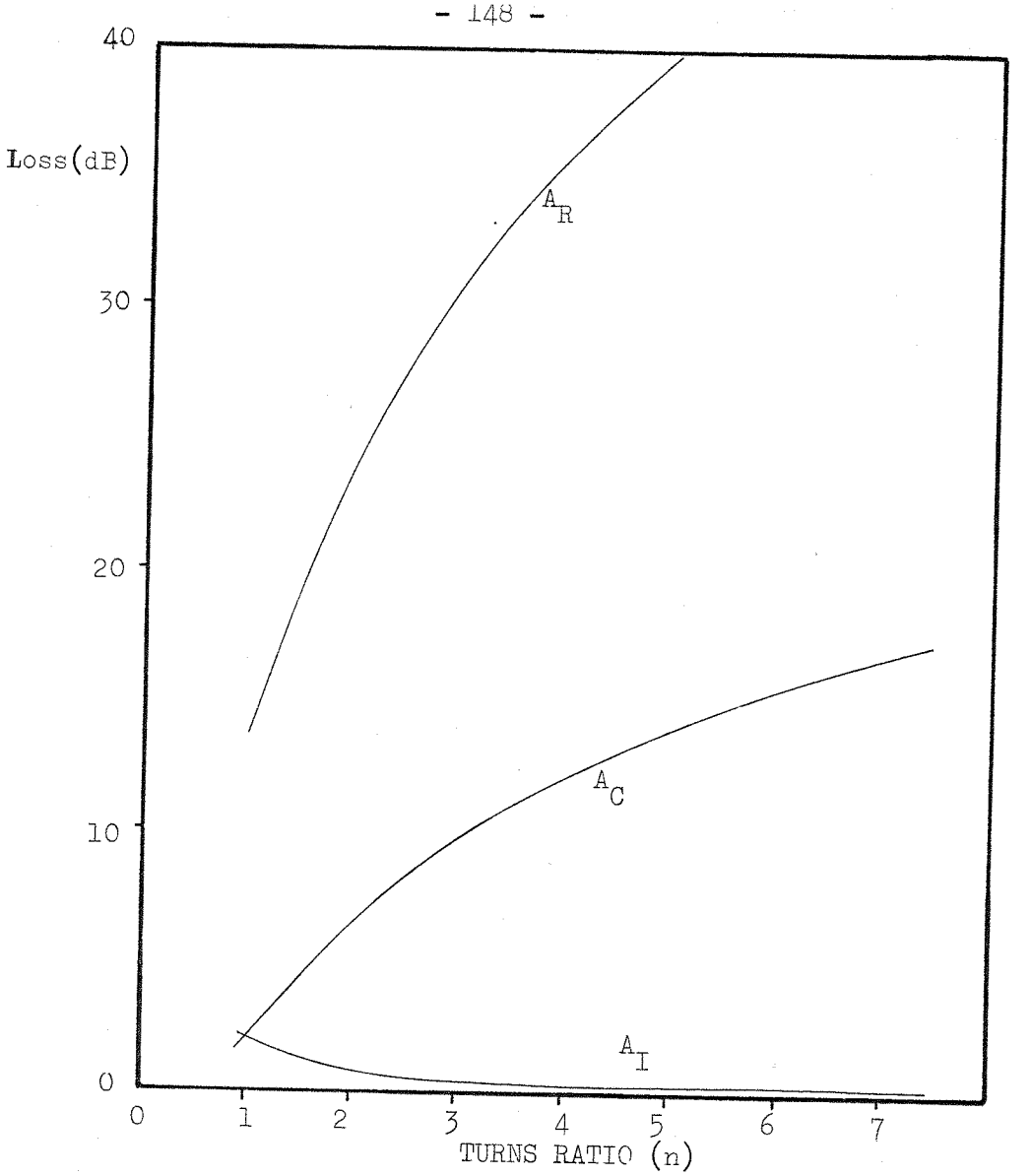
FIG 5.15





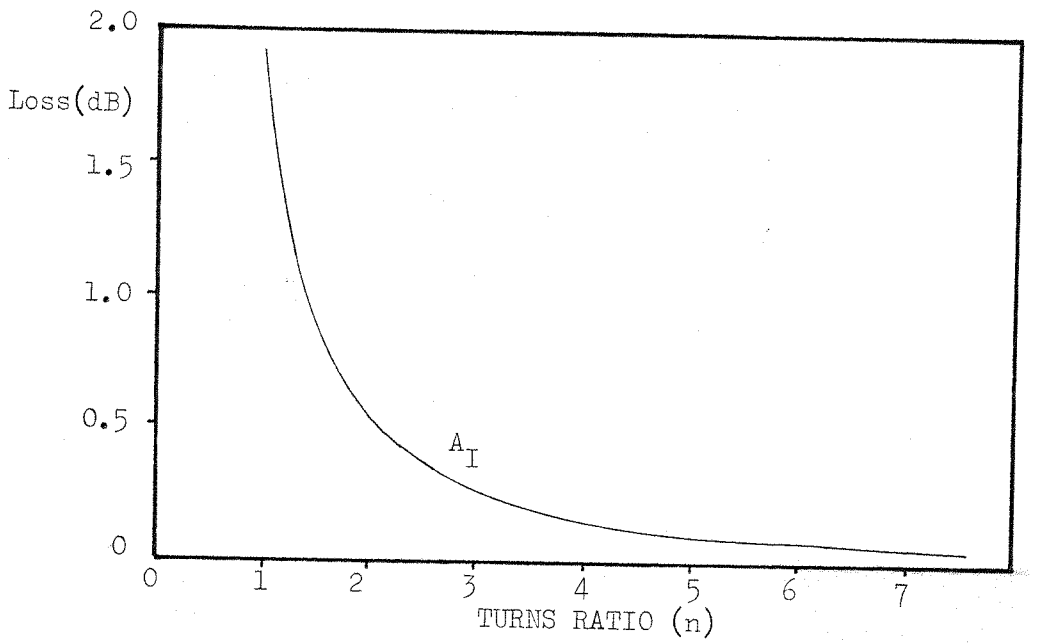
Theoretical & Experimental Performance of Correlation Demodulator and Differential Strobe Demodulator.

FIG 5.16



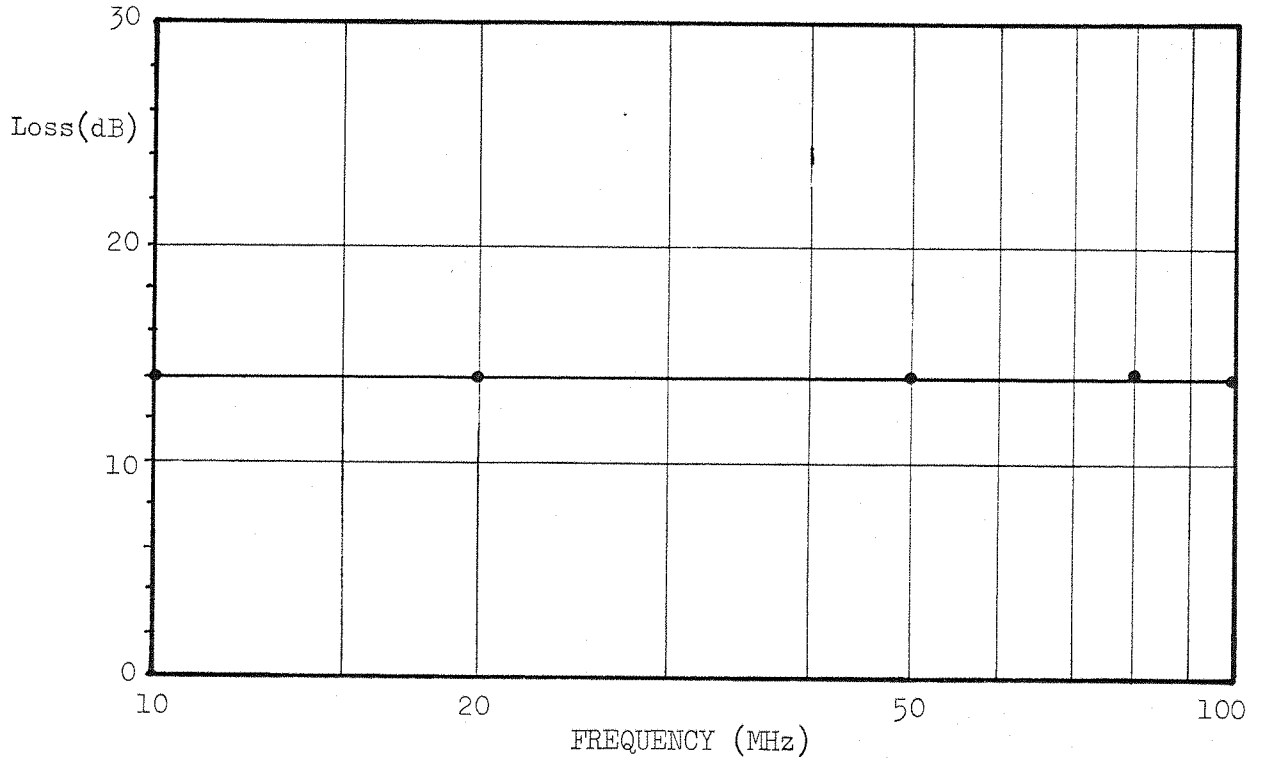
Transformer Tap Losses

FIG 5.20



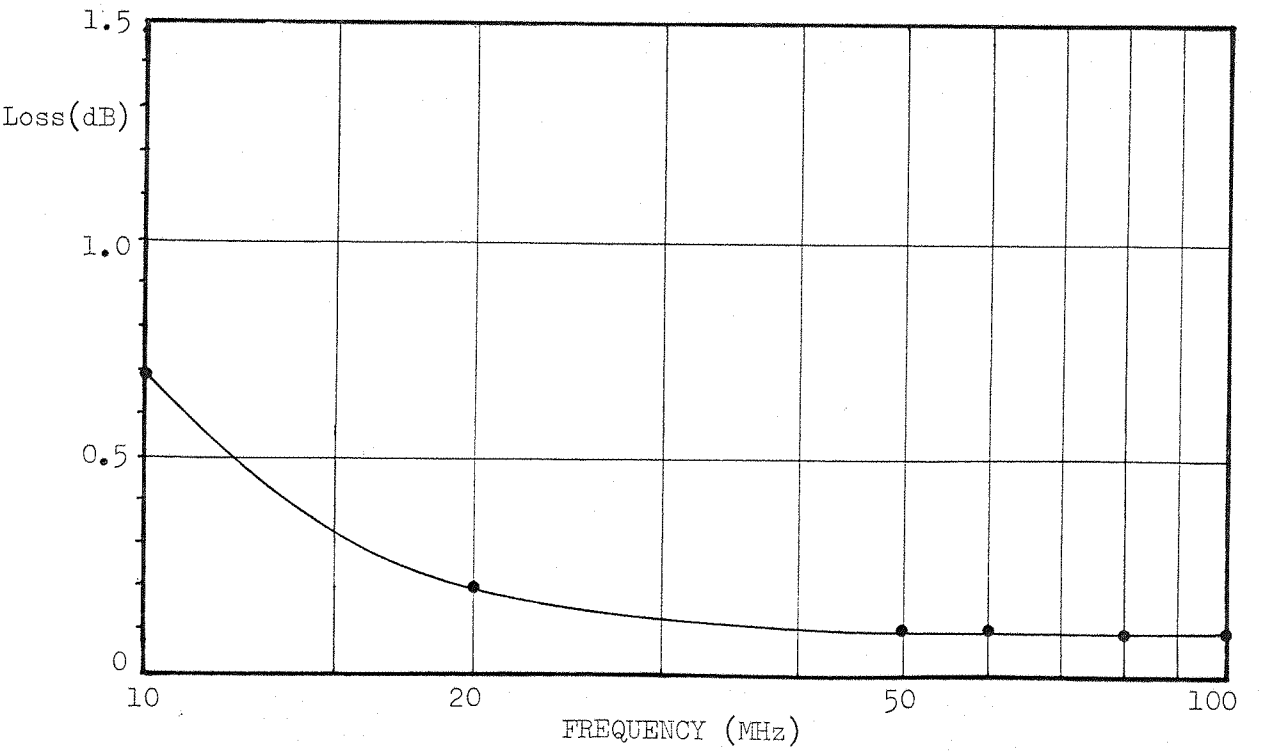
Tap Insertion Loss

FIG 5.21



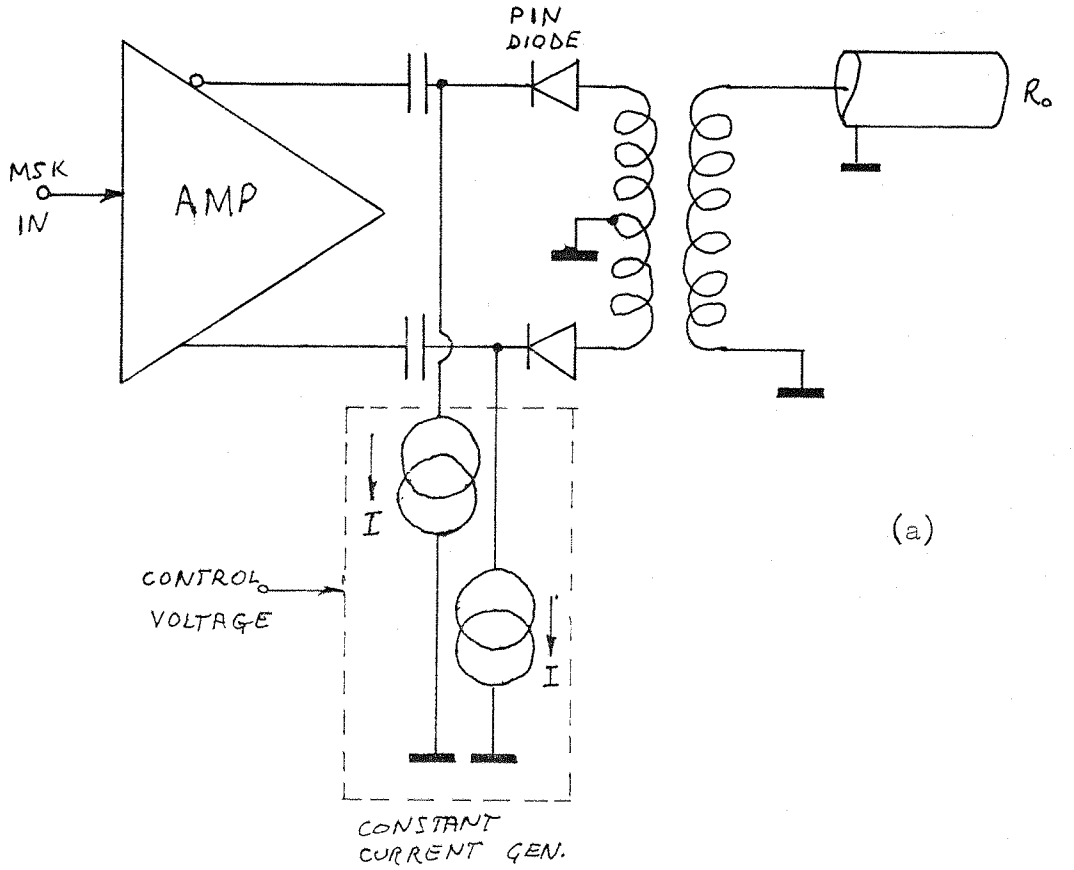
Coupling Loss Response of Transformer Tap

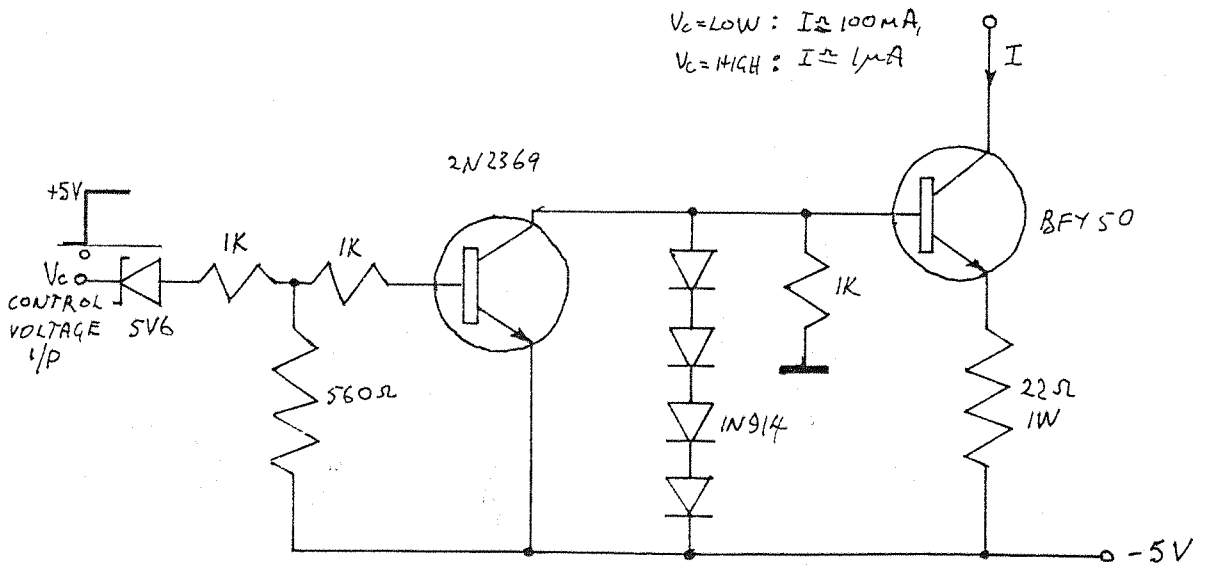
FIG 5.22



Insertion Loss Response of Transformer Tap

FIG 5.23

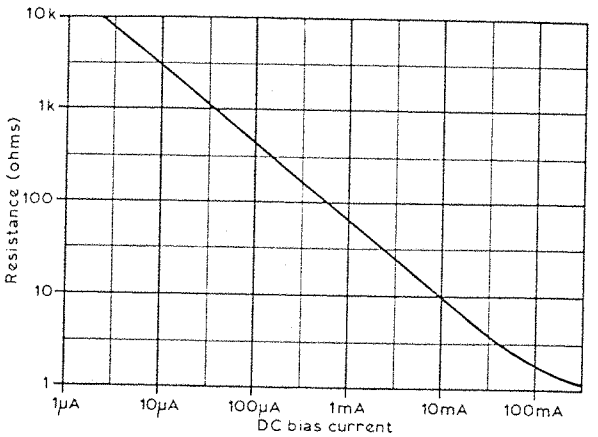




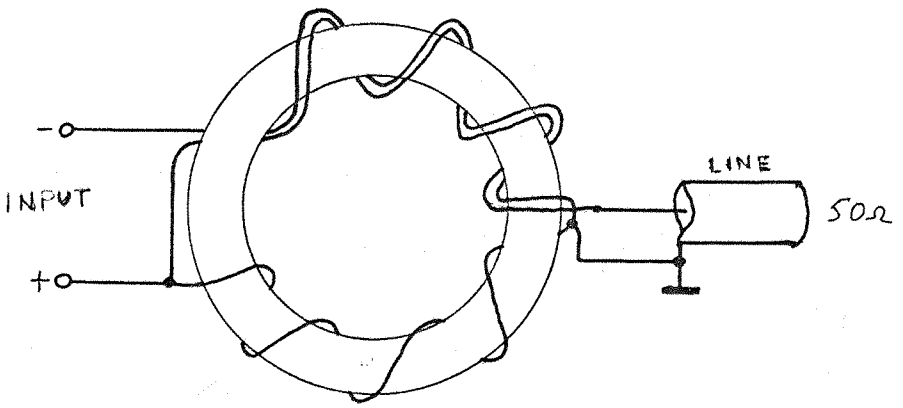
(b) CURRENT GENERATOR CCT.

Transmitter Coupling Network

FIG 5.24



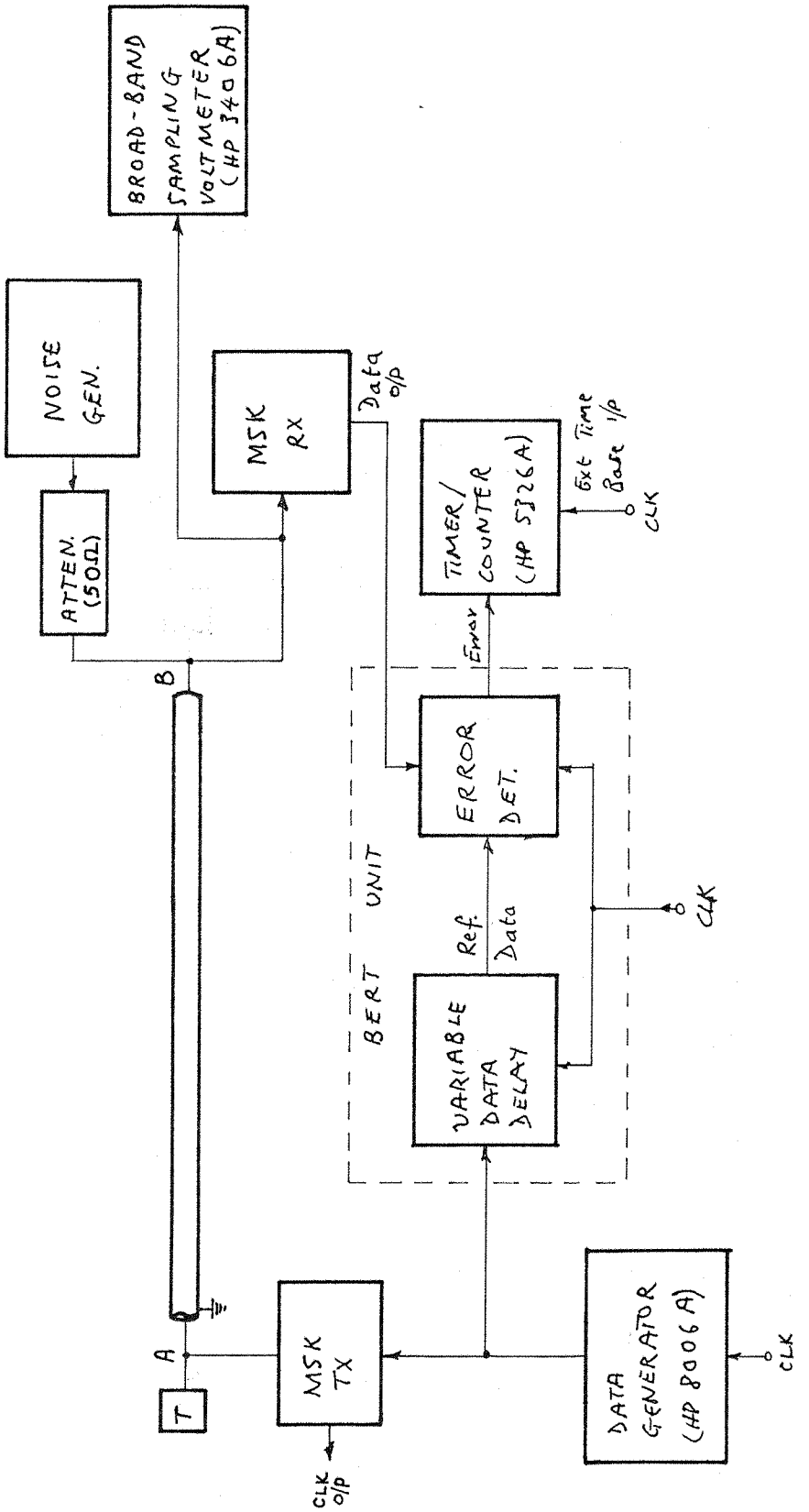
PIN Diode Characteristic (TYPE HP3081) FIG 5.25



COIL DATA

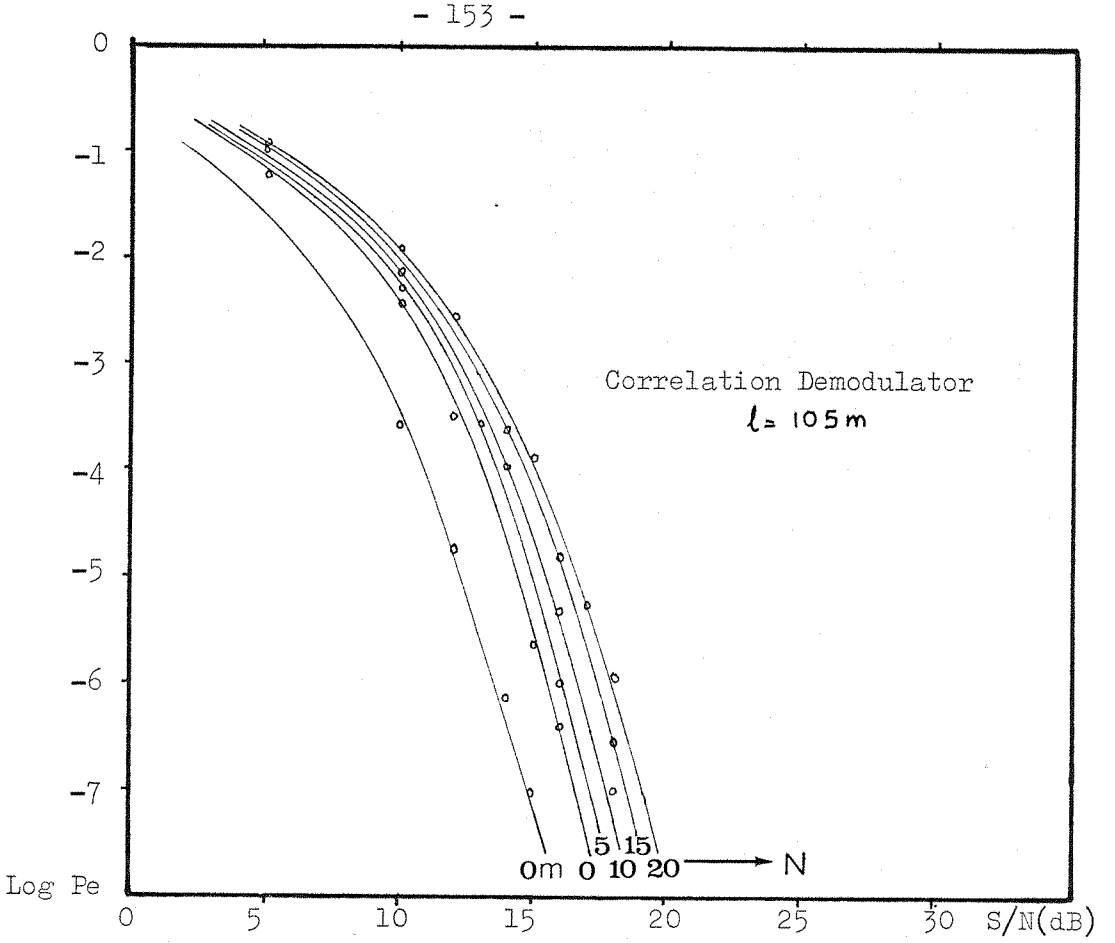
RING CORE TYPE: SEI MM622
0.5cm I.D.
1.0 cm O.D
0.3 cm Thick
3 Turns / 30 Gauge Wire

Transmitter Coupling Transformer FIG 5.26



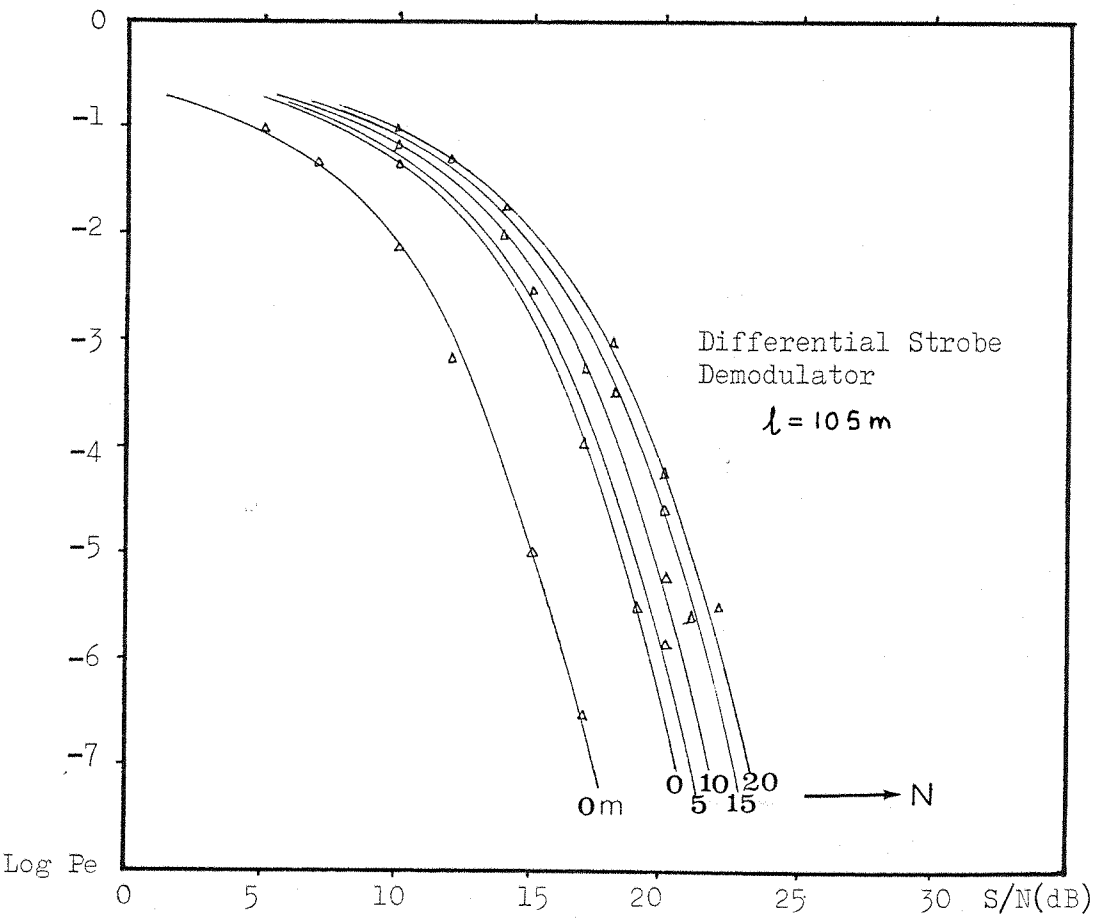
Bit Error Rate Measurement System

FIG 5.27



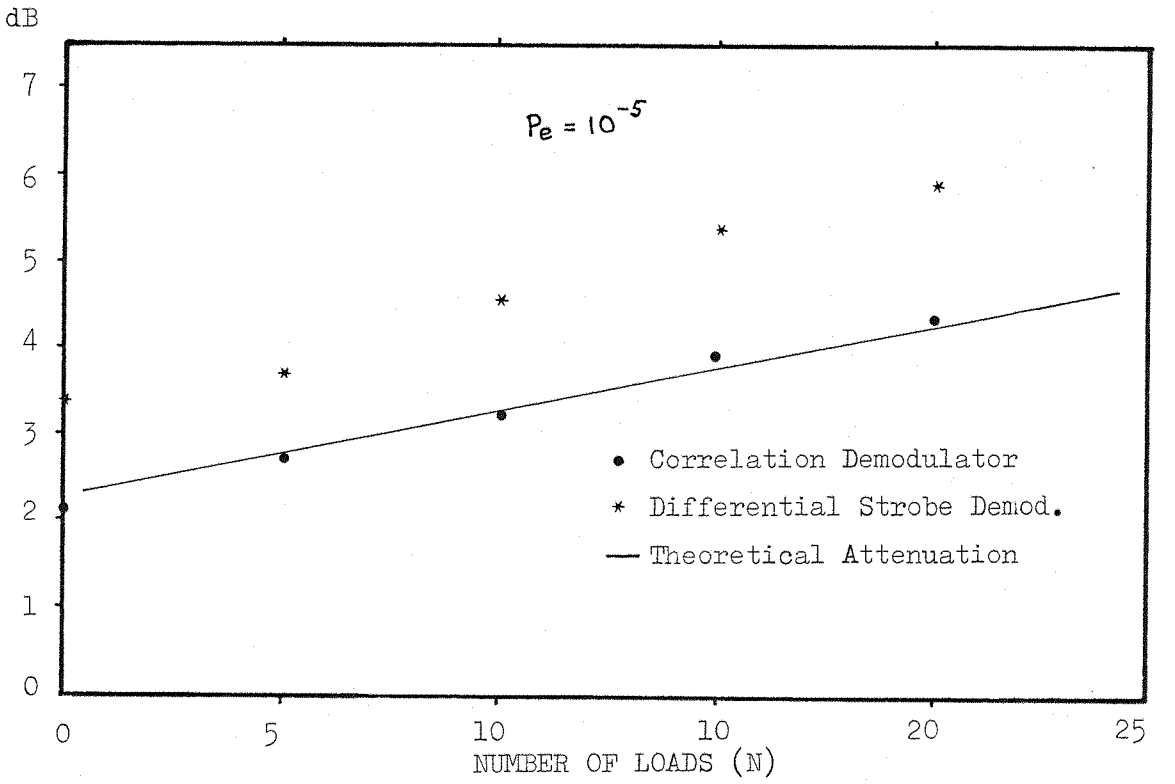
Error Rate Performance of Loaded Line

FIG 5.28



Error Rate Performance of Loaded Line

FIG 5.29



Increase in S/N Relative Om of Loaded Line

FIG 5.30

6. CONCLUSIONS

6.1 General

The primary achievement of this work has been a full assessment of the effects of loading when a large number of transformers are connected across a transmission line representing terminals in a passive highway configuration and also of the performance of an equivalent modulated carrier system. Further detailed properties and experimental performance data relating to the use of biphase and bifrequency baseband codes have been established. Particular attention has been given to evolving a discrete computer simulation model of the baseband system which provides a powerful tool for evaluation and prediction of highway performance. A simpler design approach to the modulated carrier system has been adopted which provides predictable performance.

6.2 Comparison of Baseband Codes

Comparison of the performances of the two techniques of decoding the biphase and bifrequency codes shows that the strobe detection decoder gives superior performance than the edge detection decoder.

It has been established that for strobe detection the PM code is less affected by transmission line distortion than the FM code ; this finding could be important where high speed and/or longline length situations are involved.

Also significant is the finding that a receiver filter bandwidth equal to the data bit-rate can be used satisfactorily for both codes.

Code violation testing has been shown to be a simple but powerful method of error detection. However, for PM the code error rate of two times the data error rate and the associated undetectable error rate of two times the corresponding value

for FM shows that if this error detection scheme is used, PM loses its advantage of lower error probability. Except for the case of undetectable error rate for FM coded signals the use of the message error measurement technique has facilitated the experimental confirmation of the various theoretical error probabilities associated with the two baseband codes.

From the above findings it is recommended that ;

(i) strobe detection method of decoding be used because of the added advantage of the use of synchronous clock extraction which gives improved performance.

(ii) Code violation testing should be used as an additional form of error detection.

(iii) FM code be used because of its polarity reversal advantage over PM. This is particularly useful for the passive highway configuration where the large number of terminal connections demand a high degree of ease of practical implementation. The superior error rate performance of PM coding is nullified if code violation error detection is employed.

6.3 Baseband Loading Studies

Transformer coupled loading of the passive highway has been found to cause more performance degradation than had been previously thought.

An important outcome of the investigations carried out in this area has been the precise identification and the means of predicting the individual effects of the three components of the transformer load, namely ; signal attenuation due to the core loss component ; signal distortion due to the primary self-inductance ; and multiple reflections, degradation of rise-times and additional delay caused by the stray capacitance.

The major contributions of the load components to the overall signal degradation has been found to be largely due to the core loss resistance and primary self-inductance. Both of these effects have been found to increase with the number of loads.

The effect of reflections on the signal distortion has been found to be generally negligible because it decreases as the number of loads is increased and also because it is limited by the skin effect distortion of the transmission line.

On the other hand, the signal risetime and delay have been found to increase significantly as the number of loads is increased. This result is important, considering the intended high speed applications where fast signal risetime and minimum delay between terminals is desired. It is thus necessary to keep the stray capacitance of the transformer load small in order to minimise the above effects.

An equation for predicting the mismatch loss of the transformer coupled loads has been formulated and verified experimentally. The resistive loss component of this equation has been shown to correspond to the cumulative resistive loss predicted in the CCL report (2). Using this equation, it is possible to estimate the required primary self inductance for a given total number of loads and core loss resistance.

To facilitate a more flexible and more convenient method of investigating the passive highway loading problem two computer simulation models were developed. The model using Laplace transform techniques represents the more conventional approach to the problem. The less well known discrete transmission line method used is a fairly recent and very significant advance in the general solution of electrical network problems. An important feature of this technique is that an exact solution of all aspects of the signal waveform at any terminal along the highway under any predetermined loading condition is possible without increasing the complexity of the solution, as would be necessary in the case of the Laplace transform technique. As noted by Johns in his recent

paper (31), there is a need to consider discrete model solutions as viable alternatives to the well established continuous model solution of physical phenomena. The closeness of the signal waveforms obtained to the physical situation confirm this assertion. It is worth noting that the additional capabilities of the discrete model developed include the possibility of open circuit and short circuit fault analysis of the highway. In the analysis presented, skin-effect distortion was represented as a fixed resistance per unit length appropriate to the operating frequency. The possibility of completely describing this effect in the overall discrete model is an area worth investigating.

6.4 Modulated Carrier Studies

The MSK modulation technique used has been shown to be a suitable method for the proposed high speed serial highway applications. The use of sub-optimum demodulation techniques, intended to trade-off simplicity of implementation with performance degradation has been found to be successful in the case of the correlation demodulator. On the other hand, the differential strobe demodulator has been found to be very susceptible to the effects of jitter and its use is not recommended.

An important outcome of the loading tests has been the predictable behaviour of the results obtained ; i.e. the S/N degradation due to the connection of the terminal loads is accounted for by the insertion loss of the loads. This shows that by using the narrow band signalling, the transmission line distortion effects on the signal were minimal, thus confirming one of the main predicted advantages of the modulated carrier system over the baseband system.

The tapped transformer network used has proved to be a simple, effective and predictable method of coupling the line to the receivers. Equations predicting its performance have been found to agree with the experimental results. By using the broadband approach to the design of the taps, FDM techniques as well as the broadcast mode of operation of the serial highway is made possible. The significance

of these results is that it shows that despite the apparent simplicity of the coupling device, its performance matches the more sophisticated commercial couplers in use.

The identified advantage of the modulated carrier system is that signal distortion and intersymbol interference effects suffered by the baseband system are significantly reduced. Also noted is the more predictable performance compared with the baseband system. Potentially, the modulated carrier system can accommodate more terminals than the baseband system ; in particular, the experimental system developed can tolerate up to 15 dB total transmission loss which represents up to a 100 terminals on a transmission line length of 200m for a loss per terminal of 0.1 dB.

An increase in the terminal loads for the modulated carrier system is possible by simply using a higher tap ratio ; this compares with the more stringent requirements of the baseband system which demands that all of the core characteristics of the transformers used be uniform if predictable performance is to be realised. The baseband experimental system using the transformer loads having the LCR values of 4.7 mH, 20 pF and 5.6 KΩ typically gives a loss per terminal of about 0.1 dB ; this means that up to a 100 terminals can equally be accommodated on a 200m length of cable, the total loss being about 15 dB.

The above comparative evaluation of the baseband and the modulated carrier systems show that, in terms of the proposed highway, the maximum of 64 terminals over a 300m length of cable is feasible in both cases. However, cost being an important factor because of the large number of terminal units, the baseband system is recommended because of its relative simplicity of implementation. In making this recommendation, it is also strongly suggested that the characteristics of each transformer be experimentally tested to ensure that it is within the designed specifications.

Whilst appreciating that because of the technical and economic advances in fibre optic cable technology in recent years the work

described in this report may not be of much relevance in the future, nevertheless the general contribution made is of significance to current highway system development.

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APPENDIX A

Error Probabilities in FM and PM Codes

Analysis of error probabilities considered for both PM and FM codes in this report is given below.

A.1 Bit error probability in the presence of Gaussian noise

Appleby (3) has shown that the $\frac{1}{2}$ bit element error probability (P_{es}) associates with PM and FM coded data is given by

$$P_{es} = \tfrac{1}{2}\left[1 - \text{erf}\left(\sqrt{\tfrac{1}{2}\, S/N}\right)\right] \qquad \text{(A1)}$$

where the signal to noise ratio is given by

$$S/N = \frac{V^2}{\sigma^2}$$

V = peak voltage of input square wave

σ = rms voltage of Gaussian noise

This relationship assumes zero level threshold detection and an ideal synchronous decoder.

A.1.1 FM Coded Signals

For FM data bit error arises when either, but not both $\frac{1}{2}$ bit samples are in error. If P_e is this error probability then,

$$P_e = 2P_{es}(1 - P_{es}) \qquad \text{(A2)}$$

$$= 2P_{es} - 2P_{es}^2$$

$$\simeq 2P_{es} \text{ for small } P_e$$

$$P_e = 1 - \text{erf}\left(\sqrt{\tfrac{1}{2}\, S/N}\right)$$

A.1.2 PM Coded Signals

For PM a data bit error occurs when only one $\frac{1}{2}$ bit element is in error ; in this case the data bit error probability,

$$P_e = P_{es} \qquad \text{(A3)}$$

$$P_e = \tfrac{1}{2}\left[1 - \text{erf}\ \left(\sqrt{\tfrac{1}{2}\ S/N}\right)\right]$$

A.2 Code Error Probability

Code errors are detected by checking for the presence of regular transitions (same for both FM and PM coding). The probability of code error outputs is then the probability of just one-half bit element being in error out of a pair of elements. See Figure A1, i.e.

$$P_{ec} = 2P_{es}\ (1 - P_{es})$$

For PM, referring to Equation (A3) ;

$$P_{ec} = 2P_e(1 - P_e)$$

$$P_{ec} \simeq 2P_e \qquad \text{(A4)}$$

For FM, referring to Equation (A2)

$$P_{ec} = P_e \qquad \text{(A5)}$$

A.3 Undetectable error probability

A.3.1 PM coded signals

For PM an undetectable data bit error is produced if both $\frac{1}{2}$ bit

elements are in error, i.e.

$$P_{eu} = P_{es}^{2} \tag{A6}$$

where P_{es} = probability of error in each $\frac{1}{2}$ bit element (see Figure A2).

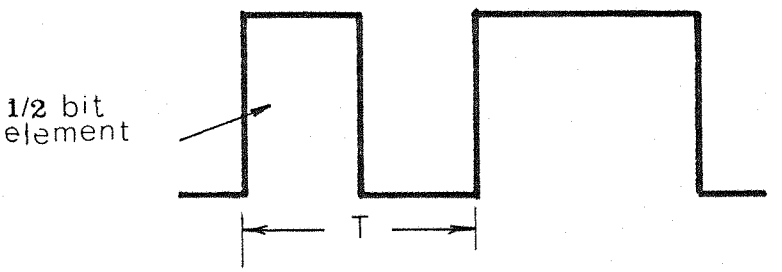


Figure A2.

Also for PM the total data bit error probability is given by

$$P_e = P_{es} \tag{A7}$$

hence we can write

$$P_{eu} = P_e^{2} \tag{A8}$$

A3.2 FM Coded Signals

In FM coding the undetectable error condition involves a pair of consecutive data bits in which the two $\frac{1}{2}$ bit elements either side of the bit boundary are in error and the other two elements are correct. Since such condition would result in two data bit errors, P_{eu} is given by

$$P_{eu} = 2P_{es}^{2}(1 - P_{es})^{2} \tag{A9}$$

For FM the total data bit error probability is given by

$$P_e = 2P_{es}(1 - P_{es}) \tag{A10}$$

thus from Equations A9 and A10 the undetectable error probability becomes

$$P_{eu} = 2\left(\frac{P_e}{2}\right)^2 = \tfrac{1}{2} P_e^{\,2} \tag{A11}$$

A.4 Message error probability

Let m = total number of bits in message,

P_e = probability of one bit in error

and P_m = probability of error in message

Probability of all bits being correct in message

$$= (1 - P_e)^m$$

∴ Probability of error in message is

$$P_m = 1 - (1 - P_e)^m \tag{A12}$$

Using the binomial expansion,

$$(1 - P_e)^m = 1 - mP_e + \frac{m(m-1)}{2} P_e^{\,2} + \ldots$$

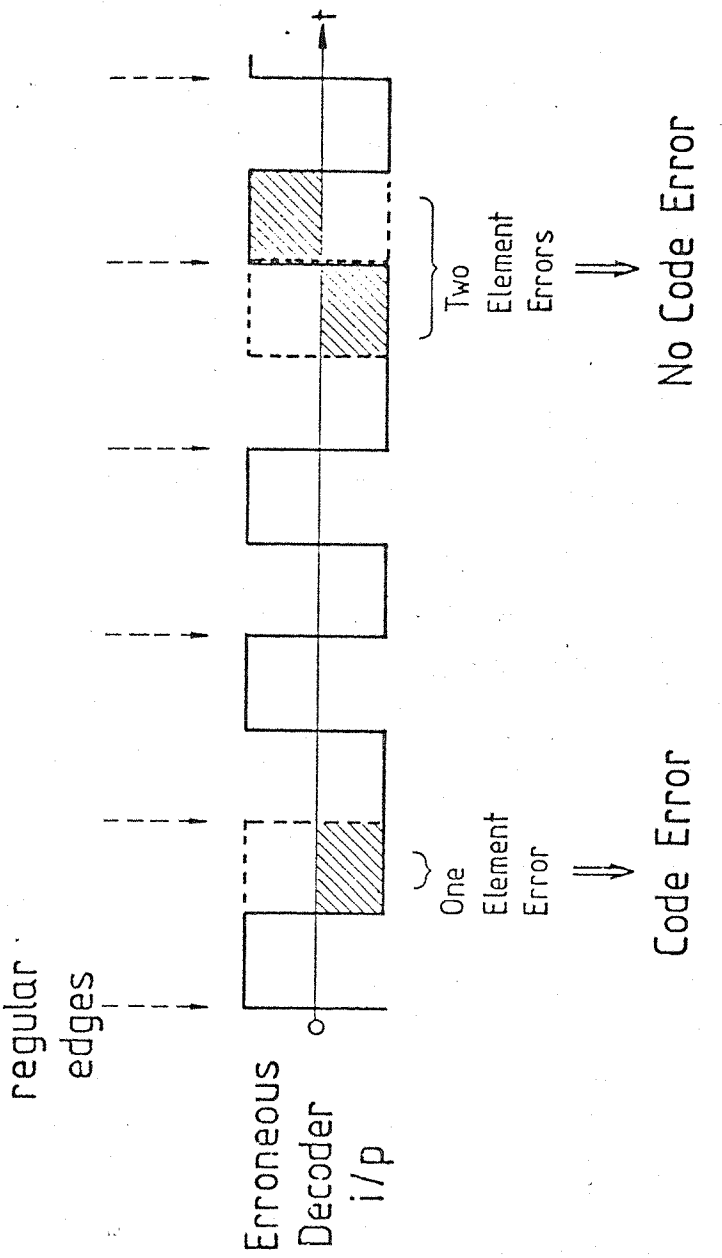
$$\simeq 1 - mP_e \tag{A13}$$

(neglecting higher order terms for small P_e)

Substituting A13 in A12, we get

$$P_m \simeq m P_e \tag{A14}$$

Equation A14 gives an approximate relationship between message error and the corresponding message length. This being a linear relationship, the slope of the graph of P_m against n gives the approximate bit error probability P_e.



Code Errors in FM and PM Codes

FIG A1

APPENDIX B

Receiver Circuits

B.1 Strobe detection decoder

After the first few tests the timing of the first strobe point in the FM decoder was changed from immediately after the regular transition to 125% of a bit period by connecting the clock input to flip-flop U3/1 to the CK3 output of the clock extraction circuits. The original circuit is shown in Figure B1.

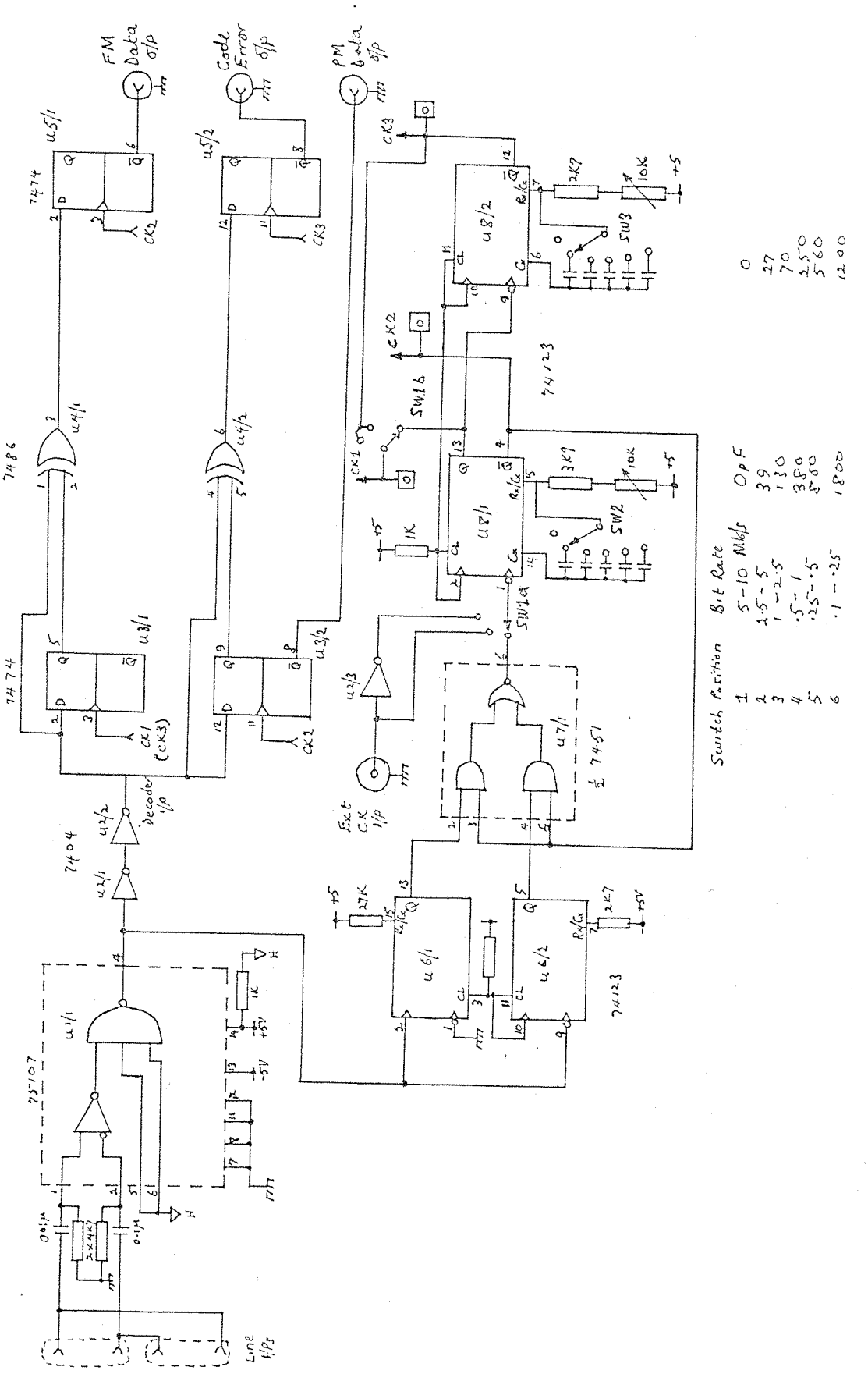
B.2 Edge detection decoder

The circuit diagram is shown in Figure B2. The line inputs can be either capacitive or transformer coupled into a high impedance differential line receiver UO/1. The monostables U1/1 and U1/2 detect the rising and falling edges of the coded signal from the line receiver and produce a 50 ns pulse for each edge detected. The monostables U3/1, U3/2 and U7/1 are adjusted to give pulse widths of 3/4, 1/4 and 1/2 bit periods respectively.

For PM coding, the decoded data is determined by the direction of the regular mid-bit transitions in the input signal. A rising edge corresponds to binary 'one' and a falling edge a binary 'zero'. The 50 ns pulse resulting from a regular edge is gated through U2/3 or U2/4 and either clears or presets flip-flop U5/1, depending on whether it was a falling or a rising edge respectively. At the same time, the 50 ns pulse which is gated through U2/1 and U2/2 triggers the monostables U3/2 and U3/1. The low state of the $\overline{Q}$ output of U3/1 disables the gates U2/2, U2/3 and U2/4 for the next 3/4 bit period thus preventing intermediate edge pulses changing the state of U5/1 or triggering U3/2. After 1/4 bit period, the rising edge of the $\overline{Q}$ output of U3/2 clocks in the data at the $\overline{Q}$ output of U5/1 into flip-flop U5/2, the $\overline{Q}$ output of which gives the decoded PM data.

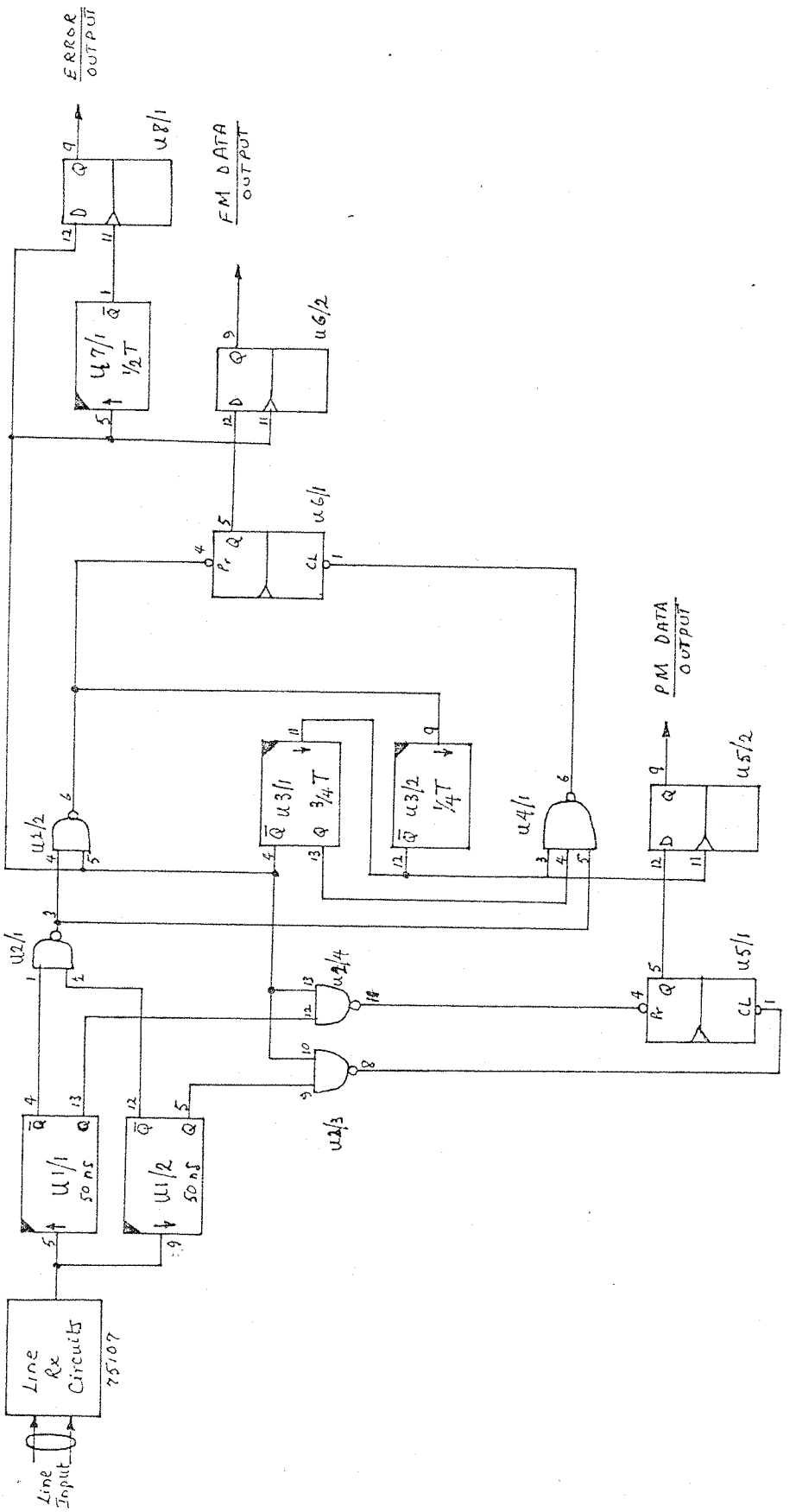
For an FM coded signal regular transitions occur at the data bit boundaries and the presence or absence of a mid-bit transition indicates a data zero or one respectively. Regular edge pulses pass through gate U2/2, trigger the U3 monostables and preset flip-flop U6/1 at the beginning of each bit period. Gate U2/2 is disabled, as explained above, up to 3/4 bit period. Gate U4/1 is enabled during the interval from 1/4 to 3/4 bit period, so that if a mid-bit edge occurs the corresponding pulse will clear the flip-flop U6/1. Thus the state of the $\overline{Q}$ output of U6/1 at the 3/4 bit position represents the decoded data and is strobed into flip-flop U6/2 by the rising edge of the Q output of U3/1.

A code error condition is detected for either FM or PM coded signals if a regular transition does not occur in the interval 3/4 to 11/4 bit period after the previous regular transition. This is affected by strobing the $\overline{Q}$ output of monostable U3/1 into flip-flop U8/1 with the trailing edge of the output of monostable U7/1 at 1 1/4 bit period.



EM / PM Rx STROBE DETECTION

FIG B1



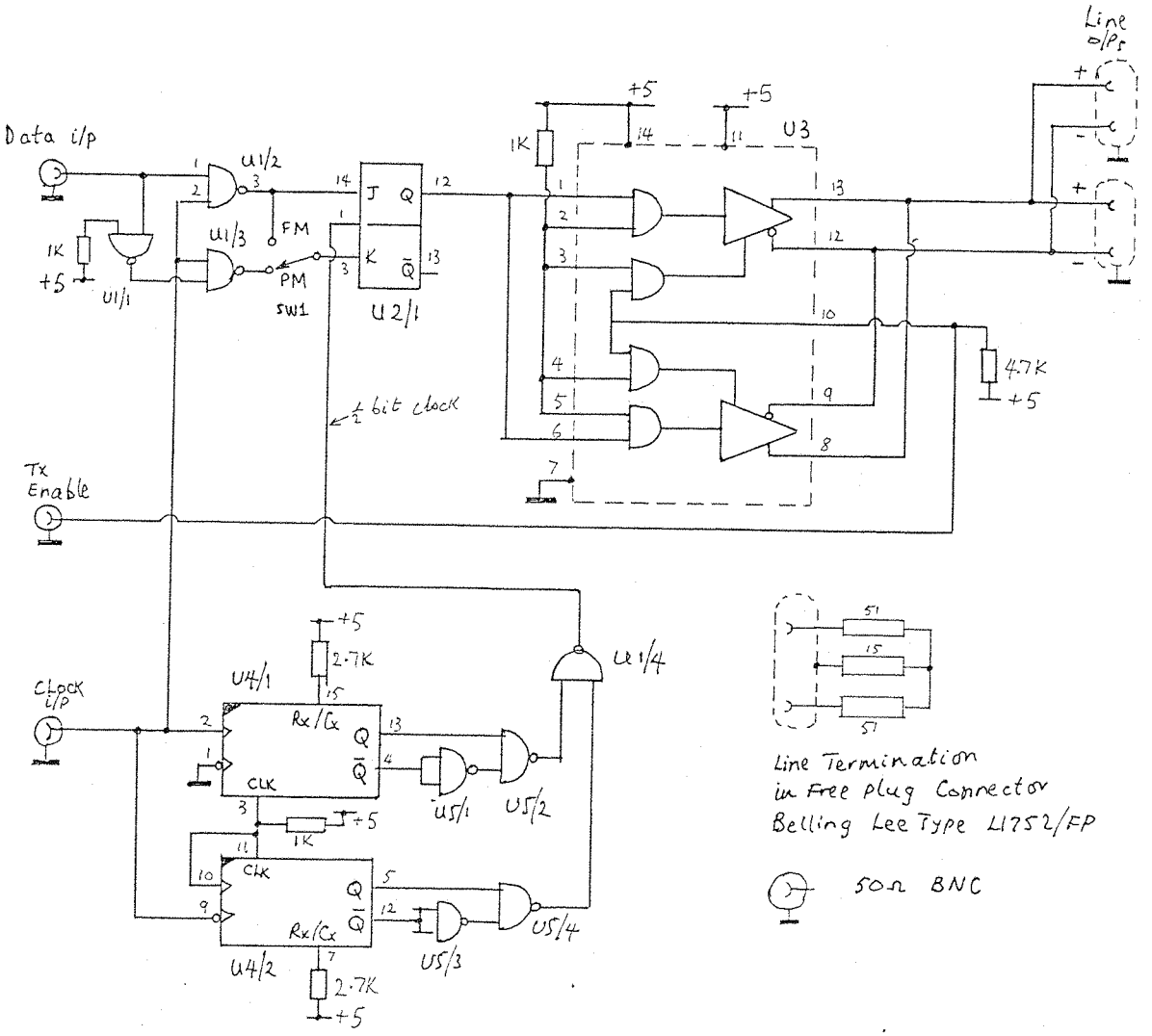
EDGE DETECTION FM/PM DECODER

FIG B2

APPENDIX C
FM/PM Transmitter Circuit

The circuit is shown in figure C1. Coding of the data input is carried out by J-K flip flop U2/1 and three NAND gates U1/1-3, FM or PM coding being selected by means of switch SW1. The coded signal is fed to both line drivers in U3 whose outputs are connected in parallel to the line output sockets, thus providing twice the output current (nominally 24 mA "pull-pull"). The common enable input to U3 has been brought out to a front panel socket so that if required the transmitter output can be completely disabled.

The clock input to the coder circuits consists of very short pulses at twice the system bit rate. The clock input (from BERT) is a square wave at the bit rate the positive going edges of which trigger monostable U4/1 and the negative going edges trigger monostable U4/2. Each monostable is connected to produce its minimum pulse width of about 40 ns. This width is further reduced by inverting the $\overline{Q}$ output and effectively ANDing it with the Q output. Since the $\overline{Q}$ output is delayed by 10 ns relative to Q and then further delayed by 10 ns in the inverter the overlap is about 20 ns. The shortened (and inverted) outputs are then effectively ORed together in NAND gate U1/4. The star connected termination network is contained within the shell of a 2 pole free plug connector, as shown in figure C1. A similar termination was used at the receiver.



Note: Supply Decoupling

10μF on each rail

0.01 μF across each IC.

ICs

U1 - 7400
U2 - 7473
U3 - 75110
U4 - 74123
U5 - 7400

PM/FM Transmitter

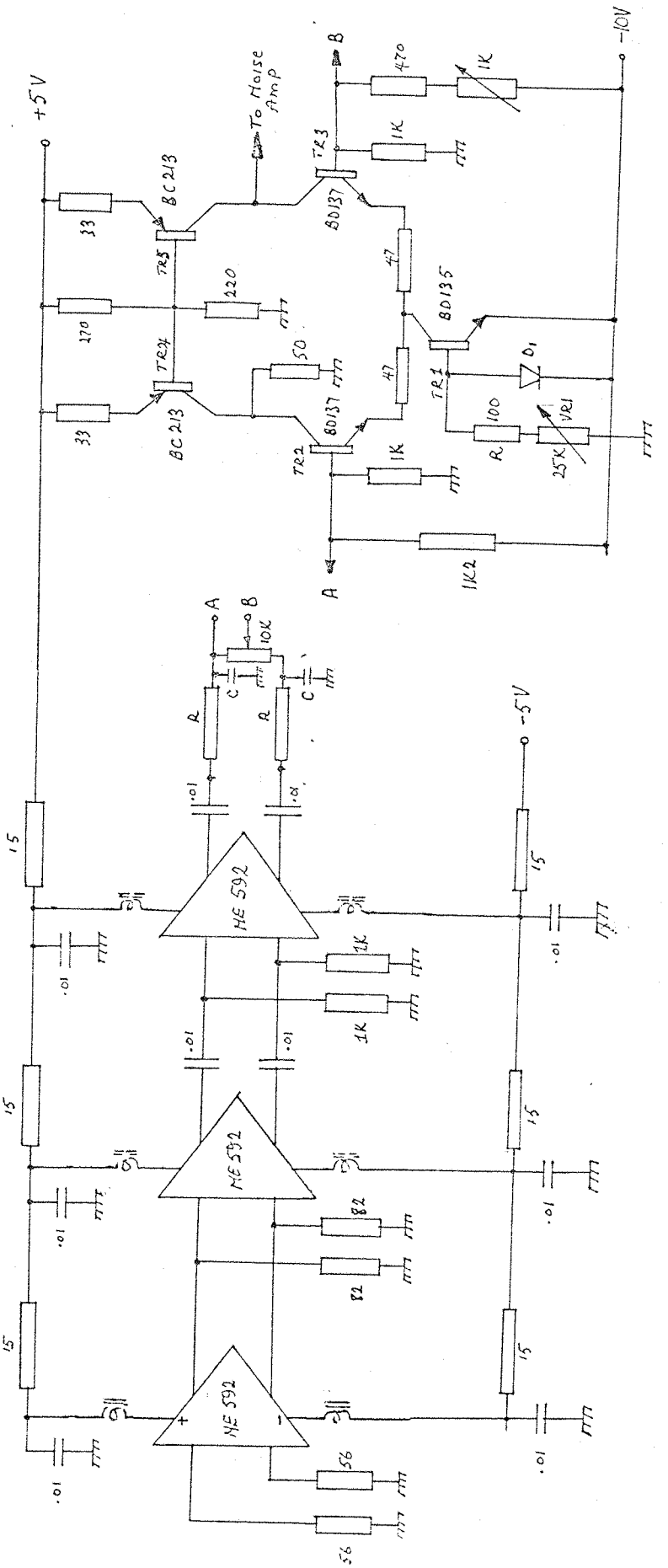
FIG C1

APPENDIX D

Noise generator and amplifier circuits

The noise generator circuit is shown in Figure D1. The output provides wideband noise with a bandwidth of up to 10 MHz at a variable level up to 1 volt r.m.s. into a 50Ωload. The noise is generated in the first stage of a 3-stage high gain video amplifier, each stage being a wideband differential IC amplifier (Signetics NE 592). Noise bandwidth variation is obtained by changing the component values of the RC network at the output of the third-stage. The output stage is essentially a long-tailed pair differential amplifier comprising TR2 and TR3 with TR1 acting as the tail current source. Transistors TR4 and TR5 act as d.c. current sources and provide most of the d.c. bias current for the long-tailed pair.

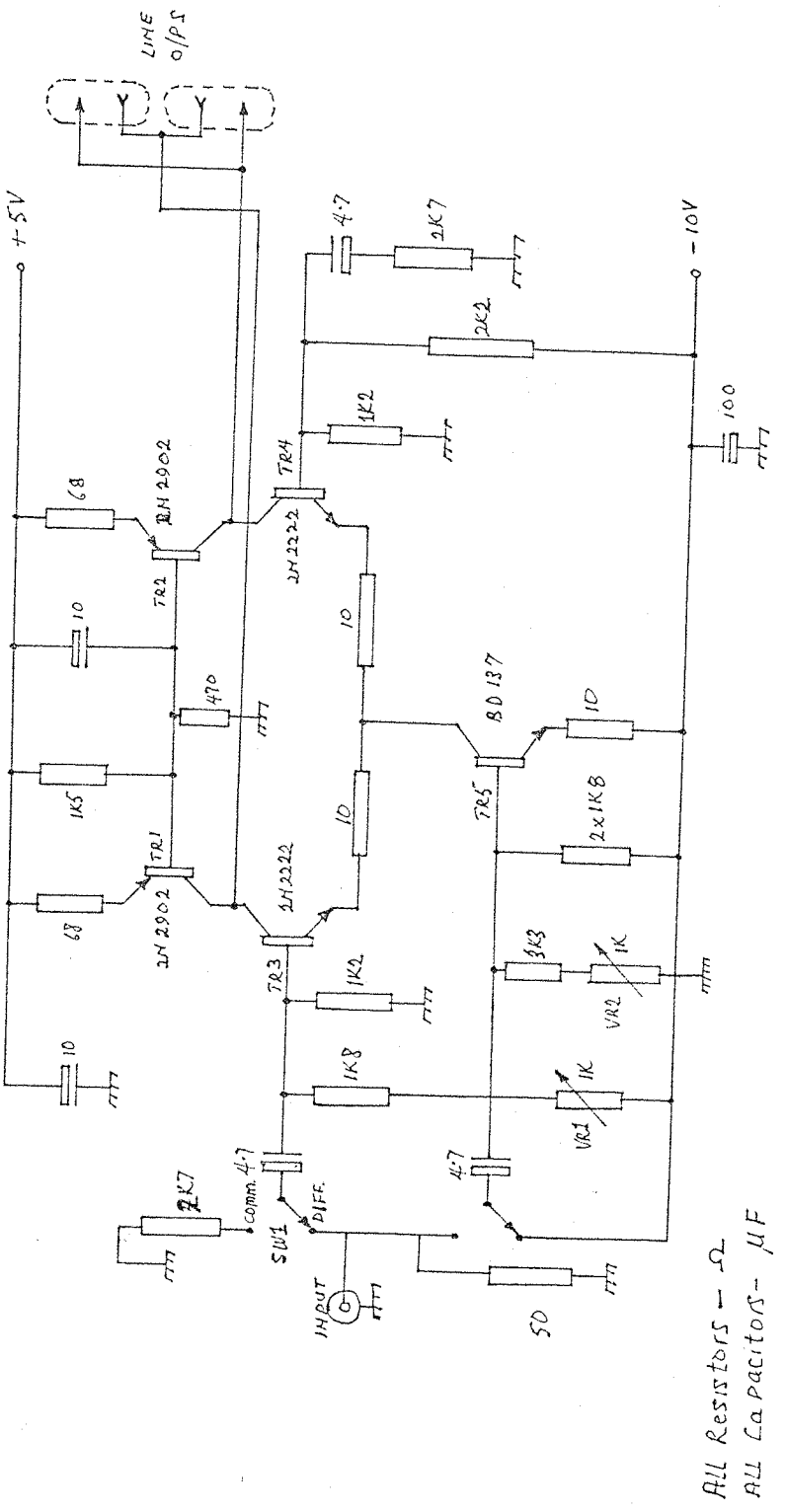
Figure D2 shows the final circuit of the noise amplifier.



NOISE GENERATOR

FIG D1

ALL Resistors in Ω
ALL Capacitors in μF



NOISE AMPLIFIER

FIG D2

APPENDIX E

Bit Error Rate Test (B. E. R. T.) Circuit

Figure E1 shows a complete circuit diagram of the BERT unit. It comprises three basic sub-circuits namely ; Clock Generator, Variable Data Delay, and Error Detector Circuits.

E.1 Clock Generator

The basic signal generator is formed by U8/1 and the RC feedback network. Switch SW7/a selects the capacitor values corresponding to the desired range of clock frequencies, and VR3 provides fine clock frequency tuning. The output of U8/1 is gated through U8/2, which speeds up the signal edges, into the divide-by-two toggle U14/2 to obtain the clock signal.

E.2 Variable Data Delay

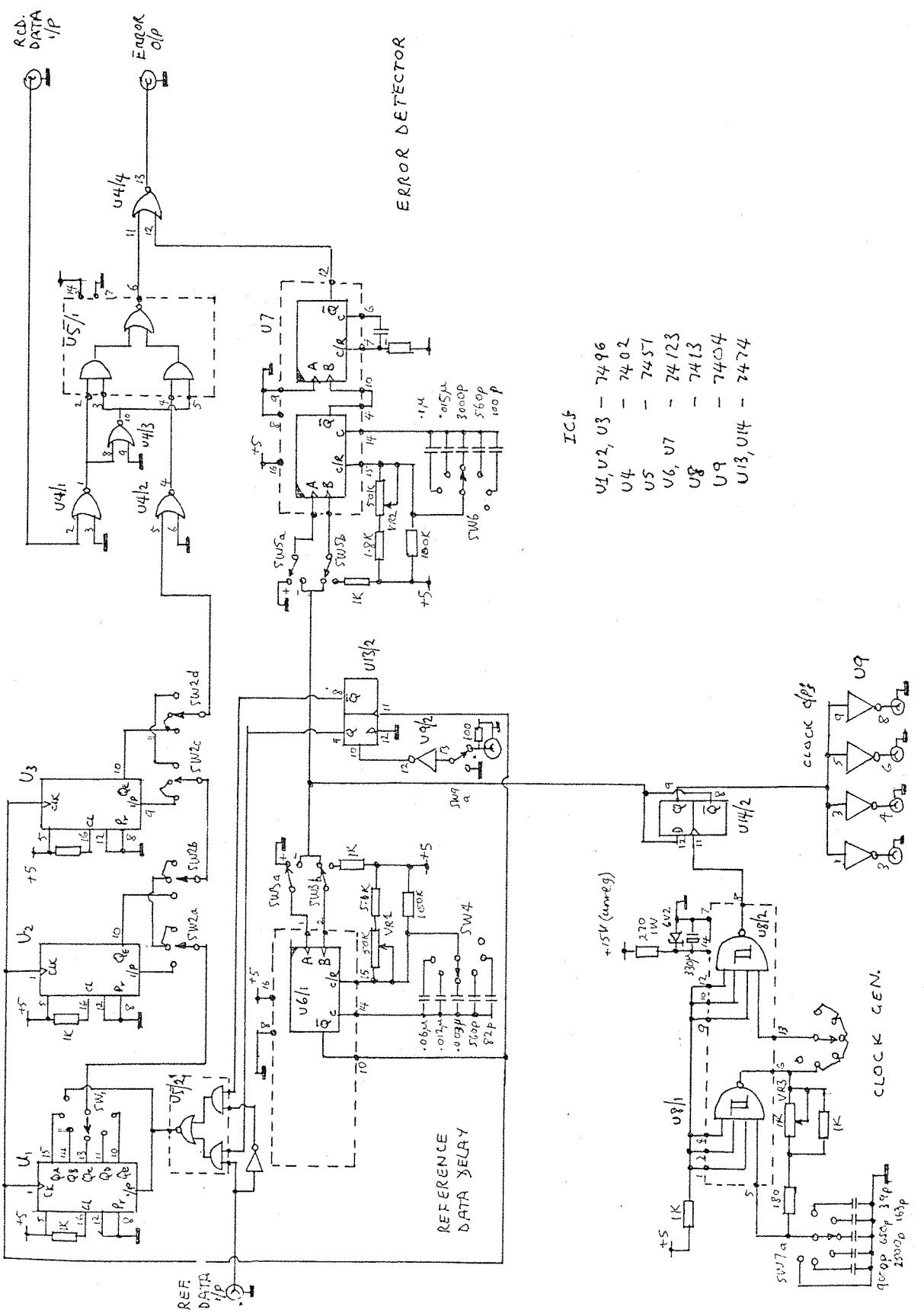
The clock output from U14/2 is fed through SW3 which selects either edge of the clock signal to trigger the monostable U6/1. The output pulse width range is varied using SW4, and VR1 provide fine adjustments to the pulse width which is less than the bit period T.

The incoming reference data is fed to the input of U1 through U9/1, and U5/2. Using SW9/a and the circuit formed by U9/2 and U13/2, the data is inverted or passed directly to U1. The data is clocked by the signal output of U6/1 into the cascaded shift register arrangement of U1, U2, and U3 to give a delay of one bit to a maximum of 12 bits or transferred without any delay, depending on the position of the selector switches SW1 and SW2. Fine setting of the data delay is obtained by varying VR1.

E.3 Error Detector

The delayed reference data at the output of SW2/c is compared with the received data in the gating arrangement formed by U4/1, U4/2,

U4/3 and U5/1. The output of U5/1 is high if the reference data and the received data are at the same logic state and low if otherwise. This output state of U5/1 is detected by U4/4 with strobe pulses, which is set to the mid-bit point, and derived from the clock output of U14/2 by the monostable U7. A high output from U4/4 correspond to a detected data error. The width of the strobe pulse ($<T/2$) is varied with SW6 and VR2, and SW5 selects either the positive or the negative edge of the clock.



Bit Error Rate Test (BERT) Circuit

FIG E1

APPENDIX F

Signal-to-noise ratio measurement

A block diagram of the measurement system is shown in Figure F1. The definition of S/N ratio used is given as

$$S/N = \left[\frac{\text{Signal voltage at transmitter end}}{\text{Noise voltage at receiver end}}\right]^2$$

This definition provides a definite basis for comparison of line performance since the transmitter end voltage is constant and easily measured.

From the above definition, the expression for the S/N is derived. Referring to Figure F1.

let V_T = r.m.s. sending end signal voltage

σ_o = r.m.s. noise output from generator

G_v = voltage gain of noise amplifier

σ_n = r.m.s. noise voltage injected at receiver end

A = attenuation in dB of attenuator

From the definition of S/N ratio above,

$$S/N = \left(\frac{V_T}{\sigma_n}\right)^2$$

$$S/N_{dB} = 20 \log V_T - 20 \log \sigma_n \qquad (F1)$$

Attenuation is given by

$$A = 20 \log \sigma_o - 20 \log \left(\frac{\sigma_n}{G_v}\right)$$

from which

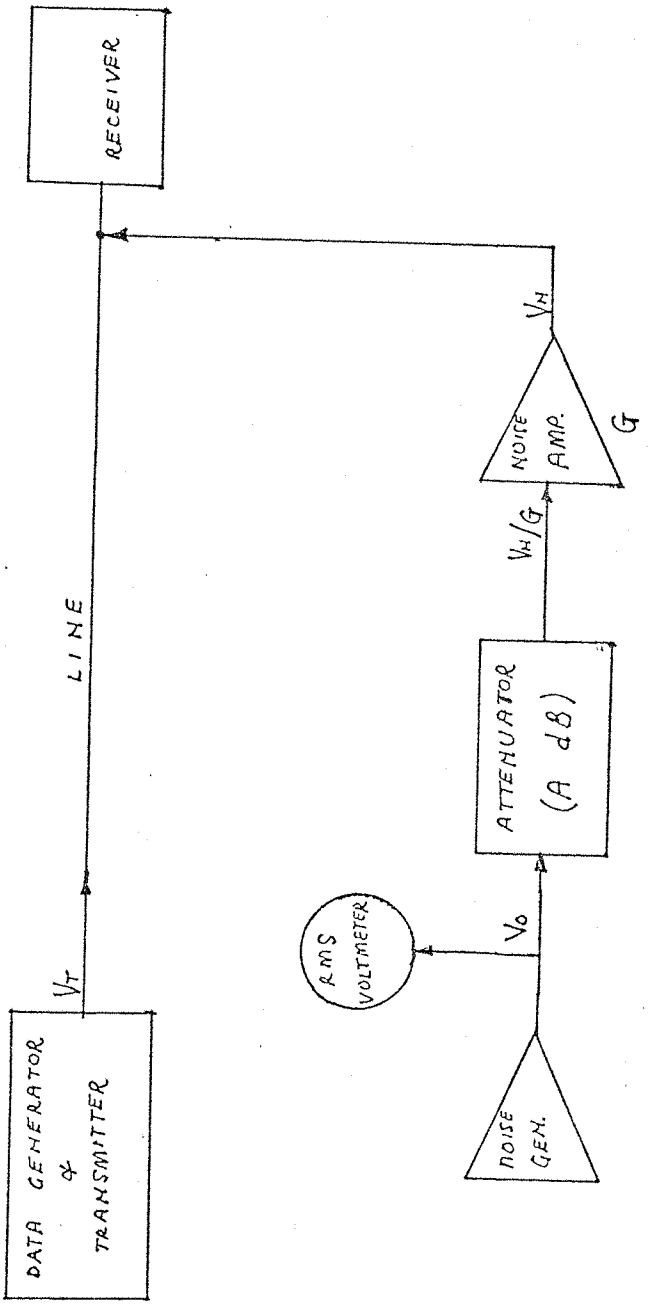
$$20 \log \sigma_n = 20 \log (G_v . \sigma_o) - A$$

Substituting into (F1) gives

$$(S/N)_{dB} = 20 \log V_T - 20 \log (G_v . \sigma_o) + A$$

$$= A, \text{ if } V_T = G_v . \sigma_o$$

V_T was measured as the peak value of the differential voltage waveform since the r. m. s. and peak magnitudes of a rectangular polar waveform are equal.



SIGNAL TO NOISE RATIO MEASUREMENT

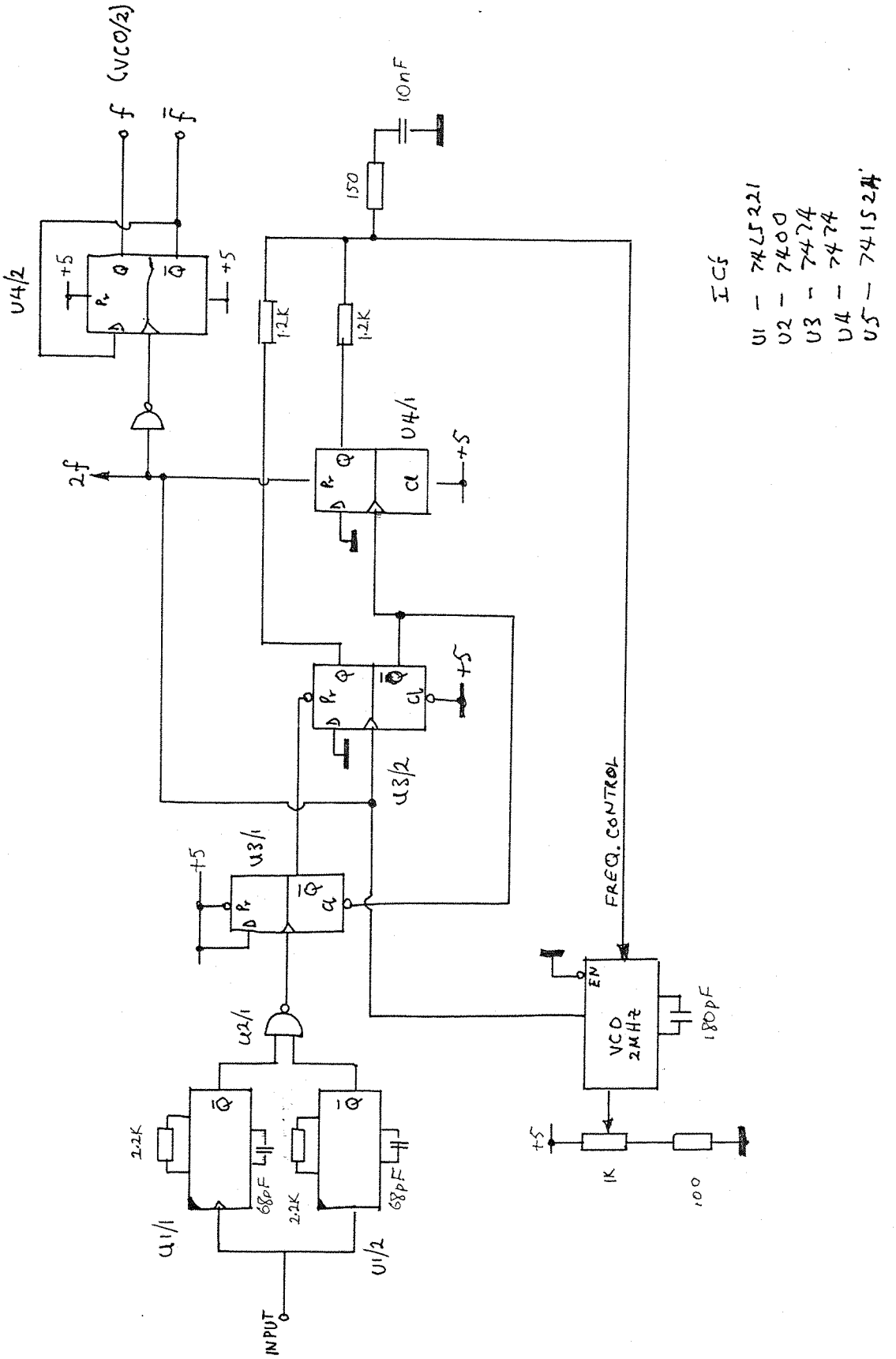
FIG F1

APPENDIX G

Phase Lock Loop (PLL) Clock Extraction Circuit

Figure G1 shows the PLL clock extraction circuit which was developed by P. I. Poskett (32) for the measurements on the baseband system. The circuit is basically an analogue PLL operating at twice the data bit rate of 1 MHz.

The transitional edges of the input coded data stream are detected by the two monostables U1/1 and U1/2 to produce pulses of bit rate 2 MHz at the output of U2/1. The arrangement of the 3 D-type bistables U3/1, U3/2 and U4/1 provide the phase comparator network. The result is 2 waveforms at the outputs of U3/2 and U4/1, which are summed to obtain the control voltage. The output of U3/2 is set high by the +ve edge of the pulses at the output of U3/1, and set low by the +ve edge of the V. C. O. and hence represents the phase difference between the two signals. The absence of mid-bit transitions in the coded PM/FM data is compensated for by the signal output of U4/1. It is set low by the -ve edge of the output of U3/2 and set high by the -ve edge of the V. C. O. The outputs of U3/2 and U4/1 are summed and filtered to provide the V. C. O. control voltage. The V. C. O. output at a frequency of 2 MHz is divided by 2 to give the extracted clock signal at the output of U4/2.



PLL Clock Extraction circuit

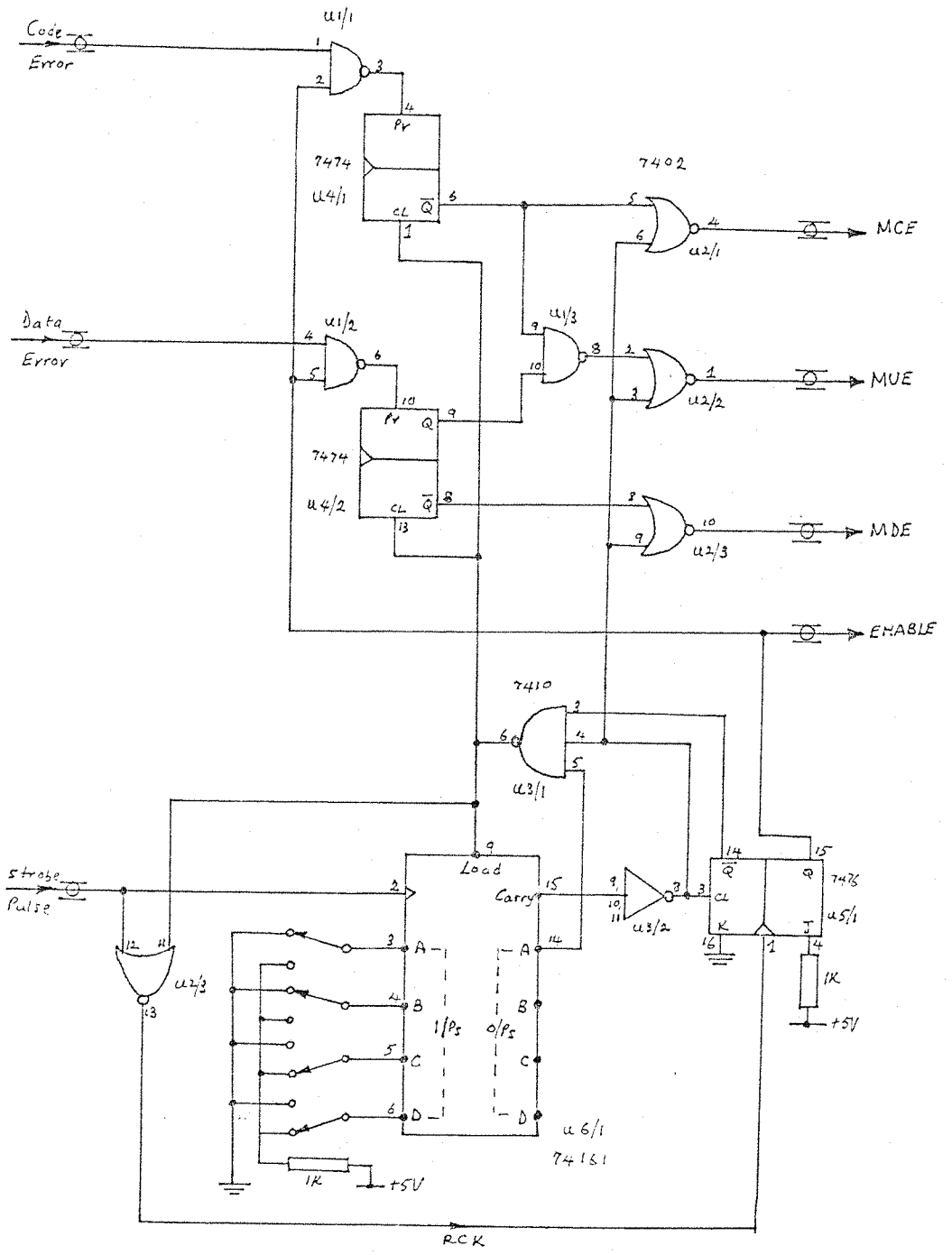
FIG G1

APPENDIX H

Message error rate test (M. E. R. T.) circuit

The circuit diagram is shown in Figure H1. The required message length is given by the ones complement of the selected binary input to the counter U6/1.

A low output at gate U3/1 clears flip-flops U4/1 and U4/2 and enables the load input of counter U6/1. The rising edge of the first strobe pulse to the counter, following the low output at gate U3/1, presets U6/1 output to the selected binary input data. At the same time, the falling edge of the pulse RCK which is gated through U2/3 presets the flip-flop U5/1. The low state of the $\overline{Q}$ output of U5/1 disables the gate U3/1 and the corresponding high state of the Q output enables the input gate U1/1 and U1/2. With the carry output of counter U6/1, the output gates U2/1, U2/2 and U2/3 are disabled through gate U3/2. The rising edge of subsequent strobe pulses advance the counter U6/1 through the selected message length. Within the message period, the presence of any code or data errors is transmitted through gates U1/1 and U1/2 which preset flip-flops U4/1 and U4/2 respectively ; otherwise the flip-flops remain in the reset state. A message undetectable error, which occurs when one or more data errors occur but no code error is detected by gate U1/3 which gives a low output. A carry output is generated by the counter U6/1 at the end of message, corresponding to all ones of its output. This carry pulse is gated through U3/2 which clears the flip-flop U5/1 and enables the output gates U2/2 and U2/3. At the same time the low state of the Q output of U5/1 disables the input gates U1/1 and U1/2. A high output is produced at the output of gates U2/1, U2/2 and U2/3 if code, data and undetectable errors occurred. The rising edge of the third strobe pulse after the carry output presets the counter outputs to the selected binary input data, restarting the cycle over again.



MESSAGE ERROR RATE TEST (M.E.R.T.) CIRCUIT

FIG H1

APPENDIX I

Cumulative Attenuation due to Mismatches

Consider a single load resistor R_L connected across an ideal transmission line of characteristic impedance R_O correctly terminated at both ends as shown in Figure I 1(a). The section of line to the right acts as an additional load resistance R_O across R_L as shown in Figure I 1(b). Thus the transmitted pulse amplitude is given by

$$V_t = V_i (1 + r_c) \tag{I1}$$

where r_c is the reflection coefficient given by

$$r_c = \frac{R_T - R_O}{R_T + R_O} \tag{I2}$$

where R_T is the parallel combination of R_L and R_O. Substituting for r_c in I 1

$$V_t = V_i \left(1 + \frac{R_T - R_O}{R_T + R_O}\right)$$

$$= V_i \left(\frac{2R_T}{R_T + R_O}\right) \tag{I3}$$

Defining the transmission coefficient as

$$T_o = \frac{V_t}{V_i}$$

and substituting

$$R_T = \frac{R_L R_O}{R_L + R_O}$$

gives

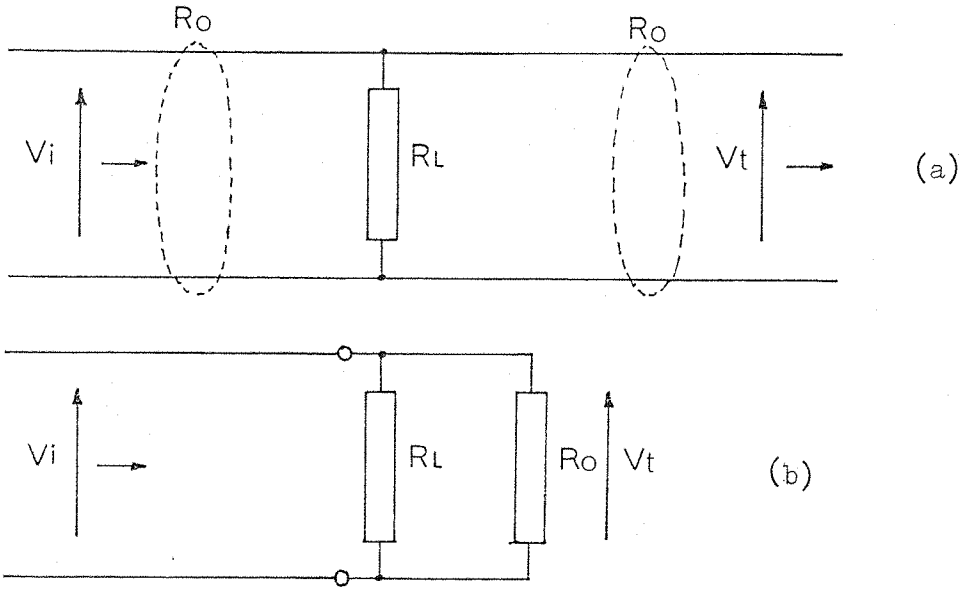
$$T_o = \frac{2R_L}{2R_L + R_O} = \frac{1}{1 + R_O/2R_L} \tag{I4}$$

Now consider a line with N identical loads R_L connected as shown in Figure I2. Neglecting the interference of reflected pulses the cumulative attenuation is given by

$$\frac{V_i}{V_t} = \left(\frac{1}{T_o}\right)^N$$

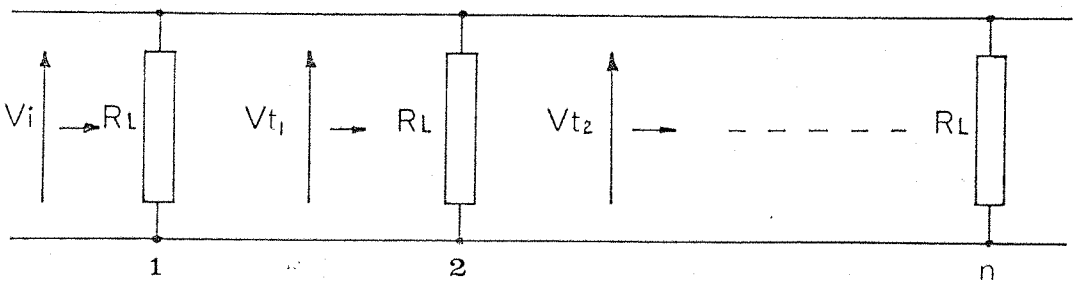
or in (dB),

$$A_N = 2ON \log \left(1 + \frac{R_O}{2R_L}\right)$$



SINGLE LOAD RESISTOR

FIG I1



MULTIPLE LOADS

FIG I2

APPENDIX J

Multiple Transformer Cut-Off Frequencies

Consider the equivalent circuit of n identical transformers and loads connected in parallel across a common source as shown in Figure J1(a) where

R_S = source resistance
R_L = primary referred load resistance
L_k = primary referred leakage inductance
L_p = primary self inductance.

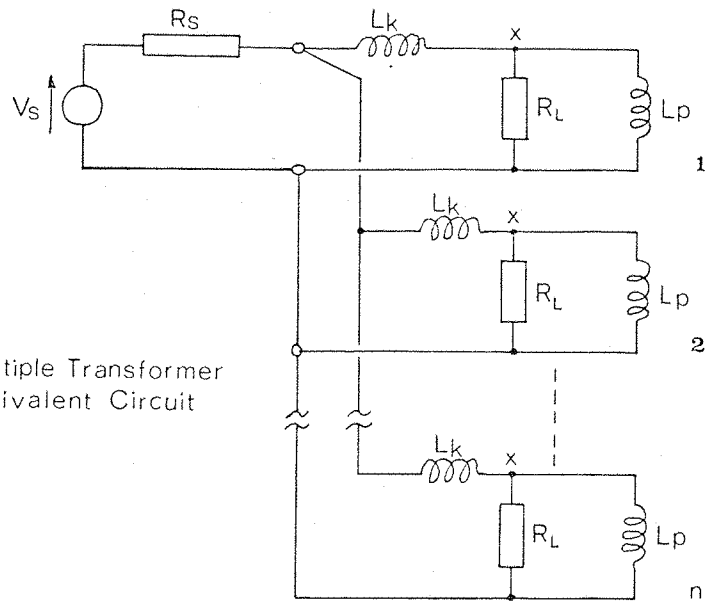
Because of the assumed similarity of the transformer equivalent circuits all the points marked x will be at the same potential and can thus be assumed to be connected together. Therefore the overall equivalent circuit can be represented as in Figure J1(b).

This circuit can now be analysed by making the usual approximations to find the low and high cut-off frequencies. Thus at low frequency the circuit reduces to that shown in Figure J1(c) and the cut-off frequency is given by

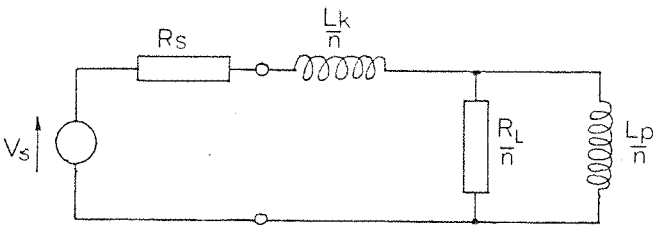
$$W_L = \frac{R_S \frac{R_L}{n}}{\frac{L_p}{n}(R_S + \frac{R_L}{n})} = \frac{R_L}{L_p}\left(\frac{nR_S}{nR_S + R_L}\right) \quad (J1)$$

Similarly from circuit (d) the high cut-off frequency is given by

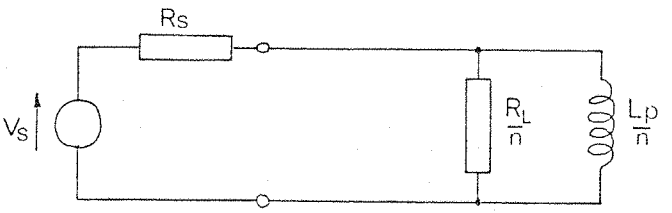
$$W_H = \frac{R_S + \frac{R_L}{n}}{\frac{L_k}{n}} = \frac{R_L}{L_k}\left(1 + \frac{nR_S}{R_L}\right) \quad (J2)$$



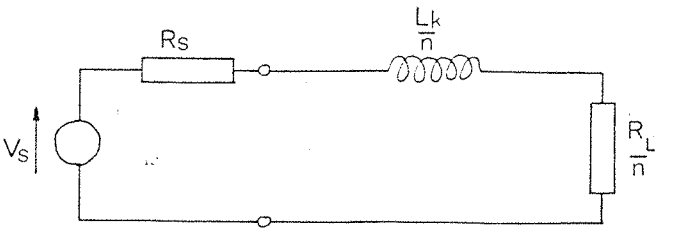
(a) Multiple Transformer Equivalent Circuit



(b) Single Equivalent Circuit



(c) Low Frequency Equivalent Circuit



(d) High Frequency Equivalent Circuit

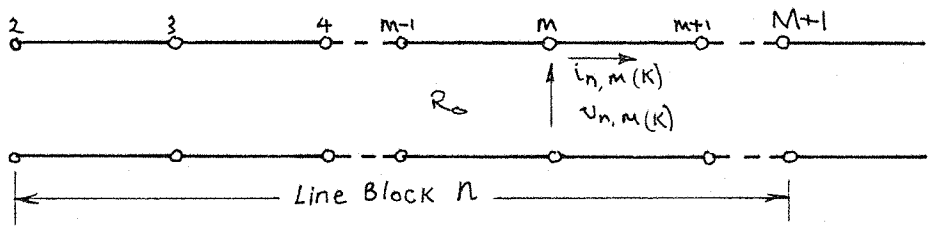
Parallel Transformer Equivalent Circuit

FIG J1

APPENDIX K

Derivation of General Line Difference Equations

Figure K1 shows a section of the numerical model representing the general transmission line.



The General Line

Fig. K1

Consider the mth node within line block n of the system model. The set of difference equations relating the current and voltage at nodes m and m-1, using the results of Equation 4.18 and 4.19 become :

$$v_{n,m}(k) + R_o i_{n,m}(k) = (1-R_o g)v_{n,m-1}(k-1)+(R_o-r)i_{n,m-1}(k-1) \qquad (K1)$$

$$v_{n,m-1}(k) - R_o i_{n,m-1}(k) = (1-R_o g)v_{n,m}(k-1)-(R_o-r)i_{n,m}(k-1) \qquad (K2)$$

Similarly the set of difference equations relating nodes m and m+1 become :

$$v_{n,m+1}(k)+R_o i_{n,m+1}(k)=(1-R_o g)v_{n,m}(k-1)+(R_o-r)i_{n,m}(k-1) \qquad (K3)$$

$$v_{n,m}(k)-R_o i_{n,m}(k)=(1-R_o g)v_{n,m+1}(k-1)-(R_o-r)i_{n,m+1}(k-1) \qquad (K4)$$

Since we are interested in finding the voltage and current relationships at node m, the relevant equations are given by (K1) and (K4). Then, from

(K1) + (K4) we get

$$2v_{n,m}(k)=(1-R_o g)\left[v_{n,m-1}(k-1)+v_{n,m+1}(k-1)\right]+(R_o-r)\left[i_{n,m-1}(k-1)-i_{n,m+1}(k-1)\right]$$

or

$$v_{n,m}(k) = \frac{1-R_o g}{2}\left[v_{n,m-1}(k-1)+v_{n,m+1}(k-1)\right] + \frac{R_o - r}{2}\left[i_{n,m-1}(k-1)-i_{n,m+1}(k-1)\right] \qquad (K5)$$

Similarly from

(K1) - (K4) we obtain

$$i_{n,m}(k) = \frac{1-R_o g}{2R_o}\left[v_{n,m-1}(k-1)-v_{n,m+1}(k-1)\right] + \frac{R_o - r}{2R_o}\left[i_{n,m-1}(k-1)+i_{n,m+1}(k-1)\right] \qquad (K6)$$

Equations K5 and K6 thus give the required general line difference equations.

APPENDIX L

Discrete Model Difference Equations for Computer Solution

L.1 Input Boundary

$$v_{1,1}(k) = y_1 v_{1,2}(k-1) - y_2 i_{1,2}(k-1) + g_1 I(k)$$

$$i_{1,1}(k) = y_3 i_{1,2}(k-1) - y_4 v_{1,2}(k-1) + g_2 I(k) \qquad \text{(L1)}$$

where, $k = 2, 3, \ldots . K_s + 1$

$$y_1 = \frac{R_o(1+R_o g)}{2R_o}$$

$$y_2 = \frac{R_o(R_o - r)}{2R_o}$$

$$y_3 = \frac{R_o - r}{2R_o}$$

$$y_4 = \frac{1 - R_o g}{2R_o}$$

$$g_1 = \frac{R_o R_s}{2R_o}$$

and

$$g_2 = \frac{R_s}{2R_o}$$

R_o = line characteristic impedance
r = resistance of elementary line section
g = conductance of elementary line section
K_s = total number of time steps for computation. (See Appendix M).

L.2 General line

$$v_{n,m}(k)=x_1\left[v_{n,m-1}(k-1)+v_{n,m+1}(k-1)\right]+x_2\left[i_{n,m-1}(k-1)-i_{n,m+1}(k-1)\right]$$

$$i_{n,m}(k)=x_3\left[v_{n,m-1}(k-1)-v_{n,m+1}(k-1)\right]+x_3\left[i_{n,m-1}(k-1)+i_{n,m+1}(k-1)\right] \quad \text{(L2)}$$

$n = 1, 2, \ldots N+1$

$m = 2, 3, \ldots M+1$

$k = 2, 3, \ldots K_s$

where,

$$x_1 = \frac{1-R_o g}{2}$$

$$x_2 = \frac{R_o - r}{2}$$

$$x_3 = \frac{1-R_o g}{2R_o}$$

$$x_4 = \frac{R_o - r}{2R_o}$$

N = total number of loads

M = total number of basic time steps between line sections.

L.3 Last Node of Line

$$v_{n,M+1}(k)= z_1 v_{n,M}(k-1)+z_2 i_{n,M}(k-1)+z_3 v_{n+1,1}(k-1)$$

$$-z_4\left[C1_n(k-1)+C3_n(k-1)+i_{n+1}(k-1)\right] \quad \text{(L3)}$$

$$i_{n,M+1}(k)=z_5 v_{n,M}(k-1)+z_6 i_{n,M}(k-1)-z_7 v_{n+1}(k-1)$$

$$+z_8\left[C1_n(k-1)+C3_n(k-1)+i_{n+1}(k-1)\right]$$

$$n = 1, 2, \ldots\ldots N$$
$$k = 2, 3, \ldots\ldots K_s + 1$$

where,

$$z_1 = \frac{R_2(1-R_o g)}{R_o + R_2}$$

$$z_2 = \frac{R_2(R_o - r)}{R_o + R_2}$$

$$z_3 = \frac{R_o}{R_o + R_2}$$

$$z_4 = \frac{R_o R_2}{R_o + R_2}$$

$$z_5 = \frac{1 - R_o g}{R_o + R_2}$$

$$z_6 = \frac{R_o - r}{R_o + R_2}$$

$$z_7 = \frac{1}{R_o + R_2}$$

$$z_8 = \frac{R_2}{R_o + R_2}$$

R_2 = equivalent characteristic impedance of load capacitance.

L. 4 First Node of Line

$$v_{n+1,1}(k) = a_1 v_{n+1,2}(k-1) - a_2 i_{n+1,2}(k-1) + a_3 v_{n,M+1}(k-1) + a_4 \left[i_{n,M+1}(k-1) - C2_n(k-1) \right] \qquad (L4)$$

$$i_{n+1,1}(k)=a_5 i_{n+1,2}(k-1)-a_6 v_{n+1,2}(k-1)+a_7 v_{n,M+1}(k-1)$$

$$+a_8\left[i_{n,M+1}(k-1)-C2_n(k-1)\right]$$

$$n = 1, 2, \ldots\ldots N$$

$$k = 1, 2, \ldots\ldots K_s+1$$

where ,

$$a_o = R_o R_2+R_o R_3+R_2 R_3+R_o R_2 R_3/R_L$$

$$a_1 = \frac{R_2 R_3(1 - R_o g)}{a_o}$$

$$a_2 = \frac{R_2 R_3(R_o-r)}{a_o}$$

$$a_3 = \frac{R_o R_3}{a_o}$$

$$a_4 = \frac{R_o R_2 R_3}{a_o}$$

$$a_5 = \frac{(R_2+R_3+R_2 R_3/R_L)(R_o-r)}{a_o}$$

$$a_6 = \frac{(R_2+R_3+R_2 R_3/R_L)(R_o-r)}{a_o}$$

$$a_7 = \frac{R_3}{a_o}$$

$$a_8 = \frac{R_2 R_3}{a_o}$$

R_3 = equivalent characteristic impedance of load inductance

R_L = load resistance

L.5 Load Terminal

$$C1_n(k) = d_1 v_{n+1,1}(k) + C2_n(k-1)$$

$$C2_n(k) = d_1 v_{n+1,1}(k-1) + C1_n(k-1) \qquad \text{(L5)}$$

$$C3_n(k) = \frac{v_{n+1,1}(k)}{R_L}$$

$$n = 1, 2, \ldots\ldots \quad N$$

$$k = 2, 3, \ldots. \; K_s+1$$

where,

$$d_1 = \frac{1}{R_3}$$

L.6 Output Boundary

$$i_{N+1,M+1}(k) = d_1 v_{N+1,M}(k-1) + d_2 i_{N+1,M}(k-1)$$

$$v_{N+1,M+1}(k) = R_o i_{N+1,M+1}(k) \qquad \text{(L6)}$$

$$k = 2, 3, \ldots\ldots K_s+1$$

where,

$$d_1 = \frac{1 - R_o g}{2R_o}$$

$$d_2 = \frac{R_o - r}{2R_o}$$

APPENDIX M

Input Parameters for Numerical Solution

The required data inputs are classified into three categories namely ;

line parameters
load parameters
and terminal parameters.

Line Parameters

These are given as :

ℓ = transmission line length (m)
R = resistance per unit length (Ω/m)
L = inductance per unit length (H/m)
C = capacitance per unit length (F/m)
G = conductance per unit length (℧/m)

Load Parameters

L_L = load inductance (H)
C_L = load capacitance (F)
R_L = load resistance (Ω)
N = total number of loads
d_n = distance between loads n and n-1 (m)
$n = 1, 2, \ldots . N$

For the uniformly distributed line, all $d_n = d$.

Terminal Parameters

T_s = basic time step (S)

I(k)= input current samples at discrete time intervals (T_s) (A)

$k = 1, 2, \ldots . NC$

t_d : duration of input current waveform

R_o: source resistance (Ω)

M.1 Initial Calculations

The relevant secondary data required in the main program is calculated using the following relationships :

Line characteristic impedance

$$R_o = \sqrt{\frac{L}{C}} \qquad (M1)$$

Delay of unit length of line

$$T_d = \sqrt{LC} \qquad (M2)$$

Resistance of elementary line section of delay T_s

$$r = R\, T_s / T_d \qquad (M3)$$

Conductance of elementary line section of delay T_s

$$g = G T_s / T_d \qquad (M4)$$

Equivalent characteristic impedance of load capacitance

$$R_2 = T_s / C_L \qquad (M5)$$

Equivalent characteristic impedance of load inductance

$$R_3 = L_L / T_S \qquad (M6)$$

Number of basic time steps within line section n

$$S_n = d_n T_d / T_s \qquad \text{(M7)}$$

$$n=1, 2, \ldots\ldots N$$

Number of basic time steps within input signal period

$$C_s = t_d / T_s \qquad \text{(M8)}$$

Total number of computation time steps

Let J be the load terminal number at which the voltage or current output is desired.

Then the total number of basic time steps to the load, from the source is given by

$$S_1 + S_2 + \ldots\ldots + S_J + J = J + \sum_{n=1}^{J} S_n$$

Note : the addition of J accounts for the unit delays introduced by the load capacitances.

Then, taking the input signal duration into account, the total number of computation time steps at load J becomes :

$$K_s = C_s + J + \sum_{n=1}^{J} S_n \qquad \text{(M9)}$$

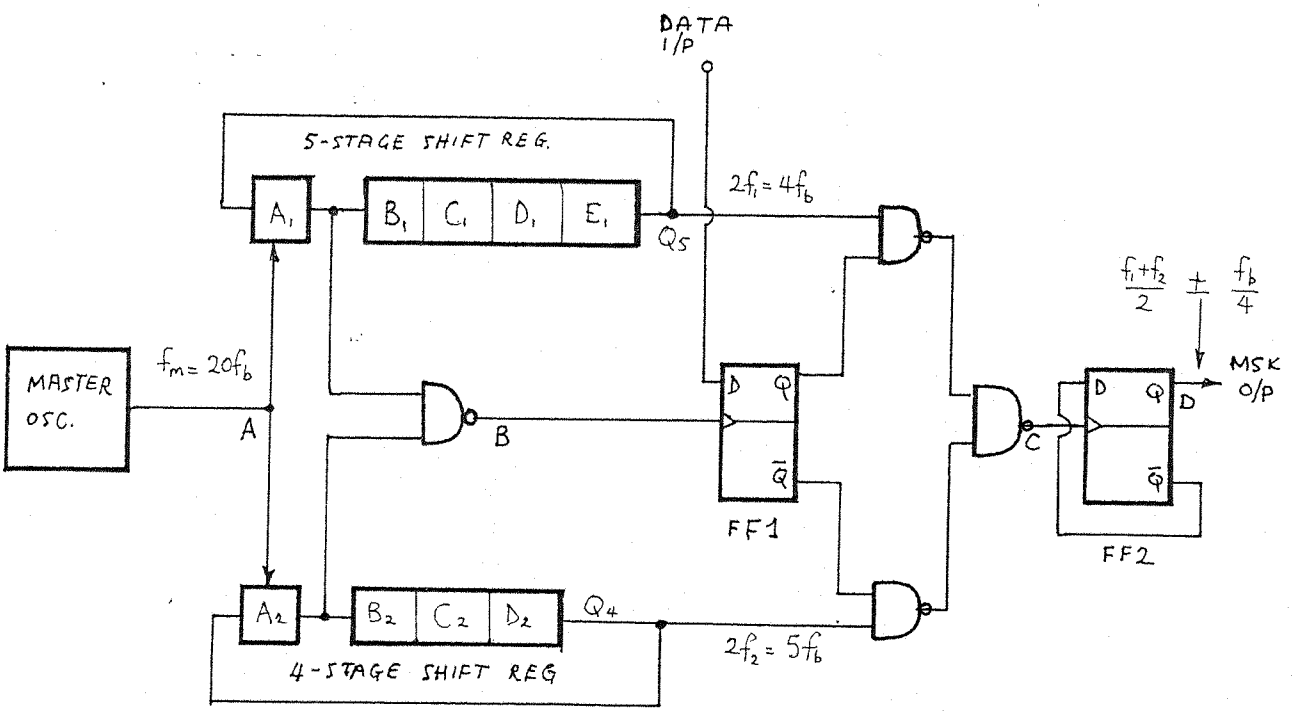
At the line output

$$K_s = C_s + J + \sum_{n=1}^{N+1} S_n \qquad \text{(M10)}$$

APPENDIX N

Description of MSK Modulator

Figure N1 illustrates the digital circuit that was used to implement the generation of the MSK signal. The master oscillator generates a frequency at the rate given by $f_m = p(p+1)f_b = 20f_b$. The output of the master oscillator clocks the 4-stage and 5-stage shift registers connected in a feedback arrangement, which continually circultates the data sequences OOOl and OOOOl respectively. (This data is initially preset). The mark and space frequencies, $2f_1$, and $2f_2$, are derived from the outputs Q_5 and Q_4 of the shift registers respectively. The clock frequency f_b is obtained by NANDing the first stage outputs A_1 and A_2 of the two shift registers. The arrangement of the threeNAND gates and the flip-flop FFl give an FSK signal with centre frequency $2f_c = f_1 + f_2$ and frequency deviation $\Delta f = f_b$ at point C. Finally the required MSK signal is derived from the output D of the divide-by-two flip-flop FF2 to give a centre frequency $f_c = (f_1 + f_2)/2$ and frequency deviation $\Delta f = f_b/2$.



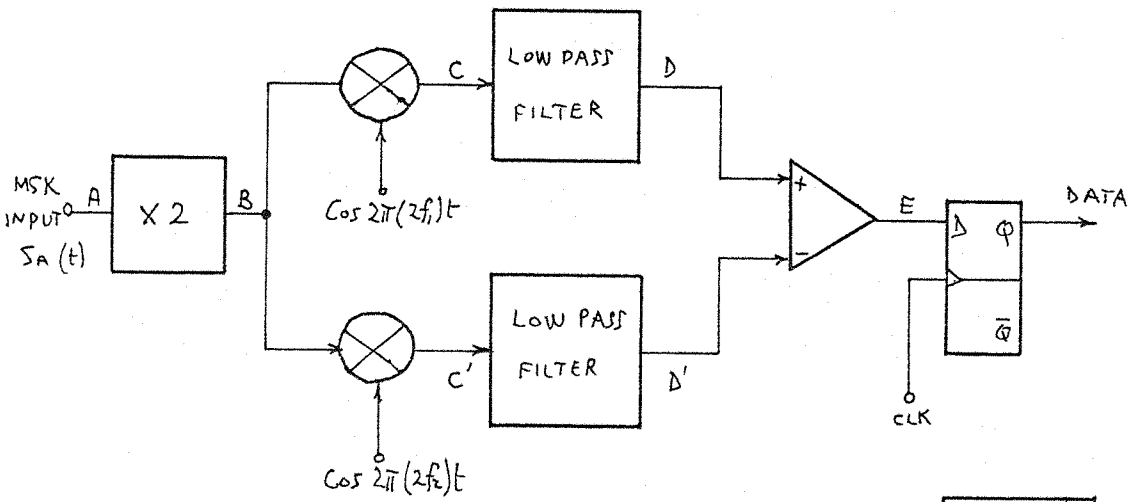
MSK Modulator

Fig. N.1

APPENDIX P

Error Probability of Correlation Demodulator

The demodulator circuit of Figure 5.13 is reproduced in Figure P1 below for convenience.



Correlation Demodulator

Fig. P.1

Let f_1 = 'mark' frequency

f_2 = 'space' frequency

f_b = bit frequency

T = bit period

A_v = input signal amplitude

N_o = noise spectral density

σ = noise r.m.s. voltage

V = signal amplitude at decision point E

E = input signal energy per bit

P.1 Output Waveform

Referring to Figure P1, the MSK signal at A can be expressed as

$$s_A(t) = A_v \cos\left[\pi(f_1 + f_2)t \pm \pi t/2T\right] \qquad \text{P.1}$$

$$O \leq t \leq T$$

The sign of the second term within the bracket is positive for space, and negative for mark.

At B, after frequency doubling we get,

$$s_B(t) = A_v \cos\left[2\pi\ (f_1+f_2)t \pm \pi t/T\right] \qquad \text{P.2}$$

$$O \leq t \leq T$$

At C, the input signal is correlated with the reference signal to give

$$s_C(t) = s_B(t) \cos\ 4\pi f_1 t \qquad \text{P.3}$$

At D, the filter passes the low frequency components of the signal at C to give

$$s_D(t) = \frac{A_v}{2} \cos\left[2\pi(f_2 - f_1)t \pm \pi t/T\right] \qquad \text{P.4}$$

But for the MSK signal $2(f_2 - f_1) = f_b = 1/T$.
Hence,

$$s_D(t) = \frac{A_v}{2} \begin{cases} 1 & \text{'mark' transmitted} \\ \cos 2\pi t/T & \text{'space transmitted} \end{cases}$$

Similarly at D' we obtain

$$s_{D'}(t) = \frac{A_v}{2} \begin{cases} \cos\ 2\pi t/T & \text{'mark'} \\ 1 & \text{'space'} \end{cases}$$

The signal at the decision point E thus becomes

$$s_E(t) = \frac{A_v}{2} \begin{cases} 1-\cos 2\pi t/T & \text{'mark'} \\ -(1-\cos 2\pi t/T) & \text{'space'} \end{cases} \qquad \text{P.5}$$

$$O \leq t \leq T$$

The peak signal occurs at T/2 and is given by

$$V = \pm A_v \qquad \text{P.6}$$

The signal waveform given by (P5) for an arbitrary input data sequence is shown in Figure P2.

Typical experimental waveform obtained at point E is shown in Figure P.3. The decoded binary data is also shown.

P.2 Error Probability

Referring to Figure P2, the signal at the decision input is decoded by strobing the $\frac{1}{2}$ bit points where the peak signal occurs.

The probability of Gaussian zero mean noise of r.m.s. level σ exceeding the peak signal voltage V at the strobing instant is given by

$$P_e = \tfrac{1}{2}\,\mathrm{erfc}\left(\frac{V}{\sigma\sqrt{2}}\right) \qquad \text{(P.7}$$

After passing through the low-pass filter of bandwidth f_o, the noise power at point E is effectively doubled because, since white noise is assumed, the variances add at the output of the subtractor.

For a noise spectral density given by N_o, then the noise power at point E becomes,

$$\sigma^2 = 2N_o f_o \qquad \text{P.8}$$

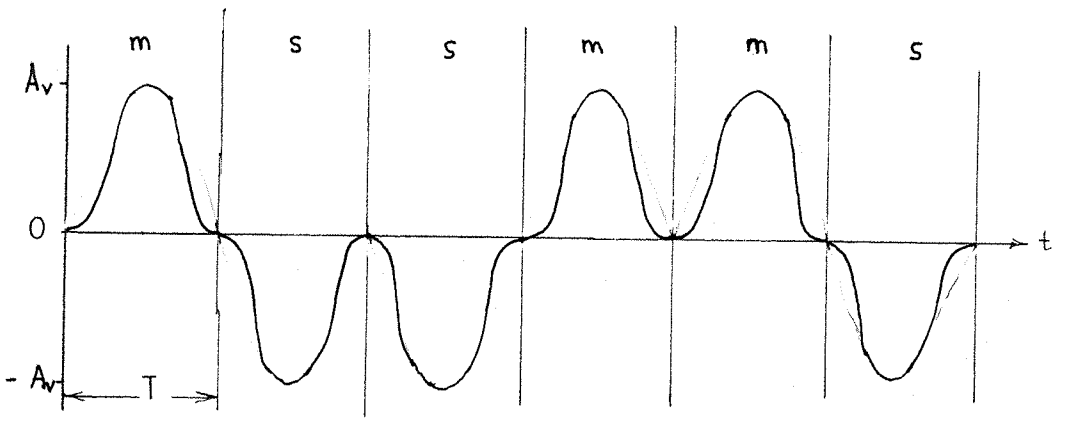
Substituting (P6) and (P8) into (P7) we obtain,

$$P_e = \tfrac{1}{2}\,\mathrm{erfc}\sqrt{\frac{A_v^2}{2}\cdot\frac{1}{2N_o f_o}}$$

$$= \tfrac{1}{2}\,\mathrm{erfc}\sqrt{\frac{A_v^2 T}{2}\cdot\frac{1}{2N_o f_o T}} \qquad \text{P.9}$$

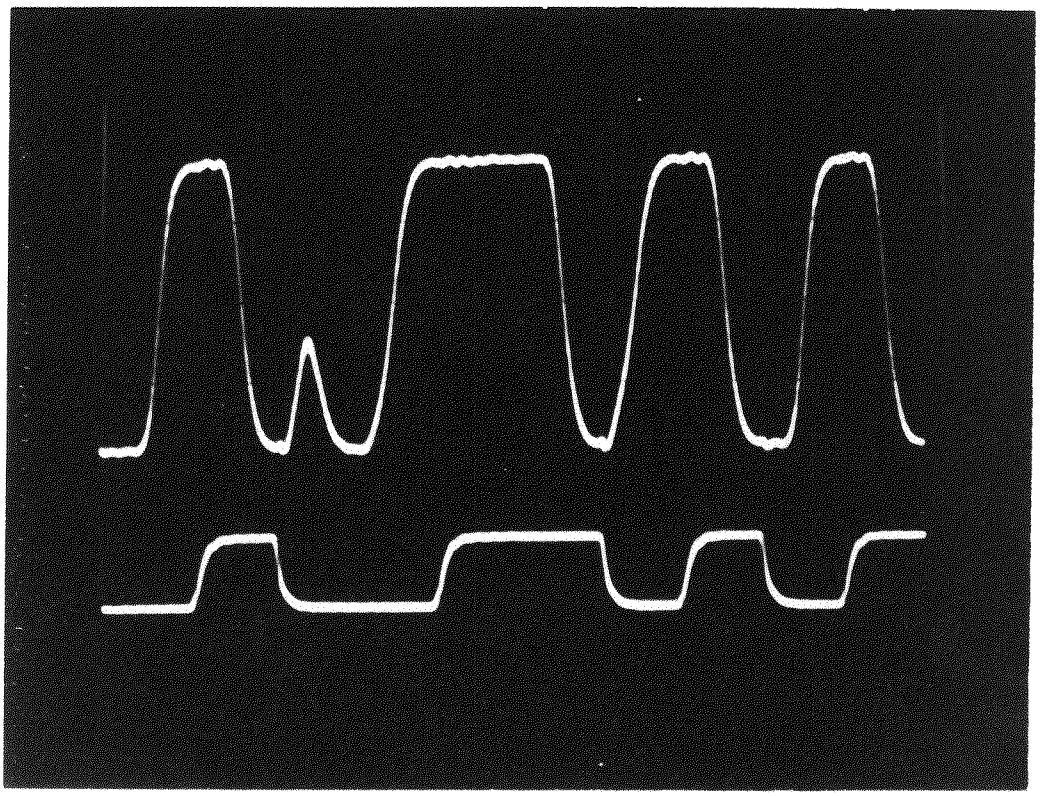
But the energy per bit of the incoming MSK signal is given by $E = A_v^2 T/2$, and (P9) becomes

$$P_e = \tfrac{1}{2}\,\mathrm{erfc}\sqrt{\frac{E}{N_o}\cdot\frac{1}{f_o T}\cdot\frac{1}{2}} \qquad \text{P.10}$$



Demodulated Signal

Fig. P. 2



Output Waveform and Decoded Data of Correlation Demodulator

FIG P3

APPENDIX Q

Error Probability of Differential Strobe Demodulator

Figure 5.13 shows the timing diagram of the demodulator. The eye diagram of the received MSK signal is also shown in Figure 5.13.

The probability of Gaussian zero mean noise of r. m. s. level σ exceeding a signal voltage level V is given by

$$P_{el} = \tfrac{1}{2}\ \text{erfc}\ \left(\frac{V}{\sigma\sqrt{2}}\right) \qquad \text{Q.1}$$

At the decision time, when the two signalling waveform amplitudes are equal as shown in Figure 5.13,

$$t = 8T/9$$

$$\text{and} \qquad V = 0.9848\ A_v \qquad \text{Q.2}$$

For a noise spectral density N_o, the noise power at the output of the filter with cut-off frequency f_o becomes,

$$\sigma^2 = N_o f_o \qquad \text{Q.3}$$

Substituting (Q2) and (Q3) into (Q1) we get

$$P_{el} = \tfrac{1}{2}\ \text{erfc}\ \sqrt{\frac{A_v^2}{2} \cdot \frac{1}{1.031\ N_o f_o}}$$

$$= \tfrac{1}{2}\ \text{erfc}\ \sqrt{\frac{A_v^2 T}{2} \cdot \frac{1}{1.031 N_o f_o T}} \qquad \text{Q.4}$$

But the signal energy per bit,

$$E = \frac{A_v^2 T}{2}, \text{ and (Q4) becomes}$$

$$P_{el} = \tfrac{1}{2}\ \text{erfc}\ \sqrt{\frac{E}{N_o} \cdot \frac{1}{1.031 f_o T}} \qquad \text{Q.5}$$

The decoding process is effected by the comparison of the polarities of two consecutive bits and makes the decision :

'mark' : if the polarities are the same,
'space' : if the polarities are opposite.

An error occurs if either one of the two consecutive bits is in error, the other being correct.

Since P_{el} is the probability of one bit error the probability of error in the decoding process (P_e) becomes

$$P_e = P_{el}(1 - P_{el}) + P_{el}(1 - P_{el})$$

$$= 2P_{el}(1 - P_{el}) \qquad \text{Q. 6}$$

Making the substitution for (Q5) in (Q6) we obtain

$$P_e = \operatorname{erfc} \sqrt{\frac{E}{N_o} \cdot \frac{1}{1{,}031 f_o T}} - \operatorname{erfc}^2 \sqrt{\frac{E}{N_o} \cdot \frac{1}{1{,}031 f_o T}} \qquad \text{Q. 7}$$

APPENDIX R

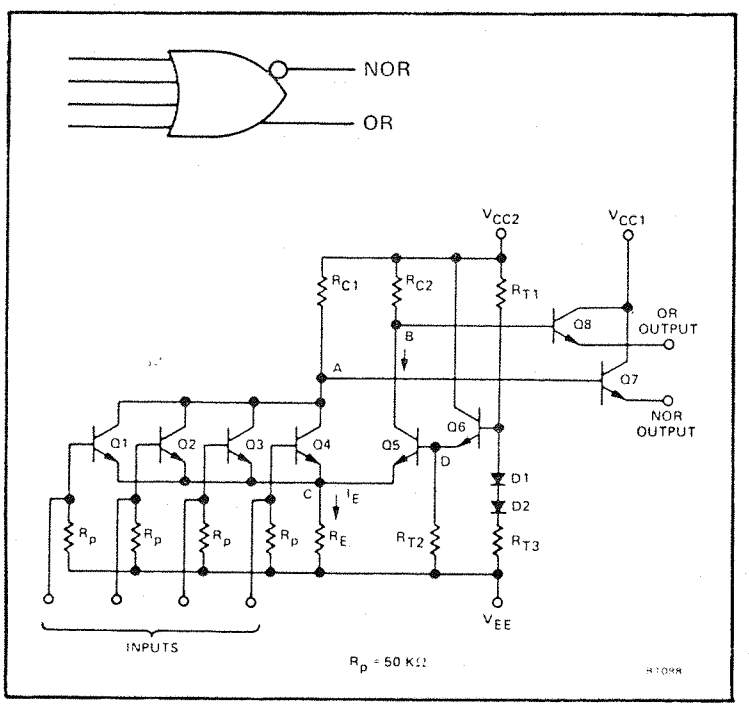
The ECL 10000 Logic

The information given here are the relevant excerpts from the manufacturers application notes (28) on the ECL 10000 logic, hither to referred as MECL as per the manufacturers ; and the layout principles used for the transmitter and receiver boards.

R.1 Basic Building Block

A basic building block of the family, the gate shown in Figure R1, is an emitter coupled (current mode) switch with emitter-follower outputs. MECL circuit operation is similar to that of a linear differential amplifier.

Input pulldown resistors of 50 KΩmaintain the inherent high input impedance of the MECL gate and to conserve power dissipation on the chip.



MECL 10,000 Basic Gate

Fig. R. 1.

R.1.1 Logic Levels

The reference voltage about which the MECL gate switches is V_{BB} (Node D) of Figure R1, as shown in Figure R2. A high logic level is obtained if the input voltage goes above V_{BB} and a low logic level if the input voltage drops below V_{BB}.

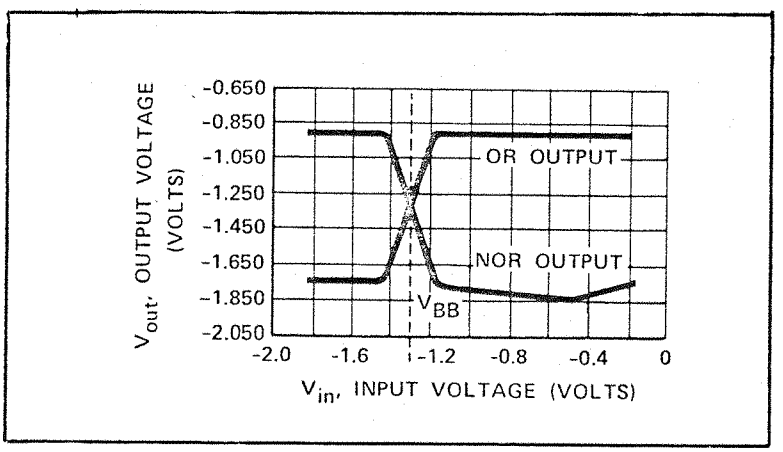


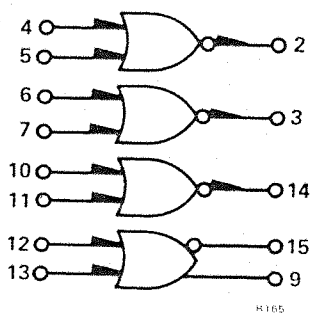
Fig. R. 2

R. 2 Characteristics and Pin Connections

The characteristics and pin connections of all the MECL packages used are given below :

MC10102

QUAD 2-INPUT GATE



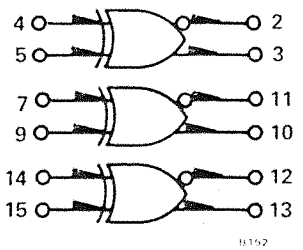
V_{CC} (GROUND) = PINS 1,16
V_{EE} (-5.2 Vdc) = PIN 8

- Slow Rise And Fall Times – 3.5 ns
- High Speed – 2.0 ns
- Low Power – 25 mW/Gate
- High Fanout – 50 mA/Output
- 50 Ω Line Driving Capability
- High Z Input Pulldowns
- Open Emitter Follower Outputs
- Wire OR Capability
- Complementary Outputs – For Added Versatility
- Standard End Power Pins – For Conventional Layout
- Separate V_{CC} Pins – Maintain High Speed And Minimize Crosstalk And Noise Generation
- Compatible With MECL III (MC10102 Is Pin Compatible MC1662)

Fig. R. 3

MC10107

TRIPLE EXCLUSIVE
OR/EXCLUSIVE NOR

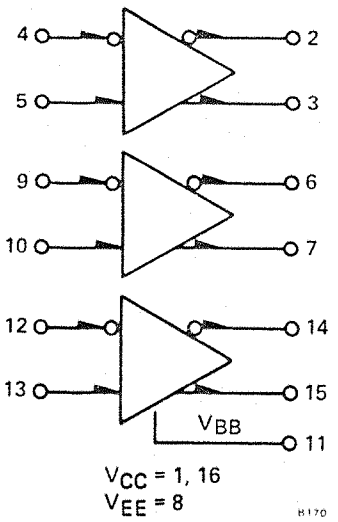


- Slow Rise And Fall Times – 3.5 ns
- High Speed – t_{pd} = 2.0 ns
- Low Power – 115 mW/pkg
- High Fanout – 50 mA
- Open Emitter Follower Outputs – For Wire OR
- Complementary Outputs – Simulaneous Functions
- Standard End Power Pins – Conventional Layout
- Separate V_{CC} Pins Maintain High Speed and Minimize Crosstalk and Noise Generation
- Compatible With MECL III – For Very High Speed Applications

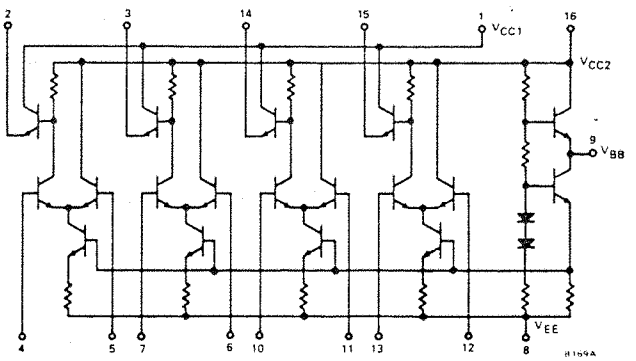
Fig. R. 4

MC10116/MC10216

TRIPLE DIFFERENTIAL
LINE RECEIVER



- High Speed – 2.0 ns (10116, 115) or 1.5 ns (10216)
- Low Power – 20 mW/Receiver
- High Z Inputs – For Reduced Power Dissipation
- Open Emitter Follower Outputs
- High Fanout
- 50 Ω Line Driving Capability
- Wire OR Capability
- Standard End Power Pins
- V_{BB} Reference
- Excellent Common Mode Noise Rejection
- Compatible With MECL III (10115 is Pin Compatible With The 1692) (10116 is Compatible With 10216)
- Separate V_{CC} Pins Maintain High Speed And Minimize Crosstalk and Noise Generation
- Common Mode Gain ≈ 12 V/V
- Balanced Twisted Pair Receiving And Driving Capability

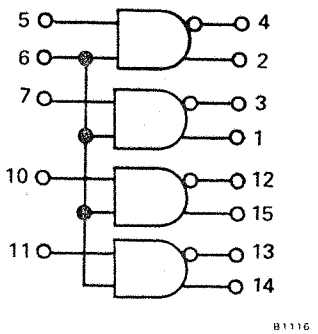


MC10115 Circuit Schematic

Fig. R. 5

MC10124

QUAD MTTL TO MECL TRANSLATOR WITH STROBE



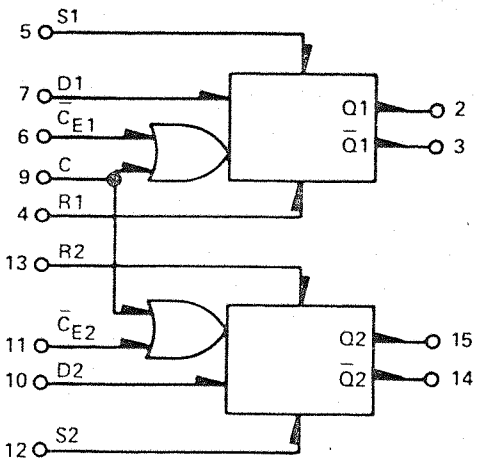
GND = 16
V_{CC} (+5.0 Vdc) = 9
V_{EE} (-5.2 Vdc) = 8

- High Speed – t_{pd} = 6 ns
- Differential Inputs And "Totem Pole Outputs" On 10125
- Standard TTL Inputs And Open Emitter Follower Outputs On 10124
- Four Translators Per Package

Fig. R. 6

MC10131/MC10231

DUAL "D" FLIP-FLOPS



V_{CC} (GROUND) = PINS 1, 16
V_{EE} (–5.2 Vdc) = PIN 8

R-S TRUTH TABLE

R	S	Q^{n+1}	$\overline{Q}^{n+1}$
L	L	Q^n	$\overline{Q}^n$
L	H	H	L
H	L	L	H
H	H	N.D.	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

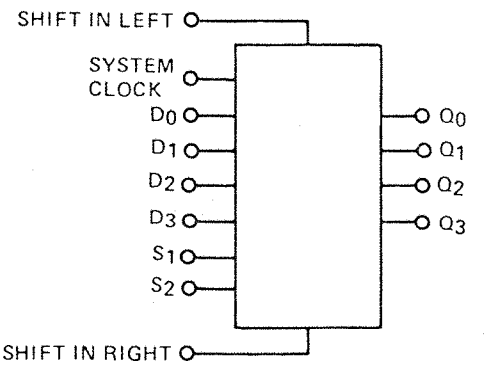
D	*C	$\overline{C}_E$	Q_{n+1}
L	L	L	Q_n
L	L	H	Q_n
L	H	L	L
L	H	H	Q_n
H	L	L	Q_n
H	L	H	Q_n
H	H	L	H
H	H	H	Q_n

- High Speed – 150 MHz (10131, 10135), 200 MHz (10231)
- Low Power – 225 mW/pkg
- Slow Rise And Fall Times – 4.5 ns Delay
- High Fanout – Better AC Performance
- 50 Ω Line Driving Capability
- High Z Input Pulldown Resistors – Minimum Power Dissipation And Ease Of Layout
- Master Slave Operation – For Dependability
- Clock Can Be Controlled On Chip – Seperate Clock Enable
- Standard End Power Pins
- Compatible With MECL III – For Very High Speed Operation

Fig. R. 7

MC10141

4-BIT UNIVERSAL SHIFT REGISTER



FUNCTION TABLE

Select		Operating Mode
S_1	S_2	
L	L	Parallel Entry
L	H	Shift Right
H	L	Shift Left
H	H	Stop Shift

- Slow Rise And Fall Times – 3.5 ns
- High Speed – 100 MHz Shift Frequency
- Low Power
- High Fanout – 50 mA
- 50 Ω Line Driving Capability On All Outputs
- High Z Input Pulldowns – Lower Power Dissipation
- Open Emitter Follower Outputs – Allow Complete Termination Flexibility
- Chip – Reduces System Package Count
- Standard End Power Pins
- Separate V_{CC} Pins Maintain High Speed And Minimize Crosstalk And Noise Generation

Fig. R. 8.

R. 3 Relevant Circuit Applications

The circuits and notes given here are the suggested applications of the MECL logic which were applied to the design of the transmitter and receiver circuits.

Overtone Crystal Oscillator

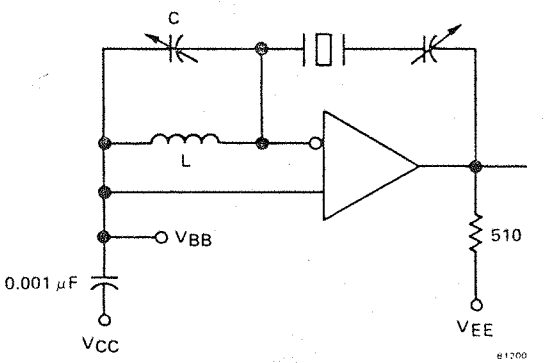


Fig. R9

Small Signal Amplifier

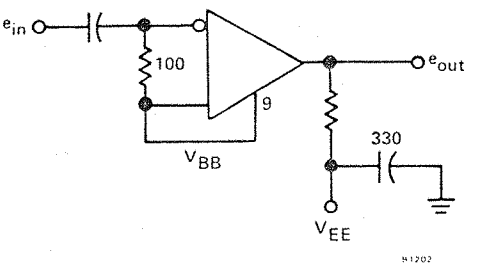


Fig. R10

Schmitt Trigger

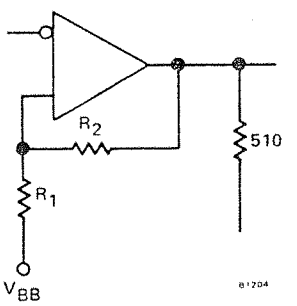


Fig. R11

R.4 Layout Principles of Transmitter and Receiver Boards

In order to achieve the high speed available to MECL 10,000 systems, two sided printed circuit boards as recommended, were used. One side of the board serves as a ground plane.

See Figure R12.

The ground plane serves two purposes. It provides a transmission line environment for high speed signal propagation, and a very low inductance path for ground currents.

Because signal interconnects on both the transmitter and receiver boards were less than 12 inches, a non-terminated line configuration as recommended, was used. This arrangement is shown in Figure R13.

A single pull down resistor (R_E) to V_{EE} provides a path for output current. The recommended values of R_E is 4.5 Z_o to 10 Z_o, where Z_o is the characteristic impedance of the transmission line formed by the microstrip interconnects.

R.4.1 Calculation of Z_o

The epoxy-glass printed circuit board used has the cross-sectional dimensions as shown in Figure R14. Referring to this figure, the characteristic impedance of the line formed was calculated using the relationship,

$$Z_o = 34.4 \log_e \frac{5.98\,h}{0.8\,W+t} \qquad \text{R.1}$$

A value of $Z_o = 100\Omega$ was used for all the interconnects, and from Equation R1, the corresponding width of the microstrip was calculated ; i.e. W = 0.026 ins.

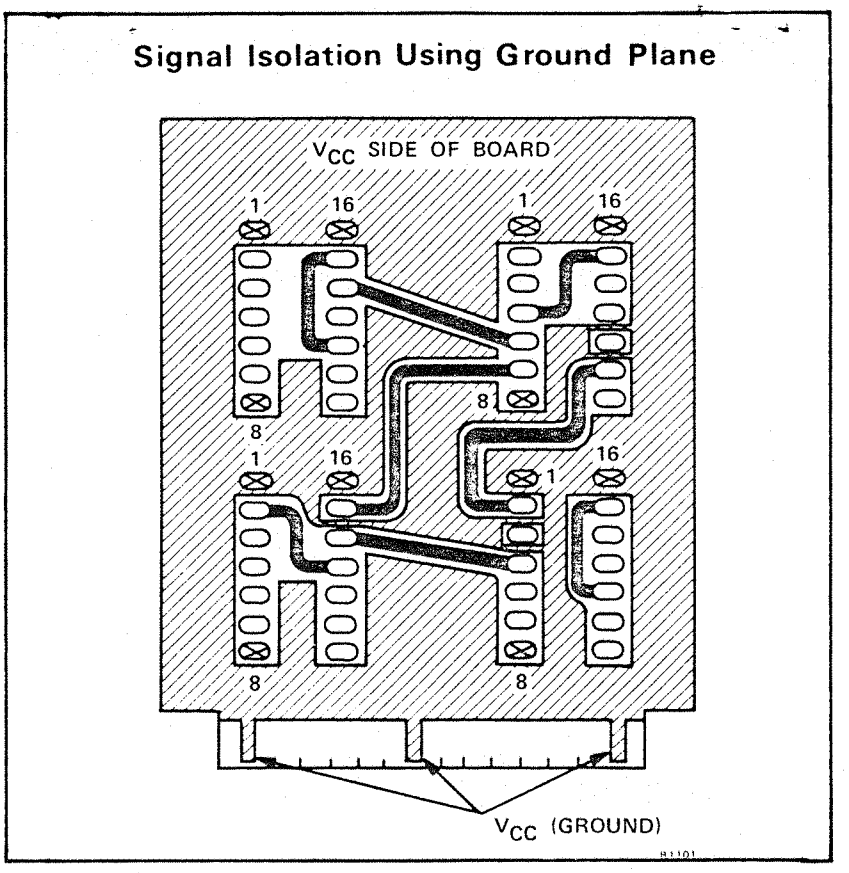


Fig. R12

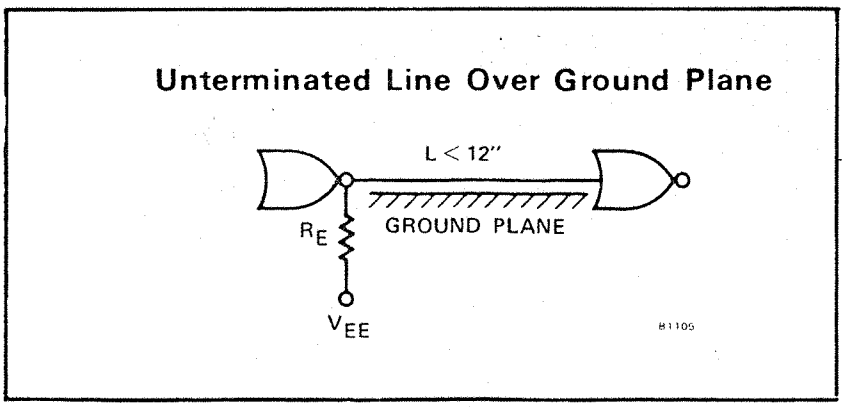


Fig. R13

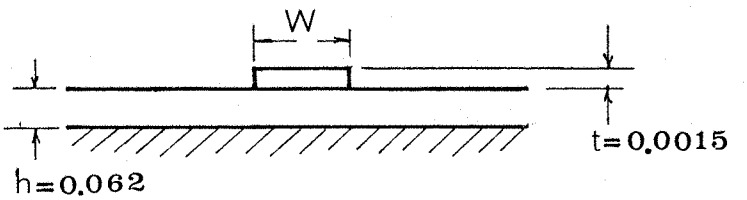
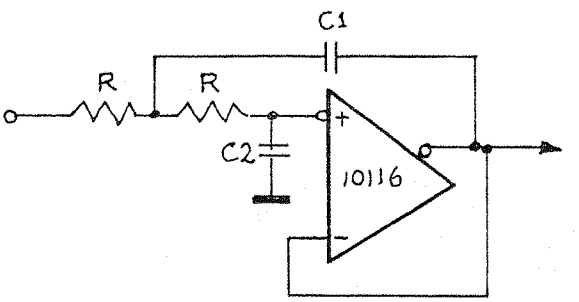


Fig. R14

APPENDIX S

Low Pass Filter Circuit

Figure S1 shows the circuit diagram of the low pass filter network used.



Filter

Fig. S1

It is an active implementation of a 2nd order Butterworth RC filter. The op-amp in this case is the ECL receiver type 10116.

Design Equations

The normalised element values of the filter as given by standard tables are :

$$C1 = 1.414$$
$$C2 = 0.7071$$
$$R = 1.0 \qquad \text{S.1}$$

Let R', C1', C2' be the desired physical element values, then

$$C1' = \frac{C1}{2\pi f_o} \cdot \frac{1}{R'} \qquad \text{S. 2}$$

$$C2' = \frac{C2}{2\pi f_o} \cdot \frac{1}{R'} \qquad \text{S. 3}$$

where f_o = 3 dB cut off frequency.

Example

Consider the design of a low pass filter with the following specifications :

Input resistance R' = 470Ω
Cut off frequency f_o = 6 MHz

Then from the above equations,

$$C_1' = \frac{1.414}{2\pi \times 6 \times 10^6} \cdot \frac{1}{470}$$

$$= 79.8 \text{ pF}$$

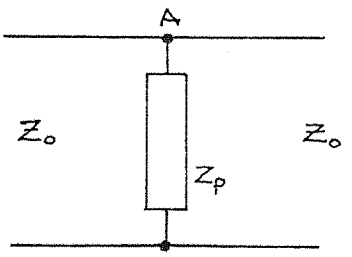
$$C_2' = \frac{0.707}{2\pi \times 6 \times 10^6} \cdot \frac{1}{470}$$

$$= 39.9 \text{ pF}$$

APPENDIX T

Transformer Tap Loss

Consider a section of a matched transmission line with a tapped load Z_p connected on the line as shown in Figure T1.



Tapped Line

Fig. T1

The reflection coefficient at the tapping point A is given by

$$r_c = \frac{-Z_o}{Z_o + 2Z_p} \qquad \text{T.1}$$

The corresponding transmission coefficient becomes,

$$T_o = 1 + r_c$$

$$= \frac{2 Z_p}{Z_o + 2Z_p} \qquad \text{T.2}$$

T.1 Transformer Tap Analysis

From figure 5.17, the effective load resistance 'seen' in parallel with the line is given by

$$R_p = n^2 R_L$$

The reflection coefficient at point A due to mismatch then becomes

$$r_c = \frac{-R_o}{R_o + 2n^2 R_L}$$

$$\therefore \quad T_o = \frac{2n^2 R_L}{R_o + 2n^2 R_L}$$

The received voltage ratio = 1/n.

Then from the loss ratio definitions given in section 5.5.1 :

$$\beta_c = \frac{T_o}{n} = \frac{2nR_L}{R_o + 2n^2 R_L} \qquad \text{T.3}$$

$$\beta_i = T_o = \frac{2n^2 R_L}{R_o + 2n^2 R_L} \qquad \text{T.4}$$

$$\beta_r = r_c = \frac{-R_o}{R_o + 2n^2 R_L} \qquad \text{T.5}$$

APPENDIX U

Wideband Noise Generator

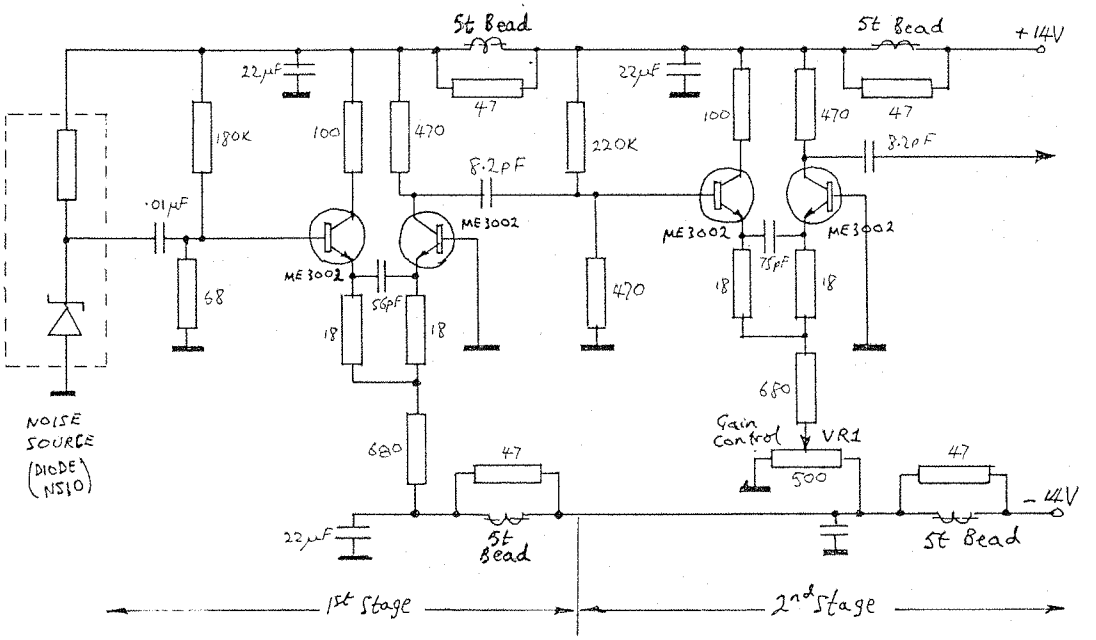
Figure U1 shows the circuit diagram of the first two stages of the 7 stage noise generator. Noise is generated by the diode which is suitably biased i.e. reverse biased, to give an output noise of 0.5 mV (rms) maximum. The noise source covers the frequency range 300 kHz to 1 GHz which is then limited at the output of the amplifier to a bandwidth of 50 MHz, with centre frequency of 60 MHz. Stages 3 to 6 of the generator are similar to the 2nd stage circuit.

The gain of the stages is kept low to increase the stability factor and resistor VR1 acts as the gain control. The supply rail is decoupled in each stage by LCR arrangement shown, to ensure against parasitic oscillations.

Power Output Stage

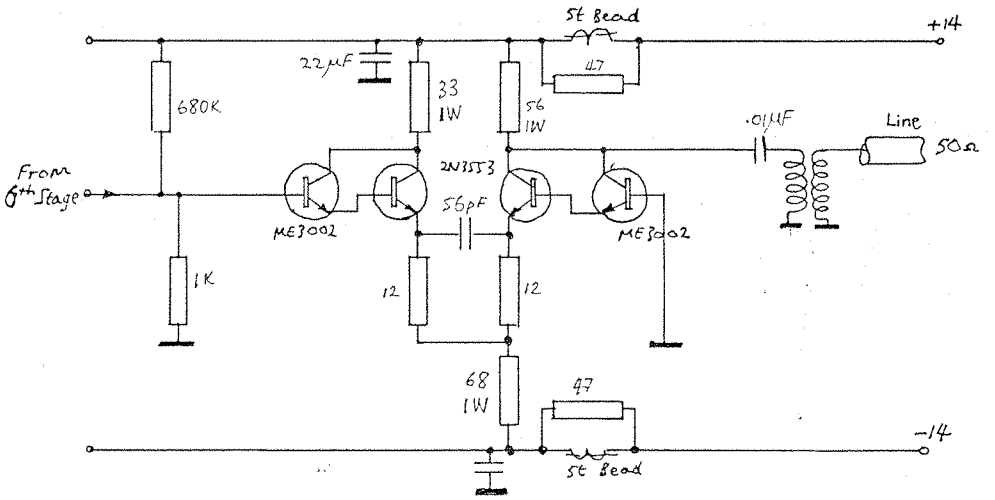
The output stage of the noise generator is shown in Figure U2. It employs a darlington pair as a single transistor to boost the current gain of the long-tail pair arrangement.

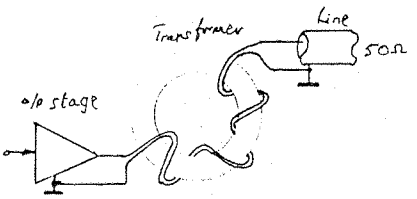
Note : The source of the design of the above noise generator circuit is given in (33).



Noise Generator Circuit

FIG U1





Output Transformer

7 turns of 30 s.w.g. wire
on Ring Core Type: SEI MM622P
Wires twisted to reduce stray capacitances.
Z_o of winding ≈ 50Ω

Noise Amplifier Circuit

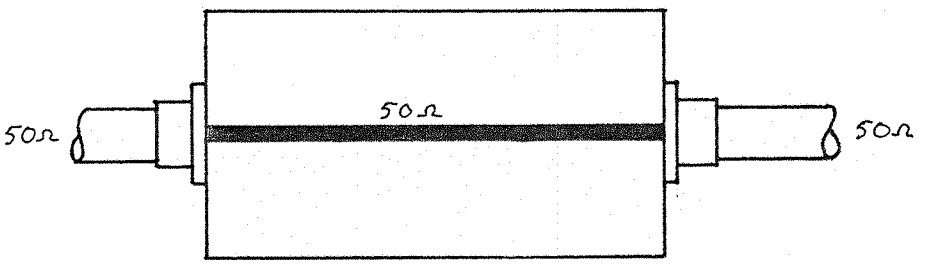
FIG U2

APPENDIX V

Coupling P. C. B.

A schematic diagram of the PCB module is shown in Figure V1. The cables are connected to the board via 50ΩN-type connectors. The 50Ω microstrip provides a through connection for the cables ; it is also used as the tapping points for the simulated terminal loads.

The details of the epoxy-glass PCB and the microstrip design equations are given in Appendix R. 4. 1.



Coupling PCB Fig. V1

Tap Data

Total Number of turns ÷ 25
Wire Gauge ÷ 33 s.w.g.
Core Type ÷ Air Cored
Winding dia ÷ 3/16 ins
Winding length ÷ 1/4 ins
Tap Ratio n ÷ 5