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Primitive Polynomials for Iterative Recursive Soft Sequential Acquisition of Concatenated Sequences

ABBAS AHMED, PANAGIOTIS BOTSINIS, (Member, IEEE), SEUNGHWAN WON, (Senior Member, IEEE), LIE-LIANG YANG, (Fellow, IEEE), AND LAJOS HANZO, (Fellow, IEEE)
University of Southampton, Southampton SO17 1BJ, U.K.

Corresponding author: Lajos Hanzo (lh@ecs.soton.ac.uk)

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ABSTRACT An iterative initial sequence acquisition technique is proposed for the pseudo-noise signal derived from a pair of *m*-sequences used for generating the concatenated sequence, which relies on the soft-in-soft-out detection to improve the acquisition performance. This recursive soft sequential estimation technique has a linearly increasing complexity with the number of chips in the concatenated sequence. Receiving as few as S consecutive chips of a $(2^S - 1)$-chip sequence is sufficient for the local concatenated-sequence generator of the receiver to synchronize. Hence, this initial synchronization technique is eminently suitable for long *m*-sequences and concatenated sequences. Another key result is the comparison of *m*-sequences and concatenated sequences regarding the acquisition time. It is also observed that low-order primitive polynomials (PPs) achieve better performances than higher-order polynomials for both the *m*-sequences and concatenated sequences. When considering PPs having a higher number of taps, the exploitation of concatenated sequences is capable of achieving in excess of 3-dB signal-to-noise ratio gains over *m*-sequences.

INDEX TERMS Recursive soft sequential estimation (RSSE), EXIT chart, acquisition time (AT), *m*-sequence, concatenated sequence, pseudo-noise (PN).

NOMENCLATURE

3GPP	3^{rd} Generation Partnership Project
5G	5^{th} Generation
AMI	Average Mutual Information
AT	Acquisition Time
AWGN	Additive White Gaussian Noise
BCH	Bose Chaudhuri Hocquengem
BER	Bit Error Ratio
BPSK	Binary Phase Shift Keying
BS	Base Station
CDMA-2000	Code Division Multiple Access-2000
dB	Decibel
DL	Downlink
DRSSE	Differential Recursive Soft Sequential Estimation
DS-CDMA	Direct Sequence Code Division Multiple Access
DS-UWB	Direct Sequence Ultra Wide Band
EXIT	EXtrinsic Information Transfer
FH	Frequency Hopping
I_A	*a priori* Information
I_E	Extrinsic Information
IS	Interim Standard
MI	Mutual Information
MS	Mobile Station
LFSR	Linear Feedback Shift Registers
LLRs	Log-Likelihood Ratios
P_e	Erroneous Loading Probability
PDAs	Personal Digital Assistants
PN	Pseudo-Noise
PPs	Primitive Polynomials
PTL	Phase-Tracking Loop
RASE	Rapid Acquisition Sequential Estimation
RF	Radio Frequency

DS-CDMA	Direct Sequence Code Division Multiple Access
SCR	Soft-Chip Register
SISO	Soft-In-Soft-Out
SNR	Signal to Noise Ratio
SS	Spread-Spectrum
TL	Tracking Loop
UWB	Ultra Wide Band

I. INTRODUCTION

The popularity of notepads, laptops, smart phones, gaming consoles, smart televisions and Personal Digital Assistants (PDAs)[1] has dramatically increased the tele-traffic [1], [2]. Efficient use of the transmit bandwidth plays a pivotal role in multi-media-centric environments [2–4]. Pseudo Noise (PN) sequence acquisition is the initial synchronization procedure of Spread-Spectrum (SS) communication systems [5–8]. Once initial synchronization has been established, symbol-synchronization may take place and the data can be demodulated [8], [9] either using coherent or non-coherent detection. Numerous different *m*-sequences have been used in both the Interim Standard (IS)-95 [8], [10] and in the Code Division Multiple Access-2000 (CDMA-2000) standards [10], [11]. The 3^{rd} Generation Partnership Project (3GPP) also opted for using *m*-sequences for initial acquisition in the 5^{th} Generation (5G) standards [12–16].

In the context of *m*-sequence acquisition, Ward [17] proposed a sequential estimation acquisition arrangement, where the correctly received *m*-sequence output by the acquisition mechanism was then loaded into the receiver's *m*-sequence generator [18], [19]. Explicitly, provided that the received Signal to Noise Ratio (SNR) is sufficiently high, the acquisition of an *m*-sequence having a period of $(2^R - 1)$ may be successfully concluded, once as few as R successive chips are perfectly recovered by the sequence acquisition device. These are then loaded into the *m*-sequence generator of the receiver. The sequence generator will produce chips that are identical to those generated by the transmitter [18], [20]. Naturally, some of the received chips might be corrupted by noise and interference, hence resulting in faulty loading of the *m*-sequence generator of the receiver with an Erroneous Loading Probability (P_e) [18], [20]. Ward [17] has demonstrated that for reasonable SNR values this technique leads to a shorter average initial Acquisition Time (AT) than the conventional sliding correlator-based initial acquisition technique [21]. However the received signal energy is typically distributed across hundreds or thousands of chips, hence the SNR per chip is extremely low. Moreover, hard decisions are typically unreliable for the estimation of R consecutive chips using a chip-by-chip-based approach [6], [8], [18], [20]. Hence, Kilgus [22] devised a majority logic aided decoder for *m*-sequence acquisition. As a further evolution of this kind of technique, Ward and Yiu [23] proposed the concept of recursive sequential estimation assisted acquisition. The basic principle of these two schemes was to adopt the hard decision approach relying on coherent detection. However, adopting any hard decision based coherent approach becomes unrealistic, since the SNR is usually very low prior to despreading [7], [9]. For this reason, we advocate the recursive Soft Input Soft Output (SISO) detection principle, which has its roots in the classic turbo channel decoding philosophy [18], [20], [24], [25]. Before delving into the new contributions of this paper we have summarized the evolution of the field in Fig. 1.

Against this background, our novel contributions are as follows:

- We introduce a new concatenated sequence acquisition concept.
- We propose the application of EXIT charts for visualizing the convergence behavior of the concatenated sequence aided synchronization. We demonstrate that the concatenated sequences produced by the low-order Primitive Polynomial (PP) relying on a low number of taps achieve higher MI than other PPs having more taps at a similar number of iterations. Our investigations verify that the convergence of our iterative acquisition scheme using high-order PPs is worse than that of low-order PPs.
- We demonstrate that low-order PPs have a lower P_e than their high-order counterparts. Among PPs of the same order having same number of feedback taps, PPs with higher-index taps perform best. Furthermore, PPs of the same order having non-consecutive feedback taps outperform those having consecutive feedback taps.
- We show that concatenated sequences attain a beneficial gain over *m*-sequences.
- We also demonstrate that concatenated sequences achieve a lower AT than *m*-sequences.

The outline of this paper is as follows: Section II illustrates the RSSE acquisition design. Section III illustrates the employment of EXIT charts. We provide our simulation results in Section IV, prior to our conclusions in Section V.

II. PROPOSED SYSTEM MODEL

Fig. 2 portrays our acquisition scheme, constituted by five major components namely: a) *m*-sequence generators, b) Concatenated sequence generator, c) SISO detector/decoder, d) Soft-Chip Register (SCR) and e) Phase-Tracking Loop (PTL). Prior to our discussion of these components, we investigate the RSSE acquisition technique. The two SCRs have the same structured delay units as those of the *m*-sequence generators of the transmitter. Their task is to store the instantaneous values of the consecutive chips in the form of their LLRs. The SISO detector/decoder calculates the related values of the soft LLRs after receiving each soft channel output. The SISO detector/decoder processes both the intrinsic information received from the channel plus the extrinsic information related to the same chip, depending mainly upon the previously processed LLR values gathered in the SCRs. An appealing feature of the RSSE is that it takes into account the reliabilities of all the successive chips

[1] All acronyms are summarized at a glance in Nomenclature

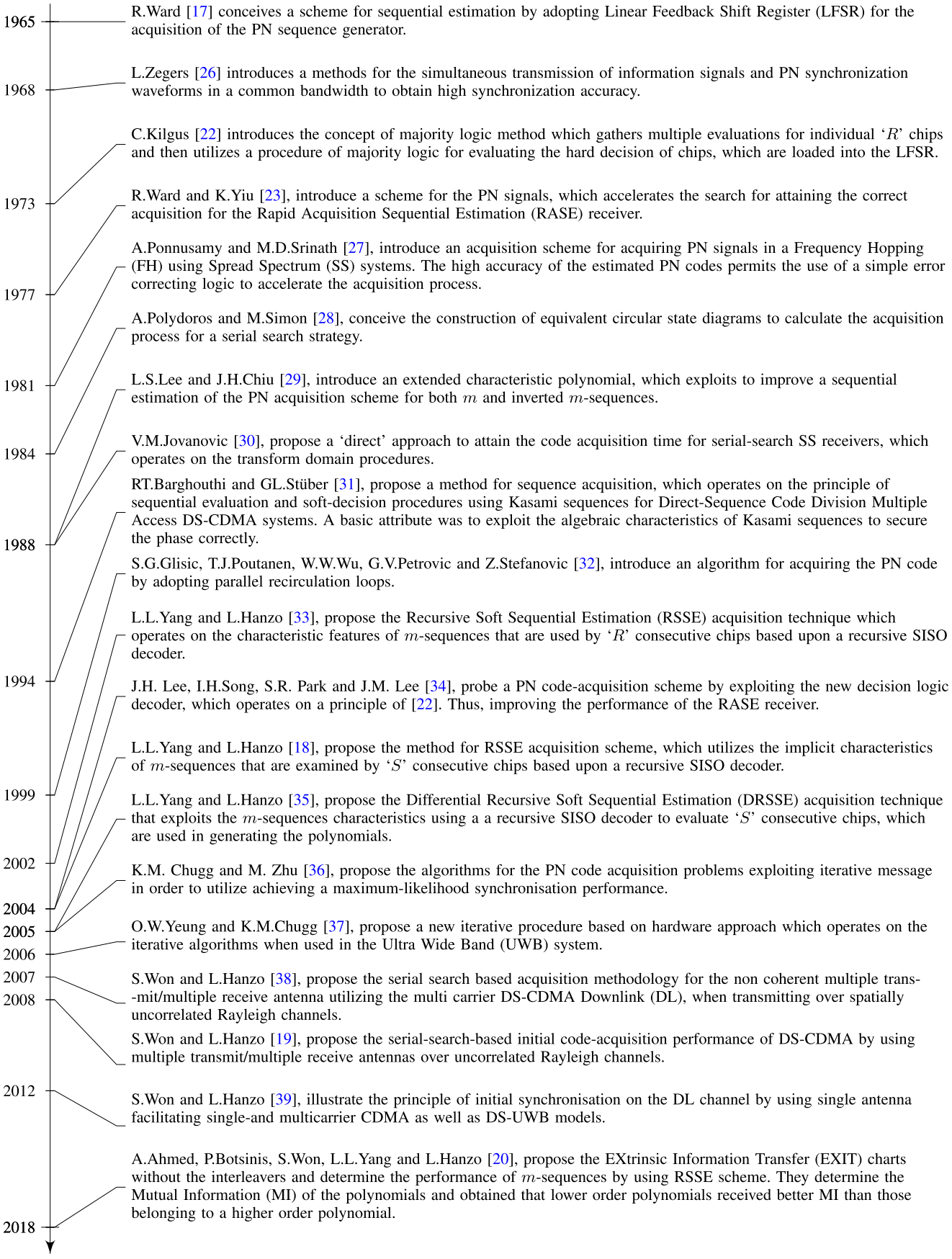

FIGURE 1. Timeline of initial acquisition for PN code sequence generator.

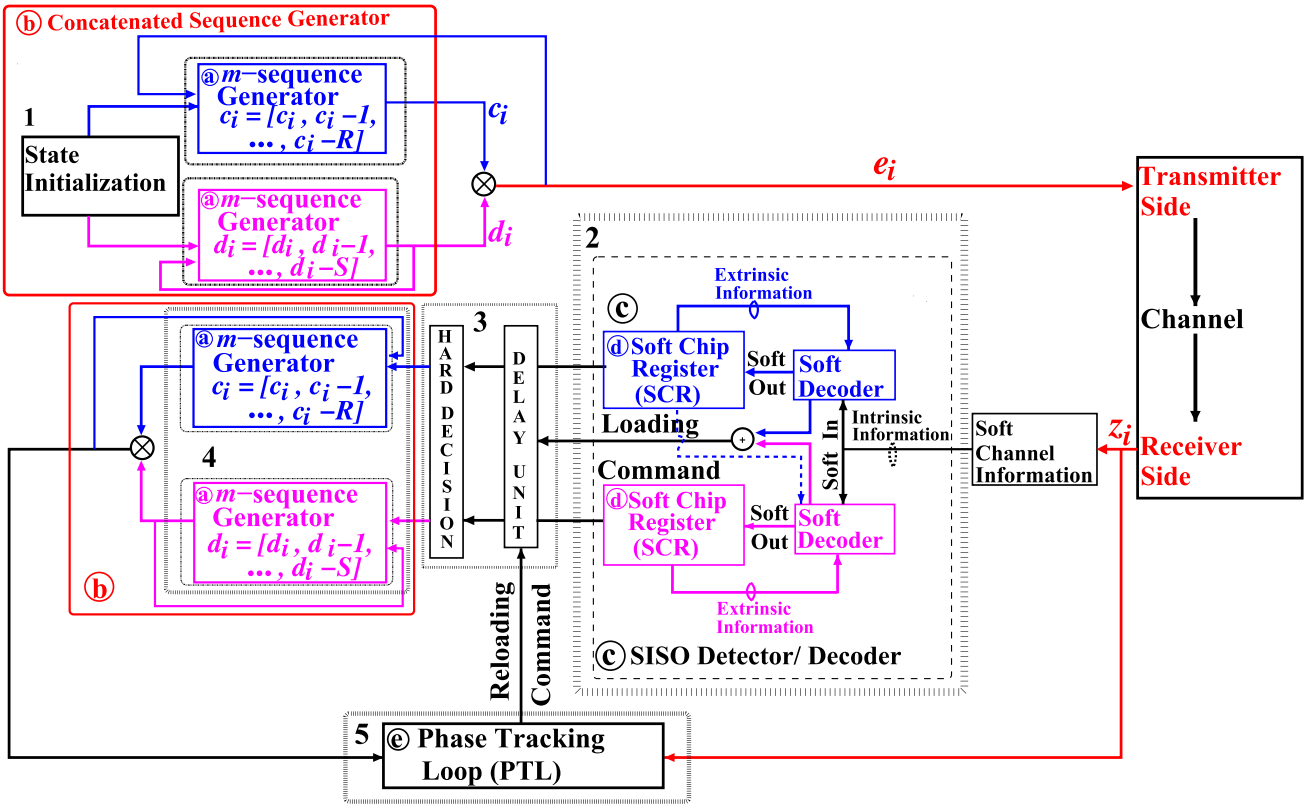

FIGURE 2. A schematic diagram of our proposed RSSE aided iterative acquisition scheme, where blue dotted line shows the information gathered from first SISO decoder to obtain the information for the second decoder, where the blue line represents the information about the SCR of c_i, which is used for calculating the soft information conveying d_i and in other words the values of one SCR at the receiver are utilized to calculate the *a priori* of the other shift register which is shown by blue dotted line.

by monitoring their LLRs. The basic steps of the RSSE are illustrated as follows:

1 At the transmitter side of Fig. 2, the pair of m-sequence generators are initialized and the transmitter sends the phase-coded carrier signal without any data modulation.[2] Both the transmitter and the receiver know the PPs and the chip values. If the receiver has exactly the same feedback for the two m-sequence generators as those of the transmitter side, then the corresponding chip values will be loaded into the appropriate registers of the two m-sequence generators.

2 The SISO detector / decoder receives a channel output sample z_i associated with the chip e_i, and then it evaluates the LLR of e_i based on z_i as well as it determines the extrinsic information. The data are then fed to the SCRs of Fig. 2, where the SCRs have the same number of taps as well as the connections as those of the two m-sequence generators at the transmitter. The most recent S and R chip values are stored in the SCRs of the SISO decoder, which are associated with S and R successive chips of the transmitted m-sequences, respectively. When the magnitudes of the most recent S and R soft outputs of the SISO detector become sufficiently high for ensuring a low P_e, a "loading command" is issued by the scheme of Fig. 2.

3 After that, S and R successive chips are calculated by using hard decisions, which is based on comparing the most recent S and R chips stored in the SCR at that instant of time to a threshold resulting in the binary value of either $+1$ or -1. After obtaining the hard decision result, the values are loaded into the corresponding delay units of the two m-sequence generators of Fig. 2.

4 As soon as the initial binary values are determined by a pair of m-sequence generators, the received signal is despread, provided that the initial chip values of the two m-sequence generators are correctly loaded.

5 The despread signal is transferred to the PTL of Fig. 2 to acquire the phase. When the phase is acquired correctly, the updated chips of S and R will be loaded into

[2]In the context of initial synchronization, the m-sequences are utilized for aiding synchronization between the Mobile Station (MS) and the Base Station (BS). They have been specifically selected as a benefit of their cyclic nature. Explicitly, during code acquisition, the receiver becomes capable of locking on to the correct stage of each shift register after as few as R or S chip transmissions, despite transmitting m-sequences of length (2^R-1) or (2^S-1). Our DL transmission is initiated by transmitting an unmodulated pilot signal over the pilot channel. The pilot channel provides a reference signal for all the MSs within a cell, which is always transmitted by the BS [7], [11], [40]. Typically it is about 4-6 *dB* stronger than the power of all other channels. The pilot channel uses the all-zero Walsh code and contains no information except for the RF carrier in the IS-95. Therefore, the pilot signal is an unmodulated spread spectrum signal because it is multiplied by an all-zero Walsh code, which is then spread according to the chip rate of the sequence [40], [41]. No data modulation is performed during this part of the transmission, as mentioned in [18–20].

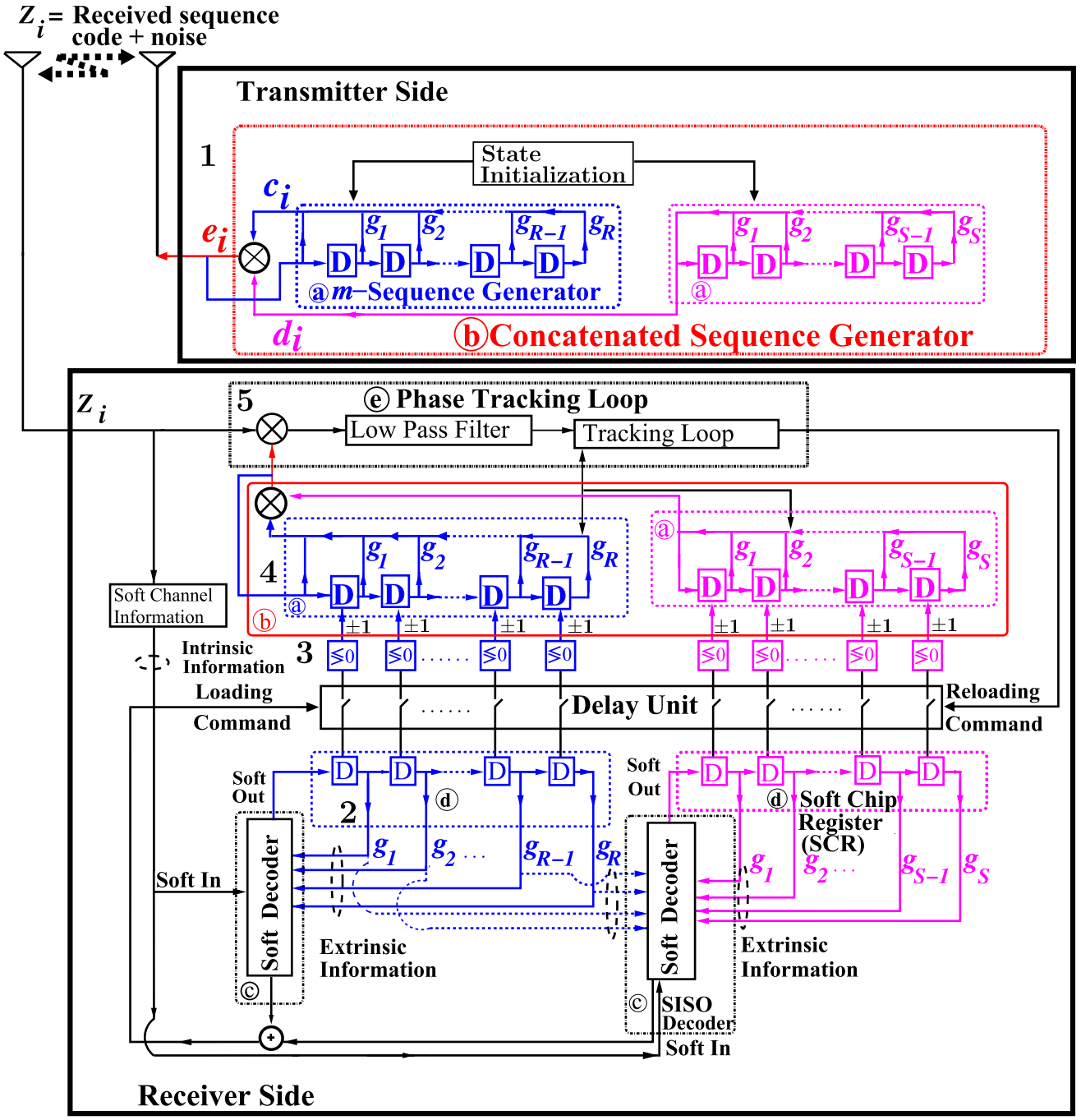

FIGURE 3. RSSE aided iterative acquisition model, where R and S have the same polynomial order, whilst c_i and d_i are the chips concerned, where the blue dotted line represents the information about the SCR of c_i, which is used for calculating the soft information conveying d_i.

the delay units of Fig. 2. By contrast, if the phase is not acquired correctly, then the PTL will be triggered to activate the "reloading command". This procedure will be repeated until the correct code is found by the PTL. In other words, the task of PTL is to retrieve a signal received over the noisy channel and to produce a secure output so that the received and transmitted signals are perfectly aligned.

Let us now discuss all the blocks of the proposed RSSE technique in detail by relying on Fig. 3.

A. m-SEQUENCE GENERATOR

Let us commence by discussing this processing block marked as ⓐ in Figs. 2 and 3. These m-sequences belong to the family of maximum length sequences [5], [7], [42], produced by LFSR. The LFSR connection polynomial uniquely describes

the sequence generator [7], [43]. In Fig. 3, the unit time delay is represented by 'D' and g_1, g_2, ..., g_R denotes the absence or presence of the connections. Explicitly, a connection being present is represented by 1, while the connection being absent is represented by 0. The generator polynomial is expressed as:

$$g(D) = 1 + D^{r_1} + D^{r_2} + \ldots + D^{r_M=R}, \tag{1}$$

where $g(D)$ is a PP, therefore it cannot be factorized [18], [44] and the r_1, r_2 ... are the index set corresponding to the feedback tap connections of the concerned PP used in generating the m-sequences concerned. According to Fig. 3, the m-sequence can be generated by the following recursion

$$c_i = c_{i-r_1} c_{i-r_2} \ldots \; c_{i-(r_M=R)} = \prod_{m=1}^{M} c_{i-r_m}, \text{ for } i = 0, 1, \ldots, I. \tag{2}$$

where c_i denotes the chip-values of the m-sequence having output values of $\{+1, -1\}$ respectively, since SS communication systems usually employ binary spreading sequences having chip values of $\{+1, -1\}$. In this contribution we assume that the m-sequence generator outputs duo-binary $\{+1, -1\}$ symbols,[3] representing a logical zero by $+1$, while the product operation is denoted by $\prod(\cdot)$. In the scenario of our iterative calculation-based acquisition method of Fig. 3 utilized for m-sequences, the generator's state can be calculated by iterative detection schemes, where each m-sequence generated by an 'R'-stage shift register having a length of $(2^R - 1)$ chips is represented by a cyclic Bose Chaudhuri Hocquengem (BCH) code of length $(2^R - 1)$, having a displacement of $(2^R - 1)$ [22]. Consequently, after the receiver has obtained $[2 \times (2^R - 1)]$ successive patterns of the m-sequence generated, the first stage of R chips is calculated for the m-sequence generator by iteratively detecting the m-sequence obtained with the help of its tap connections. Note that a pair of m-sequence generators and the SCRs of Fig. 3 have the same feedback elements. Moreover, the feedback branches are duo-binary in the m-sequence generator and the results obtained from these branches are utilized for producing a binary feedback flag.

B. CONCATENATED SEQUENCES

Let us now turn our attention to processing the block marked as ⓑ in Figs. 2 and 3. Concatenated sequences are widely used in wireless communication as these sequences are derived from two PPs, having similar cross correlation and auto-correlations properties to those of the Gold codes and of long PN-sequences [45–49]. A pair of m-sequence generators are used for generating the concatenated sequence by XORing or performing modulo-2 addition of the appropriately shifted versions of the two m-sequences created by two different PPs having the length of $2^R - 1$ and $2^S - 1$ respectively, as shown in Fig. 3. In this paper we assume R = S, so that the generated concatenated sequences has the properties as the Gold sequence. These PPs cannot be factorized and they obey:

$$\begin{aligned} c_i &= c_{i-r_1} c_{i-r_2} \ldots c_{i-(r_M=R)} \\ &= \prod_{m=1}^{M} c_{i-r_m} \text{ for } m = 0, 1, \ldots, M, \\ &\qquad i = 0, 1, \ldots, I, \end{aligned} \tag{3}$$

$$\begin{aligned} d_i &= d_{i-s_1} d_{i-s_2} \ldots d_{i-(s_N=S)} \\ &= \prod_{n=1}^{N} d_{i-s_n} \text{ for } n = 0, 1, \ldots, N, \\ &\qquad i = 0, 1, \ldots, I, \end{aligned} \tag{4}$$

where c_i and d_i of Fig. 3 represent the chip values of the two m-sequences used for generating the concatenated sequence, respectively.[4] Eqs. (3) and (4) can be combined as follows:

$$\begin{aligned} e_i &= c_i \cdot d_i \\ &= \prod_{m=1}^{M} c_{i-r_m} \cdot \prod_{n=1}^{N} d_{i-s_n} \quad \text{for } i = 0, 1, \ldots, I, \end{aligned} \tag{5}$$

where e_i is the resultant output of two m-sequence generators, i.e, the chip values of the concatenated sequence.

C. SOFT CHIP REGISTER AND SISO DECODER

We now continue our discourse by discussing the processing block marked as ⓒ in Figs. 2 and 3. In Fig. 3 the SCRs have R and S number of delay-units. The number of SCRs is identical to that of the delay units in a pair of m-sequence generators. Furthermore, the two SCRs rely on the same feedback connections as those of the transmitter side, because the PPs are known to both the receiver and to the transmitter. The chip-LLR values of the R and S successive chips are stored and shifted by the SCR. Again, at the first iteration the likelihood of having a '1' or '0' chip is identical, hence the LLRs are set to zero [18], [20]. As portrayed in Fig. 3, the LLRs of these R and S chips will be used to obtain the hard decisions of the successive chips that are then loaded into the pair of m-sequence generators. The SISO decoder utilizes the previous LLRs computed by the SCR as the *a priori* information [18], [20]. The information gleaned at the output of the channel for a specific chip is referred to as intrinsic information, which is calculated by the SISO decoder. The soft output of the SISO decoder of Fig. 3 is then entered at the left-most location of the SCR, while the right-most SCR's value

[3]Please note that c_i over here will be feed to the channel when exploit the RSSE scheme of [18] and [20] to obtain synchronization for m-sequence.

[4]The chip-values of the two m-sequence have output values of $\{-1, +1\}$ respectively. The information about the chip d_i can be obtained by taking the information about e_i plus the information obtained by the corresponding chip c_i of the first SISO decoder because both sequences are used for producing the concatenated sequence. Therefore by performing the modulo-2 addition or XORing we generate a concatenated sequence, as shown in Figs. 2 and 3. Hence for calculating the soft information d_i we have to obtain the information from the e_i and also from the chips of the other m-sequence's decoder. This is because the values of the one of the m-sequences SCR at the receiver are utilized to calculate the *a priori* of the other shift register.

is removed [18], [20]. At the last iteration we observe the maximum values of our two SISO decoders as seen in Fig. 3, and then a "loading command" is triggered,[5] provided that the soft outputs of the SISO decoders become sufficiently high for ensuring a low P_e. The corresponding chips are evaluated by applying hard decisions to the most recent values of the LLR, which are stored in the SCR. Finally, after the hard-decisions the resultant binary chips are entered into the related shift registers of the two m-sequence generators of the receiver of Fig. 3.

D. SOFT CHANNEL OUTPUTS

Focusing our attention on the block marked as ⓓ in Figs. 2 and 3, the chip e_i is related to the received signal as

$$z_i = \alpha_i e_i + n_i, \quad i = 0, 1, \ldots, \tag{6}$$

where n_i is the Additive White Gaussian Noise (AWGN) having a zero mean, N_0 is the noise power spectral density and α_i is the channel state. Given z_i, the LLR of e_i is expressed as

$$\begin{aligned} L_{ex}(e_i) &= L(e_i|z_i) = \log\left[\frac{P(e_i = +1|z_i)}{P(e_i = -1|z_i)}\right] \\ &= L_e z_i + L(e_i), \quad i = 0, 1, \ldots, \end{aligned} \tag{7}$$

where $L_e = 4\alpha_i \frac{E_c}{N_0}$, the energy per chip is E_c and $L_e(e_i) = 0$, since we assume that the chip's value e_i is binary and equiprobable. Observe from Eq.(5) and Fig. 3 that the soft outputs of the SISO decoder are calculated at the time instants of $(i - r_1), (i - r_2), (i - r_3), \cdots, (i - r_M)$, as well as $(i - s_1), (i - s_2), (i - s_3), \cdots, (i - s_N)$ and then fed into the SISO decoder. These outputs constitute the *a priori* inputs of $(c_{i-r_1}), (c_{i-r_2}), (c_{i-r_3}), \cdots, (c_{i-r_M})$, and $(d_{i-s_1}), (d_{i-s_2}), (d_{i-s_3}), \cdots, (d_{i-s_N})$. Then, the extrinsic information calculated at its output is used for correctly detecting the chip e_i with a high probability. Assuming that the previous R and S number of soft outputs of the SISO decoder are denoted by $L_{ex}(e_{i,-1}), L_{ex}(e_{i,-2}), \ldots, L_{ex}(e_{i,-R})$ and $L_{ex}(e_{i,-S})$. As opposed to the *a priori* LLRs of traditional EXIT charts [50–52], in our model the magnitude of the *a priori* LLR of the i^{th} chip is equal to the least confident LLR value of the previous chip that was utilized for generating a concatenated sequence. Hence, the procedure of evaluating the *a priori* LLR of the i^{th} chip $L_{apr}(e_i)$ is represented as [8], [18–20], [52].

$$\begin{aligned} L_e(e_i) = L_{apr}(e_i) \approx \Bigg[\prod_{m=1}^{M} \text{sign}(L_{ex}(e_i - r_m)) \\ \cdot \prod_{n=1}^{N} \text{sign}(L_{ex}(e_i - s_n))\Bigg] \times \left[\min\left\{|L(e_{i-r_1})|\right\},\right. \\ \left\{|L(e_{i-r_2})|\right\}, \ldots, \left\{|L(e_{i-r_M})|\right\} \\ \left\{|L(e_{i-s_1})|\right\}, \left\{|L(e_{i-s_2})|\right\}, \ldots, \\ \left.\left\{|L(e_{i-s_N})|\right\}\right] \quad i = 0, 1, \ldots, I, \end{aligned} \tag{8}$$

where we assume that $L_{apr}(e_{-\infty}) = \ldots = L_{apr}(e_{1-r}) = L_{apr}(e_{-2}) = L_{apr}(e_{-1}) = 0$ and $L_{apr}(e_{-\infty}) = \ldots = L_{apr}(e_{1-s}) = L_{apr}(e_{-2}) = L_{apr}(e_{-1}) = 0$. Finally, the channel's output information $L(e_i|z_i)$ in Eq.(7) and the *a priori* information $L_{apr}(e_i)$ in Eq.(8) will yield the soft output of the SISO decoder related to the chip e_{out} as

$$\begin{aligned} L(e_{out}) &= L_{ex}(e_i) = L(e_i|z_i) + L_e(e_i) \\ &= L_e z_i + L(e_i) + \Bigg[\prod_{m=1}^{M} \text{sign}(L_{ex}(e_i - r_m) \\ &\quad \prod_{n=1}^{N} \text{sign}(L_{ex}(e_i - s_n))\Bigg] \times \left[\min\left\{|L(e_{i-r_1})|\right\},\right. \\ &\quad \left\{|L(e_{i-r_2})|\right\}, \ldots, \left\{|L(e_{i-r_M})|\right\} \\ &\quad \left\{|L(e_{i-s_1})|\right\}, \left\{|L(e_{i-s_2})|\right\}, \ldots, \\ &\quad \left.\left\{|L(e_{i-s_N})|\right\}\right] \quad i = 0, 1, \ldots, I. \end{aligned} \tag{9}$$

Note that Eq.(9) represents the recursive relationship used for evaluating the consecutive chips required by a pair of m-sequence generators in order to produce the concatenated sequence. Thus, the acquisition device becomes more confident in correctly deciding the R and S consecutive chips from the magnitudes of the LLR in the SCRs of Fig. 3. When the SISO detector attains a channel output sample z_i linked to the chip e_i, it calculates the LLR utilizing Eqs.(8) and (9) for estimating the intrinsic information.

1) ALGORITHM USED FOR ACQUIRING THE SYNCHRONIZATION OF THE CONCATENATED SEQUENCE

The followings are the basic steps involved in acquiring the concatenated sequence as shown in Fig 4.

- Step 1: Generate two m-sequences having the same length of $2^R - 1$ and $2^S - 1$, where R and S are the same polynomial orders [46–48], [53], [54]. These two m-sequences have $+1$ and -1 values. As an example generated PPs are $g_{c_i}(D) = 1 + D^2 + D^5$ and $g_{d_i}(D) = 1 + D^3 + D^5$. We will use this example for further clarification throughout this algorithm.
- Step 2: As shown in Figs. 2, 3 and 4, we XOR c_i and d_i to obtain e_i, where e_i is mapped to $+1$ or -1, respectively as shown in Eq. 5.
- Step 3: After transmitting e_i over an AWGN channel, we obtain z_i as shown in Eq. 6.
- Step 4: z_i is fed to both soft decoders of Figs. 2 and 3, where SCR values are initialized to zero as the probability of zeros and ones will be the same.
- Step 5: After some iteration between the soft decoders and the SCRs of Figs. 2 and 3, we obtain the LLRs values by calculating Eq. 8. The $D(0), D(2), C(0)$ and $C(3)$ are the concerned taps involved in generating the PPs of two m-sequence to obtain concatenated sequence

[5]When the magnitudes of the LLR values in the SCR become sufficiently high after a set of iterations, then the SISO detector carries out hard decisions to generate the binary values -1 or $+1$ of the chip, which are loaded into the two m-sequence generators at the receiver. Let us assume that we carry out the i^{th} iteration, with $i = 1, \ldots, I$ and the number of extrinsic LLRs to be evaluated is S and R, thus the values calculated in the LFSR are updated at the receiver. During each iteration S and R chips have to be transmitted. Thus after I iterations the total number of received chips will be $I \cdot R$ or $I \cdot S$, where R and S have the same polynomial order.

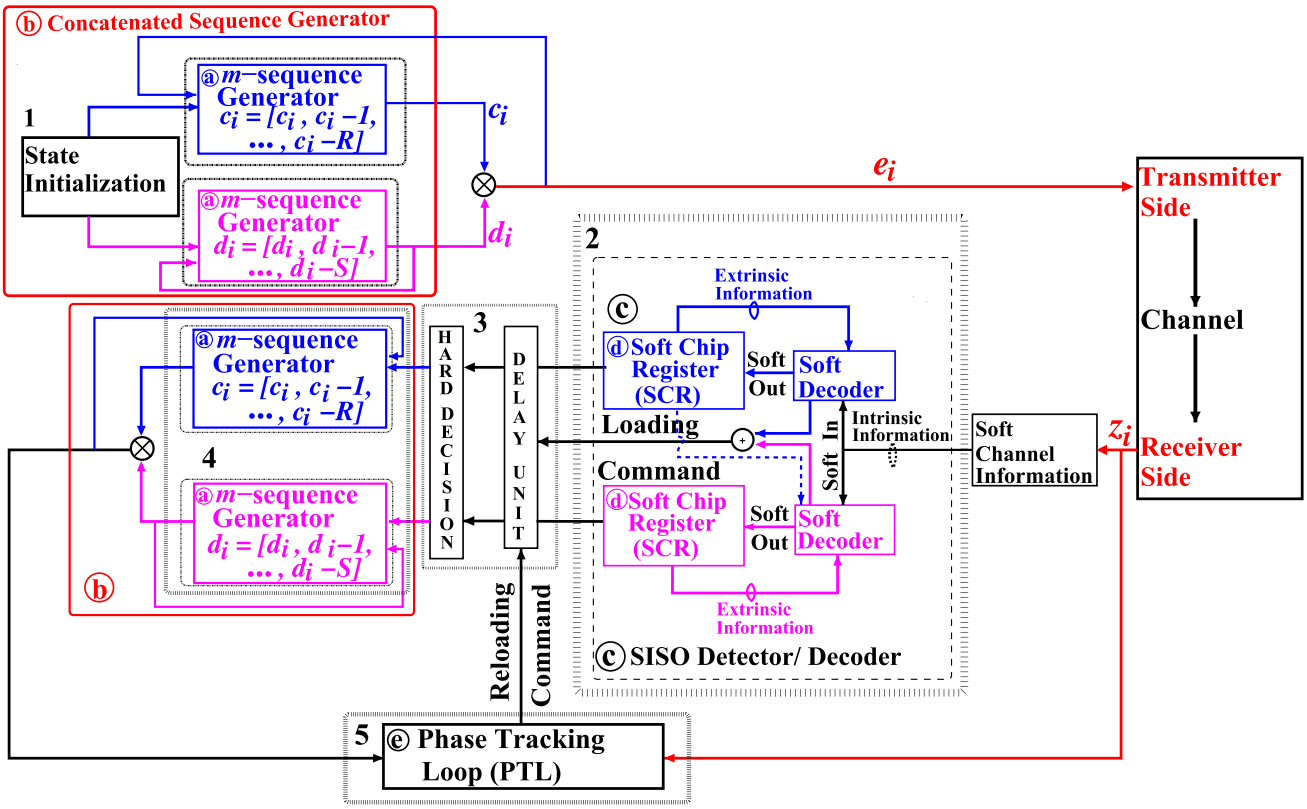

FIGURE 4. Flow chart of our proposed algorithm for obtaining the concatenated sequence.

as shown in our proposed algorithm in Fig. 4. Fig. 4 manifests that for evaluating the soft information about d_i which is the other SISO decoder, we need to exploit the concerned taps of the first m-sequence generator, i.e. c_i. These tap values are $C(0)$ and $C(3)$ for the c_i value given above. As a result, the values of the first m-sequence SCR are utilized to calculate the *a priori* of the other shift register to decode the transmitted value of d_i at the receiver.

- Step 6: After obtaining the desired values, the loading command is activated by the SISO decoders, which helps to retrieve the data from the delay unit to perform hard decision as shown in Fig. 4.
- Step 7: After gaining the information from the hard decision, the values 1 or 0 are processed to the LFSRs of the two m-sequence generator of Figs. 2 and 3. The output of these m-sequences are again XORed together.
- Step 8: The value calculated in Step 7 is compared with the value of z_i by the PTL, if these values match, then the synchronization is achieved by our purposed system.
- Step 9: If there is decoding error, then PTL will restart the command "reloading command", which means we need to go back to Step 5, where the two m-sequences will have distinguished values in the delay units of the two m-sequence generators and the process will repeated again until the correct code is achieved.

E. PHASE TRACKING LOOP

Finally, we discussed block marked as ⓔ in Figs. 2 and 3. Prior to despreading, the chip-SNR is typically too low for attaining accurate carrier phase tracking [55], [56]. The despread signal is then entered into the low-pass filter of Fig. 3. Following this, the information is forwarded to the Tracking Loop (TL) of Fig. 3. If the initial phase is determined accurately by the TL, then payload data reception may commence.[6] This procedure is repeated until correct code acquisition is accomplished.

III. EXIT CHART ANALYSIS FOR *m*-SEQUENCE DESIGN

Ten Brink introduced the principles of EXIT charts [50], [51] as an accurate mechanism of predicting the convergence characteristics of iteratively decoded techniques. They are capable of estimating the specific SNR value at which an infinitesimally low Bit Error Ratio (BER) can be achieved instead of conducting time-consuming bit-by-bit detection based Monte-Carlo simulations. To elaborate a little further, accurate EXIT chart techniques rely on the condition that the inputs of two SISO components of an iterative receiver have a Gaussian distribution, which can only be approached using a sufficiently long interleaver. Since this is not the case

[6] If not, the TL will activate the reloading command, where the two m-sequences will have distinguished values in the delay units of the two m-sequence generators.

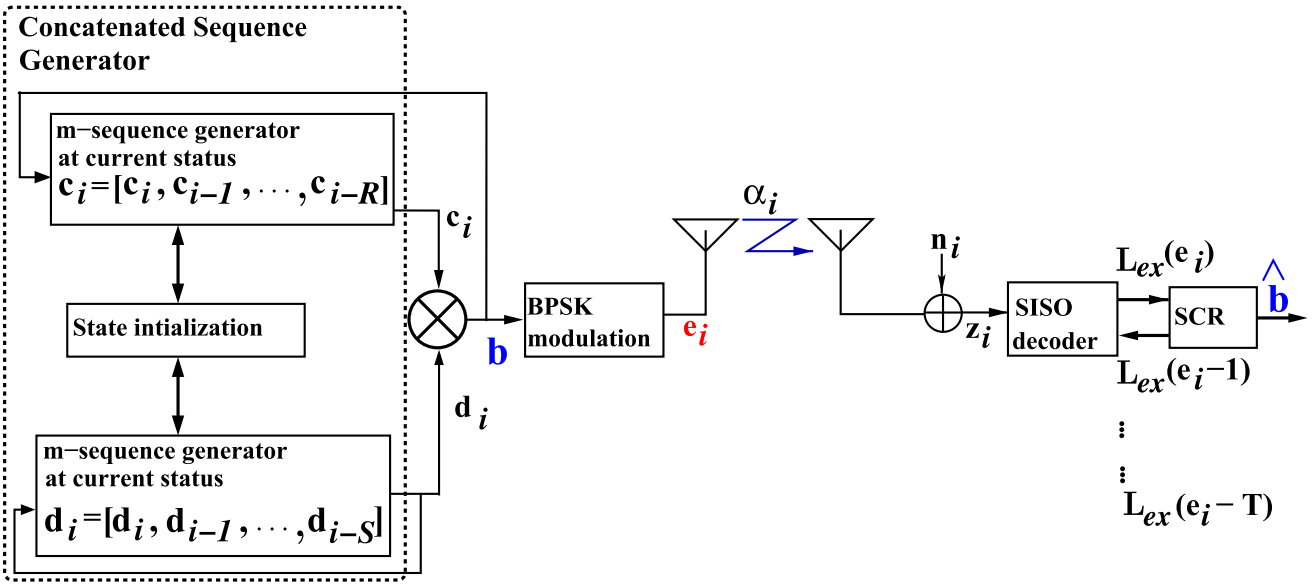

FIGURE 5. The system model used for the RSSE scheme of Fig. 3.

for our initial acquisition scheme, a bespoke EXIT-chart has to be conceived. Hence we introduce a novel EXIT chart design for predicting the convergence characteristics of our RSSE scheme utilized for investigating the evolution of the input/output Mutual Information (MI) transfer among the receiver's SISO components in successive iterations. In a traditional EXIT chart there are three components, namely the inner detector's MI-curve, the outer detector's MI-curve and the stair-case-shaped iterative detector trajectories based on a specific instance of iterative detection. More explicitly, the stair-case-shaped detection trajectory visualizes how much extra MI improvement is achieved during each iteration. This can be readily arranged, provided that interleavers are used between the inner and outer components. However, in contrast to the conventional EXIT chart [50], the same detector is operated repeatedly in our 'self-concatenated' approach, where the output of the acquisition scheme is used as its inputs in the next iteration, as portrayed in Fig. 5. More explicitly, Fig. 5 illustrates the two inputs of the SISO detector, namely the channel output and the SCR output of Fig. 3. Hence the inner and the outer decoders' EXIT curves are the same. However, they are mirrored with regard to the diagonal $x = y$ of the EXIT curves, as shown in Fig. 6, where the Extrinsic Information (I_E) / *a priori* Information (I_A) is plotted against the intrinsic or *a priori* Information (I_A) / the Extrinsic Information (I_E), when the SNR is fixed to -2 *dB*. Fig. 6 also reveals that the polynomial $g_2(D) = 1 + D^3 + D^5$ requires 5 to 6 decoding iterations to reach the [1,1] point. Furthermore, the trajectory of $g_2(D)$ approximately matches the inner and outer curves represented by red solid lines. Again, the inner and outer curves are the same and have a mirror image with regard to the diagonal line $x = y$ of the EXIT curves.

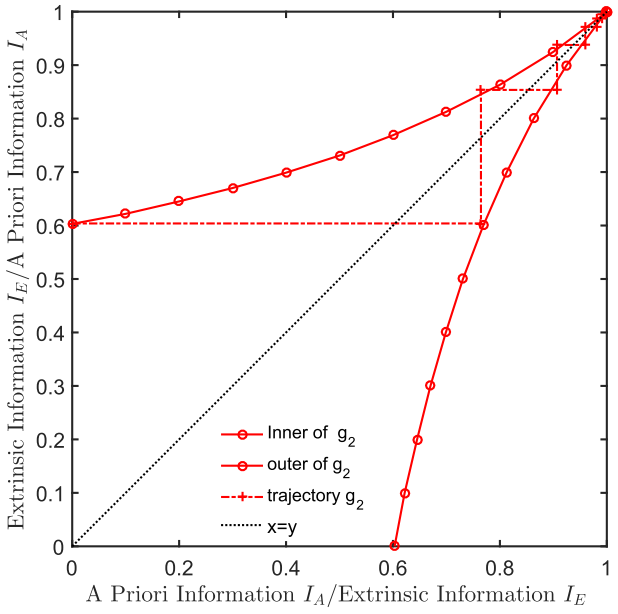

FIGURE 6. EXIT chart of $g_2(D) = 1 + D^3 + D^5$ over AWGN channels at SNR $= -2dB$.

Below we examine the theoretical resemblance between the self-concatenated detection design of [57] and our existing initial acquisition problem. However, there is also a significant dissimilarity between them, since in [57] an interleaver was adopted for changing the detector's output before passing it back to its input. As opposed to this, we introduce the new concept of using EXIT charts without any interleavers. We arrange this by the online exploitation of the inherent correlation between the chips in the two *m*-sequence generators, as enforced by the LFSRs of Fig. 5 instead of

invoking any iterations for decoding similar bit sequences. This is the main aspect which differentiate it from the traditional EXIT chart.

The SISO decoder's output will be modified according to the *a priori* LLR values L_{ex}, which in turn, contains the extrinsic LLR values of the preceding iteration at the receiver of Fig. 5. Binary Phase Shift Keying (BPSK) is employed, the value e_i of the i^{th} generated chip also becomes the value of the first LFSR stage in the two m-sequence generators. As illustrated in Fig. 5, during reception the signal obtained by the SCR is fed back to the SISO decoder in form of the extrinsic LLR values $L_{ex}(e_{i-1}), \ldots, L_{ex}(e_{i-(T=R=S)})$ that were gathered during the most recent I detection iterations, which were estimated for the T earlier generated chips. Based on these previous extrinsic LLRs, the *a priori* LLR of E_i is calculated from Eq.8. Later, the extrinsic LLR of e_i is evaluated from Eq.9 and the same method is also used for the subsequent chip e_{i+1}. Again, the task of the SCR in Fig. 5 is to store the most recent T extrinsic LLRs and to shift them by one position. Once a detection iteration[7] has been carried out, a hard decision is invoked and the most recent estimate of the generator's concatenated sequence $\hat{\boldsymbol{b}}$ becomes available.

A. SELF-CONCATENATED APPROACH

In the self-concatenated approach of [51] and [57], the same detector/decoder component is used twice, namely once as the inner SISO component and once as the outer SISO component, as shown in Fig. 5. The SISO detector has two inputs, namely the output of the two m-sequence generators and the channel's output. The LLR $L_e(e_i)$ is determined by the SISO detector. Note that the receiver utilizes the information of the two m-sequence generators, related to the time instant of determining the *a priori* LLR values. Thus, the information in the LFSRs of the two m-sequence generators will be shuffled during each SISO iteration, therefore we have to store the previous values of $\hat{\boldsymbol{b}}$, which are constituted by the $(2^R - 1)$ and $(2^S - 1)$ values of the two m-sequence generators having the same length. Again, for the sake of avoiding any acquisition delay, we do not employ any interleaver in our self-concatenated system represented by Fig. 5. This is the specific feature that differentiates our approach from the traditional EXIT charts [50]. Therefore, we may observe a conceptual similarity with the self-concatenated decoding approach of [51] and [52]. Again, our basic EXIT chart model relies on Fig. 5, where there is a single detector processing different inputs during its two operating phases. The channel's output is used as the initial input of the SISO decoder. The SCR's output in Fig. 5 is the second input of the SISO detector, which shifts the extrinsic LLR sequence, hence its action is reminiscent of the basic role of an interleaver in a traditional iterative receiver. Hence, the SISO detector computes $L_e(e_i)$ based on Eq.(8).

[7]Each iteration refers to the exchange of information between the SISO decoder and the SCR of Fig. 5 where the iteration depends upon two factors, namely on the number of chip received and on the polynomial order.

B. MUTUAL INFORMATION

In this scenario, we opted for time-averaging in order to determine the MI between the associated extrinsic LLRs and the chips generated [20], [50], [51].

IV. SIMULATION RESULTS

In this section the polynomial orders of 5, 6, 13, 15 and 23 are selected, because these sets are extensively used in wireless communication [18–20], [36], [58], [59]. Among the PPs having similar orders, we opt for the PPs having the best P_e versus SNR performance. This section is divided into the following five subsections. Section IV-A deals with the performance of the m-sequence. Section IV-B quantifies the performance of the Concatenated sequence, while in Section IV-C our P_e versus SNR performance comparisons of the m- and Concatenated sequences are provided. Finally, in Section IV-D the AT is evaluated, while Section IV-E deals with the EXIT chart analysis of both the m- and concatenated sequences.

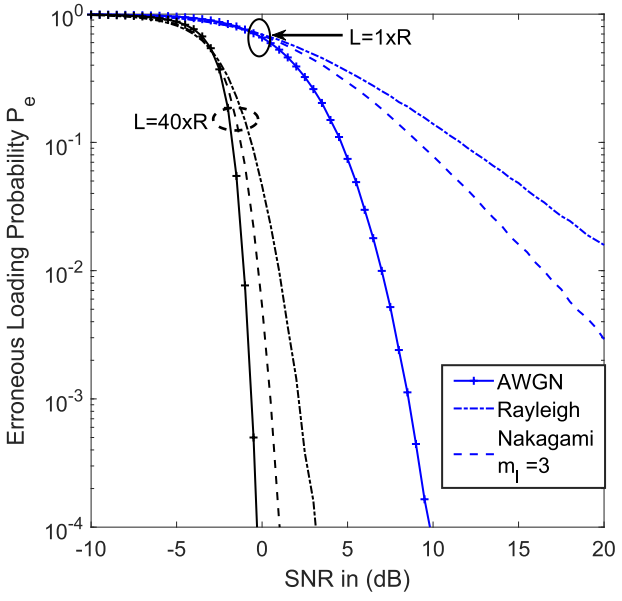

FIGURE 7. Performance comparisons between three different communication channels.

Fig. 7 depicts the performances of the PP $g_5(D) = 1 + D + D^3 + D^4 + D^{13}$ having a period of $N = 2^{13} - 1 = 8191$ chips produced by a 13^{th}- order polynomial. The affordable number of iterations is $L = (40 \times R)$, where L is the total number of chips that the SISO decoder processes and R denotes the number of chips corresponding to the PP's order. In Fig. 7, the acquisition performance of the RSSE technique is evaluated for transmission over three different communication channels. It can be concluded that reliable acquisition is achieved above an SNR value of -0.5 dB by entering $40 \times 13 = 520$ chips into the SISO detector, when transmitting through an AWGN channel. It is also inferred that for a given SNR value, P_e decreases upon increasing the number of received chips entered into the SISO detector. Fig. 7 illustrates that for a given number of received chips

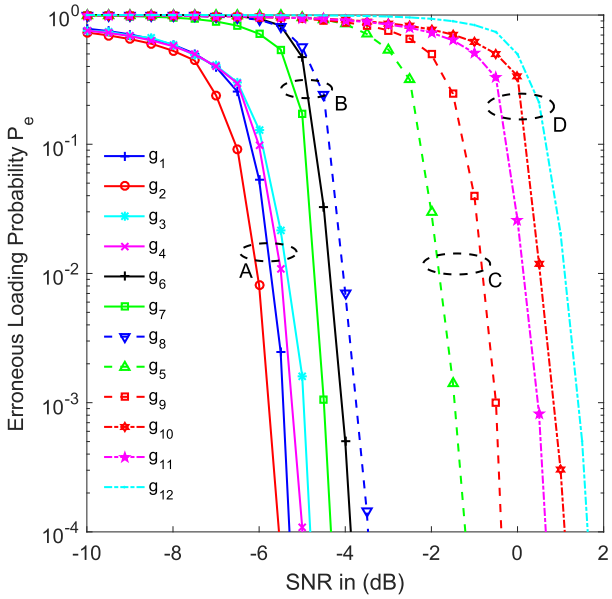

FIGURE 8. Performance comparisons between Primitive Polynomials (PPs) having three and more feedback taps, where A, B, C and D represent groups of PPs showing similar performance of *m*-sequences.

input into the SISO detector, the SNR gain attained for an AWGN channel is significantly lower than those under a Nakagami channel having $m_l = 3$ as well as under a Rayleigh channel. Naturally, our RSSE scheme attains a lower P_e for an AWGN than for fading channels. To limit the paper's length, only an AWGN channel is considered for our further simulations.

TABLE 1. Primitive polynomials (PPs) invoked for our RSSE scheme, where g_{12} has consecutive feedback taps ranging from 2 to 15.

Groups	Polynomials	Representation of polynomials
A	$g_1(D)$, $g_2(D)$	$(0, 2, 5)$, $(0, 3, 5)$
	$g_3(D)$, $g_4(D)$	$(0, 1, 6)$, $(0, 5, 6)$
B	$g_6(D)$, $g_7(D)$	$(0, 1, 15)$, $(0, 4, 15)$
	$g_8(D)$,	$(0, 5, 23)$,
C	$g_5(D)$, $g_9(D)$	$(0, 1, 3, 4, 13)$, $(0, 5, 11, 17, 23)$
D	$g_{10}(D)$	$(0, 2, 3, 5, 6, 7, 8, 9, 10, 11, 13)$
	$g_{11}(D)$	$(0, 1, 2, 3, 4, 5, 6, 8, 10, 12, 13)$
	$g_{12}(D)$	$(0, 2, 3, \ldots, 15)$

A. PERFORMANCE RESULTS FOR m-SEQUENCES

Table 1 describes the PPs used for constructing the *m*-sequences. The affordable number of iterations is $L = (200 \times R)$, and the total length of the *m*-sequence is $(2^R - 1)$. Our P_e versus SNR comparisons are recorded for various PPs, as depicted in Fig. 8, where the groups A, B, C and D are created by grouping the curves according to their P_e versus SNR performance. In group A, we have four PPs, namely (g_1, g_2) and (g_3, g_4) having orders of 5 and 6, respectively. The PP g_2 has a better performance than g_1, since its second feedback tap is connected to the third position of the entire feedback tap arrangement (tap 3), whereas in g_1 the second feedback tap is linked to the second position (tap 2), as described in Table 1. It is observed that PPs g_3 and g_4 have consecutive taps, where g_3 performs worse, because its consecutive taps are at lower connection indices of 0 and 1 (taps 0 and 1), whereas the consecutive taps of g_4 are located at higher connection indices of 5 and 6 (taps 5 and 6). More explicitly, g_2 has the best performance because it belongs to a lower-order PP and its second feedback tap is connected to a higher index than the second tap of g_1. The minimum of the LLR values of all the tap connections are used to generate the extrinsic information. For this reason, the transmitted PP using a low number of tap connections associated with the higher indices has a higher likelihood of giving the exact extrinsic information for the SISO acquisition design, than that of utilizing a high number of tap connections. In group B, we have three PPs, namely g_6, g_7 and g_8 as portrayed in Table 1, where g_6 and g_7 have the order of 15. Here, g_7 performs better than g_6, since the former does not contain any consecutive feedback taps. In g_6 consecutive feedback taps are present at indices 0 and 1 (taps 0 and 1). Since these consecutive taps act as a switch and during normal operation they may become contaminated by the noise, the performance of g_6 is worse than that of g_7. Furthermore, g_8 has a PP order of 23, as depicted in Table 1, hence it has a worse performance as compared to g_6 and g_7. When comparing the PPs of different order, PPs having higher order exhibit a longer memory requirement and they exhibit excessive confidence in their own soft approximations. Therefore, they do not benefit sufficiently from the extrinsic information provided by the iterative scheme. It also transpires from Fig. 8 that if the taps are non-consecutive and the PP's order is lower, the SNR required for achieving a given P_e will be lower, especially for lower-order PPs, since less taps become less contaminated by noise than those having a higher number of taps.

In Table 1, group C has (g_5, g_9), whereas g_{10}, g_{11}, and g_{12} belong to group D, since they all contain more than three taps. As visualized in Fig. 8, the SNR performance is degraded, as the number of consecutive feedback taps is increased. In group C we have g_5 and g_9, where g_5 performs better than g_9, because it has a 13 order PP, while g_9 has a 23 order PP. More explicitly, in group D g_{12} has more consecutive feedback taps than the rest of the group, namely as many as 2 to 15 taps, where each feedback-sample is noise-contaminated, hence degrading the achievable performance. Upon comparing the performances of PPs having an order of 13, i.e. g_{10} and g_{11} generated using 10 taps each, it is found that both PPs have two consecutive feedback taps. The PP g_{11} leads to an improved performance, because second higher feedback tap is connected to index 12 while in g_{10}, the second most index is connected to index 11. We infer that the detection capability of the receiver is reduced by the presence of consecutive feedback taps. The receiver exploiting g_{11} has a better chance of detecting the chips in the presence of noise as opposed to that employing g_{10}, since the detection capability of the receiver is degraded proportionally to the connecting indices of the feedback taps. Based on

our simulation results seen in Fig. 8, we conclude that the performance of the PPs predominantly depends upon three factors, namely on the order of the PP, on the number of connecting taps and on the specific indices of the connecting taps. When comparing PPs of similar order, PPs with less connecting taps will outperform those having a higher number of connecting taps, since the latter precipitated the noise-effects by having more feedback taps. Furthermore, if the connecting taps are same, then PPs with the second highest indices perform better. Therefore, the required SNR depends partially on the specific positions of vacant indices, when comparing PPs having similar orders. Finally, when comparing PPs of different order, the low-order PPs avoids the avalanche-like error-propagation of higher-order PPs, since the noise imposed on the chips of lower-order PPs results in fewer inaccuracy transmission than of higher-order PPs.

B. PERFORMANCE OF THE CONCATENATED SEQUENCES

We proceed by generating results for the concatenated sequences by utilizing the affordable number of iterations given by $\mathrm{L} = (200 \times R \text{ or } S)$, where R and S represent the two PPs of the same order. A total of eight concatenated sequences are generated as shown in Fig. 9 by utilizing the information given in Table 2, where E to L represent the concatenated sequences denoted as gg. The P_e versus SNR performance of the concatenated sequences demonstrates that the low-order PPs perform better than the high-order PPs, if they have fewer taps. The performance of gg_1 is superior to the rest, because it has a lower polynomial order of 5 as evidenced by Fig. 9. The performance of gg_3[8] is better than gg_7[9] and gg_8,[10] despite having the same polynomial order of 15. Therefore, similarly to the m-sequence's case, it can be inferred that PPs having less taps provide a higher likelihood of accurate extrinsic information for the SISO acquisition model. Consequently, PPs having fewer taps are adopted, as the malevolent effects of noise contaminates their chips less gravely, than for their higher-order counterparts. Furthermore, gg_1 performs better than the rest of the PPs, since it relies on a shorter memory. However, gg_1 has less confidence in its own soft values and thus it benefits more substantially from the use of an iterative scheme.

C. COMPARISON BETWEEN THE m-SEQUENCES AND THE CONCATENATED SEQUENCES

Let us now embark on comparing two types of PN sequences. A variety of simulation results are obtained for distinguishing the performances of the RSSE in an AWGN channel. In Figs. 10 and 11, P_e versus the SNR comparisons are recorded for the polynomial orders of 5, 6, 13, 15 and 23 for both m- and concatenated sequences. It may readily be

[8] gg_3 is obtained by two different PPs of order 15, namely g_6 and g_7 having three taps

[9] gg_7 is obtained by two different PPs of the order 15, namely g_7 and g_{12} having three and fourteen taps respectively.

[10] gg_8 is obtained by two different PPs of the order 15, namely g_6 and g_{12} having three and fourteen taps respectively

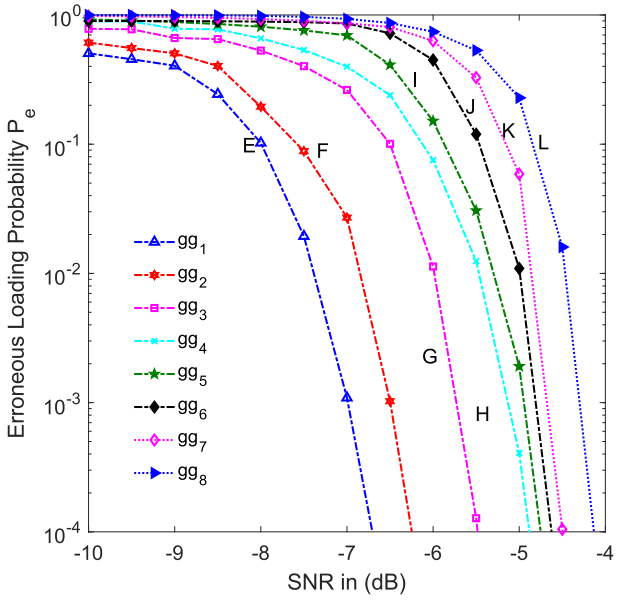

FIGURE 9. Performance comparisons between the different concatenated sequences, where E, F, G, H, I, J, K and L represent the concatenated sequences generated by two different PPs of the same length, as illustrated in Table 2 and gg denotes concatenated sequences.

TABLE 2. Generation of concatenated sequence from primitive polynomials invoked for our RSSE scheme.

Groups	Representation of Polynomials	Polynomials Achieved by Concerned PPs	Polynomial Order
E	$gg_1(D)$	$g_1(D) \oplus g_2(D)$	5
F	$gg_2(D)$	$g_3(D) \oplus g_4(D)$	6
G	$gg_3(D)$	$g_6(D) \oplus g_7(D)$	15
H	$gg_4(D)$	$g_8(D) \oplus g_9(D)$	23
I	$gg_5(D)$	$g_5(D) \oplus g_{11}(D)$	13
J	$gg_6(D)$	$g_5(D) \oplus g_{10}(D)$	13
K	$gg_7(D)$	$g_7(D) \oplus g_{12}(D)$	15
L	$gg_8(D)$	$g_6(D) \oplus g_{12}(D)$	15

inferred that the performances of concatenated sequences are better than those of m-sequences, which are represented by the dotted lines and are labelled as E, F, G, K and L in Figs. 10 and 11. We achieve a 1.85 dB gain for the best case upon comparing gg_1 to g_1 and also attain 1.5 dB gain compared to g_2, as observed in Fig. 10 for group E. This conclusion is confirmed by comparing the blue dotted line of gg_1 to the red solid line of g_2 and the blue solid line of g_1 to the blue dotted line of gg_1, which represents the PP order of 5 having three taps. When we compare PPs gg_2 to g_3 and g_4 of order 6 having three taps, we acquire a 1.85 dB gain in the best-case upon comparing gg_2 to g_3 and 1.5 dB gain, when compared to g_4. This result indicates that by using a low-order PP we can achieve a better performance for concatenated sequences. In Fig. 10, gg_3 performs better than gg_7 and gg_8. Upon comparing gg_3 to the chosen m-sequences, it is observed that in the best-case P_e versus SNR performance scenario of g_6 we obtain 1.85 dB gain by gg_3 over g_6 and 1.5 dB gain when compared to g_7, since it has the order 15 having three taps. When considering gg_7, we achieve 0.75 dB

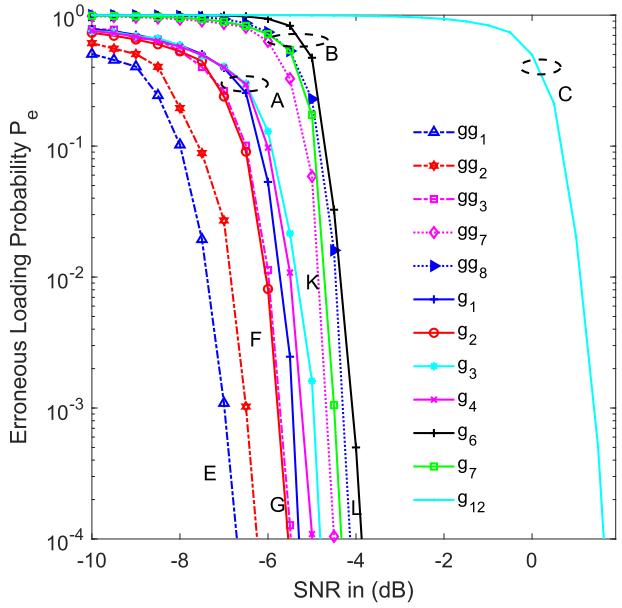

FIGURE 10. Comparisons between concatenated sequences and *m*-sequences are provided for polynomial orders of 5, 6 and 15. The dotted lines show the performances of concatenated sequences.

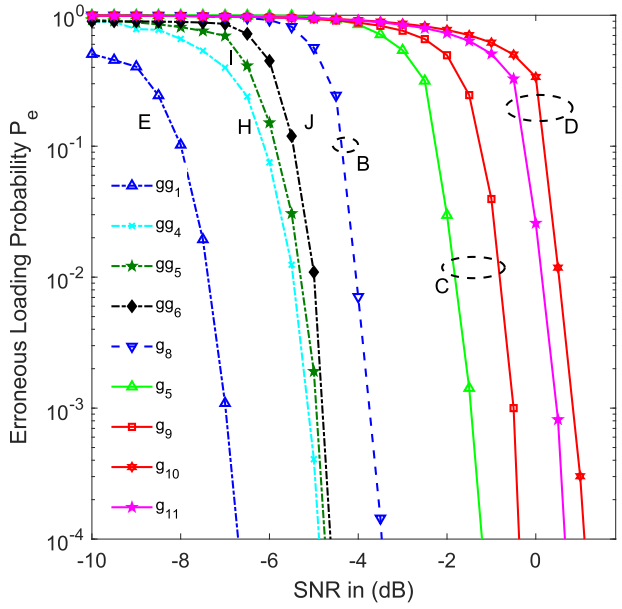

FIGURE 11. Comparisons between concatenated and *m*-sequences are carried out for PPs of 5, 13 and 23 order. The dashed lines show the performances of concatenated sequences.

gain compared to g_7, while upon comparing g_6 to gg_8 denoted by L in Fig. 10 we obtain 0.75 *dB* gain. For the polynomial order of 15, we obtain 7.5 *dB* gain in the best-case upon comparing gg_3 to g_{12} as g_{12} contains all consecutive taps located at the positions 2 and 15 (taps 2 and 15). For the worst case, we obtained at most 5.8 *dB* gain, if we compare gg_8 to g_{12}, as depicted in Fig. 10.

In Fig. 11 we have compared *m*- and concatenated sequences of the polynomial orders of 5, 13 and 23. It is evident that the concatenated sequences perform better than *m*-sequences. For the polynomial order of 5, the performance gain of concatenated sequences is 1.5 *dB* for the worse-case scenario when comparing the SNR at a P_e values of 10^{-4}, as discussed earlier in the context of Fig. 10. For a polynomial order of 13, gg_5 achieves a 5.5 *dB* gain for the best-case scenario over g_{11} and even in the worst-case we achieve a 3.0 *dB* gain over g_5. This is because the concatenated sequence gg_5 is composed of the PPs g_5 and g_{11} having an order of 13. The PP g_5 has two consecutive taps, namely one located at the positions of 0 and 1 (taps 0 and 1) and the other located at the positions 3 and 4 (taps 3 and 4), similarly, PP g_{11} also has two consecutive taps, namely one located at the positions of 0 and 6 (taps 0 and 6) and the other located at the positions 12 to 13 (taps 12 to 13). This indicates that the presence of consecutive taps dominates the performance of the PPs. More clearly, these consecutive taps gravely boost the deteriorated effect of noise. Hence the performances of gg_5 and gg_6 are better than those of g_5, g_{10} and g_{11}. On the other hand, for the worst-case, we obtain at most 5.5 *dB* gain if we compare gg_6 to g_{10}, as depicted in Fig. 11. Furthermore, for gg_4 the gain attained is 1.35 *dB* compared to g_8 of a polynomial order of 23, where this concatenated sequence is composed of g_8 and g_9, as depicted in Tables 1 and 2, respectively. Upon considering the polynomial order of 23 and comparing gg_4 to g_9, we attain a gain of 3.8 *dB*. In summary, PPs having more taps are substantially influenced by the noise imposed on them, therefore they cannot provide better LLR values than their counterparts having less taps, which can be visualized upon comparing gg_3 to both gg_7 and to gg_8.

D. COMPARISON BETWEEN THE ACQUISITION TIME OF *m*-SEQUENCES AND CONCATENATED SEQUENCES

Our iterative detection aided RSSE acquisition technique proficiently exploits the reliabilities of the latest successive chips during examining the magnitudes of the related soft outputs stored in the SCRs of Fig. 5. When P_e is as low as 10^{-4}, successful *m*-sequence acquisition can typically be declared with a sufficiently high likelihood after the initial loading of the chips. Resultantly, the total AT of the RSSE acquisition technique may be approximated by the time interval required by the RSSE for carrying out SISO detection, at a sufficiently low P_e. According to the iterative decoding principle [60], [61], the time required by the RSSE scheme for operating at a sufficiently low SNR value[11] and for generating a recursive SISO detection output depends both upon the number of stages, as well as on S and R in the associated *m*-sequence generators. Based on our design proposed in Fig. 5 the performance of the RSSE acquisition technique is determined by the SCR having the periods of S and R for the two *m*-sequence generators. Fig. 12 characterizes the acquisition performance of the 13^{th} order polynomial g_5 having a length of $N = 2^{13} - 1 = 8191$ chips. Observe in

[11]The value indicates that P_e is in the range of between 10^{-3} to 10^{-4}.

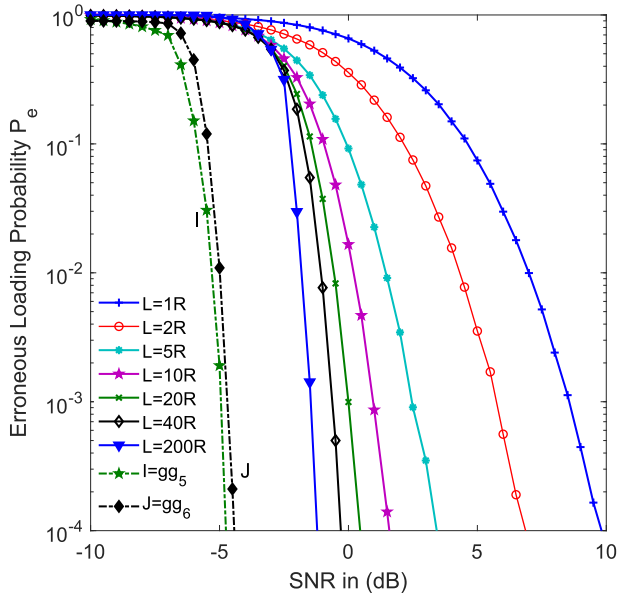

FIGURE 12. Erroneous loading probability P_e versus SNR parametrized by the number of chips entered into the recursive SISO decoder, when transmitting the m-sequence generated using the PP of $g_5(D) = 1 + D + D^3 + D^4 + D^{13}$ over an AWGN channel, where $gg_5(D)$ and $gg_6(D)$ are the concatenated sequences.

Fig. 12 that $P_e = 10^{-4}$ is achieved at an SNR value of 9.5 dB by entering $L = 1 \times R = 1 \times 13 = 13$ chips into the iterative SISO detector of Fig. 5. In this case our system does not have any *a priori* information, hence it acts as the traditional acquisition technique of [17]. However, we can achieve a better performance by entering more chips into the proposed iterative acquisition technique scheme. As seen in Fig. 12, by entering $L = 40 \times R = 40 \times 13 = 520$ chips into the iterative SISO detector of Fig. 2 we achieved $P_e = 10^{-4}$ at an SNR value of -0.8 dB. Furthermore, we attained a better SNR value of -1.8 dB at a $P_e = 10^{-4}$ upon entering $L = 200 \times R = 200 \times 13 = 2600$ chips into the SISO detector. Therefore, the SNR gains at a P_e of 10^{-4} are about 10.3 to 11.3 dB compared to the traditional acquisition technique of [17], when the total number of received chips are 520 and 2600, respectively. Even though a total of 2600 chips have been received by the SISO scheme for attaining $P_e = 10^{-4}$ at the SNR per chip of -1.8 dB, the AT still remains significantly inferior to that of any traditional serial search technique [21], [62]. This observation indicates that the AT is directly proportional to the length of the sequences measured, which is 8191 chips in this case. As compared to the concatenated sequences of similar orders, such as gg_5 and gg_6, the required SNRs are -4.9 and -4.6 dB, respectively when entering 2600 chips into the iterative SISO detector for attaining reliable acquisition. It has been stated in [21] that the AT τ_D of a conventional technique has to obey $N_{\tau_D/2}$[12] $= 4095 \cdot \tau_D >> 2600$ chips, even if the SNR value is sufficiently high. Therefore, the proposed RSSE acquisition technique becomes the best, substantially outperforming the best known benchmarkers of [18], [21], [23], [63], and [64].

[12] $N_{\tau_D/2}$ represents the mean acquisition time of a sequence having a particular chip length, i.e. 8191. and τ_D corresponds to the dwell time which normally spans from hundreds to thousands of chip periods [21]

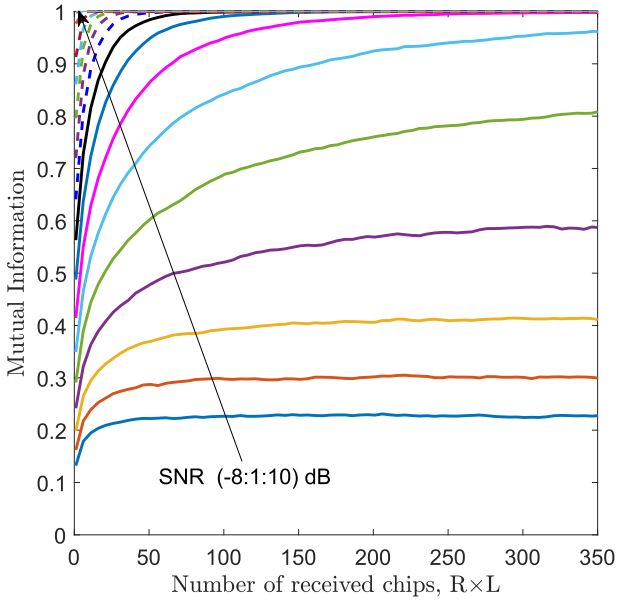

FIGURE 13. Mutual information versus the number of received chips for the m-sequence of PP $g_1(D) = 1 + D^2 + D^5$ having a polynomial order of 5 parametrized by various SNR values ranging from -8 to 10 dB having a maximum of $L = 70$ decoding iterations to reach MI= 1.

E. EXIT CHART ANALYSIS OF CONCATENATED SEQUENCES

The relationship between the MI and the number of received chips is revealed by Fig. 13, when the PP g_1 of Table. 1 is used. As expected, the MI of the PP g_1 increases upon increasing the number of received chips, provided that the SNR is increased. We may infer from Fig. 13 that we need fewer received chips to approach $MI = 1$ upon increasing the SNR. The results of Fig. 13 also reveal that for SNR values higher than -3 dB, the MI reaches unity after receiving at most 300 chips. The PP g_1 has $R = 5$ register stages, hence the highest number of detection iterations is given by the ratio of the number of received chips to the polynomial order. Hence we have $L = 350/5 = 70$.

Fig. 14 shows the MI versus the number of received chips for the PP gg_1 of Table 2. We observe that a lower number of received chips is required to approach MI $= 1$ at a higher value of SNR. Furthermore, we infer that the MI approaches unity after receiving less than 100 chips for SNRs higher than -4 dB. Upon comparing Fig. 13 to Fig. 14, we observe that the concatenated sequences need fewer iterations to achieve MI $= 1$ than the m-sequences. Hence, the performance of the concatenated sequence is better than that of the m-sequence.

Fig. 15 depicts the Average Mutual Information (AMI) versus the number of iterations at an SNR of 0 dB, when PPs of different orders are utilized for generating m-sequences. It is predicted that the AMI becomes unity for a maximum of 25 iterations. Fig. 15 also shows that PPs associated with

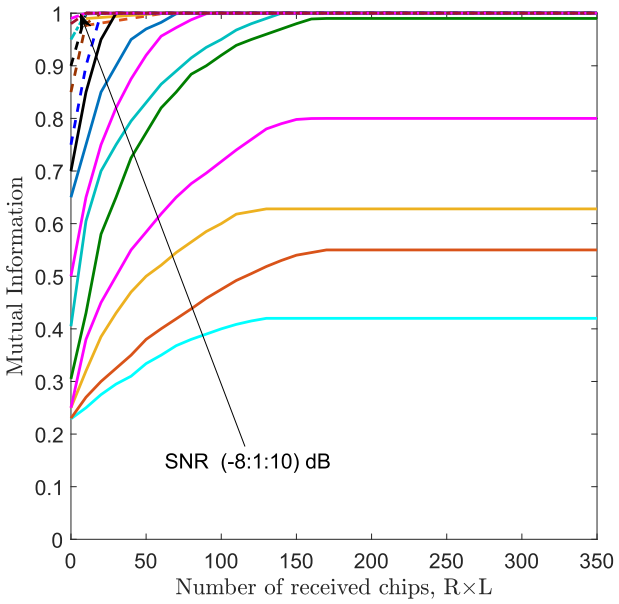

FIGURE 14. Mutual information versus the number of received chips for the concatenated sequence of PP $gg_1(D) = g_1(D) \otimes g_2(D)$ having the polynomial order of 5 parametrized by various SNR values ranging from −8 to 10 *dB* having a maximum of $L = 70$ decoding iterations to reach MI = 1.

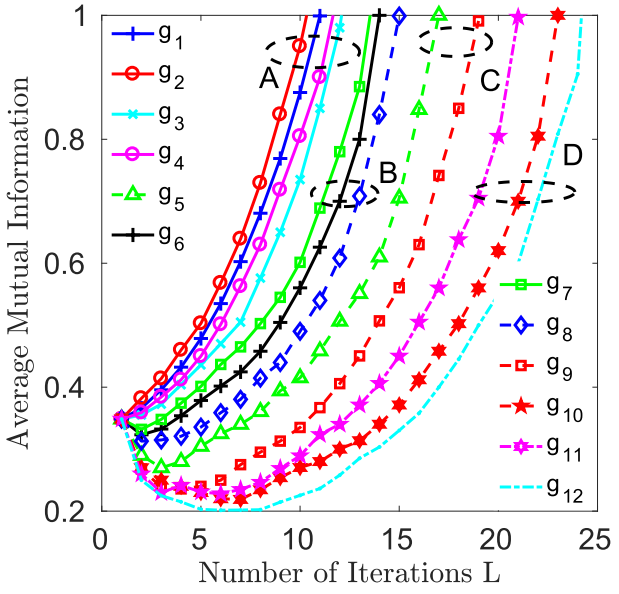

FIGURE 15. Average mutual information versus the number of decoding iteration when SNR = 0 *dB* for *m*-sequences.

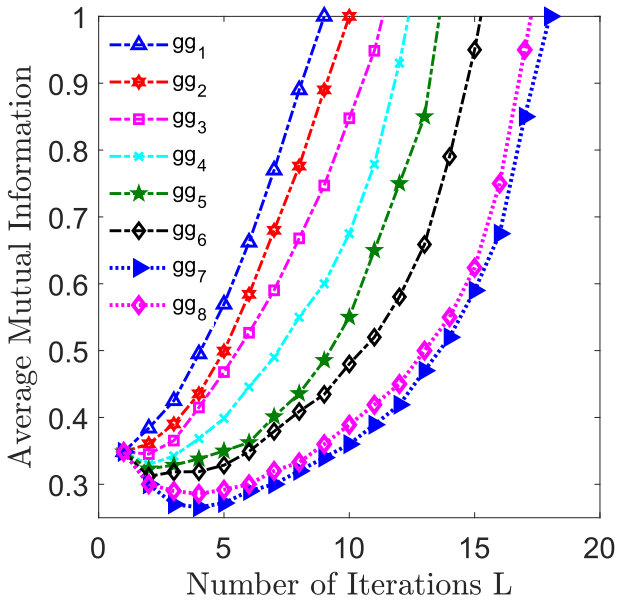

FIGURE 16. Average mutual information versus the number of decoding iterations at SNR = 0 *dB* for concatenated sequences.

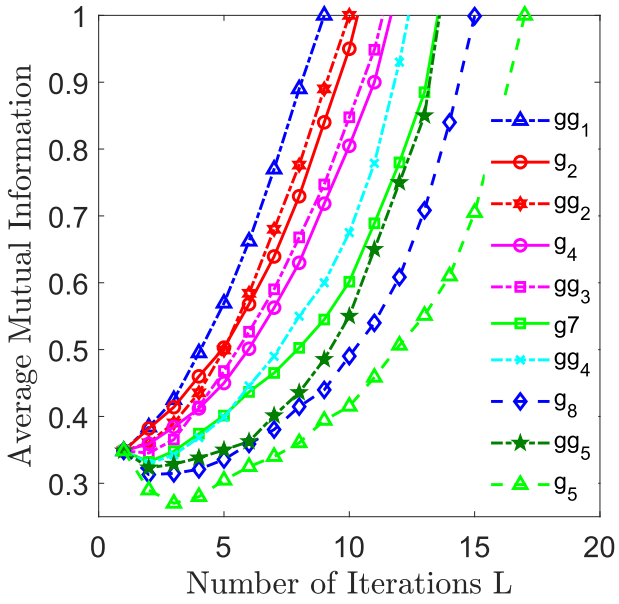

FIGURE 17. Comparison between *m*- and concatenated sequences w.r.t. the number of decoding iterations versus average mutual information when plotted at SNR = 0 *dB*.

a lower polynomial order perform better, which is a benefit of their lower number of taps. Moreover, when comparing PPs, which have the same order and a similar number of taps, the ones having their second tap at a higher index result in a higher AMI after a specific number of iterations. The AMI analysis also corroborates that PPs having less taps guaranteed better performance than those having more taps, because the adverse effects of noise imposed on their chips resulted in lower distortion than for their counterparts having more taps, as exemplified by comparing g_5 to both g_{14} and to g_{15}, respectively.

Fig. 16 characterizes the AMI versus the number of iterations at an SNR of 0 *dB*, when PPs of the same order are used for producing concatenated sequences. It is anticipated that for any PPs employed for generating the concatenated sequence we need fewer than 18 iterations to approach the maximum MI of one. Fig. 16 also reflects the same fact that the PPs of lower order perform better due to having less taps, as discussed earlier in Figs. 11 and 15. Similarly, Fig. 17 shows our comparison between the performances of *m*- and concatenated sequences by plotting the AMI against

TABLE 3. Comparisons of SNR values in *dB* versus the location of the second highest tap present in PP as well as the number of iteration, where PPs of the orders 5, 13 and 23 are evolved in producing *m*- and concatenated sequences.

Poly--nomial order	Represent--ation of Polynomials	SNR (dB) at P_e 10^{-3}	Location of the second highest tap present in PP	Number of Iterat--ion
5	$g_1(D)$	-5.6	2	11
5	$g_2(D)$	-5.8	3	10
5	$gg_1(D)$	-7.0	3	8
13	$g_5(D)$	-1.0	4	17
13	$g_{10}(D)$	0.6	11	23
13	$g_{11}(D)$	0.5	12	21
13	$gg_5(D)$	-5.0	12	14
13	$gg_6(D)$	-4.5	11	15
23	$g_8(D)$	-3.8	5	15
23	$g_9(D)$	-0.5	17	19
23	$gg_4(D)$	-5.5	17	12

the number of iterations. The results also confirm the same trend as those found in Figs. 15 and 16.

Table 3 compares three major factors in the focus of this analysis, namely the P_e versus SNR, the location of the second tap present in the PP as well as the number of iterations. Our findings of Figs. 9 to 17 as well as Table 3 corroborate that the concatenated sequences have superior performance in terms of P_e versus SNR when different orders of PPs are compared. It can also be concluded that any pair of concatenated sequences require less iterations to achieve AMI $= 1$ and attain a better iteration gain compared to *m*-sequences. Fig. 18 illustrates the EXIT chart of the self-concatenated method used for characterizing the RSSE technique at an SNR value of 0 *dB*. We have selected PPs according to their P_e versus SNR performances and AMI versus iteration index. The PPs having orders of 5, 13 and 23 are used for generating the EXIT-trajectories. It is observed that all detection trajectories match their related outer and inner decoder curves. Based on the open EXIT tunnel we expect a low BER for an RSSE receiver, namely when an open EXIT tunnel is guaranteed between the inner/outer decoder's EXIT curves. When the open tunnel becomes wider, less iterations are required.

Additionally, it can be observed that the PP g_{11} of order 13 failed to reach the [1,1] position at the top right end, since the outer and inner curves intersect prior to reaching the [1,1] point. Hence, the decoding trajectory exhibits no MI improvements beyond the crossover point. As expected, a lower number of taps widens the gap between the inner and outer EXIT curves. Furthermore, the associated decoding trajectory perfectly matches the inner and outer EXIT curves. We also deduce that the *m*-sequences having more taps tend to require larger memory and therefore a reduced iteration gain is attained. Both g_5 and g_{11}, perform worse than the other PPs, because they have more feedback taps, as discussed in Section IV-B. Accordingly, we conclude that the use of a lower number of taps provides wider opening between their inner and outer decoder curves and have better match between their stair-case-shaped decoding trajectory and the EXIT-curves of the inner and outer decoders.

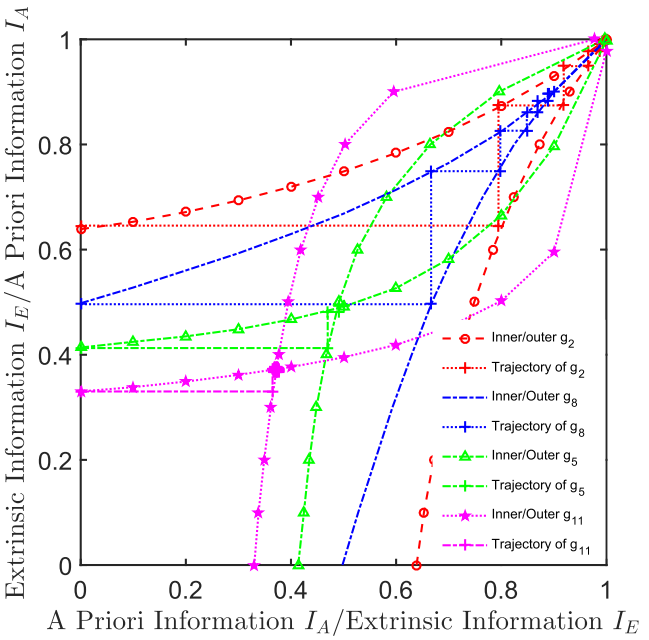

FIGURE 18. EXIT chart for PPs of different orders for transmission over an AWGN channel, at SNR = 0 *dB*.

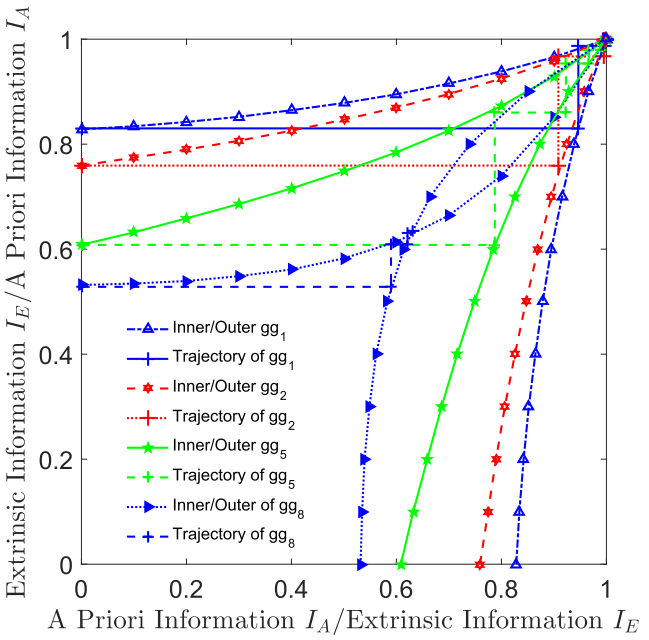

FIGURE 19. EXIT chart for the PPs of gg_1, gg_2, gg_5 and gg_8 for transmission over an AWGN channel at SNR = 0 *dB*.

Fig. 19 demonstrates that the polynomial gg_1 of Table 3 approaches the [1,1] point at SNR $= 0$ *dB*. An improved resemblance amongst the detection trajectories as well as the outer and inner EXIT curvatures arises at higher SNR values. This illustrates that the EXIT chart trends confirm the AMI-trends of Figs. 15 and 16. Explicitly, the lower-order PPs have a superior convergence, since they benefit more substantially from the iterative procedure. Accordingly, PPs having more taps are directly influenced by the noise and

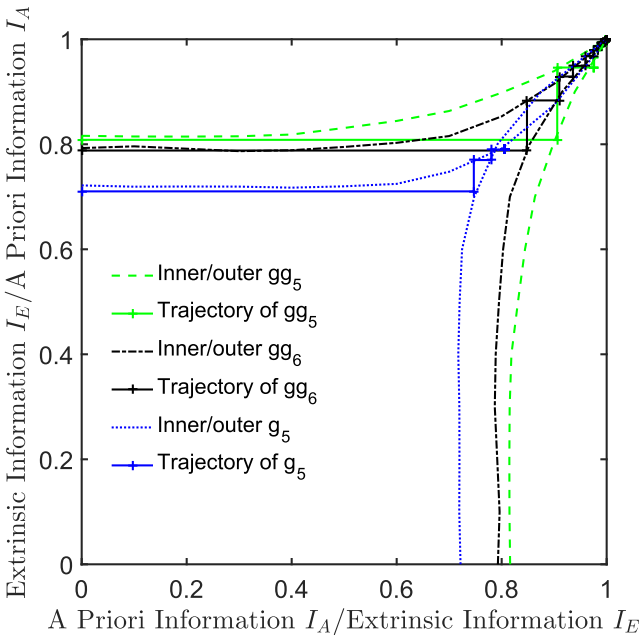

FIGURE 20. EXIT chart for the PPs of order 13 for transmission over an AWGN channel at SNR = 2 *dB*.

need more iterations to attain error-free decoding. We further benchmark the performance of our system by investigating PPs of the order 13 in Fig. 20. The PP gg_5 of Table 3 requires the least detecting iterations to approach the [1,1] point at SNR $= 2$ *dB*. Moreover, by invoking more decoding iterations, the SISO detector approaches the [1,1] point of perfect convergence to a vanishingly low P_e. Therefore, we conclude that the lower-order polynomials having less taps perform better, despite requiring less computations.

V. CONCLUSIONS

We conclude that the performance of concatenated sequences is superior to that of *m*-sequences, when comparing their P_e versus SNR performance. When considering PPs having the same order but different number of taps, the PPs having less taps outperform the PPs having more taps. This is due to the noise affecting the chips of PPs having more taps more gravely, than their counterpart having less taps. In other words, the PPs relying on a low number of tap connections have a higher probability of reaching MI $= 1$ for the SISO acquisition technique than those utilizing a higher number of tap connections. It is revealed that the PPs having taps located at higher indices yield a wider EXIT tunnel, indicating more rapid convergence for concatenated sequence acquisition. The simulation results of Figs. 8 to 11 and Table 3 also confirm the validity of the EXIT chart model proposed. Owing to these appealing attributes, our iterative RSSE acquisition scheme is capable of performing efficient initial synchronization of both long *m*- and concatenated sequences with a low AT. Furthermore, the proposed scheme performs better than the family of conventional serial and parallel search-based acquisition techniques. Accordingly, its exploitation may shed light on more efficient receiver design for PN sequence detection in 5G.

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ABBAS AHMED received the B.E.E. degree in electrical engineering (specialisation in electronics) from Air University, Islamabad, Pakistan, in 2007, and the M.Sc. degree (Hons.) from the University of Southampton, U.K., in 2009, where he is currently pursuing the Ph.D. degree with the Southampton Wireless Group, School of Electronics and Computer Science. His research interests include frequency hopping systems, multiple access systems, coded modulation, iterative detection, and initial synchronization.

PANAGIOTIS BOTSINIS (S'12–M'15) received the M.Eng. degree from the School of Electrical and Computer Engineering, National Technical University of Athens, Greece, in 2010, and the M.Sc. degree (Hons.) and the Ph.D. degree in wireless communications from the University of Southampton, U.K., in 2011 and 2015, respectively, where he is currently a Research Fellow with the Southampton Wireless Group, School of Electronics and Computer Science. Since 2010, he has been a member of the Technical Chamber of Greece. His research interests include quantum-assisted communications, quantum computation, iterative detection, OFDM, MIMO, multiple access systems, coded modulation, channel coding, cooperative communications, and combinatorial optimization.

SEUNGHWAN WON (SM'16) received the B.S. and M.S. degrees in radio science and engineering from Korea University, Seoul, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree from the Communications Research Group, School of Electronics and Computer Science, University of Southampton, U.K. He was a Research Engineer with the Mobile Communication Technology Research Laboratory, LG Electronics Inc., from 2001 to 2004. From 2004 to 2008, he conducted research, working toward his Ph.D. degree. Upon completing his Ph.D., he returned to South Korea and joined Samsung. In 2013, he was appointed as an Associate Professor with the University of Southampton. He is currently teaching and conducting research at the University of Southampton, Malaysia. His major research interests include synchronization and multi-user MIMO in mmW mobile communications, the intelligent Internet of Things, and intelligent unmanned aerial vehicle-assisted mobile communication systems. He has published a host of papers in these research fields and secured more than 20 U.S. patents. He was a recipient of the 2004 State Scholarship of the Information and Telecommunication National Scholarship Program, Ministry of Information and Communication, South Korea.

LIE-LIANG YANG (M'98–SM'02–F'16) received the B.Eng. degree in communications engineering from Shanghai Tiedao University, Shanghai, China, in 1988, and the M.Eng. and Ph.D. degrees in communications and electronics from Beijing Jiaotong University, Beijing, China, in 1991 and 1997, respectively. In 1997, he was a Visiting Scientist with the Institute of Radio Engineering and Electronics, Academy of Sciences, Czech Republic. Since 1997, he has been with the University of Southampton, U.K., where he is currently a Professor of wireless communications with the School of Electronics and Computer Science. His research interests include wireless communications, wireless networks, signal processing for wireless communications, molecular communications, and nano-networks. He has published over 350 research papers in journals and conference proceedings, has authored/co-authored three books, and has also published several book chapters. He is a Fellow of the IET, U.K., and a Distinguished Lecturer of the IEEE Vehicular Technology Society. He has served as an associate editor for several academic journals, has co-organized several special issues, and has acted in different roles for conference organization.

LAJOS HANZO (M'91–SM'92–F'04) received the degree in electronics, in 1976, and the Ph.D. degree, in 1983. Since 1986, he has been with the School of Electronics and Computer Science, University of Southampton, U.K., where he currently holds the Chair in telecommunications. During his 38-year career in telecommunications, he has held various research and academic posts in Hungary, Germany, and U.K. He has successfully supervised 112 Ph.D. students, has co-authored 18 John Wiley/IEEE Press books on mobile radio communications totaling in excess of 10 000 pages, and has published over 1800 research contributions at the IEEE Xplore. He is currently directing an academic research team, working on a range of research projects in the field of wireless multimedia communications sponsored by industry, the Engineering and Physical Sciences Research Council, U.K., the European Research Council's Advanced Fellow Grant, and the Royal Society's Wolfson Research Merit Award. He is an Enthusiastic Supporter of industrial and academic liaison and he offers a range of industrial courses. He has acted both as the TPC and as the General Chair of the IEEE conferences, presented keynote lectures, and has been awarded a number of distinctions. In 2009, he was awarded the honorary doctorate *Doctor Honoris Causa* by the Technical University of Budapest.

He was a Chair Professor with Tsinghua University, Beijing. He is a Fellow of the Royal Academy of Engineering, the Institution of Engineering and Technology, and the European Association for Signal Processing. He is also a Governor of the IEEE VTS. He was the Editor-in-Chief of the IEEE Press.