An Investigation into the Suitability of Insulated Core Transformer Technology for an Ultra High Voltage Power Supply

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ABSTRACT

A growing area of interest is HVDC supplies. This paper represents an initial study into possible designs of HVDC transformers that could provide 2 A at 1 MV, with the added specification that any proposed technology should be scalable to 5 A at 5 MV. Insulated core transformers (ICTs) have been initially selected as a potentially suitable technology. Careful design of the ICT magnetic core is required to ensure that flux loss is limited so that higher voltages are achievable. Simulation studies have shown that the voltage produced in an ICT does not scale linearly, meaning that there is an effective limit to the voltage that they can produce. In addition to this, a technique is proposed to increase the available current output of an ICT. The full analysis is presented in this paper.

Index Terms — **HVDC, transformer, insulated core transformers, simulation, magnetic flux**

1 INTRODUCTION

THERE is currently growing interest in both academia and industry for a power supply capable of producing 2 A continuous DC current, at 1 MV, with a maximum voltage ripple of 0.5%. Any design must be as compact as possible; ideally able to fit inside a three-meter cube, and should store limited energy of the order of hundreds of joules or less. This final requirement is a safety measure, as a fault in the HV circuits of a supply that stores a lot of energy could be catastrophic and irreparable. At the same time there is also interest in developing such a supply further, in the future, to ultimately be able to generate 5 A continuous DC current at 5 MV.

Several technologies are currently used ubiquitously in compact HV power supply design, most notably the Cockroft Walton (CW) Generator. These are popular, in no small part, due to their simplicity; they can easily generate several megavolts using relatively few components. However, they suffer from severe voltage drop under heavy load, and require a large amount of stored energy [1].

For this reason, other technologies with a higher power density are being investigated. Amongst the most promising are resonant transformers (RTs), cascade transformers (CTs), and insulated core transformers (ICTs). The aim of the work reported in this paper is to examine the feasibility of using an ICT based design for this particular application.

This work is based on assuming the limitations of current insulating film technologies. That is to say, the simulation studies do not anticipate any significant developments in core electrical properties of thin film insulation materials. All designs assume that insulation of the individual cores is achieved using a 250 micron thick film of a commonly used solid insulator such as mylar, teflon, or kapton.

2 CORE LAYOUT

The first ICTs, as patented by Van de Graaf [2], consisted of a single stack of electrically insulated cores, effectively creating a bar core transformer. In order to prevent the magnetic flux from bypassing the HV cores completely, the stack was placed inside a

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metal container. This container was connected to the core around which the primary winding was wound. Flux could then bridge the gap between the top of the stack and surrounding container before completing the path to the primary winding.

As the grounded container had to be insulated from the total operational voltage of the device, it was necessary for a large gap to exist between the top of the stack and the container. This limited the flow of flux to the top of the stack. The reduction in flux, reaching the higher cores, reduced the operational voltage of secondary windings further away from the primary.

Soon a three-phase variant of the ICT was developed for high power applications [3], thus eliminating the need for the grounded container, by providing a complete flux path between phases. This worked in the same way as a three-phase transmission, or distribution, transformer.

Van de Graaf sought to get around the voltage drop, associated with flux loss, by wrapping more windings around cores situated further away from the primary. This however, adds complexity to the system design as the windings around each insulated core have to be unique. A more economical design would have identical windings around each core to reduce system cost and complexity. In addition to this, there is a practical limit to the voltage that can be obtained using a single stack, as increasing the height of the stack will soon yield diminishing returns, in terms of voltage, as the flux loss becomes too great.

A number of different core configurations were examined in [4] and it was concluded that the most effective way of reducing flux loss is, as with a conventional transformer, to create a closed flux path from soft magnetic material. This technique was employed, amongst others, by Cross, who patented an ICT that produced 375 kV. That was then doubled to 750 kV using power electronics [5], at several hundred milliamps. This design has since been scaled up to 1 MV [6].

A necessity of creating a continuous flux path from soft magnetic material is that there needs to be two insulated cores operating at each voltage level. This is to stop the HV core needing to be insulated from the grounded primary winding. The Cross ICT achieved this by having two parallel insulated stacks connected, at the bottom, by a grounded core around which the primary winding is wound and, at the top, by another core section that would allow flux to pass between the two HV sections (Figure 1). This is an elegant solution as it means that the LV primary is at the bottom while the voltage, in the stacks, increases in the cores further away from the primary. However, there are problems with flux passing between the two stacks and being reluctant to change direction at the top of the stacks.

In this paper, the authors have investigated an alternative arrangement in which a single stack is constructed that is driven by a primary winding at either end. These primary windings are electrically connected in parallel, meaning that they operate in phase with each other. The voltage increases towards the center of the stack, where it is insulated from the LV winding at each end. Flux can then pass between the two windings via a solid clamp, as seen in Figure 2. This layout has the advantage that the magnetic flux has a straight path through the cores. In addition to this, having insulated gaps in a core effectively reduces the relative permeability of the core material. This means that the clamped system will reduce the amount of flux leaving the stack to return to the primary winding through the parallel flux path.

The relative flux path found in each layout was calculated and compared using a finite element analysis (FEA) model. In each case, an ICT was simulated with a core cross sectional area of 100 mm by 100 mm, and a thickness of 5.75 mm. There was a distance of 200 mm between the insulated stack and the return path, and a gap of 0.25 mm between each insulated core. Each core was surrounded by 100 windings. These parameters are reasonable as they are based on those commonly used in ICTs based on the Cross design [6]. ICTs with stack heights from 1 to 50 cores were simulated, in both layouts, and the minimum normalized flux in each system was recorded as shown in figure 3.

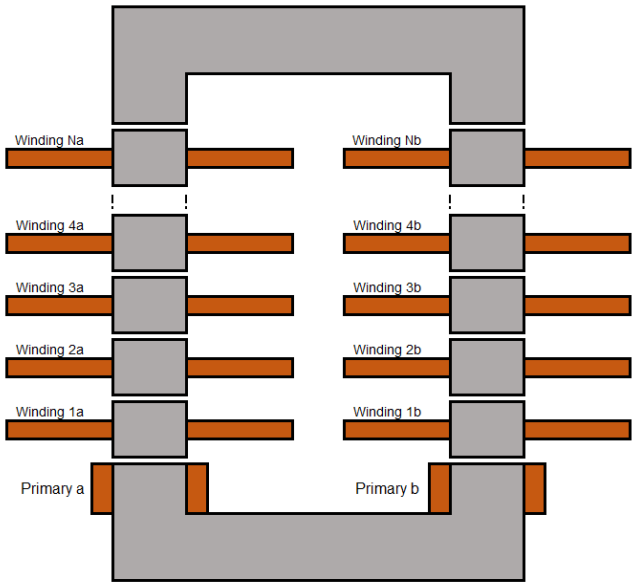

Figure 1. The traditional layout of the Cross type ICT.

From Figure 3 it can be seen that there is no significant difference between the flux losses obtained using either arrangement when the number of insulated cores is less than 30. For this reason, in a single phase ICT, a flux return clamped layout is inefficient as it effectively doubles the height and material cost of the design, without significantly reducing the flux loss. However, in designs that consist of multiple phases and a significant number of insulated cores (e.g. more than 40), the single stack configuration may prove advantageous; this is discussed further in Section 4.

The flux loss predicted in these simulations, and detailed in Figure 3, is approximately half of that previously reported for an ICT [6] that was operating a higher voltage than used in this simulation study. The use of 2D simulation will lead to an underestimate of flux loss in the third dimension.

3 BENEFITS OF CROSS CORE TECHNOLOGY

In addition to the closed flux path, there are several other appealing features of Cross transformer technology (CTT). Most apparent is that the secondary windings are constructed from PCB windings [5]. The HV power electronics are also surface mounted to these PCBs for reduced construction cost and complexity. An advantage of PCB printed transformer windings is that they consist of one or two layers of windings spiraling outwards; this makes very flat windings and has the

benefit of reducing the thickness of each insulated core stage, therefore reducing the overall height of the design. However, a disadvantage of this technique is that it increases the surface area of each winding, thus increasing the parasitic capacitance between layers.

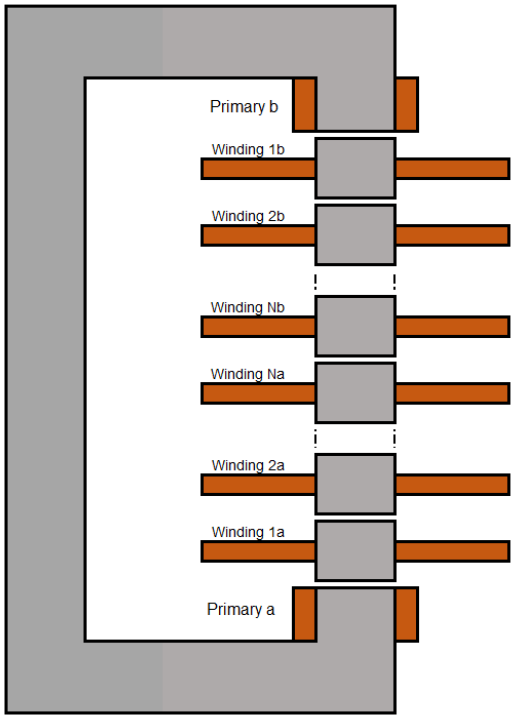

Figure 2. The proposed alternative layout of the Cross type ICT.

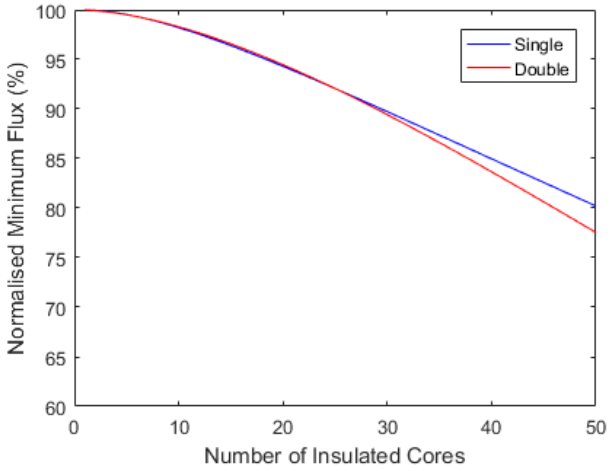

Figure 3. The minimum flux found in ICTs, arranged using both the traditional double stack layout and the proposed single stack layout, with a number of insulated cores ranging from 1 to 50.

While conventional ICTs operate at single or three phase grid frequency, CTT uses power electronics and specialist core materials, such as nanocrystalline, to operate at a frequency close to 100 kHz. This significantly reduces the necessary size of the design, as well as the energy that must be stored in the voltage doublers to reduce ripple.

The key advantage of CTT is the use of tuned capacitors, connected across each secondary winding, to compensate for the flux lost between core slices [5]. A circuit diagram of the voltage doubler combined with flux compensation is shown in Figure 4.

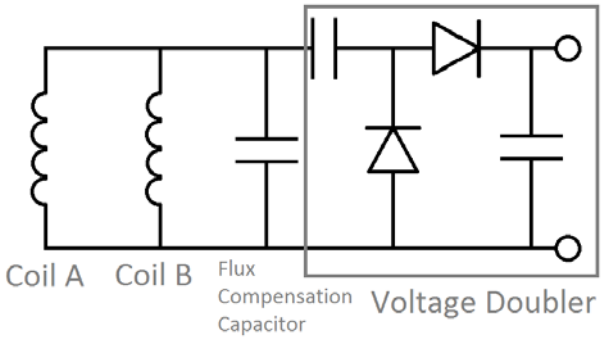

Figure 4. Circuit diagram of the secondary windings.

The capacitors are tuned to have a capacitance, C_{flux}, calculated using:

$$C_{flux} = \frac{l}{\mu_0 A N^2 (2\pi f)^2} \quad (1)$$

in which l is the length of the gap between insulated cores in meters; μ_0 is the permeability of free space; A is the cross sectional area of the gap between cores in meters squared; N is the number of windings around each core; and f is the operational frequency of the transformer.

An ICT, consisting of a stack of 50 cores, with the dimensions described in the previous section and a single core stack with clamped return path, was constructed in an FEA software package. The device was driven by a 500 Hz sinusoidal AC voltage source. Each secondary winding was connected in parallel with that of the other core acting at the same potential. The stack was driven by one of the secondary windings with a 100 V sinusoidal voltage acting upon it. A 1 kΩ resistor was connected across each set of secondary windings to draw an expected current of 100 mA. This design was simulated with, and without a compensation capacitor, and the peak voltage found in each respective winding is shown in Figure 5.

From Figure 5, it can be seen that the inclusion of a flux compensation capacitor reduces the flux loss by around 10%, and also makes the output voltage more consistent.

However, these simulations were carried out on a purely sinusoidal signal, which consists of a single frequency. In reality, an ICT that operates at high frequencies will likely be driven by square waves, which contain a large number of different frequencies. As the compensation capacitor can only be tuned to one frequency, it will add distortion to the overall signal. In order to evaluate this phenomenon, a single stack clamped return path ICT, with 50 pairs of secondary windings, each consisting of 100 turns, and driven by a pair of primary windings, each consisting 4 turns, at either end of the stack, was constructed in MagNet. This ICT was simulated, being powered by a sinusoidal signal, with a frequency of 100 kHz and an amplitude of 400 V_{pk-pk}, with and without a flux

compensation capacitor. Figure 6 compares the voltage across the 50th windings of both of these simulations, with the ideal output, over the course of a power cycle. These simulations were repeated using square wave excitation, with the results being shown in Figure 7.

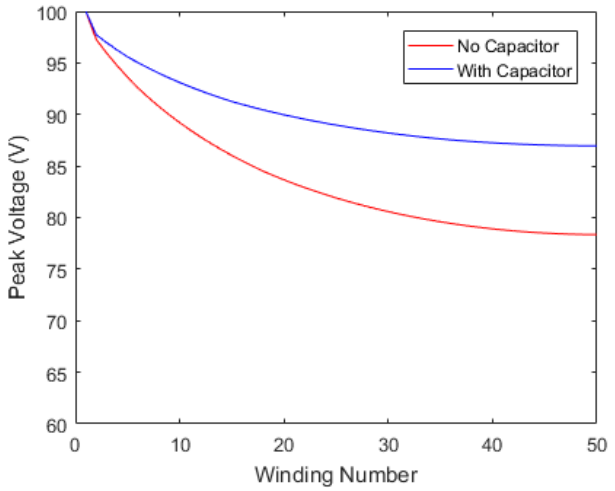

Figure 5. The peak voltage found in each secondary winding of an ICT, with 50 secondary circuits, with and without a flux compensation capacitor.

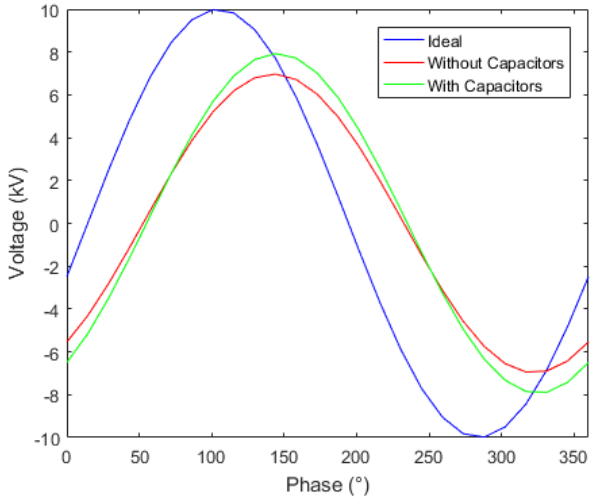

Figure 6. The 100 kHz voltage across the 50th pair of secondary windings, when excited by a sinusoidal signal with an amplitude of 400 V.

Figure 6 confirms the conclusions drawn from Figure 5; when sinusoidaly excited, the flux compensation capacitor raises the output voltage by approximately 10%. However, there is no significant difference in terms of average voltage, between the waveforms in Figure 7. The results produced by the flux compensation capacitor are more distorted, including a peak that has an amplitude nearly twice that of the average voltage. This could lead to failure of the dielectric film used to isolate the stacks and make the quality of the output voltage difficult to control. Practical experiments, verifying the results of these simulations, are currently being undertaken.

Two more techniques are employed, when manufacturing Cross type ICTs [6], to compensate for the effect that flux loss in the windings furthest from the primary winding has on the overall operational voltage of the design.

The first is to increase the voltage in the primary windings. This raises the voltage in each of the secondary windings, meaning that the lower secondary windings operate above their nominal voltage to compensate for the voltage lost in the higher windings. However, operating the secondary windings at a voltage above what they were rated for comes with the risk of placing additional strain on the components, and may reduce the lifespan of the windings.

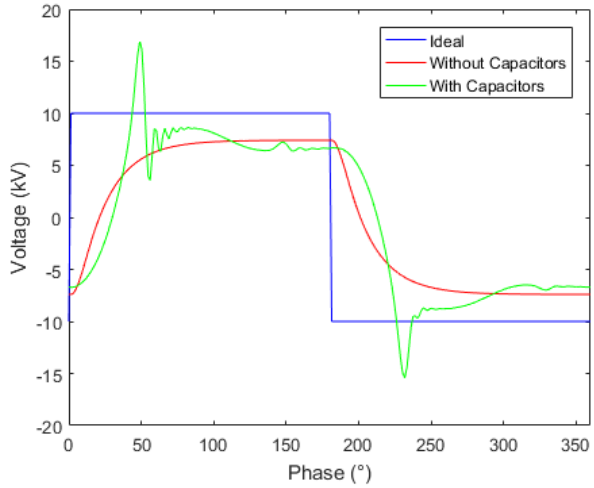

Figure 7. The 100 kHz voltage across the 50th pair of secondary windings, when excited by a square signal with an amplitude of 400V.

The other is simply to add additional cores to the top of the stack, each operating below their nominal voltage, until the desired overall voltage is reached.

4 STORED ENERGY

The use of capacitors, in flux compensators and voltage doublers, inherently stores energy in a system. The size of the capacitor, C, needed to reduce voltage ripple in a voltage doubler can be calculated using:

$$C = \frac{I}{2fV_{ripple}} \tag{2}$$

where I is the current drawn from the system; and V_{ripple} is the maximum allowable voltage ripple from the output voltage. The energy stored in each capacitor, E, can then be calculated using:

$$E = {}^{1}/_{2}\ CV^2 \tag{3}$$

Assuming each secondary winding produces 10 kV, doubled to 20 kV with a maximum allowable ripple of 0.5%, and operates at a frequency of 100 KHz, each capacitor will store 0.5 J. Multiplying this across all the capacitors in a stack means that the total stored energy per stack will be 50 J.

The energy stored in each compensation capacitor can be calculated using (1) and (3). Using the parameters described above, each capacitor will store 252 µJ of energy, meaning that across the whole stack, they will store only 25 mJ. This is a

negligible value and hence will be omitted from further calculations.

For reference, a Cockcroft Walton Generator, consisting of 10 stages, that produced 100 mA at 1 MV would need to store 1.1 MJ if operated at 50 Hz, or 550 J if operated at 100 kHz.

5 INCREASING THE CURRENT OUTPUT

There are three factors that limit the current that can be drawn from an ICT. These are the flux density of the core, the power electronics, and the winding thickness. The power electronics can, theoretically, be designed to accommodate any current, simply by selecting components rated to suitable specifications. The saturation of the core is more problematic in ICTs than in conventional transformers, as the relative permeability of the core material is effectively reduced by the insulated gaps. The saturation current becomes difficult to predict due to the non linear nature of the insulated cores.

The limitations imposed by the winding thickness are easier to calculate as the largest current that can safely pass through the tracks of a PCB can be determined by the IPC-2221 standard [7]. This standard dictates that the largest current that can safely be used in a PCB can be calculated using:

$$I = k\Delta T^{0.44} {A_{track}}^{0.725} \quad (4)$$

where I is the current passing through the track in Amperes; ΔT is the permissible change in temperature in °C; A_{track} is the cross sectional area of the track in mil^2; and k is a constant determined by the IPC-2221. For tracks printed on the surface of a PCB, k = 0.048.

Assuming each PCB is printed on a board with a copper thickness of 0.305 kg/m^{2,} the most commonly used copper thickness in PCB design, and the tracks are printed with a width of 0.5 mm, then the maximum safe current would be 1.46 A. This is even supposing that a maximum temperature increase of only 10 °C was imposed. Given the potentially dangerous nature of a fault in this project, it is not unreasonable to impose a large margin of error onto the maximum current, say, no more than half of the PCBs rated current may flow through the PCB windings during normal operation. This brings the effective rated current of each PCB down to 0.73 A, though because in this design, each winding is connected in parallel to another winding, the effective rated current of the stack once again becomes 1.46 A.

There are two ways in which the operational current of the ICT could be increased. The first is to increase the size of the single phase ICT, by widening the diameter of the tracks and the core. This will raise the saturation flux of the core and the current that can safely pass through the windings.

The second is to connect multiple stacks in parallel, as shown in Figure 8. This arrangement has the advantage that scaling up a design becomes a trivial exercise as, rather than having to redesign the whole design from first principles, to increase the operational current of the supply, one simply needs to add additional stacks to the existing design. Using multiple stacks also reduces voltage ripple, providing they each operate out of phase [8].

The stacks can be driven out of phase using a circuit, similar to the one in Figure 9, to power the primary windings. In this case, V_{in} can be provided by a rectified, three phase mains outlet and can be treated as a 400 V busbar. The switches, which would be replaced by MOSFETs in a practical circuit, can be operated in pairs to create a H-bridge. In this way, the voltage across the primary windings can be alternated, from +400 to -400 V, at a frequency determined by a microcontroller. The circuit shown in Figure 9 is designed for an ICT consisting of four stacks, but can be expanded to accommodate any even number of stacks.

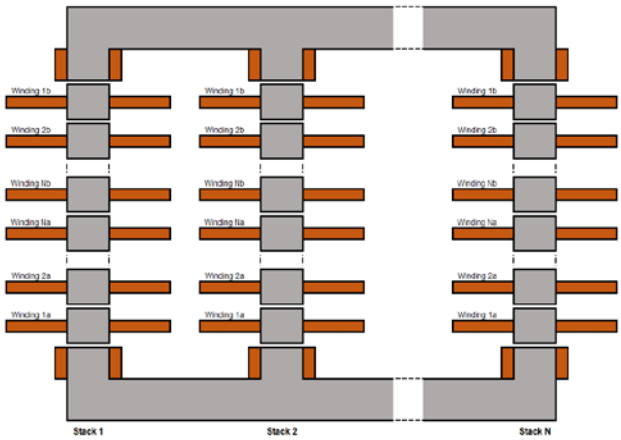

Figure 8. The layout of a multiphase ICT.

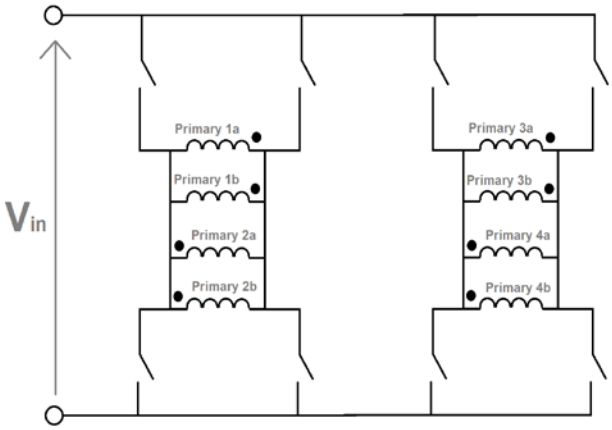

Figure 9. Diagram of the primary circuit for a four stack ICT.

6 POSSIBLE FUTURE DEVELOPMENT

It has been shown that an ICT can be used to produce 500 kV AC, which can then be doubled and rectified to produce 1 MV DC. It has also been shown that several of these ICTs can be connected in parallel to, theoretically, achieve any output current. Thus, a power supply, based on CTT, could be constructed to produce 2 A at 1 MV.

In order to evaluate whether this technology is suitable for future development, with the aim of creating a 5 MV power supply, the process that was carried out in Section 2 was extended to ICTs of up to 100 pairs of cores. Once again, the minimum normalized flux linkage in each model, calculated using FEA, was recorded and plotted in Figure 10.

From Figure 10, it can be seen that the minimum system flux drops significantly as the stack height is increased. Using the system parameters listed in Section 2, there is expected to be roughly 40% flux loss in the HV secondary windings of a 1 MV stack. Although this flux loss could conceivably be

compensated for by having more windings around the higher voltage cores, given the exponential decline of flux linkage in higher stacks, it is unlikely that this technique could practically be applied to a 2.5 MV ICT.

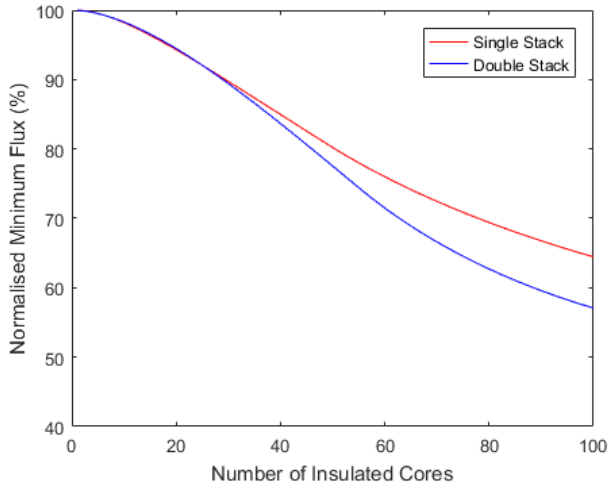

Figure 10. The minimum flux found in ICTs, arranged using both the traditional double stack layout and the proposed single stack layout, with a number of insulated cores ranging from 1 to 100.

7 CONCLUSIONS

The effectiveness of ICTs in producing 500 kV, which can then be rectified and doubled using voltage doublers, has been evaluated, as well as a number of ways of reducing flux loss. It can be concluded that ICTs may be used as the basis of a 1MV power supply that produces currents in the order of hundreds of milliamps. It was then shown, in Section 5, that by connecting multiple ICTs in parallel, the design could be expanded to produce outputs of an Ampere or more, with little voltage ripple. To meet the requirement of minimal stored energy, it is necessary to design a primary excitation source capable of switching mains voltages (e.g. 400 V) at frequencies of 100 kHz or higher. This in turn has the effect of negating some of the advantages of using the flux compensation capacitors as the primary waveform is very likely to be non-sinusoidal.

Finally, it has been shown that, although ideal for a 1 MV power supply, ICT technology is currently not suitable to be scaled up to 5 MV. Further work will focus on investigating other promising technologies. It is possible that an ideal solution would be a combination of ICTs and another technology, for example the cascade transformer.

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