

# An electrical characterisation methodology for identifying the switching mechanism in TiO<sub>2</sub> memristive stacks

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## Abstract:

Resistive random access memories (RRAMs) can be programmed to discrete resistive levels on demand via voltage pulses with appropriate amplitude and widths. This tuneability enables the design of various emerging concepts, to name a few: neuromorphic applications and reconfigurable circuits. Despite the wide interest in RRAM technologies there is still room for improvement and the key lies with understanding better the underpinning mechanism responsible for resistive switching. This work presents a methodology that aids such efforts, by revealing the nature of the resistive switching through assessing the transport properties in the non-switching operation regimes, before and after switching occurs. Variation in the transport properties obtained by analysing the current-voltage characteristics at distinct temperatures provides experimental evidence for understanding the nature of the responsible mechanism. This study is performed on prototyped device stacks that possess common Au bottom electrodes, identical TiO<sub>2</sub> active layers while employing three different top electrodes, Au, Ni and Pt. Our results support in all cases an interface controlled transport due to Schottky emission and suggest that the acquired gradual switching originates by the bias induced modification of the interfacial barrier. Throughout this study, the top electrode material was found to play a role in determining the electroforming requirements and thus indirectly the devices' memristive characteristics whilst both the top and bottom metal/oxide interfaces are found to be modified as result of this process.

**Keywords:** RRAM, TiO<sub>2</sub>, Resistive Switching, Switching Mechanism, interfacial Schottky barrier

## Introduction

Resistive Random Access Memories (RRAM) are two terminal devices that can support a multitude of resistive memory levels in a non-volatile fashion, triggered by an appropriate electrical stimulus<sup>1,2</sup>. This unique feature, also referred to as resistive switching (RS), along with the technology's potential to co-integrate RRAM cells with conventional semiconductor devices sparked a great interest in this field over the past decade. The potential of RRAM technology is thought to be fulfilled by enabling reconfigurable<sup>3,4</sup> and neuromorphic systems<sup>5,6</sup> towards establishing a new era in electronics technologies. The state-of-art in this field is also summarized in several topical reviews<sup>7,8</sup>. It is therefore timely to study and develop in more depth techniques and methodologies that allow us shining more light in the physical mechanism underpinning RS effects. This is essential for maturing this technology<sup>9</sup> and to achieve performance optimization and reliability towards realization of commercial applications.

RS effects appear to depend upon various parameters including the active area material, the metal electrodes employed and the electroforming process that is typically required in most of the RRAM technologies reported to date. RS can be categorized in different ways. A macroscopic approach based on considering the polarity of the external stimulus that “sets” and “resets” a switching effect, referred to as bipolar or unipolar RS when opposite or identical polarity stimulus is respectively required<sup>10</sup>. If a more physics view is employed, RRAM technologies can be identified as i) electrochemical metallization cells (ECM) where RS relies upon the dissolution of an active electrode typically Ag or Cu<sup>11</sup>, ii) valence change memories (VCM) where redox reactions lead to changes in the conductivity of the metal-oxide (MO) film<sup>11</sup>, iii) thermochemical (TCM) in which RS is a result of a fuse/anti-fuse process due to current-induced temperature variation<sup>11</sup> and iv) interfacial, arising by the modification of the potential barrier at metal electrode/core film interface<sup>12</sup>.

While the nature of the switching mechanism can be directly studied by laborious physicochemical characterisation techniques<sup>13</sup>, indirect approaches employing electrical characterization of RRAM prototypes can be rather beneficial due to their ease of use. This can be particularly useful in the case of interfacial mechanisms, where prompting the nature of nanoscale materials does not necessarily provide relevant information; certainly not with ease. RRAM devices typically exhibit a non-switching regime up to a certain threshold that onsets the switching process. When such technologies are operated within their switching regime, the nature of the RS mechanism has been reported to obey several operational characteristics such as

abrupt or smooth/gradual transition from the High Resistive State (HRS) to the Low Resistive State (LRS), area dependent/independent current magnitude and linear/non-linear current voltage (I-V) characteristics to name a few. Recently, we demonstrated how the analysis of the I-Vs obtained at different temperatures can help with extracting signature plots that shine more light on the conduction mechanisms responsible for the transport at distinct resistive levels<sup>14</sup>. Inspired by this, the present paper introduces a methodology for extracting the switching mechanism nature of TiO<sub>2</sub> RRAM cells by analysing the temperature dependence of their I-V characteristics in their non-switching regime, just before (after) a switching event takes place. Our methodology is validated with RRAM cells having common gold (Au) bottom electrodes (BE), identical TiO<sub>2</sub> active area films and three distinct top metal electrodes namely gold (Au), nickel (Ni) and platinum (Pt). The top electrode (TE) material has been found to play important role on the electrical properties of these stacks in their pristine state<sup>15</sup>. Although hysteresis loops may be obtained in this state as well, they are more associated with mobile ions following the sweeping rate rather than with RS effects as those studied in this work. Nevertheless, the electrode materials may also affect even the post-electroforming<sup>16</sup> electrical response of the device thus is a parameter to be considered.

## **Methodology**

Application of electrical stimulus on RRAM cells onsets the RS effect. In order for this to take place and depending on the materials of the stack under investigation a threshold limit is needed to be reached. Identifying this limit that separates the switching from the non-switching operation regimes is the first step for our experimental methodology. This is performed by leveraging the capabilities of our in-house memristor characterization platform ArC ONE<sup>17</sup> and by following the algorithm described in details in <sup>18</sup>. Specifically, a sequence of programming pulses is applied and the normalized change in the resistive state is recorded after the application of a fixed number of pulses. Data resulting from this process are presented in Figures 1 (a), where apart from a bipolar RS type, it can be observed that a range of biases do not cause any change in the resistive state (highlighted by the red rectangle), defining the non-switching operation regime. An I-V curve is then recorded in a loop mode, eliciting stimulating pulses within the switching regime (Figure 1(b)). Notwithstanding, this paper only focuses in analysing results acquired within the range of biases corresponding to the non-switching regime. We argue that analysing the mechanism responsible for the transport before the

device reach the switching regime and just after this, remaining always in the non-switching area thus under equilibrium, it would be possible to conclude on the nature of the RS. As most of the conduction mechanism responsible for the transport in semiconductors and wide band gap materials exhibit both field and temperature dependence<sup>19</sup>, we opt recording the corresponding I-V curves of our samples over a range of temperatures. This allows separating between conduction mechanisms following similar dependencies<sup>19,20</sup> and thus to minimize misinterpretations.

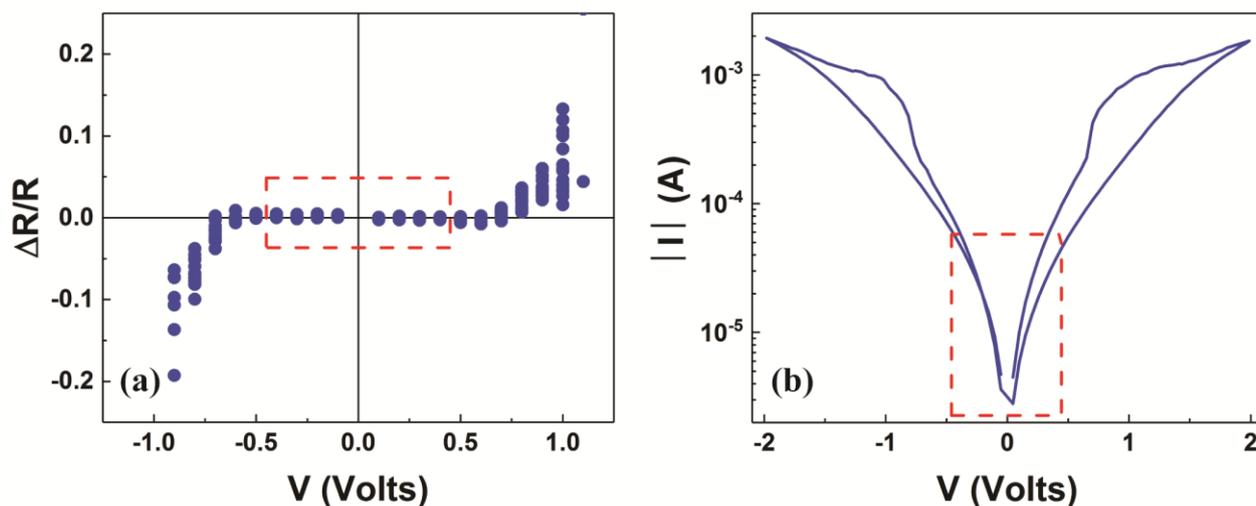


Figure 1: (a) Normalized change in the device resistive state as result of a sequence of applied pulses. The red rectangle defines the non-switching regime, i.e. the limit under which the stimulus bias does not affect the resistive state. (b) I-V curve showing RS behaviour. The non-switching regime (red rectangle) is defined by Fig. 1(a) and indicates where the analysis should be focused.

## Experimental Results

All samples employed in this work require an initial electroforming step in order to reveal their memristive character. Typically the electroforming of RRAM cells is performed by driving the device to a soft-breakdown and protecting them by using a current compliance<sup>21</sup>. This procedure has been successfully applied in similar stacks in the past<sup>22</sup>, however presently our electroforming protocol is based upon a pulsing-based, compliance free, procedure<sup>14</sup>. This is achieved by applying pulses of increasing amplitude and duration until the device resistance reaches a predetermined resistance level (Figure S1 in the supplementary material). This protocol has been proven to be gentler with respect to the typical current compliance based one, possibly due to the ability of our characterisation instrument ArC ONE to respond promptly, i.e. minimizing the induced damage.

For this specific study and in order to be able to have some comparative outcomes, all prototype samples were formed by identical procedures with their parameters summarized in Table I. As presented, all the devices can be formed using pulses having amplitudes ranges from 8 V to 12 V, but different durations are required for each one of them. Devices having Au TE require 1 $\mu$ sec pulses for forming, while in the case of Pt or Ni TE, 500 – 750  $\mu$ secs and 1 msec are required respectively. This is in straightforward correlation with the interface barriers obtained on pristine devices<sup>15</sup>. More specifically, the lower the barrier in the pristine state the longer pulse duration is required to form the stack, possibly to its ability to adapt due to the higher conductivity. It is worth mentioning that the applied protocol allows for discrete devices to attain the same resistive levels, showing very similar I-V characteristics, particularly in the their non-switching operation regime (Figure S2 in the supplementary material).

	<i>Au</i>	<i>Pt</i>	<i>Ni</i>
<b>Starting voltage (V)</b>	<b>8</b>	<b>8</b>	<b>8</b>
<b>Voltage step (V)</b>	<b>0.1</b>	<b>0.1</b>	<b>0.1</b>
<b>Up to ending voltage (V)</b>	<b>12</b>	<b>12</b>	<b>12</b>
<b>Number of pulses per bias</b>	<b>200</b>	<b>200</b>	<b>200</b>
<b>Pulse width (<math>\mu</math>sec)</b>	<b>1</b>	<b>500-750</b>	<b>1000</b>
<b>Series resistance</b>	<b>no</b>	<b>no</b>	<b>no</b>

Table I: Conditions of the pulsing-based compliance free protocol applied to the devices through ArC ONE.

Following from this initial step, all the devices reached stable operation condition, showing clearly distinguishable resistive states (Figure S3 in the supplementary information). These, apart from using the switching IVs sweeps are also attained successfully by stimulus pulses of the opposite polarity (Figure S4 in the supplementary information). I-V characteristics were then recorded in the temperature range from 300 K – 350 K that are presented in Figure 2. Devices with Ni TE are breaking down at 350 K, thus the maximum operational temperature was 340 K. Using the acquired data, the transport properties for each I-V branches before and after each RS, for positive and negative bias polarities, were analysed, ensuring that the samples

remain within their non-switching regimes by employing biases with amplitudes lower than 0.5 V. At this point it is important to clarify that the transport properties are strongly related to the operation temperature. Therefore our analysis provides related information for the applied range of temperatures only. Studies employing measurements in wider temperature range<sup>23</sup> may reveal different character regarding the device electrical behaviour and/or even their ability for RS.

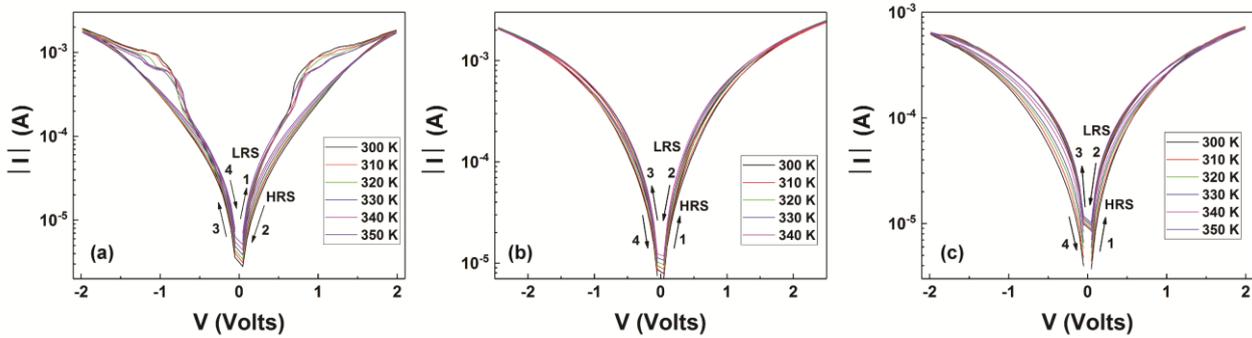


Figure 2: Extracting the transport properties requires recording of the I-Vs at different temperatures up to bias level that ensures RS. Three stacks with different TE studied in this work (a) Au/TiO<sub>2</sub>/Au, (b) Au/TiO<sub>2</sub>/Ni and (c) Au/TiO<sub>2</sub>/Pt. The arrows indicate the sweeping sequence, while the HRS/LRS levels should be considered only in the non-switching regime.

The Metal-TiO<sub>2</sub>-Metal stacks studied in this work can be equivalently modelled with a series combination of elements for the two interfaces and the active area, allowing us to extract the transport properties in their non-switching regimes. The overall dominant conduction mechanism is primarily determined by the most resistive one<sup>15,24</sup>. For a core-area dependent controlled transport (thus in the absence of interfacial barriers or if these are negligible), I-V curves should be symmetric with respect to the bias polarity. When the interfaces dominate the transport, asymmetric characteristics are expected<sup>25</sup>. This is a first indication useful for assessing the signatures supporting the dominant conduction mechanism. A second critical factor is the temperature dependence.

All the stacks studied in this work exhibit asymmetric and temperature activated characteristics. Considering the possible conduction mechanism<sup>19</sup> this appears to be transport dominated by Schottky emission over the interfacial barriers.

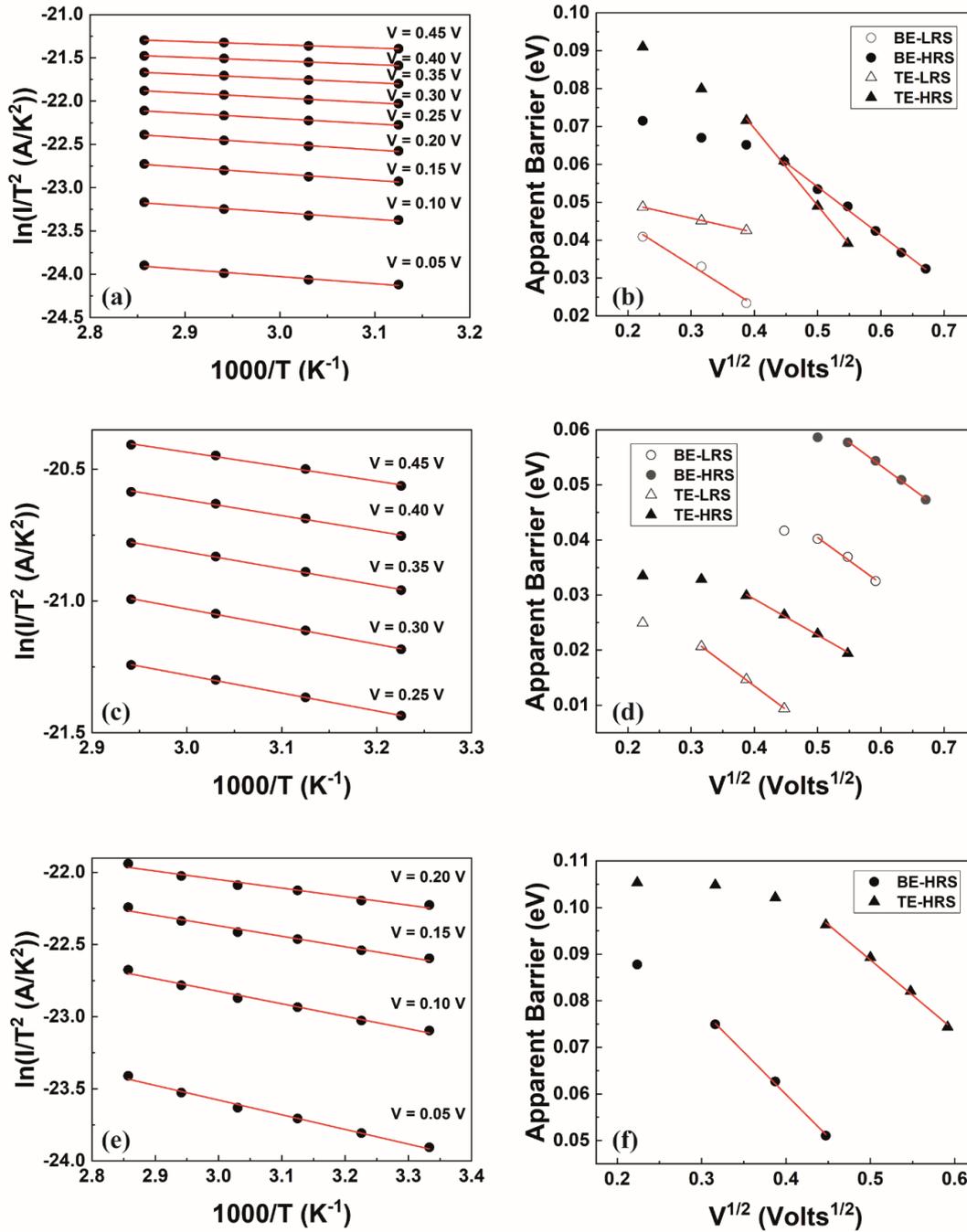


Figure 3: (a), (c) and (e) are signature plots confirming the validity of equation 1 for the HRS branch correspond to the positive bias polarity of the I-V (see supplementary for the signature plots correspond to the other I-Vs branches), thus supporting interface controlled transport, for Au, Ni and Pt TE respectively. (b), (d) and (f) additional signature plots generated by the previous ones and indicating modulation of the interfacial barrier further supporting the interface controlled transport for all the I-V branches of Au, Ni and Pt TE respectively.

For evaluating this it is essential to extract the so-called signature plots, which is a characteristic field and temperature dependence that uniquely defines a conduction mechanism. Schottky emission is described by Equation 1<sup>19</sup>:

$$I = AT^2 e^{-\frac{q(\Phi_{B0} - \alpha\sqrt{V})}{KT}} \quad (1)$$

Where A = (area x Richardson constant),  $\alpha$  the barrier lowering factor, T the absolute temperature, K the Boltzmann constant, q the electron charge and  $\Phi_{B0}$  the potential barrier at the interface under zero applied bias.

<i>Au</i>		
$\Phi_{B0}$ (eV)	BE	TE
HRS	0.117	0.151
LRS	0.065	0.057
<i>Ni</i>		
$\Phi_{B0}$ (eV)	BE	TE
HRS	0.104	0.055
LRS	0.085	0.048
<i>Pt</i>		
$\Phi_{B0}$ (eV)	BE	TE
HRS	0.133	0.164
LRS	Very low	Very low

Table II: Post electroforming interface barrier heights extracted by the temperature analysis of the I-Vs in the non-switching regimes.

Therefore, by plotting  $\ln(I/T^2)$  vs  $1000/T$ , while ensuring applied biases maintain a non-switching regime, a linear relation is expected, where the slope corresponds to the apparent effective barrier ( $\Phi_{B0} - \alpha\sqrt{V}$ ) under each specific electric field<sup>15,24</sup>, as depicted in Figures 3 (a), (c) and (e). Moreover, we note that the apparent effective barrier should decrease by increasing the applied electric field as:

$$\Phi = \Phi_{B0} - \alpha\sqrt{V} \quad (2)$$

and thus a plot of the apparent barrier calculated from the slope versus  $V^{1/2}$  should obey a linear relation. If both these signatures are satisfied then the intercept of the last plot corresponds to the potential barrier at the interface under zero applied bias<sup>15,24</sup> (Figure 3 (b), (d) and (f)). Further to this and for the range of biases where the two plots described above are confirmed, bearing in mind equation 1, a straight line is also expected if the I-V curve at a specific temperature is plotted in  $\ln(I)$  vs  $V^{1/2}$  plot (Fig. S6 to Fig. S9 in the supplementary material). The analysis for the different stacks is presented in Figure 3 and at the supplementary information, supporting our findings for an interface-controlled transport in all cases. Regarding the LRS states in case of Pt TE, these appear to be temperature activated showing marginal asymmetry, indicating also an interface controlled transport but without being possible to extract clear signature plots. Such behaviour may be attributed to very low interface barriers and a boundary case towards a core material controlled transport (i.e. purely symmetric I-V).

## Discussion

The analysis of the transport properties in the non-switching regimes, before and after switching effects, supports for all the cases studied in this work (all branches of the I-V curves) the existence of an interface controlled transport due to the presence of potential barriers at the TE or BE/TiO<sub>2</sub> interfaces. Under this perspective the read-out resistance is a result of a reverse biased Schottky contact, corresponding to the bottom interface for positive biases and to the top one for negative polarities (Figure 4).

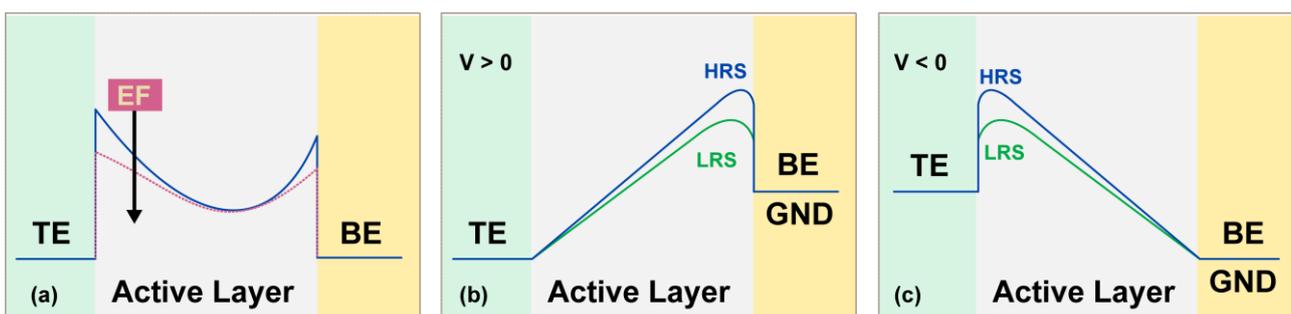


Figure 4: (a) A schematic diagram showing the potential barrier at the top and bottom interface for a pristine and an electroformed (EF) device. (b) Application of positive bias on the TE results in a forward biased Schottky contact at the top interface and a reverse biased one at the bottom interface. The barrier height is modulated during the sweep resulting in two different resistive states (LRS/HRS). (c) The situation is reverse when a negative bias is applied at the TE.

Our analysis also revealed different barrier heights for the various branches of the I-V assessed in the non-switching regime, suggesting that driving the device through the switching regime results in modulation of the height for the dominant (each time) interfacial barrier; thus, the read-out resistance changes denoting an interfacial RS mechanism. This is also supported by the gradual “set” and “reset” processes in contrast to abrupt changes expected in cases where conductive filaments are formed and ruptured. The calculated barrier (Table II) in this case is an effective one. Modifying this barrier by external electrical stimulus results in RS. Therefore for an interfacial type RS it is not necessary to obtain a uniform area dependence; although can be in support of this case. Moreover, the fact that the transport is controlled by the interfaces does not allow to further assess the properties of the core-film. Thus there is not enough evidence for commenting on possible changes in the MO microstructure as a result of the electrical stimulus (considering purely electrical measurements). Finally, considering equation (2) and the barrier lowering factor  $\alpha$ , highlights the importance for the choice of the read-out voltage for characterizing and implementing in circuits interfacial type devices. Regarding the electrical stimulus and the reasons that modulate the barrier at the interface, this could stem from different origins. From the electronic point of view, modulation of the barrier is a result of changes in the charge existing at the interface and the depleted area of the reverse biased Schottky contact. This can be attributed to the migration of ions and/or cations<sup>12,26</sup>. Additionally, redox reaction<sup>27</sup> may result in changes of the ionic concentration at the vicinity of the interface. A third reason could be electronic trapping/de-trapping at states existing at the interface or close to it. The latter one is a parameter that favours engineering towards bespoke modification of the barrier rendering interfacial RS devices as a potential candidates for applications require analogue behaviour. Separating these contributions to the interfacial barrier and particularly for an amorphous material it is not a straightforward task however, and requires thorough studies by multiple characterization techniques applied in parallel.

Considering also the pristine state of the devices<sup>15</sup> and the electroforming process, no straightforward correlation to the post-forming RS is revealed. Despite that there are some interesting observations worth to be discussed. As a result of the electroforming process, both the top and bottom interfacial barriers are modified. Bearing in mind that in our case only positive polarity pulses applied, this indicates that it is most probably the film electronic properties rather than just the reverse biased interface that is affected by the forming protocol. These changes in the electronic properties of the film (e.g. by generated oxygen vacancies) result also in the reduction of the interfacial barriers at the post forming condition. Further to this and despite

any straightforward correlation to the pristine barrier has not been revealed, the latter appears to determine the electroforming conditions, in our case the required pulse duration, and thus the post-forming characteristics. Thus we may comment as a proof of concept evidence that proper selection of the TE metals may tune the forming process towards specific post-forming characteristics, although at the present state this should be considered as just a preliminary indication.

Finally we would like to add some thoughts regarding the I-V curves beyond the non-switching regime. Devices having Ni and Pt as TE, exhibit a typical bipolar character. As indicated in Figure 1(a), devices with Au TE exhibit bipolar switching behaviour, as well, suggesting resistance increase when positively biased. However the shape of the IV characteristic also resembles quite well that of complementary switching. Complementary RS takes place when two bipolar stacks are connected back to back<sup>28</sup> and has been also demonstrated for single stacks having an internal metallic nanolayer<sup>29, 30</sup>. This however is not the case for our stacks. We believe that understanding the electrical response of devices operate with interfacial RS mechanisms, outside the non-switching regime is not straightforward. The macroscopically obtained current conduction in this case is affected by the change in the dominant transport parameter from a reverse polarised Schottky to the opposite forward one (due to Schottky effect that diminishes the barrier) including effects of transient transports, due to trapping/de-trapping and/or ionic motions, notwithstanding the sweep characteristics. This is the major point of the proposed methodology. Understanding the induced modification required assessment in the non-switching operation regime just before and after switching occurs. Therefore the HRS/LRS should be considered only in this regime (Figure 2).

## **Conclusions**

A methodology for revealing the nature of RS mechanism by analysing the transport properties of RRAM cells in their non-switching regime is presented. A pulsing based algorithm was initially applied in order to identify the switching/non-switching stimulus range. Afterwards the I-V characteristics were recorded and analysed at different temperatures considering both their field and temperature dependence along with additional features such as their symmetric/asymmetric response with respect to the applied bias polarity. The study presented in this work was focused on TiO<sub>2</sub> based devices having identical Au BE, active area films and three discrete TE, Au, Ni and Pt. Signatures

supporting transport controlled by the interfacial barriers extracted for all the cases, indicating RS due to bias induced modification of the interfacial barriers. Moreover although no straightforward correlation obtained for the different TE or with respect to the pristine state interface barriers there some indications that this is critical for the electroforming requirements and thus might indirectly affect the device RS characteristics. Finally the features of interfacial type RS have also been discussed.

## **Methods**

### **Device Fabrication**

The devices implemented in this work were fabricated on the same six-inch Si wafer having a 200 nm thick SiO<sub>2</sub> layer that was grown by dry oxidation at 1000°C with 5 slm O<sub>2</sub> flows. All electrodes and active areas were patterned via standard optical lithography and liftoff processes<sup>31</sup>. A common BE metal was utilized, Au, with a thickness of 20 nm preceded by 5 nm Ti adhesive layer. The 24 nm active film, an amorphous TiO<sub>2-x</sub>, was deposited on top of Au BE by Lambda controlled plasma assisted reactive magnetron sputtering (Helios Pro XL, Leybold optics) using a Ti target, with 8 sccm O<sub>2</sub>, 35 sccm Ar flows and 2 kW at the cathode, and 15 sccm O<sub>2</sub> flow and 2 kW at an additional plasma source. This industrial tool allows having high quality films with low thickness variations across the wafer. Using “Woolham Ellipsometer MC05” TiO<sub>2-x</sub> thickness across six-inch wafer was found to be of  $24.1 \pm 0.27$  nm. Films deposited by the above recipe exhibit an amorphous and almost stoichiometric nature of TiO<sub>2-x</sub>, with x in the range of 0.05-0.10, as previously demonstrated in the X-ray absorption spectroscopy study<sup>22</sup>. For the TEs, three separate areas were defined to deposit different TE metals: Au, Ni, and Pt, with thicknesses of 15 nm deposited by electron beam evaporation at a low rate of 0.5 Ås<sup>-1</sup>, comparable to deposition rate of the BE.

### **Electrical Characterisation**

The current vs voltage (I-V) characteristics were obtained on  $20 \times 20 \mu\text{m}^2$  devices using our in-house memristor characterization platform ArC ONE. The voltage sweeping was carried out always towards positive biases, while both positive and negative polarities were always applied to the TE with respect to the BE that was continuously kept grounded. All experiments were performed on a Cascade SUMMIT 12000B semi-automatic probe station that incorporates a thermal chuck, whose temperature can be controlled by an ESPEC ETC-200L

unit. Measurements were performed in the temperature range of 300 K to 350 K. The discontinuity appearing at  $V=0$  V in some I-V curves is a result of our data acquisition system that does not acquire this point. This effect is negligible in most of the cases but not when measuring more conductive samples and for higher temperatures (340K-350K) when the conductivity/current further increases. However this has no effect on the measured data. Finally it is worth mentioning the role of moisture which was reported to affect both the transport and switching properties of devices based on sputtered oxide films<sup>32</sup>. Bearing this in mind our experimental procedure was performed on environment where humidity and temperature were carefully controlled. Nevertheless this effect hasn't shown significant influence in case of TiO<sub>2</sub> layers<sup>33</sup>.

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### **Author Contribution**

L.M and T.P planned the experiments, L.M. performed the electrical characterization and analysed the results. A.K and S.S. optimised the processes and fabricated the samples. L.M. wrote the manuscript. T.P. A.K. and S.S. provided useful suggestions for improving it.

### **Additional Information**

**Competing Interests:** The authors declare that they have no competing interests

### **Data availability**

All data supporting this study are openly available from the University of Southampton repository at:

<https://doi.org/10.5258/SOTON/D0930>

### **References**

1. Kim, W. *et al.* Multistate Memristive Tantalum Oxide Devices for Ternary Arithmetic. *Sci. Rep.* **6**, 36652 (2016).
2. Stathopoulos, S. *et al.* Multibit memory operation of metal-oxide Bi-layer memristors. *Sci. Rep.* **7**, 17532 (2017).
3. Edwards, A. H. *et al.* Reconfigurable memristive device technologies. *Proc. IEEE* **103**, 1004–1033 (2015).
4. Zidan, M. *et al.* Field-Programmable Crossbar Array (FPCA) for Reconfigurable Computing. *IEEE Trans. Multi-Scale Comput. Syst.* **7766**, 1–13 (2017).

5. Serb, A. *et al.* Unsupervised learning in probabilistic neural networks with multi-state metal-oxide memristive synapses. *Nat. Commun.* **7**, 12611 (2016).
6. Mehonic, A. & Kenyon, A. J. Emulating the electrical activity of the neuron using a silicon oxide RRAM cell. *Front. Neurosci.* **10**, 57 (2016).
7. Pan, F., Gao, S., Chen, C., Song, C. & Zeng, F. Recent progress in resistive random access memories : Materials , switching mechanisms , and performance. *Mater. Sci. Eng. R* **83**, 1–59 (2014).
8. Gao, S. *et al* Organic and hybrid resistive switching material and devices. *Chem Soc.Rev.* **48**, 1531 (2019).
9. Adam, G. C., Khiat, A. & Prodromakis, T. Challenges hindering memristive neuromorphic hardware from going mainstream. *Nat. Commun.* **9**, 5267 (2018).
10. Waser, R. & Aono, M. Nonoionics-based resistive switching memories. *Nat. Mater.* **6**, 833 (2007).
11. Valov, I. Interfacial interactions and their impact on redox- based resistive switching memories (ReRAMs) *Semicond. Sci. Technol.* **32**, 093006 (2017).
12. Yang, J. J. *et al.* Memristive switching mechanism for metal/oxide/metal nanodevices. *Nat. Nanotechnol.* **3**, 429–433 (2008).
13. Yang, Y. & Huang, R. Probing memristive switching in nanoionic devices. *Nat. Electron.* **1**, 274 (2018).
14. Michalas, L. *et al.* Conduction mechanisms at distinct resistive levels of Pt / TiO<sub>2-x</sub> / Pt memristors *Appl. Phys. Lett.* **113**, 143503, (2018).
15. Michalas, L., Khiat, A., Stathopoulos, S. & Prodromakis, T. Electrical characteristics of interfacial barriers at Metal - TiO<sub>2</sub> contacts. *J. Phys D: Appl. Phys.* **51**, 425101, (2017).
16. Kim, W.-G. & Rhee, S.-W. Effect of the top electrode material on the resistive switching of TiO<sub>2</sub> thin film. *Microelectron. Eng.* **87**, 98–103 (2010).
17. Berdan, R. *et al.* A  $\mu$ -Controller-Based System for Interfacing Selectorless RRAM Crossbar

- Arrays. *IEEE Trans. Electron Devices* **62**, 2190–2196 (2015).
18. Serb, A., Khiat, A. & Prodromakis, T. An RRAM Biasing Parameter Optimizer. *IEEE Trans. Electron Devices* **62**, 3685–3691 (2015).
  19. S.M., S. & K.K., N. *Physics of Semiconductor Devices*. (John Wiley & Sons, 2006).
  20. Michalas, L., Koutsourelis, M., Papandreou, E. & Papaioannou, G. Electrical Characterization of Undoped Diamond Films for RF MEMS Application. *IEEE Intern. Reliabil. Phys. Sympos.* **6B** 3.1 (2013).
  21. Cao, X. *et al.* Effects of the compliance current on the resistive switching behavior of TiO<sub>2</sub> thin films. *Appl. Phys. A Mater. Sci. Process.* **97**, 883–887 (2009).
  22. Carta, D. *et al.* X-ray absorption spectroscopy study of TiO<sub>2-x</sub> thin films for memory applications. *J. Phys. Chem. C* **119**, 4362–4370 (2015).
  23. Voronkovskii, V.A. *et al.* Conduction mechanisms of TaN/HfO<sub>x</sub>/Ni memristors. *Mat. Res. Express* **6**, 076411, (2019).
  24. Michalas, L. *et al.* Interface asymmetry induced by symmetric electrodes on metal-Al:TiO<sub>x</sub>-metal structures. *IEEE Trans. Nanotechnol.* **17**, 867 (2018)
  25. Pintilie, L., Vrejoiu, I., Hesse, D., LeRhun, G. & Alexe, M. Ferroelectric polarization-leakage current relation in high quality epitaxial Pb (Zr,Ti) O<sub>3</sub> films. *Phys. Rev. B - Condens. Matter Mater. Phys.* **75**, 1–14 (2007).
  26. Wedig, A. *et al.* Nanoscale cation motion in TaO<sub>x</sub>, HfO<sub>x</sub> and TiO<sub>x</sub> memristive systems. *Nat. Nanotechnol.* **11**, 67–74 (2016).
  27. Schönhals, A. *et al.* Role of the Electrode Material on the RESET Limitation in Oxide ReRAM Devices. *Adv. Electron. Mater.* **4**, 1700243 (2018).
  28. Linn, E., Rosezin, R., Kügeler, C. & Waser, R. Complementary resistive switches for passive nanocrossbar memories. *Nat. Mater.* **9**, 403–406 (2010).
  29. Gao, S. *et al.* Implementation of Complete Boolean Logic Functions in Single Complementary Resistive Switch. *Sci. Rep.* **5**, 15467 (2015)

30. Gao, S. *et al.* Tuning the switching behavior of binary oxide- based resistive memory devices by inserting an ultra-thin chemically active metal nanolayer : a case study on the Ta<sub>2</sub>O<sub>5</sub> – Ta system. *Phys. Chem. Chem. Phys.* **17**, 12849–12856 (2015).
31. Serb, A., Khiat, A. & Prodromakis, T. Seamlessly fused digital-analogue reconfigurable computing using memristors. *Nat. Commun.* **9**, 2170 (2018).
32. Lübben, M., Wiefels, S., Waser, R. & Valov, I. Processes and Effects of Oxygen and Moisture in Resistively Switching TaO<sub>x</sub> and HfO<sub>x</sub>. *Adv. Electron. Mater.* **4**, 1700458, (2017).
33. Tsuruoka, T. *et al.* Effects of moisture on the switching characteristics of oxide-based, gapless-type atomic switches. *Adv. Funct. Mater.* **22**, 70–77 (2012).