Practical Implementation of Digital In-Analogue Out Memristor-based Threshold Logic Circuit

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An important aspect for implementing neuro-inspired circuits and systems is the data pattern recognition and classification circuits. Memristor is one of the most prominent emerging technology to take effectively the place of synaptic weights, in neuro-inspired techniques such as Threshold Logic (TL) [1], by showcasing continuously tunable resistance capabilities [2]. The design and experimental validation of such circuits, by taking into consideration the practical non-linearities of the memristor components, is worth investigating. The introduction of Digital In- Analogue Out (DI-AO) memristive TL will enable us to complete the picture of the available circuit modalities that can process information using memristors, by additionally taking into consideration the more conventional digital [3], analogue [4] and Analogue In-Digital Out (AI-DO) memristor-based logic families [1].

In this work, a DI-AO method of performing reconfigurable memristor-based TL is proposed and experimentally validated using real memristor devices and incorporating 1T1R-based mixed-signal circuit modalities, to compute physically (Kirchhoff's law at the intermediate node) the comparison between two adverse dot-products, one pulling towards V_{DD} and the other pulling down to GND (see Fig.1). Hence, the computation is equivalent to a digital in (MOS gate control) – analogue out (readout voltage from the intermediate node) TL operation. The circuit performs the TL operation physically in the form of distance of the readout circuit response from $V_{DD}/2$ voltage level. An example of the experimental validation of the circuit is presented in Fig. 2, where the pull-up (PU) pMOS and pull-down (PD) nMOS vectors are defined as {Ip11, Ip12, Ip13} and {In21, In22}, respectively. The memristor weights [2] used for this configuration are configured as{5.5kΩ, 10.8kΩ, 11.5kΩ} and {7.3kΩ, 6kΩ}, for the PU and the PD arrays, respectively.

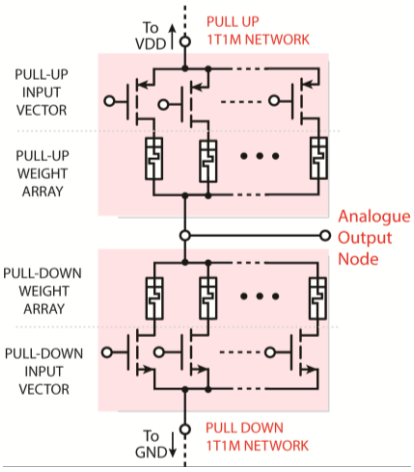

Figure 1: Circuit consists of two weighted vectors are compared physically through intermediate node current sensing.

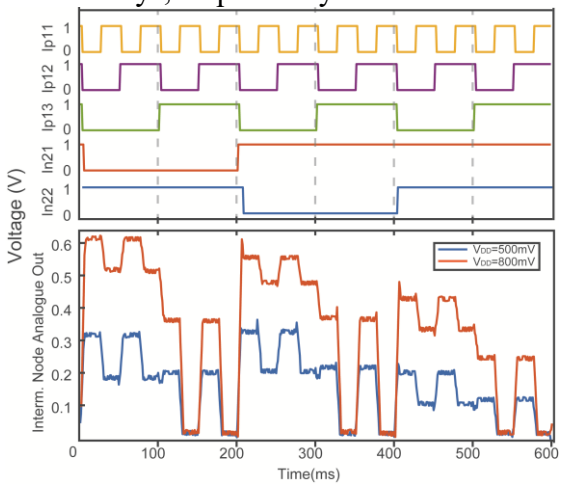

Figure 2: Input control for the PU and PD vectors and the analogue output of the circuit is also presented for two different V_{DD} cases (blue: 500mV, orange: 800mV).

References

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