Integrating flexible filament circuits for e-textile applications

Abiodun Komolafe, Russel Torah, Yang Wei, Helga Nunes-Matos, Menglong Li, Dorothy Hardy, Tilak Dias, Michael Tudor and Stephen Beeby*

Dr. A Komolafe, Dr. R. Torah, Mrs. H. Nunes-Matos, Dr. M. Tudor, Prof. S. Beeby
Dept. of Electronics and Computer Science
University of Southampton, Highfield Campus
SO17 1BJ, United Kingdom
Email: a.o.komolafe@soton.ac.uk

Dr. Y Wei
School of Science and Technology
Nottingham Trent University

Dr. M. Li
School of Materials
University of Manchester, United Kingdom.

Dr. D. Hardy, Prof. T. Dias
Advanced Textiles Research Group
Nottingham Trent University, United Kingdom.

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Abstract: Practical wearable e-textiles must be durable and retain as far as possible, the textile properties such as drape, feel, lightweight, breathability and washability that make fabrics suitable for clothing. Early e-textile garments were realized by inserting standard portable electronic devices into bespoke pockets and arranging interconnects and cabling across the garment. In these examples, the textile merely served as a vehicle to house the electronics and had no inherent electronic functionality. Reduction in electronic component size, the development of flexible circuits and the ability to weave robust interconnects offer the potential for improved levels of electronic integration within the textile. This paper introduces the weaving of electronic circuit filaments less than 2 mm wide into fabrics such that the electronics are fully concealed in the textile and given extra protection by the surrounding textile fibers. The failure mechanisms for different filament circuit designs before and after integration into the textile are investigated with a 90° cyclical bending test. Results showed that encapsulated filament circuits embedded within the textile survive 45 washing cycles and more than 1500

cycles of 90° bending around a bending radius of 10 mm, performing 5 times better than equivalent filament circuits before integration into the fabric.

1. Introduction

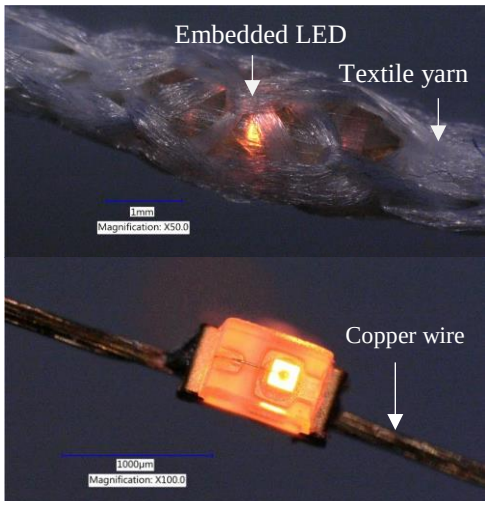
E-textiles (also known as smart fabrics) are textiles that incorporate electronic functionality. E-textile garments enable electronic systems to be mobile, personalised and accessible to users anywhere and anytime. E-textiles exploit the universality of textiles which covers all types of woven, non-woven and knitted materials/fabrics used in a huge variety of applications from clothing (e.g. fashion, workwear and protective clothing), interior design (e.g. upholstery and carpets), agriculture (e.g. crop protection), civil engineering (e.g. soil retentions and reinforcement), marine (e.g. sails, inflatables) and industry (e.g. filters, lifting/conveying). The functionalisation of clothing with electronic intelligence offers benefits in application domains including medical and healthcare, fashion, military, first responders and workwear [1, 2]. In all such applications, it is important that the functional electronics and materials are incorporated in a manner that does not significantly alter the physical properties of the fabric and, unlike previous examples, is invisible to the user. Fabrics are by their very nature highly compliant, soft and typically breathable. These properties make fabrics ideally suited for clothing but they make them a very challenging medium on, or in, which electronic functionality must be incorporated [3]. This is in addition to the reliability/durability challenges presented by the abrasive, compressive and tensile forces that the fabrics experience during normal use.

The first generation of e-textile garments involved portable conventional electronics being inserted into pockets designed into clothing specifically for that purpose. The Life shirt from Vivometrics [4] is an example of a commercialised product from 2001. In these first generation e-textiles, the textile itself played no role in the electronic functionality of the garment and the shirt itself was also heavy, uncomfortable and unaesthetic. The second generation of e-textile garments include limited electronic functionality added in the form of woven or knitted

conductive interconnects [5,6,7], electrodes [8,9] and antennas [10,11]. This generation also demonstrated e-textile prototypes that included sensing functionality such as temperature, heart rate and gas sensors developed for firefighters within the ProeTEX project [12]. Commercial second generation products such as the Adidas heart rate monitoring sports bra [13,14] have also emerged. In all such examples the electronic processing and wireless communications is performed in a conventional rigid module that snaps onto the garment and must be removed for washing. In the research domain, increased levels of electronic functionality has been demonstrated with minimal compromise on the properties of the fabric by the knitting, weaving and embroidering of coated yarns for producing 1D or thread-like electronic devices [3,15,16,17,18] and by the printing of functional materials onto the surface of the textile to realise 2-D electronics devices on fabrics [19,20,21,22,23]. The development of functional thick-film polymer inks has enabled standard high-volume printing techniques that are familiar to the textile industry to be used to integrate a wide range of electronic functionality onto the surface of the fabric [19-29]. The effect of the printed layers on the feel of the textile and its breathability can be minimised by ensuring the films are flexible, as thin as possible and only printed where required. Functionality is defined by the ink formulation and includes conductive inks for printed interconnects [24], resistive inks for resistors and strain gauges [19,25], piezoelectric inks for energy harvesting and sensing [26] and electroluminescent inks for displays [27]. The printing approach is also used to produce electronic circuits, or fabric PCBs [19,28] on which surface mount electronic components can be bonded using conductive adhesives [28,29]. However, the durability of these circuits is poor with cracks developing in the conductive inks and conductive adhesives due to mechanical forces and bending. The electronics are also still visible to the wearer and approaches for improving the durability by encapsulation only accentuates the presence of the electronics on the fabric[25,30].

The third generation of e-textiles has demonstrated increasing levels of 1D electronic integration within the fabric using flexible plastics as carrier substrates [16,31,32,33,34]. This approach benefits from the use of conventional electronic circuit fabrication techniques on flexible substrates [35]. The state of the art following this approach is detailed in [33] where periodic weft yarns of a fabric are replaced during weaving with two terminal electronic plastic strips (e-strips) that are interconnected along the warp direction of the fabric with conductive threads. The individual e-strips have been demonstrated with widths between 1 and 5 mm, and incorporating humidity and temperature sensors, thin-film sensors, and LEDs. Mounted electronics and conductive threads are attached using isotropic conductive adhesives and are protected by glob topping. The entire e-strip was encapsulated with a spray-on silicone layer and examples containing a 600 nm thick copper thin film transistors (TFTs) survived 1000 tensile bending cycles around a 10 mm bending radius [36, 37]. Woven textile swatches containing LED e-strips failed after five washing cycles at a 30 °C due to corrosion of the 18 µm thick copper tracks and flaking of the silicone encapsulation on the LEDs [32]. A further limitation of this embodiment is that the e-strips were still visible to the wearer after integration into the fabric and the effect of the fabric on the reliability of the e-strips have not been investigated. In another form of 1-D electronics integration in textiles (e-yarns), Hardy et al[38] improved the concealment of electronics into the fabric by integrating two terminal components such as LEDs and thermistors into the core of textile yarns with multi-strand copper wires as shown Figure 1a. This approach is, however, unsuitable for incorporating complex circuits that typically require multiple connections to circuits and devices. Other forms of 1-D electronics are based on using coated textile fibers to realize woven transistor/logic circuits or electrical interconnections on fabrics [39, 40] but like the 2-D printed structures, the reliability of the integrated electronics is largely dependent on the durability of the functional inks that is used to coat the textile fibers and the top layer encapsulation [41]. In addition to these durability and wearability limitations, the 1D and 2D e-textile prototypes are potential sources of e-waste that

may prove ecologically challenging to recycle or dispose if mass produced due to the contamination of the textile host by the functional inks [42, 43].



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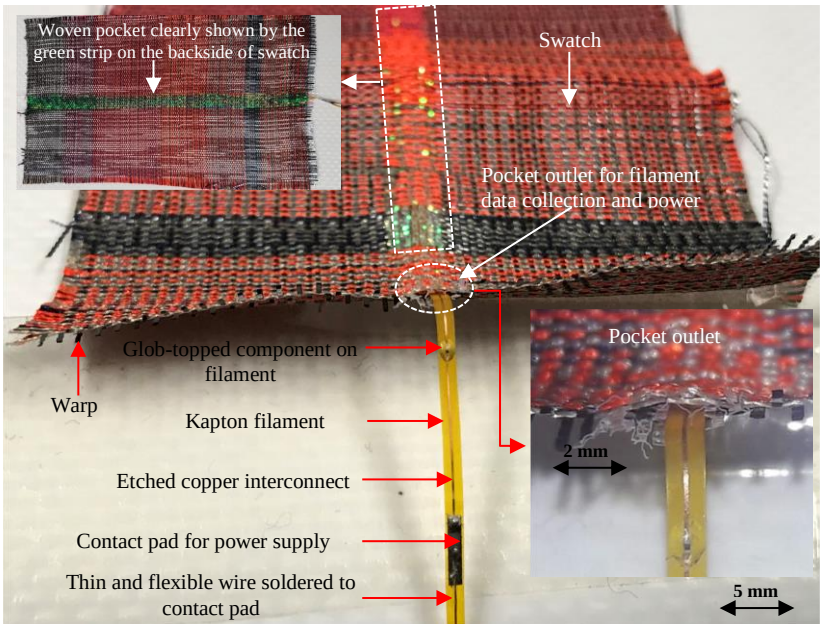


(b)

Figure 1: (a) An operational LED yarn showing the two-terminal connection of an LED inside a yarn, (b) Embedded flexible filament circuit in a textile swatch of a total thickness of 230 µm.

This paper addresses the wearability and recyclability of e-textiles using a woven approach that exploits the 1D e-strip concept to achieve flexible modular circuits in the form of filaments and extends the concept by weaving the filaments into the fabric in a manner that conceals its presence from the wearer and uses the surrounding textile fibers/yarns to offer extra protection

to the circuits. This approach locates the filament circuits in the body of the fabric during the weaving process by forming bespoke pockets within the structure of the textile as shown in Figure 1b. These pockets allow the placement of the filaments and routing of wires within the fabric in a way that has minimal impact on the feel of the fabric and undetectable by the wearer. It also ensures that the filament circuits can be easily removed and isolated from the fabric to be separately recycled or disposed as electronic waste and thereby preventing any electronic contamination of the fabric. Functioning e-textile swatches implementing components such as LEDs and microcontrollers on demonstrator filaments of widths ranging from 2 mm down to 0.8 mm have been demonstrated. The filament circuits before and after weaving were subject to a cyclical bending and washing routine to investigate the limits of conventional filament circuit design rules and the effect of the bespoke fabric pocket on the electrical and mechanical reliability of the filaments.

2. Results and discussions

2.1. Material and process selection for fabricating filament circuits

The functional flexible filament circuit shown in Figure 1b consists of a substrate, metal interconnections, electronic components, conductive adhesives or solder pastes for bonding the electronic components and underfill adhesives for improving mechanical strength. Significant research has been undertaken in order to achieve the circuit resolution necessary for integrating bare die components. Different materials, techniques for handling and mounting the components and design features have been investigated in order to maximize reliability.

2.1.1. Substrate and Adhesive selection and characterization:

Mechanical reliability is an essential consideration for practical applications of wearable e-textile due to the need to survive bending and washing and this can be influenced by the properties of the substrate material [44,45]. Components were mounted onto PEEK, Kapton and Mylar substrates using the different adhesives listed in Table 1 and were subjected to standard

shear and bending tests. The adhesives were found to fail under mechanical loads up to 200 N. The optimum material combination was found to be Masterbond EP37-3FLF with a Kapton substrate. The finite element analysis identified an optimum adhesive thickness of between 0.048 mm and 0.05 mm at which the stress induced within the adhesive due to applied forces is minimized.

Table 1: Material properties of substrates and adhesives [44]

Types	Materials	Young's Modulus (MPa)	CTE (K^{-1})	Density (gcm^{-3})	Tensile Strength (MPa)
Substrates	PEEK	3800	4.7×10^{-5}	1.32	98
	Kapton	2500	2×10^{-5}	1.42	231
	Mylar	3100	1.7×10^{-5}	1.39	138
Adhesives	Dymax 3031	100	178×10^{-6}	1.03	10
	Delo-Monopox NU355	1700	150×10^{-6}	1.1	42
	Delo-Monopox Mk055	3200	6.4×10^{-5}	1.2	50
	EP30A0	3447	25×10^{-6}	1.06	41
	EP37-3FLF	344	9×10^{-5}	1.05	35
	Epo-Tek 301 2fl	3664	56×10^{-6}	1.07	≥ 13.7
	Loctite 4902	400	425×10^{-6}	1.06	16
	Loctite 4860	430	1×10^{-4}	1.07	≥ 5
	Loctite 480	2000	8×10^{-5}	1.1	≥ 1.8

2.1.2. Substrate and Adhesive selection and characterization:

Flexible filament circuits on Kapton were fabricated using three types of metallization: screen printed silver polymer inks, evaporated thin films (gold and aluminum) and commercially available copper clad Kapton. The screen-printing process is a straightforward method for directly printing the circuit design on the Kapton using flexible conductive polymer inks. However, the bonding of electronic components onto printed inks using standard soldering is not possible due to the high temperatures involved and components can only be attached using conductive adhesives, the mechanical strength of which is inferior to solder. The minimum feature size possible with standard screens is 100 µm, which is suitable for fabricating simple electronic circuits [46]. As the circuit complexity increases, the required feature size shrinks beyond the limits of standard screen printing. Figure 2a below shows an example printed electronic filament designed to mount 0603 LED packages using isotropic conductive adhesive. The fabricated filaments functioned correctly and survived bending around a 12 mm diameter

radius. However, the adhesive was difficult to apply resulting in inconsistent contact resistances and varying illumination intensities. Such adhesives also have a short working time that is not ideal for scaling up to a larger scale commercial process.

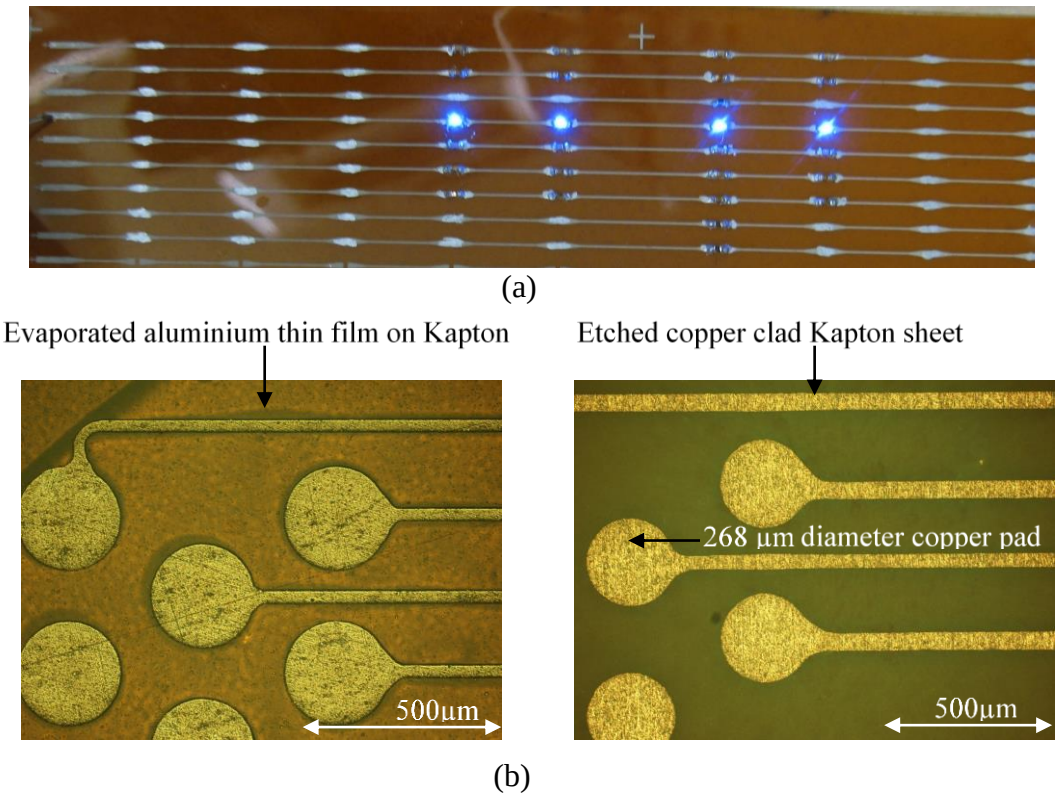


Figure 2: (a) Screen printed silver polymer conductors on Kapton with LED's attached using conductive epoxy and (b) Filament metallization by thermally evaporated aluminum 30 µm wide interconnects (left) and etched copper 55 µm wide interconnections (right).

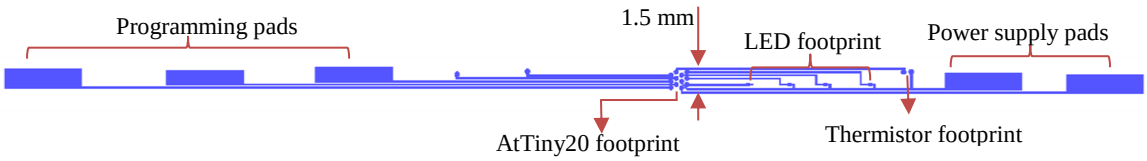
Thermal evaporation was used to metalize a 50 µm thick Kapton substrate with 100 nm thick gold and aluminum films. This enables the linewidth and spacing of the circuit to be fabricated down to 1 µm using standard contact lithography and etching. However, several technical issues were encountered. First, the aluminum film exhibited poor adhesion to the Kapton and failed the adhesion tape test. This was solved by oxygen or argon plasma treatment of the surface of the Kapton. Next, suitability for soldering and wire bonding were investigated. Solder bump attachment was found to not be possible due to the gold film burning off during soldering and the incompatibility of the solder with the aluminum. Wedge and ball wire bonding was also not possible because the bond wires would not adhere to either metal films [47] even at high bonding

forces [53]. However, when these thin films were replicated on a rigid silicon or alumina substrates, the wire bonding processes worked as expected. This non-stick effect is due to the mechanical properties of the Kapton substrate, which results in the dissipation of the ultrasonic energy during wire bonding. Therefore again electronic components could only be mounted using conductive adhesives. The patterned thin film aluminum filament is shown in Figure 2b. Copper clad Kapton from GTS Flexible Materials Ltd with a copper thickness of 18 µm, adhesive thickness of 17 µm and Kapton thickness of 25 µm was identified as the preferred solution. The adhesive bonding the copper film to the Kapton survives the tape test and the high conductivity and increased thickness of the copper give the lowest track resistance (≈ 0.003Ω/mm for a track width of 100 µm) of the three methods. This compares to track resistances per unit length of the printed 5 µm thick silver tracks and 500 nm thick evaporated aluminum are approximately 0.6 Ω/mm and 82 Ω/mm respectively. The copper film was also fully compatible with soldering and wire-bonding processes enabling a variety of chip mounting and interconnecting processes to be used. Circuit features were fabricated using photolithography and etching (see Figure 2b) and these processes and the minimum feature sizes achievable are discussed in the following section. Kapton thicknesses from 12 µm to 125 µm and copper film thicknesses ranging from 9 µm to 105 µm are available and bespoke dimensions can be obtained if ordered in large enough quantity [48].

2.2. Fabrication of filament circuits on copper-clad substrate

The copper clad Kapton substrates were patterned using a wet copper etch and a photoresist masking layer which is discussed in details in the experimental section. The minimum feature size is dependent on the thickness of the copper film due to the isotropic nature of the copper etching process that undercuts the masking layer. For the 18 µm thick copper film, feature sizes of less than 36 µm will result in the mask being completely undercut leaving an uneven copper thickness and inconsistent track resistance. For the 18 µm thick copper film a sensible minimum

feature size is 80 µm and thinner copper films should be used for smaller feature sizes. While the linewidths of circuit should be as fine as possible to minimise the size of the filament, it is important that the track resistivity is low enough to reduce voltage drops across the circuit and, in the case of higher current applications, resistive heating. The IPC-2221 standard for flex circuits for 18 µm thick copper suggests a track width of 24.4 µm for a length of 100 mm and 100 mA current [49]. The designed circuit is a digitally controlled LED lighting filament containing an Atmel microcontroller, AtTiny20, and LED (as shown in Figure 3a). The addition of a thermistor enables this filament circuit design to also work as a temperature sensor with an LED output. The circuit is 1.5 mm wide and is fitted on a 2 mm wide filament. The copper interconnections are 85 µm wide with a spacing of 96 µm, and a spacing of 25 µm was required between the bond pads of the microcontroller. During fabrication, some air bubbles can be trapped between the copper-coated Kapton and the wafer as shown in Figure 3b, but these were found not to affect the resolution of the fabricated circuits. Using stronger adhesives can reduce these bubbles but this will make the separation of the Kapton Sheet from the wafer difficult.



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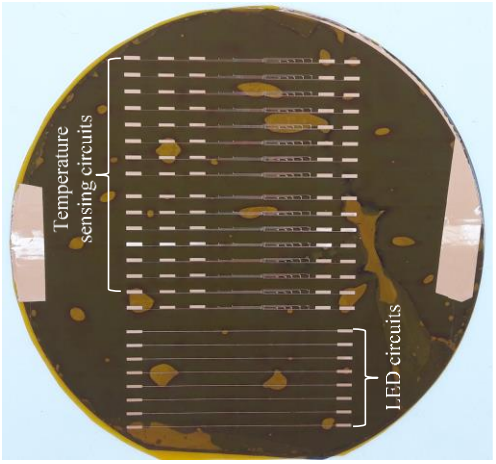
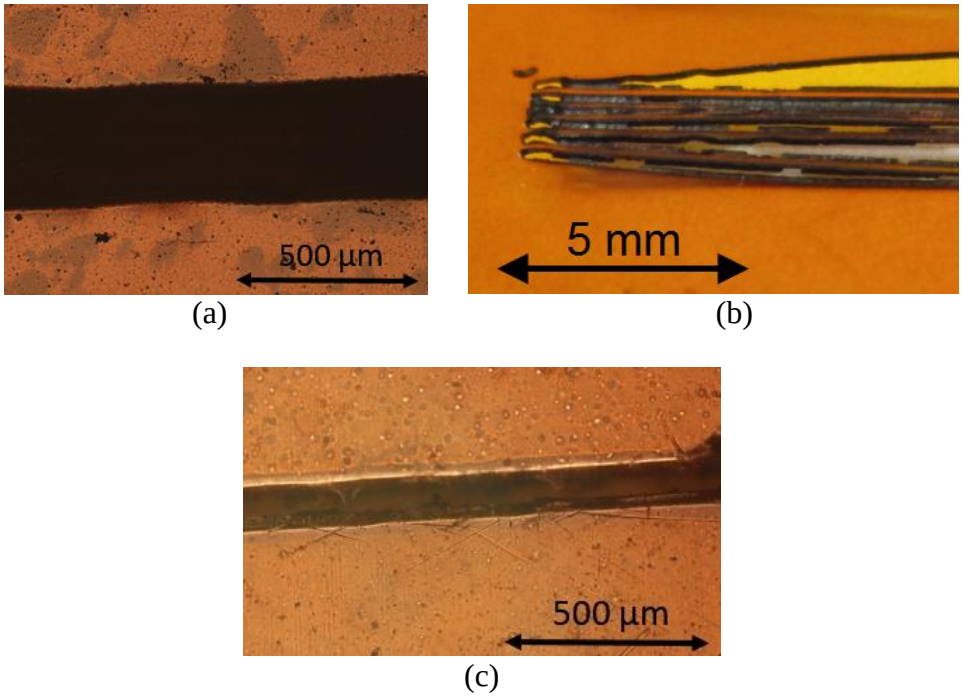


(b)

Figure 3: (a) Circuit layout of the temperature sensor filament and (b) Circuit patterns on Kapton sheet after Photolithography and etching.

2.2.1. Cutting patterned substrates into strips

Cutting the Kapton into the individual filament strips is not a trivial process and requires a repeatable high resolution process that produces clean edges. Laser cut tests on uncoated 25 µm thick Kapton was investigated by varying the stage speed, laser power, frequency and number of passes of the laser. The best results (shown in Figure 4a) were achieved using 30 W laser power, 100% speed and 5 kHz frequency, producing a 300 µm wide cut.



(a) (b)

(c)

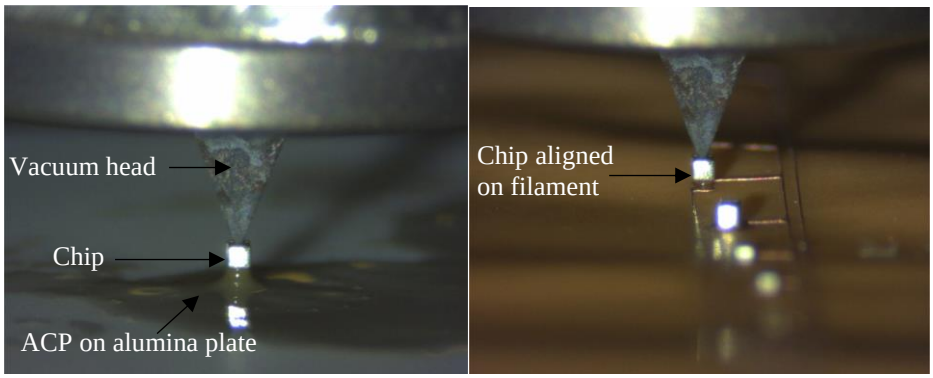
Figure 4: (a) Example laser cut with best settings, 50% power, 100% speed, producing a 300 µm wide cut, (b) Example of warping and excess carbon fouling from 0.25 mm laser cuts in Kapton and (c) Example Graphtec cut at 300 mm/s with a force setting of 14, producing a 100 µm wide cut.

Although the results are acceptable for a single isolated cut, further testing showed that cutting thin strips (<1 mm wide) from the Kapton was more difficult due to the heat affected zone either side of the cut that would cause the strip to warp. In addition, each cut would produce a significant amount of carbon powder from the burnt Kapton that fouls the surface. Example cuts forming 0.25 mm wide strips are shown in Figure 4b, the warping can be seen where the right hand sections of the strip have raised up from the surface, affecting the width of subsequent

cuts. An alternative approach was investigated using an automated flatbed cutter/plotter. The best results on Kapton are shown in Figure 4c and were achieved using a cutting speed of 300 mm/s and a force setting of 14. The cutter can provide accurate cutting and a smooth, clean edge to the strip with no warping or fouling caused when cuts are in close proximity unlike the laser cutter.

2.2.2. Attachment of components

Two different types of pastes, anisotropic conductive paste (ACP) and solder paste were investigated for attaching components on the filaments using a Fineplacer lambda commercial pick and place tool as shown in Figure 5. The tool is designed to handle components of minimum dimensions of 0.1 mm x 0.1 mm x 0.1 mm. The use of the tool for the different pastes is discussed in detail in the experimental section.



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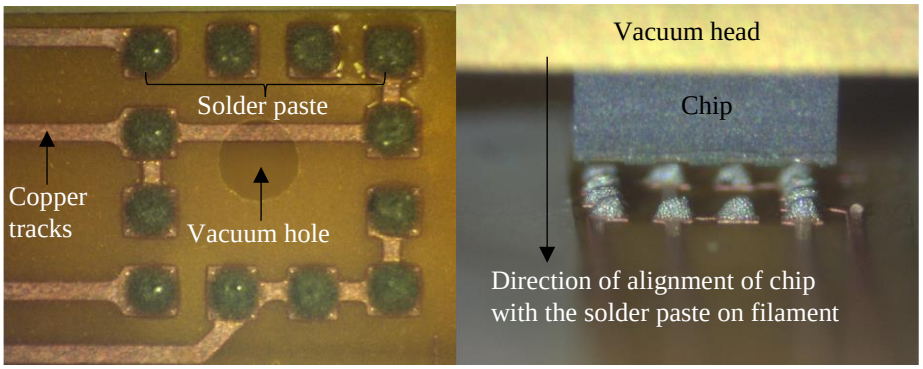


(b)

Figure 5: (a) Mounting of a thermistor chip with ACP and (b) Mounting of components on filament using stencil printed solder paste

Anisotropic conductive pastes (ACPs): ACPs are ideal for attaching components on circuits with very small (< 60 µm) pitch and spacing between footprints. This is because they provide electrical conduction in the vertical direction and prevent short circuits between interconnections that are in close proximity. They also act as an under-fill for the components thereby improving the bond strength to the substrate. Sixteen LED filaments circuits were produced using the ACP. The mechanical attachment was successful but components were found to be electrically unreliable when the filament was flexed or bent. The contact resistance of the electrical connection varies with strain.

Solder pastes: Initially, solder paste (BLT Circuit Services type 4 lead free) was pneumatically dispensed on the filament on each bond pad. However, the small volume of paste (pico-litres) required a nozzle diameter <150 µm which was found to get clogged by the conductive particles in the pastes. Therefore the solder paste was printed using a 100 µm thick stainless steel stencil aligned with the substrate producing solder bumps on the surface as shown in Figure 5b. Solder plus underfill was found to provide a mechanically and electrically reliable bond and the connection wires to the circuits were also soldered as shown in Figure 6.

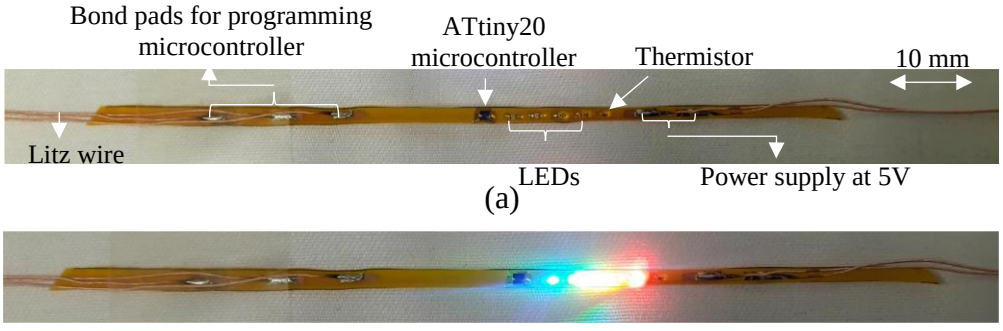
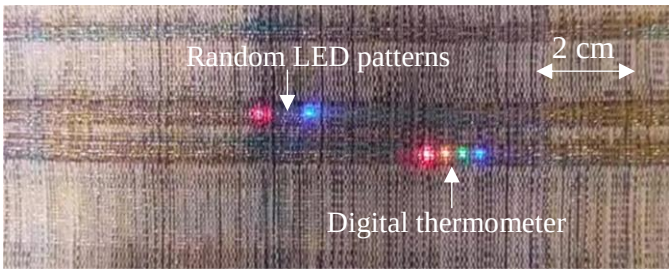


Figure 6: (a) Mounted components on a filament using soldering and (b) an operational digitally controlled LED filament switched on at 5 volts.

2.3. Weaving filament into fabrics

The weaving process for the filaments into fabrics using a commercial dobby weaving loom is discussed in details in the experiment section. The fabricated demonstrators include a digitally

controlled LED or temperature sensing filament and passive LED filament circuits as shown in Figure 7. The LEDs on the temperature sensing filament light up in turn with increasing temperature. The temperature thresholds are defined in the microcontroller and are fully adjustable. The filament has been designed to respond to body heat and could form a visual digital thermometer, with blue light signaling "cold (< 10°C)" and the red light signaling "hot (> 40°C)" conditions, Figure 7a. Alternatively, the LEDs are driven directly from the microcontroller enabling, for example, a random pattern, Figure 7a. These filament circuits are reprogrammable after integration and can be adapted to suit desired applications.



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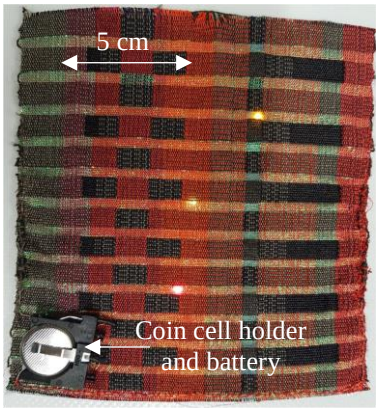


Packaged with a coin cell

(b)

Figure 7: (a) Woven fabric containing digitally controlled LED filaments with random patterns and a digital thermometer (b) woven fabric swatch containing passive LED filaments with a 3V coin cell integration.

Figure 7b shows LED filaments woven into a textile swatch. The power supply wires coming out from the woven pockets were laced back through the edge of the swatch and stitched in place before connecting to a coin-cell holder fastened to the backside of the swatch. A 3V coin

cell powers the swatch and, in contrast to previous works[31-33], the filaments are completely concealed in the textile swatch and the LED is only visible when turned on.

2.4. Bending test

The minimum filament width (W) for a circuit containing the smallest available microcontroller (ATtiny20) is 2 mm. The number of electrical interconnections (or conductive tracks), *n*, that can be positioned symmetrically on the filament can be calculated from equation (1), where *l* is the line-spacing between the tracks, *x* is the distance between the outer most tracks and the edge of the filament, and *D* is the track width as shown in Figure 8.

$$n = \frac{W + l - 2x}{l + D} \tag{1}$$

Figure 8: Positioning conductive tracks on filament of width, *W*

As the value of "*n*" increases, the track width, *D* must reduce in order to maintain the 2 mm circuit width. In general, circuits with $D \geq 200$ µm give good performance [35] and based on equation (1) this will enable circuits with $n \leq 5$, when l = 200 µm and x = 100 µm. The gap sizes between bond pads on the ATtiny20 requires the value of *D* to be less than 200 µm.

The influence of track width and length on circuit reliability was explored from the 90° bending test shown in Figure 9a performed on the LED filament circuits in Figure 7c for track widths, D = 80 µm, 100 µm, 150 µm and 200 µm and track length, L = 2.5 mm, 5 mm, 7.5 mm and 10 mm. Track widths will reduce by 36 µm after etching due to undercut of the copper. To

investigate failure at the joint between the tracks and the bond pads, different joint designs [35] were tested as shown in Figure 9b.

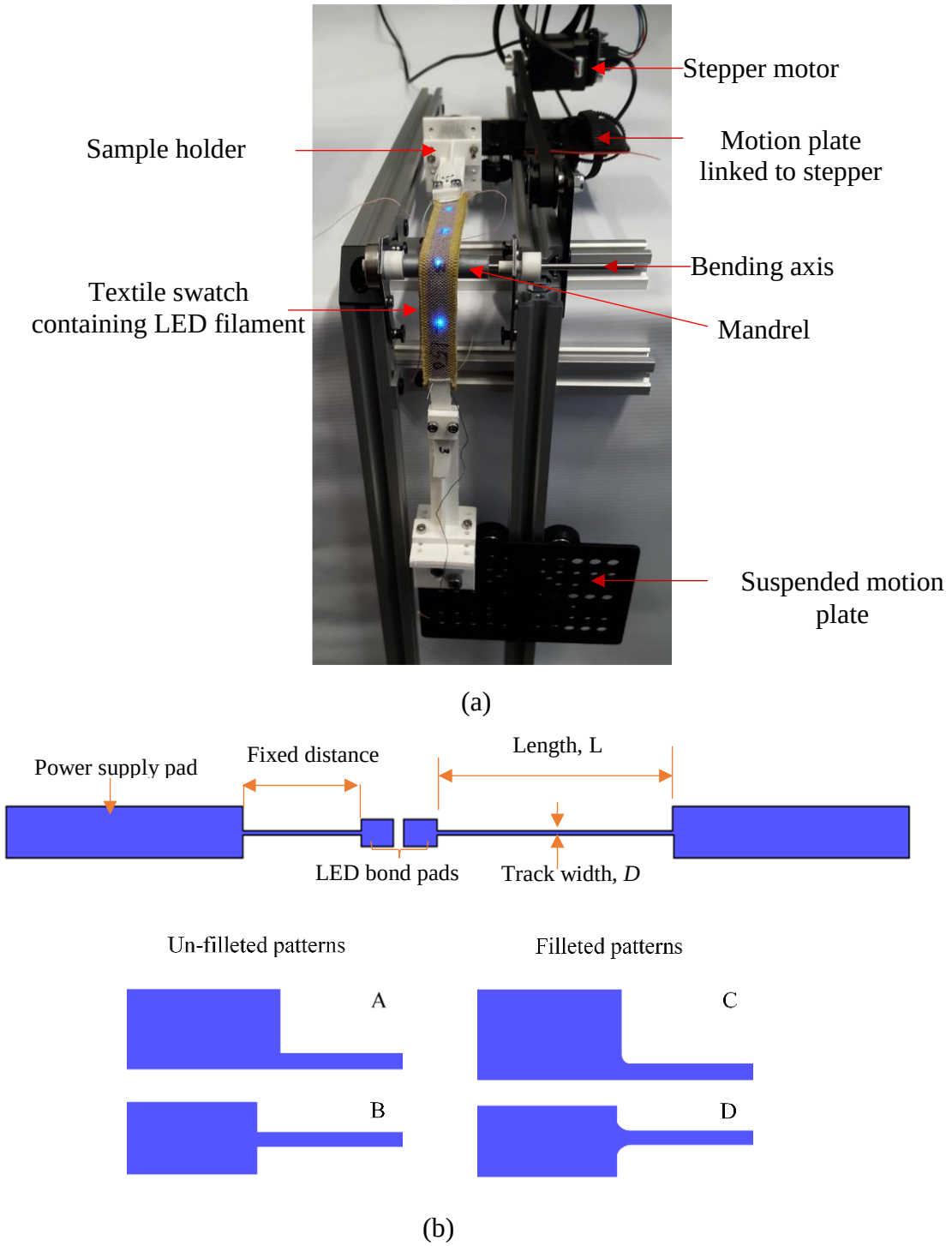


Figure 9: (a) Filament circuits with swatch sample shown under 90° bending test (b) circuit designs for filament showing filleted and un-filleted patterns at bond pad/track joint.

2.4.1. Effect of bending on filleted and un-filleted bond pads

Examination of filaments after bending indicated the joint between the track and bond pad is a failure point (Figure 10a) and showed that the addition of the fillets in the design affects the location of the break (see Figure 10 b and c) but do not prevent these from occurring. The filleted filaments did not perform any better than the un-filleted filaments because the average number of bending cycles in both cases before failure was 62 cycles for a track width of 150 µm.

(a) (b) (c)

Figure 10: Post-bending failure points on 150 µm wide copper tracks (a) with no fillet to the bond pads (b) filleted at the edge of the bond pad and (c) filleted at the centre of the bond pads.

2.4.1. Effect of bending on filaments with and without glob-top encapsulation

The LEDs on 9 bare filaments were glob-topped using UV-curable polymer EC-9519 and the results were compared with 7 unencapsulated bare LED strips. The glob top was nozzle dispensed at a pressure of 22 kPa and UV cured for 30 seconds. Samples were tested around a 5 mm bending radius and the results are shown in Figure 11. The glob-topped filaments survive on average twice the number of cycles of the unencapsulated samples. The filaments without glob-top failed due to the presence of cracks at the point where the copper tracks terminates on the LED bond pad as shown previously in Figure 10 and with the LED in place in Figure 12. For the glob-topped filaments, the failure point is moved to the interface where the glob-top terminates on the copper track a shown in Figure 12. The glob top protects the circuit around the LED making the circuit stiffer in this region and delays the onset of the cracking in the copper track.

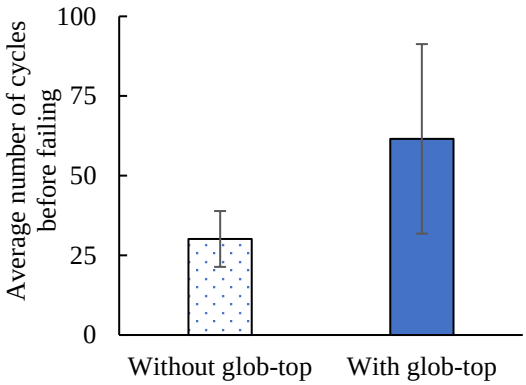


Figure 11: Impact of glob-topping on durability of filament circuit

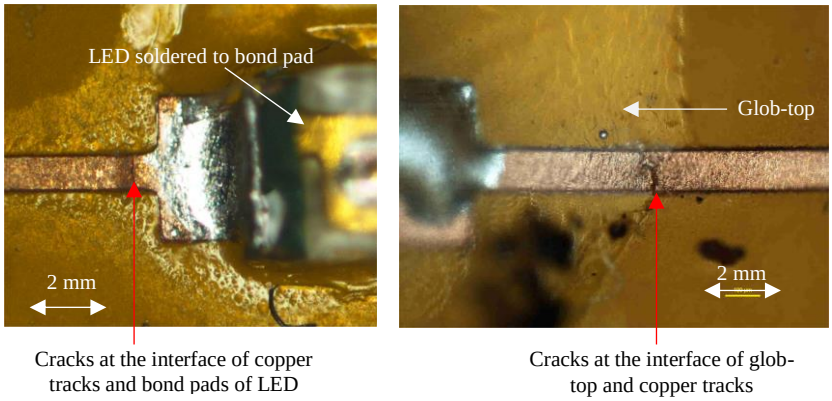


Figure 12: Post-bending failure modes on 150 µm wide copper tracks on filament with (right) and without (left) glob-top encapsulation.

2.4.3. Effect of track width, bending radius and fabric swatch

The bending results in Figure 13 show that the average number of cycles survived by the filaments increases with increasing track width and bending radius. Samples with track width of 80 μm performed particularly poorly and almost 50% of the test samples failed before testing due to handling. Hence these samples were not integrated into the swatch. The fabric swatch doubles the average cycles survived by the glob-topped filaments for all track widths at a bending radius of 5 mm. In the swatch samples, the fabric is clamped directly and the tension is acting along the fabric instead of being directly applied to the filaments. Fabric samples with $D = 200\ \mu m$ filaments survived 1500 cycles at a tension of 0.5 N and a bending radius of 10 mm.

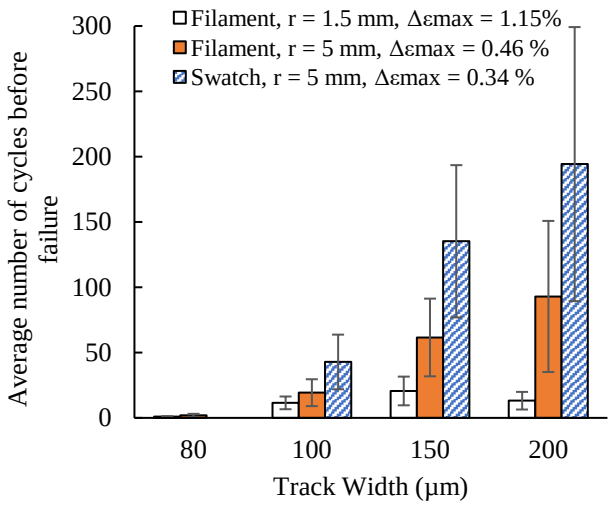


Figure 13: Effect of fabric swatch on the reliability of filament circuit, r is the bending radius and $\Delta\varepsilon_{max}$ is the maximum strain on the copper film.

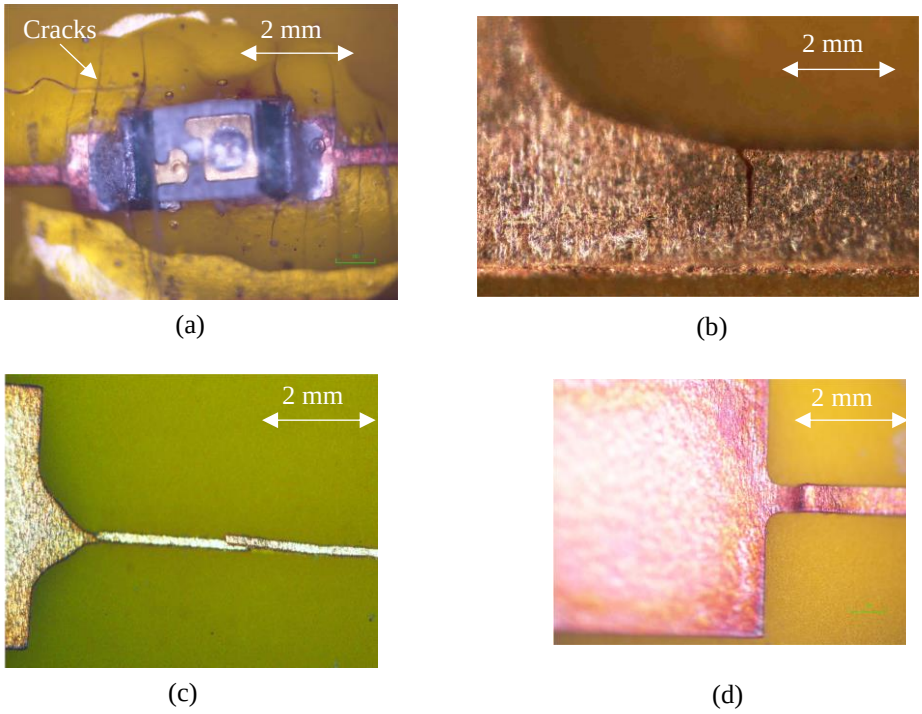


Figure 14: Post-bending failure modes of circuits (a) Cracks forming on glob-top encapsulation at 1.5 mm bending radius, (b) micro-fractures forming on 150 µm wide copper tracks close to the bond pads, (c) flaking of 80 µm copper tracks due to adhesion failure and (d) buckling of 150 µm wide copper track due to adhesion failure.

The failure modes shown in Figure 14 apply to all filaments both integrated in the textile and freestanding across all bending radii. The failure modes include breaks in the copper tracks, the development of cracks on the glob-top encapsulation, and flaking and buckling of the copper

tracks due to adhesion failure between the copper and the Kapton filament. The flaking of the copper tracks were common for filaments with track width D = 80 µm.

2.4.4. Maximum cyclic strain range, $\Delta\varepsilon_{max}$ induced on filaments in bending

Three bending radii, r = 1.5 mm, 5 mm and 10 mm were used in the bending test. The deformation of the filament circuit (without the fabric swatch) as it bends around the mandrel is shown in Figure 15. The neutral axis, NA positions (where the strain ε = 0) of the filament before and after integration into the fabric are 48.5 µm and 296 µm respectively. These were calculated from equation 2 [30,50] based on the material properties listed in Table 2. In both cases, the elastic modulus of the copper dominates the composite structure such that the NA positions are located within the copper layer close to the boundary between copper and adhesive films. Given these NA values, the induced strain at any point 'y' from the center of the filament is obtained from equations 3 [30] and the maximum strain range $\Delta\varepsilon_{max}$ is the sum of the compressive and tensile strains. As expected, the $\Delta\varepsilon_{max}$ results given in Table 2 shows that the strain induced on the filaments reduce as the bending radius is increased. . For filaments within the swatch, the fabric reduces the strain induced on the copper by 26 % (i.e. a strain difference of 0.0012) for r = 5 mm. This explains the increased fatigue lifetime (i.e. number of cycles before failure) of the filaments in the swatch samples as shown in Figure 13. However, the strain results and the NA representation in Figure 15 still indicate the need to reduce the thickness of the copper so that the film is located closer to the NA thereby enhancing its fatigue life.

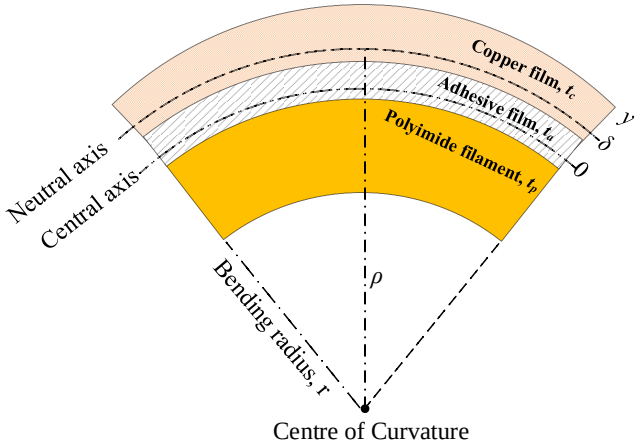


Figure 15: The bending of a filament circuit around a mandrel of radius, r. Where ρ and δ represent the distance of the NA from the center of curvature and central axis respectively.

$$NA = \frac{\sum_{i=1}^{n} E_i t_i \left(2\sum_{j=1}^{i} t_j - t_i\right)}{2\sum_{i=1}^{n} E_i t_i} \quad (2)$$

$$\varepsilon = \frac{y - \delta}{\rho} \quad (3)$$

Where 'n', E_i and t_i in equation 2 are the total number of layers, elastic modulus and thickness of the 'i^{th}' layers in the filament respectively.

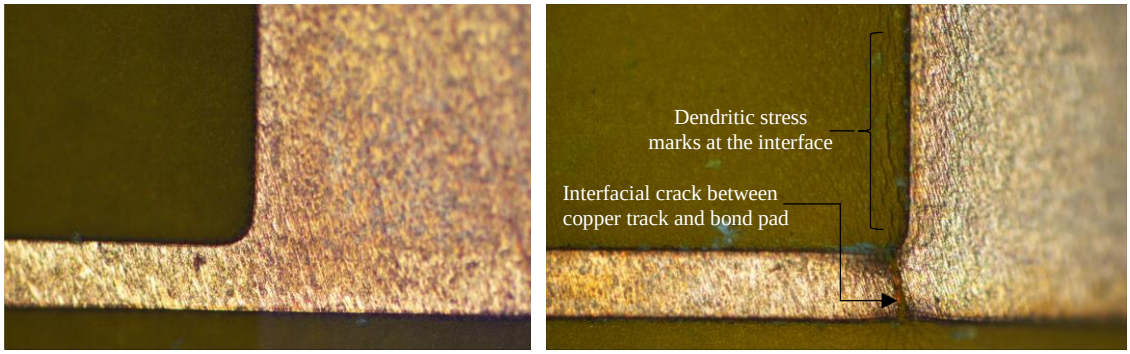
Table 2: Material properties of filament circuit

Materials	Thickness, t (µm)	Elastic Modulus, E (GPa)	NA position (µm)		$\Delta\varepsilon_{max}$ without swatch (%)		$\Delta\varepsilon_{max}$ with swatch (%)	
			Without swatch	With swatch	r = 1.5 mm	r = 5 mm	r = 5 mm	r = 10 mm
Copper	18	70[51]	48.5	296	1.15	0.46	0.34	0.18
Adhesive	17	1.8			1.94	0.58	0.51	0.28
Apical Polyimide	25	3			4.6	1.43	1.3	0.69
Swatch	496	0.155			-	-	11.63	5.99

2.5. Effect of washing on filaments integrated within the fabric

Five glob-topped filaments in two swatch samples as shown in Figure 7b were subjected to the ISO 6330:2000-6A washing standard as described in section 4. Filaments of *D = 200 µm* were used for the wash test since they performed best in bending. After five washing cycles, interfacial cracks surfaced between the copper tracks and the power supply bond pads on the filaments as shown in Figure 16. Dendritic stress marks had also grown on the polyimide base in the region where the copper track interfaced the bond pad as shown in Figure 16b. These

stress dendrites were not visible in other areas on the filament which suggests that the copper track-bond pad interfaces constitute a major failure/stress point for the circuits and the polyimide substrate. The glob-top encapsulations were unaffected by the washing and all samples worked when probed before the interfacial cracks. Further testing with a different encapsulation method that completely protects the copper tracks and the chip using a thermally molded polyimide filament [52] increased the washing span of the filaments to 45 cycles.



(a) (b)

Figure 16: A comparison of filament circuits (a) before and (b) after washing showing interfacial cracks and dendritic stress mark growth.

2.5. Challenges for integrating filament circuits in textiles

There are a significant number of challenges to overcome in fabricating flexible filament circuits suitable for integration inside a yarns or woven into the textile. Wherever possible, scalable processes have been used to enable future mass manufacture, which is essential for achieving low cost solutions.

2.5.1. Cutting filament circuits for e-textiles

The goal of this technology is to ultimately produce filaments of < 0.5 mm width and reliably cutting filaments that are up to 15 cm long and 0.5 mm wide is not trivial. The automated scalpel cutter has proved capable of meeting this requirement and produced smooth, repeatable cuts with no additional damage to the substrate. Furthermore, larger roll-to-roll cutters of this type are commercially available thus making this a viable approach for mass production. The lab-

based cutter used in this work is not able to cut the filaments after the components have been mounted which complicates subsequent assembly and this would have to be addressed.

2.5.2. Mounting components on filaments

Mounting the components to the filament circuits is also not straightforward. Bond pad sizes of less than 300 µm square present a challenge when dispensing solder pastes, but stencil printing is suitable and is a process widely used in the printed circuit board (PCB) industry. The stencils used for larger components (e.g. 0805 package) are 100 µm thick and this results in a paste transfer efficiency (TE) higher than 0.66, which is the minimum surface area ratio (SAR) necessary to achieve a complete paste transfer from the stencil to substrate (IPC-7525 standard). However, as the size of the component and pitch is reduced, as is the case in this research, achieving a surface area ratio (SAR) in excess of 0.66 becomes challenging because the stencil thickness must be reduced accordingly. This complicates the stencil manufacturing process and increases the difficulty of handling the stencil during use. The minimum feature in this work is 60 µm × 170 µm, and the resulting SAR from a 50 µm thick stencil is 0.44 which is below the minimum IPC-7525 standard. In addition to the stencil, the type of solder paste is also critical. Solder paste consists of liquid flux and alloy particles. The alloys used in the solder paste are typically soft metals that are easily deformed whilst printing. A typical rule of thumb within the PCB industry is that the solder particle should be 5 times smaller than the minimum stencil aperture width. Commercial type 3 (particles size between 25 and 45 µm) and type 4 (20-38 µm) pastes are often used but, for smaller components (<100 µm), type 5 (15-25 µm) or even type 6 (15-25 µm) may be needed to achieve an optimised paste transfer in conjunction with a thin stencil. The type 4 solder paste used in this work for mounting the electronic components has a maximum particle size half that of the minimum feature size on the stencil. This introduces the difficulty of applying sufficient alloy particles on to the filament circuit, thereby reducing

the yield of the soldering process. This challenge will be addressed by evaluating the other types of paste with a smaller particle size.

2.5.3. Durability of woven filaments in fabrics

At present, filament circuits are manually inserted in the pockets during weaving and the placement accuracy can be challenging because of the surrounding fabric yarns. Automating this process will allow high throughput for the mass production. It would improve the placement accuracy of the filaments with in the fabric and prevent poor handling of the filaments before they are embedded. The durability of the embedded filament circuits in the textile is also crucial. Embedded filament circuits must be reliable over the life-time of the fabric to be useful in many applications. With glob-top encapsulations, these filaments can survive more than 1500 bending cycles at a 1 cm bending radius. However the bending and washing results show that the durability achievable with glob-top encapsulation of components is limited by the migration of stress points to other areas on the filament circuit that are not protected. To eliminate the stress points, the entire filament should be uniformly encapsulated. This can be achieved by sealing the filament circuit with another layer of Kapton or a thermoplastic material such that circuit is located the neutral axis[52,53]. Although with the use molded Kapton, filaments survive 45 wash cycles but there is need for new methods to optimize the filament circuit design so that interconnect lines are reliably terminated on the larger bond pads where external circuitry or power sources are connected. These approaches will improve the life-time of integrated filaments in fabrics under bending and washing stresses which are typical stresses for fabrics.

3. Conclusion

This paper described a technology that allows electronic circuits to be fully concealed and integrated within a fabric. Prototype fabrics have been demonstrated that contain 2 mm wide filament circuits successfully incorporated inside bespoke pockets during the garment manufacture. The filaments circuits contain sensors and processing capabilities and represent

the state of the art in terms of e-textile functionality and integration. This is particularly promising for healthcare applications where electronics for remote monitoring of patients can remain invisible and non-intrusive to the patients leading to improved user acceptability and compliance.

Currently, the integrated circuits on the filaments are etched from 18 µm thick copper material but the reliability of the filament circuits degrade significantly during bending as the track width of circuit reduces beyond 200 µm. As the copper thickness reduces, the integrated electronics can be easily positioned in close proximity to the neutral axis with new encapsulation methods and materials that would improve the fatigue life of the filaments after integration. The interfacial cracks between the copper tracks and the bond pads for connecting to external circuitry are also a major failure mode limiting the bending and washing of the filaments. Methods for optimizing filament circuit design, to achieve reliable interfaces between interconnects and bond pads (or encapsulation materials) are still needed to significantly reduce interfacial failures.

4. Experimental section

Fabrication of filament circuits on copper-clad substrate: The copper coated Kapton was mounted on a 150 mm diameter silicon handle wafer using a wet resist bonding layer and was patterned using contact based photolithography process. A 6 µm thick films of AZ9260 positive photoresist was deposited (spin speed of 3000 rpm for 30 seconds and oven baked for 3 minutes at 110 °C) and patterned using an EVG 620T contact mask aligner with a 20 second exposure at an energy density of 8.88 mW/cm^2. The resist was developed by immersion in a 1:4 solution of AZ400K developer and water for 5 minutes. The copper was then patterned in a PCB etch crystal solution (Sodium Peroxidsulfate) at 45 °C for 8 minutes followed by rinsing in de-ionised water and cleaning with acetone to strip the remaining resist.

Cutting the filament: An Epilog Mini 24 laser cutter with a 60W CO_2 laser with a cutting pattern resolution of 1200dpi, repeatability of +/- 0.0127 mm and an accuracy of +/- 0.0254 mm over the length of the table (600mm) was evaluated. The laser was used to cut the Kapton after the copper surrounding the circuit has been etched away. Graphtec CE600-40 with a 100 µm steel tip cutting blade was used. The cutter moves at speeds up to 600 mm/s with a resolution of 10 µm and repeatability of 100 µm.

Attachment of components with anisotropic conductive pastes (ACP): An arbitrary volume of anisotropic conductive paste (Elecolit 3061 from Eurobond Adhesives Ltd) was manually dispensed on to a flat alumina plate as shown in Figure 5a. The component was picked up and dipped into the ACP using the pick and place tool such that the adhesive forms a glob on the bottom of the component. The filament substrate was positioned on the heating plate of the Finetech tool and the component was aligned and positioned with a bonding force of 10 N (contact pressure of 130 MPa) and heated up to 100 ºC in 10 seconds, held for 60 seconds and then cooled.

Attachment of components with solder paste: Solder paste was printed using a 100 µm thick stainless steel stencil aligned with the substrate producing solder bumps on the surface as shown in Figure 5b. The filament was positioned on the heating plate and the component aligned and then lowered onto the substrate. The bond was formed using the temperature profile in Table 3. To improve the mechanical attachment of the chip to the substrate, Loctite 4902 was used as under-fill. This was dispensed just after stencil printing the solder paste and was heated simultaneously with the solder paste to bond the chip to the filament. Components supplied with solder bumps were initially dipped into a small volume of solder-flux paste to aid the flow and wetting of the solder on the copper bond pads. The component was then aligned on the filament and bonded using the temperature profile in Table 3.

Table 3: Temperature profile for soldering of chip

Process step	Temperature	Duration
Ramp up rate	T < 150ºC	10 secs
Pre-heat soldering temperature	150 ºC	25 secs
Second ramp up rate	150 ºC - 240 ºC	10 secs
Peak temperature	240 ºC	10 secs
Ramp down	T = 40 ºC	15 secs

Weaving filament circuits into fabric: A Toika dobby weaving loom was used to integrate the filaments into the fabric. The filament circuits were positioned in narrow pockets that are created as part of the fabric weaving process. The bespoke pockets are formed within the fabric using a double cloth (or double weave) set up. This involves weaving two or more sets of warp and one or more set of weft yarns that forms two layers of fabric interlaced together by one of the weft yarns [54]. Two sets of warp yarns are wound on two separate wooden back beams of the loom and guided through metallic heddles as shown in Figure 17a. These series of warps are woven with individual weft or filling yarns to make two layers of cloth with a plain weave structure for making a strong, stable and even fabric [54]. The pocket is created when the position of the top cloth and the bottom cloth is interchanged i.e. the top cloth becomes the bottom cloth and vice versa. This creates a stitched line across the fabric, a woven intersection of both fabric layers that opens up the pocket shown in Figure 17b and repeating the process at the required point in the weave design closes the pocket. The filament is manually inserted immediately the pocket is created (Figure 17c) and the connecting copper wires from the filaments are manually routed at the same time as shown in Figure 17d. The optimum wire for this process was found to be a silk coated multistrand Litz wire that moves feely within the woven pockets. This weaving method can create vertical and horizontal pockets within the fabric for routing the wires and the filaments in the warp and weft directions as required.

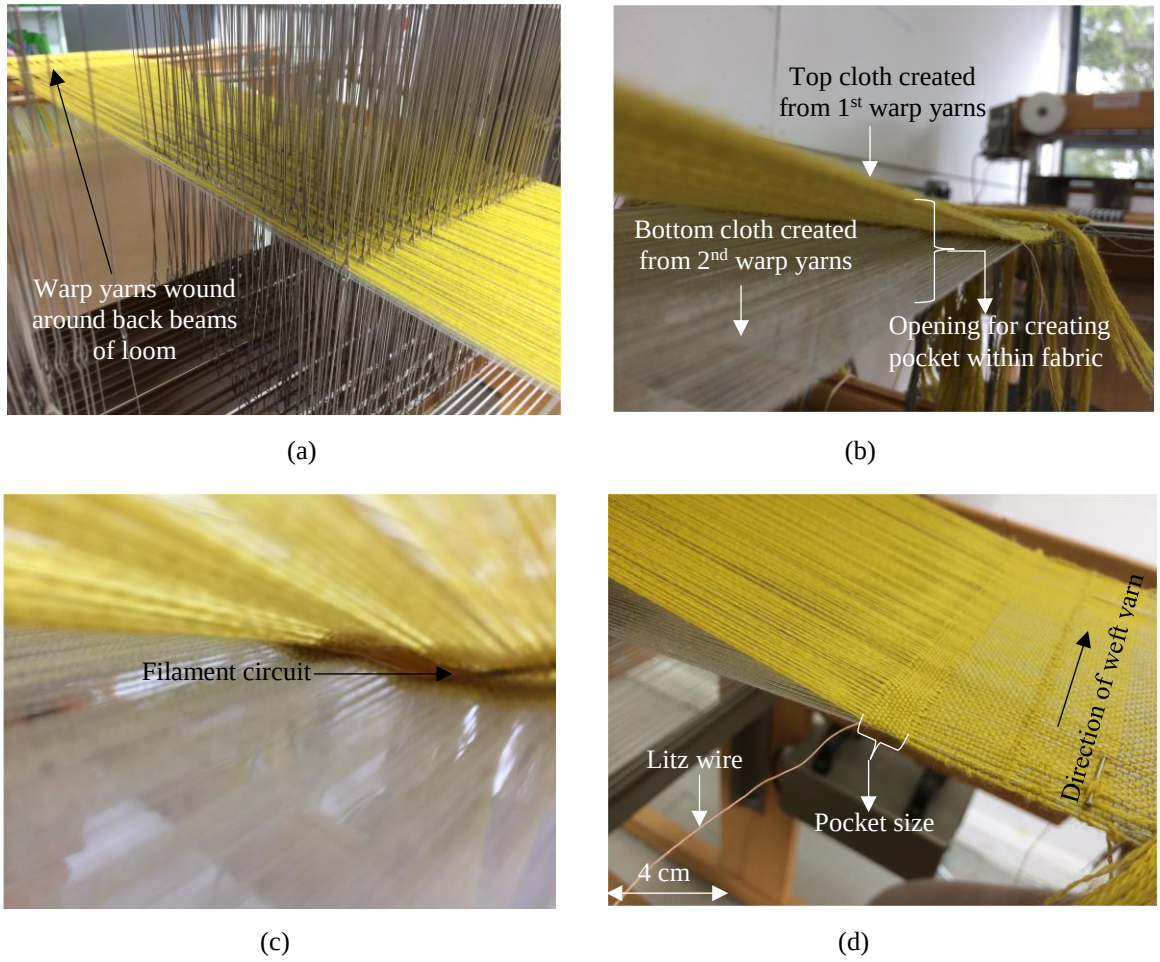


Figure 17: Weaving of filaments into fabric (a) Loom set up for weaving a fabric swatch, (b) Weaving of pocket into fabric swatch, (c) Filament placement in pocket and (d) Routing of wire in and out of the pocket

Bending test: The bending rig, shown in Figure 9a, was used to cyclically strain the LED filament circuits. The bending rig is driven by a stepper motor that moves the sample holder backwards and forwards with the test sample being folded around a specified radius. The 1.5 N tension in the sample is defined by the weight of the sample holder and plate attached to the other end of the sample. The LED filaments are powered during the test and cycled around bending radii of 1.5 mm, 5 mm and 10 mm until the LED blinks or fails completely. A total of 171 LED filament circuits were tested of which 54 were integrated into the fabric swatch shown in Figure 7c.

Washing test: The swatches containing the filament circuits were loaded with seven other clothes in a domestic washing machine for five washing cycles that consisted a 58 minute wash at a temperature of 40°C with a 1000 rpm spin dry cycle. The fabrics were washed in a commercial Beko washing machine WME7247W with the DAZ washing detergent for every wash cycle. This wash cycle was chosen to closely replicate the normal washing procedure as stated in the ISO 6330:2000-6A washing standard [53]. To enhance the durability of the filaments, the Litz wires extending from the power supply bond pads of the filaments were stitched to the swatches before washing using a PFAFF Creative 3.0 sewing and embroidery machine. The samples were washed without the battery.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author. The data for this paper can be found at DOI: 10.5258/SOTON/D0365.

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[1] F. Axisa, P. M. Schmitt, C. Gehin, G. Delhomme, E. McAdams, A. Dittmar, *IEEE Trans. Info. Tech. biomedicine*, **2005**, 9(3), 325.

[2] L. M. Castano, A. B. Flatau, *Smart Mater. and Struc.* **2014**, 23(5), 053001.

[3] K. Cherenack, L. van Pieterson, *Journal of Applied Physics*, **2012**, 112(9), 091301.

[4] K. J. Heilman, S. W. Porges, *Biological psychology*, **2007**, 75(3), 300.

[5] R.Ma, J. Lee, D. Choi, H. Moon, S. Baik, *Nano letters*, **2014**, 14(4), 1944.

[6] T. Hughes-Riley, P. Lugoda, T. Dias, C. L. Trabi, R. H. Morris, *Sensors*, **2017**, 17(8), 1804.

[7] R. Bhattacharya, L. van Pieterson L, K. van Os, *IEEE Trans. CPMT*, **2012**, 2(1),165.

[8] N. Taccini, G. Loriga, A. Dittmar, R. Paradiso, in *Proc. 26th Annual Int. Conf. IEEE EMBS*, San Francisco, CA, USA, September **2004**.

[9] N. Noury, A. Dittmar, C. Corroy, R. Baghai, J.L. Weber, D. Blanc, F. Klefsat, A. Blinovska, S. Vaysse, B. Cornet presented at *26th Annual Int. Conf. IEEE Eng. in Medicine and Biology Society*, September **2004**.

[10] I. Locher, M. Klemm, T. Kirstein, G. Trster, G. *IEEE Trans. Adv. Packaging*, **2006**, 29(4), 777.

[11] D. Patron, W. Mongan, T. P. Kurzweg, A. Fontecchio, G. Dion, E. K. Anday, K. R. Dandekar, *IEEE Trans. biomed. cir. and sys*, **2016**, 10(6), 1047.

[12] D. Curone, E. L. Secco, A. Tognetti, G. Loriga, G. Dudnik, M. Risatti, G. Magenes, *IEEE Trans. Info. Tech. Biomed.*, **2010**, 14(3), 694.

[13] M. A. Oleson, C. Dibenedetto, S. Tomlinson, A. W. Van Noy, A. J. Vaterlaus, and S. M. Vincent, *U.S. Patent*, No. 9, 645,165, **2017**.

[14] N. Davies, *AATCC Review*, **2017**, 17(5), 46.

[15] E. R. Post, M. Orth, P. R. Russo, and N. Gershenfeld, *IBM Sys. Journal*, **2000**, 39(3.4), 840.

[16] X. Tao, V. Koncar, T. H. Huang, C. L. Shen, Y. C. Ko, G. T. Jou, *Sensors*, **2017**, 17(4), 673.

[17] S. de Mulatier, M. Nasreldin, R. Delattre, M. Ramuz, T. Djenizian, *Adv. Mater. Tech.* **2018**, *3*(10), 1700320.

[18] J. S. Heo, T. Kim, S. G. Ban, D. Kim, J. H. Lee, J. S. Jur, S. K. Park, *Adv. Mater.* **2017**, *29*(31), 1701822.

[19] Y. Kim, H. Kim, H. Yoo, *IEEE Trans. Adv. Packaging*, **2010**, 33 (1), 196.

[20] M. A. Yokus, R. Foote, J. S. Jur, *IEEE Sensors Journal*, **2016** 16(22), 7967.

[21] W. Dang, V. Vinciguerra, L. Lorenzelli, R. Dahiya, *Flexible and Printed Elect.* **2017**, 2(1), 013003.

[22] J. Byun, E. Oh, B. Lee, S. Kim, S. Lee, Y. Hong, *Adv. Funct. Mater.* **2017**, 27(36), 1701912.

[23] J. Yoon, Y. Jeong, H. Kim, S. Yoo, H. S. Jung, Y. Kim, S. H. Choa, *Nature commun.* **2016**, *7*, 11477.

[24] K. Yang, R. Torah, Y. Wei, S. Beeby, J. Tudor, *Textile Research Journal*, **2013**, 83(19), 2023.

[25] A. Komolafe, R. Torah, J. Tudor, S. Beeby, in *MDPI Proc.* **2017,** 1 (4), 613.

[26] A. Almusallam, Z. Luo, A. Komolafe, K. Yang, A. Robinson, R. Torah, S. Beeby, *Nano Energy*, **2017**, 33, 146.

[27] M. De Vos, R. Torah, M. Glanc-Gostkiewicz, J. Tudor, *Journal of Display Tech.*, **2016**, 12(12), 1757.

[28] C. R. Merritt, H. T. Nagle, and E. Grant, *IEEE Trans. Info. Tech. in Biomed.* **2009**,13(2), 274.

[29] K. Yang, C. Freeman, R. Torah, S. Beeby, J. Tudor, *Sensors and Actuators A: Physical*, **2014**, 213, 108.

[30] A. O. Komolafe, R. N. Torah, M. J. Tudor, S. P. Beeby, *Smart Mater.and Struc.* **2018,** *27*(7), 075046.

[31] G. A. Salvatore, N. Münzenrieder, C. Zysset, T. Kinkeldei, L. Petti, G. Tröster, in IEEE 36th Annual EMBC Int. Conf. August, **2014**.

[32] C. Zysset, T. W. Kinkeldei, N. Munzenrieder, K. Cherenack, G. Troster, *IEEE Trans. Comp. Packaging and Manufacturing Tech*. **2012**, 2(7), 1107-1117.

[33] K. H. Cherenack, T. Kinkeldei, C. Zysset, G. Troster, *IEEE Electron Device Letters*, **2010**, 31(7), 740.

[34] S. Takamatsu, T. Yamashita and T. Itoh in *IEEE Symposium on DTIP of MEMS and MOEMS*, **2015**.

[35] J. Fjelstad, "Flexible circuit technology", Fourth edition, **2018**.

[36] C. Zysset, T. Kinkeldei, N. Münzenrieder, L. Petti, G. Salvatore, G. Tröster, *Textile Research Journal*, **2013**, 83(11), 1130-1142.
[37] K. Cherenack, C. Zysset, T. Kinkeldei, N. Münzenrieder, G. Tröster, *Adv. Mater.* **2010**, 22(45), 5178.
[38] D. Hardy, I. Anastasopoulos, M. N. Nashed, C. Oliveira, T. Hughes-Riley, A. Komolafe, T. Dias, in IEEE Symposium on DTIP, May, **2018**.
[39] C. Müller, M. Hamedi, R. Karlsson, R. Jansson, R. Marcilla, M. Hedhammar, O. Inganäs, *Adv. Mater.* **2011**, *23*(7), 898.
[40] M. Hamedi, R. Forchheimer, O. Inganäs, *Nature Mater.* **2007**, *6*(5), 357.
[41] D. H. Kim, Y. S. Kim, J. Wu, Z. Liu, J. Song, H. S. Kim, J. A. Rogers, *Adv. Mater.* **2009**, *21*(36), 3703.
[42] A. R. Köhler, L. M. Hilty, C. Bakker, *Journal of Industrial Ecology*, **2011**, *15*(4), 496.
[43] A. R. Köhler, *Materials & Design*, **2013**, *51*, 51-60.
[44] M. Li, J. Tudor, R. Torah, S. Beeby, 67th IEEE Electronic Components and Technology Conference (ECTC), May, **2017**.
[45] M. Li, J. Tudor, R. Torah, S. Beeby, *IEEE Trans. Components, Packaging and Manufacturing Technology*, **2018**, 8(2), 186.
[46] H. Ushijima, Y. Kusaka, M. Fujita, K. I. Nomura, S. Kanazawa, Y. Horii, N. Yamamoto, in *Int. Conf. Electronics Packaging (ICEP)*, April, **2017**.
[47] P. S. Chauhan, A. Choubey, Z. Zhong, M. G. Pecht, *Copper wire bonding*, Springer New York, **2014**.
[48] GTS Flexible Materials LTD, *GTS 7800 – Copper polyimide laminates*, *GTS Ultraflex datasheet*, **2015**.
[49] Institute of Printed Circuits Standard IPC-2221, PCB Trace Width Calculator, website: http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator/ - last accessed 7th May, **2019**.
[50] W. Engelmaier, A. Wagner, *Circuit World*, **1988**, *14*(2), 30.
[51] J. Zhu, J. Feng, Z. Guo, *RSC Advances*, Z. **2014**, 4(101), 57671.
[52] M. Li, J. Tudor, J. Liu, R. Torah, A. Komolafe, S. Beeby, *IEEE Trans. CPMT*, **2019**, *9*(2), 216.
[53] A. Komolafe, Phd Thesis, University of Southampton, **2016**.
[54] N. Gokarneshan, *Fabric structure and design*, New Age International, **2004**.
[55] http://gow.epsrc.ac.uk/NGBOViewGrant.aspx?GrantRef=EP/M015149/1, last accessed 7th May, **2019**.

Table of Contents Entry

An electronic textile that completely conceals the presence of any integrated electronic functionality from the wearer is produced by weaving traditional textile fibers/yarns with electronic filament circuit prototypes consisting of reprogrammable temperature sensor and digitally controlled LED lightings. The textile fibers disguise the filaments in bespoke pockets that enhance durability of filaments during the bending and washing of the e-textile.

Keyword: woven filament circuits, wearable e-textiles, durable e-textiles, bending and washing reliability

A. Komolafe*, R. Torah, Y. Wei, H. Nunes-Matos, M. Li, D. Hardy, T. Dias, M. Tudor and S. Beeby

Integrating flexible filament circuits for e-textile applications