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Fabrication and Characterization of Silicon Nanowire FETs with Coupled Dopants Induced Quantum Dot

by

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ABSTRACT

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FABRICATION AND CHARACTERIZATION OF SILICON NANOWIRE FETS WITH COUPLED DOPANTS INDUCED QUANTUM DOT

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Few dopants silicon transistor has been increasingly proposed in recent years, which provides a platform to understand the MOSFET scaling issues like threshold voltage shift, device performance non-consistent and dopant distribution fluctuations. The single and few dopants localized in silicon field effect transistor (FET) channel could also be used as the quantum dot (QD) for the single electron transistor (SET), which leads to an alternative way to achieve the quantum devices against the traditional method like structurally defined quantum dot. The modern fabrication technology like ion implantation and STM provide a more accurate method to define the single dopants in channel. However, the complex fabrication process makes these methods not practical. To overcome this technique challenge, Moraru and Tabe proposed the new fabrication method with spin-on dopants and selective doping to form the dopants cluster as a quantum dot. The study of the few dopants transistor also establishes the possibility for the future transistor with molecular and atomic scale.

In this work, I introduce two generations of silicon nanowire FETs (NW-FETs) with different device designs and fabrication processes with silicon on insulator (SOI) platform. The innovation introduced is the nanowire design with notch structure. The nanowire notch structure helps to confine the dopants without thinning the silicon layer to be sub-5 nm, which reduces the complexity of fabrication process but increases the tolerance. The aim of these two generations is to develop the few dopants transistor with spin-on dopants. The rapid thermal annealing (RTA) is used for the first device batch. As for the second generation, the thermal diffusion is applied to form the clustered dopants and provide sufficient current flow at low temperature. The silicon dioxide is used as the doping mask in both experiments. The commercial device simulator software Silvaco is first used to prove the suitability of the NW-FET device design. Through the fabrication, hundreds of NW-FETs with various doping configurations are fabricated in parallel. Different Ebeam resist HSQ and ZEP are used successfully to transfer the nanowire design and the smallest width of nanowire after dry etch is around 50 nm.

For the first device generation, different NW-FETs with various device dimensions and doping configurations are measured. The short-channel effects are obtained from I-V characteristics including drain induced barrier lowing (DIBL) and gate induced drain leakage (GIDL) effects. By comparing the I-V performances of different devices at room temperature, the narrower and shorter the channel will contribute higher output current. However, the issue of the dopants freeze-out at low temperature make the device to be only measurable until 100K.

By analysing the feedbacks of the first generation device, both device design and fabrication process are upgraded for the second generation. The new spin-on dopants solution with higher concentration is used with the thermal diffusion method, which increases the doping concentration at source and drain. By comparing the device with intrinsic and doped channel, the difference between threshold voltage is analysed to be corresponding to the channel doping of approximate 5×10^{18} cm^{-3}. The QD Coulomb oscillation and Coulomb diamonds characteristics obtained at 5K indicate single electron tunnelling through localized QD. Through the analysis of the characteristics of QD, the formation of QD is due to the confined dopants under top gate are strongly coupled. The number of dopants in QD is estimated to be 4-5. Through the temperature dependent measurement, the electron transport follows the Mott variable hopping mechanism. The hopping distance is found to be 6.7 nm and the critical temperature is calculated to be 57K, which is consistent with the Arrhenius plot.

In a conclusion, the combination of thermally diffused spin-on dopants and notched nanowire successfully create the few dopants silicon NW-FET with clustered dopants. The standardized fabrication process is also established during the project. Through different measurements and analysis, the nature of QD is proved to be localized dopants deliberately doped selectively.

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Declaration of Authorship

I, Zhencheng Tan , declare that the thesis entitled *Fabrication and Characterization of Silicon Nanowire FETs with Coupled Dopants Induced Quantum Dot* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
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List of Publications

Conference Poster Publications

[1] Z. Tan, T. Iwasaki, L. Boodhoo, H. Mizuta, and H. M H Chong. Fabrication and characterization of silicon notched nanowire FETs with selective channel dopants. MNC, 27th International Microprocesses and Nanotechnology Conference, Japan, November 2014.

[2] Z. Tan, W. Zhongwang, S. Schaal, G. Agbonlahor, T. Iwasaki, M. Muruganathan, H. Mizuta, and H. M H Chong. Electron Transport of Dopants Induced Quantum Dots in Silicon Nanowire Field Effect Transistor at Low Temperature. SSDM, 2018 International Conference on Solid State Devices and Materials, Japan, September 2018.

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Chapter 1

Introduction

With the development of semiconductor industry and silicon IC technology, more transistors are arranged into one single chip for low power consumption and powerful faster operations. The number of transistors on the microprocessor changes from 8000 using 8 μm process to 10 billion using 10 nm process from year of 1971 to 2018 based on the Moore's law. As the semiconductor industry matures, the size of the fundamental device MOSFET decreases. The smaller size can make the power consumption lower and powerful integrated circuits can be created based on more MOSFETs to achieve more complicated functions. However, there are a lot of issues existed with the MOSFET scaling including short-channel effects, threshold voltage fluctuations, output current and dopants number fluctuations. Among these problems, the non-uniform distribution of dopants is an essential issue. With the size of silicon CMOS scaling down, the problems caused by random distributed dopants can lead threshold voltage fluctuation and non-uniform electrical performance from device to device [1, 2, 3, 4]. Since the nuclear spins of donor atoms in doped silicon was found that they could be used as the quantum information host [5] and the possibility to control the nuclear spin [6], the single or few dopants devices became a hot research topic. This type of single atom device uses single or very few dopants as the localized potential well to form the quantum dot for electron tunnelling transport. The accidentally random diffused dopants in channel was reported as the original proposal to produce single atom devices to study the tunnelling transport through individual dopant atom in silicon transistor [7, 8]. With the development of novel state-of-art fabrication process and understanding of atom devices, single dopant could be precisely controlled within the channel by ion implantation [9] or scanning tunnelling microscope (STM) tip manipulation [10]. These results have shown important potentials of the atom level dopant controllability, but the limitations of ion implantation or STM make the process hard to be compatible with CMOS processing technology. In order to make the device more practical with simple fabrication process, the thermally diffused spin-on dopants method was successfully applied to create the few dopants silicon transistor based on SOI platform and the electron transport spectroscopy

was obtained at low temperature [11]. However, this techniques has a restriction that the thickness of the active device silicon layer needs to be thinned down to around 5 nm, which limits the compatibility and tolerance of device fabrications. In this work, the new device design with notch nanowire is introduced. By applying the spin-on dopants and thermal diffusion techniques, the dopants induced QD is successfully created with the help of notch nanowire. The low temperature measurement results show classical quantum effects and the electron transport is analysed based on the temperature dependent measurements.

1.1 Motivations and objectives

While the few dopants effect is problematic in CMOS, the phenomena of few carriers interaction with the dopants can still be used for the device like few-dopants transistor, turnstile electron pump and memory device. Based on the few dopants transistor, the electron transport through the coupled dopants is eligible to be observed under the low temperature. This helps to understand the device performance when the device size is scaled down. On the other hand, the localised dopants can be used as the quantum dot and the device is able to show the quantum effects like Coulomb blockade and Coulomb oscillations, which provides a method to fabricate the quantum device. Various proposals report the single or few dopants FET can be achieved by the modern fabrication process with the help of ion implantation or STM method [10, 12]. Meanwhile, the corresponding electric characteristics like I-V curves and electron transport through dopant are proposed.

However, both ion implantation and STM approaches are not quite compatible with practical device. Therefore, the easier fabrication process technique needs to be developed. The technique with spin-on dopants and selective doping was developed by Moraru and Tabe [11]. By controlling the size of selective doping window and the doping concentration, devices with different doping configurations could be fabricated. Moraru and Tabe have proposed the device quantum characteristics of single and few dopants at low temperature. In order to make sure the dopants could be confined in 2D dimension properly, the thickness of silicon layer is controlled to be around 5 nm. The drawback for ultra-thin nanowire is the complicated fabrication process with little tolerance. Therefore, in this work, I aim to develop the new device structure and VLSI compatible process for parallel fabrication of few dopants QD devices on silicon on insulator (SOI) platform. I also aim to form different dopants patterns by applying different doping configurations. Meanwhile, the temperature dependence of the device operation will be discussed. In order to establish this relationship, the silicon nanowire FET (NW-FET) will be used as the main device in this project. The device simulation software like Silvaco will be used to check the device design and obtain the possible

electric characteristics. The standard MOSFET fabrication process will be applied to fabricate the device. The following objectives will be achieved during the project:

1. The models of NW-FET will be designed and simulated in commercial software Silvaco. The simulation results will be used for curve fitting with the measured characteristics.
2. Various doping methods will be applied to control the position and quantity of dopants in channel.
3. The NW-FET with different dimensions will be designed and fabricated in series.
4. The final devices will be measured at both room and low temperature. Investigations of dopant distribution and quantum electrical characteristics will be carried out.

Another aim of the project is to establish the standardised fabrication process of the few dopants silicon NW-FET for quantum application. The standardised process could help to simplify the device fabrication and reduce the turnover time of fabrication. More time and efforts could be applied for device design and characteristics, which helps to build the better understanding of dopants induced QD.

1.2 Report structures

The thesis introduces the development of fabrication process for few dopants quantum silicon NW-FET with clustered dopants. Different device designs and fabrication methods are applied, which is compared to find the best combinations for practical applications.

Chapter 2 outlines the literature reviews of the development for different types of quantum devices. Various fabrication methods and device characteristics are introduced. The development of silicon single and few dopants device are presented as a critical part. Meanwhile, the device performances are discussed, especially the charge stability and I-V characteristics. Because the few-dopants NW-FET could also be used as the SET, the theories obeyed by SET are then presented in Chapter 3, which explains the formation of quantised energy levels in QD and the corresponding electrical properties. The 2D simulations of NW-FET using Silvaco are proposed in Chapter 3 as well.

The fabrication development of first batch device are presented in Chapter 4. The device design and Ebeam lithography dose tests are introduced. Meanwhile, the device SEM images are presented to track the device structures with different fabrication steps. The measurement of different devices at room and low temperature with electric characteristics and analysis are included in Chapter 5. The short-channel effects observed

during the room temperature measurements are discussed. The device feedbacks concluded from low temperature measurements are discussed in Chapter 6. Based on these feedbacks, the fabrication process of the second batch device with improved fabrication methods are presented in Chapter 6 as well. In Chapter 7, the room and low temperature measurements of the new batch devices are highlighted. Different devices are measured and compared to analyse the existence of clustered dopants. The physics behind the QD is discussed with Coulomb diamonds analysis. Meanwhile, the single electron transport mechanism through dopants induced QD is analysed based on the measurement results obtained at JAIST.

Finally, Chapter 8 is used to conclude the achievements and various findings through the whole project, followed by the potential research directions of the future work.

Chapter 2

Literature Reviews

The potential of the quantum bits (qubits) realization in semiconductor provides a strong support to the development of electron spin study and quantum information processing. As the basic state of qubits, quantum dot formations and characteristics have been studied for many years.

Various proposals show that there are various ways to form QDs by fabrication of physical structure using different semiconductor materials as the host for quantum dots, like GaAs-based and Si-based. The GaAs-based quantum dots in GaAs/AlGaAs heterostructure are treated as the main research subjects in the early time, which are developed well because the epitaxial growth in group III-V lattice-matched materials has been studied much earlier and easier device fabrication by using photo lithography. On the contrast, the nuclear spins in the host materials phenomena cannot be avoided in GaAs/AlGaAs heterostructure, which results in relatively short spin relaxation and coherence time. The material with large fraction of non-magnetic nuclei like silicon will be a good choice to enhance the coherence time. This natural characteristic of silicon makes it to have weak spin-orbit coupling and possibility zero nuclear spin and become an ideal environment for spins in the solid state [13].

In this section, different structures and characteristics of silicon-based SET will be introduced with the results and advantages towards to recent research. The brief reviews of fabrication methods and electric performances will be introduced to provide a better image of the device operations for the silicon quantum transistor. Then the work of few dopants devices will be focused with the latest development. Through the reviews of few dopants and other quantum devices, the device structures and fabrication methods will be used as the reference for our following work after literature reviews.

2.1 Geometrical structure defined quantum dot

2.1.1 Tunnelling controlled by top gate

Takahashi *et al* [14] from NTT laboratories was one of the world's first groups who fabricated the silicon SETs in 1994. They managed to observe the conductance oscillations of drain current at room temperature as a function of gate voltage. Fig.2.1 (a) shows the design structures of SET. A 30 nm thick one-dimensional silicon wire was defined by Ebeam on p-type SIMOX (separation by implanted oxygen) wafer. The poly-silicon gate electrode was used to introduce inversion carrier layer at the top of silicon wire to provide a conduction path. The thick gate oxide was formed from 1000°C dry thermal oxidation. At the same time, two constrictions at the ends of silicon wire were formed as well. Details of the silicon wire after dry oxidation is shown in Fig.2.1 (b) with cross-sectional image of SET. During the thermal oxidation process, the oxidation on the middle part of silicon wire will be suppressed because of the stress accumulation during thermal oxidation [15]. As for two ends of the silicon wire, the oxidation process will be enhanced due to less stress accumulation. Therefore, the position of the oxidation can be modulated by the initial patterns. They gave the name PADOX (pattern dependent oxidation) to this method. As a result of PADOX, two constrictions work as tunnel barriers of electrons transition within the silicon wire, which helps the formation of single QD. The size of the silicon island can be much smaller than initial size defined by patterns and the two barriers are formed automatically. This method directly contributes a small value capacitance to SET, which makes the SET can operate at room temperature. The resistance of two tunnel barriers are relatively low from KΩ to MΩ.

One of the necessary conditions for SET to work at the room temperature is the value of total capacitance is as small as possible at around aF level. Regarding the experimental results in Fig.2.1 (d), the conductance oscillation cycle could be averaged to 500 mV and the resulting gate capacitance (C_G) is about 0.3 aF. By using the same device, they managed to get the relationship between conductance and backgate voltages (V_{BG}) under different gate biases at 28K [14]. The period of conductance oscillation cycle with various V_{BG} was 1/30 times that for V_{GS}, so that the value of backgate capacitance (C_{BG}) is 0.01 aF. Meanwhile, The drain capacitance (C_D) was estimated to be 1 aF and the source capacitance (C_S) was estimated to be smaller than 1 aF. Based on the calculations and assumptions, the total capacitance (C_Σ) of SET was concluded as $C_\Sigma = C_G + C_{bg} + C_D + C_S < 2.3$ aF. This extremely small capacitance value makes the conductance oscillation effects can be obtained at room temperature.

The general ideas of PADOX and their challenged results of SET with aF capacitance provide inspirations to the future researches. However, Takahashi *et al* [14] and [15] did not mention the charge stability of their SET in the measurements. The charge stability of a SET indicates how stable the quantum states are and how good the fault tolerance

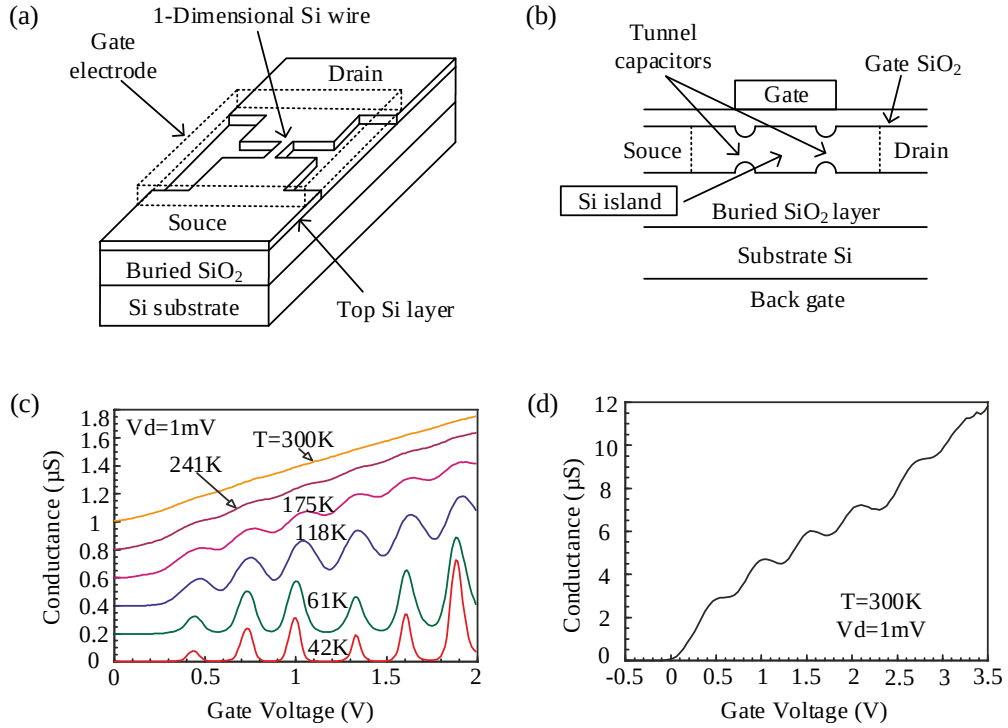


Figure 2.1: Structures and characteristics of silicon SET. The initial structure is in (a) and the cross-sectional diagram of SET after oxidation is in (b). The conductance oscillation under different temperature from 42K to 300K as a function of gate voltage (V_{GS})is shown in (c). A zoom out version of G vs V_{GS} at 300K is shown in (d). Drain voltage of 1 mV is applied for both (c) and (d) measurements. All images are from [15].

of the device is. In 2010 and 2011, Shin *et al* [16, 17] from the same group reported a sub 5nm silicon SET with high charge stability at room temperature. Based on the previous study, Lee *et al* [18] reported a silicon SET with multiple quantum states and large quantum-well spacing demonstrating single electron transport at room temperature.

The device in Fig.2.2 (a) was fabricated from the (100) silicon-on-insulator (SOI) wafer, where the 40 nm × 200 nm nanowire was defined by Ebeam lithography and helicon dry-etching. Through further wet etching, the width of nanowire was reduced to less than 10nm. Then the nanowire was suspended by etching the buried oxide in BHF, followed by the thermally oxidized to form the gate oxide. The resulting silicon nanowire after oxidation is shown in Fig.2.2 (b). As the oxide grown from all directions of nanowire, so the size of the nanowire was further reduced to smaller than 5 nm. At the same time, the QD and tunnel barriers were formed by PADOX method discussed in the previous contents. The poly-silicon/SiO_2 gate stack used to generate the inversion layer was deposited by chemical vapour deposition method and the gate-all-around (GAA) structure was shown in Fig2.2 (c). Finally, the source and drain were formed by ion implanted with 10^{20} cm^{-3} n^+ dopants.

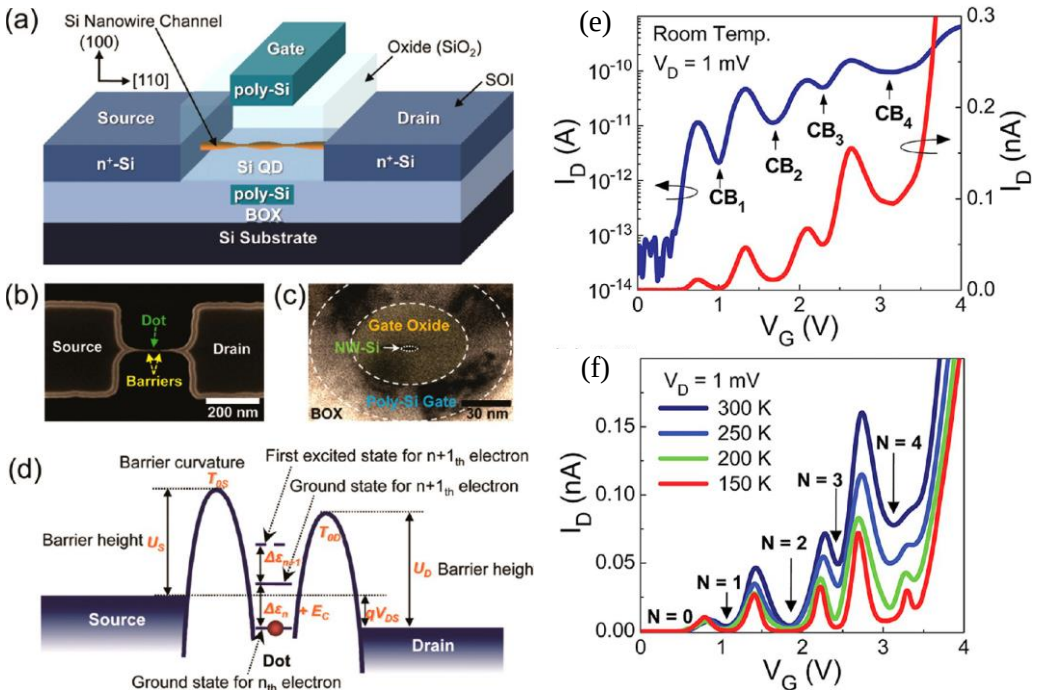


Figure 2.2: (a) Schematic diagrams of the silicon SET. (b) SEM image of nanowire after gate oxidation and the QD are formed. (c) Cross-sectional SEM picture of the nanowire after GAA structure fabrication. (d) Expected potential profile along the nanowire. (e) I_{DS}-V_{GS} characteristics at room temperature when V_{DS}=1 mV. The blue and red lines indicate logarithmic and liner scales respectively. (f) I_{DS}-V_{GS} cures under different temperatures. N is the number of electron in QD. All pictures are from [18].

Such a small silicon island introduced a great charging energy (E_C < 140 meV) and quantum level spacing ($\Delta\varepsilon$ > 75 meV) than thermal energy at room temperature, which is about 26 meV. Meanwhile, a larger gate capacitance was formed by GAA structure, which ensured the gate to control the electron transport modulation. The I_{DS}-V_{GS} relations from 150K to 300K were measured to check how many QDs were used for electron transport. CB_1-CB_4 in Fig.2.2 (e) donated four Coulomb-blockade oscillation states. Various intervals between these valleys indicated that the electron transport was modulated through the discrete quantum states of a QD. Furthermore, the positions of CB_1-CB_4 kept regular even at lower temperatures in Fig.2.2 (f), which proved there was a single QD existed in the system.

By combining the I_{DS}-V_{DS} and I_{DS}-V_{GS} curves, the spectrum of I_{DS} and conductance (dI_D/dV_D) based on V_{DS} and V_{GS} were shown in Fig.2.3. α_1-α_3 and β_1-β_3 were slopes of the Coulomb diamonds (CDs) in the charge stability diagrams. -A-A indicated the Coulomb blockade regions in Fig.2.3 (c). From Fig.2.3 (a) and (b), the Coulomb blockade regions were shown clearly at 300K and the size of Coulomb diamonds at 200K were similar to those at 300K, which indicates the high charge stability of the electron transport through single QD. The information about capacitor ratios (-C_G/C_D and $C_G/(C_D+C_s)$)

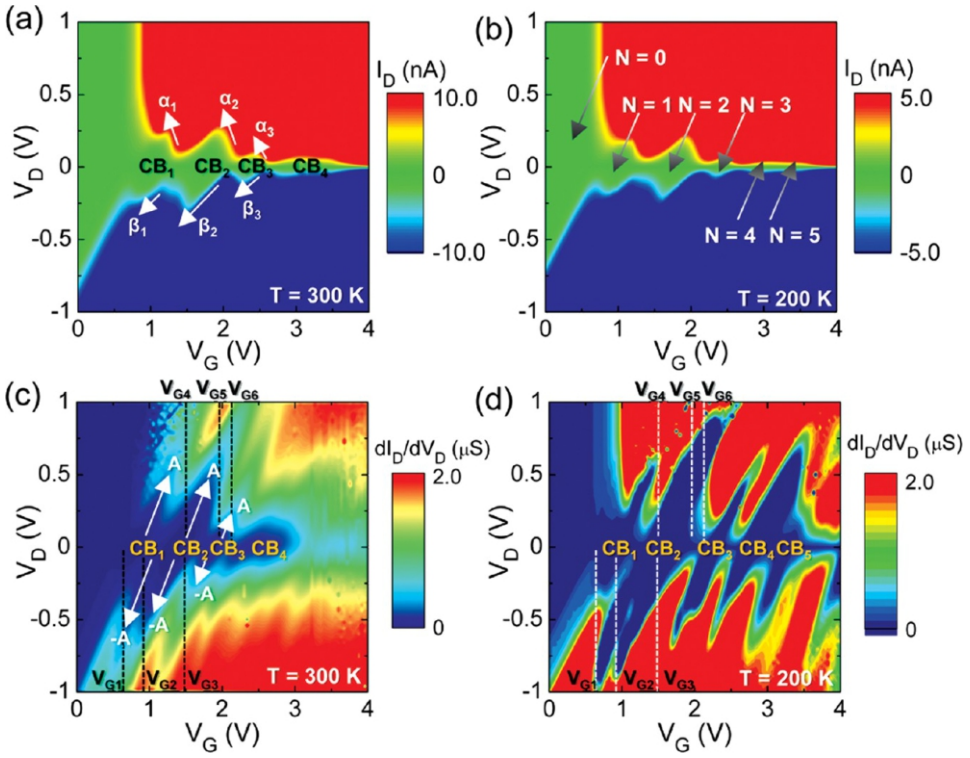


Figure 2.3: (a) and (b) show the contour of I_{DS} as a function of V_{DS} and V_{GS} at 300K and 200K separately. The corresponding conductance diagram are in (c) and (d). All images are form [18].

can be extracted from α and β. Based on experimental results, C_G:C_D:C_S=1:0.443:0.581 was calculated. Then the Coulomb blockade regions were allowed to be extended toward $\pm$ V_{DS} regions (in Fig.2.3 (c)) due to the high gate to drain voltage gain ($C_G > C_D$). This high voltage gain permitted the effective control of QD by gate potential but not the drain bias. The GAA structure single silicon QD devices reports a way to measure the single electron transport via quantum states at room temperature and can be used as an example for the sub 10 nm silicon SET study.

2.1.2 Tunnelling controlled by side gate

From the previous two examples, the top gate electrode can be used to introduce an inversion layer and control the QD operations. From other literatures, the use of side gates for controlling the carrier transport through QD are also reported.

In 2000, the group of R. Augke *et al* [19] reported a uniformly highly doped silicon SET, which is shown in Fig.2.4 (a). They wanted to use this application to solve the problem of differing geometrical and electrical structures in highly doped single electron devices. The device could not only act as single electron transistor, but also multiple tunnel junction (MJT) device with the control of side gates. The device was fabricated on SOI

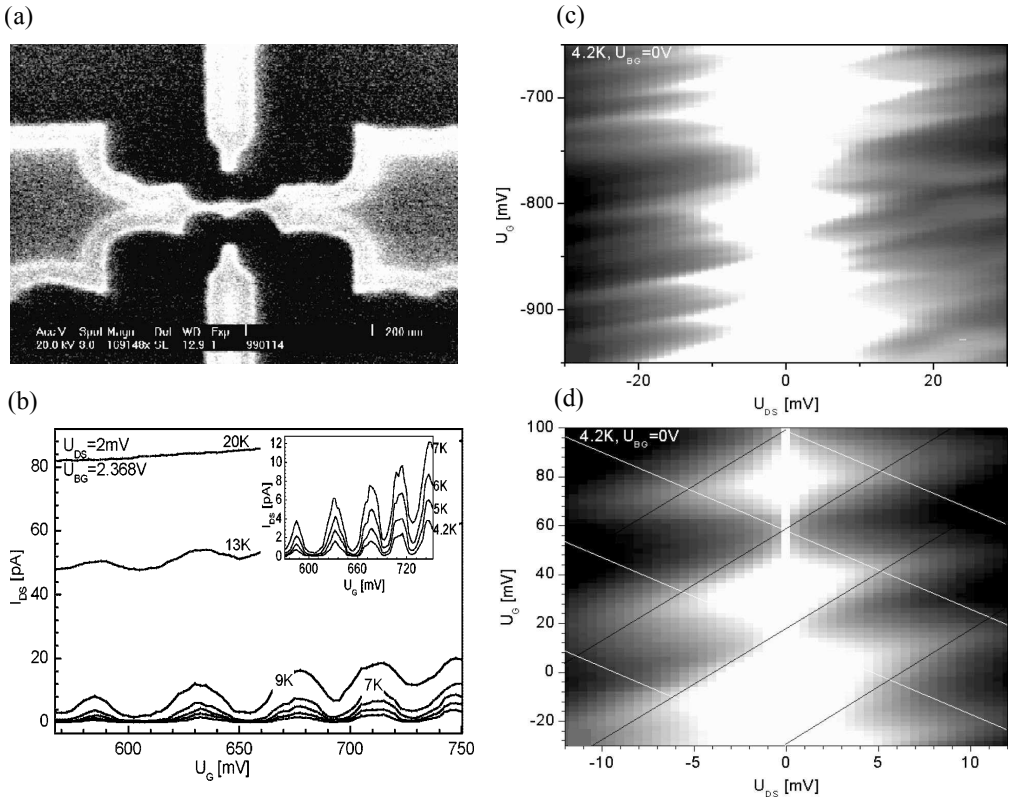


Figure 2.4: (a) shows the SEM image of the uniformly doped silicon SET. (b) and (d) are Coulomb stability plots at 4.2K under different ranges of side-gate biases. (c) represents the temperature dependent I_{DS}-U_G characteristics. All images are form [19].

platform doped with 3×10^{18} cm^{-3} n-type dopants. The single island and constriction structures were fabricated with Ebeam lithography and dry etching, followed by the thermal oxidation to reduce the island dimension and to reduce the etching damages. Due to the heavily doped silicon layers, the substrate could also be used as backgate during measurements. This backgate would be used to adjust the channel energy level so that both single electron transport and MJT could be observed.

The device was measured at 4.2K and the logarithmic Coulomb stability diagrams with different ranges of side-gate voltage (U_G) were shown in Fig.2.4 (b) and (d). When U_G was below -10 mV as Fig.2.4 (c), the irregular blockade regions could be explained that the blockade was not completely lifted and only the modulation of threshold voltage could be achieved, indicating the presence of MJT operation. With the increase of U_G, the periodic blockade regions were observed as Fig.2.4 (d) and the device performed as single electron transport. From these results, the conclusion could be summarised as the constriction geometrical structure only contributed to the device operation at high U_G but the MJT was not determined by this structure. The team claimed that the MJT was due to the random potential induced by dopants within channel. With the changing of U_G, the Fermi level was raised above the barriers of MJT, and the

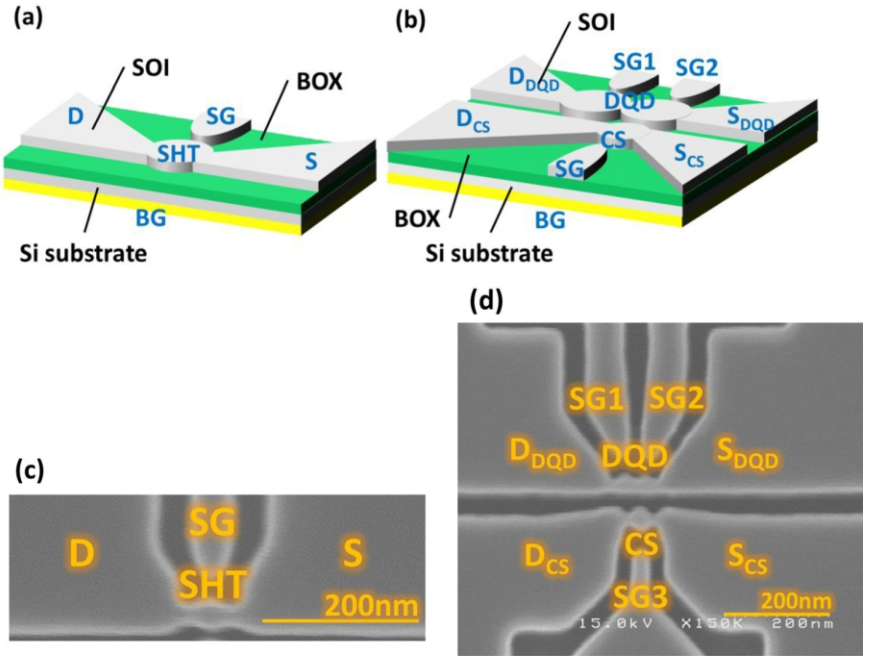


Figure 2.5: (a) and (c) shows schematic diagram and SEM image of p-channel SHT. (b) and (d) are schematic and SEM of DQD devices with SHT charge sensor. All images are form [20].

small dots merged into the larger dots. The Fermi level of dopants was raised but still below the geometrical structure barriers, and this could explain the periodic blockade regions with higher U_G. From the Coulomb stability plot, the capacitance values were extracted as C_G=3.4 aF, C_D=16 aF and C_Σ=32 aF. The corresponding charging energy was calculated to be 4.9 meV. The temperature dependent measurement was shown in Fig.2.4 (c). Based on the measurement results, the single electron charging effect could be observed at 13K but disappear at 20K. From $KT_{max}=q^2/C_\Sigma$, the T_{max} for observing single electron transport was 28K, which was quite close to the measurement results. Through this experiment, the uniformly doped silicon transistor was shown that the device could operate as MJT or SET by shifting the Fermi level of barriers of random dopants or geometrical tunnelling with side gate.

In recent researches, a group of Yamada *et al* [20] reported a p-channel silicon double QD (DQD) devices with single-hole transistor (SHT) charge sensor. The p-type $<110>$ SOI with 145nm buried oxide was used to fabricate the silicon QD devices. The structures of SHT and DQD transistors are shown in Fig.2.5 (a) and (b). The Ebeam lithography was used to write the structures of side gates (SG) and nanowire with constrictions. The back gate (BG) was used to generate the inversion layer in the silicon channel by applying negative voltage and SG was used to control the potential of QD. The two constrictions were formed by PADOX and the size was controlled to 10 nm. The source and drain reservoirs were ion implanted with BF_2^+ to form the ohmic contacts, where

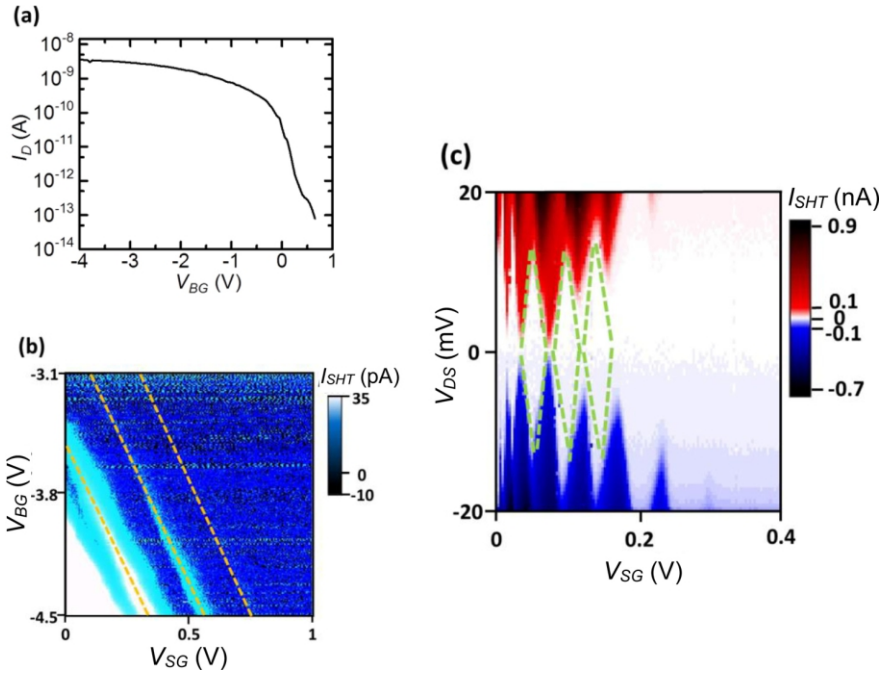


Figure 2.6: (a) ON-OFF characteristic of SHT. (b) Charge stability diagram of SHT by sweeping V_{BG} and V_{SG}. (c) I_{DS} is in a plane with various V_{DS} and V_{SG}. The CDs are represented as green dotted lines. All images are from [20].

the peak carrier concentration was around 8×10^{19} cm^{-3}. The final thickness of SHT device layer was 33 nm after fabrication.

The ON-OFF characteristic of SHT at room temperature was plot in Fig.2.6 (a). The I_{DS} was measured when the V_{BG} was swept from -4 V to 1 V. From the curve shape of I_{DS}-V_{BG}, the I_{DS} was modulated by p-channel MOSFET. The yellow lines in Fig.2.6 (b) indicated the Coulomb peaks in the charge stability diagram at 4.2K. The height and potential of the tunnel barrier was controlled by SG. The white colour of the charge stability diagram at the bottom left corner meant the tunnelling rate of holes through QD was high and the constriction barrier was strongly inverted by V_{BG} and V_{SG}. On the contrary, the top right region was the OFF state, where the tunnelling rate was low and no current went through. Based on these results, there was only one QD existed in channel. There were three stable Coulomb diamonds at 4.2K in Fig.2.6 (d) when V_{DS} was from -20 mV to 20 mV and V_{BG} was swept from 0 V to 0.4 V. Each diamond corresponded to the single-hole tunnelling through QD without any other unexpected states. The charging energy was estimated to be 16 meV according to these Coulomb diamonds (CD). The SHT shows a solution of p-channel single Si-QD transistor by using hole transport. By using hole as a spin qubit, the weaker hyperfine interaction can be found due to hole wave functions in the silicon valence band with enhanced coherence time and the manipulations of qubit [20].

2.2 Gate induced quantum dot

2.2.1 Tunnelling barriers induced by doping modulation in nanowire

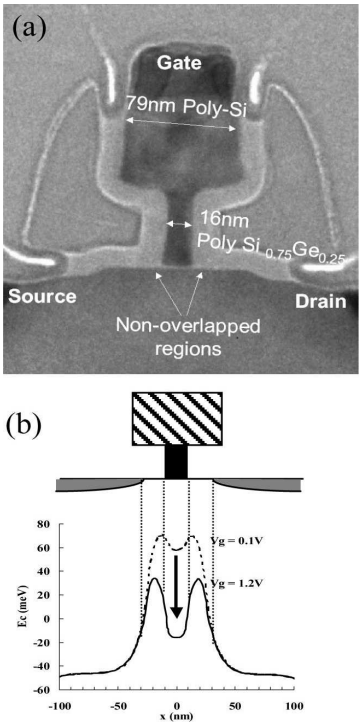


Figure 2.7: (a) The TEM image of FET, whose gate length is about 16 nm. (b) The schematic of gate-controlled electrostatic potential along the channel. The barriers are built up with higher V_{GS} and the Coulomb blockade effect will occur at low temperature. All images are from [21].

In 2003, Boeu *et al* [21] fabricated a ultra-short silicon field effect transistor (FET) with single QD with low doped channel. Instead of creating the QD with geometrical constrictions, they managed to get the low doped channel with highly doped source and drain. The non-overlapped regions between source/drain and channel were nearly intrinsic and they worked as tunnelling barriers for QD. The transmission electron microscope (TEM) image of the device is shown in Fig.2.7 (a). The non-overlapped regions prevented the short-channel effects without increasing the channel doping. The special T-shape gate stack was used as the doping mask for source/drain and provided the intrinsic non-overlapped regions. The simulation of potential profile along channel was based on the nMOS with 16 nm gate as shown in Fig.2.7 (b). The maximum barrier height was 70 meV above E_F and the center of channel was 60 meV above E_F when V_{GS} was 0.1 V. However, when V_{GS} was increased to 1.2 V, the maximum barrier was 30 meV above E_F and the center of channel was 20 meV below E_F, which makes the effective barrier height becomes 50 meV rather than 10 meV. Therefore, the 50 meV potential difference helped the channel to perform like a QD at low temperature. The low temperature

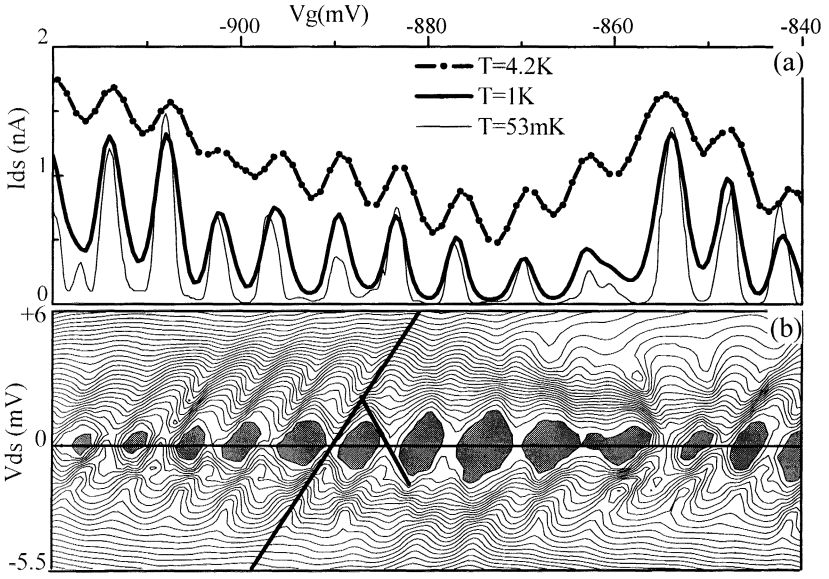


Figure 2.8: (a) I_{DS}-V_{GS} measurements at different temperatures when V_{DS} = 0.5 mV. (b) represents the Coulomb stability diagram when T = 53 mK. The blockade regions are marked with black color with $I_{DS} < 0.27$ mA. The long and short lines are applied to extract capacitor values according to orthodox theory. All images are from [21].

measurements of nMOS of width 280 nm and gate length 27 nm are shown in Fig.2.8. The current oscillations at low temperature in (a) and Coulomb diamonds in (b) indicated the presence of QD defined in channel. By applying orthodox theory of Coulomb blockade, the values of C_D was 37 aF and C_S was 7 aF, and the correspond charging energy was calculated to be around 1.2 to 1.8 meV. The compatible sizes between pMOS and QD (estimated to be 100 nm × 16 nm) also suggested that the QD was created in channel.

As for detecting the QD at low temperature, this method shows the possibility to fabricate single QD in silicon FET by modulating the doping concentration. In 2006, Hofheinz *et al* [22] reported silicon SET on nanowire with high charge stability based on doping modulation CMOS technology. The cross-section TEM image of the device is in Fig.2.9 (b) with equivalent circuits in (c). The insert image (d) shows the top view TEM image.

Device was fabricated on the SOI platform with 400 nm buried oxide and 10^{15} cm^{-3} boron doped substrate. Firstly, the silicon layer was thinned down to 17 nm, followed by Ebeam and wet etching to define the nanowire with dimensions of 200 nm × 30 nm. At this step, the whole nanowire was doped with 10^{18} cm^{-3} As. The SiO_2/poly-silicon gate stack was deposited at the middle of nanowire with length of 30 nm. Two 50 nm-wide Si_3N_4 spacers were deposited on both sides of the gate and all uncovered areas of the nanowire were highly doped with 4×10^{19} cm^{-3} As. With the help of the spacers, the

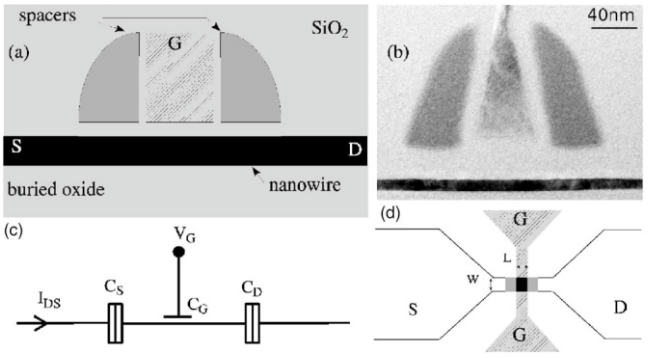


Figure 2.9: (a) The cross-sectional schematic diagram of the device with spacers and top gate. (b) TEM image of the fabricated silicon FET from cross-section views. (c) The equivalent circuit of the device. The tunnel barriers under spacers are replaced with tunnel junction box and the gate is replaced with gate capacitor. (d) The top view schematic, which shows the low doped areas under the spacer (grey color) and the silicon island under top gate (black color). All images are from [22].

channel region under gate was low doped but all other regions were highly doped. A single QD then could be created with doping modulation under the gate bias and the top gate was used to accumulate electrons in the channel. In Fig.2.10 (a), the clear conductance oscillations started from 4.2K but performed as a normal FET at 300K and 110K. The reason is that the total capacitance of the fabricated device was not as low as the charging energy to overcome the thermal fluctuations. The details will be introduced in the theory section. The resulting doping and potential profiles along the nanowire were like the simulation results in Fig.2.10 (c) and (d) separately. With the increase of V_{GS} from 0 V to 4 V, more electrons would be accumulated under the gate then the electron energy at the channel became lower than the region under spacers, so the barriers were formed at these regions. Therefore, electrons were confined under the gate as a single QD. From the conductance oscillation periods, the C_G was calculated to be around 15 aF. The regular size CDs were shown in Fig.2.10 (b), which ensured the stable electron transport and operations. The $C_S \approx 42$ aF and $C_D \approx 32$ aF could also be extracted from the CD slopes.

Based on the doping modulation method, the recent publications such as Voisin *et al* [23] fabricated a silicon FET with parallel QDs in the top surface of nanowire. These devices show simple fabrication methods using CMOS technology and stable performance, which may be a better choice for the much more complex quantum system design.

2.2.2 Tunable tunnelling barriers induced by turnstile gates in nanowire

A silicon SET with gate-induced tunable barriers using silicon nanowire MOSFET was fabricated in 2006 by Fujiwara *et al* [24]. The SET could operate as a single dot or double

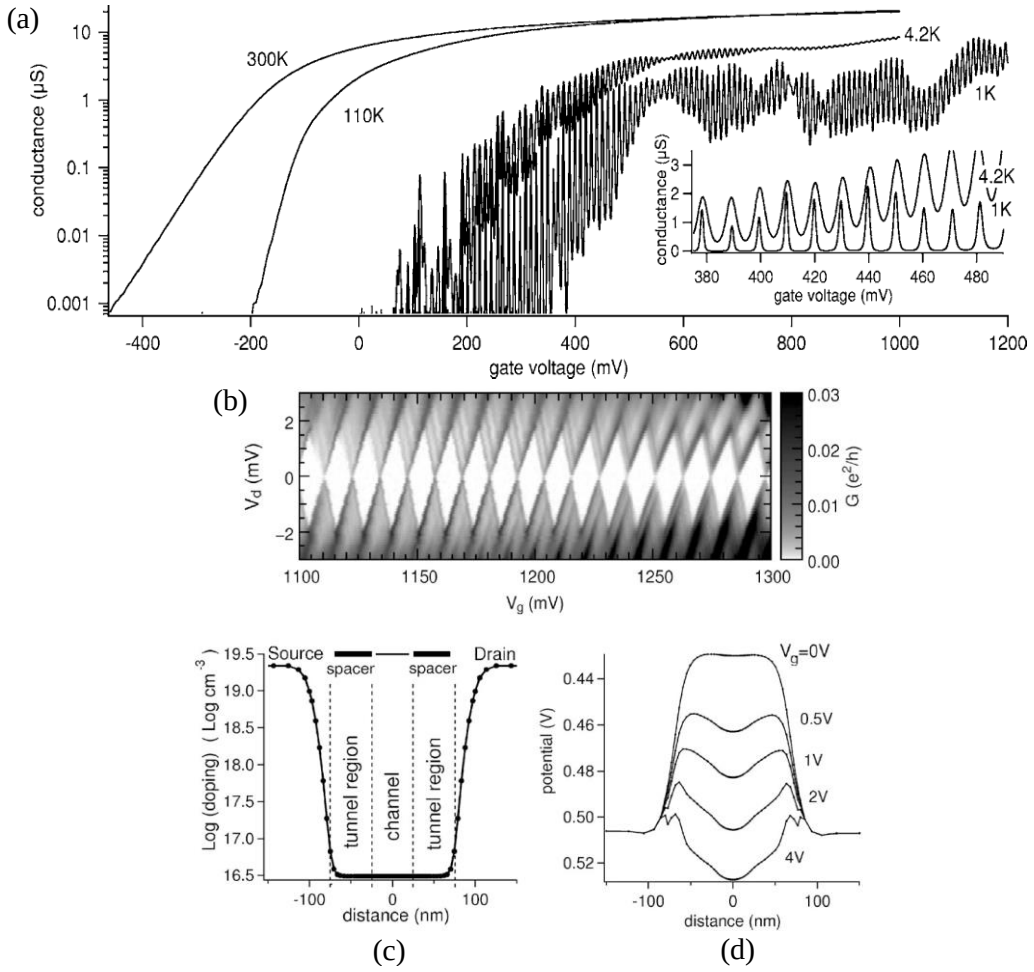


Figure 2.10: (a) Drain-source conductance oscillations as a function of V_{GS} at different temperatures. V_{DS} were 500 μV at 300K, 100 μV at 100K and 4.2K and 80 μV at 1K. (b) CD of the fabricated devices when V_{GS} from 1.1 V to 1.3 V and V_{DS} from -3 mV to 3 mV. (c) Simulation results of the doping profile along the nanowire. (d) Simulation results of the potential profile along the nanowire. All images are from [22].

dots device depending on the gate bias. The top and cross-sectional view schematic of the device are shown in Fig.2.11 (a). Three symmetrical Ebeam lithography defined lower poly-silicon gates (LGS, LGC, LGD) were used to form the barriers and control the charge island. The upper gate (UG) was used to invert the channel and control the potential of the QD. During the fabrication process, the UG was also used as the doping mask for n^+-type source and drain. The thickness and width of nanowire were both 20 nm. Each lower gate was 10 nm wide and 30 nm-thick SiO_2 was used as the spacer between lower gates and upper gate.

By applying the negative voltage bias to one of the lower poly-si gates, the electrons under the lower gate will be depleted, which results in a tunnelling barrier. The height of the tunnelling barrier could be adjusted by the potential applied to the lower gates. As

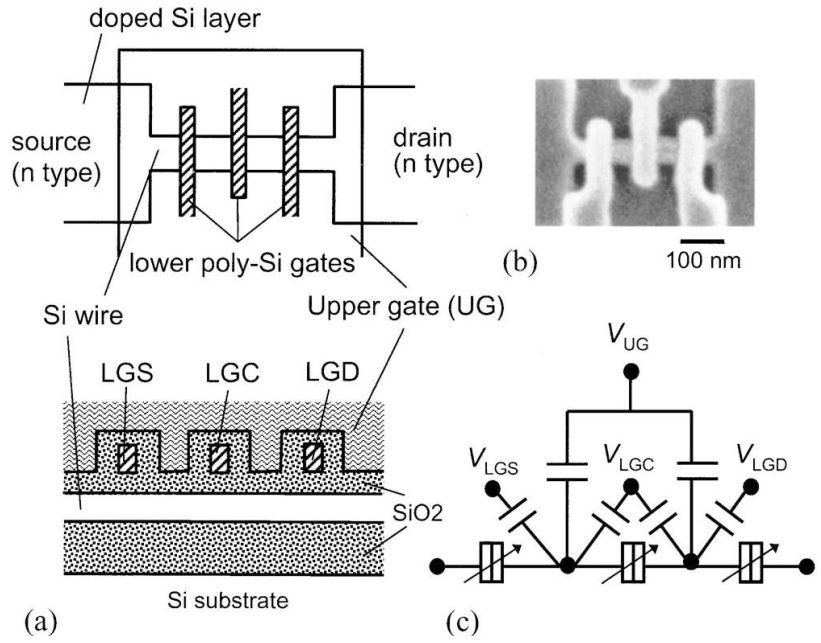


Figure 2.11: (a) Schematic of the device from cross-sectional and top view. (b) SEM image of the device before upper gate deposited. (c) The equivalent circuit with tunnelling barriers controlled by lower gates. [24]

there were three lower gates, the barrier could then be formed at different positions. For a single dot operation, negative voltage were applied to LGS and LGD. Then the region between LGS and LGD acted as a single island and the QD was controlled by UG and LGC at the same time. The source-drain conductance for single dot operation is shown in Fig.2.12 (b) and (c). When there was a single barrier under the LGD, the thermally activated conductance started to appear when $V_{LGD} >$ -1.9 V as shown in Fig.2.12 (a), because the conductance was thermally activated. In Fig.2.12 (b), two barriers were formed under LGS and LGD with G = 1 μS. The UG was used to invert the channel and the oscillations became periodic when $V_{LGC} >$ -1 V. The reason was that there was another barrier formed under LGC when $V_{LGC} <$ -1 V then the single island was divided into two smaller islands. The insert picture shown the source-drain conductance when the conductance of barriers were 8 μS, 4 μS, 1 μS and 20 nS respectively. Fig.2.12 (c) represented the CB oscillations under various V_{UG} when there was a long island. The oscillation period corresponding to UG could be used to calculate the C_G. If the long island was split into two individual islands like Fig.2.12 (d), the conductance oscillation period would be half of the period for the long island.

The SET with tunable electrical barriers can be used as single dot or double dot device by changing the gate configurations. Gonzalez *et al* [25] and Koppinen *et al* [26] reported a similar SET with single dot on a SOI nanowire and improved the charge stability. The device overviews of group Gonzalez *et al* are shown in Fig.2.13 (a) and (b). The device was fabricated on 100 nm p-type SOI platform. The source and drain were implanted

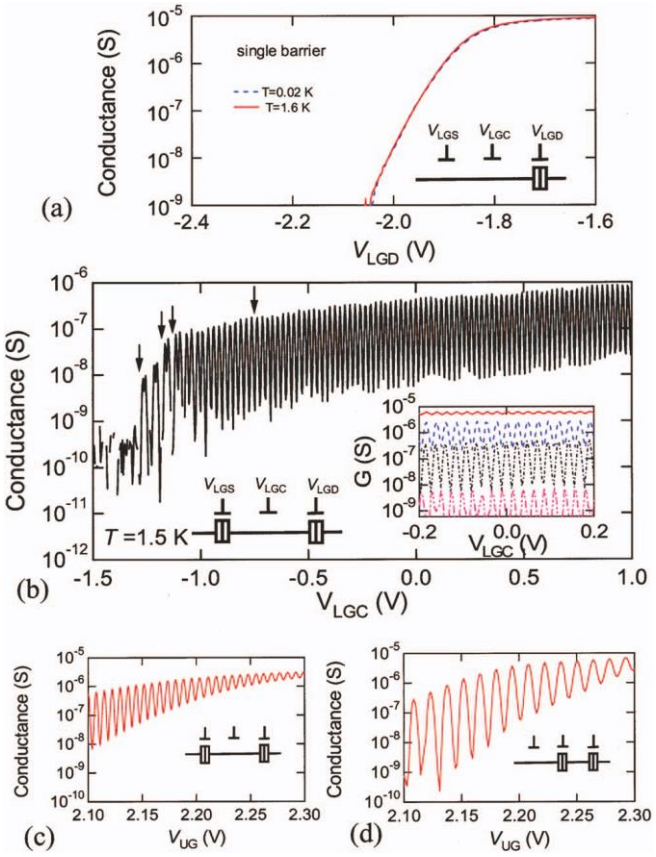


Figure 2.12: (a) Drain-source conductance for a single barrier at 1.6K and 0.02K (V_{UG} = 2 V, V_{LGS} = V_{LGC} = 0 V, V_D = 1 mV). (b) CB oscillations as a function of V_{LGC} at 1.5K when the island was formed between LGS and LGD (V_{LGS} = -2.352 V, V_{LGD} = -1.902 V, V_D = 1 mV and V_{UG} = 2 V). (c) CB oscillations as a function of V_{UG} at 1.5K when the island was formed between LGS and LGD (V_{LGS} = -2.465 V, V_{LGC} = 0 V, V_{LGD} = -1.95 V). (d) CB oscillations of the short island with barriers at LGC and LGD (V_{LGS} = 0 V, V_{LGC} = -1.426 V, V_{LGD} = -1.95 V). All images are from [24].

with phosphorous with dose 10^{15} cm^{-2} and energy of 22 keV, followed by global arsenic implant with dose 2 × 10^{10} cm^{-2} and energy of 90 keV. The Ebeam lithography was applied to define nanowire structure and the plasma dry etching was used to transfer the nanowire. 18 nm gate oxide was grown at 850°C for 55 minutes, followed by 20 minutes Ar annealing at 950°C to reduce the fixed charge density. The final dimension of nanowire was 1 μm × 25 nm × 85 nm. The 4 nm-thick AlO_x was used to separate the lower barrier gates (SB and DB) and top gate. The 15 minutes 400°C forming gas annealing was applied to decrease the interface trap charges. The resulting silicon island defined by barrier gates was 90 nm × 25 nm.

The device was characterised at room and low temperatures as shown in Fig.2.13 (c). At room temperature, the device performed like MOSFET with V_{th} = 0.1 V. At 290 mK, the conductance oscillations around the turn-on voltage 1.4 V disappeared with

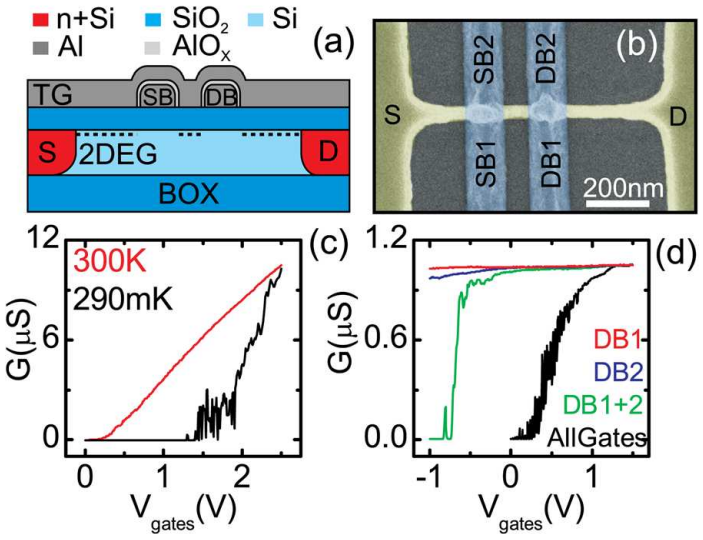


Figure 2.13: (a) The schematic cross-section of the device, which shows the 2-dimensional electron gas (2DEG) accumulated electrons. (b) SEM image of the device after low gates deposition. (c) shows the relationship of conductance with gate biases applied on all three gates under different temperatures. (d) From another device at 4.2K, which shows the dual or three gates could be used to control the device flexible. All images are from [25].

increasing V_{GS} due to well defined 2DEG along nanowire. The performance of the barrier gates was measured as shown in Fig.2.13 (d), which indicates that the dual sided gating using DB1 and DB2 could control the barriers completely. The characteristics of SET operations at 290 mK were shown in Fig.2.14. From the diagonal lines in Fig.2.14 (a), the increased current could indicate the SET island was coupled equally to both barrier gates. Meanwhile, the vertical and horizontal lines suggested that the CB oscillations coupled to each barrier strongly. And they claimed that the oscillations may come from the Coulomb blockade in potential or resonant tunnelling through dopant states. The Coulomb stability plot was shown in Fig.2.14 (b) and the corresponding charging energy was 2.1 meV. The small positive biases were applied to barrier gates to deplete the channel. The similar values of source and drain capacitance indicated that the charge island was coupled to source and drain equally. The advantages of repeatable characteristics and easy fabrication process make this type of SET to be a popular research topic in many groups.

2.2.3 Planar silicon SET based on MOS structures

All the previous SET proposals use the nanowire on SOI wafer as the start point. However, the cost of SET on SOI are higher than designing SET on bulk silicon wafers. In 1999, one of the first MOS QD was demonstrated by Simme *et al* [27] as shown in Fig.2.15. The whole device was fabricated on the bulk silicon wafer instead of SOI by

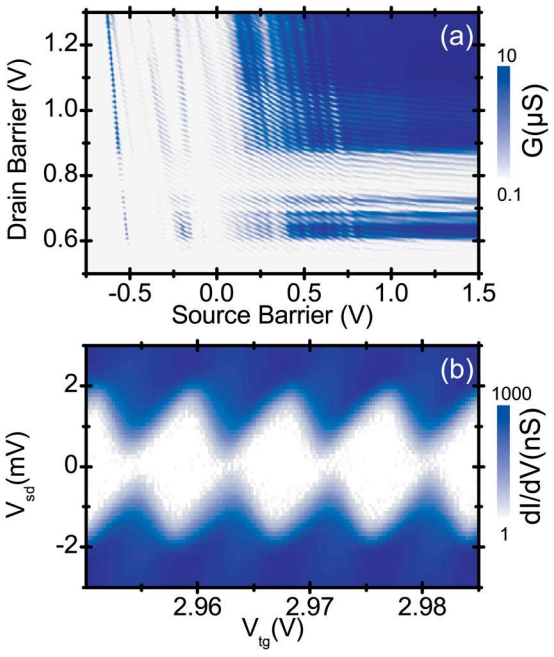


Figure 2.14: (a) The relationship between conductance and source barrier gate when $V_{TG} = 3$ V and $V_{SD} = 1$ mV. (b) Coulomb diamonds plot as a function of V_{TG} when $V_{BS} = 230$ mV and $V_{BD} = 900$ mV. All images are from [25].

using the MOS structures. In this structure, the large UG was used to introduce the 2DEG at Si/SiO_2 interface, while the four lower gates were used to screen the electrons underneath and the QD could be confined between two lower gates. The estimated dimension of QD was 200 nm × 200 nm, which was comparable to the photo lithography dimensions.

In order to reduce the UG to nanoscale, Angus *et al* [29] from University of New South Wales reported the multiple gates MOS architecture. It was developed to construct the large range of single QD by Lim *et al* [28] as shown in Fig.2.16 and double QDs by Lai *et al* [30]. Here we will discuss the proposal from Lim *et al* [28]. Three layer Al gates were separated by 5 nm Al_2O_3, which was formed by thermally oxidation of the Al gate at 150°C. The gate L1 and L2 were used to introduce the 2DEG layer in channel. B1 and B2 were used as barrier gates to deplete the electron to form tunnelling barriers. The plunger gate P controlled the electron occupancy of the confined QD. There were two annealing steps after the gate oxidation and plunger gate deposition to reduce the Si/SiO_2 interface trap density and the final trap density was reported as 1×10^{10} $cm^{-2}eV^{-1}$. The size of the QD was estimated to be 30 × 60 nm × 60 nm. The measurements were taken at 20 mK and the AC lock-in techniques were used for source-drain conductance measurements. The charge stability map as a function V_P and V_{DS} is shown in Fig.2.16 (c). The first CBD was opened completely, indicating that the QD was fully depleted of electrons. The size of diamonds after the first two were similar, which proves the device could work with high stability. Fig.2.16 (d) shows the

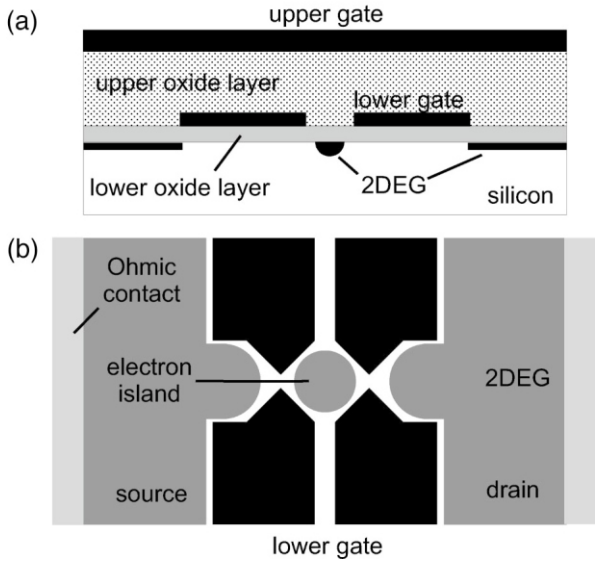


Figure 2.15: (a) Cross-sectional diagram, showing two gate layers and oxide layers. The 2DEG at Si/SiO_2 interface was induced by UG, while the lower gates depleted the 2DEG to form the QD. (b) Top view schematic, showing the four lower gates (black) and 2DEG electron layer (grey). All images are from [27].

conductance oscillation under different V_P for the first 27 electrons in QD. The insert shows the addition voltage of each electron into QD as a function of number of electrons in QD.

The successful reports of the planar type quantum device prove the current developed MOS technology could be applied to create the high standard quantum device, which could increase the chances to develop quantum device applications in the future.

2.3 Single or few dopants in silicon MOSFET as QD

The importance of dopants were realized after the development of the first semiconductor transistor [31, 32] with different types of impurities for current support. With the size of semiconductor transistor scaling down, the random distribution of individual dopant has important effects on the device performances [33, 34] like threshold voltage shift and device-to-device performance variability. With the first report on the dopants characteristics from the scaled down silicon MOSFET [35], the novel research topic about single dopant atom transistor could bring new understanding about the impacts from individual dopant atom and how the single dopant atom transistor could be used for future development. Since the dopant atoms become discrete, the interactions between electrons and dopant atoms need to be considered. By comparing to the SET with island QD, the single dopant atom device is based on the control of individual dopant and the

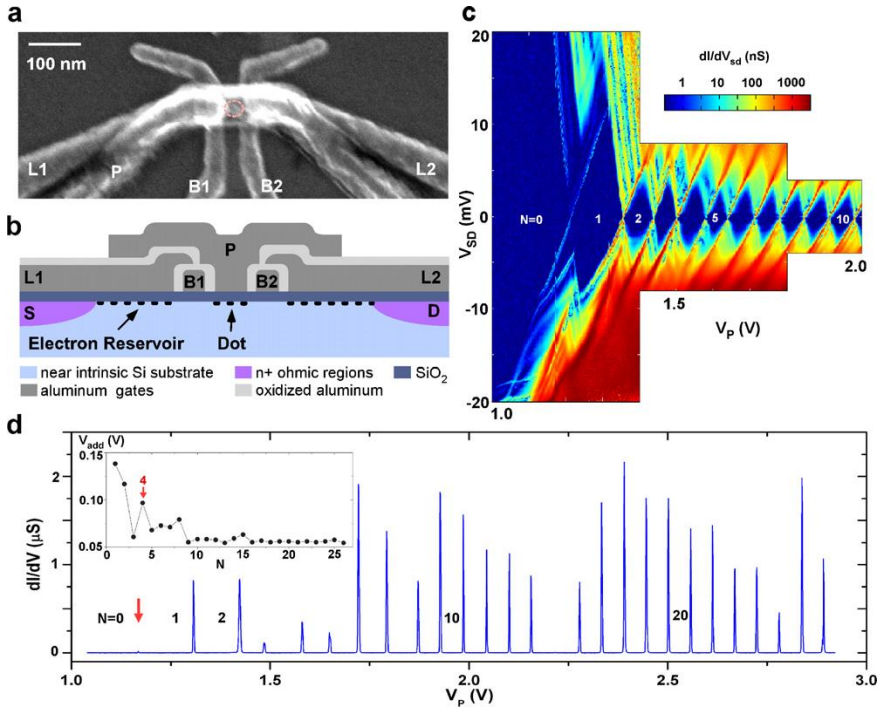


Figure 2.16: (a) SEM image of the device. (b) Cross-sectional schematic of the device. (c) CD charge stability map when V_{DS} from -20 mV to 20 mV and V_P from 1 V to 2 V. (d) Source-drain conductance oscillation as a function of V_P of the first 27 electrons in QD. All images are from [28].

single dopant atom could form the potential well for electron confinement naturally. In this section, we will review different types of single dopant atom transistors, followed by the reviews of few dopants devices with clustered dopants. Through these reviews, the fabrication process, measurements methods and the low temperature characteristics will be used as references for our device.

2.3.1 Observation of single or few dopants in silicon MOSFET channel

The single or few dopants are usually introduced into device using thermally diffusion or ion implantation methods. The number and position of dopants in device can be controlled more accurately by ion implantation. The dopants distribution along the channel is important for understanding the impacts of dopants to the device performance. Therefore, the directly observations of the electrical potential modulated by dopants become essential to characterise the nano-scale silicon transistor.

The KPFM is designed to not only measure the sample surface topography but also the potential profile along the sample. The potential is the contact potential difference measured through the electrostatic force between the cantilever and the sample [36]. With the help of low temperature KPFM measurement at 13K, the individual dopants existed

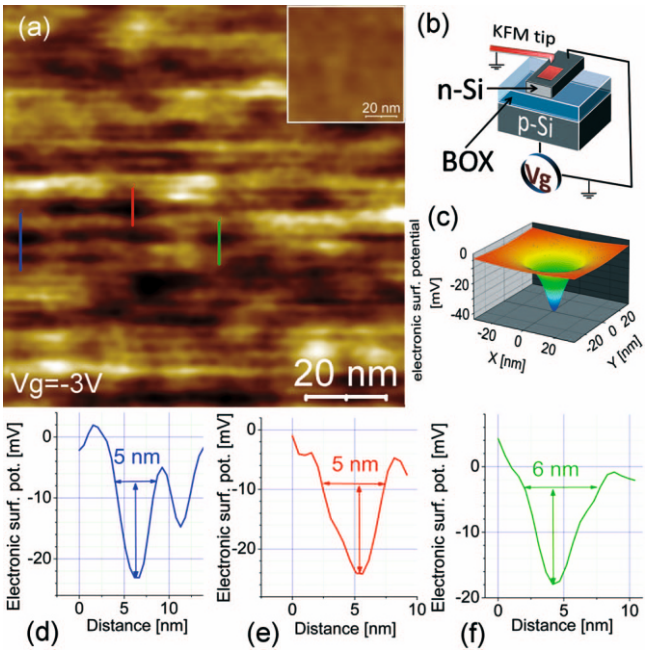


Figure 2.17: (a) The map of surface potential measured by KPFM at 13K. (b) indicates the measurement setup and the device structure. (c) is the expected profile of the surface potential with single dopant induced potential valley. (d)-(f) are the profiles of the surface potential measured at different surface positions by KPFM. All images are from [37].

in the thin silicon layer was observed Maciej Ligowski *et al* [37]. The measurement setup and results are shown in Fig.2.17.

The device used for measurement was the thin SOI-FET without top gate. The substrate was used as the backgate with 1×10^{18} cm^{-3} boron. The whole silicon layer on SOI was thermally doped with n-type phosphorus and the doping concentration was 5×10^{17} cm^{-3}. The dopants need to be ionized for the observation, which means the electrons should be depleted from the channel [38]. Therefore, the source and drain were grounded and the negative bias was applied to the backgate, which removes the free electrons through the leads. Meanwhile, the ionized phosphorus donors with positive charge were remained inside the silicon. The potential fluctuation induced by the random distribution dopants in channel could be detected by observing the channel surface potential. The map of the surface potential was obtained, as shown in Fig.2.17 (a). The electrostatic potential was measured at three different surface positions and the corresponding potential profiles are shown in Fig.2.17 (d) to (f). The diameter of the potential well at the position whose electrostatic potential was 15 mV above the valley is selected as the reference to compare the size of localised dopants. From the electrostatic potential profiles, the diameters of the potential was around 5 nm - 6 nm, which is approximate 2 times the Bohr radius of the phosphorus donor in silicon (3 nm). The measurement results of the surface potential matches the predicted electrostatic potential

profiles from single phosphorus atom in Fig.2.17 (c). Therefore, through the KPFM low temperature measurement, the single or few dopants existed in silicon MOSFET channel can be detected. With the help of this technique, the understanding of device with discrete dopant induced QD is improved [39]. Furthermore, this technique has shown potentials for other nano technology subjects like nano-scale pn junction [40] and doped semiconductor sensor for nano-biotechnology [41].

2.3.2 Device with single dopant

Dopants act as the charge provider have been studied as the basic element in silicon quantum electronics in the past decade [42, 43, 44, 45]. To observe the resonant transport through the isolated dopant, the device channel volume and the number of dopants need to be controlled in a small value. Therefore, the advanced CMOS with short and narrow channel with dopants could be used for single dopant study. Pierre *et al* [46] reported the fabrication and characteristics of single dopant device with CMOS structure as shown in Fig.2.18 (a). The device was fabricated on 200 nm SOI wafer on a CMOS platform. The 200 nm × 50 nm × 20 nm nanowire as formed by etching and 4 nm SiO_2 gate oxide was grown around the nanowire. The device was operated by single poly-silicon gate with 30 nm gate length and the gate was deposited at the central of nanowire. The source and drain were ion implanted with As and the diffusion simulation of doping was shown in Fig.2.18 (b). All the regions with a concentration above the Mott transition (n = 8 × 10^{18} cm^{-3}) were treated as the part of source and drain. As a result, the effective channel length was of the order of 10 nm. Another diffusion simulation of discrete As dopant was shown in Fig.2.18 (c) and there were some isolated dopants under the gate region. Three identical devices were measured at room temperature as shown in Fig.2.18 (d). The average threshold voltage was -0.5 V ± 0.05 V by extrapolating the maximum transconductance in the linear I_{DS}-V_{GS} curve. When V_{GS} = -2 V, the different off-state current were observed from three devices and the reason was due to the current contribution from isolated dopants under gate.

The device with high off-state current was measured at low temperature. When the gate voltage was down to -1.3 V, the differential conductance resonance appeared as shown in Fig.2.19 (a). The black lines in (a) were the thermal activation to the first resonance. The 2D plot of differential conductance versus V_{DS} at 4.2K was shown in Fig.2.19 (b). From the Coulomb diamond, the lever arm factor was extracted to be 0.16, which indicates that the orbital responsible for the resonance was coupled with source and drain more than gate. From the Coulomb diamond plot in Fig.2.19 (b), the first conductance peak represented the first As dopant with strong ionization energy due to dielectric potential confinement near the BOX interface. Based on the threshold voltage -0.5 V, lever arm factor 0.16 and the gate voltage of first resonance peak at -1.3 V, the ionization energy for the first donor was calculated to be 108 ± 10 meV, as shown

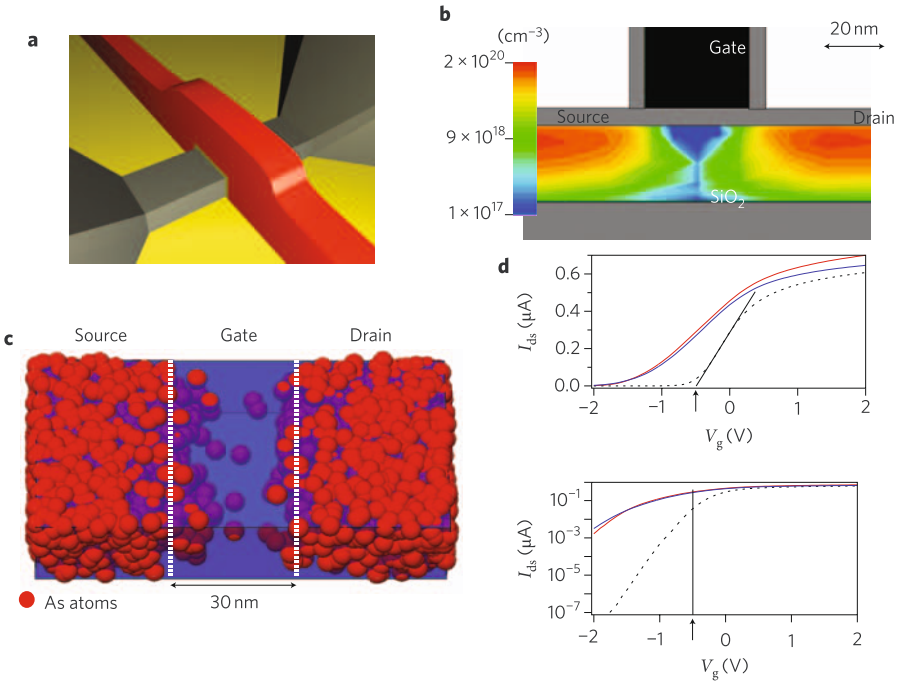


Figure 2.18: (a) The 3D schematic diagram of device with single poly-silicon gate (red color). (b) Simulation of the doping diffusion along the channel. (c) Simulation with discrete As dopants, shown in red circle with radius equals to Bohr radius 2.2 nm. The isolated dopants under gate contribute to the large off-state current. (d) Linear and logarithmic scale room temperature I_{DS}-V_{GS} characteristics of three identical devices measured with V_{DS} = 10 mV. Two devices show large off-state current and the threshold voltage is around -0.5 V. All images are from [46].

on the top energy scale in (b). The second and third resonance peaks corresponded to electronic occupations of another donor.

In this experiment, the enhanced ionization energy of single As donor due to dielectric confinement near an oxide interface was observed. Meanwhile, the CMOS structure with advanced fabrication process were proved that they could be applied for the single donor atom device study. With the development of single atom ion implantation, the positions and number of dopants can be controlled precisely and resulting in the homogeneous potential distribution along the active regions. Though there will be three main limitations using ion implantation to put dopant in channel: the control of individual ion strikes, the overall registration of ion implant sites and the untidy ions due to the nature of stopping process [13]. In 2010, Tan *et al* [12] successfully reported the control and transport spectroscopy of a single phosphorus dopant in nano-FET based on MOS structures and ion implantations technique as shown in Fig.2.20 (a).

The nano-FET was fabricated on the intrinsic silicon wafer with 10^{12} cm^{-3} P-type background doping. Ion implantation energy of 14 kev and 10 keV were used on the 100 nm × 200 nm doping area. As a result, 3 phosphorus dopants estimated to exist in

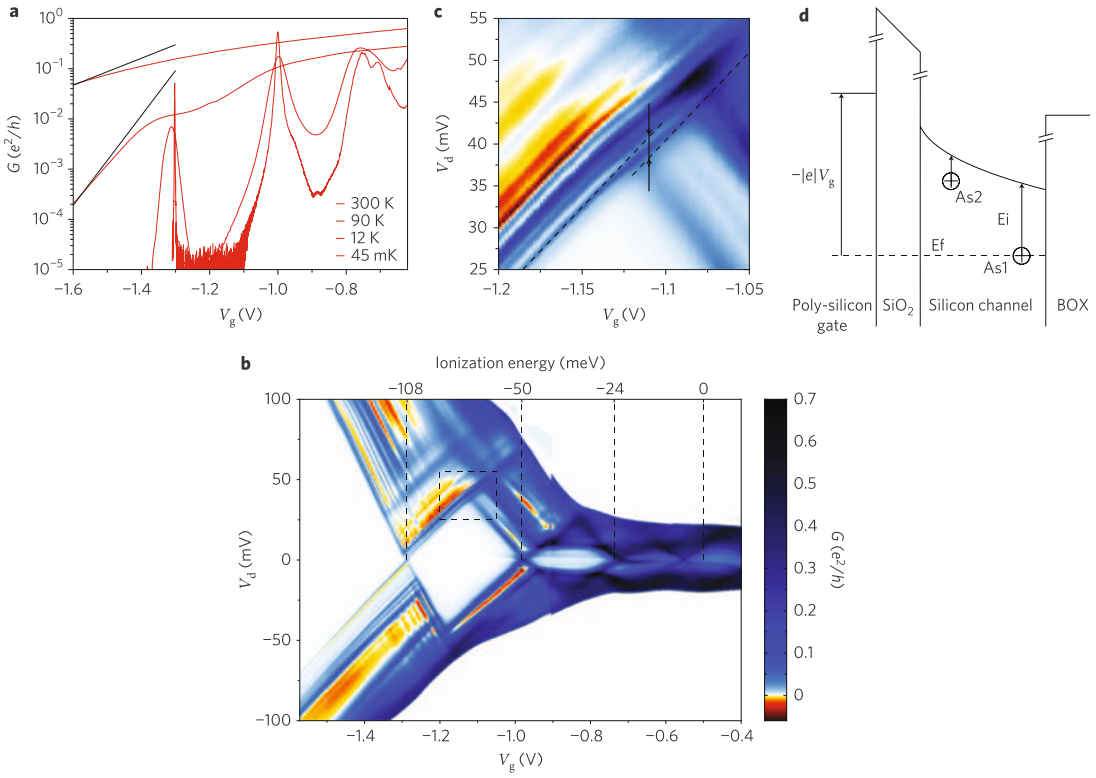


Figure 2.19: (a) The differential conductance with gate at different temperatures. (b) The Coulomb stability plot around the threshold voltage. The top horizontal scale is the ionization energy in the channel measured from the threshold voltage. (c) The zoom in details of the dashed black box in (b), where the first and second diamonds cross with each other. The arrow indicates the energy shift of the first donor. (d) The energy diagram of the device from gate to BOX. Two As donors are represented and the one closer to the BOX has larger ionization energy, which contributes to the large negative V_{GS}. All images are from [46].

50 nm × 30 nm active area. Then the dopants were activated and the damage caused by ion implantation was repaired by rapid thermal annealing (RTA) at 1000°C for 5 seconds. The source/drain were n^+ doped and the top gate was used to invert the channel. The barrier gate was used to control the energy level of three dopants and the device overviews are shown in Fig.2.20 (a)-(c). The Coulomb stability diagram with back gate was measured at temperature lower than 100 mK and the top gate bias was set to be 3.5 V. The channel turned on when the barriers became transparent. Three resonant tunnelling peaks a_1, b_1 and c_1 proved there were three dopants in the active area. Under the global magnetic field changing from 0 T up to 7 T, they found the a_1 and c_1 peaks shifted to the lower V_{BG} value and b_1 shifted to higher V_{BG} value. This shift direction information provided the spin-polarity. Therefore, a_1, b_1 and c_1 corresponded to the dopant transition from positively charged state D^+ to neutral state D^0 (spin-up electrons tunnelling) and the a_2, b_2 and c_2 were the transition from neutral state D^0 to negatively charged state D^- (spin-down electron tunnelling). Due to this experiment,

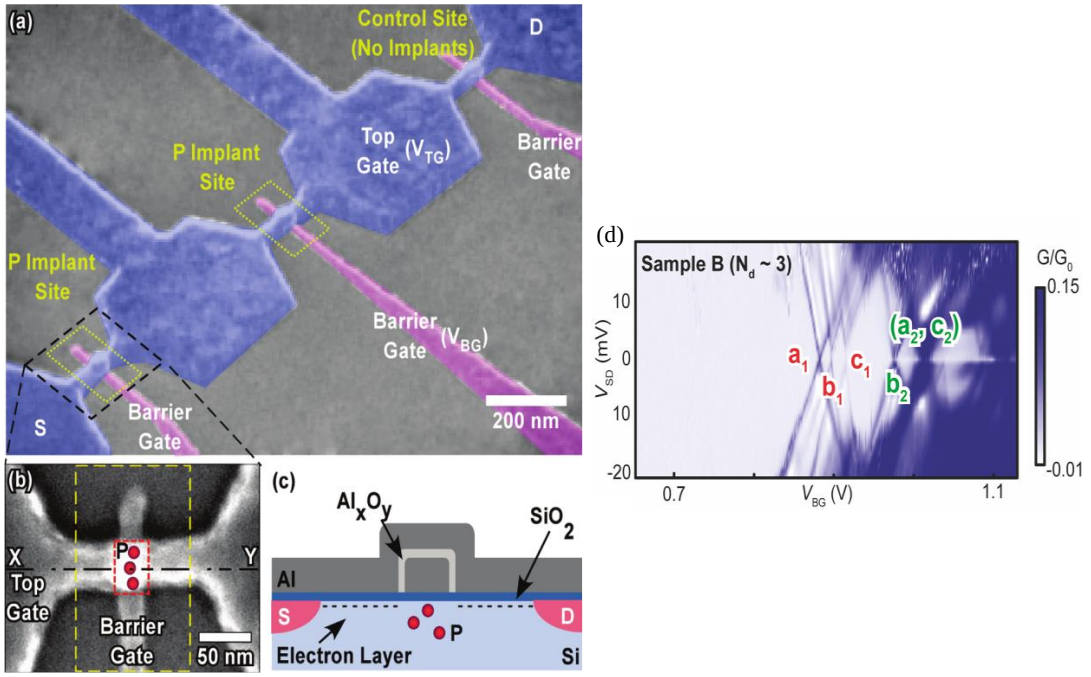


Figure 2.20: (a) Coloured SEM image of nano-FET. (b) Scaled SEM image, where the yellow line indicates the doping window and the red line is the active dopants with 3 P donors. (c) Cross-sectional schematic along XY in (b). (d) Stability diagram of the conductance as a function of barrier gate voltage (V_{BG}) and V_{DS}. Three resonant tunnelling peaks indicate three donors a_1, b_1 and c_1 are highlighted. All images are from [12].

the transport of single dopants could be observed on planar nano-FET based on dopants control.

2.3.3 Device with clustered dopants

Previous work show that the single dopant in channel could be used as quantum dot for tunnelling transport and the fabrication process to achieve the single dopant in channel is challenging. With the development of novel state-of-art fabrication process and understanding of atom devices, single dopant could be precisely controlled within the channel by ion implantation [12] or scanning tunnelling microscope (STM) tip manipulation [10]. These results have shown important potentials of the atom level dopant controllability, but the limitations of ion implantation or STM make the process hard to be compatible with CMOS processing technology. There are several proposals shown that the single-electron transport also can be observed in the heavily doped silicon device [47, 48]. In order to make the device more practical with simple fabrication process, Moraru *et al* [11] reported the thermally diffused spin-on dopants method was successfully applied to

create the few dopants silicon transistor based on SOI platform and the electron transport spectroscopy was obtained at low temperature. The device schematic with different doping profiles are shown in Fig.2.21.

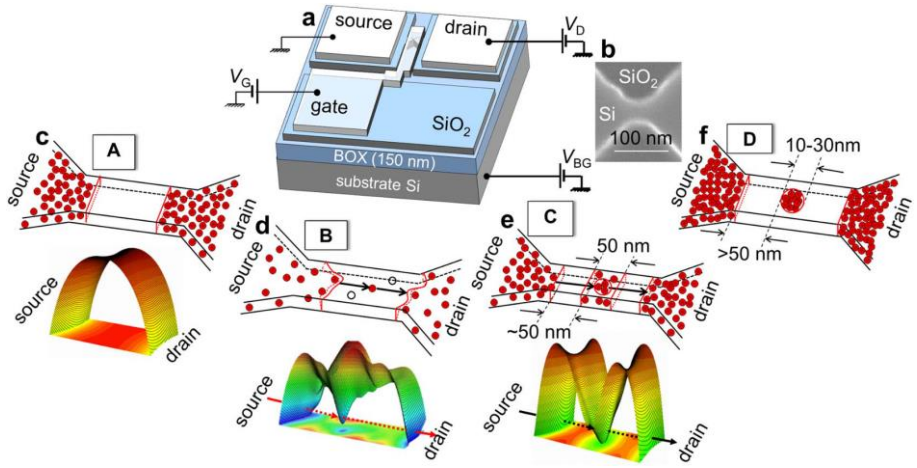


Figure 2.21: The device schematic and SEM image are shown in (a) and (b) separately. (c)-(f) show the different expected doping situations with corresponding potential landscape: (c) is the device A, that represents the intrinsic device without doping; (d) is the device B, which is randomly doped with $N_D \cong 1 \times 10^{18}$ cm^{-3}; The device C in (e) is selectively-slit-doped with $N_D \cong 5 \times 10^{18}$ cm^{-3}; Device D in (f) is selectively-circle-doped with $N_D > 1 \times 10^{19}$ cm^{-3}. All images are from [11].

The FET device was fabricated on the SOI platform. The dimension of final nanowire was 150 nm $\times$ 100 nm $\times$ 5 nm. The ultra-thin channel could make sure enough potential confinement to the dopants. SiO_2 was used as the doping mask for selective doping. There were four devices as shown in Fig.2.21, each of them had different doping profile along the channel. Device A and B were used for comparison so we will focus on device C and D. For the device C in Fig.2.21, the central region of the channel was doped by thermal diffusion through the 30-nm-wide slit doping window. The 70-nm-wide intrinsic gaps between the central doping area and the source/drain were applied to isolate the dopants. In order to minimise the thermal budget, the dopants drive in process was run with the gate wet thermal oxidation. By estimating the dopants lateral diffusion, the width of the central isolated dopants was 50 nm and the width of the non-doped gaps are 50 nm as well. Through the doping mask and dopants drive in process, the result doping concentration was around 5×10^{18} cm^{-3}. This high doping concentration was used to form the dopants cluster with strongly coupled dopants. According to the dimension of the doping region, 50 nm $\times$ 50 nm $\times$ 10 nm and their assumption about the distribution of dopants, at least one dopants cluster with multiple donors can be found within the doping region. As for the device D in Fig.2.21 (f), the higher doping concentration with $N_D > 1 \times 10^{19}$ cm^{-3} was applied to increase the possibilities of

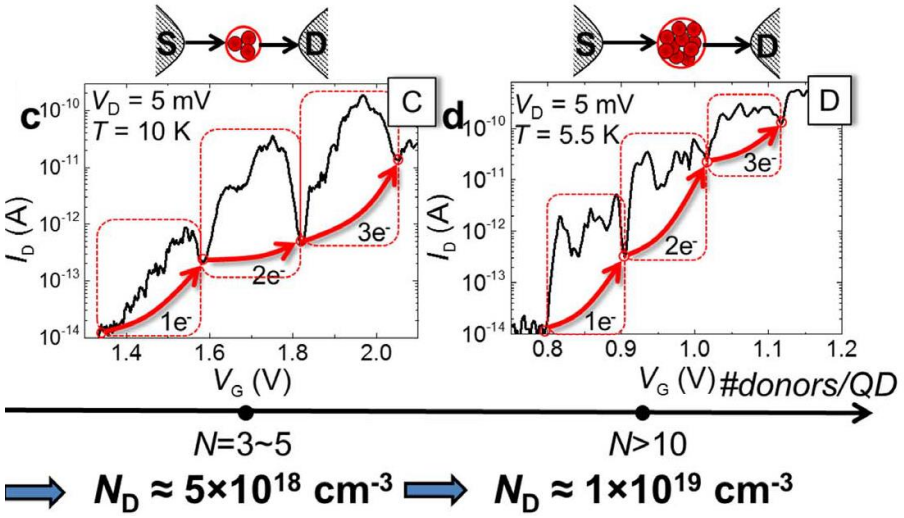


Figure 2.22: The I_{DS}-V_{GS} curve of the device C and D when V_{DS} = 5 mV are shown. The letter 'N' represents the predict number of dopants in cluster. All images are from [11].

dopants cluster formation and enhance the coupling effects between donors. The doping process was applied by using a circular doping window with diameter of 10-30 nm.

The electrical characteristics of the devices were obtained at low temperature around 15K. The electrical characteristics of device C and D are shown in Fig.2.22. The I_{DS}-V_{GS} curve of the device at low temperature shown isolated current peaks with the gate voltage increasing, which indicates the single-electron tunnelling transport. This evidence indicates that the coupled dopants acted like a QD in the channel for charge transport. However, the I_{DS}-V_{GS} curves of device C and D perform differently. The I_{DS}-V_{GS} relationship of device C represents that there were several repeated current peaks envelope as gate voltage increases from 1.4 V to 2 V. These current envelops appeared with the periodic V_{GS} spacing of 0.2 V and presence of sub-peaks features along the current peak envelop also repeated with the consecutive envelop. Through these phenomena, the current peak envelops indicate that the single-electron tunnelling effects occurred via the few dopants induced cluster QD. The I_{DS}-V_{GS} relationship of heavily doped device D also shown the similar current envelops. The V_{DS} was set to be 5 mV and V_{GS} was swept from 0.8 V to 1.2 V. By comparing the I_{DS}-V_{GS} relationship of device C and D, the current features in the envelop of device D had more inflections. The reason was that the device D had higher doping concentration and the estimated number of dopants was larger than 10, which is much higher than that of in device C. As a result, in device D, the stronger interaction between dopants in cluster brought more inflections in current envelop.

In 2015, Tyszka *et al* [49] reported the SOI-FET which contains the dopants cluster as the QD for single-electron tunnelling operation. The sub-10 nm-thick silicon was doped with

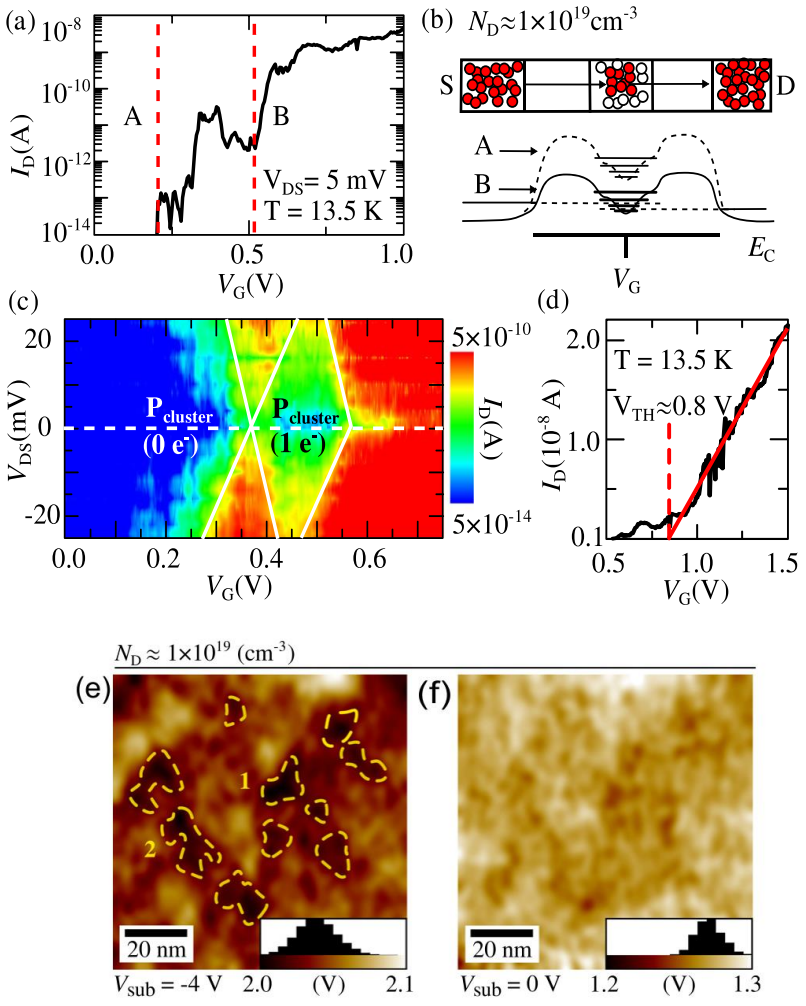


Figure 2.23: (a) The low-temperature I_{DS}-V_{GS} curve when V_{DS} = 5 mV with small V_{GS} sweep. (b) The possible schematic of the dopants distribution and the potential profile along the lines A and B in (a). (c) The stability diagram is represented with one coulomb diamond. (d) The linear fitting of the I_{DS}-V_{GS} curve at low V_{GS} and the threshold voltage is calculated to be 0.8 V. (e)-(f) The SOI-FET surface potential maps are measured by KPFM with different backgate biases. All images are from [49].

spin on dopant method with the SiO_2 doping mask. The non-doped regions were used to isolate the central dopants to be depleted efficiently. The resulting doping concentration was around 1×10^{19} cm^{-3}. The device without top gate was also fabricated for KPFM measurement. The I_{DS}-V_{GS} curve was obtained when temperature was 13.5 K and V_{DS} was 5 mV. The measurement results are shown in Fig.2.23. Similar I_{DS} peak envelops were obtained with the gate voltage swept from 0 V to 1 V. The sub-peaks feature inside the envelop indicates the energy state density in the cluster QD as in Fig.2.23 (b). At the region B in Fig.2.23 (a), one electron was occupied in the QD and the following electron transport could be described as the single-electron tunnelling with one electron occupied inside QD. The sub-figure (c) is the stability diagram combined with the I_{DS}-V_{DS} and

I_{DS}-V_{GS} curves. The blue open region at lower gate voltage indicates the empty QD. When the gate voltage was between -0.35 V and 0.55 V, the coulomb diamond could be found with higher I_{DS}. This could be explained by one electron occupancy inside the QD. With the V_{GS} increasing, the coulomb diamond vanished and the output current became much higher. Therefore, the value of V_{GS} just before the red zone in Fig.2.23 (c) was the threshold voltage. By applying the linear fit of the I_{DS}-V_{GS} curve as (d), the threshold was calculated to be 0.8 V. From the stability diagram and the value of threshold voltage, the electron transport below the V_{th} was dominated by single-electron tunnelling within the dopants cluster QD. Another evidence for the dopants cluster QD in channel was the KPFM images shown in Fig.2.23 (e). The deeper colour on the potential map means that there were coupled donors within that region when the negative voltage was applied to the backgate. This phenomena can be suppressed by increasing the backgate bias due to electron screening as sub-figure (f).

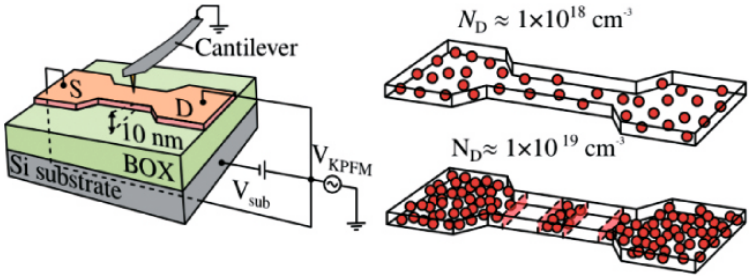


Figure 2.24: (a) SOI-FET device with the setup of KPFM measurement at the channel region. (b) Device with low channel doping concentration of $N_D = 1 \times 10^{18}$ cm^{-3}. (c) Device with high channel doping concentration of $N_D = 1 \times 10^{19}$ cm^{-3} and selective doping. All images are from [50].

Tyszka *et al* [50] also reported the surface potential profile details of clustered dopants with KPFM technology. The schematic diagram of the KPFM measurement and devices are shown in Fig.2.24. The devices were fabricated on SOI platform with thin nanowire (< 10 nm) structure. Two devices with different doping profiles were applied for comparison as shown in Fig.2.24 (b) and (c). The device in (b) had uniform channel doping and device in (d) had selective channel doping with higher doping concentration. For the KPFM measurements, the group designed devices without top gates and with ultra-thin oxide layer. The backgate was used as the gate to control the channel potential during KPFM measurements. For real I-V measurements, all devices had Al top gate and thick gate oxide.

The room temperature KPFM measurement results are shown in Fig.2.25 for both devices. The surface potential for device with lower doping concentration is shown in Fig.2.25 (a). The negative backgate voltage V_{SUB} = -4 V was applied to remove electrons in channel and P donors remained ionized in the channel. The fine potential features could be observed within 100 nm × 100 nm region. The line profiles of surface potential were shown in the right panel of (a), which was measured under different V_{SUB}.

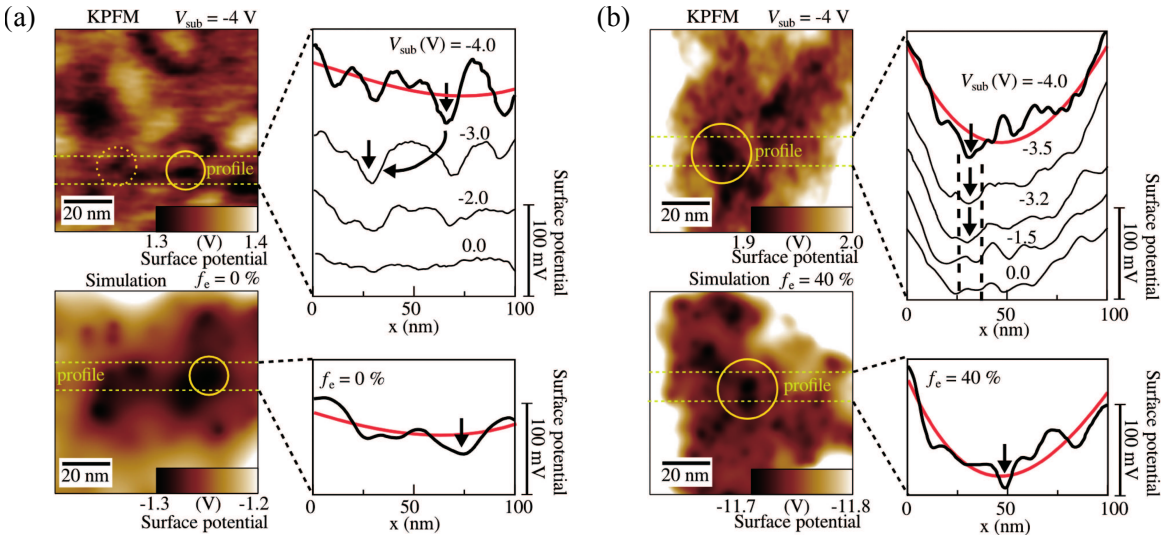


Figure 2.25: (a) Surface potential of device with low channel doping concentration of $N_D = 1 \times 10^{18}$ cm^{-3}. (b) Surface potential of the device with high doping concentration $N_D = 1 \times 10^{19}$ cm^{-3}. The diagrams at bottom are simulated surface potential profiles. The right side line curves are profiles cross the channel potential under different backgate biases. All images are from [50].

With the increase of V_{SUB}, the minimum potential position changed significantly. This suggested that the QD position was sensitive to the backgate bias. For device with higher doping concentration, the KPFM surface potential was shown in Fig.2.25 (b). The device channel was selectively doped and isolated from source and drain by intrinsic regions. V_{SUB} = -4 V was applied to deplete the channel and the result surface potential was shown on the right panel of (b). Under the same V_{SUB} bias, the surface potential was enhanced by comparing to the device with low doping concentration. With increasing V_{SUB}, the position of the minimum potential remained localized at the same area and close to the centre of channel, which was the selective doping region. The dark region within circle indicated the QD formed by strongly coupled P donor, which results in the macroscopic U-shape potential background.

Low temperature measurements were carried out using the similar device with Al top gate. The source-drain bias was controlled to be small as $V_{DS} = 5$ mV and the device was measured at 15K and lower temperature for clear single electron transport signal. The measurement results are shown in Fig.2.26. The images of Fig.2.26 (a)-(c) represent the device with low channel doping concentration. The isolated current peaks with irregular period in (a) were due to the different individual P donors at channel. By extracting the lever-arm factors from Coulomb stability plot in (b), the first three factors were 0.43, 0.64 and 0.51 for the first three diamonds. The different values of lever-arm factors also indicated that the current peaks were due to QDs with different coupling to the gate. With the help of the simulated potential landscape in (c) and C_D/C_S ratios, the position of QD changes along channel with V_{GS}. This analysis supported that the current peaks

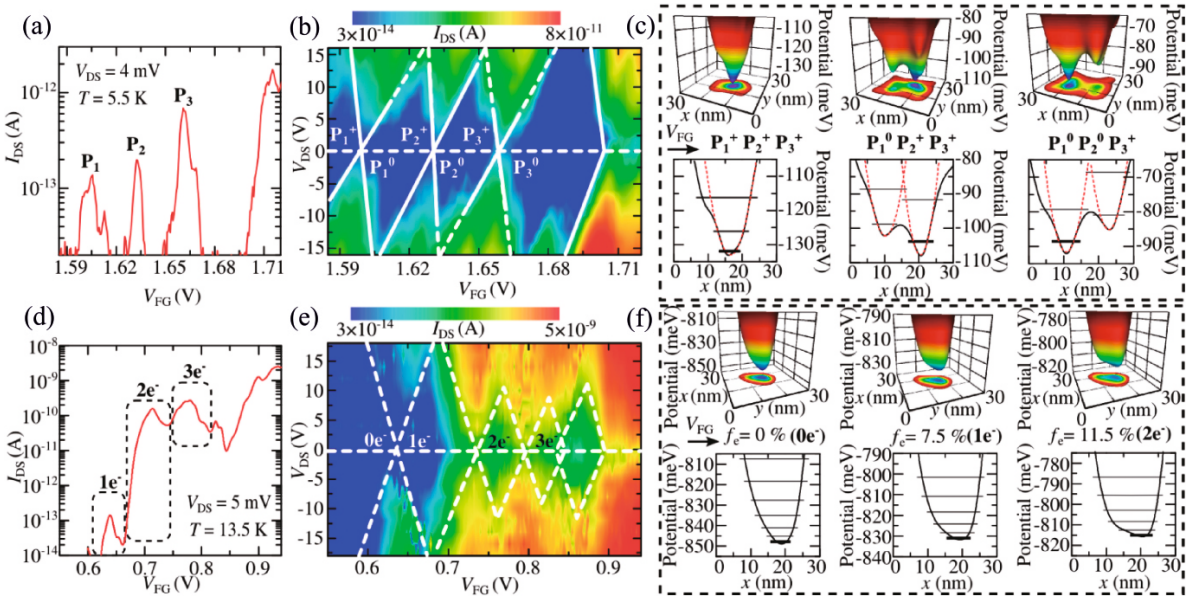


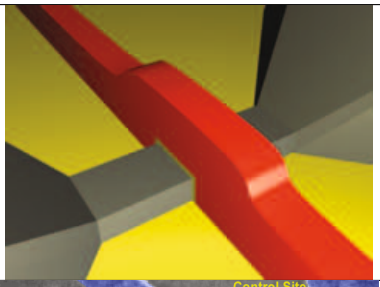
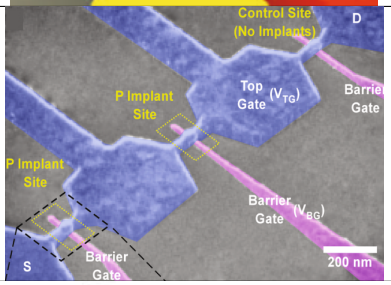
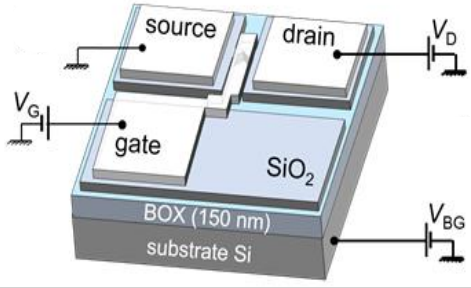
Figure 2.26: (a)-(c) are results for device with low channel doping concentration. (d)-(f) are results for device with high channel doping concentration localized at the centre position. The I_{DS}-V_{GS}, Coulomb stability plots and simulated potential landscapes are shown for each devices. All images are from [50].

were from different individual P donors. For the device with high doping concentration at central of channel, the I_{DS}-V_{GS} curve presented current envelop rather than isolated peaks. Due to the high doping concentration, the background current level was high as shown in stability diagram. From the stability diagram, several Coulomb diamonds with similar features could be observed, which suggests that the multiple electron occupancy for the same QD. The QD was formed by cluster of dopants with strong interactions of number of P donors. The simulated potential profile also could be an evidence. By adding the single electron to QD, the position of QD did not change significantly. All the results shown the location stable donor cluster on single electron tunnelling transport.

From the previous literature reviews, the characteristics of SET with different designs have been studied well. With the size of transistor scaling down, the random distribution of dopants in channel will cause irregular device performance. With the help of modern fabrication process, the position and number of dopants in channel could be controlled. Besides the structured QDs, dopants have been proved to act as the QD as well. Single-electron transistor based on few dopants devices have shown strong carrier-dopant interaction and single-electron tunnelling transport phenomena between dopants. Although the fabrication of single dopants QD is challenging, the QD induced by clustered dopants are possible. Instead of ion implantation, the method of spin-on dopants could be used to simplify the fabrication process and increase the tolerance. Different single and few dopants devices are summarised in Table.2.1. All of the selected

devices show single electron tunnelling transport through single or few dopants induced QD.

Table 2.1: Three literatures about the single or few dopants induced QD with the device schematics and the briefly introduction is concluded.

Device structure	Reviews
	The silicon CMOS is designed for single dopant application. The QD is formed by random diffused As donor under the top poly-silicon gate. Clearly quantum effects are measured at low temperature.
	The silicon MOS structure device is doped in the central channel with ion implantation. The lower gate is used to control the single dopant QD and the upper gate is used to create the channel. The number of donors in channel is predicted to be three.
	The selective doping process through the SiO_2 doping mask is used on this SOI-FET. Different types of dopants induced QD can be formed by single dopant or dopants cluster. Meanwhile, the single-electron tunnelling transport through single or coupled dopants can be measured.

The idea of device with clustered dopants reduces the complexity of device fabrication by applying selective doping and thermal diffusion. However, the thickness of the silicon device needs to be controlled to around 4 nm from literature reviews. The ultra-thin channel is used for better potential confinement of clustered dopants. Therefore, in this work, the main target is to develop the new device design and fabrication process to improve the device's tolerance. The new notched nanowire design will be developed to provide essential potential confinement without thinning down the silicon layer down to 4 nm. Different device performances will be compared at room and low temperatures to validate clustered dopants QD. From the literatures, the QD with clustered dopants can be created based on NW-FET devices and the doping concentration needs to achieve around 1×10^{18} cm^{-3}. By summarising the device designs of few dopants NW-FETs, the size of selective doping window on nanowire is approximately 50 nm $\times$ 50 nm. And the width nanowire is about 50 nm - 100 nm for better confinement. All of these information will be used as the initial parameters to the device design.

Chapter 3

Theoretical Background and Device Simulations

3.1 Theoretical background theories of SET

Since few dopants FET performs similar to the silicon quantum dot device and the cluster dopants can be treated as the QD, silicon SET can be used as the reference to explain the electron transport through QD. An assumption is made that the few dopants are strongly coupled and the corresponding dopant cluster can be treated as a QD.

SET is considered as a solution of the MOSFET scaling problems. The SET is a single electron device with ON and OFF state controlled by single electron tunnelling through the tunnelling barrier junctions. The basic structure of SET is similar to the MOSFET. And SET can be treated as a FET with small and low capacitance island coupled to the source and drain electrode by two tunnelling junctions. The gate coupled to the island is used to modulate the transport and electron energy occupancy of the QD. In this chapter, the basic theory of QD and Coulomb blockade will be introduced firstly, followed by the electron transport operation of the SET.

3.1.1 The basics of Coulomb blockade

Assume that the nano-scale capacitor with capacitance C between two metal electrodes with a positive bias applied. The charge stored in the capacitor plates are Q and -Q separately. Therefore, the initial energy E_i stored in the electrical field is [51],

$$E_i = \frac{1}{2}CV^2 = \frac{Q^2}{2C}. \tag{3.1}$$

If there is an electron tunnelling through the capacitor from the negative terminal to the positive terminal. Then, the charge on the positive terminal plate becomes Q+q.

And the new energy stored in the capacitor becomes [51]

$$E_f = \frac{(Q+q)^2}{2C}, \tag{3.2}$$

where E_f represents the final energy. And the value of q here is -1.6 $\times$ 10^{-19} C. Thus, by comparing the energy before and after the electron tunnelling, the change of the stored energy is [51],

$$\Delta E = E_f - E_i = \frac{q(Q+q/2)}{C}. \tag{3.3}$$

The change of the energy needs to be negative for the electron tunnelling to happen because this process is energetically favourable, so the following conditions can be obtained [51],

$$\begin{aligned} \Delta E &< 0, \\ \Rightarrow Q &> \frac{-q}{2}, \\ \Rightarrow V &> \frac{-q}{2C}. \end{aligned} \tag{3.4}$$

At the same time, the voltage across the capacitor will decrease by $|q|$/C due to the single electron tunnelling. On the other hand, another condition can be calculated with the same method if the electron tunnels from the positive terminal to the negative terminal [51],

$$\begin{aligned} \Delta E = \frac{q(Q-q/2)}{C} &< 0, \\ \Rightarrow Q &< \frac{q}{2}, \\ \Rightarrow V &< \frac{q}{2C}. \end{aligned} \tag{3.5}$$

By combining these two conditions, the condition for one electron to tunnel through the nano-scale capacitor is [51],

$$\begin{aligned} V > \frac{|q|}{2C}, V < -\frac{|q|}{2C}, \\ E_C = qV = \frac{q^2}{2C}. \end{aligned} \tag{3.6}$$

The energy E_C is called the charging energy and this effect is the Coulomb blockade. The charging energy is the minimum energy needed for single electron transport through the nano-scale capacitor. The Coulomb blockade can also be treated as the suppression effect due to charge repulsion. With the Coulomb blockade effect, the resulting I-V relation is shown in Fig.3.1. The region between $\pm|q|$/2C represents the Coulomb blockade region.

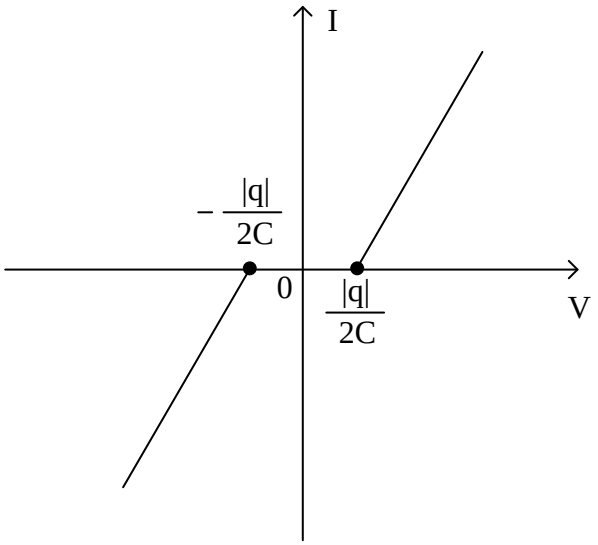


Figure 3.1: I-V curve of nano-scale capacitor due to Coulomb blockade effect.

3.1.2 Electron transport through QD of SET

The QD in SET is a small island with confined electrons and the quantised energy levels. The basic structure and equivalent circuit of SET are shown in Fig.3.2. The tunnelling junctions and QD are assumed to be perfect models. The source and drain are coupled to island through two tunnelling junctions. The barrier can be simplified as one resistor parallel to one capacitor as shown in Fig.3.2 (b). The gate is coupled to the island through capacitor C_G, which modulates the electron occupancy and potential of QD.

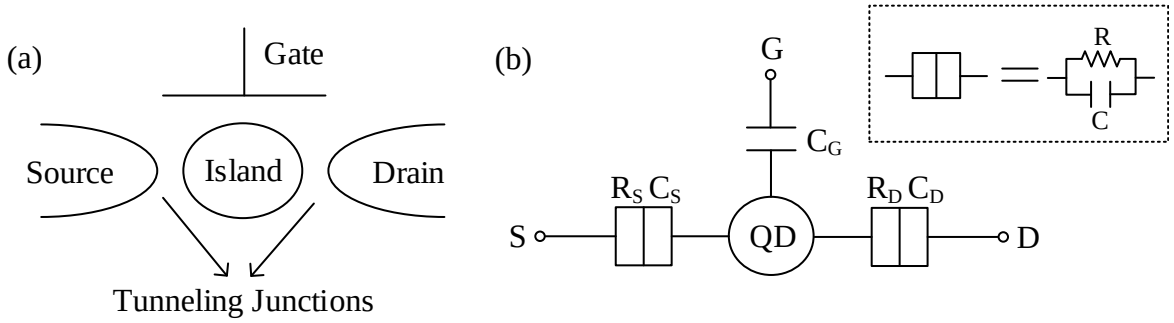


Figure 3.2: (a) Schematic model of SET. (b) Equivalent circuit of SET.

Because there is initial charge (Q_0) inside the QD, there will be repulsion force between QD and the single electron coming toward the QD. The effect of suppressed electron transport is the Coulomb blockade effect explained above. The charging energy of the single electron to tunnel through the tunnelling junction onto the QD is from Eq.3.6

and can be written as [51],

$$E_C = \frac{q^2}{C_\Sigma}$$
$$C_\Sigma = C_S + C_D + C_G. \tag{3.7}$$

C_S, C_D and C_G are parallel viewing from QD. The Coulomb blockade is one of the conditions to observe single electron tunnelling and charge quantisation. Two requirements for Coulomb blockade are listed as following:

1. $E_C \gg k_B T$, the charging energy must overcome the thermal fluctuation at temperature T. Otherwise the thermal fluctuation will suppress most of the single electron effects.

2. R_S, $R_D > \frac{h}{q^2} \approx 25.8K\Omega$. The barrier resistance needs to be larger than the quantum resistance so that electrons could be confined in QD.

Due to the Coulomb blockade effect, the energy induced by V_{DS} needs to overcome the charging energy of each tunnelling junctions for current flow between source and drain without the help of gate. Since the charging energy of each barrier is $|q|/2C_\Sigma$ and there are two tunnelling junctions controlled by the source/drain voltage bias. As a result, the I_{DS}-V_{DS} curve of SET will be look like the Fig.3.3 under different V_{GS}. The threshold voltage (V_{th}) is $|q|/C_\Sigma$ due to two tunnelling barriers. The region between two dots represents the Coulomb blockade region because the V_{DS} could not provide enough energy to overcome the charging energy of tunnelling junctions for electron transport. By changing the V_{GS}, the energy of QD can be modulated for the electron tunnelling through, which removes the Coulomb blockade. Therefore, the solid line in Fig.3.3 will shift to the dotted lines. Therefore, the electron tunnelling can be controlled by using the V_{DS} and V_{GS}.

The gate bias V_{GS} can be used to control the potential of QD and electrons can tunnel through tunnelling junctions on or off the QD. By varying the V_{GS} applied to gate, the electrochemical potential μ_d of QD will be changed. Therefore, the electron occupancy in QD can be adjusted for current flow. The band diagram of SET under low source/drain bias ($V_{DS} < |q|/C_\Sigma$) of electron tunnelling is shown in Fig.3.4. The available states in QD are drawn in solid lines and the empty states are dotted lines. The source and drain are represented with Fermi level E_{FS} and E_{FD} separately. Assuming there are N electrons on QD at fixed V_{GS}. The corresponding electrochemical potential of QD is [51],

$$\mu_{d(N)} = E_N + |q|\varphi_N = E_N + \frac{(n-\frac{1}{2})q^2}{C_\Sigma} - |q|\frac{C_G}{C_\Sigma}V_{GS}. \tag{3.8}$$

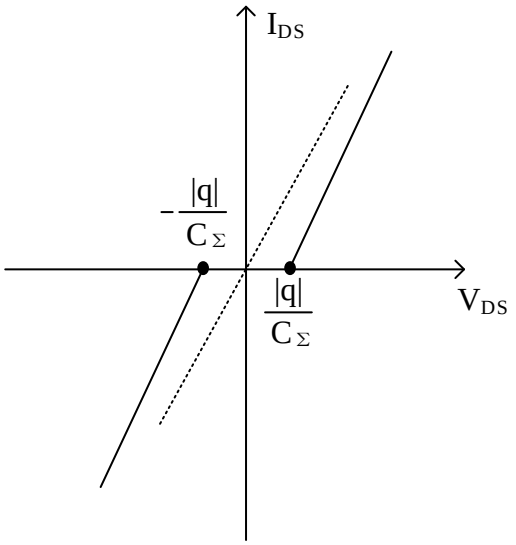


Figure 3.3: I_{DS}-V_{DS} curve of SET under different V_{GS}.

E_N is the discrete energy level of N^{th} electron in QD. φ_N is defined as the electrostatic potential of QD with N electrons measured from the base of source conduction band and the base of QD conduction band. And the term $|q|\varphi_N$ represents the electrostatic charging energy. If the number of electrons in QD increases by 1, the resulting change in electrochemical energy at fixed V_{GS} is [51]

$$E_a = \mu_{d(N+1)} - \mu_{d(N)} = E_{N+1} - E_N + \frac{q^2}{C_\Sigma} = \Delta E + \frac{q^2}{C_\Sigma} \tag{3.9}$$

The addition energy E_a is the energy difference between the lowest empty state and the highest available state in QD and forms the Coulomb blockade region. The adjust energy states are separated by the single-particle energy difference ΔE. And the ΔE is assumed to be constant between two energy levels.

Assuming there are N electrons in QD at V_{G0} as Fig.3.4 (a). There is no available state in QD within the energy window occupied to the source and drain Fermi level, which represents the Coulomb blockade region and no electron can tunnel through the barriers. The Coulomb blockade can be overcame by changing the gate voltage from V_{G0} to V_{G1}, which aligns the available energy state $\mu_{d(N+1)}$ to E_{FS}, as shown in Fig.3.4 (b). Under this situation, a single electron tunnels from source to the available state $\mu_{d(N+1)}$ in QD. Once the electron is added to QD, the number of electrons on QD becomes N+1 and the new QD electrostatic potential ($\varphi_{(N+1,V_{G1})}$) can be calculated based on Eq.3.8 and

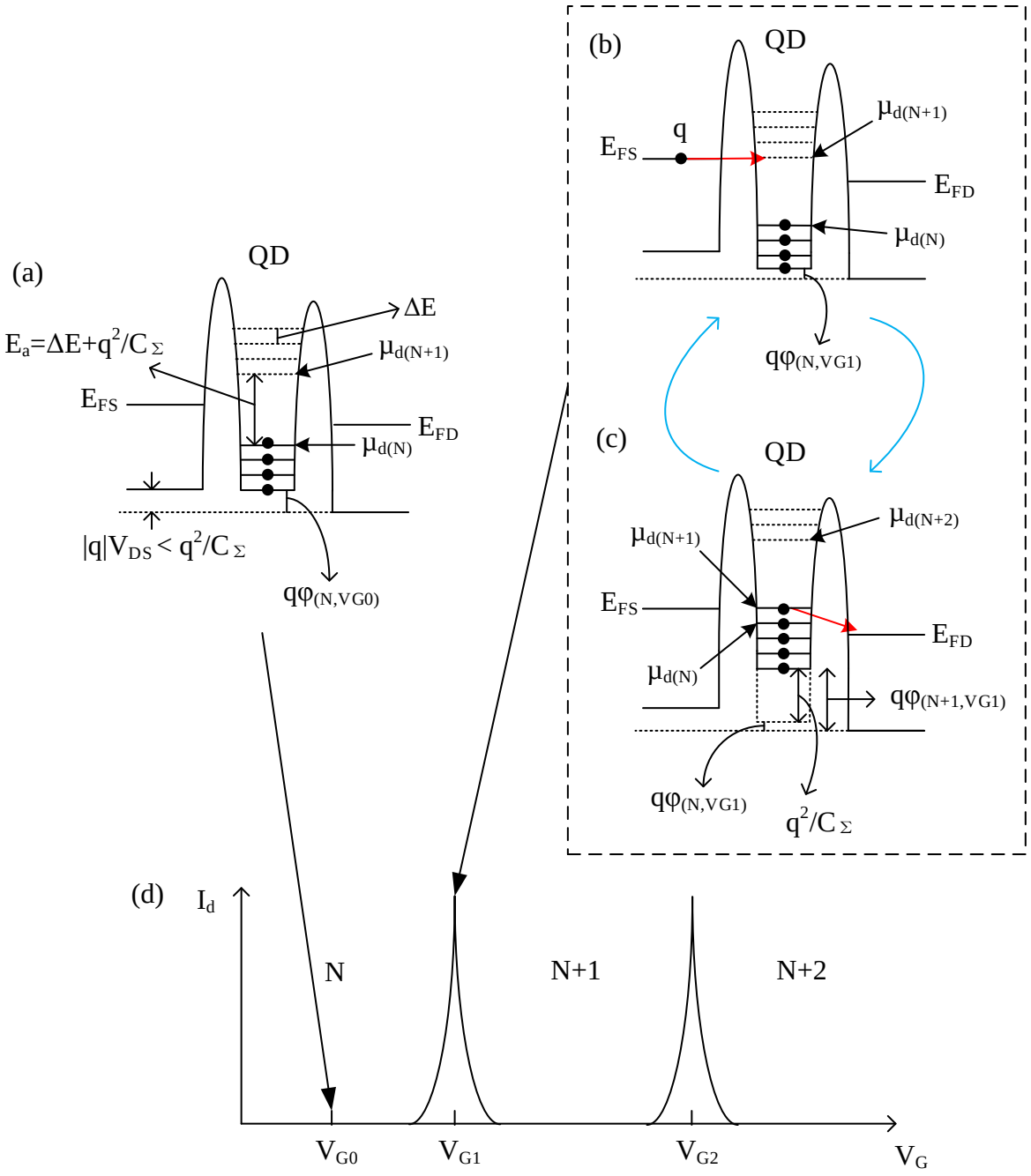


Figure 3.4: (a) The band diagram of SET at V_{G0} and there is no electron can tunnel through due to the Coulomb blockade effect. (b) When gate bias changes to V_{G1}, the energy of QD is lifted, so one electron can occupy to the available state. (c) shows the energy change in QD due to one electron is added. And this electron can tunnel to drain. (d) shows the Coulomb oscillation of I_{DS}-V_{GS} relationship.

Eq.3.9 [51],

$$\begin{aligned}\varphi_{(N+1,V_{G1})} &= \frac{1}{|q|}(\mu_{d(N+1)} - E_{N+1}) \\ &= \frac{1}{|q|}(\mu_{d(N)} + \Delta E + \frac{q^2}{C_\Sigma} - E_{N+1}) \\ &= \frac{1}{|q|}(E_N + |q|\varphi_{(N,V_{G1})} + \Delta E + \frac{q^2}{C_\Sigma} - E_{N+1}) \\ &= \varphi_{(N,V_{G1})} + \frac{|q|}{C_\Sigma}. \end{aligned} \tag{3.10}$$

Therefore, the change in the electrostatic potential will lead the change in the corresponding energy, which is [51],

$$|q|\varphi_{(N+1,V_{G1})} = |q|\varphi_{(N,V_{G1})} + \frac{q^2}{C_\Sigma}. \tag{3.11}$$

The change of the electrostatic charging energy is represented as a change in the QD bottom conduction band in Fig.3.4 (c). At the same time, the energy gap between state $\mu_{d(N+1)}$ and $\mu_{d(N)}$ vanishes because the filled states shift up when one electron added in QD. Since the energy of QD increases by q^2/C_Σ, the Coulomb blockade between QD and drain is overcame. Then the electron can tunnel from QD to drain leading the energy state $\mu_{d(N+1)}$ becomes unoccupied again. The new electron will repeat the previous process and a loop between Fig.3.4 (b) and (c) is formed. By sweeping the V_{GS}, electrons can tunnel on and off the QD one by one, causing the drain current I_{DS} oscillates with V_{GS}. This phenomena is the Coulomb oscillation shown in Fig.3.4 (d). When the single electron tunnels on and off the QD at Coulomb oscillation peaks, the electrochemical potential will remains unchanged at each peak. Therefore, the condition of $\mu_{d(N,V_{G1})} = \mu_{d(N+1,V_{G2})}$ is satisfied. From this condition and Eq.3.8, the Coulomb oscillation period can be calculated as [51],

$$\begin{aligned}\Delta V_{GS} &= \frac{C_\Sigma}{C_G}(\frac{\Delta E}{|q|}) + \frac{|q|}{C_G} \\ &\simeq \frac{|q|}{C_G}(as\ \Delta E \approx 0). \end{aligned} \tag{3.12}$$

Because the energy splitting ΔE is very small by comparing with q^2/C_G, so ΔE could be assumed to be 0.

By combining the I_{DS}-V_{DS} (Fig.3.3) and I_{DS}-V_{GS} (Fig.3.4 (d)), the charge stability diagram can be plotted as Fig.3.5. The diamonds shaded areas represent the Coulomb blockade regions and the diamond is named as Coulomb blockade diamond. The electrons cannot tunnel on or off the QD inside these regions. Because neither V_{GS} nor V_{DS} can provide enough energy to produce an available state in QD aligned the source and

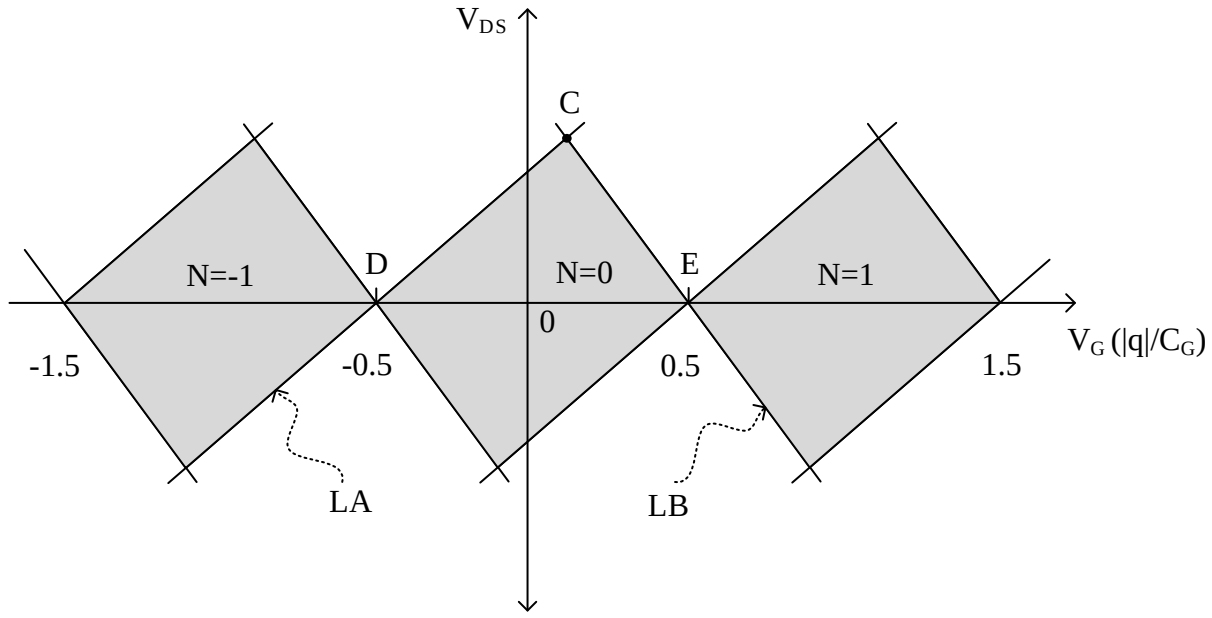


Figure 3.5: The schematic of charge stability diagram as a function of V_{DS} and V_{GS}.

drain. The line LB represents one single electron tunnels from source to QD if [51],

$$\begin{aligned} &\frac{V_{DS}C_D}{C_\Sigma} + \frac{V_{GS}C_G}{C_\Sigma} \geq \frac{|q|}{2C_\Sigma} \\ &\Rightarrow V_{DS} = \frac{|q|}{2C_D} - \frac{V_{GS}C_G}{C_D} (giving\ minimum\ value\ of\ V_{DS}) \\ &\Rightarrow \frac{dV_{DS}}{dV_{GS}} = -\frac{C_G}{C_D}. \end{aligned} \tag{3.13}$$

As for the line LA, it shows the situation when electron tunnels from QD to drain when [51],

$$\begin{aligned} V_{DS} - (\frac{V_{DS}C_D}{C_\Sigma} + \frac{V_{GS}C_G}{C_\Sigma}) &\geq \frac{|q|}{2C_\Sigma} \\ \Rightarrow V_{DS} &= \frac{(|q|/2) + V_{GS}C_G}{C_G + C_S} (giving\ minimum\ value\ of\ V_{DS}) \\ \Rightarrow \frac{dV_{DS}}{dV_{GS}} &= \frac{C_G}{C_G + C_S}. \end{aligned} \tag{3.14}$$

These slopes characteristics of charge stability diagram can be used to calculate the values of C_S, C_D and C_G for real devices. The point C is the intersection point of LA and LB, which has the value of $|q|/C_\Sigma$ (assuming $C_D = C_S$), which is exactly the V_{th} in the I_{DS}-V_{DS} curve. Not only V_{GS} controls the single electron tunnelling, but also the V_{DS}. At point C, the CB can still be suppressed because the sufficient V_{DS} decrease the Fermi level of drain so that the electron is free to move from source to drain through QD. The maximum width between point D and E of the Coulomb blockade diamond is

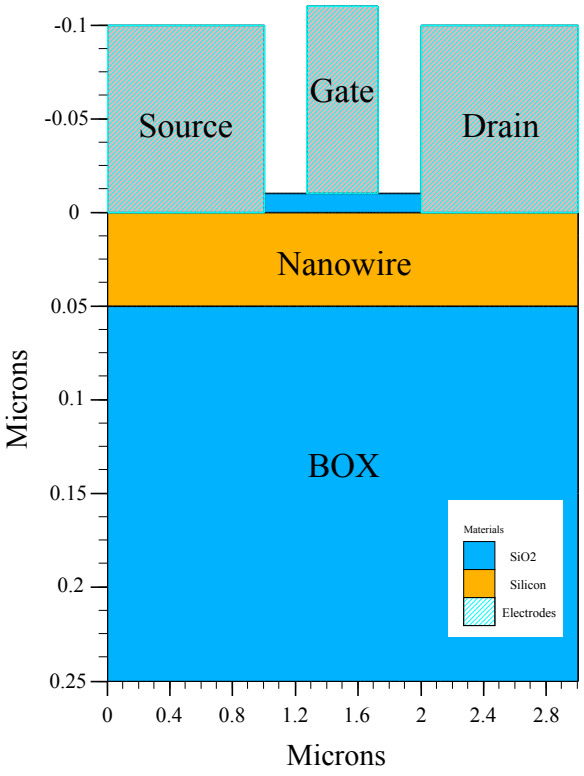


Figure 3.6: The 2D structure of the simulation device with Silvaco.

$|q|/C_G$, which equals to the ΔV_G in Coulomb oscillation. At points D and E, there will be an available state in QD for single electron tunnelling, which describes the electron tunnelling process in Fig.3.4 (b) and (c). And the points like D and E correspond the Coulomb oscillation peaks in Fig.3.4 (d).

3.2 Device simulations of NW-FET

In terms of device structure, our SET device design follows the structure of NW-FET device. The special criteria of the SET is that there is dopants induced QD within channel. The purpose of the simulation is to find the relationship between device performance and central dopants. In order to test the feasibility of our NW-FET device, the 2D device simulation is carried out using the device simulator Silvaco. Due to the limitation of the simulator, the device can only be simulated at the room temperature. Therefore, this preliminary simulation will be used as a design and characteristic guide to the real device room temperature measurements. At the same time, the device with intrinsic and selectively doped channel will be simulated and compared to classical MOSFET equations.

In order to process the device simulations, the 2D device in Fig.3.6 is created using Silvaco's structure builder DEVEDIT. The whole device region is limited within 3 μm

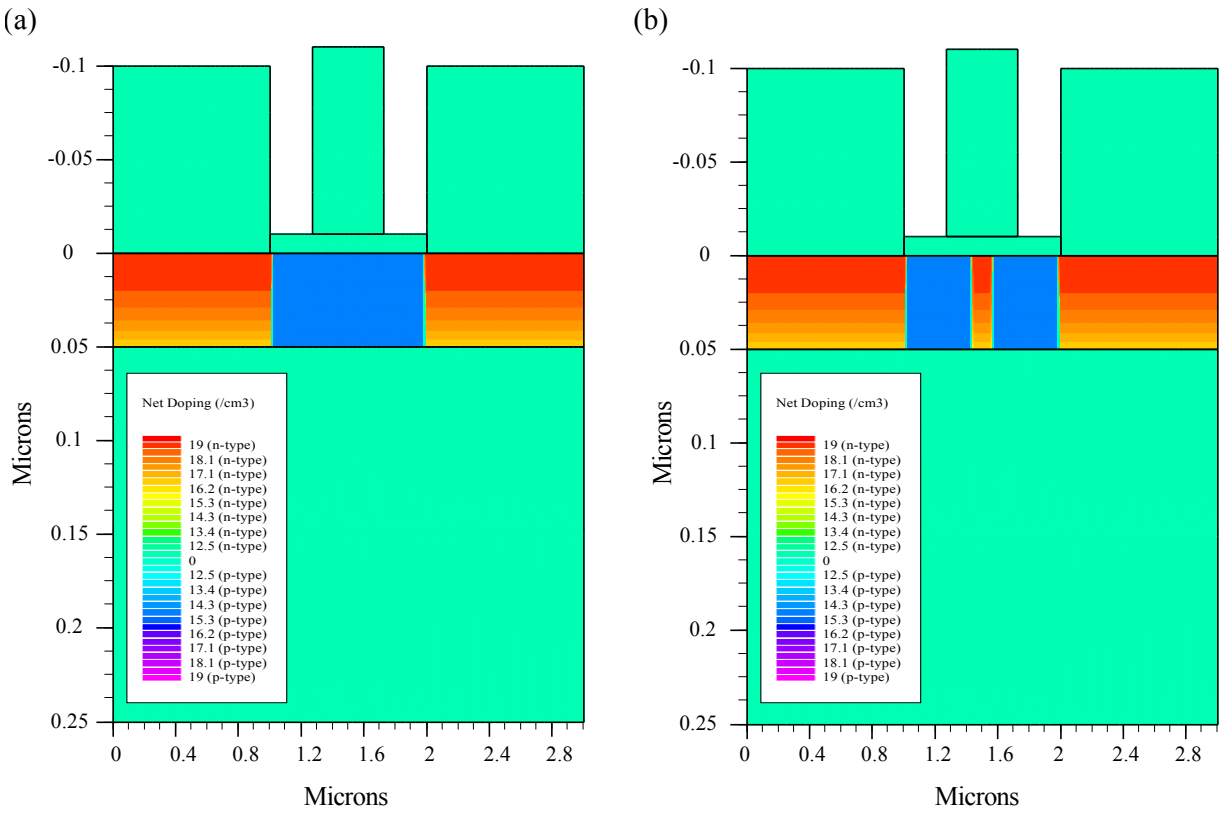


Figure 3.7: (a) shows the structure with intrinsic channel and (b) represents the device with selectively doped channel.

to decrease the simulation time. The structure is designed to be similar to the real device in order to get the more accurate simulation results. The device selected for simulation is the NW-FET with 500 nm length, 100 nm width and 50 nm thickness nanowire. The gate length is 450 nm at the middle of nanowire. The thickness of the gate oxide is set to be 10 nm, which is located between the gate and nanowire in Fig.3.6. According to the SOI used for the device fabrications, the thickness of BOX layer is 200 nm. The silicon substrate is ignored in the simulation for simplification. The thickness of source/drain and gate contacts are set to be 100 nm, which is sufficient for simulation. In order to get more accurate simulation results, the number of mesh layers in each part is designed to be four according to the simulator manual. Two different types of NE-FETs with intrinsic and selectively doped channels are simulated. The base resistivity of the p-type silicon layer of SOI sample is 14 Ωcm from the manufacture data sheet. Therefore, the corresponding base concentration is 1×10^{15} cm^{-3}. The NW-FET is designed as the n-channel device and the source/drain are doped with 1×10^{19} cm^{-3} phosphorus. As for the selectively doped device, the 50 nm-wide selective doping region is located under the gate and the doping concentration is the same as source/drain regions. The intrinsic and selectively doped structures with phosphorus doping are shown Fig.3.7. The whole silicon layer is firstly uniformly doped with p-type impurities. For the phosphorus doped regions, the dopants are distributed based on Gaussian distribution. The position of the

peak concentration appears under the doping region surface.

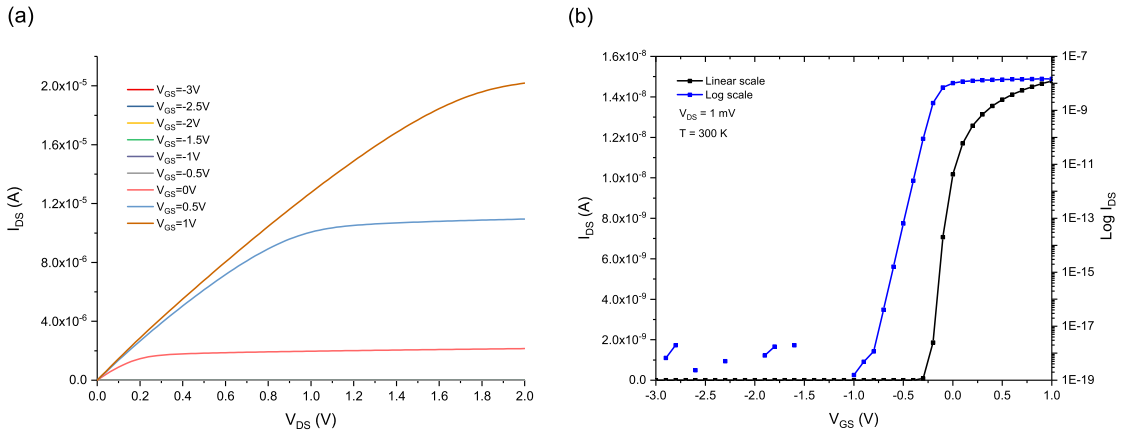


Figure 3.8: I_{DS}-V_{DS} (a) and I_{DS}-V_{GS} (b) simulation characteristics of the intrinsic channel device. The rest of curves when $V_{GS} < 0$ V are close to 0 A and are not obvious in plot (a).

The properties of silicon are modified in the simulation for better accuracy. The values of electron affinity and band gap energy of silicon are defined to be 4.05 eV and 1.12 eV separately. And the work function of contacts is defined to be 4.1 eV. Both I_{DS}-V_{GS} and I_{DS}-V_{DS} curves of two different type NW-FETs are simulated and compared. Fig.3.8 shows the I-V relationships of the device with intrinsic channel. For I_{DS}-V_{DS} measurement, the drain voltage changes from 0 V to 2 V with the step 20 mV and the gate voltage sweeps from -3 V to 1 V with the step 0.5 V. As for the I_{DS}-V_{GS} measurement, the gate sweeps from -3 V to 1 V with the 0.1 V step and the drain voltage is selected to be 1 mV. The logarithmic I_{DS} is plotted against V_{GS} as well.

From the simulation results, the threshold voltage V_{th} is extracted as -0.23 V from the simulator default extraction program. And the sub-threshold slop is extracted to be 63 mV/decade. The MOSFET V_{th} equation is shown in Eq.3.15,

$$\begin{aligned} V_{th} &= V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_{si} q N_A (2\psi_B)}}{C_o} \\ V_{FB} &= \phi_{MS} - \frac{Q_f + Q_m + Q_{ot}}{C_o} \\ &= \phi_M - \phi_S(Q_f, Q_m, Q_{ot} = 0). \end{aligned} \tag{3.15}$$

The term V_{FB} represents the flat-band voltage, which includes the work function difference (ϕ_{MS}) between metal and silicon, the fixed oxide charge (Q_f), mobile ionic charge (Q_m) and interface trapped charge (Q_{ot}). All the values of oxide charges are assumed to be 0 in the simulation. From the threshold voltage equation, the term $2\psi_B$ is the inversion voltage to create the inversion layer within the substrate, which can be calculated

from,

$$2\psi_B = \frac{2KT}{q} ln(\frac{N_A}{n_i}). \tag{3.16}$$

N_A and n_i represent the substrate impurities concentration and the silicon intrinsic carrier concentration separately. The term C_O is the gate oxide capacitance per unit area and C_O=ε_{ox}/d, where d is the gate oxide thickness. Among these terms, the value of ϕ_S depends on the substrate impurity concentration. The p-type silicon energy band diagram in Fig.3.9 can be used to calculate the substrate work function as,

$$\phi_S = \chi + \frac{0.5E_g}{q} + \psi_B. \tag{3.17}$$

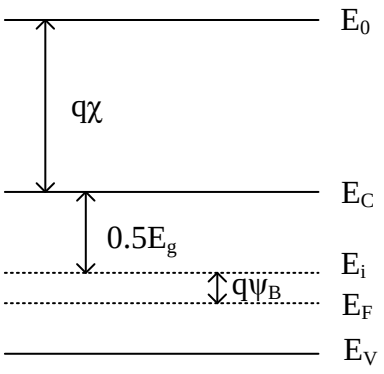


Figure 3.9: The energy band diagram of p-type silicon. χ is the electron affinity in silicon and E_g is the silicon band-gap energy. The line E_0 represents the vacuum energy level.

Based on the previous equations and the values of different parameters in equations, the Table.3.1 can be created and the value of threshold voltage could be calculated.

Table 3.1: The values of parameters for the threshold voltage analytical calculation.

Parameter	Value
ϕ_M	4.1 V
χ	4.05 V
E_g	1.12 eV
KT/q	0.026 V
q	1.6×10^{-19} C
N_A	1×10^{15} cm^{-3}
n_i	9.65×10^{9} cm^{-3}
ε_{si}	1.03×10^{-12} F/cm
ε_o	3.45×10^{-13} F/cm
ϕ_S	4.91 V
V_{th}	-0.2 V

The relative permittivity of silicon and SiO_2 are set to be 11.9 and 3.9 respectively. The threshold voltage V_{th} is calculated to be -0.2 V, which is very close to the value from the simulation. The threshold voltage from the simulation and analytical calculation is consistent. As for the output current I_{DS} within the saturation region, the value can be calculate from the V_{th} value and the following equation,

$$I_{Dsat} = (\frac{Z\mu_n C_o}{2L}) \times (V_{GS} - V_{th})^2$$
$$\mu_n = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (\frac{N_D}{N_r})^{\alpha}}. \tag{3.18}$$

The parameter Z and L are the device width and channel length. In the 2D simulation, the device width cannot be defined and the default value is 1 μm. The channel length has the same value as the gate length, which equals to 450 nm. The electron mobility will be effected by the n-type doping concentration and the relationship of the real mobility and doping concentration is shown in Eq.3.18. To calculate the saturation drain current, the V_{GS} is selected to be 0.5 V and the Table.3.2 can be created.

Table 3.2: The values of parameters for the saturation drain current calculation.

Parameter	Value
Z	1 μm
L	450 nm
C_O	3.45×10^{-7} F/cm^2
N_D	1×10^{19} cm^{-3}
N_r	9.2×10^{16} cm^{-3}
α	0.711
μ_{min}	68.5 cm^2/V-s
μ_{max}	1414 cm^2/V-s
V_{GS}	0.5 V
V_{th}	-0.2 V
I_{Dsat}	2×10^{-5} A

By comparing the calculation result and the simulation result in Fig.3.8, the calculated I_{Dsat} is higher than the simulation value 1.1×10^{-5} A. The reason is that the whole silicon region between source and drain in Fig.3.6 is regarded as the nanowire channel in the simulation. The length of channel becomes 850 nm instead of 450 nm. By substituting L=850 nm in the Eq.3.18, the new I_{dsat} is calculated to be 1.04×10^{-5} A, which is similar to the simulation result.

In order to compare the electrical characteristics of NW-FET with intrinsic channel and selectively doped channel. The I-V simulation of the device with 50 nm width doping windows under gate is carried out and the simulation results are shown in fig.3.10.

For the I_{DS}-V_{GS} curve, the gate voltage changes from -3 V to 2 V with the step 0.1 V when V_{DS} is set to 1 mV. As for the I_{DS}-V_{DS} curve, the drain bias sweeps from 0 V to 2 V with the step 20 mV and V_{GS} is from -3 V to 1V with 50 mV step. From the

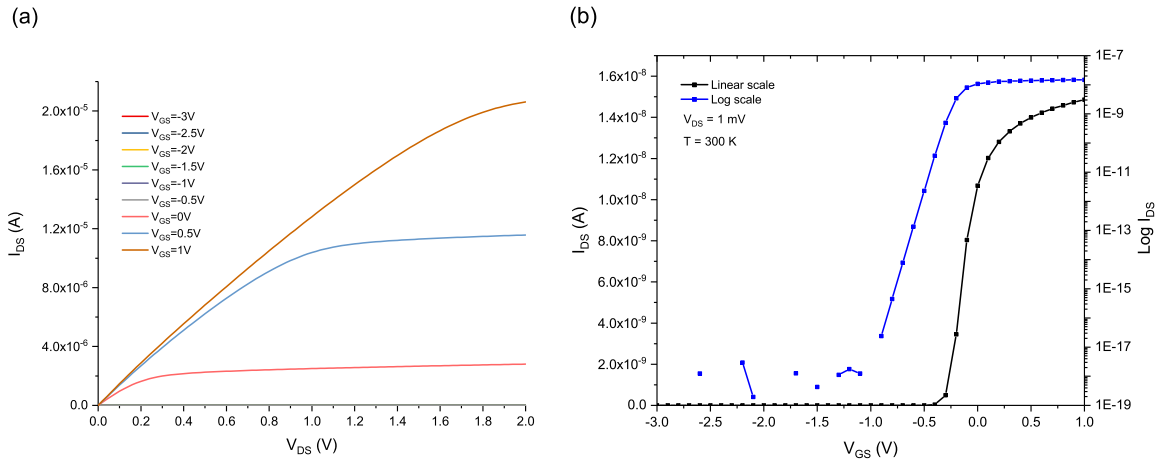


Figure 3.10: I_{DS}-V_{DS} (a) and I_{DS}-V_{GS} (b) simulation characteristics of the selectively doped channel device. The rest of curves when $V_{GS} < 0$ V are close to 0 A and are not obvious in plot (a).

simulation extraction, the threshold voltage V_{th} is -0.28 V and the sub-threshold slope is 70 mV/decade. The V_{th} is smaller than that of NW-FET with intrinsic channel. Due to the specific doping region under top gate, less voltage is need to create the inversion channel for electron transport. Therefore, the dopants in channel have the effect to shift the threshold voltage to the negative direction [52]. Based on the saturation drain current equation Eq.3.18, the more negative V_{th} will let the I_{Dsat} becomes larger as well. And from I_{DS}-V_{DS} simulation result in Fig.3.10 (a), the I_{Dsat} when V_{GS}=0.5 V and V_{DS}=2 V is around 1.2 $\times$ 10^{-5} A, which is larger than the I_{Dsat} shown in Fig.3.8 (a).

From the Silvaco 2D device simulations, two different type NW-FETs are simulated and the I-V characteristics are compared. Both devices show the classical MOSFET characteristics. Based on the simulation results, both devices show the negative value threshold voltage. And the channel doping has the effect to make the threshold to become more negative. This effect will be used as a reference for the real devices to detect the channel dopants. At the same time, the channel dopants have the effects to increase the output current. The simulation results are compared with the equation calculation results, which proves the simulation models are reliable. These simulation results will be used for curve fitting with the measurement results in the later chapter for the better device understanding and analysis.

Chapter 4

Fabrication of First Batch Few Dopants NW-FET Transistors

This chapter describes the fabrication and process development of few dopants NW-FET inspired from the previous literature reviews and device simulations. The aim of the project is to fabricate and analyse the characteristics of few dopants silicon transistor at room and low temperature. The advantages and disadvantages of various devices based on device structures, fabrication methods and measurement results are reviewed in the literature chapter 2. Based on these reviews and the project aim, there are some important criteria listed below need to be met during the design and fabrications:

1. The transistor can demonstrate that few dopants could be achieved by selective diffusion method with silicon dioxide doping mask.
2. Devices with different doping profiles need to be fabricated parallel for comparisons.
3. Different dimensional devices are needed to be included in the design for comparisons.
4. Both fabrication process and device characteristics are reproducible.
5. The fabrication cycle including Ebeam lithography and doping process needs to be controlled within a suitable range.

Base on the above requirements, the NW-FETs are proposed with the help of Ebeam lithography (EBL). There are five Ebeam layers in total start from the alignment marks layer. Both global and chip marks are used to get a better alignment from layer to layer. In order to achieve the selective doping area within the sample, the PECVD SiO_2 is used as the doping mask during the spin-on dopants and dopants annealing process.

Meanwhile, the size of doping area changes from device to device. In order to compare the electric characteristics of NW-FETs with different doping situations, devices with intrinsic and fully doped channel will also be included in the design. Besides different doping conditions, various dimensional nanowires are going to be applied for comparison. The silicon nanowires will be fabricated with the help of EBL resist HSQ and plasma dry etching followed by the gate oxidation. The lift-off Al source/drain and gate contact will be deposited finally, followed by the contacts annealing process to form the ohmic contact and active dopants. The following sections will explain the details of the device design and fabrication processes. At the same time, the advantages and disadvantages of each fabrication step will be analysed.

4.1 EBL layer mask design

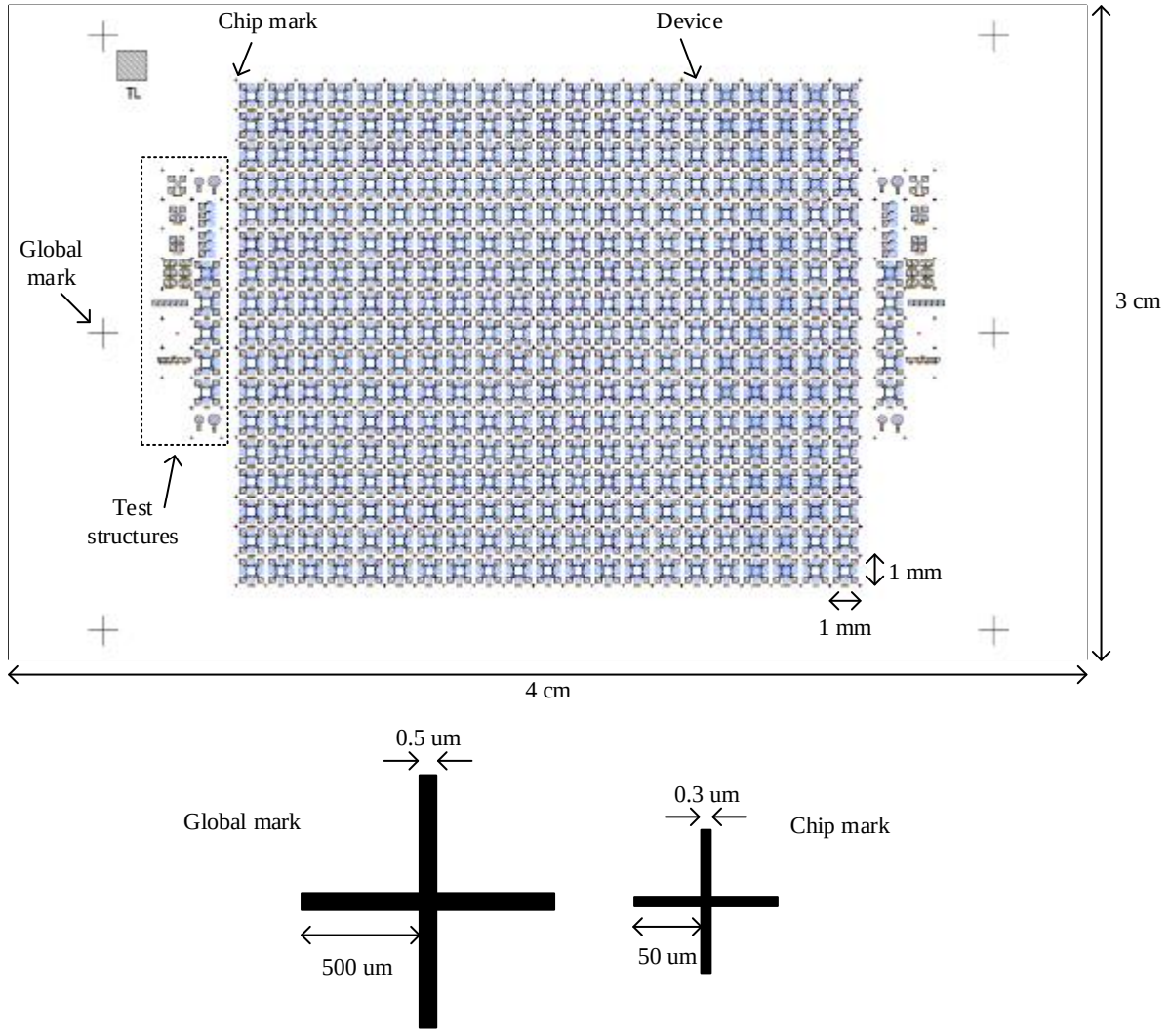


Figure 4.1: 4 cm × 3 cm EBL chip mask layout with the labels of different on-chip design. Both global and chip marks are shown as well.

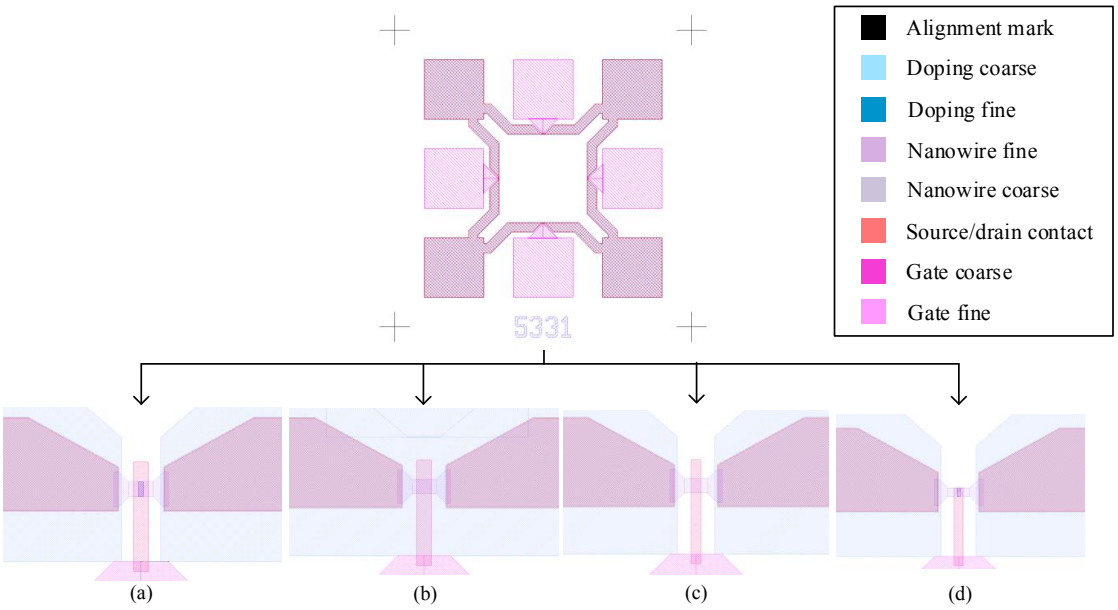


Figure 4.2: The example is one of the device blocks containing four identical NW-FETs. The number "5531" is the dimension of nanowire: L(500 nm) × W(300 nm) nanowire with 300 nm gate and 100 nm × 300 nm doping region at the centre of nanowire. The following sub-figures (a)-(c) are selective doping, fully doped and intrinsic NW-FETs. (d) is a special type of NW-FET, whose nanowire has a notch at the centre.

In order to reduce the fabrication cycle and improve the fabrication efficiency, the devices will be fabricated based on the 4 cm × 3 cm chip scale SOI substrate. The full chip layout is shown in Fig.4.1. All Ebeam lithography layers are included in the figure with two types Ebeam alignment marks and test structures. Six global marks inside the chip are used for the coarse alignment at the beginning of each Ebeam lithography. In order to minimise the misalign of different layers, four smaller chip marks are also used around each device for the fine alignment. By applying the global and chip marks, the misalignment can be controlled within 20-100 nm. The actual misalignment is much less than 100 nm mostly. Therefore, a 100 nm misalign between different layers is considered when design the mask. Although the chip size is 4 cm × 3 cm, the size of the real devices area without test structures is only 21 mm × 17 mm. The reason is that the edges of the chip are likely to be contaminated during the fabrication process by tools and tweezers. At the same time, the variation of surface conditions is large along the edges and it is not suitable for devices fabrication. The size of device block is set to be 1 mm × 1 mm square due to the limitations of Ebeam machine JEOL JBX-9300FS. Based on the Ebeam machine manual [53], the maximum beam scan area is 1 mm × 1 mm. If the patterns are larger than this filed size, it will be stitched by exposing the 1 mm × 1 mm filed and then moving by 1 mm to write the next field. The movement between fields during exposure can cause the misalign along the patterns. Therefore, the real NW-FET

is put inside a 1 mm × 1 mm block area to avoid the field stitch misalignment. Based on the above chip and device block size information, 357 device blocks can be managed into the chip. These 357 blocks contain all the combinations of different doping and dimensions for nanowire. Each device block is repeated twice along the whole chip. In this way, not only all the combinations of device variations are included, but also the possibility of valid working devices is increased. The design layout of NW-FET is shown in Fig.4.2. The wide range of nanowire and gate dimensions are selected to perform the detailed comparisons. The matrix of applied dimensions are shown in Table.4.1.

Table 4.1: Details of the device dimension combinations are represented. The length and width of the nanowire are shown with the length of top gate. The dimension of real device is picked by grouping values from length of nanowire, width of nanowire and gate length using permutation and combination method.

Length of nanowire (nm)	Width of nanowire (nm)	Gate length (nm)
50	50	50
100	100	100
150	150	200
200	200	300
300	250	
400	300	
500		

In this work, there are two types of nanowires in the design. The first type is the original nanowire with the single top gate covered. The another type nanowire has a notch at the middle of nanowire to provide extra potential confinement. All five EBL layers are shown in Fig.4.2. Except the alignment and source/drain contact layers, all other layers need both the coarse and fine beam during exposure. The coarse beam is used to write larger patterns and the writing time can be reduced. For the device critical parts, the fine beam must be used to get the most accurate dimensions as design. Regarding the sub-figures (a)-(d) of Fig.4.2, the coarse doping region is larger than the coarse silicon nanowire to make sure the coarse silicon patterns are properly doped. As for the selectively doped NW-FET (a), the gate width is larger than the fine doping area at the centre nanowire so that the centre doping region can be fully controlled by single top gate. The width of overlap region between coarse and fine nanowire layer is 100 nm due to the 100 nm misalign between two layers discussed above. The taper-style fine nanowire is deigned deliberately to reduce the thermal oxidation stress at the corners. The thermal oxidation stress at the shaped 90° silicon nanowire corner can be accumulated due to the oxidation volume is larger than the volume of replaced silicon [54]. The built-up stress at concave and convex corners decreases the oxidation rate and the resulting oxidation at corners is shown in Fig.4.3.

As a result, the width of nanowire is reduced at two ends, which shrinks the current flow path. However, the thermal oxidation stress can be significantly reduced by using obtuse angle instead of right angle at convex and concave corners. From Fig.4.2, the

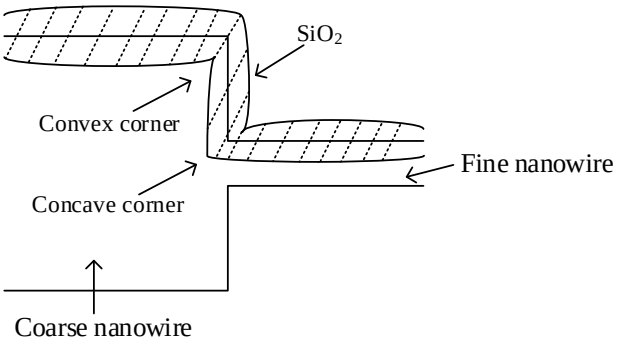


Figure 4.3: The thermal oxidation at 90° convex and concave corners along the nanowire.

source/drain contact is slightly smaller than the coarse nanowire. At the same time, the edge of the contact is designed to be close to the fine nanowire as close as possible to reduce the resistance. In order to get a good control of channel with top gate, the top gate is designed to fully cover the nanowire perpendicularly. This can help to keep the metal top gate to be continues during the lift-off process.

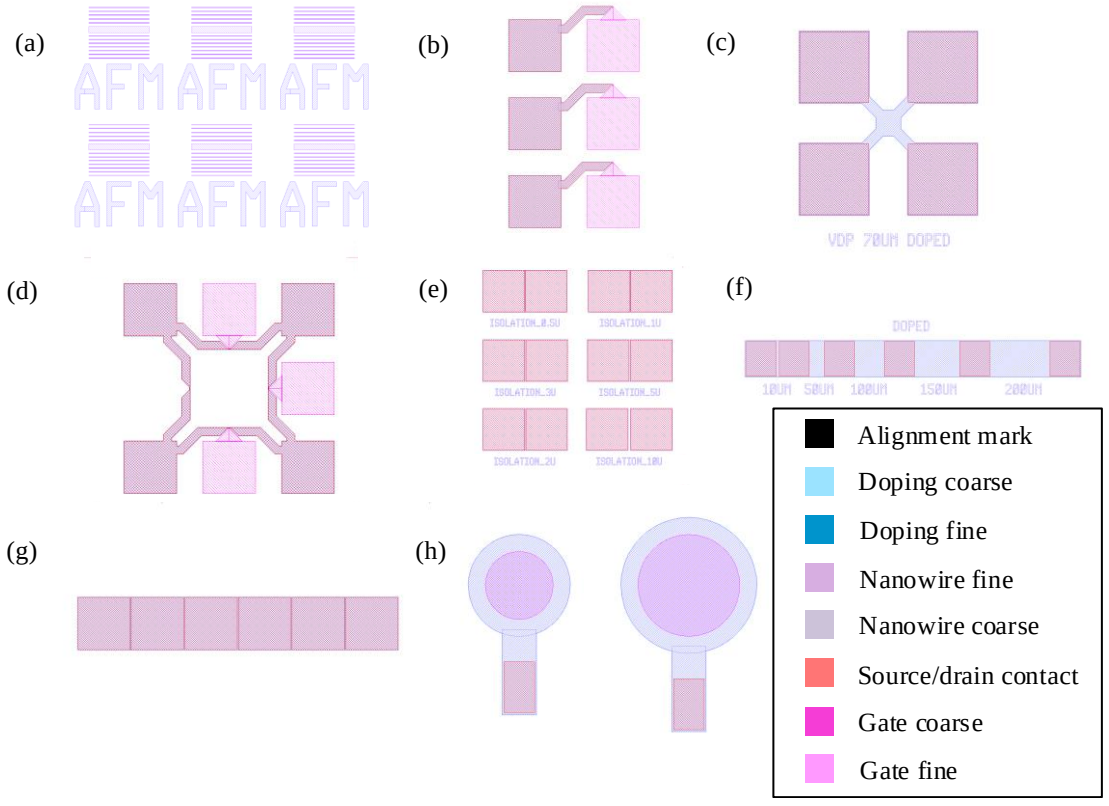


Figure 4.4: Different test structures are included in the chip design to characterise the device and fabrication results.

Apart from the devices, there are two areas on the chip containing different types test structures. The electrical properties of the devices after fabrication such as the doping

Table 4.2: Briefly introduction and function of each type test structure.

Test structure type	Function of the test structure
(a)	The group of nanowires has different width and the gap of each nanowire is various in the group. It is used for the AFM measurement to check whether the nanowires are properly isolated or not after etching.
(b)	The structure is like the standard NW-FET without drain contact. It is used for capacitance measurement, gate leakages current test and the gate oxide breakdown voltage could also be extracted.
(c)	This Van der Pauw structure is used for the 4-point measurement to extract the doping concentration of the doping areas.
(d)	It is like the normal NW-FET introduced above but with three top gates only. This structure is used for the SEM inspection after each process. On the other hand, the KPFM scan can be applied to the left-side device that has no top gate to get the information of the doping situation along the channel.
(e)	These isolation pads is used to measure the current leakage through BOX.
(f)	The doped TLM structure is used to measure the contact and sheet resistance. By measuring the IV curve between two adjacent contact pads with different gaps, the relationship of calculated resistance and gap can be combined as a curve. As a result, the contact and sheet resistance can be extracted from the curve.
(g)	Different dimensional nanowires between contact pads are used to check whether the nanowires exist or not after the whole process.
(h)	Two different size capacitance pads are used for the gate oxide capacitance measurement.

concentration, contact resistance and sheet resistance can be measured through these test structures. All different types test structures are shown in Fig.4.4. Each test structure is used for different measurement and the corresponding fabrication characteristic can be detected. The function of each test structure is introduced in Table.4.2 based on Fig.4.4. These test structures are fabricated in parallel with the real devices during the process.

4.2 Sample preparation and SOI thickness reduction

The original sample used for this project is the 6 inch p-type SOI with (100) orientation. The top silicon layer is 100 nm and the thickness of SiO_2 BOX is 200 nm. As explained above, the 4 cm $\times$ 3 cm SOI chip will be used for the EBL NW-FET fabrication. So the 6 inch SOI is cleaved into 4 cm $\times$ 3 cm chips by diamond pen. In order to meet the design targets, the top silicon layer needs to be thinned down to 60 nm. However, during the cleave process, the sample surface will be contaminated by silicon dusts. Thus, it is necessary to run the sample clean process to clean the chip surface. The sample is first put into the FNA for 10 minutes, which can remove any organic on the surface. After

water clean in wired water tank and dry with nitrogen gun, the sample is placed in $45°C$ heated RCA1 and RCA2 beaker for 10 minutes separately. Two steps of water clean are applied during this process. Both RCA1 and RCA2 have the ability to remove the surface particles. However, a thin SiO_2 layer will be formed after RCA clean. Therefore, the sample is dipped into 20:1 BHF at last to remove any oxide left on the surface. There are various methods can be used to make the top silicon layer thinner. In order to keep the good quality of the silicon layer after thinning process. The thermal oxidation method is chosen as it is a contamination free process and the oxidation rate can be controlled precisely. For the thermal oxidation, both wet and dry thermal oxidation can be used and the reaction functions during the oxidation are shown below:

$$Wet\ oxidation\ \ :Si + 2H_2O(vapor) \rightarrow SiO_2 + 2H_2(gas) \tag{4.1}$$

$$Dry\ oxidation\ \ :Si + O_2(gas) \rightarrow SiO_2 \tag{4.2}$$

By comparing the wet and dry oxidation process, the wet oxidation has higher oxidation rate but the quality of SiO_2 is lower due to the remained element H in oxide. The higher oxidation rate will reduce the controllability of the thinner oxidation thickness. Since the thickness of silicon layer needs to be controlled accurately. Therefore, the dry thermal oxidation is used to thin down the SOI. Based on the default dry oxidation recipes stored on the furnace, the temperature of oxidation can be 800°C, 850°C, 900°C, 950°C and 1000°C. In order to reduce the oxidation time, the temperature 1000°C is selected. The relation between thermal oxide thickness (T_{ox}) and consumed silicon thickness (T_{Si}) is

$$T_{Si} = 0.46 \times T_{ox} \tag{4.3}$$

In order to get 60 nm silicon from 100 nm, 40 nm silicon needs to be consumed. By applying the above equation, the result SiO_2 thickness should be 87 nm. By checking the thermal oxidation curve table and several test run with SOI cut and silicon test chip, the relationship between SiO_2 and oxidation time is plotted in Fig.4.5. As a result, 1 hour 47 minutes dry oxidation process in furnace can provide the oxide with desired thickness. Fig.4.6 shows the map of oxidation layer and silicon layer thickness on SOI after dry thermal oxidation measured by ellipsometer.

From the layer thickness map, the thickness of SiO_2 is non-uniform along the chip. The reason is that the oxidation rate at centre and edges are different. In the main area, the roughness is much smaller to be around 3-5 nm. The formed oxide needs to be removed afterwords. There are various methods can be used to remove the oxide. In order to protect the silicon layer underneath the oxide, the wet etch is used. For the wet etch, both 7:1 and 20:1 BHF can be used. In general, silicon cannot be etched in the HF, but if the sample is left in HF for long time or the HF solution has higher acid concentration then there is still a chance to etch silicon. As a result, the 20:1 BHF is used to remove the oxide layer. Through various etching rate test, the thermally oxidised SiO_2 etching

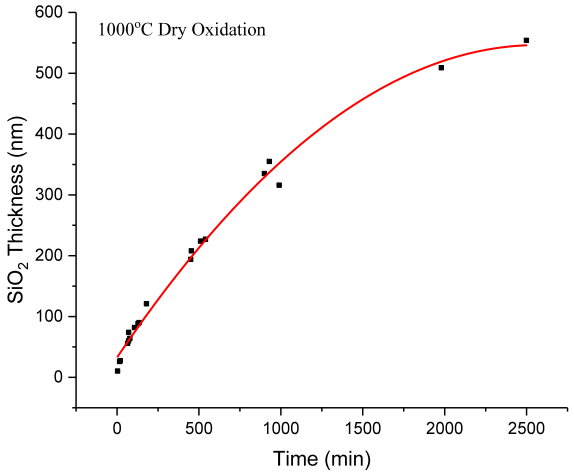


Figure 4.5: Measured SiO_2 thickness against dry oxidation time.

rate in 20:1 BHF is around 30 nm per minute. Based on this etching rate and the oxide thickness, the chip is put into BHF for 3 minutes 30 seconds to remove all 81 nm oxide with a little bit over etch. The purpose of over etch is to make sure there is no oxide left on the SOI surface.

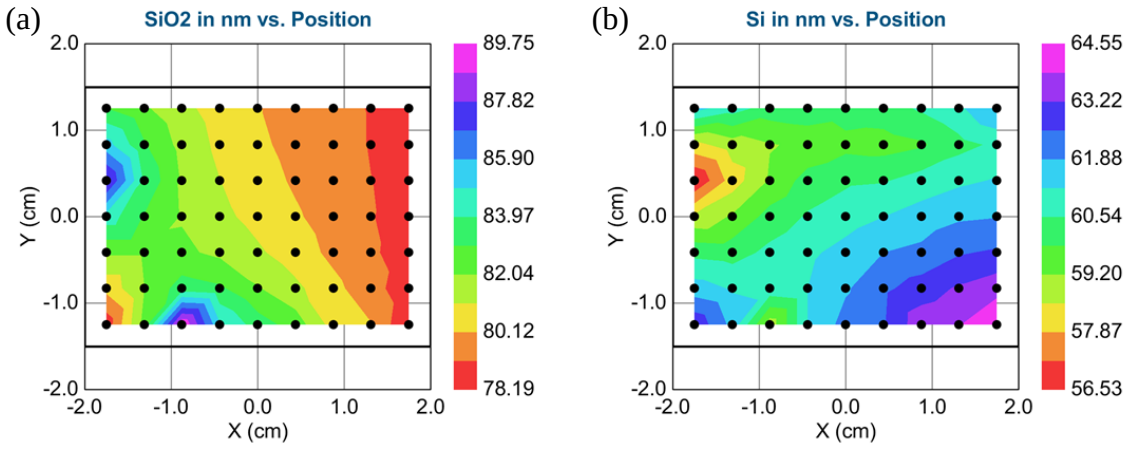


Figure 4.6: (a) Ellipsometry measurement of the dry thermal oxidation SiO_2 with average thickness 81 nm. (b) The silicon average thickness of SOI is 61 nm. For (a) and (b), MSE=19.6 and the SOI measurement model is used with fixed BOX thickness 200 nm. The unit of the contour is nm.

4.3 EBL alignment marks formation

After the sample preparation process, the SOI chip is ready for the first EBL layer. From Fig.4.1, the purpose for using small dimensional chip marks is to achieve the best alignment during exposure. Because the alignment marks need to be etched down

after exposure, positive Ebeam resist is used for alignment marks writing. Due to the high resolution of the chip marks and the alignment mark dry etch process after EBL, the positive resist ZEP520A is selected. The deeper alignment marks are, the better the alignment will be. So the thickness of ZEP needs to be as high as possible with the proper surface roughness and quality. Based on the ZEP data sheet and various spinning test, the ZEP is spun at 3370 rpm for 180 seconds with open lid and then the sample is baked at 180°C for 3 minutes to harden the layer. The result thickness of ZEP is 411 nm. The reason to open the spinner's lid is that the air pressure on sample surface reduces during spinning and the thickness of ZEP will be increased. The principle of the EBL is that the accelerated electron beam is applied to the resist then the energy of the beam can break the chemical bonds of the resist. After the development process, the exposed area of positive resist is cleaned away. In order to get the correct energy to break the chemical bonds and the desired design dimensions, the base dose of the electron beam for ZEP is chosen to be 250 μC/cm^{-2}. Higher or lower dose will cause the size of structure to be larger or smaller. One problem of the EBL is that the backscattered electrons during exposure can expose more areas. To reduce the backscattering effect, the proximity error correction (PEC) is applied during EBL files generation. The function of PEC is that the structure patterns will be divided into smaller blocks firstly, then the dose level adjustment will be applied to these blocks based on Gaussian approximation and the electron backscattering effect. The base dose is used as the dose reference for dose level adjustment. As a result, the corners and edges of the pattern will have higher dose than the large middle area. After exposure, the developer ZEDN50 is used for 2 minutes followed by 2 minutes IPA rinse. The SEM pictures of alignment marks after development are shown in Fig.4.7. After the alignment marks are developed, the etch process can be carried out to form the real alignment marks.

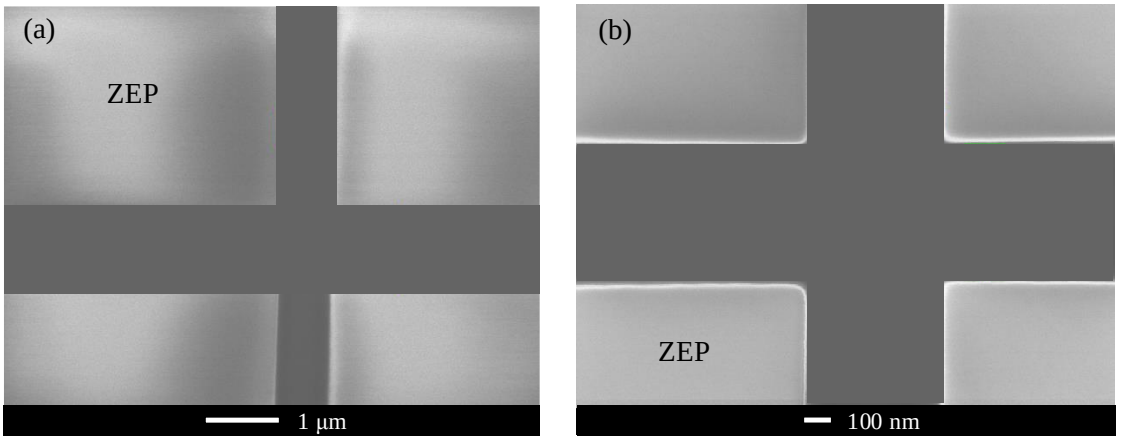


Figure 4.7: The SEM pictures of global and chip alignment marks after development are shown in (a) and (b) separately. The actual line width of global and chip marks are 0.53 μm and 305 nm. By comparing with the design dimensions in Fig.4.1, the actual dimensions are very close to the desired values.

Table 4.3: Silicon and SiO_2 RIE etch recipes for alignment marks. The chemical etching is mainly used for silicon etching process. Both chemical and physical etching are included in the SiO_2 etching process. The values of all parameters are obtained from several tests.

Parameters	Si RIE etch recipe	SiO_2 RIE etch recipe
O_2 gas flow rate (sccm)	13.5	0
SF_6 gas flow rate (sccm)	18	0
CHF_3 gas flow rate (sccm)	0	12
Ar (sccm)	0	38
Set pressure (mTorr)	30	30
Strike pressure (mTorr)	0	50
RF power (W)	160	200
Table temperature (°C)	20	20
Table type	quartz	quartz
Etch rate	$\sim$ 3 nm/s	$\sim$ 17 nm/min
Selectivity to ZEP	4:3	7:3

In order to get the deeper alignment marks with vertical side walls, the RIE plasma dry etch is used. In order to form the deep alignment marks, three layers need to be etched in sequence. Thus, the alignment marks can be etched down into the SOI substrate. However, the resist ZEP can be etched at the same time during the etch process. Therefore, the etch selectivity of silicon/ZEP and SiO_2/ZEP need to be as higher as possible. In order to measure the etch rate of silicon, SiO_2 and ZEP during the process, the SOI cut, silicon chip with thermally oxide and silicon chip with ZEP are used as test samples. At the same time, the big square located at the top-left corner in Fig.4.1 is used to monitor the etching depth during the SOI etch process. The RIE etch recipes of silicon and SiO_2 are shown in Table.4.3.

The silicon etch is a chemical etch process. During the process, the gas SF_6 has the electron impact dissociation reaction to release the atom F. The element F in SF_6 can react with silicon to form the volatile SiF_4 gas. However, the radicals fluorosulfur will remain on the silicon and they can react with atom F to reform the SF_6. As a result, the silicon surface is prevented to have reactions with F. The gas O_2 is added to solve this problem. The added oxygen can react with radicals fluorosulfur and increase the net concentration of F, which leads the increase of silicon etch rate [55]. As for the SiO_2 etch process, it contains the chemical and physical etch at the same time. The gas CHF_3 is used for chemical etch like the SF_6 used in silicon etch. Gas Ar is used for the physical etch. The ion Ar can bombard the SiO_2 surface to increase etch rate. However, the polymer fluorocarbon builds up on both horizontal and vertical sides during the process. Another purpose of adding gas Ar is to remove the polymer layer through Ar ion bombardment with polymer. The polymer on vertical side of the trench is less likely to be removed by Ar. Thus, the gas Ar is also good for the anisotropic etch. After the alignment mark RIE etch, the chip is put into asher to clean the remaining ZEP. By measuring with the profiler, the etched depth of the alignment marks is around 580 nm.

Table 4.4: SiO_2 PECVD recipes used for doping mask. The values of all parameters are obtained from several tests. The deposition rate is measured with the help of ellipsometer.

Parameters	SiO_2 PECVD recipe
SiH_4 gas flow rate (sccm)	4.2
N_2 gas flow rate (sccm)	80
N_2O gas flow rate (sccm)	350
Set pressure (mTorr)	1000
RF power (W)	20
LF power (W)	0
Table temperature (^oC)	350
Number of steps	3
Step time (second)	100
Deposition rate (nm/s)	$\sim$ 1.1

4.4 Doping regions definition and spin-on dopants

After the formation of the alignment marks, the next step is to define the doping regions and apply the doping process. The surface pre-clean process is done with the standard FNA, RCA and BHF clean to remove any containments after dry etch process. There are two mainly doping processes for the source and drain can be used: ion implantation and spin-on dopants. Due to the limited access to ion implantation facility, the spin-on dopants approach is used to fabricate the prototypes. The spin-on dopants can also reduce the fabrication cycle time. The target concentration is set to be in the 10^{20} cm^{-3} level, which can provide enough current during the low temperature measurement. The spin-on dopants (SOD) solution P507 from Filmtronics is chosen as the phosphorus concentration contained in the solution is about 5 $\times$ 10^{20} cm^{-3} [56]. Based on the design criteria, different doping situations need to be applied, especially the selectively doped NW-FET. Therefore, the doping mask is needed to prevent the dopants going to undesired doping regions. In this process, the 100 nm PECVD SiO_2 is used as the doping mask. The diffusion of phosphorus into SiO_2 is much slower than in silicon because the diffusion coefficient of phosphorus in SiO_2 is usually three to five order smaller than that in silicon [57]. The PECVD SiO_2 deposition recipe is shown in Table.4.4.

The resulting thickness of the PECVD oxide is around 110-115 nm measuring by ellipsometer. In order to define the doping windows on PECVD oxide, the EBL positive resist PMMA950K A7 is used. The resolution of this resit can reach around 50 nm by using the optimised dose. Since the smallest doping windows in the design is 50 nm $\times$ 50 nm, the PMMA950K A7 is used to achieve the desired size. Another reason for using PMMA950K A7 is the same resist will be used for the top gate fabrication. So the same process can be used later to save the fabrication time.

Based on the device design, both coarse and fine beam will be used. The fine beam is used to define the doping windows at the centre of nanowire. The coarse beam is

used form the rest of patterns. Based on the resist data sheet [58], the PMMA is spun at 6000 rpm for 60 seconds. The 90 seconds baking at 180°C is followed directly after spinning, which can produce a 430 nm uniform layer. The SOI cut is used for dose test to establish the proper dose. The same patterns as real sample are also used on test chip, which makes the test results to be more accurate. In order to get the coarse and fine dose information at the same time, the test chip contains a 9 × 9 patterns matrix. The fine dose changes from 1400 $\mu C/cm^{-2}$ to 3000 $\mu C/cm^{-2}$ with the step 200 $\mu C/cm^{-2}$ along column 1 to column 9, which means the patterns from the same column will have the same fine dose for their fine patterns. For the coarse dose, it changes from 1300 $\mu C/cm^{-2}$ to 2900 $\mu C/cm^{-2}$ with the step 200 $\mu C/cm^{-2}$ along row 1 to row 9. In this way, different combinations of coarse and fine dose can be tested at the same time. The electron beam current is 1 nA for the fine beam and the beam aperture is 60 μm. By comparing with the 25 nA and 200 μm used for coarse beam, the fine beam current and aperture are much smaller and it can help to achieve the best resolution. The PEC is also applied during the EBL files generation. In general, the PMMA can be developed in the MIBK and IPA mixed solution. Different MIBK and IPA ratios lead to different resolution. Based on the datasheet [58], the best development resolution can be achieved with 1:3 ratio of MIBK and IPA. Different development time is tried from 30 seconds to 90 seconds. Both microscope and profiler are used to check the development results. The 60 seconds development can remove all the exposed resist based on the microscope and profiler check. The developed patterns are imaged using SEM to check for resist clearance, especially in the doping window of the nanowire. In Fig.4.8, the pattern with different dose combinations are shown. The designed dimensions of the small doping windows in sub-figure (b) is 150 nm × 50 nm. Both images were taken after the PMMA development process. The darker regions represent the resist PMMA after development and the rest of regions are SiO_2 underneath.

And the gap between two coarse doping areas is 300 nm. At the same, the PMMA is removed clearly either on coarse and fine doping areas. By comparing the design dimensions and the SEM image, the coarse beam and fine beam dose are chosen to be 1650 $\mu C/cm^{-2}$ and 2400 $\mu C/cm^{-2}$ separately. The new dose information is then used for the real sample. The sample is dehydrated in 120°C oven for 15 minutes to remove the surface moisture followed by spinning and baking process. After exposure, the sample is developed in solution of MIBK and IPA with the ratio 1:3 for 60 seconds. Then the 1 minute IPA rinse is applied after development to remove the developer. The SEM image of one of the test devices on the real sample after development is shown in Fig.4.9 (a). The PECVD SiO_2 region is exposed after development process. The middle small region represents the central doping area in the design.

The design size of the fine doping window in Fig.4.9 is 100 nm × 300 nm. From sub-figure (a), the size of the fine window is 140 nm × 330 nm, which is very close to the design dimensions. And no PMMA is obtained left on the small doping area after

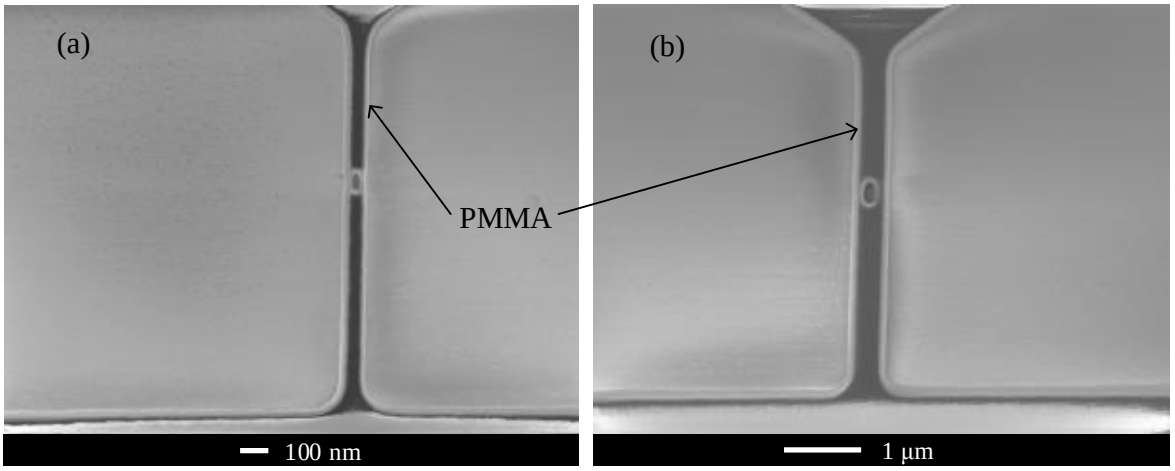


Figure 4.8: SEM images of doping windows patterning with PMMA950K A7 after development on the test chip. (a) An example of over-dose with 2900 μC/cm^{-2} coarse beam and 3000 μC/cm^{-2} fine beam. (b) An example of proper dose with 1700 μC/cm^{-2} coarse beam and 2400 μC/cm^{-2} fine beam.

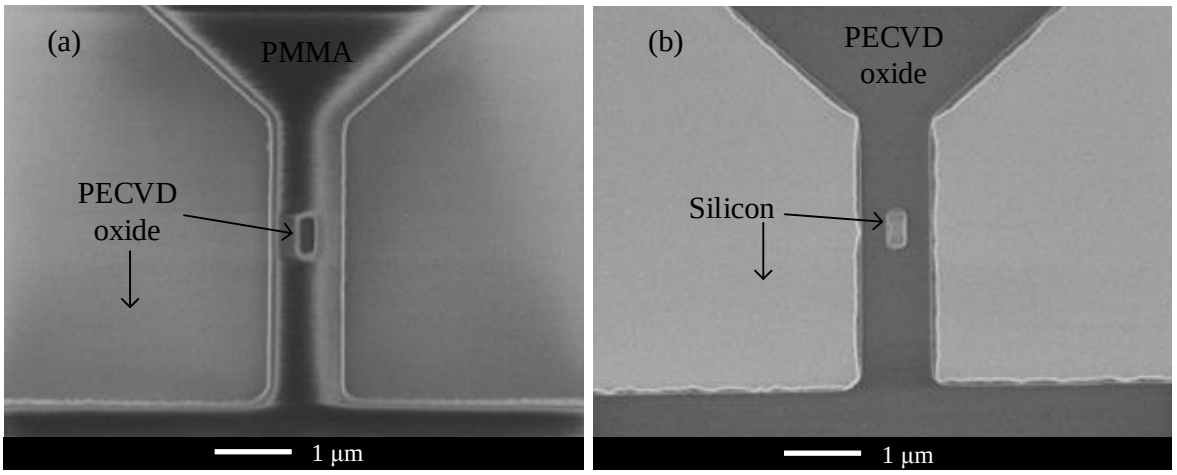


Figure 4.9: SEE images of the test devices on real sample. (a) The SEM is took after the development process. (b) This sub-figure shows the device after PECVD SiO_2 etch and PMMA removal.

development, which helps the dopants to diffuse into the silicon later. As for the coarse patterns, the gap between then is 800 nm in design. The developed gap shows 680 nm and it is acceptable. Therefore, the desired patterns dimensions can be transferred properly by using the above dose and development process based on PMMA950K A7. The PECVD oxide is exposed after PMMA development. The SiO_2 RIE dry etch is used to open the doping windows on the oxide doping mask and the SiO_2 etch recipe is shown in Table.4.5. More Ar is used for the physical etch to produce the vertical side wall. The sample is etched for 6 minutes to ensure all PECVD oxide has been removed, followed by 15 minutes resist removal process. The SEM image of the same device after SiO_2 etch and PMMA removal is shown in Fig.4.9 (b). Due to the over-etch, the size

Table 4.5: PECVD SiO_2 RIE etch recipes for opening doping windows.

Parameters	SiO_2 RIE etch recipe
CHF_3 gas flow rate (sccm)	12
Ar (sccm)	38
Set pressure (mTorr)	30
Strike pressure (mTorr)	50
RF power (W)	200
Table temperature (^oC)	20
Table type	quartz
Etch rate	$\sim$ 21 nm/minute
Selectivity to PMMA950K A7	4:3

of the fine doping becomes 180 nm $\times$ 380 nm, which is slightly larger than design but it is still acceptable. With the over-etch, the PECVD oxide at coarse and fine doping areas is removed clearly. Otherwise, there will be a problem for dopant to diffuse into the silicon.

There are two general methods to diffusion dopants, thermal diffusion in tube furnace and rapid thermal annealing (RTA) diffusion. For thermal diffusion with tube furnace, the sample will be annealed at the certain temperature for the set time under the N_2 environment. During the drive in process, the dopants will diffuse into silicon in downward and lateral directions at the same time and it is more difficult to control the lateral diffusion length using furnace. By comparing with the furnace thermal diffusion, RTA is designed to produce the shallow diffusion depth and the lateral diffusion effect can be minimised. On the other hand, the temperature ramp up in RTA can be much faster than furnace to reduce the lateral diffusion length. Through the review of furnace diffusion and RTA method, the RTA is decided to be used for diffusion.

As stated above, the spin-on dopant method is going to be used for doping process. In general, the dopants P707 is put inside the fridge for storage. Based on the dopants manufacture report, it is better to make sure the dopants are at room temperature before use. So the dopants is put into room temperature for overnight to keep the dopants at the best condition for doping. The dopant is spun on the sample at 3000 rpm for 30 seconds. Due to the main chemical material of SOD is SiO_2, so the thickness of the SOD layer can be measured by using ellipsometer. The resulting thickness of SOD is around 200 nm. The problem of SOD is that there will be many bubbles remained in the SOD layer after spinning, where oxygen can react with the silicon during the diffusion process. In order to remove the bubbles and extra solvent, the sample is baked at 165°C for 15 minutes on hot plate firstly followed by the 30 minutes furnace baking at 430°C. The bubbles and extra solvent cannot be removed using the hot plate only, so another bake process in furnace is needed. The temperature of the furnace baking is set to be 430°C. This temperature can help with the extra baking without diffusing any dopants into silicon. After the sample is coated with SOD, the dopants are ready to be diffused.

In order to keep the RTA chamber without contamination, 100 nm PECVD SiO_2 is deposited on sample as the cap layer. The doping target is to get the shallow diffusion with 10^{20} cm^{-3} concentration in the silicon layer of SOI. Thus, 10 nm is set to be the diffusion depth out of 60 nm silicon. In order to control the control the diffusion depth and lateral diffusion more precisely, the drive in temperature is chosen to be 950°C. Meanwhile, the rate of temperature ramp up and down is controlled to be 10°C/sec. In order to get the diffusion time, the diffusion length equation Eq.4.4 can be used to estimate the diffusion time, where L is the diffusion length, D is the diffusion coefficient and t is the diffusion time [59].

$$L \cong \sqrt{Dt} \tag{4.4}$$

The diffusion coefficient D is temperature dependent, the value of D at 950°C is about 6 $\times$ 10^{-15} cm/s [59]. Based on the above equation and the diffusion coefficient, the time calculated to be around 2 minutes. The Eq.4.4 is used to estimate the time, so in the real situation, different annealing time around 2 minutes need to be tested and compare the resulting doping concentration to select the proper diffusion time. Three 70 nm SOI samples are used for test with 1 minute, 1 minute 30 seconds and 2 minutes diffusion time separately. The resulting sheet resistance are 72 Ω/□, 66 Ω/□ and 60 Ω/□ respectively. The corresponding doping concentration can be calculated from Eq.4.5, where L is the diffusion depth and μ_n is the electron mobility.

$$\begin{aligned} \rho &= R_S \times L = \frac{1}{\mu_n q N} \\ \mu &= \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (\frac{N}{N_r})^{\alpha}} \end{aligned} \tag{4.5}$$

The value of mobility depends both on the dopants type and doping concentration. For phosphorus, the values of μ_{min}, μ_{max}, N_r and α are 68.5 cm^2/Vs, 1414 cm^2/Vs, 9.2 $\times$ 10^{16} cm^{-3} and 0.711 respectively [60]. For those three tests, the junction depth is assumed to be 60 nm. By substituting these parameters into Eq.4.5, the doping concentration can be calculated and shown in Table.4.6.

Table 4.6: Doping concentration for different RTA diffusion time.

RTA diffusion time	R_S (Ω/□)	ρ (Ω-cm)	Doping concentration (cm^{-3})
1 minute	72	4.32 $\times$ 10^{-4}	1 $\times$ 10^{20}
1.5 minute	66	3.96 $\times$ 10^{-4}	2 $\times$ 10^{20}
2 minute	60	3.6 $\times$ 10^{-4}	2.4 $\times$ 10^{20}

Through the calculation results, the doping concentration is above 10^{20} cm^{-3}, which meets the design target. The TLM structure will be used for room temperature to extract the doping concentration in the measurement chapter. In order to increase the chance to get dopants clusters at low temperature, the diffusion time 1 minute is used due to its lower doping concentration is lower than the other two situations. After RTA

annealing, the SOD becomes the SiO_2 and can be removed by 20:1 BHF. At the same time, two PECVD SiO_2 layers can also be etched away. The BHF etch rates of PECVD oxide and SOD are different to the thermally grown oxide. Through couple of each tests, the PECVD SiO_2 etch rate is about 1.1 nm/second in 20:1 BHF. As for SOD, 20 seconds 20:1 BHF dip is enough to remove all surface SOD. The total thickness of SiO_2 on SOI after RTA is 420 nm, including 220 nm PECVD SiO_2 and 200 nm SOD. Based on the test etch rates, the sample is etched in 20:1 BHF for 7 minutes with 75% over-etch. The sample is now doped on the designed areas and its ready for the next process.

4.5 Nanowire definition with HSQ and RIE dry etch

The Ebeam lithography is still needed for the nanowire definitions. Instead of using the positive resist, the negative resist HSQ is used. The nano-scale high resolution nanowire can be remained after electron beam exposure. Both coarse and fine beams are needed for nanowire layer Ebeam lithography and there is an overlap between coarse and fine regions. The detail of the design is shown in Fig.4.10.

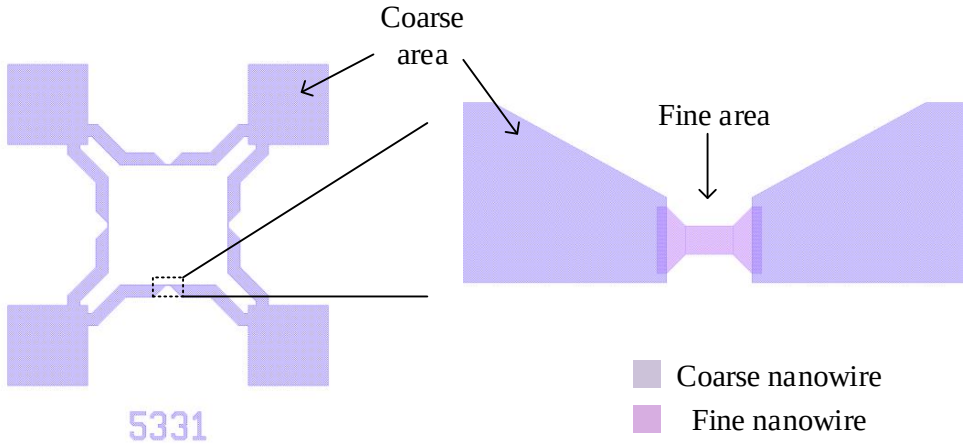


Figure 4.10: The EBL design of the nanowire layer is shown. The coarse and fine regions are indicated.

The overlap of the coarse and fine regions is designed to keep the continuity of the nanowire from misalignment. The taper shape coarse region can help reduce the oxidation stress accumulation. The fine beam used for the nanowire has 1 nA current and 60 μm aperture. The resulting beam spot size is 4 nm and it can be used to achieve the nanometer-scale fine patterns. The 25 nA current and 200 μm aperture are applied for coarse beam. The resulting beam spot size is 20 nm, which can be used to write the coarse regions with less writing time. There are two different negative Ebeam lithography resist provided, HSQ and UVN30. The Ebeam lithography resolution of UVN30 is around 150 nm [61] and the resolution of HSQ has been demonstrated to achieve 10 nm

[62]. Therefore, HSQ is used over UVN30. There are different diluted HSQ 2%, 4% and 6% can be used. The lower the dilution is, the better the resolution is. On the other hand, the lower dilution HSQ will produce the thinner layer after spinning. Like the SOD used for doping, the HSQ will be similar to SiO_2 after process and can be removed by BHF. The ranges of the HSQ thickness for different dilution are 30 nm-60 nm for 2%, 55 nm-115 nm for 4% and 85 nm-180 nm for 6%. Since the silicon layer on SOI sample needs to be RIE dry etched after the Ebeam lithography, so the thickness of HSQ has to be thick enough to etch all 50 nm silicon. Therefore, the 6% HSQ is used. The 6% HSQ is spun at 5000 rpm for 30 seconds followed by 4 minutes baking at 80°C, which will produce 93 nm HSQ layer. In order to get the correct dose information for coarse and fine beams, the dose test is processed firstly with 6% HSQ on silicon chip. By using the same dose test strategy as the PMMA950K A7, 9 × 9 patterns matrix is used for the HSQ dose test. For the coarse beam dose, the dose ranges from 1200 $\mu C/cm^{-2}$ to 2000 $\mu C/cm^{-2}$ with step 100 $\mu C/cm^{-2}$ along row 1 to row 9. For the fine beam dose, it changes from 1600 $\mu C/cm^{-2}$ to 2400 $\mu C/cm^{-2}$ with 100 $\mu C/cm^{-2}$ step along column 1 to column 9. The PEC is also applied to the patterns during the Ebeam lithography files formation. Different development time from 1 minute to 2 minutes are tried in developer MF319. Through the development test, 1 minute 40 seconds development followed by DI water rinse and 1 minute IPA rinse can give the best results. Due to the HSQ will be used as the RIE dry etch mask later, 4 minutes 30 seconds hard bake at 250°C on hot plate is applied to harden the resist layer. The SEM check of the patterns at different chip locations are shown in Fig.4.11. The design dimensions of (a) is 500 nm × 300 nm and 500 nm × 200 nm for (b). Both SEM images show that the real dimensions decrease around 50 nm, which is still acceptable to transfer the patterns using 6% HSQ. At the same time, there is no contrast difference or suddenly dimension change at the overlap area. Therefore, those coarse and fine beam dose can be applied to the real sample.

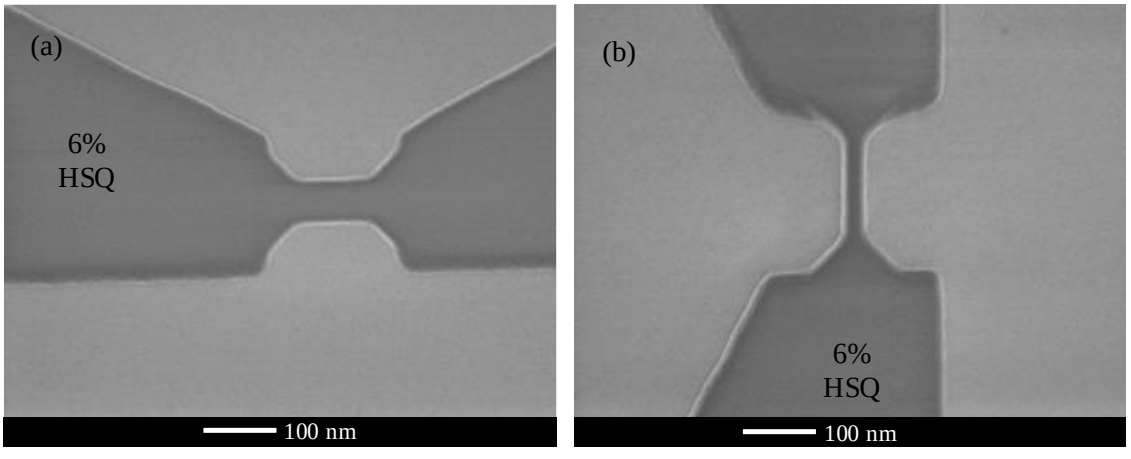


Figure 4.11: SEM of the 6% HSQ on silicon chip after exposure and development. For both (a) and (b), the fine beam dose is 1600 $\mu C/cm^{-2}$ and coarse beam dose is 1200 $\mu C/cm^{-2}$.

Table 4.7: The silicon nanowire RIE recipe with 6% HSQ.

Parameters	Silicon RIE etch recipe
O_2 gas flow rate (sccm)	36
SF_6 (sccm)	36
Set pressure (mTorr)	30
Strike pressure (mTorr)	50
RF power (W)	100
Table temperature (^oC)	20
Table type	quartz
Etch rate	$\sim$ 0.8 nm/second
Selectivity to 6% HSQ	3:2

In order to transfer the patterns from HSQ to silicon layer, the RIE dry etch is used. The RIE silicon etch recipe is shown in Table.4.7. The sample is etched for 80 seconds to fully remove the unwanted silicon to minimise the current leakage between two adjacent devices. Through the dry etch recipe, the selectivity is controlled to be 3:2, which helps to etch all silicon without consuming all the HSQ. Then the sample is put into 20:1 BHF to remove the surface HSQ. The etch rate test is carried out firstly with the 6% on silicon sample and the resulting etch rate is approximate 11 nm/second. As for the real sample, the areas without HSQ are etched away. So the BOX layer is exposed without any protection. Thus, the BOX and the surface HSQ will be etched in BHF at the same time. The longer the etch time is, the more BOX will be etched and this will cause the profile change problem of the device. So the etch time needs to be controlled precisely. Based on the thickness of 6% HSQ and the etch rate, there is around 50 nm HSQ left on surface after RIE etch. So the sample is dipped in 20:1 BHF for 5 seconds to remove all HSQ and prevent the over-etch of BOX. The SEM images of the nanowire after RIE etch and BHF clean are shown in Fig.4.12. From Fig.4.12, there is no silicon left on the BOX region so that the current leakage from device to device can be minimised. Meanwhile, the nanowire dimension deviation is around 5%, which means the desired nanowire design is transferred to silicon successfully. The size of notch region is controlled to be around 50-70 nm for better potential confinement.

4.6 Gate oxide formation

After the nanowire formation, the gate oxide is ready to be grown. In order to achieve the better gate current leakage isolation and better gate control over the nanowire, the thickness of gate oxide is chosen to be 10 nm. The thickness cannot be too thick, otherwise the thickness of silicon layer will be too thin and decrease the output current. The dry oxidation is used to form the gate oxide since the oxidation rate can be controlled accurately and the oxide quality is better. Several silicon chips are used for the oxidation test at 950 °C in furnace for 5 minutes, 10 minutes and 15 minutes. Through the test,

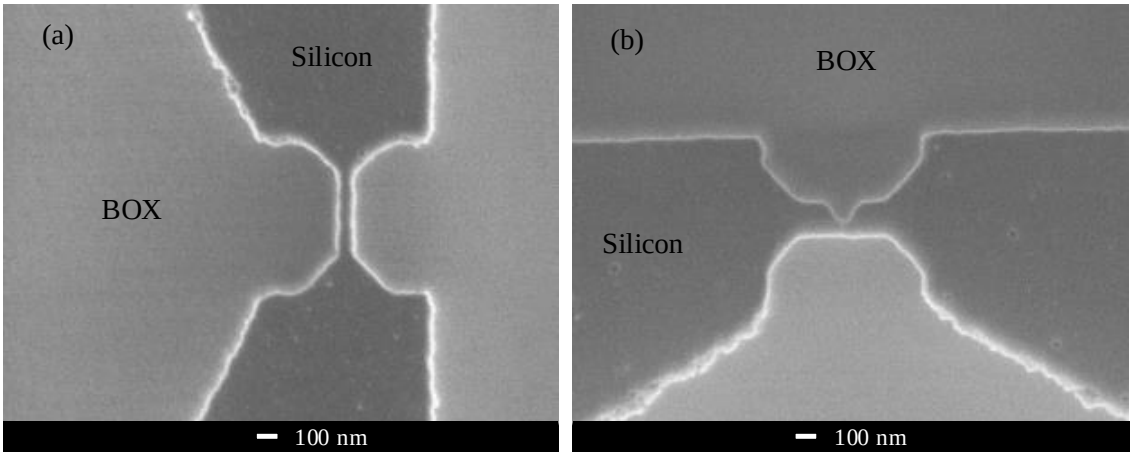


Figure 4.12: The SEM images of two different shape nanowires are shown.

10 minutes dry oxidation at 950 °C produces around 10 nm SiO_2. However, the doped silicon will be oxidised faster than the intrinsic silicon. So the dry oxidation at 950 °C for 7 minutes is applied to the real sample for gate oxide. As a result, the new thickness of silicon layer on SOI is around 55 nm.

4.7 Source/drain and gate contacts metallization

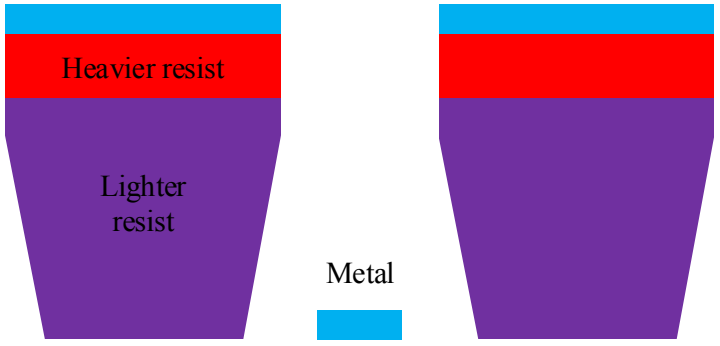


Figure 4.13: The resit profile of the bi-layer EBL resit after exposure, development and metal deposition. The heavier means higher molecular weight and the lighter means low molecular weight. The bi-layer resist undercut feature is also shown.

The final steps of the device fabrication is the contacts metallization. For this device batch, the Al is used as the source/drain and gate contacts. The source and drain Al contacts will be deposited firstly due to the different EBL resist. In order to minimise the source and drain resistance, the contacts need to be brought to the edge of nanowire as close as possible. Therefore, there is a 200 nm gap between the source/drain Al contact edge to the edge of nanowire. In order to avoid the misalignment, the EBL method is also used for the source and drain contacts. As for the source and drain contact

patterns, there are only coarse patterns but not fine regions. So only the coarse beam is used. The thicker Al contact can help to make the better contact with the silicon layer underneath. At the same time, the thicker Al pads also can prevent them being scratched away by the prober needle during the measurement. Therefore, the thickness of source and drain Al contacts is set to be 150 nm. In order to achieve this thickness and make the metal lift-off process more effective, the bi-layer positive EBL resist is used. The heavier resist on the lighter resist can produce the profile after exposure and development like Fig.4.13.

Because the beam electron and the backscattering electrons move easily inside the lighter resist so more resist will be exposed. The resulting resist profile prevent the metal being deposited on the resist side wall and the unneeded metal can be lifted off much easier. In order to make sure the metal can be lifted off properly, the thickness of the lighter resist is better to be double of the thickness of metal and the thickness of upper heavier resist needs to be thinner than that of the lighter resist. So the PMMA950K A4 is used as the upper layer and the PMMA495K A6 is used as the second layer. The number "950K" and "495K" represent the molecular weight of the material. For PMMA resist, the exposed polymer could form undergo cutting, which helps it to be dissolved quickly in the developer and make the lift-off process easier.

Through multiple tests, the thickness of PMMA495K A6 is 300 nm at 3000 rpm and it is the double thickness of metal. As for the upper layer PMMA950 A4, the 3000 rpm spinning speed is also selected and the resulting thickness is around 200 nm. Therefore, the PMMA495K A6 is firstly spun at 3000 rpm for 60 seconds followed by 65 seconds hot plate baking at 180°C . Then the sample is left at room temperature for 10-15 minutes to let it cool down. Then the PMMA950 A4 is spun at 3000 rpm for 60 seconds, followed by 90 seconds baking at 180°C . The overall resist thickness is 500 nm. The coarse beam dose is selected through the dose test with the same testing method as before and the dose 700 $\mu C/cm^{-2}$ is used. Since the source and drain patterns are large, so the sample is developed in the solution of 1 to 1 ratio MIBK/IPA for 90 seconds and rinsed with IPA for 1 minute. Before the Al electron beam evaporation, the sample is dipped in 20:1 BHF for 30 seconds to remove the SiO_2. The metal Ebeam deposition machine Lab700 is used to deposit the Al. The sample is put under vacuum for overnight to decease the chamber pressure for better adhesion. 150 nm Al is deposited at the 0.5 $\mathring{A}$/second deposition rate with the 22% soak power and 4×10^{-7} mbar chamber pressure. The metal lift-off is finished in the 40°C heated acetone for 1 hour. The ohmic contacts between Al and SOI are formed by RTA annealing directly after the metal lift-off process. The contacts are annealed in the N_2 chamber at 450°C for 2 minutes to form the ohmic contacts and further reduce the contact resistance.

The final step of the NW-FET fabrication is the gate metal deposition. The gate patterns are different to the source and drain. The most smallest gate width in the design is 50 nm, so the fine beam is also needed. Regarding the 45 nm silicon layer and 10 nm oxide

on SOI, the thickness of the gate Al is set to be 150 nm as well to avoid the metal break at the nanowire edges. Thus, the thicker Ebeam lithography resist PMMA950K A7 single layer is used to define the gate patterns. The reason to use single layer is because the single layer could provide the higher resolution. Based on the previous doping test for doping windows, the fine beam dose is set to 2200 $\mu C/cm^{-2}$ and the coarse beam dose is 1650 $\mu C/cm^{-2}$. The PMMA is spun at 6000 rpm for 60 seconds to produce the 400 nm resist. 90 seconds hard baking on hot plate at 180°C is applied afterwards. The sample is developed in 1:3 MIBK with IPA developer for 60 seconds followed by 1 minute IPA rinse. The 150 nm Al is deposited using Lab700 with the deposition rate 0.5 $\mathring{A}$/second and the 22% soak power. The sample is put in the chamber overnight so the chamber pressure is about 3×10^{-7} mbar before deposition. The sample is soaked in the 80°C heated NMP solution for 1 hour 30 minutes for metal lift-off. The final device SEM image is shown in Fig.4.14. From the SEM image, the top and turnstile gates are properly lifted-off. By comparing with the design, the gate width is around 90 nm and the gap between top gates is 100 nm, which follows the design target.

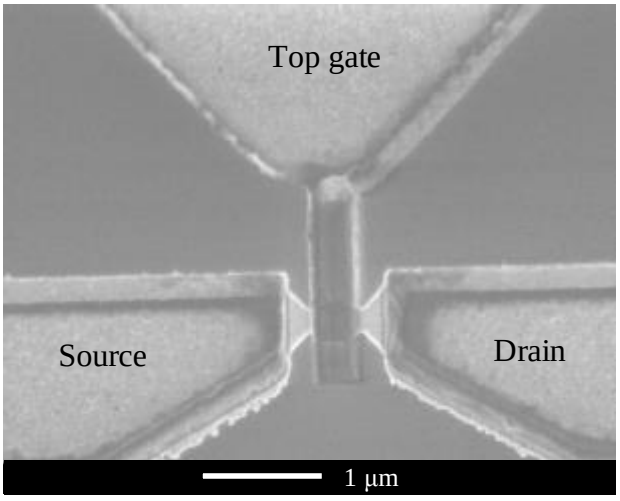


Figure 4.14: The SEM image of the an example final NW-FET with source/drain and gate contacts.

4.8 Conclusions

The Fig.4.14 shows the final NW-FET after fabrication and the design is properly transferred into the real device. Through this VLSI compatible modern fabrication process, hundreds of NW-FETs are fabricated in parallel. Based on several dose test of each EBL resist, the proper dose is used and the resulting pattern dimensions are quite close to the design dimensions. Especially the nanometer-scale nanowires are successfully fabricated with the help of HSQ and RIE dry etch. The dose test strategy is developed through the fabrication process. The real design pattern are used inside the 9×9 pattern matrix to

get the coarse and fine beam dose at the same time. By using the real patterns for dose test can help to get the more accurate dose information. Table.4.8 shows the doses used for different EBL resist for the device fabrications.

Table 4.8: The electron beam doses for different EBL resist.

EBL resist	Corresponding patterns	Ebeam type	Dose ($\mu C/cm^{-2}$)
ZEP520A	Alignment marks	Coarse beam	250
PMMA950K A7	Doping windows	Coarse/fine beam	1650/2400
6% HSQ	Nanowire	Coarse/fine beam	1100/1600
PMMA495K A6/950K A4	Source/drain contact	Coarse beam	700
PMMA950K A7	Gate contact	Coarse/fine beam	1650/2200

With the spin-on dopants and proper doping mask design, the intrinsic, selectively doped and fully doped NW-FETs are fabricated at the same time. All these different types devices will be measured in the measurement to compare the electric characteristics. On the other hand, different dimensional devices are fabricated in the same chip. By combining the doping types and different dimensions, the map of device with different situations can be measured and compared further more. At the same time, the selectively doped NW-FETs provide the chance to get the cluster of few dopants inside the channel. For the previous fabrication batches, the thickness of source/drain and gate contacts is only 80 nm-100 nm. The thin metal especially the gate metal layer, causes a lot of problems to cover the nanowire with breaks. In this fabrication process, the new PMMA resists (PMMA950K A7 and PMMA495K A6) are used. The PMMA950K A4/PMMA495 A6 PMMA bi-layer is used for the source and drain metal deposition. The 500 nm overall PMMA layer helps that the 150 nm Al is deposited as source and drain contacts. On the other hand, the thicker PMMA also makes the metal lift-off easier and quicker. Meanwhile, the thick Al on source and drain let the metal can be annealed for 2 minutes using RTA method. If keep using the 80 nm Al source/drain contacts, the 2 minutes RTA will make the Al react with the doped silicon to form pinholes and increase the contact resistance. As for gate contact, the 400 nm single PMMA950 A7 layer is used and 150 nm Al can be deposited as the top gate. At the same time, the single PMMA layer also maintain the gate resolution and the resulting gate width reaches nanometer scales.

Chapter 5

Electrical Characteristics of First Generation NW-FET and Process Feedbacks

In order to understand and gain the experience of the device design and fabrication process, the electrical characteristics of the first batch NW-FET are carried out at room temperature and low temperature 5K. The measurement results are used as feedbacks to improve the fabrication process and device design for the better device performance.

5.1 Measurement results at room and low temperature

5.1.1 Fabrication process validation from test structures

As mentioned in the fabrication chapter, there are different test structures used to characterise the fabrication process like the current isolation and sheet resistance. Firstly, the current isolation test is carried out by using two isolation pads. The isolation test is used to find if there is any current leakage, which tells whether the SOI silicon layer is fully etched or not. The voltage applied is swept from -1 V to 1 V with the step 20 mV. The corresponding current is measured and the I-V curve is shown in Fig.5.1. From the I-V measurement, the leakage current is from -150 pA to 25 pA between two adjacent contact pads and the current leakage is close to the lowest current limit fA of Agilent measurement equipment. Such a small leakage current can be negligible and it proves that the silicon is properly etched away and the devices are isolated well.

The doping and contact metallization process are two important process, which can affect the device output current and electrical characteristics. From the test structures, the transfer length measurement (TLM) structure can be used to extract the sheet

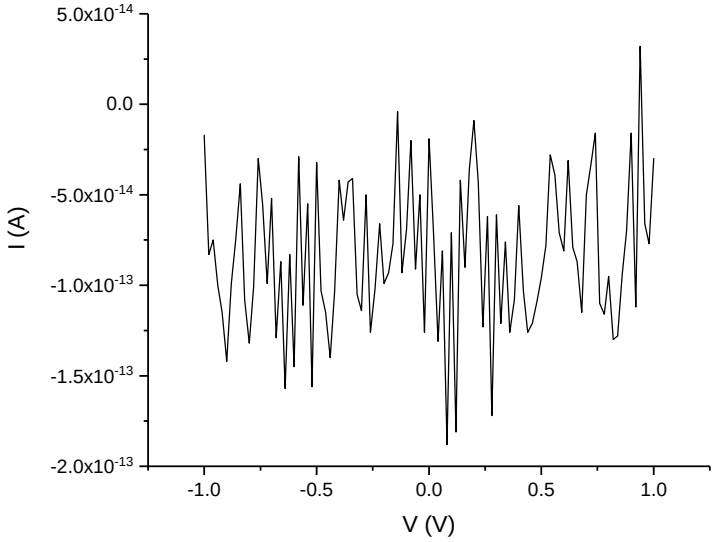


Figure 5.1: Current leakage test from isolation pads at room temperature. The measured leakage current is between -150 pA and 25 pA under bias voltage of -1 V to 1 V.

resistance and contact resistance of the doped region. Fig.5.2 shows the TLM structure and the measurement methods of sheet and contact resistance.

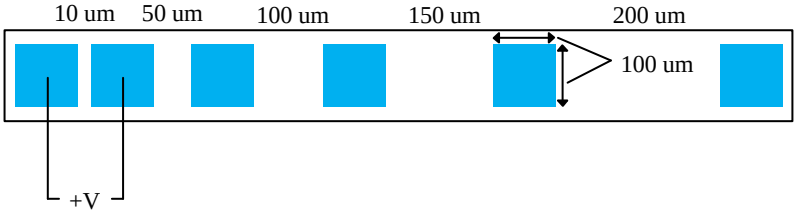


Figure 5.2: The TLM structure on the doped region for the sheet resistance and contact resistance measurement. The whole rectangular region is doped.

Al contact pads are patterned and metallized on the doped silicon region. The distance between two adjust pads are shown in Fig.5.2 from 10 μm to 200 μm and the dimension of each contact pad is 100 μm $\times$ 100 μm. By applying the voltage bias across two adjust pads, the corresponding resistance can be calculated based on the measured current. Therefore, the relationship of the resistance and distance can be plotted, where the sheet resistance and contact resistance can be extracted from the plot. During the measurement, the applied voltage across two adjust pads are from -0.5 V to 0.5 V with 5 mV step. The plot of resistance (R) with distance (D) is shown in Fig.5.3.

By applying the linear fit to the discrete points, the slope of the line is 9.86 Ω/μm. And the value of intersect point with the y-axis is 844 Ω. The physical meaning of the slope is the R_S/W, where R_S is the sheet resistance and W is the length of contact pad. Because the slope is 9.86 Ω/μm and the pad's length is 100 μm, so the sheet resistance

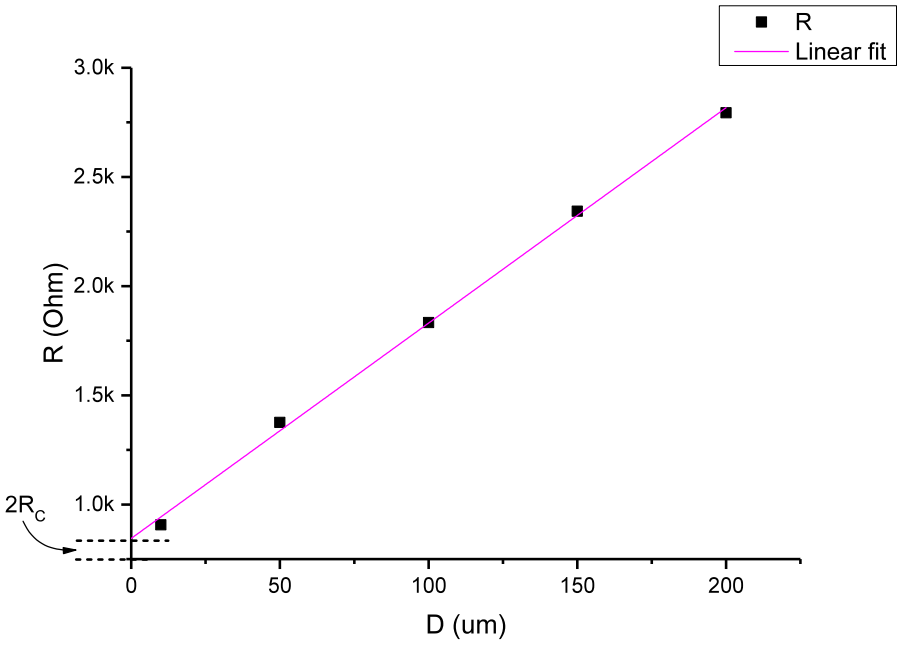


Figure 5.3: The relationship of resistance and pads distance of TLM structure measured at room temperature.

is 986 Ω/□. As for the intersect point with y-axis, its value equals to 2 × R_C, where R_C is the contact resistance. Therefore, the contact resistance is 422 Ω. The intersect point with x-axis is 85.6 μm, which is the double of transfer length (L_T) of electrons under the contact pad. From the previous chapter, the junction depth of the doped region is about 50 nm. Based on the previous parameters, the sheet resistance, doped area resistivity (ρ_{Si}), contact resistance and contact resistivity (ρ_C) can be calculated as

$$\begin{aligned} W &= 100\mu m \\ R_S &= 986\Omega/\square \\ X_j &= 50nm \\ R_C &= 422\Omega \\ L_T &= 42.8\mu m \\ \rho_{Si} &= R_S \times X_j = 4.93 \times 10^{-3}\Omega \cdot cm \\ \rho_C &= R_C \times L_T \times W = 0.018\Omega \cdot cm^2. \end{aligned} \tag{5.1}$$

Based on the resistivity value, the doping concentration is calculated to be 1.3 × 10^{19} cm^{-3}. By comparing with the four-point measurement on SOI sample, the sheet resistance is 72 Ω/□ and its smaller than the 986 Ω/□ calculated from TLM structure. The reason is that the position of the test structures are at the edge of SOI chip. During the spin-on dopants process, the SOD is non-uniform across the whole chip and it will be thinner at the edges with less dopants. On the contrary, the four-point measurement is

carried out at the middle of the test SOI chip. Therefore, the doping concentration at TLM is lower and the resulting sheet resistance is higher.

5.1.2 Short-channel effects and low temperature characteristics

The electrical characteristics measurement of the NW-FETs are conducted at room temperature using Cascade prober system and Agilent B1500A semiconductor parameter analyser. As the device design, the devices with different dimensions and different doping situations are fabricated across the whole chip. By using the same measurement setup and tools, different devices are measured at the room temperature in order to obtain the device's electrical performance. At the same time, by comparing the characteristics of different devices, the relationship of device dimension and doping situation can be got. In this section, the device with various channel width, gate length and channel doping will be discussed and compared. There are four devices will be discussed in the following sections. Table.5.1 shows the device dimensions and nanowire doping situations.

Table 5.1: Device dimensions and doping situations of four NW-FETs.

Device	Channel doping	Nanowire length	Nanowire width	Channel length
D1	Intrinsic	500 nm	200 nm	400 nm
D2	Intrinsic	500 nm	200 nm	450 nm
D3	Intrinsic	500 nm	300 nm	450 nm
D4	Selective doping	500 nm	200 nm	450 nm

The device D1 with the intrinsic channel is measured first. The length and width of the nanowire are 500 nm and 200 nm. There is a single top gate of 400 nm length at the middle of nanowire. Three probes are connected to source, drain and gate respectively. The source is always grounded. In order to get the I_{DS}-V_{DS} curve, the drain voltage bias is swept from 0 V to 2 V with step of 20 mV. Meanwhile, the V_{GS} is from -3 V to 1 V with the step 0.5 V. Fig.5.4 shows the resulting I_{DS}-V_{DS} curve.

The saturation drain current output of 5.5 μA has been achieved when the drain voltage reaches saturation at 1.5 V at gate bias of 1 V. The spread of the curves indicates that the channel can be properly controlled by the top gate. The curve shows a clear linear and saturation region indicating switching characteristic, which can be used in future low temperature measurement. During the measurement, low gate leakage current in the region of hundreds of fA is detected. Such a small gate leakage current indicates that the gate oxide formed by dry oxidation has a good quality and isolates the electrons flow from source to gate.

For the device D1, the I_{GS}-V_{DS} curve is measured when V_{GS} sweeps from -3 V to 1V with 40 mV step. Different drain biases are applied as 10 mV, 50 mV, 100 mV and 200 mV. Fig.5.5 shows the I_{GS}-V_{DS} curves under various drain bias. Through the linear fitting of the I_{DS}-V_{GS} curves, the values of threshold voltage are extracted to be -0.5 V,

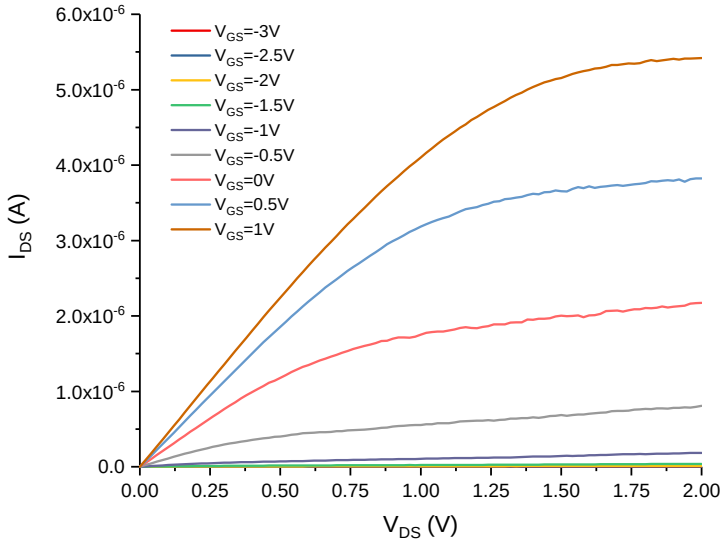


Figure 5.4: The I_{DS}-V_{DS} characteristics of device D1. The rest of curves when V_{GS} < -1 V are close to 0 A and are not obvious in plot.

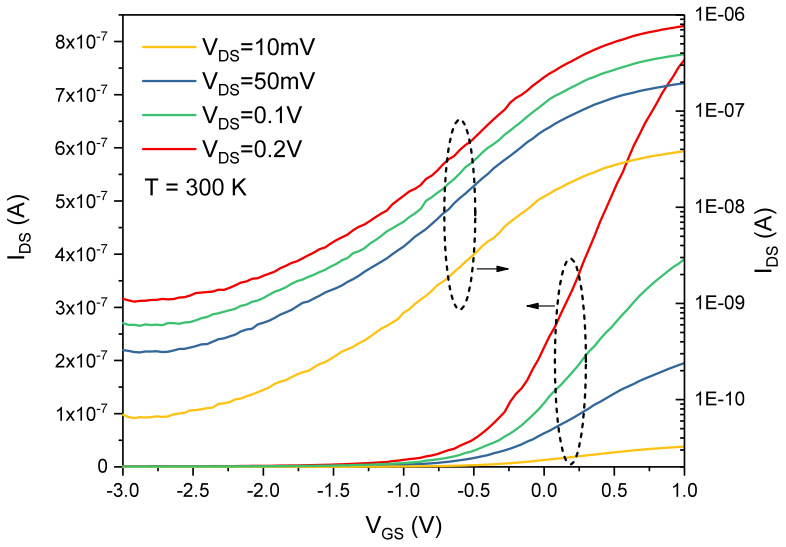


Figure 5.5: Both linear and Logarithmic I_{DS}-V_{GS} curves under various V_{DS} of D1 at room temperature.

-0.52 V, -0.53 V and -0.55 V when V_{DS} changes from 10 mV to 0.2 V. By substituting the threshold voltage into equation Eq.3.18, when V_{GS} is 0.5 V, the calculated I_{Dsat} is about 6.38 $\times$ 10^{-6} A. The re-calculated electron mobility is 107 cm^2/Vs and the new doping concentration is calculated to be 1.3 $\times$ 10^{19} cm^{-3}. By comparing the measurement result with the calculation result, the calculated value is slightly higher than the 3.5 $\times$ 10^{-6} A in the measurement. One possible reason is that the drain contact resistance, which decrease the effective voltage bias on the drain region. As a result, the real saturation current is slightly lower than the ideal calculated value. As for the threshold voltage,

based on the previous equation Eq.3.15, the calculated value should be -0.2 V. However, the real V_{th} extracted from the linear fitting I_{DS}-V_{GS} curve is around -0.5 V. The smaller V_{th} indicates that less gate voltage is needed to form the inversion layer under gate. The possible reason is that the charge form source and drain regions assist the formation of the inversion layer with gate at the same time. Due to the channel length of device D1 is 400 nm, which is shorter than 1 μm and the device can be affected by the short-channel effects.

From Fig.5.5, the sub-threshold current is very different under different drain bias. When V_{DS} is 10 mV, the OFF current is only 1×10^{-10} A, but the device can be turned on and off effectively. The OFF current is increased to be 1×10^{-9} A when the V_{DS} is 0.2 V. From Fig.5.5, the OFF current increases with the increase of V_{DS}. Meanwhile, the values of threshold voltage decrease slightly when the drain bias increases. By combining these two phenomenons, the device is influenced by the drain induced barrier lowering (DIBL) effect [63]. For the DIBL effect, when V_{DS} increases, the charge in the drain region will affect the channel formation, which makes the V_{th} to become smaller. Meanwhile, the distance between source and drain is closer when the channel length is 400 nm than a long channel device. Therefore, the source and drain become electro-statically coupled and the potential barrier becomes further lower when V_{DS} increases. As a result, the sub-threshold current increases due to the lower barrier. And the sub-threshold slop changes from 0.8 V/decade when V_{DS}=10 mV to 0.9 V/decade when V_{DS}=0.2 V. The increase of the sub-threshold slop indicates that with the increase of drain bias, the gate will lose the control of the channel further and the punch-through will happen [63].

In order to compare the device electrical characteristics of different dimensions, the second device D2 with longer gate length of 450 nm is measured. The channel is also intrinsic. The I_{DS}-V_{DS} and I_{DS}-V_{GS} curves are shown in Fig.5.6. The I_{DS}-V_{DS} curves are measured when V_{DS} sweeps from 0 V to 2 V with 20 mV step and V_{GS} is from -3 V to 1 V with the step 0.5 V. For the I_{DS}-V_{GS} curve, the V_{GS} applied is from -3 V to 1 V with 40 mV step when V_{DS} is set to be 0.3 V.

From the I_{DS}-V_{GS} curve, the device can be switched on and off and the current sweeps from 10^{-10} A to 10^{-6} A. The sub-threshold current is kept to be smaller than 1×10^{-10} A when the device is off and V_{DS} is 0.3 V. By comparing the I_{DS}-V_{GS} curve of device D1, the OFF current is one order lower at a higher drain bias. The value of V_{th} is exacted to be 0.25 V and the sub-threshold slope is around 0.56 V/decade. The possible reason for the higher V_{th} is due to the charges in gate oxide or trapped interface charges. Based the previous equation Eq.3.15, the negative charge can increase the flat band voltage and then make the V_{th} to be larger. By comparing the output current I_{Dsat} for device D1 and D2, the I_{Dsat} of D2 is smaller than that of D1 under the same drain and gate bias. As the channel length increases, the channel conductance will decrease. At the same time, the threshold voltage of D2 is higher than that of D1, which will also make the output current become lower for D2. From the MOSFET I_{Dsat} equation Eq.3.18,

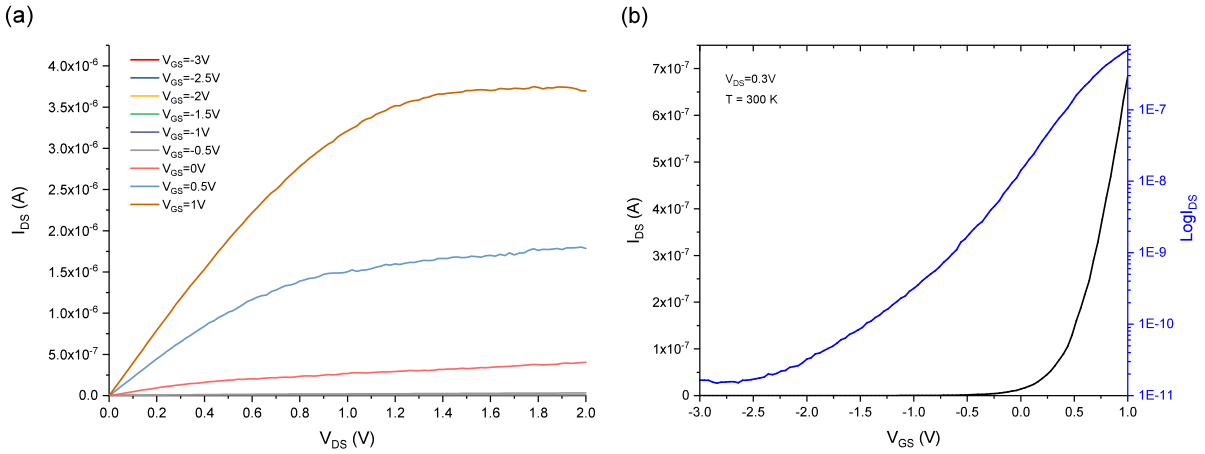


Figure 5.6: The I-V characteristics of device D2 with 450 nm top gate at room temperature. The rest of curves when $V_{GS} < 0$ V are close to 0 A and are not obvious in plot.

the current decreases with the increase of channel length, which aligns the measurement results. For device D1 and D2, the channel length has the same value as the gate length, which is around 450 nm. The third device D3 with wider channel width of 300 nm is measured to compare with D2. The nanowire length and gate length are 500 nm and 450 nm, which is the same as D2. The I-V characteristics of D3 are shown in Fig.5.7.

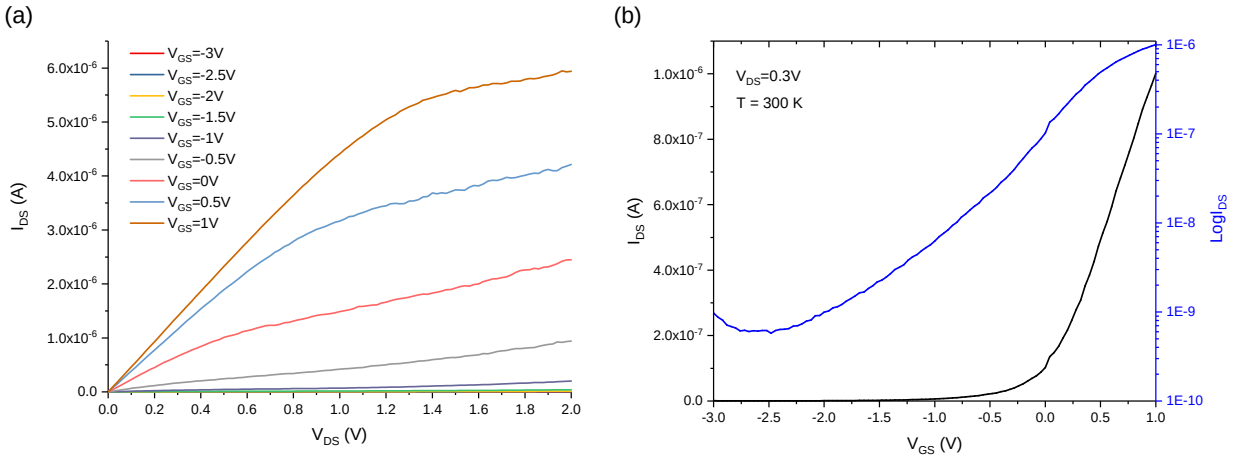


Figure 5.7: The I-V characteristics of device D3 at room temperature. The rest of curves when $V_{GS} < -1$ V are close to 0 A and are not obvious in plot.

The threshold voltage and sub-threshold slope are extracted to be -0.2 V and 0.8 V/decade. The negative value of V_{th} is similar with the calculation value as previous. By comparing the I_{DS}-V_{DS} curves of D2 and D3, the I_{Dsat} of D3 is about 1.7 times of that for D2 under the same V_{GS} and V_{DS}. Based on the MOSFET I_{Dsat} equation, the saturation current is proportional with the channel width. The ratio of channel width

for D3 and D2 is 300/200=1.5, which is the same as their I_{Dsat} ratio. One noticeable point is that the sub-threshold current of D3 is around 7×10^{-10} A, which is higher that D2. And when V_{GS} is smaller than -2.5 V, the logarithmic I_{DS} increase with decrease of V_{GS}. The reason of this phenomena could be due to the gate induced drain leakage (GIDL) [64]. Because the gate length is 450 nm, which is close to the nanowire length 500 nm. The edge of the gate may cover n-type dopants diffused from drain region from doping process. When the negative bias applied to the gate, the narrow depletion region will be formed in the drain region due to its high doping concentration. A larger band-bending will be formed under the more negative V_{GS}, which will cause the band-to-band tunnelling between p-type substrate and drain region. Meanwhile, the electron-hole pairs will be created and the electrons will flow to the drain region, which makes the drain leakage current to be high. Instead of the device with intrinsic channel, the device D4 with selectively doped channel is measured as well to be compared. The I_{DS}-V_{DS} and I_{DS}-V_{GS} curves are shown in Fig.5.8. For both I-V curves, the V_{GS} and V_{DS} bias are the same as those for D3 measurement.

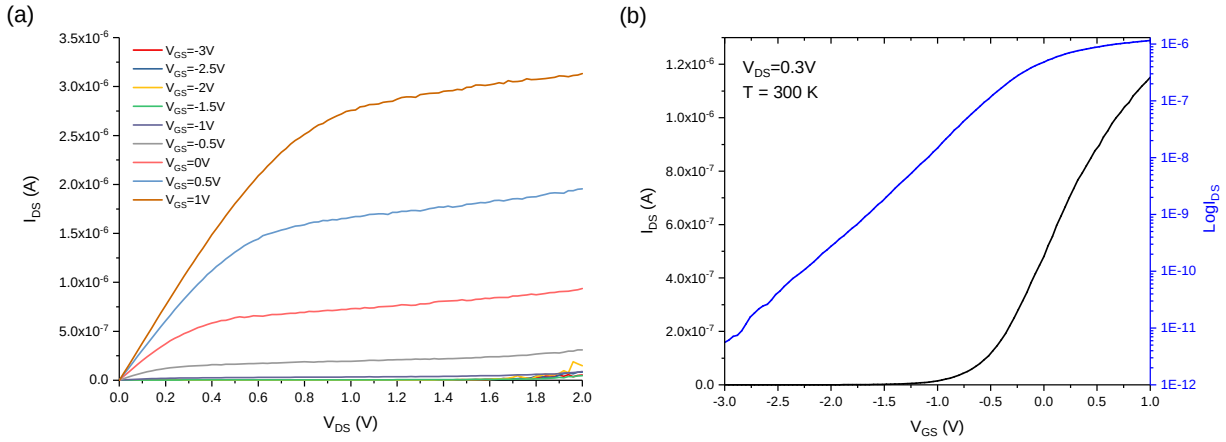


Figure 5.8: The I-V characteristics of device D4 at room temperature. The rest of curves when V_{GS} < -1 V are close to 0 A and are not obvious in plot.

The dimension of the nanowire is 500 nm by 200 nm. The gate length is 450 nm. The channel doping area is 50 nm by 200 nm under the top gate. The V_{th} is extracted to be -0.7 V and sub-threshold slop equals to 0.5 V/decade. The OFF current is controlled to be smaller than 1×10^{-11} A when V_{DS} is 0.3 V. And the ON current can reach to 1×10^{-6} A and the ON/OFF current ratio is about order 5, which shows a proper switching characteristic. From the previous device simulation results, the centre doping area along the channel has the effect to reduce the V_{th}. The V_{th} of D4 is the smallest one by comparing with D1, D2 and D3. By comparing the I_{DS}-V_{DS} curves with D2, the output current I_{Dsat} has the similar value at the same V_{DS} and V_{GS}. Based on the conclusion from device simulation, the selectively channel doping will decrease the threshold voltage but the saturation output current will be remained at the same level, which matches the measurement results.

Four devices with different dimensions and channel doping situations are measured at room temperature. The same V_{DS} and V_{GS} biases are used for all I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics in order to get the accurate device comparison. Due to the channel length for all device is around 400 nm to 450 nm, the electric characteristics are influenced by the short-channel effects including DIBL and GIDL. The I-V characteristics like V_{th} shift and high sub-threshold leakage current are existed in different device due to these effects. The corresponding signatures in the I-V characteristics are pointed out and explained. Based on the measurement, the shorter channel will let the device to have higher output current, which is proven by classical MOSFET equations. The main difference between the device with intrinsic and doped channel is their threshold voltage. Through the device simulation and measurement, the selectively channel doping will make the V_{th} to be lower. The reason is that the extra charge provided by dopants under gate decrease the voltage needed to form the inversion layer. Through the measurement, the I-V characteristics of devices prove that they can work properly at room temperature.

The device with central selective doping and notched nanowire structure is selected for low temperature measurements. The whole 3 cm × 4 cm chip is diced into 4 mm × 4 mm dies and mounted onto the special low temperature carrier. The helium cryostat low temperature measurement station from Oxford Instrument is used for measurements. The dimension of the device nanowire is 500 nm × 100 nm and the gate length is 450 nm. The preliminary measurement of the device at 5K shows transistor characteristics with V_{th} shift, which is because the amount of free charge induced by dopants decreases at low temperature and more voltage is needed to create the inversion layer. With the temperature increasing, the temperature dependent measurements are carried out. The temperature dependent measurement results are shown in Fig.5.9 when V_{DS} is 1.4 V.

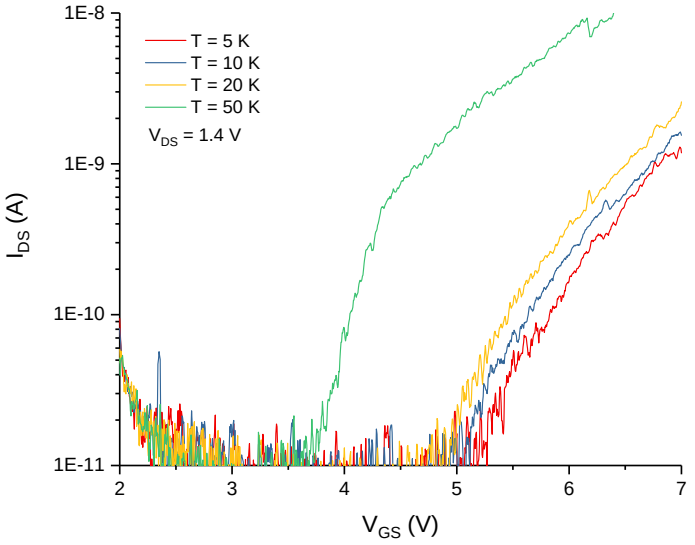


Figure 5.9: The I_{DS}-V_{GS} characteristics at different temperatures when V_{DS} = 1.4 V.

With the temperature decreasing, the V_{th} shifts to the positive direction. The reason is that less active dopants could be used to generate free electrons. As a result, the higher gate voltage is needed to form the channel. By comparing the I_{DS}-V_{GS} curves at different temperatures, the output current becomes lower with the temperature decrease. At low temperature, the mobility of electrons will become lower. Due to the dopants freeze-out, less free carriers are available to contribute for the output current. Therefore, the output current becomes much lower than room temperature. The dopants freeze-out issue requires the high V_{DS} to be applied for device operation, which decreases the Fermi level of the drain electrode. The low Fermi level of drain is not favourable for the quantum operations, because the larger energy difference between source and drain will let the electron tunnelling directly from source to drain and miss the quantum state of QD. The small current peaks observed may due to the charge scattering. From the Fig.5.9, there are no Coulomb oscillations or obvious current peaks at 5K as explained above. Although the device does not show proper quantum effects at low temperature, the room and low temperature measurement results indicate the fabrication process and device design could be applied for further batches. In the next chapter, we are going to discuss the feedbacks from the device measurements and the fabrication improvements applied for the new batch device.

From the room and low temperature measurements, the short-channel effects are obtained across different devices. Devices with different dimensions are compared and the results follow the MOSFET equations. Preliminary low temperature characteristics help to raise some defects of the device design and fabrication process. For example, the low current level indicates that the doping concentration and source/drain contacts need to be improved. Meanwhile, the potential confinement needs to be enhanced further more to provide localized sates for QD application. All of these feedbacks will be applied for the next device generation, which will be discussed in the following chapter.

Chapter 6

Fabrication and Optimisation of Few Dopants Silicon NW-FETs

6.1 Feedbacks from last batch and relative solutions

The NW-FET fabricated with process discussed in Chapter 5 shows proper FET characteristics at room and low temperatures. The preliminary results indicate the current fabrication process and device design could be applied for future devices. Based on the measurement results, the extremely low current at low temperature due to dopants freeze-out is not suitable for the measurements. From the TLM measurement results, the doping concentration is estimated to be 10^{19} cm^{-3}. However, the 1 minute RTA process will allow dopants to diffuse over short distance in silicon, which forms a very shallow doped region under silicon surface. Therefore, the shallow doped region will become frozen at low temperature quickly. In order to increase the current output, the solution is to increase the doping concentration and diffusion depth of the source and drain regions. Instead of RTA, the furnace diffusion method could be applied. By using the furnace drive-in diffusion method, the whole source/drain regions could be doped from top to bottom to prevent forming the shallow doped region. However, the issue of furnace drive-in method is that the lateral diffusion distance will increase so the diffusion simulation is needed to find out the doping profile. Meanwhile, P509 can be used as the new dopant source instead of P507 due to its high dopants concentration. Another issue of the previous fabrication process is the 5 Ebeam layer, which increases the total time of fabrication and makes it hard to get the device feedbacks quickly for further improvement. The optical lithography can be applied for large structures to decrease the fabrication time. Due to the nature of optical lithography, the alignment marks and source/drain contact layers will be exposed by optical lithography. The issue of previous device with shared contact pads is that the four devices can be treated as parallel connection when voltage applied to source and drain pads, which changes the resistance

of the device. Meanwhile, the long silicon taper also increases the device resistance. Therefore, for the next batch of device, the source and drain will be close to nanowire with shorter taper structure and each device will be isolated without shared contact pads.

6.2 New batch device design and upgraded fabrication process

6.2.1 Device design

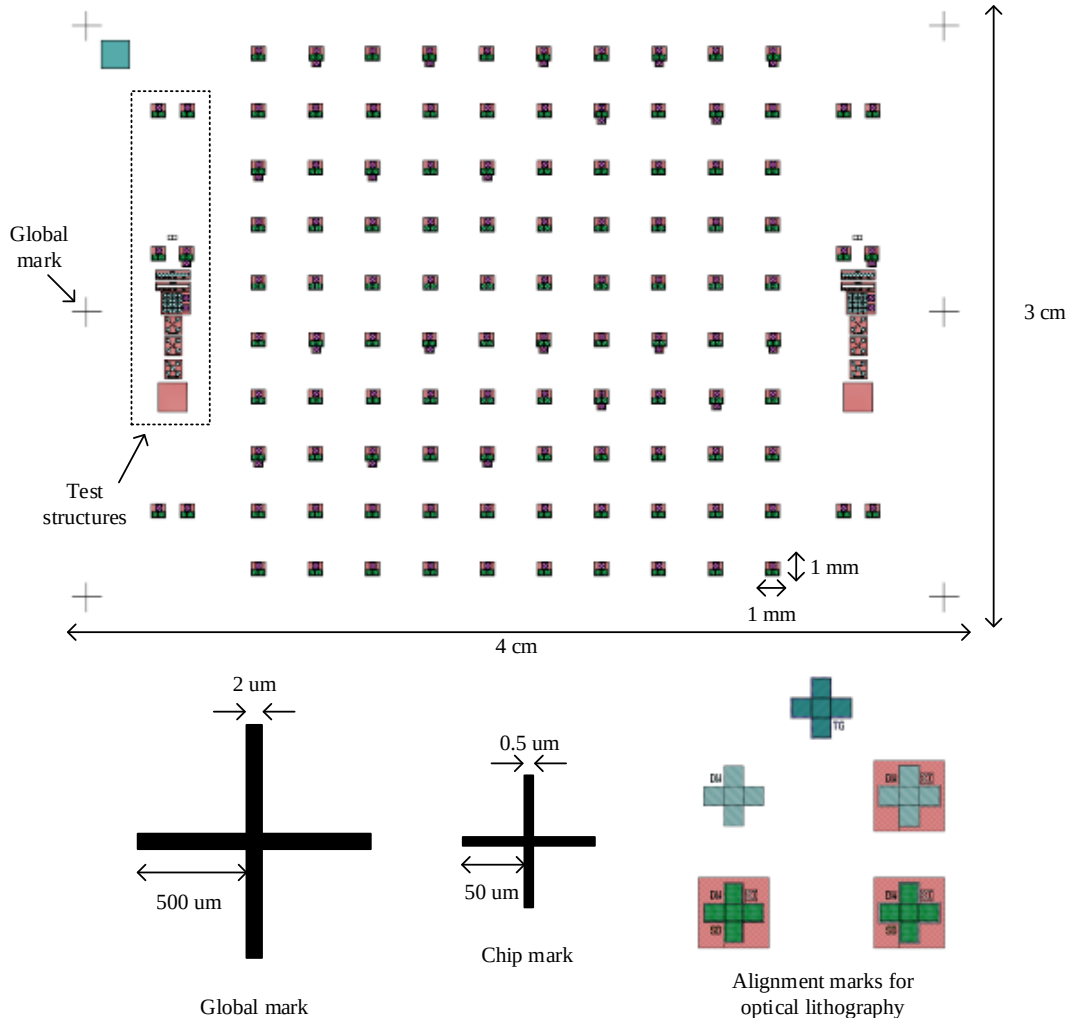


Figure 6.1: The chip layout of new batch device.The global, chip alignment marks and optical lithography alignment marks are represented.

Based on the previous discussion, the overall chip design is show in Fig.6.1. By comparing with the layout of batch one in Fig.4.1, empty spaces are inserted between device blocks. Those spaces are designed for the future chip dicing or cleaving. Instead of

Ebeam lithography, the global and chip marks are patterned with optical lithography and the size of marks are slightly larger. In addition, the group of cross shape optical alignment marks are designed as shown in Fig.6.1. The misalignment between each optical layer is set to be 2 μm. There are 50 different designs on the chip and each design is repeated twice on the chip. Wide ranges of devices dimensions are selected and the details of applied nanowire and gate dimensions are shown in Table.6.1.

Table 6.1: Details of the device dimension combinations are represented. The length and width of the nanowire are shown with gate length. The dimension of real device is picked by grouping values from length of nanowire, width of nanowire and gate length using permutation and combination method.

Length of nanowire (nm)	Width of nanowire (nm)	Notch size (mn)	Gate length (nm)
100	100	40	100
200			200
300			
400			
500			

The top and cross-section device schematics are shown in Fig.6.2. The p-type SOI sample with 100 nm silicon and 200 nm BOX layer is selected as the platform for device fabrication. The details of new design and fabrication process will be introduced in details in the following sections.

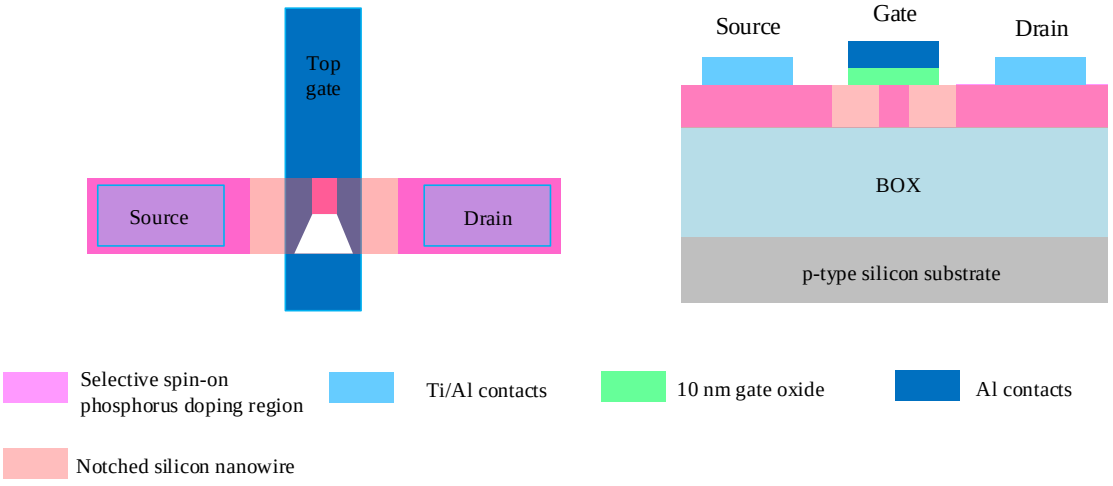


Figure 6.2: The device's top and cross-section schematic diagrams of notched nanowire.

6.2.2 Sample preparation and alignment marks formation

In order to provide a better potential confinement and standardize the process, the thickness of the silicon layer is set to be 50 nm.The dry oxidation at 1000°C is applied for 2 hours 30 minutes to thin down the silicon layer to around 40-50 nm. The resulting

formed SiO_2 is about 130 nm. Instead of stripping the SiO_2, it will be used as the doping mask for diffusion process. The reason is that the PECVD oxide can have pinholes on the surface. The dopants can diffused into silicon layer through these pinholes, which introduces random dopants in the intrinsic regions. After the sample thinning process, the alignment marks for Ebeam and optical lithography are ready to be patterned. The optical resist S1813 is spun at 5000 rpm for 30 seconds, followed by 1 minute bake at 115°C. The thickness of S1813 is around 1.2 μm, which can help to form the deeper alignment marks. After exposing with the full spectrum light for 2.5 seconds, the sample is developed in MF319 for 45 seconds. The same recipes as Table.4.3 are used to dry etch the alignment marks with the sequence of 130 nm SiO_2, 50 nm silicon, 200 nm BOX and substrate for 8 minutes, 20 seconds, 13 minutes and 3 minutes separately.

6.2.3 Diffusion with drive-in process

PMMA 950 A7 is still used as the Ebeam lithography resist for doping window patterns and the doping mask etch recipe is the same as Table.4.5. After opening the doping apertures, the SEM image of the device is shown in Fig.6.3 after removing the resist. From the SEM images, the coved SiO_2 doping mask is etched clearly and the underneath silicon layer is exposed. The size of the selective doping aperture on nanowire is around 70 nm $\times$ 100 nm, which meets the design criteria.

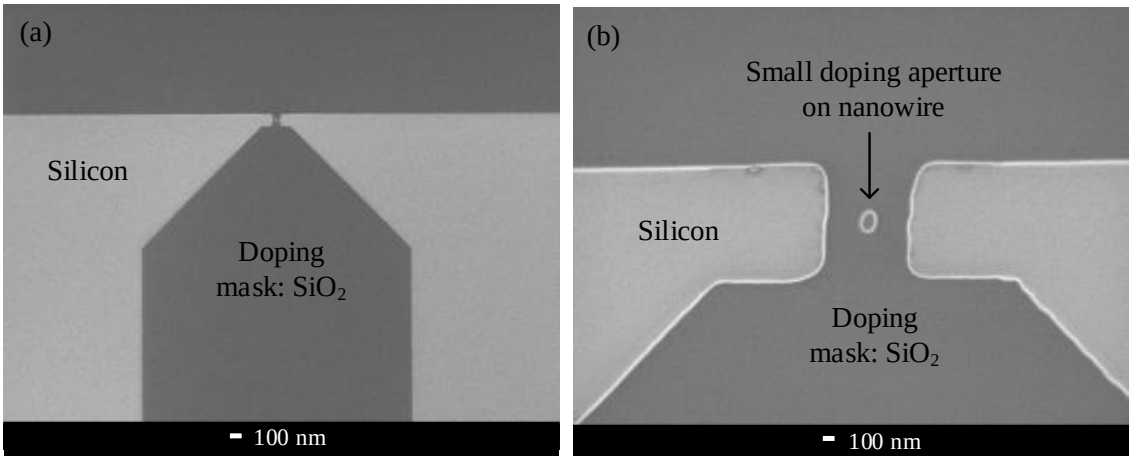


Figure 6.3: SEM images of doping windows after etching and removing resist in (a). The selective small doping aperture on nanowire is shown in (b).

The doping process is a critical step for few dopants devices. As stated previously, the spin-on dopants and doping diffusion technique are applied to simply the fabrication process and provide higher doping concentration. After doping process, the selective dopants are confined within the notch region whose volume is 40 nm $\times$ 40 nm $\times$ 40 nm after gate oxide formation. The notch design could help to increase the dopants confinement by shrink the size of notch region. There is then no need to thin down

the device silicon layer down to sub-10 nm for dopants confinement, which improves the fabrication tolerance and makes the fabrication process to be more practical. In order to get enough current flow and prevent the carrier freeze out at low temperature, the silicon layer is doped from 5×10^{18}cm^{-3} to 1×10^{19}cm^{-3}. The estimated doping profiles with different drive-in time at 950 °C are calculated with constant-total-dopant diffusion equation (6.1), S is the total amount of dopant per unit area with value 10^{14} dopants/cm^2 and D represents the value of diffusion coefficient for phosphorus at 950 °C, which is 3.2×10^{-15}cm^2/s. The calculated diffusion curves are shown in Fig.6.4 (a).

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} exp(-\frac{x^2}{4Dt}). \tag{6.1}$$

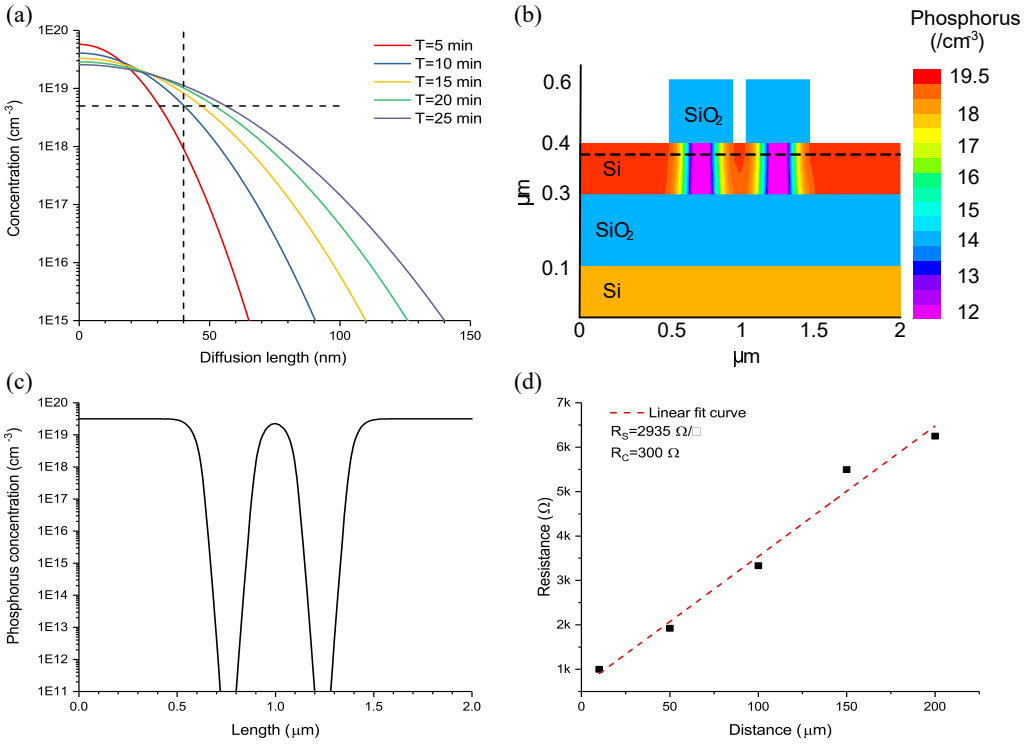


Figure 6.4: Constant-total-dopant diffusion calculations and simulations. The numerical modelling with different drive-in time is shown in (a). The 2D dopants diffusion profile simulation of phosphorus on SOI structure is presented in (b) with log scale. The phosphorus concentration along the cut line in (b) is shown in (c). The sheet resistance R_S and contact resistance R_C are extracted from TLM results (d) to be 2935 Ω/□ and 300 Ω respectively.

The vertical dash line indicates the boundary of the silicon layer thickness of 40 nm and the horizontal dash line presents the doping concentration of 5×10^{18}cm^{-3}. Based on the desired concentration explained above, the drive-in time 15 - 25 minutes can be used. Therefore, the doping concentration of whole silicon layer could be reach 5×10^{18}cm^{-3} and higher value. By comparing the different drive-in time, 15 minutes

is selected because it provide less lateral diffusion. The 2D doping simulation is run with Silvaco to confirm the lateral diffusion length of centre doping as shown in Fig.6.4 (b). The contour represents the log scale phosphorus concentration within silicon layer after diffusion process. The SiO_2 in the simulation represents the doping mask for selective doping. By reading the concentration value along the dash line in (b), the central dopants are confined successfully with the help of doping mask. By comparing the figure (b) and (c), the length of lateral diffusion is extracted to be around 100 nm to 150 nm. The lateral diffusion length is then applied during device layout design to control the position of dopants. The TLM structure is measured and the relationship of resistance and distance is shown in Fig.6.4 (d). The measured resistivity is 0.01 Ω/cm and the corresponding doping concentration is about 5×10^{18}cm^{-3}, which meets the desired value. Because the TLM structure is located at the edge of sample, the average doping concentration in the main device region will be higher due to the spin-on dopants uniformity.

6.2.4 Nanowire Ebeam lithography with ZEP520A

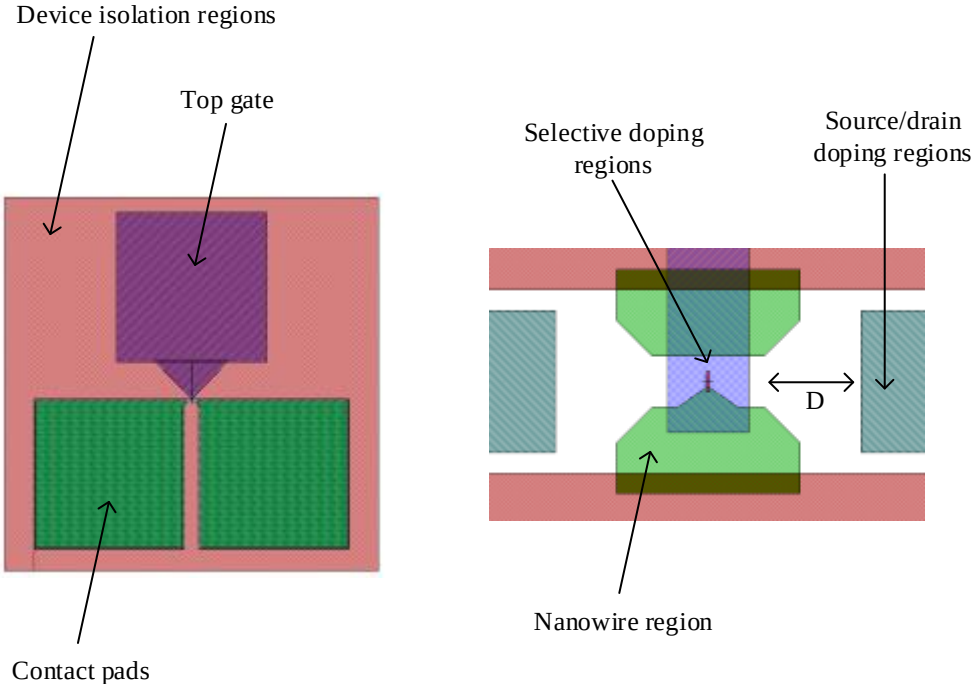


Figure 6.5: Layout design of nanowire with notch structure. The size of the nanowire is 500 nm $\times$ 100 nm. Parameter D indicates the distance between the edge of source/drain doping region and the edge of nanowire.

From the previous fabrication process, 6% HSQ was used for the nanowire Ebeam process. However, the resist HSQ is very sensitive and the dose changes with time. The exposure dose has to be recalibrated every time before exposure. Another issue of the sensitive HSQ is that the relative dry etch rate and BHF etch rate will change as well. All

of these changes need to be considered and tested, which makes the fabrication process more complicated and decreases the device yield. The solution is to used the alternative resist like ZEP520A to define the nanowire. ZEP520A is positive resist with high resolution. Apart form the fabrication process, the device design needs to be improved as well. The details of nanowire design is shown in Fig.6.5.

The use of ZEP positive resist will require exposure of the outline area around nanowire and source/drain silicon regions need to be exposed. In this way, the nanowire patterns will stay after developing process because the exposed regions are removed by developer. The large red region in Fig.6.5 is the isolate island between devices to devices. The green region on the right side is the nanowire structure with notch structure. The smallest size of the notch structure is around 50 nm after develop. ZEP is spun at 3370 rpm for 3 minutes with open lid, followed by 3 minutes bake at 180°C. After exposure, the sample is developed in ZED-N50 for 2 minutes and rinsed in IPA for 2 minutes to clean the developer. The RIE dry etch is applied to form the nanowire and the recipe is the same as Table.4.7. The SEM images after nanowire etch is shown in Fig.6.6.

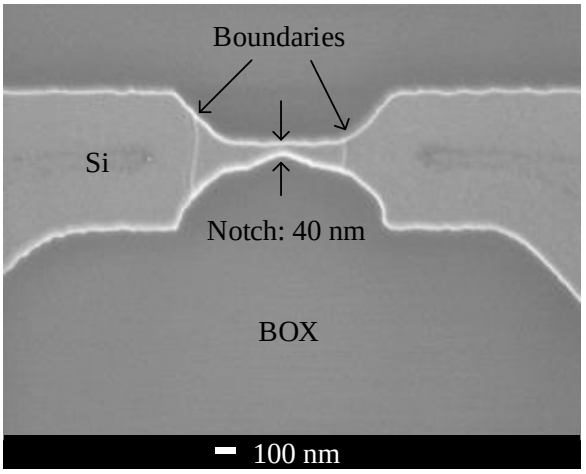


Figure 6.6: SEM image of nanowire after etch and resist ZEP removal.

The notch region is indicated by arrow in Fig.6.6 with width of 40 nm. The vertical boundaries lines at the ends of nanowire are the boundaries of intrinsic and doped silicon regions. After the nanowire etch, the sample is cleaned with FNA, RCA1 and RCA2. Then 8-10 nm gate oxide is formed with dry oxidation at 950°C for 8 minutes. The width of notch region after oxidation becomes approximately 40 nm. Meanwhile, the thickness of silicon layer is reduced to 40 nm after oxidation.

6.2.5 Source and drain contact metallization

Optical lithography is used for the source and drain patterning. In this case, negative resist AZ2070 is used for metal lift-off. Another reason of using AZ2070 is because

undercut will be formed at the edges of patterns after exposure and development, which makes the lift-off process to be easier. After the gate oxidation, the sample is dehydrated at 120°C for 10 minutes on hot plate. The 15 minutes HDMS evaporation is used to enhance the adhesion between resist and sample surface. The resist is spun at 6000 rpm for 30 seconds and baked at 110°C for 1 minute. The resulting thickness of AZ2070 is around 4 μm. Because AZ2070 is a negative resist, the optical i-line filter is used during exposure to allow the light with 365 nm wavelength passing through. After exposure for 5.5 seconds, the sample is post baked at 110°C for 1 minute again to form the cross link within resist. The sample is then developed in AZ726 for 90 seconds.

After patterning the source/drain window, the exposed gate oxide SiO_2 is removed in 20:1 BHF and the sample is ready for metallization. The metal stack Ti/Al is deposited for source and drain. The sample stays in vacuum overnight before deposition, which helps to get better vacuum condition and the metal quality will be improved. Ti is deposited firstly at 0.5 $\mathring{A}$/second for 20 nm, followed by Al deposition at 1 $\mathring{A}$/second of 200 nm. The reason of using Ti is to prevent the reaction between Al and silicon to form the pits [65], which improves the electrical conductivity of contacts. Although the chemical reactions between silicon and Ti is not very active, the reaction product $TiAl_3$ can still react with silicon to form pits within contacts. Therefore, the contact annealing temperature, time and Ti thickness need to be controlled properly. From literature study [66], the contacts quality keeps decreasing with annealing temperature and it becomes stable when the temperature is around 425°C. The annealing time of 2 minute is selected for better alloy contacts from fabrication process of the first device generation. The following equation is used to calculate the thickness of Ti layer

$$X^2 = dt$$
$$d = d_0 \times exp(-E_a/kT), \tag{6.2}$$

where $d_0 = 0.15$ cm^2/second, $E_a = 1.85$ eV. X is the thickness of Ti layer, t is the annealing time and T is the annealing temperature. The parameter d is the Ti consumption rate during the reaction with Al. As a result, the minimum thickness of Ti layer is at least 10 nm if the contacts are annealed at 425°C for 2 minutes. Therefore, 20 nm Ti is chosen to be deposited to prevent all Ti is consumed. After source/drain metallization, the metal lift-off is performed using OptiWet system. The high pressure NMP solution is applied to make sure the resist and metal will be removed clearly. The acetone bath is applied after lift-off to clean the sample and remove all the NMP left on sample. The same gate fabrication process for previous batch is used for new batch device as well. The SEM image of the device is shown in Fig.6.7. From the device SEM image, there is no gate breakage over the nanowire,which indicates that the nanowire is fully covered by the gate and this will help to provide the better gate control.

The new device generation is fabricated with the help of Ebeam and optical lithography.

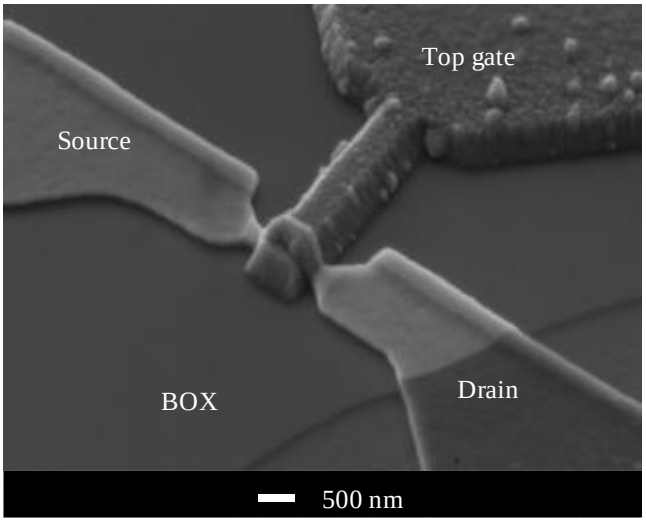


Figure 6.7: SEM image of the final device.

New Ebeam resist ZEP520A s used for nanowire patterning, which simplifies the fabrication process and reduces the device turnover time. The new spin-on dopants solution is used for higher doping concentration. Both numerical and Silvaco modelling of thermal diffusion are carried out to find the best drive-in time of 15 minutes. Meanwhile, the simulation also indicates that the lateral diffusion length is around 100 - 150 nm. Instead of pure Al contacts for source and drain, the Ti/Al contact stack is deposited to enhance the ohmic performance and provide better conduction. The device measurements and performance analysis at room and low temperatures will be presented in next chapter.

Chapter 7

Room and Low Temperature Characteristics of Optimised NW-FETs

As mentioned in the last chapter, the optimised silicon NW-FETs are fabricated with improved process. The simulation results show that the selective doping could create the localized potential well for electron tunnelling. In this chapter, devices with different doping configurations are compared under room and low temperature to understand any quantum effect induced by localized cluster dopants. Meanwhile, the device characteristics will be analysed corresponding to the optimised fabrication process, which helps to establish the relationship between electrical performance and the new fabrication methods.

7.1 Room temperature characteristics of device with intrinsic and doped channel

The devices with different doping conditions and structures will be measured at room temperature with Agilent B1500A firstly to validate the function. The test structures are measured firstly to evaluate the fabrication process. To test whether the silicon etch process is successful or not, the I-V relation is measured on the isolation pads. The bias applied is swept from -1 V to 1 V and the corresponding I-V relationship is shown in Fig.7.1. The current level shifts between -5 $\times$ 10^{-13} A to 5 $\times$ 10^{-13} A level, which closes to the lowest current limit of measurement tool. The low leakage current indicates that each device is isolated properly and there is no device to device current leakage. The TLM measurement result is shown in Fig.6.4 (d). The extracted sheet resistance R_S and contact resistance R_C are 2935 $\Omega/\square$ and 300 Ω respectively. The corresponding doping

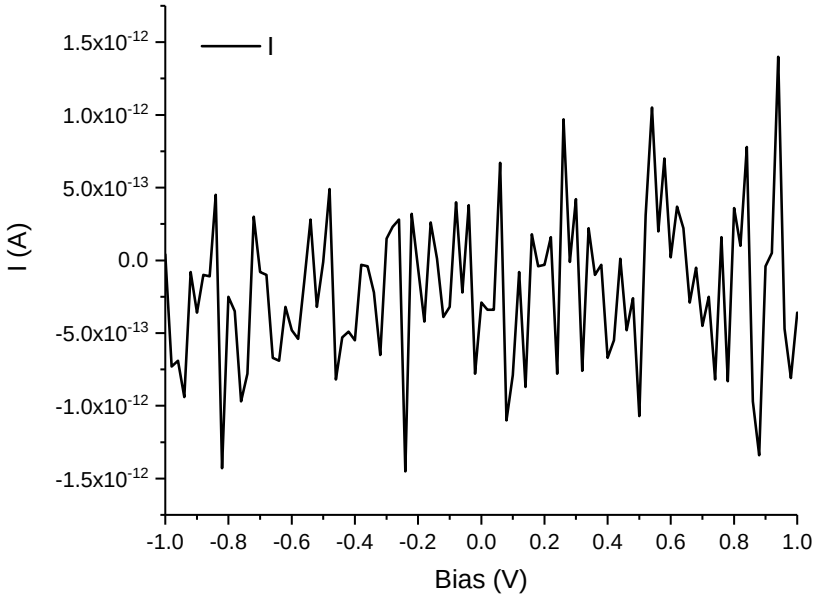


Figure 7.1: The current measured from the isolation pads when the applied voltage is from -1 V to 1 V at room temperature.

concentration can be calculated through the following parameters as shown in Eq.7.1. Based on the value of ρ_{Si}, the doping concentration is calculated to be around 3×10^{18} cm^{-3}. Though the concentration is slightly smaller than the desired value, the doping concentration at the main device area will be higher than the measured value due to the non-uniformity spinning of the dopants layer.

$$\begin{aligned} W &= 100\mu m \\ R_S &= 2935\Omega/\square \\ X_j &= 50nm \\ R_C &= 300\Omega \\ L_T &= 10\mu m \\ \rho_{Si} &= R_S \times X_j = 0.0146 \times 10^{-3}\Omega \cdot cm \\ \rho_C &= R_C \times L_T \times W = 0.003\Omega \cdot cm^2. \end{aligned} \tag{7.1}$$

Before measuring the devices with selective dopants, the devices with intrinsic channel will be measured as a reference for the following measurements. There are five different types of devices are designed to be intrinsic. The different parameter between each device is the distance from source/drain doping region boundaries to edge of nanowire, which is represented as the parameter D in Fig.6.5. The distances are 0 nm, 50 nm, 100 nm, 200 nm and 300 nm and the I_{DS}-V_{GS} curves of these five devices are shown in Fig.7.2. The drain bias is set to be 1 mV for all devices. By comparing the threshold voltage of each device in Fig.7.2, the threshold voltage keeps increasing with the increase

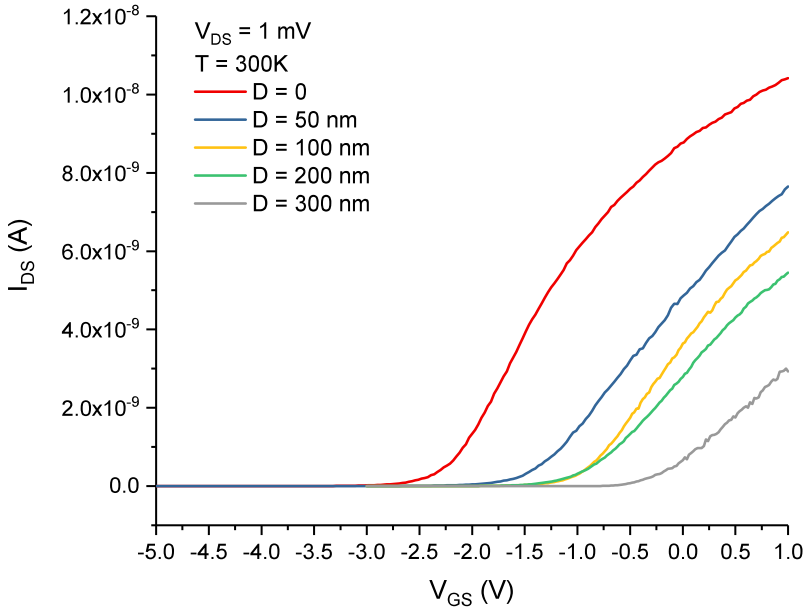


Figure 7.2: The I_{DS}-V_{GS} curves of devices with different lateral diffusion distance from 0 nm to 300 nm.

of the distance between source/drain doping region to nanowire. The V_{th} changes from around -2.5 V to -0.5 V by plotting the transconductance gm-V_{GS} curves [67]. The work function of gate Al metal contact is around 4.1 V [68]. From the Eq.3.15, the calculated V_{th} is around -0.3 V for intrinsic channel device. The V_{th} of device with D = 300 nm is -0.5 V, which is close to the calculated value. The possible reason of the value difference is because the surface and trap charges are assumed to be zero. The change of threshold voltage also makes the drain current when V_{GS} = 1 V to increase with the decrease of D, which follows that classic MOSFET drain current equation as Eq.7.2

$$I_{DS} = \frac{W}{L} \times \mu C_o (V_{GS} - V_{th}) V_{DS}, V_D << (V_{GS} - V_{th}). \tag{7.2}$$

When D = 0 nm, the dopants are diffused from source/drain to nanowire and the dopants diffusion makes the whole nanowire to be doped. Under this situation, the device becomes the junctionless transistor [69] and it performs like the accumulation mode MOSFET. The diffused dopants form the conduction path without gate bias and free charges are pushed away when the negative gate voltage is applied, which makes the device to be switched off. The threshold voltage of the junctionless transistor can be calculated from Eq.7.3 [70]

$$V_{th} = V_{FB} - qN_D[\frac{WH}{C_o} + \frac{1}{\varepsilon_{si}}(\frac{WH}{2H+W})^2], \tag{7.3}$$

where W and H are nanowire width of 100 nm and thickness of 40 nm respectively. Assuming the channel doping concentration is the same as source and drain about 5 ×

10^{18} cm^{-3}, the calculated value of V_{th} is -3 V and it is close to the extracted value -2.5 V.

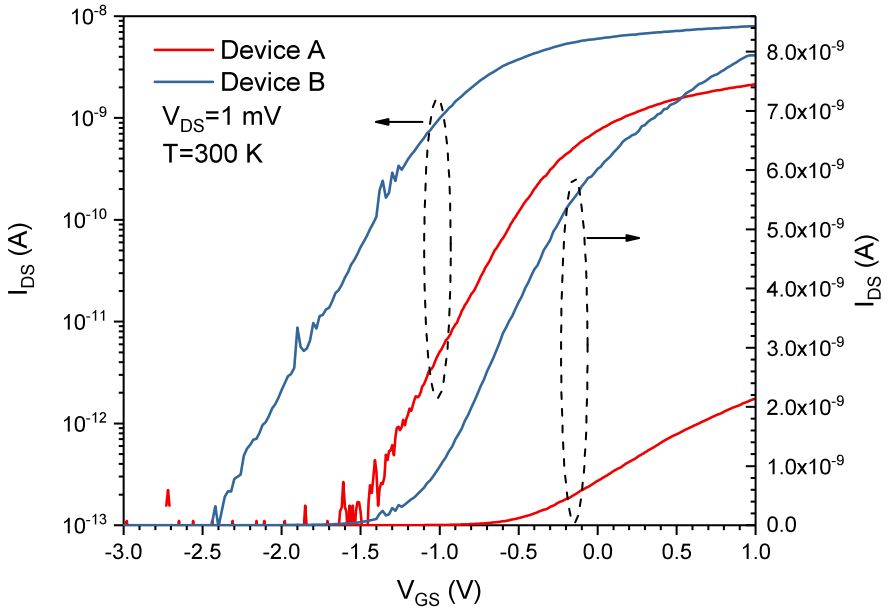


Figure 7.3: Room temperature I_{DS}-V_{GS} measurement results of Device A and B when V_{DS} = 1 mV and V_{GS} from -3 V to 1 V. Both linear and log scale plots are represented.

Based on the comparison of the electric characteristics of devices with different D, the lateral diffusion length of drive-in process is extracted to be around 200 nm to 300 nm and this value matches with the simulation result. After comparing the devices with intrinsic channel, the device with selective doping will be compared with intrinsic device. Two devices are compared: (i) a control device without channel doping Device A and (ii) Device B with central doping at the notch region of nanowire. Device A and B are firstly measured at room temperature using B1500 Agilent semiconductor analyser. The source and substrate are grounded. The I_{DS}-V_{GS} curves are measured by sweeping the V_{GS} from -3 V to 1 V with 10 mV step when V_{DS} = 1 mV and the measured results are shown in Fig.7.3.

Table 7.1: Summary of room temperature characteristics of Device A and Device B.

Device number	Channel doping	V_{th}	SS (V/decade)	On/Off ratio order
A	No	-0.7 V	0.35	10^4
B	Yes	-2.5 V	0.4	10^5

The room temperature electrical characteristics are summarized in Table.7.1. The high on/off current ratio and the low off state current indicate that the device channel could be switched on and off with top gate properly. The same threshold voltage extraction method from transconductance gm-V_{GS} is applied for Device A and B to find the V_{th}

values. From the previous V_{th} equations, the calculated threshold voltage of the intrinsic device is around -0.3 V. The difference between the calculated and measured threshold voltage may because the fixed oxide charge (Q_f), oxide trapped charge (Q_{ot}) and mobile ionic charge (Q_m) are assumed to be zero during calculation. The amount of total charge could be estimated from Eq.7.4

$$Q_f + Q_m + Q_{ot} = \frac{\Delta V_{th} \times C_o}{q}, \tag{7.4}$$

where the ΔV_{th} is the threshold voltage difference 0.4 V. The estimated amount of charge density is around 8.6 $\times$ 10^{11} cm^{-2}. By comparing the threshold voltage of Device A and Device B, since the device dimensions are identical, the difference between threshold voltage is mainly due to the channel dopants. The accumulated charge under the top gate from phosphorus dopants will decrease the potential needed to form the channel. The threshold voltage shift $\Delta V_{th-dopant}$ due to channel dopants can be expressed as

$$\Delta V_{th-dopant} = \frac{qN}{C_o}, \tag{7.5}$$

where the term qN represents the additional channel impurity density. The sign of the $\Delta V_{th-dopant}$ is negative if the doping impurities are n-type and positive if the impurities are p-type. By substituting the channel doping concentration, the calculated $\Delta V_{th-dopant}$ is around -1.7 V. Therefore, the estimated value of V_{th} for device with channel doping is -2.4 V and this value is very close to the measured data.

7.2 Low temperature characteristics of device with localized dopants

The devices A and B are proven to work properly at room temperature. Through the analysis of the values of threshold voltage of Device A and B, we can confirm that the phosphorus dopants are successfully doped into the device's channel. After the room temperature measurements, low temperature measurements are carried out to find out the device could be used for quantum application or not. Due to the absence of the measurement equipments, the device low temperature measurements are taken in the cooperate laboratory at University College London and Japan Advanced Institute of Science and Technology. For the low temperature measurement, the Helium-3 fridge system is applied to provide cryogenic conditions. The Stanford SR830 lock-in amplifier with mixed AC and DC lines is used for source/drain bias to obtain the low noise signals.

Both Device A and B are measured at 5K firstly. The source is always ground and the drain bias is kept to be mV range during the measurement to make sure the electron transport are mainly controlled by top gate. Meanwhile, the small V_{DS} value could

make the energy difference between source and drain Fermi level is minimised. The I_{DS}-V_{GS} measured curve of Device A at 5K is shown in Fig.7.4.

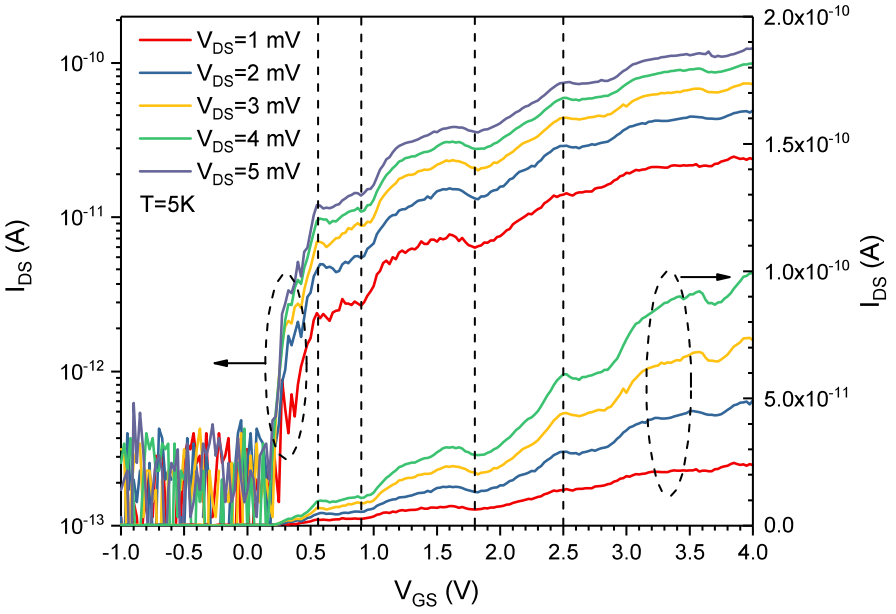


Figure 7.4: Low temperature I_{DS}-V_{GS} measurement results of Device A at 5K when V_{DS} is from 1 mV to 5 mV. Both linear and log scale plots are represented.

The V_{GS} is swept from -1 V to 4 V with 25 mV step and V_{DS} is from 1 mV to 5 mV with 1 mV step. The dash lines indicate the step-like current patterns. When V_{GS} is lower than 0 V, the device operates at the off state with 10^{-12} A current level. Due to the temperature change, more surface potential is needed to form the inversion layer as channel. As a result, the V_{th} shifts to approximately 0.3 V. At low temperature, though some dopants are frozen-out, the device can still be switched properly and the output current is in 10^{-10} A level. The step-like current shape is because the electrons are trapped and released from potential wells along the channel. However, from the room temperature measurement, there are no dopants diffused into channel through source and drain. Therefore, the main reason for potential well formation is due to the interface traps between silicon and silicon dioxide. Charges are built up at the interface and potential wells are formed along the channel. However, the potential wells are not deep enough nd the corresponding tunneling barriers are low to confine electrons deeply, which makes it hard to form quantum dot at low temperature. The Coulomb blockade effects are not obtained from Device A, which also proves that there is no proper quantum dot formed.

The Device B is then measured at 5K firstly. The measured I_{DS}-V_{GS} at 5K is shown in Fig.7.5. The gate bias applied is swept from 0.3 V to 0.9 V with 2 mV step and the drain bias changes from 2 mV to 20 mV with 2 mV step. The threshold voltage is around 0.5 V and the device could be turned on and off from 10^{-13} A to 10^{-10} A. With the

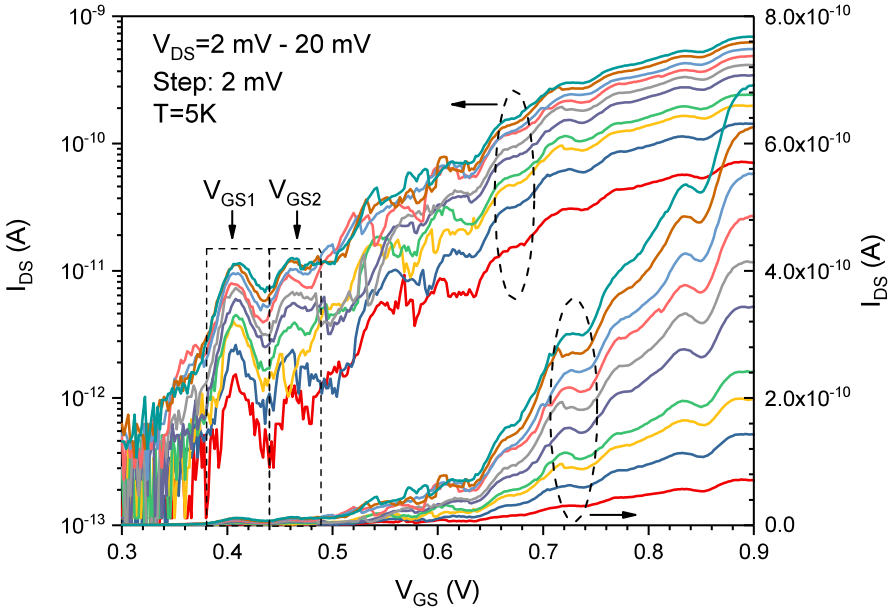


Figure 7.5: Low temperature I_{DS}-V_{GS} measurement results of Device B at 5K when V_{DS} is swept from 2 mV to 20 mV. Both linear and log scale plots are represented.

increasing of V_{GS}, two current peak envelopes with periodic V_{GS} spacing are observed at the device's sub-threshold region between 0.35 V to 0.5 V of V_{GS} and labelled with dashed boxes. The trend of the current peaks is similar under different V_{DS}, which indicates that the current features are real phenomenons. The reason of these current peaks is because the transport electrons are confined within the QD induced by dopants under top gate. Unlike the single dopant device, the QD is formed by clustered dopants coupled together closely. The selective doping region volume is around 50 nm × 40 nm × 40 nm and the doping concentration is around 5×10^{18} cm^{-3}. The calculated P-P donor distance with $N^{-1/3}$ is around 5 nm, which is smaller than the value of $2 \times r_B$ (r_B is the phosphorus Bohr radius, which is 3 nm). Therefore, the smaller P-P donor distance suggests that there is a great chance for dopants to be close and coupled together to form the clustered dopants QD at notch region. As the current peak envelop structure is consistent under different V_{DS}, it is possible that there is only one QD contributes electron transportation.

From the presence of the current peak envelop, the Coulomb stability diagram in Fig.7.6 is plotted to analyse the details of QD and electrons transport. The white lines present the Coulomb diamonds corresponding to the current peak envelopes as shown in Fig.7.5. The state 0 is the open diamond when the device operates at its off state. The next 1 and 2 states are the available states of QD. According to the position of current peak envelopes at two available states, the average gate voltage spacing ΔV_{GS} is 40 mV. Therefore, the corresponding gate capacitance is calculated from Eq.3.12 to be C_G = 3.56 aF. By applying the capacitance sphere model ($C = 4\pi\varepsilon_r\varepsilon_0 r$), the radius of the QD

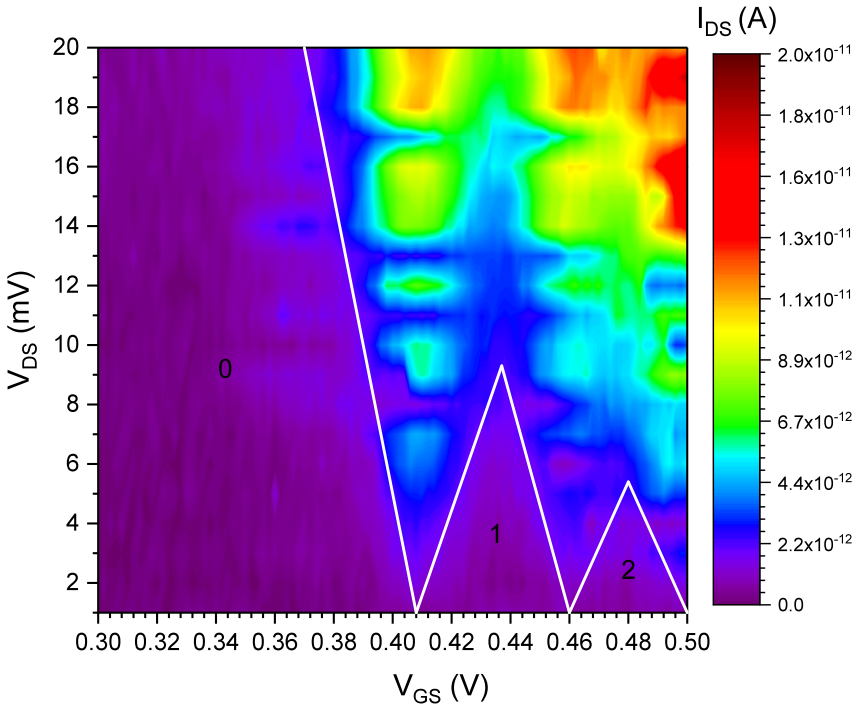


Figure 7.6: Low temperature Coulomb stability diagram of Device B at 5K.

is approximately 8.2 nm. The QD radius is significant larger than the Bohr radius of phosphorus donor in bulk silicon, which suggests that the QD has several phosphorus donors. From the slopes of current triangle boundaries from Coulomb diamonds, the values of C_D and C_S are extracted to be 9.85 aF and 8.87 aF separately. In theory, the value of C_D will be equal to the value of C_S for perfect symmetry device. However, the structures and doping conditions of the source and drain during fabrication process cannot be controlled to be exactly the same. The difference between the value of C_D and C_S shown above is due to the fabrication process but the small difference is acceptable. By comparing the slopes of two diamonds, the lack of variation of the slopes suggests that the source/drain bias-induced QD barrier modulation is not significant as the top gate in the device [71]. Regarding the capacitance values and the Coulomb stability diagram, the addition energy for single electron into the QD can be calculated to be 9 meV, which is presented to be the voltage spread along the V_{DS} direction of the diamond. According to the charging energy equation Eq.3.7, the charging energy E_C is calculated to be 7.2 meV. When the V_{GS} is over 0.5 V, the high diffusion current superimposes the fine features within the current envelopes. However, the current sub-peaks can be treated as a new energy level of single QD showing between the source/drain energy window. From the Fig.7.5, 4-5 sub-peaks could be obtained. Under different V_{DS}, the small features and sub-peaks within the peak envelopes embedded with the current envelopes with the increase of V_{GS}. This characteristics indicates that the transport energy window is wide enough to contain several energy levels [11]. The multi-fold energy levels is formed when atoms are coupled together and the number of split energy levels equals to the number of

interacted atoms [72]. From this observation, it is estimated that the QD is the dopants cluster with 4-5 dopants.

Based on the Coulomb stability diagram in Fig.7.6, the lever-arm factor α is calculated to be $\alpha = 0.125$ eV/V. With the gate voltage spacing $\Delta V_{GS} = 40$ mV, the energy separation ΔE between available states of QD can be calculated to be $\Delta E = 5$ meV. By comparing the ΔE with the energy separation of 12 meV between the ground state and the first excited state for phosphorus donor, the much smaller ΔE proves that the splitting of ground state levels and the QD is formed by closely coupled phosphorus donors. From the above analysis, each current peak envelops could be treated as different charge states of QD with one electron transport. At low V_{GS}, the QD is empty and the electron tunnels one-by-one through the QD from source to drain. With the increase of V_{GS}, the single electron is trapped within QD leading to the first current peak envelope. And the first confined electron occupies with the lowest energy level of QD. This occupied electron decreases the heigh of tunnelling barriers and the tunnelling rate increases. As a result, the current level of the second peak is higher than the first one. When the value of V_{GS} keeps increasing further, the second electron is trapped leading to the second current peak envelope. Although the shape of two current peak envelopes are nor exactly the same, the upper part of the envelopes are similar, which indicates that the two electrons remains on the same energy level of QD. Based on the above analysis, the current peak envelopes could be ascribed to electron tunnelling of the single QD induced by clustered phosphorus dopants.

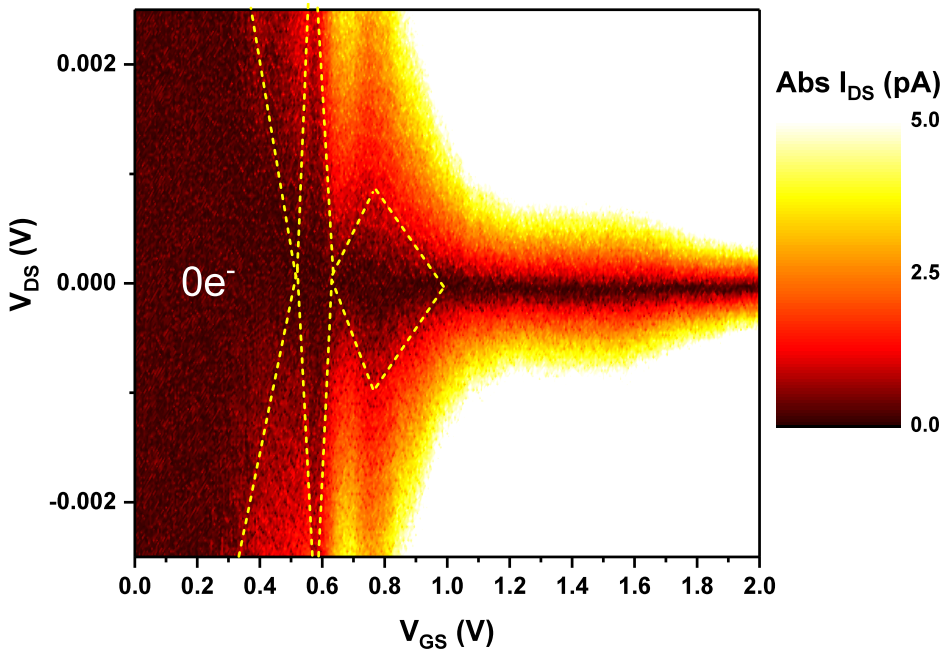


Figure 7.7: Low temperature Coulomb stability diagram measured at 5K showing two Coulomb diamonds. The absolute I_{DS} value s used to create the stability plot.

The duplicated device at different location on the chip is measured at JAIST for temperature dependent measurements. The measured device has the exactly same structure and fabrication processes on the same batch. The device is firstly measured at 5K with Agilent B1500 semiconductor analyser and low temperature probe station. The Coulomb stability diagram is shown in Fig.7.7. The V_{GS} is swept from 0 V to 2 V with 5 mV step and the V_{DS} is from -2.5 mV to 2.5 mV with 0.03 mV step. The Coulomb diamonds are labelled with dashed golden boundaries. The sate 0 represents the first open diamond. The device operates at the off region when V_{GS} is lower than 0.4 V. With the increase of V_{GS}, two Coulomb diamonds are observed at low V_{GS} region. The V_{GS} range of the corresponding current peaks are from approximately 0.5 V to 1 V. The range of the current peaks is similar to the range of Device B shown above in Fig.7.5. The ΔV_{GS} of two diamonds are 0.15 V and 0.3 V separately. The significant different shapes of diamonds are corresponding to different QDs. From the slopes of each diamond, the values for each QD's capacitance could be calculated to be 1.1 aF and 0.5 aF. Therefore, the radius of each QD is around 3 nm and 1.2 nm separately. The size of the first QD is just over the Bohr radius of phosphorus donor in bulk, which indicates there is a high possibility he first QD is formed by small number of dopants. However, the size of the second QD is quite small and the possible nature of the second QD is the randomly diffused single dopant in channel.

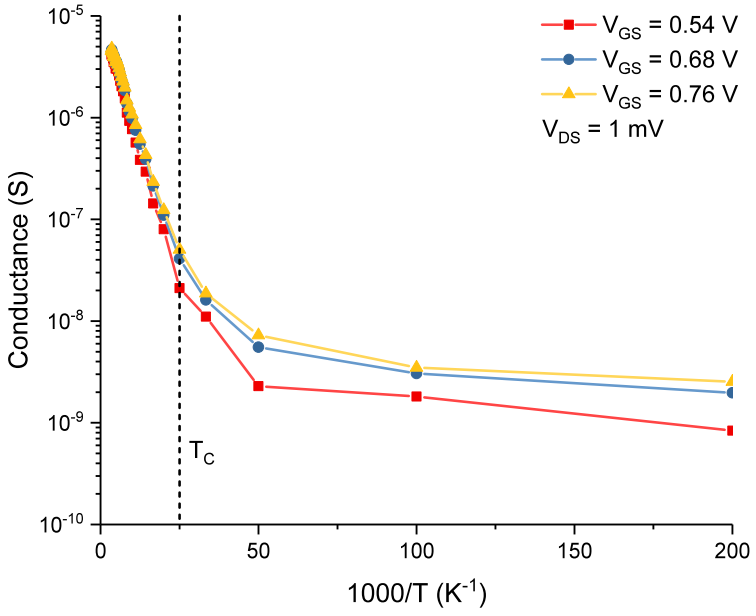


Figure 7.8: Measured conductance G as a function of 1000/T under different V_{GS} of the silicon notched nanowire device.

In order to further understand the electron transport mechanism, the Arrhenius plot is shown in Fig.7.8. The device is measured from 5K to 300K under different V_{GS} and the V_{DS} is kept at 1 mV. The values of V_{GS} are selected from the corresponding current

peaks in Fig.7.7. The general relationship of conductance G with temperature is [73]

$$G = G_0 exp(-\frac{T_0}{T})^v, \tag{7.6}$$

where the T_0 is the fitting parameter with the unit of Kelvin and the parameter v is the temperature coefficient that describes the types of temperature dependence. If v = 1, the electron transport is the nearest neighbour hopping. When v = 0.25, the transition belongs to the Mott variable range hopping and v = 0.5 means the Efros-Shklovskii variable range hopping (ES-VRH) could be applied to explain the electron transport. As shown in Fig.7.8, the conductance performs differently with the change of temperature and the electron transport changes from single electron tunnelling to the thermally activated transport separated by the critical temperature T_C. From the Arrhenius plot, the value of T_C is extracted to be around 50K. When the temperature is greater than T_C, the thermal activation will make electrons to transport through the potential wells created by QDs. And the conductance follows linear relationship with the temperature (1000/T), which indicates that the electron transport is dominated by nearest neighbour hopping. Therefore, the corresponding conductance relationship becomes [74]

$$G = G_0 exp(-E_a/k_B T), \tag{7.7}$$

where the k_B is the Boltzmann constant and the E_a is the activation energy. The value of E_a could be extracted from the slope of linear fitting at the nearest neighbour hopping region, which is calculated to be 9.46 meV. The activation energy E_a could be defined as [74]

$$E_a = (\frac{3}{4} g_0 \pi r^3)^{-1}, \tag{7.8}$$

the g_0 is the density of states within the hopping radius r. The value of radius r could be estimated to be the mean distance between phosphorous donors, $N^{-1/3}$ = 5.8 nm. From the above equation, the value of the density of states is calculated to be 1.17 × 10^{20} eV^{-1} cm^{-3}. This value will be used later to calculated the critical temperature.

For the region $T < T_C$, the conductance is weakly dependent with the change of temperature. By applying different parameters on the linear fitting curves, the relationship between conductance and temperature could be better fitted with Mott variable-range hopping. The variable range hoping mechanism indicates that the electrons transport between localised QDs. And according to the Mott variable range hopping model, the average hopping distance could be expressed as [74]

$$r_0 = (\frac{9\alpha}{8\pi g_0 k_B T})^{-1/4}, \tag{7.9}$$

where the parameter α is the localization length and its value could be estimated to be the same as the QD radius. By substituting the values of T_C = 50K and g_0, the calculated hopping distance is around 6.7 nm, which is approximately to be the distance between phosphorous donors of 5.8 nm from previous estimation. The electron transport transfers from thermally activated to Mott variable hopping separated by critical temperature. The critical temperature could be calculated by assuming the activation energy of variable range hopping equals to the Coulomb interaction energy [75]. The following equation could be then formed [74]

$$T_C = \frac{2.4e^4 a g_0}{k_B(4\pi\varepsilon_r\varepsilon_0)^2}. \tag{7.10}$$

Using the previous density of states and localization length, the value of T_C is calculated to be 57K, which is consistent with the value of critical temperature 50K extracted from Arrhenius plot.

In this chapter, the devices with improved fabrication process are measured and analysed. Through the measurement results, the new fabrication process is proven to have the potential to create the QD with clustered dopants. The consistent device's performance also indicates that the fabrication process is reliable. Both devices represent the quantum effects at low temperatures and both have two coulomb diamonds. Due to the variation of fabrication process, the second device shows the different electron transport mechanism, which transfers from the thermally activated transition to the Mott variable range hopping separated by temperature of 50K.

Chapter 8

Conclusion and Further Work

8.1 Conclusions

The reason of using the silicon as the quantum device platform is introduced at the beginning. The literature reviews about different silicon quantum devices with various fabrication processes and electrical characteristics are reviewed and compared, which provides inspirations of few dopants silicon device for our design. The following theory section provides the basic and fundamental understanding of the quantum device operations. The classic device characteristics and equations listed in this chapter are used for the device analysis in the later chapters. By reviewing the literatures for few dopants silicon NW-FETs, especially the work from Moraro and Tabe [38], the novel device structure with notched nanowire is developed to provide better potential confinement without sacrificing the current loss and complicating fabrication processes. Meanwhile, the methods of spin-on dopants and selective doping are used for forming the isolated QD with dopants.

The first generation of silicon NW-FETs device are fabricated with pure Ebeam lithography. The NW-FETs with different dimensions and doping situations are fabricated in parallel. In order to prove the reliability of the device design, the 2D device simulation are carried out by commercial software Silvaco. Through the simulation results, the device electrical characteristics are convinced with the classical MOSFET equations. Different Ebeam resists are applied during fabrication process and the unique dose test method is applied to find the best does for each resist. The critical nanowire is fabricated with 6% HSQ and RIE dry etch, which helps to achieve the nanowire with 100 nm $\times$ 100 nm. RTA method is applied for dopants diffusion with less lateral diffusion and better control. The device room temperature measurement results show standard MOSFET performance with various short-channel effects including DIBL and GIDL. Meanwhile, the device with different nanowire dimensions are compared with MOSFET equations. However, the device freeze-out issues found at low temperature measurements indicate

various design and fabrication issues like low doping concentration, shared contact pads design and high resistance source/drain contacts. All of these feedbacks are applied to improve the further batches.

Based on the feedbacks gathered as explained above, the second batch of silicon NW-FETs are fabricated. Instead of using Ebeam lithography of all device layers, the optical lithography is used to replace the alignment and contacts layers. The overall turnover time of fabrication is reduced with the VLSI compatible fabrication process, which also allows large scale of devices to be fabricated in parallel. New spin-on dopants source P509 is used for higher doping concentration with thermally diffusion process. Both numerical model and Silvaco are used to simulate the diffusion profile, which helps to determine the best drive-in time and lateral diffusion length. The device with and without central selective doping are compared for room and low temperature measurements. The device ON/OFF ration is around 10^4 - 10^5 and there is no gate leakage. The difference between threshold voltage indicates that the dopants are successfully introduced selectively under the top gate. And the concentration of central dopants is calculated to be 5×10^{18} cm^{-3}. The Coulomb blockade effect with two available states is successfully detected during the low temperature measurement at 5K. By analysing the Coulomb diamonds, the nature of the QD is from clustered phosphorous dopants closely coupled. The temperature dependent characteristics from duplicated device indicate the electron transport follows the transition from thermal activation to Mott variable range hopping separated by critical temperature at 50K. Meanwhile, two QDs are observed within the channel. By calculating the size of each QD, the radius of each QD are 3 nm and 1.2 nm. Therefore, the nature of these two QDs are concluded to be clustered dopants and randomly diffused single dopant. Although the details of QD system are different from these two measured devices, the consistent quantum effects and QDs observations indicate that the combinations of notched nanowire design and thermally diffused spin-on dopants could be applied for the few dopants quantum applications for the future study.

In this work, the few dopants silicon NW-FETs are designed for quantum application. The standardised fabrication process is developed during the project and the device performance proves that the spin-on dopants could be applied to form clustered few dopants QD with thermal diffusion. The additional potential confinement created by novel nanowire notch design helps the device to show quantum effects at low temperature without thinning down the device layer to sub-10 nm scale. During the low temperature measurements, the clustered dopants induced QDs are obtained successfully at 5K and the corresponding quantum effects are detected. Different electron transport mechanisms are analysed based on the characteristics of two devices, the first device follows the traditional single electron tunneling transport through QD and the electron transport mechanism for the second device transfers from thermally activated transition to Mott variable range hopping separated by temperature of 50K.

8.2 Further Work

The purpose of this project is to develop the silicon few dopants quantum FET and standardize the fabrication process for the future research. Besides the devices introduced above in the previous chapters, there are different future work could lead to further insights.

8.2.1 Device with chain of dopants

Prati *et al* [76] proposed a new type of few dopants silicon device for quantum application. Multiple QDs were created by chain of dopants localised in channel. The chain of dopants are introduced with precisely controlled ion implantation. Both the position and acceleration speed of ion implantation need to be chosen carefully. Within the same batch as previous devices, the special doping design is applied to introduce chain of dopants. Due to the lateral diffusion of dopants drive in process, the doping window could be put near the side of nanowire and the dopants will diffuse into nanowire. By controlling the distance between nanowire and doping window, the amount and profile of dopants within nanowire could be controlled precisely. The device design and the SEM image after doping window open after SiO_2 etch are shown in Fig.8.1.

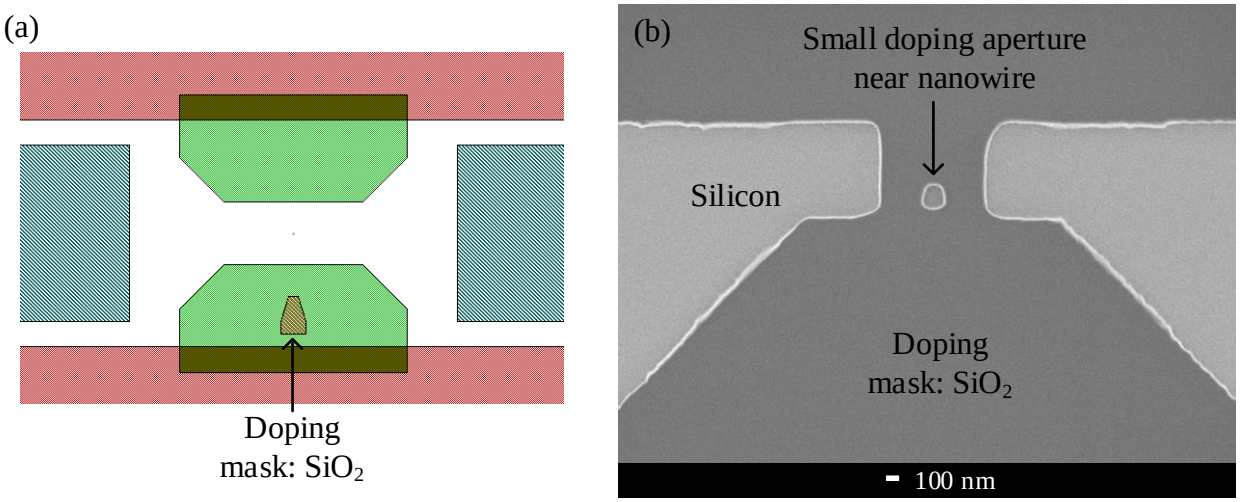


Figure 8.1: The device design is shown in (a). The SEM image after opening doping window is shown in (b). The small aperture is the doping window near the side of nanowire and the size of doping window is around 170 nm × 200 nm.

Different distances between doping window and nanowire are applied for measurement comparison. Meanwhile, the shallow shape design of the doping window is used for better doping profile control. This design turns the problematic side diffusion into a new method for creating the quantum FET with chain of dopants, which simplifies the fabrication process by comparing with the ion implantation method. The further

room and low temperature measurements are needed to analyse the nature of dopants in channel. And different devices with different distance need to be compared to find the best parameter for the quantum device application.

8.2.2 Fabrication process optimisation

The interface trapped charge between silicon and SiO_2 existed in current device has the effect on the device low temperature, which performs like the localized potential well for electron tunnelling at low temperature. The future fabrication process like forming gas annealing should be introduced at the end of fabrication to remove the interface charge. By reducing the density of interface trapped charge, both the device performance and fabrication yield could be improved. Meanwhile, the low temperature measurement could be more accurate and the characteristics of QD will be clear for observations.

Appendix A

Few dopants Silicon NW-FET fabrication process

Process	**Process details**
SOI substrate	100 nm silicon device layer and 200 nm BOX.
Sample preparation	
Sample clean	FNA/RCA1/RCA2 clean, 10 minutes in each step. RCA1/2 need to be heated to 60°C . 20:1 BHF dip for 1 minute to remove the native oxide.
Sample thinning	Dry oxidation at 1000°C for 2 hours 30 minutes.
Alignment marks formation	
S1813 coating	Dehydration at 120°C for 10 minutes. Spin S1813 at 5000 rpm for 30 seconds, followed by 115°C bake for 1 minute on hot plate.
Optical lithography	2.5 seconds exposure without filter.
Develop	Develop in MF319 for 45 seconds, followed by DI water rinse.
RIE dry etch	Four steps etch. (1) SiO_2 layer etch with Ar : CHF_3 (38:12) under 200 W RF for 7 minutes. (2) Silicon layer etch with O_2 : SF_6 (13.5:18) under 160 W RF for 30 seconds. (3) BOX etch with the same conditions as (1), but run for 13 minutes. (4) Substrate silicon etch with the same conditions as (2), but run 3 minutes.
Resist removal	Strip S1813 in heated 80°C NMP for 15 minutes, followed by 5 minutes Asher.

Doping windows definition	
Sample clean	10 minutes clean in FNA.
PMMA 950 A7 coating	Dehydration at 120°C for 10 minutes. Spin PMMA at 6000 rpm for 60 seconds, followed by 180°C bake for 90 seconds on hot plate.
Ebeam lithography	The dose of 1600/2200 $\mu C/cm^{-2}$ for coarse and fine beam is applied.
Develop	Developed in MIBK : IPA = 1:3 for 1 minute, followed by IPA rinse for 1 minute.
RIE dry etch	SiO_2 etch with Ar : CHF_3 (38:12) under 200 W RF for 7 minutes.
Resist removal	Strip PMMA in 80°C NMP, followed by 5 minutes Asher.
Doping with phosphorous	
Sample clean	10 minutes clean in FNA, followed by 200:1 BHF clean for 2 minutes.
Dopants diffusion	Dehydration at 120°C for 10 minutes. Spin P509 solution at 3000 rpm for 30 seconds. Leave the sample in desiccator for 1 hour. Thermal diffusion at 950°C for 15 minutes.
Sample clean	Dip in 20:1 BHF for 8 minutes to remove spin-on dopants and doping mask.
Nanowire definition	
Sample clean	10 minutes clean in FNA, followed by 20:1 BHF clean for 1 minute.
ZEP520A coating	Dehydration at 120°C for 10 minutes. Spin ZEP520A at 3370 rpm for 180 seconds with open lid, followed by 180°C bake for 3 minutes on hot plate.
Ebeam lithography	The dose of 250/190 $\mu C/cm^{-2}$ for coarse and fine beam is applied.
Develop	Developed in ZED-N50 for 2 minutes, followed by IPA rinse for 2 minutes.
RIE dry etch	Silicon etch with O_2 : SF_6 (36:36) under 100 W RF for 45 seconds.
Resist removal	The sample in cleaned with Asher for 15 minutes.
Gate oxide formation	
Sample clean	FNA/RCA1/RCA2 clean, 10 minutes in each step. RCA1/2 need to be heated to 60°C .20:1 BHF dip for 30 seconds to remove the native oxide.
Dry oxidation	Dry oxidation at 950°C for 5 - 8 minutes to form 10 nm SiO_2.
Source and drain contacts formation	

AZ2070 coating	Dehydration at 120°C for 10 minutes. HDMS evaporation for 15 minutes. Spin AZ2070 at 6000 rpm for 30 seconds, followed by 110°C bake for 1 minute on hot plate.
Optical lithography	Exposed for 5.5 seconds with 365 nm filter. Post bake at 110°C for 1 minute.
Develop	Developed in AZ2070 for 90 seconds.
Contact metallisation	Dip in 20:1 BHF for 30 seconds to open the contact windows. Dehydration at 120°C for 10 minutes. Over-night pump in Lab700. Deposit 20 nm/200 nm stack Ti/Al at rate 0.5/1 $\AA$/s and power 7%/25%. Lift-off in OptiWet with 40 psi. Clean in Acetone. RTA at 425°C for 2 minutes to form ohmic contacts.
Top gate contact formation	
PMMA 950 A7 coating	Dehydration at 120°C for 10 minutes. HDMS evaporation for 15 minutes. Spin PMMA at 6000 rpm for 60 seconds, followed by180°C bake for 90 seconds on hot plate.
Ebeam lithography	The dose of 1400/1700 μC/cm^{-2} for coarse and fine beam is applied.
Develop	Developed in MIBK : IPA = 1:3 for 1 minute, followed by IPA rinse for 1 minute.
Contact metallisation	Over-night pump in Lab700. Deposit 100 - 200 nm Al at rate 1 $\AA$/s and power 25%. Lift-off in OptiWet with 40 psi. Clean in Acetone.

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