Mathematical Model and Optimization of a Thin-Film Thermoelectric Generator

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April 2019

Abstract. The thriving of Internet of Things is set to increase the demands of low power wireless sensing devices. Thin-film thermoelectric generators are ideal as a sustainable power source for Internet of Things device, as they allow for low maintenance and energy autonomy. This work presents a model to estimate the performance of a thin-film thermoelectric generator. Verified by finite element method simulation, the results from the model show that by increasing interconnect electrical conductivity and reducing device pitch increases the power density. The power density can also be increased by increasing fill factor and reducing the thermal conductivity of insulating materials. A new corrugated thin-film thermoelectric generator design is proposed in this work that allows for higher fill factors compared to conventional square designs where a limit on the minimum feature size is imposed, as is the case with photo-lithography.

Keywords: Thin-film Thermoelectric, Mathematical modelling, FEM Simulation, Device Optimization, Fill factor

1. Introduction

With increasing interest in renewable energy and energy efficiency, direct thermal to electrical energy conversion via the thermoelectric Seebeck effect has gained significant interest [1–3]. These devices are constructed by connecting together both n and p-type thermoelectric material electrically in series and thermally in parallel. Once connected to a load, power will be generated by these devices that depends heavily on the material properties (Seebeck coefficient, thermal conductivity, and electrical conductivity) of the thermoelectric materials, but also on the device design.

The thriving of Internet-of-Things (IoT) increases the demand of low power sustainable power sources. Thermoelectric generators (TEGs) offer high reliability, long lifetimes, and low maintenance [4–10]. Particularly for thin-film TEGs the advantages are the reduction in the use of rare and costly elements by reducing the volume of thermoelectric material [11], and also their possible integration for on-chip cooling or energy harvesting [12]. The reason these devices are well suited for IoT devices is that a heat source could be available at all times, unlike solar energy that is only useful during the day. A lot of research has been going into increasing the figure of merit of thermoelectric materials [13–15], but material optimization does not necessarily lead to high performance devices. These devices must be well designed to minimize the effects of both thermal and electric parasitic resistances to maximize performance. However, device design is often a difficult task as there are many parameters to optimize and these optimizations depend on the application [16, 17]. The device performance can either be defied as the power output (or density) for a particular temperature difference, or by the conversion efficiency of the device. The importance of each depends on the application, for a fixed temperature system the power output will be more important and with a fixed heat flux system, the efficiency is a more useful parameter.

Device architecture is usually based on a conventional square design used for bulk TEG's [18–21]. However, using thin film fabrication methods a wide range of different designs are possible; for instance cylindrical thermoelements [10, 22], planar generators [23–26], and Y-type structures [27, 28].

One of the parameters that can have a significant effect on performance is the fill factor. Fill factor is defined as the ratio between the area of the thermoelectric material, and the area of the device. In a fixed heat flux system, such as in wearable technologies [29], it can be shown that there is an optimum fill factor for a maximum power density, especially where the thermal resistance of the heat source is quite high. In the case of a fixed temperature difference, such as harvesting from temperature controlled reservoirs/radiators, the power density will increase with increasing fill factor [6]. However, where the minimum feature size is limited by fabrication or lithography methods, a large filling factor may be challenging to achieve.

In this work, a new thermoelectric generator design, corrugated thin-film thermoelectric-generator (CTF-TEG), is evaluated. This architecture uses thermoelectric elements that are long and narrow (typically 1 mm x 10 μm) as opposed to the conventional checker-board design which has the length and width equal to each other. It will be shown that this design compared to the conventional thermoelectric device design has similar performance, however, the advantage of the design used here is the larger fill factors possible, which can improve power output and efficiency. Using mathematical modelling and finite element method (FEM) simulations, design parameters such as the fill factor, pitch, and choice of interconnecting material will be optimized for the highest power output and efficiency for a thin film device operating under a fixed temperature difference.

2. Methods

A diagram of the thermoelectric generator used in this paper is shown in figure 1. The n and p-type thermoelectric legs used are Bismuth Telluride (properties taken from the COMSOL material library [30]) and a perfect inverse match by negating the Seebeck coefficient to reduce the complexity in calculations. This still gives valid results as the expected change by using a material such as Antimony Telluride would be relatively minor. For the interconnecting metal TiN has been chosen for its high electrical conductivity, high resistance against corrosions, and its use as a barrier material. The exact material properties used are shown in Table 1.

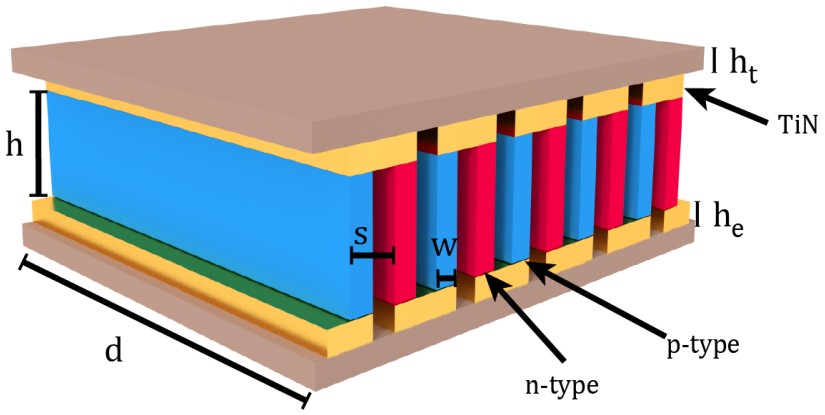

Figure 1. Diagram of the corrugated thin film thermoelectric generator (CTF-TEG) used in this paper.

The devices are 1 $mm \times 1$ mm in width and length, and height depends on optimization of legs but is usually between 5-20 μm. Unlike conventional devices the thermoelectric leg extends for the full 1 mm which leads to the fill factor being related to the pitch and leg width in a linear relation, rather than a squared relation. This gives a larger possible ranges of fill factors compared to conventional square devices. These benefits are particularly significant when a minimum limit for dimensions are used, as would be the case when fabricating these devices. Throughout this work, there is either air or silicon dioxide between the thermoelements. Air (or another extremely low thermal conductivity material) will give the best performance of the device. However, fabrication of suspended interconnects may not always be possible and so an insulating/supporting material of silicon dioxide is used in between the thermoelements. The design is similar to the design proposed in [31] which investigates a design using longer thermoelements but still having multiple rows of these longer elements, and their investigation is focused on a fabrication by folding the substrate. The investigation here is not limited to any particular fabrication method as long as the parameters investigated here are able to be tuned to the optimum values.

In this paper optimization of some of the parameters including pitch s, fill factor $Area_{\mathrm{TE}}/Area_{\mathrm{Device}} = w/s$, and interconnect conductivity σ_{IC} will be attempted using

Material	α ($\mu V/K$)	σ (S/m)	κ ($W/(m \cdot K)$)
Bi_2Te_3	-210	8.70×10^4	1.6
$\sim Bi_2Te_3$	210	8.70×10^4	1.6
TiN	-	1.25×10^6 [32]	3.80
SiO_2	-	-	1.2
Air	-	-	0.026

Table 1. Material properties used for FEM simulation and mathematical modelling. Properties shown are at 300 K all properties unless otherwise noted are from ref [30].

Parameter	s	FF	h	h_e	h_t	σ_{IC}
Range	1-1000 μm	0.05-0.95	1-9 μm	1 μm	0.5 μm	10^4-10^{10} S/m

Table 2. Ranges of the physical parameters explored in this paper.

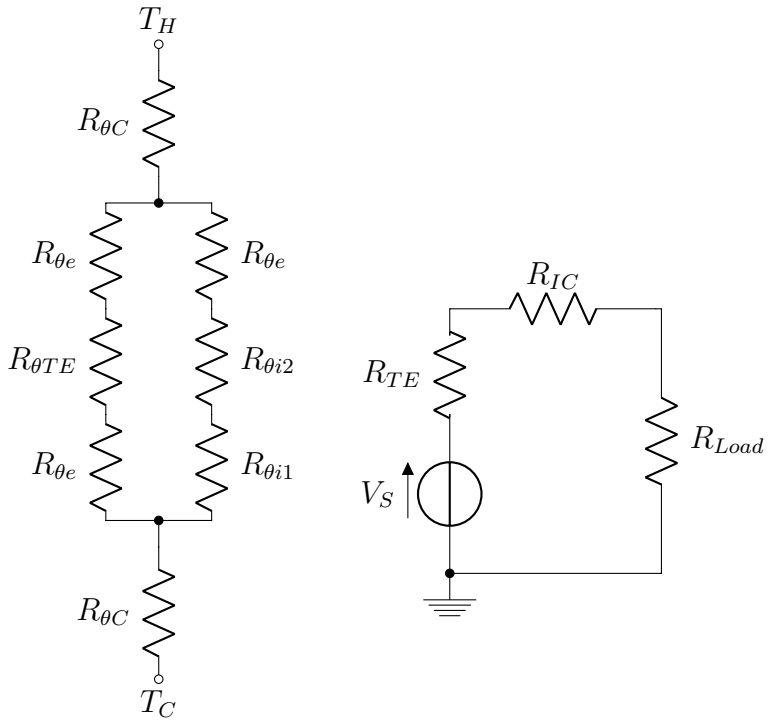

Figure 2. Equivalent Circuit of thermal and electrical resistances of a single thermocouple in the TEG device. Subscipt θ denotes a thermal resistance.

mathematical modelling and finite element method simulations.

2.1. Modelling

A simple model shown in figure 2, for the maximum power output from thermoelectric device including parasitic resistances is developed from a single thermocouple of

thermoelectric material with metal and thermal contacts on the top and bottom. Extended from a model from [33], this model assumes a constant temperature difference held across the device, and that the heat conduction is all in one dimension. This gives the power output as a function of both thermal resistances and electrical resistances of both the active material, insulating material, and the contacts.

$$P = \frac{N\alpha^2\Delta T^2}{(2R_{\theta \mathrm{C}}((2R_{\theta \mathrm{e}} + R_{\theta \mathrm{TE}})^{-1} + (R_{\theta \mathrm{e}} + R_{\theta \mathrm{i}1} + R_{\theta \mathrm{i}2})^{-1}) + 1)^2(2R_{\theta \mathrm{e}}R_{\theta \mathrm{TE}}^{-1} + 1)^2} \times \frac{1}{(R_{\mathrm{IC}} + R_{\mathrm{TE}})} \tag{1}$$

The power output shown in (1) is a function of the number of thermocouples, N, the Seebeck coefficient (assuming identical n and p material), α, temperature difference across the device, ΔT, the interconnect and thermoelectric electrical resistances, R_{IC} and R_{TE}, and the thermal resistances of the thermal contacts, electrical contacts, insulating material and thermoelectric legs, $R_{\theta \mathrm{C}}$, $R_{\theta \mathrm{e}}$, $R_{\theta \mathrm{i}}$, and $R_{\theta \mathrm{TE}}$ (all resistances have been defined in the supplementary material). This model (figure 2) then leads to the relationships between the power and leg length, area, and conductivities by explicitly writing the resistances in full.

$$\frac{P}{A} = \frac{\alpha^2\Delta T^2}{4\rho_{\mathrm{TE}}h}E_{\mathrm{elec}}E_{\mathrm{thermal}}, \tag{2}$$

$$E_{\mathrm{elec}} = \frac{FF}{(1 + (\sigma_{\mathrm{IC}}\rho_{\mathrm{TE}})^{-1}(1 - aFF)FFs^2(hh_e)^{-1})}, \tag{3}$$

$$E_{\mathrm{thermal}} = \left(\frac{2h_{\mathrm{t}}}{\kappa_{\mathrm{t}}}\left(\frac{FF}{2h_{\mathrm{e}}\kappa_{\mathrm{e}}^{-1} + h\kappa_{\mathrm{TE}}^{-1}} + \frac{(1 - FF)}{(h + h_{\mathrm{e}})\kappa_{\mathrm{i}}^{-1} + h_{\mathrm{e}}\kappa_{\mathrm{e}}^{-1}}\right) + 1\right)^{-2} \times \left(2\frac{h_{\mathrm{e}}\kappa_{\mathrm{TE}}}{h\kappa_{\mathrm{e}}} + 1\right)^{-2} \tag{4}$$

$$FF = \frac{w}{s} \tag{5}$$

Equation (2-4) show a more complete model for the power (P) per unit area (A) when the fill factor is defined using (5). Equations (3) and (4) show the models for the electrical and thermal power efficiencies (E_{elec} and E_{thermal}) respectively. Here the influence of the heights of the thermoelements, the electrical and thermal contacts ($h, h_{\mathrm{e}}, h_{\mathrm{t}}$); the thermal conductivity of the electrical and thermal contacts, the filling material, and the thermoelectric materials ($\kappa_{\mathrm{t}}, \kappa_{\mathrm{e}}, \kappa_{\mathrm{i}}, \kappa_{\mathrm{TE}}$); the fill factor FF; the conductivity of the interconnects and resistivity of the thermoelectric material ($\sigma_{\mathrm{IC}}, \rho_{\mathrm{TE}}$) are shown. The term a (in equation (3)) is used as a fitting parameter for this model. This is used to correct for the non-uniform current density through the interconnecting material and thermoelements. This current crowding causes the resistance to deviate from the standard formula for a resistor ($\rho l/A$, where l and A are length and cross sectional area). Simulations will then be used to compare the resistance of the interconnects to the calculated value of the resistance to find the function or value

represented by a. It can be seen that the value of a is roughly constant at higher interconnect conductivities, smaller interconnect heights (less than 3 μm) and higher fill factors, as shown in figure S2. As will be shown later in the paper these are the conditions for the higher power densities, so throughout the rest of the paper a will be treated as a constant value of 0.34.

2.2. Simulation

Simulations were carried out using COMSOL multiphysics, a finite element method of simulation. The device model used is the same as in figure 1. The models were set up so a fixed temperature difference of 20 K is held across the device giving a varying heat flux dependant on device parameters. The power output was extracted from the voltage across and current through a load resistor that was optimized to give a maximal power output using method of moving asymptotes optimization [34], a gradient based form of optimization. And the conversion efficiency was found by integrating the heat flux over the device area to give the total input thermal power. The full 1 $mm \times 1$ mm device was simulated so to include any edge effects in thermal gradients that would be present in a fabricated device. COMSOL simulations using the thermoelectric effect module will include both the Thomson effect and ohmic heating, which have been neglected in the mathematical model. In both the mathematical model and the simulations, the electrical and thermal contact resistances have been neglected. Therefore the mathematical model will be used herein as an estimation of the performance, and the simulations will be used to verify this model by comparing the results.

3. Results

3.1. Leg height optimisation

Leg height optimisation of these devices at a fixed temperature difference gives a similar trend than [33] as shown in figure 3. For a set of device and operating parameters, an optimum leg height for power output can be identified. This trend is caused by a balance of E_{elec} and E_{thermal}. As the leg height increases the thermal resistance of the thermoelement increases, causing a larger temperature difference across the thermoelement and therefore increases the power density. However, at the same time, as the leg height increases, this will increase resistance of the thermoelements, so the power density reduces. This then leads to there being an optimum point for the maximum power output. As the pitch increases, the maximum possible power density decreases, but also the optimum leg height increases as well. This is due to the change in relative values for both E_{elec} and E_{thermal}. For the rest of this paper a leg height of 4.5μm and a pitch of 10μm will be used unless otherwise mentioned.

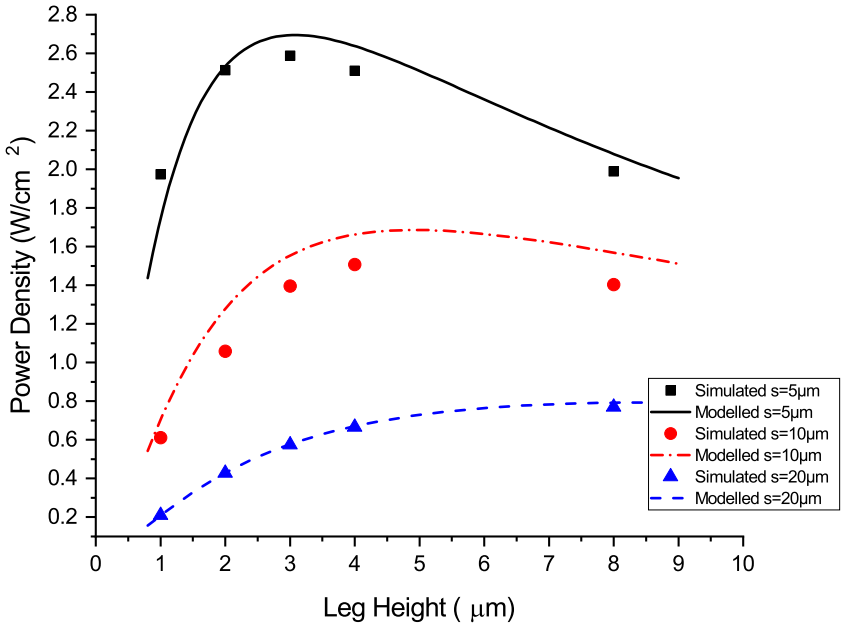

Figure 3. Power density with changing leg height for pitches of $5, 10$, and 20 μm. Device parameters: $FF = 0.75, h_{\mathrm{e}} = 1$ $\mu m, h_{\mathrm{t}} = 0.5$ μm.

3.2. Interconnect Conductivity

The interconnect resistance reduces the overall power density and efficiency. This parasitic resistance is much more prevalent in thin film devices as the thickness of the interconnects tend to be of the order of hundreds of nanometres. So then the resistance of these interconnects tends to be of a similar order to the resistance of the thermoelements. The impact of σ_{IC} on the power density depends mostly on the ratio between the interconnect resistance and the leg resistance. Fixing R_{TE} and changing R_{IC} by varying the electrical conductivity of the material leads to the relationship in figure 4. As conductivity increases and so R_{IC} decreases, the power density also increases, but this increase is not linear and the effects of the change in conductivity begin to significantly decrease after $\sigma = 1 \times 10^7$ S/m (roughly within 5% of the asymptotic value). This is due to the internal resistance then being dominated by the thermoelectric legs (i.e. $R_{\mathrm{TE}} >> R_{\mathrm{IC}}$).

The increase in fill factor shown in figure 4 increases the power density but does not affect the relationship with interconnect conductivity, agreeing well with the mathematical model presented in equations (2) to (4). The differences in the simulated data with the modelled data can be explained by the absence of the Thomson effect and ohmic heating (shown in the supplementary material). As interconnect conductivity is changed, both the resistance of the interconnects and the current through the device will change and therefore change the temperature difference across the thermoelements.

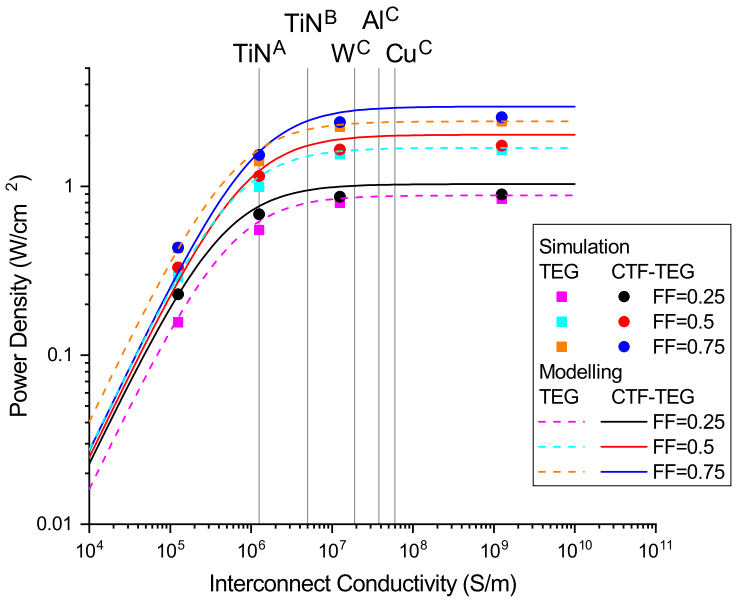

Figure 4. Power density of both a conventional square generator and the CTF-TEG design presented in this paper, and the dependence on interconnect conductivity and fill factor. Device parameters: $s = 10\ \mu m, h = 4.5\ \mu m, h_e = 1\ \mu m, h_t = 0.5\ \mu m$. Reference materials from A: [32] B: [35] C: [36]. The points show the simulation results and lines are the results from the mathematical model.

Figure 4 also shows some popular metallic materials as reference for the reader. Note however values for TiN^B, W, Al, and Cu are for bulk electrical conductivity and will be reduced when deposited as thin films (similar to TiN^A) modelled by desciptions such as Mayadas and Shatzkes resistivity model for polycrystalline films [37]. This model takes into account grain boundaries that are created by deposition of thin films, using the average mean free path and distance between grains.

Using a similar method to mathematically model the conventional square design of a thermoelectric generator leads to the same equation as in equation (2). The only difference is that the fill factor is defined as equation (6). So from the modelling we can conclude that for the same fill factor, the power density will be almost the same, except for w being different value for the same fill factor.

$$FF_{sq} = \frac{w^2}{s^2} \tag{6}$$

The difference between the two designs can be shown in figure 4, which shows the modelled and simulated power density of the two designs at different fill factors and interconnect conductivities. The results from the simulation show that generally the design presented in this paper gives a similar power density to the conventional square design. The real significance is that because of the definitions of the fill factors, for a fixed minimum dimension, the CTF-TEG design will always allow for a higher fill factor, leading to a higher power density. This difference in fill factor is much larger when the pitch is close to the minimum dimension limit.

3.3. Pitch

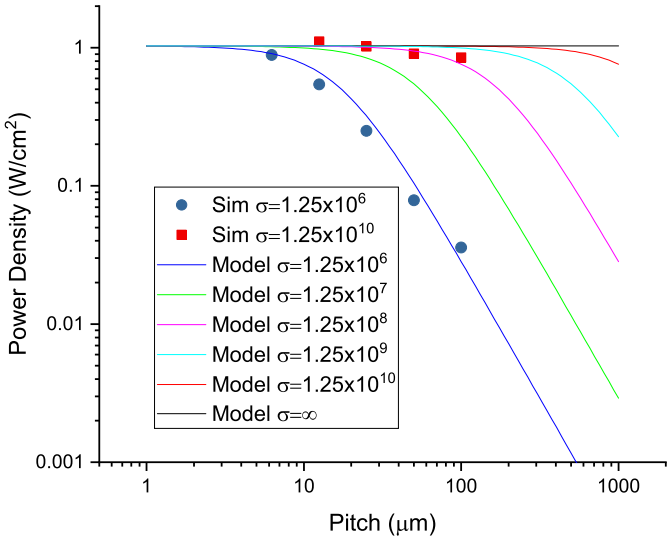

Figure 5. Power density using both simulation and mathematical modelling with pitch for devices with interconnect material of different electrical conductivities, using TiN as the baseline material. Device parameters: $FF = 0.25, h = 4.5\ \mu m, h_{\mathrm{e}} = 1\ \mu m, h_{\mathrm{t}} = 0.5\ \mu m$.

According to equation (3) it can be shown that the output power is roughly inversely proportional to the pitch squared, this is because as the pitch decreases, R_{IC} decreases as well, increasing E_{elec}. This prediction from the mathematical model is shown in figure 5 using thin film TiN ($\sigma = 1.25 \times 10^6\ S/m$) as the baseline interconnect material. To reduce the effects of pitch in fabricated devices, the interconnect material can be exchanged for one with a higher electrical conductivity, or alternatively h_{e} could be increased to reduce interconnect resistance. However, achieving such high interconnect conductivity and h_{e} is impractical, in particular in thin-film TEGs.

For devices with interconnect material of a finite electrical conductivity, reducing pitch improves power performance. This is because the effect of the parasitic interconnect resistance is less significant at smaller pitches. For thin film TiN of 1 μm, a pitch less than 10 μm significantly improves performance. Another advantage particularly for IoT applications is that for a smaller pitch, for a fixed device area, this increases the number of thermoelements, and therefore the voltage output.

3.4. Fill Factor

A theoretical prediction of how fill factor (FF) and thermal conductivity of the insulating material (κ_{i}) affects the maximum power density and percentage of Carnot efficiency (η/η_{c}) can be found using (2-5). The input thermal power is calculated by using the

thermal resistances in figure 2. These predictions in figure 6(a) show that for smaller pitches (10 μm), power density increases with FF but does not vary strongly with κ_{i}. This can be explained by the reduction in leg resistance by increasing cross-sectional area, changing the ratio between R_{IC} and R_{TE}. As well as some changes in interconnect resistance by changing the effective conducting length. With larger pitches, figure 6(b) (100 μm), the power density increases with FF but more significantly at lower FF with decreasing κ_{i}. This is because at smaller FF the decrease in κ_{i}, increases the temperature across the thermoelements more significantly.

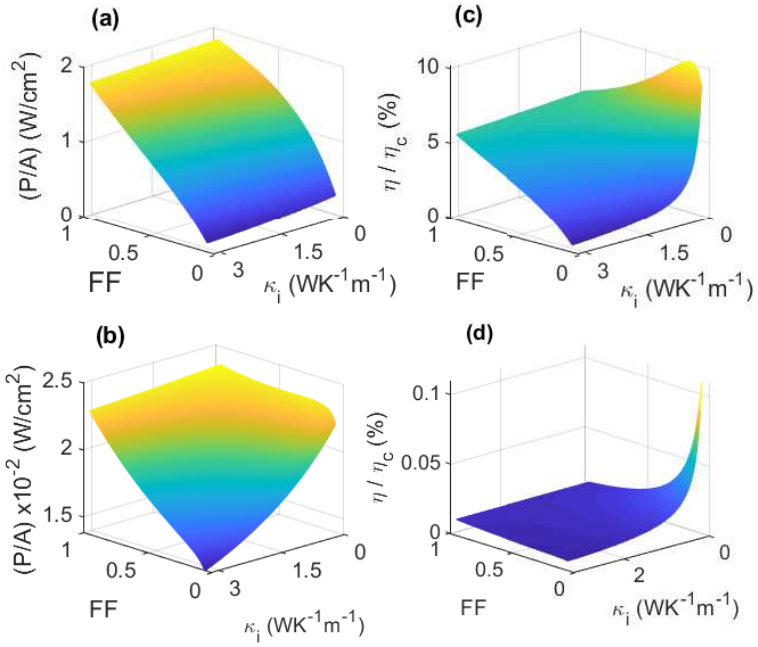

Figure 6. Power density (P/A) and percentage of Carnot efficiency (η/η_{c}) with Fill Factor and thermal conductivity of insulating material (κ_{i}) for TEG device with pitch of 10 μm (a & c) and 100 μm (b & d).

For smaller pitches (10 μm) the thermal efficiency increases with FF at higher values of κ_{i}, but transitions to a regime where decreasing FF increases efficiency when κ_{i} is lower than $\kappa_{\mathrm{TE}} = 1.6\ W/(m \cdot K)$ as shown in figure 6(c).The change in the trends of efficiency with different κ_{i} can be explained by the change in thermal resistance in the filling material. With a lower κ_{i} the efficiency increases with lower fill factor, because the overall device thermal resistance is higher and so the thermal power input reduces for a fixed temperature difference. With higher κ_{i} the efficiency increases with fill factor, this is because the overall device thermal resistance is not changed much as it is similar to the thermal conductivity of the thermoelectric material. So because the power density increases with increasing fill factor, this increases the efficiency. For larger pitches (100 μm), shown in figure 6(d) the thermal efficiency has a similar trend, where it increases with high values of κ_{i} and decreases when this is lower than κ_{TE}. The differences between (c) and (d) for low FF and κ_{i} can be explained by the very low thermal resistance, leading

to a much smaller thermal power input and therefore increasing efficiency much more. Notice also that the power density and thermal efficiency decrease with increasing pitch, as the parasitic interconnect resistance becomes larger and therefore so do the losses.

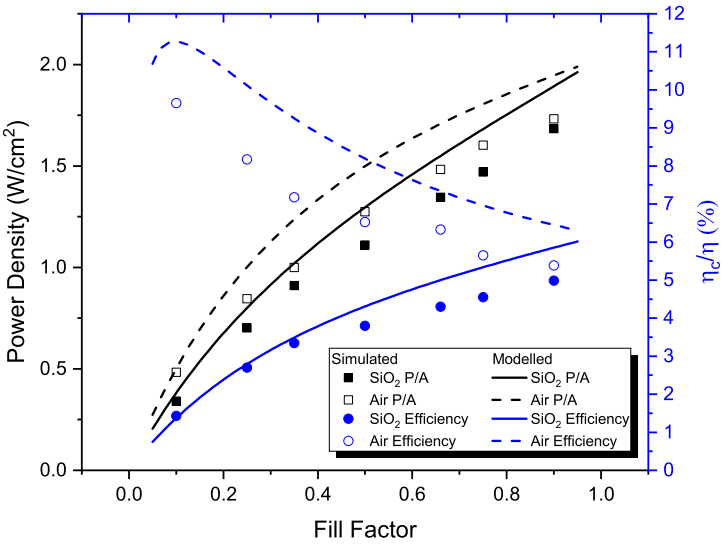

Figure 7. Power density (P/A) and percentage of Carnot efficiency (η/η_c) with Fill Factor for device with poly-crystalline SiO_2 and air as filling material. Simulated device has pitch of 10 μm and thermoelement height of 4.5 μm

Simulations using poly-crystalline SiO_2, ($\kappa = 1.2\ W/(m \cdot K)$) and air ($\kappa = 0.026\ W/(m \cdot K)$) [30] as filling materials shows these trends in figure 7. These simulation results are used to validate the accuracy of the mathematical modelling results shown in figure 6. There is some error between the mathematical model and the simulations which is due to the simulation including both the Thomson effect and ohmic heating, and also these simulations can more accurately calculate the conduction path through the device, where in the model a correction factor is used. However, the trends of the mathematical model is very similar to the simulated results with a maximum discrepancy between the simulated and calculated power density of $\approx 15\%$. This suggests the model is a useful tool to quickly evaluate chosen design parameters for devices.

This model could be improved by including boundary thermal resistance [25], electrical contact resistance [38, 39], the Thomson effect [40], and ohmic heating [41]. Another aspect that has been neglected here is the thermal exchange between the device and the heat source, to model this an exact application would have to be decided on and so this has been simplified for any application that could provide a fixed temperature difference at the device level. For this to be included a more complex thermal resistance network would have to used, such as in [41–43].

4. Conclusion

In this work a CTF-TEG has been modelled and optimized for increased power density and efficiency. We found that for a fixed temperature difference, decreasing the ratio between interconnect resistance and the resistance of the thermoelements decreases the losses. Reducing the pitch of the device thermocouples increases the power density by reducing the interconnect resistance and increasing voltage output. And that increasing fill factor will increase power density for the devices modelled, but depending on the fill material, efficiency will either decrease if the filling materials thermal conductivity is less than that of the thermoelements, or increase if this is larger. As this design allows for a larger fill factor compared to the conventional design especially at smaller pitches, a significant increase in power density can be achieved by using this design.

The model provides an easy method for evaluating the performance of a thin-film TEG. It has been shown that the model follows the trends for power density with a discrepancy of $\approx 15\%$. This model could be improved by incorporating both the Thomson effect and Ohmic heating.

Acknowledgments

Daniel Newbrook would like to thank both BAE and EPSRC for funding the iCASE studentship. The authors would also like to acknowledge the use of the IRIDIS High Performance Computing Facility at the University of Southampton.

The authors also acknowledge project STFC reference ST/P00007X/1, and the ADEPT project EPSRC reference EP/N035437/1.

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