University of Southampton

Faculty of Engineering and Physical Sciences

Optoelectronics Research Centre

GeSi Franz-Keldysh Modulator for Silicon Photonic Integrated Circuits

by

Lorenzo Mastronardi

Thesis for the degree of Doctor of Philosophy

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Abstract

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The growing of Internet has driven recent development of Silicon Photonics in the attempt of coping with the unceasing demand of bandwidth at cheap cost; datacentres with large footprint and enormous computational performances are deployed every year with a rate that, by 2021, will represent the 53% of the total count of installed servers. An ambitious yet necessary objective is envisioned by 2030, link speed above 1 Tb/s allowing sophisticated web-services to grow and reach users worldwide. Offering a fast, power efficient and easy to produce, integrated optic modulator working in the C and L band of the communication spectrum for datacentre applications, this thesis presents an innovative Franz-Keldysh based modulator, integrated in a rib waveguide on the 800 nm platform and fully CMOS compatible. The novelties of this design are found in the thick platform, which permits better optical confinement, and the wrap-around junction design that enables definition of wide rib while keeping strong electric field distribution in the active portion of the rib.

Starting from a blank canvas, this project benefited from simulation study, process development and fabrication run. A simulation platform was, in fact, built to estimate electro-optic performances of design variations and define process recipes; the design reference was, then, translated in a set of masks used in the fabrication run. As a result, a

device with cutting edge performances was realised, measuring dynamic extinction ratio of 5.2 dB at 56 Gbps with 3dB bandwidth of 56 GHz. Scattering parameters measurements also permitted to evaluate a power consumption of 44 fJ/bit, confirming the exceptional electro-optical efficiency of the design. A side study investigating material engineering by means of rapid thermal annealing to tune the device absorption spectrum, that together with the possibility of customising the device design, permits to expand the operation bandwidth while supporting either the transverse electric or transverse magnetic polarisation, is also presented.

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Academic Thesis: Declaration Of Authorship

I, Lorenzo Mastronardi

declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

GeSi Franz-Keldysh Modulator for Silicon Photonic Integrated Circuits

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
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First Author Journal Paper

- L. Mastronardi, M. Banakar, A.Z. Khokhar, N. Hattasan, T. Rutirawut, T. Domínguez Bucio, K. M. Grabska, C. Littlejohns, A. Bazin, G. Mashanovich, and F.Y. Gardes, "High-speed Si/GeSi hetero-structure Electro Absorption Modulator," Opt. Express 26, 6663-6673 (2018).

Co-author Journal Paper

- K. Debnath, D. J. Thomson, W. Zhang, A. Z. Khokhar, C. Littlejohns, J. Byers, L. Mastronardi, M. K. Husain, K. Ibukuro, F. Y. Gardes, G. T. Reed, and S. Saito, "All-silicon carrier accumulation modulator based on a lateral metal-oxide-semiconductor capacitor," Photon. Res. 6, 373-379 (2018).

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Conference Paper

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Previous Publication un-related to this Work

- C. E. Campanella, L. Mastronardi, F. De Leonardis, P. Malara, G. Gagliardi, and V. M. N. Passaro, "Investigation of refractive index sensing based on Fano resonance in fiber Bragg grating ring resonators," Opt. Express 23, 14301-14313 (2015).
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Signed:

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Date:

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Definitions and Abbreviations

- AC - Alternate Current
- AFM – Atomic Force Microscope
- ASK - Amplitude-Shift-Key
- BER - Bit Error Rate
- BH - Bottom Half
- BOX - Buried Oxide
- CAGR - Compound Annual Growth Rate
- CB - Conduction Band
- CDR - Clock and Data Recovery
- CEI - Common Electrical (I/O)
- CG – Grating Coupler
- CMOS - Complementary Metal Oxide Semiconductor
- CMP - Chemical Mechanical Polishing
- CW - Continuous Wave
- CWDM - Coarse Wavelength Division Multiplexing
- DC - Direct Current
- DCA - Digital Communication Analyser
- DPSK - Differential- Phase-Shift-Key
- DUT - Device Under Test
- E - Electric Field
- EAM - Electro Absorption Modulator
- EOM - Electro-Optic Modulator
- ER - Extinction Ratio
- ER-Dyn - Dynamic ER
- FDM - Finite Difference Method
- FDTD - Finite Difference Time Domain method
- FIB - Focused Ion Beam
- FKE - Franz-Keldysh Effect

- FOM - Figure Of Merit
- FSK - Frequency-Shift-Key
- GB - Giga Byte
- Gbps - Giga bit per second
- GC - Grating Coupler
- GDP - Gross Domestic Product
- GS - Ground Signal
- H - Magnetic Field
- HAADF - High Angle Annular Dark Field
- IC Layout - Integrated Circuit layout
- ICP - Inductively Coupled Plasma
- IL - Insertion Loss
- IPA - IsoPropyl Alcohol
- IR - Infrared
- IV - Current Voltage
- KE - Kerr Effect
- LASER - Light Amplification by Stimulated Emission Of Radiation
- LED - Light Emitting Diode
- MBE - Molecular Beam Epitaxy
- MCSMF - Multi Core Single Mode optic Fibres
- MMF - Multi Mode optic Fibres
- MMI - Multi Mode Interference coupler
- MOS - Metal Oxide Semiconductor
- MZI - Mach-Zehnder Interferometer
- M-QAM - M-Quadrature Amplitude Modulation
- NCUS - Nanofabrication Centre of the University of Southampton
- NRZ - Non-Return to Zero
- OEIC - Opto-Electronic Integrated Circuit
- OIF - Optical Internetworking Forum
- OOK - On Off Key
- PAM-x - Pulse Amplitude Modulation-x
- PDE - Plasma Dispersion Effect
- PE - Pockels Effect
- PEDT - Precession Electron Diffraction Technique
- PECVD - Plasma Enhanced Vapour Deposition

- PML - Perfectly matched layer
- PoE - photoelectric effect
- PIN - Acceptor Intrinsic Donor
- PM-SMF - Polarisation maintaining Single Mode optic Fibre
- PRBS - Pseudo Random Binary Sequence
- PSK – Phase Shift Key
- QC - Quantum Confinement
- QCSE - Quantum Confined Stark Effect
- QPSK - Quadrature Phase Shift Key
- QW - Quantum Well
- RF - Radio Frequency
- RMS - Root Mean Square
- RPCVD - Reduced Pressure Chemical Vapour Deposition
- RSA - Rack Scale Architecture
- RTA - Rapid Thermal Annealing
- SC-x - Standard Clean-x
- SDM - Spatial Division Multiplexing
- SEM - Scanning Electron Microscopy
- SER - SerDes (Serialiser)
- SHR - Shockley Hall Read recombination
- SIMS - Secondary Ion Mass Spectrometry
- SMF - Single Mode optic Fibre
- SOI - Silicon On Insulator
- STEM - Scanning Transmission Electron Microscopy
- TCAD - Technology Computer-Aided Design
- TDD - Threading Dislocation Density
- TE - Transverse Electric
- TH - Top Half
- TIA - Trans Impedance amplifier
- TIR - Total Internal Reflection
- TM - Transverse Magnetic
- TOR - Top of Rack
- TPA - Two-Photons Absorption
- UV - Ultra Violet light
- UHVCVD - Ultra High Vacuum CVD

- VIA - Vertical Interconnect Access
- VB - Valence Band
- VCSEL - Vertical Cavity Surface Emitting Laser
- WDM - wavelength Division Multiplexing

Chemicals

- As - Arsenic
- Ar - Argon
- B - Boron
- AsH_3 - Arsine
- B_2H_6 - Diborane
- BF_2 - Difluoroboryl
- CF_4 - Tetrafluoroethane
- C_2F_6 - Hexafluoroethane
- C_4F_8 - Octafluorocyclobutane, or Perfluorocyclobutane
- CHF_3 - Fluoroform
- HCl - Hydrochloric acid
- HF - Hydrofluoric acid
- H_2O_2 - Hydrogen peroxide
- IBGe - Iso-Butyl Germane
- N_2 - Nitrogen gas
- N_2O - Nitrogen Oxide
- NH_3 - Ammonia
- Ge - Germanium
- $GeCl_4$ - Germanium Chloride
- GeH_4 - Germane
- GeO_2 - Germanium Oxide
- GeNi - Germanide
- GeSi - Germanium Silicon
- SF_6 - Sulfur Hexafluoride
- Si - Silicon
- SiH_4 - Silane
- SiO_2 - Silicon dioxide
- SiOH - Silanol

- O_2 - Oxygen
- P - Phosphorus
- PH_3 - Phosphine
- TiN - Nitinol

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Chapter 1

Introduction

Light applications surround every human activity from luminaire to advanced science, deeply affecting modern society. Globally, photonics represents about the 13% of the Gross Domestic Product (GDP), registering a Compound Annual Growth Rate (CAGR) of 5.8% circa per year in the last 6 years, with an estimated growth of 6.6% for the 2018 [1], counting ~3300 companies spread in 52 countries (Figure 1-1).

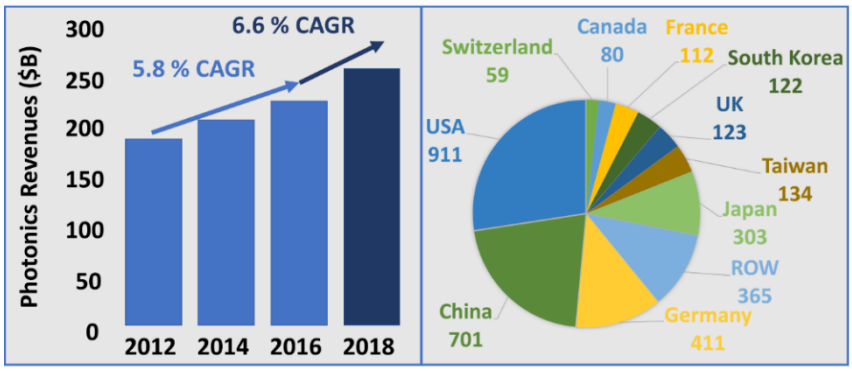

Figure 1-1 (left) Photonics revenue CAGR%, (right) Photonics company count by country [1].

The photonics market, divided in 10 areas from lighting to defence, is big and diverse [2]; in Figure 1-2, the CAGR rate of different sectors gives a comprehensive insight. The communication sector, accounting for 8% CAGR, is driven by communication growth in the east, web-based applications and especially datacentres, hence thrusting Opto-Electronic Integrated Circuits development for photonic transceivers.

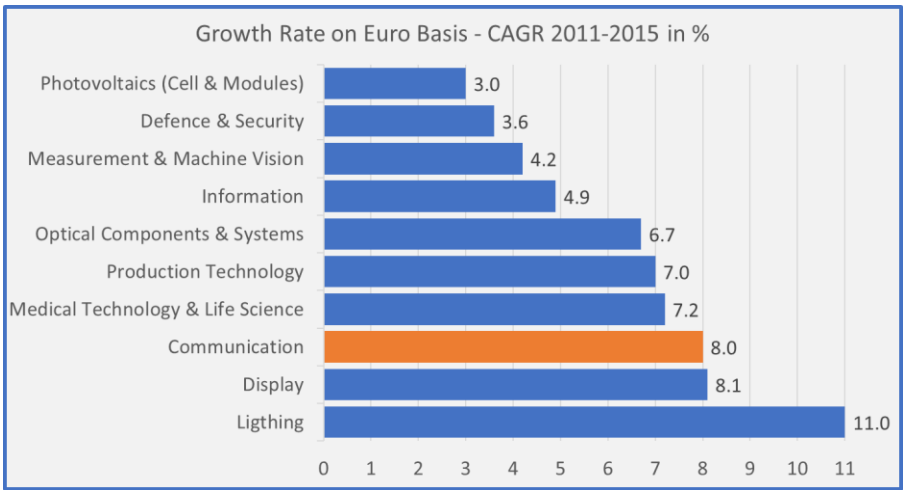

Figure 1-2 Photonics market Global growth rate in Euro, CAGR% [2] divided in ten areas. In orange the Communication sector growth, mostly affected by datacentre development.

The advent of Opto-Electronic Integrated Circuit (OEIC) in the silicon platform can be dated to mid-1980 [3] when Soref and Lorenzo [4] presented the very first optical component integrated in silicon, working at $\lambda = 1.3$ μm and 1.6 μm, giving birth to a new field of research that in few years attracted industries (INTEL, Luxtera, IBM), research institutes and governments (AFOSR, DARPA, etc.). The breakthrough in 1986, when the first active device [5] was presented, envisioning the possibility of replacing copper and electrons with waveguides and light.

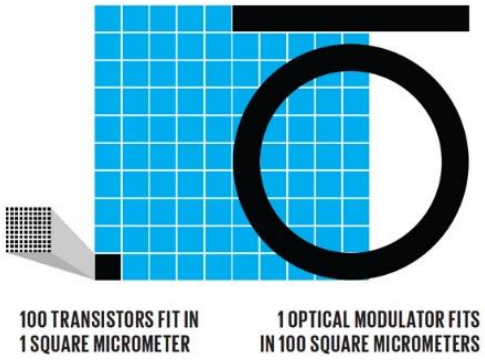

Figure 1-3 Footprint comparison between transistors and optic ring resonator modulator, demonstrating that in-chip optic transmission is not practical with current technologies, reproduction from reference [6].

Unfortunately, the replacement of transistors with photonic circuits has not yet happened due to limitation of current technology in miniaturising optical devices, the footprint drawback is qualitatively depicted in Figure 1-3 where a ring resonator occupies the same space of ten thousand transistors; such big difference reduces possibility for photonic devices to replace critical computer components, like CPU, memory controller, etc. Silicon photonics [7], however, by exploiting the very same knowledge, tools and process used to fabricate modern sophisticated electronic chips in CMOS facilities, has the

potential to reduce the cost and scale up volume data transmission in datacentre environment.

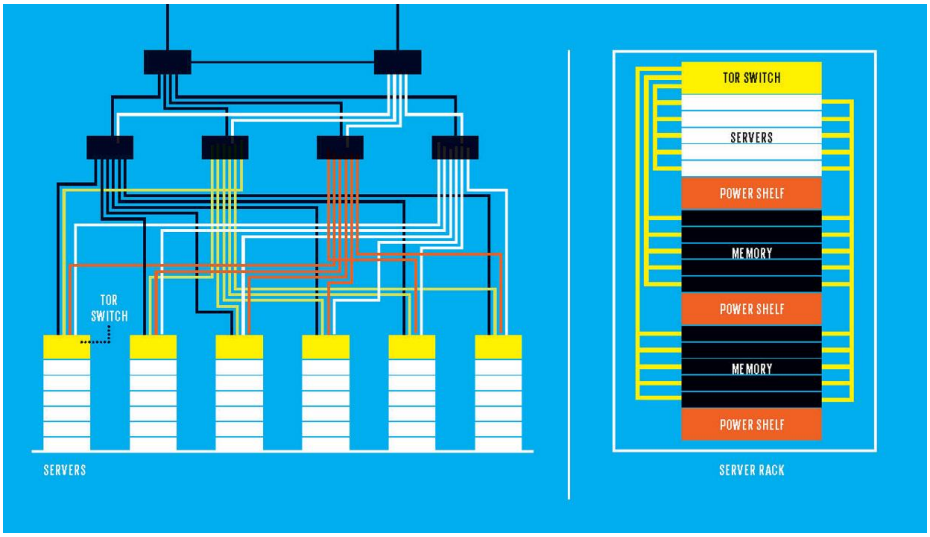

Figure 1-4 Standard datacentre topology, from the internet link (top), data is routed via optic fibres to the servers (yellow-white). On the right the Rack Scale Architecture provides distributed server architecture by optically connecting computers to memory, reproduction from reference [6].

In datacentres (Figure 1-4), optical links route data from the Internet (top) to blade servers (white blocks), an aggregate system of components (processors, memory, storage) hosted in a rack chassis, representing the datacentre core. If multi-terabit-per-second optical interconnects are available, a distributed server architecture whose components can be placed within the same rack or in different racks (Figure 1-4 right), is possible. This Rack Scale Architecture (RSA) can offer better use of computing resources [6] by assigning dynamically components such as CPU, memory, power supply to the task by the operator using a software [8], providing a flexible computational power for different needs. These architecture is also thought to simplify the replacement and update of hardware to cope with an increasing computational demand over time [6].

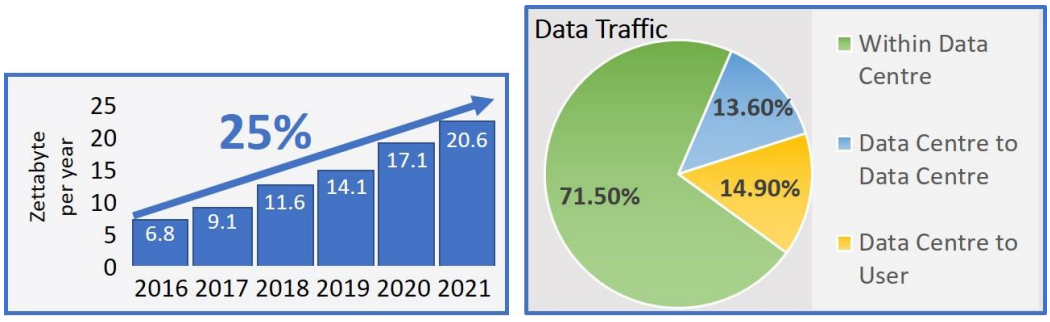

Figure 1-5 Cisco Global Datacentre IP growth Prediction (left) and Data traffic ratios (right) [9].

Optical interconnects are vital for connecting datacentre servers too, with an expected global datacentre IP traffic exceeding 20 Zettabyte by 2021 [9] (left graph of Figure 1-5) and the majority of the traffic generated within datacentres (right pie chart of

Figure 1-5), link speed up to 1.6 Tb/s will be necessary in the next few years, as envisioned by the Ethernet Alliance roadmap (Figure 1-6) [10], although no details have been given regarding the technology to be used.

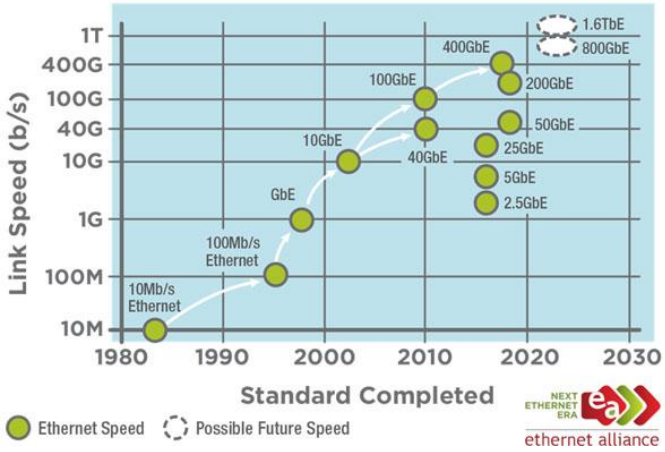

Figure 1-6 Ethernet Alliance's roadmap for the Terabit Ethernet, reproduction from reference [10].

Finally, as the number of distributed datacentres (hyperscale datacentres, occupying superficies over 1000 m^2) is estimated to reach 628 by 2021 representing the 53% of the global amount of installed servers [9], distances between servers are destined to get over 300 m, making optical interconnects crucial to assure low latency and fast connections for services that span from finance to gaming and wireless communication (5G) [11].

Photonics research groups are currently tackling three limiting factors for silicon photonics to be widely adopted: lack of monolithically integrated coherent light sources (LASER), weak electro-optic effects on Si and packaging costs. Having an indirect bandgap, silicon is in fact a poor emitter. Different approaches have been proposed to enhance emitting effects on silicon, among those nanocrystals [12] demonstrated to be a viable solution, although work still needs to be done to reach performances comparable to those of the III-V counterparts. Big improvements have been made in integrating III-V materials and devices on silicon wafers by using wafer bonding technique [13][14][15], giving the opportunity of designing a full photonic transceiver in the silicon platform. Wafer bonding is a simple technique for integrating III-V material on Si to realise transmitters with improved efficiency [16] and photodiodes operating at 1.55 μm with low dark current [17]. Limits of this technology are found in the crystalline quality and the limited size of the available commercial wafers. Direct III-V epitaxial growth on Silicon On Insulator (SOI) [18][19][20][21][22][23], can overcome the yield deficiency of wafer bonding by allowing integration of III-V directly on SOI wafers with any dimension, improving scalability and reducing costs [24]. Works on reducing treading dislocations,

microcracks and all sort of nonradiative recombination centres [19] to improve efficiency, needs to be tackled. Transceivers, however, require efficient modulators, that is why countless studies [25][26][27] tackling the improvement of electro-optic effect on Si are found in literature. Costs can be dramatically reduced by ultra-dense integration (submicrometric footprint) [28], which is achievable if efficient light sources and modulators are made available on a silicon substrate, improving the yield and reducing the power and thermal budget.

This project by exploiting the electro-absorption effect in a germanium silicon alloy [29], proposes for the first time a modulator realised with a vertical PIN structure integrated in a rib waveguide to achieve rib width independency of the modulation efficiency, better optic confinement and support for both polarisations. This device also provides almost twice the speed in Gbps and 3dB bandwidth with a third of power consumption of similar designs developed in GeSi [30], making it comparable to devices developed in Ge [31].

1.1 Thesis outline

The thesis is divided in eight chapters:

- The first chapter briefly introduces the birth of silicon photonics and the economic reasons of its development.
- The goal of the second chapter is to compare advantages and disadvantages of principal CMOS compatible group IV optic modulators; for this purpose, material characteristics are briefly introduced and compared. In the second part of the chapter, the optic communication link is widely shown starting from the transceiver diagram and concluding with the optic channel requirement for the short-range C-band communication system. The core parts of this chapter are the modulation strategies in group-IV materials and relative modulation structures; theory behind and schemes adopted in different kind of implementation are given to support choices that led to development of a Franz-Keldysh optic modulator.
- The third chapter investigates optic modulators found in literature that belong to the modulation strategies adopted for silicon, germanium and GeSi platforms, presented in chapter two. Tables are used to easily compare DC, high-speed and power consumption performances of different devices; in the last table, belonging to the Franz-Keldysh effect-based modulators, performances of the modulator developed and realised for this project are included to have direct comparison with literature.
- Chapter four presents methods applied in this work, from computer-aided software to fabrication and characterisation tools; this chapter delves into the techniques used for simulating designs, choosing the reference design and drawing fabrication masks. Then, fabrication and characterisation techniques are presented in detail.
- The fifth chapter investigates capabilities of the informatic platform realised for this project. From the mathematical model of Franz-Keldysh effect to the electro-optic simulations for DC and high-speed signals, this chapter includes simulation results that yielded to the device design reference chosen for the first fabrication run. In the first part, the mathematical model is examined and validated by comparing results taken from literature, then the simulation platform is examined with charts and examples to better understand the concept behind it; a case study is proposed to validate its accuracy. Following of the chapter, instead, three simulation sets are presented; in the first set, device characteristics such as junction shape and doping concentration are investigated, then simulations to determine the

doping recipes and finally, DC and high-speed performances of devices simulated with a process approach are used to select the design reference. Effect of the Ge buffer layer to the spectral efficiency is discussed, further. Following the active device simulations, transmission and coupling efficiencies are simulated on passive devices to define grating coupler, taper designs and evaluate losses due to different material etch rates and angled interfaces. In the last part of the chapter, the process mask layout is presented.

- Chapter six gives results from a side study on a 500 nm SOI platform investigating an annealing technique to tailor the GeSi direct bandgap for modifying the operation wavelength regime of devices based on the Franz-Keldysh Effect and reduce the propagation losses.
- The seventh chapter, by focusing on the realised device, represents the outcome of the work previously examined. The process is fully described, then electric and optic characterisation in both DC and high-speed are presented for devices realised in the first fabrication run. The chapter concludes with simulation fitting of the device DC performances.
- Chapter eight summarises this work and opens discussion for future work.

Chapter 2

Theoretical Backgrounds

The exponential growth of users and web-services worldwide demands the implementation of fast, reliable and cost-effective transceivers. In the last decades, integrated silicon and multilayer [32][33] based systems, including high speed photodetectors [34][35], wavelength division multiplexing (WDM) filters [36] and electro-optic modulators [37] have been developed with the objective of realising optical interconnects with conventional CMOS technology.

In this chapter CMOS compatible materials are first introduced with principal optical characteristics, then the theoretical basis of an optical communication link is given, focusing on the transmitter components and modulation schemes. Later on, the optical channel is introduced with its common implementation and future development; in this regard, datacentre internal structure is analysed to better understand motivations leading towards integration of photonic circuits in communication systems.

In the second part of the chapter, common modulation strategies adopted in silicon photonics are reviewed heightening advantages and drawbacks of each category, concluding with common structures for realising CMOS compatible modulators.

2.1 Germanium, Silicon and GeSi

Germanium and silicon belong to the group IV column of the periodic table of elements and share the same diamond crystal lattice with face-centred cubic unit cell. An important advantage over III-V material is the CMOS compatibility of Ge allowing simple integration of active devices with standard processes. The main characteristics of these two semiconductors are summarised in Table 2-1 from reference [38], highlighting the difference in bandgap, mobility and lattice constant.

Table 2-1 Principal properties of silicon and germanium

Properties	Bandgap [eV]	Electron Mobility [$cm^2V^{-1}s^{-1}$]	Hole Mobility [$cm^2V^{-1}s^{-1}$]	Lattice Constant [nm]
Silicon	1.11	1400	450	0.5431
Germanium	0.66	3900	1900	0.5658

The semiconductor energy bandgap is the separation between the Valence Band (VB) and the Conduction Band (CB). The VB is the highest energy region where electrons are found at the absolute zero temperature and CB is the lowest energy region with vacant electronic states. From the band structure [39], semiconductors are classified as direct or indirect bandgap depending on whether the maximum of the VB and the minimum of the CB are aligned or not; this aspect is fundamental for photonic devices that use absorption and/or emission of photons as active mechanism for interacting with light, as explained in section 2.3. In Figure 2-1 the difference between direct and indirect bandgap semiconductors is depicted; on the left, in a direct bandgap semiconductor photons with energy close to the direct bandgap can be absorbed by an electron to form an electron-hole pair with no change in momentum, whereas in indirect bandgap semiconductor (right drawing) absorption is accompanied with absorption or emission of phonons (reticular vibration) needed to vary the electron momentum, making this process less efficient.

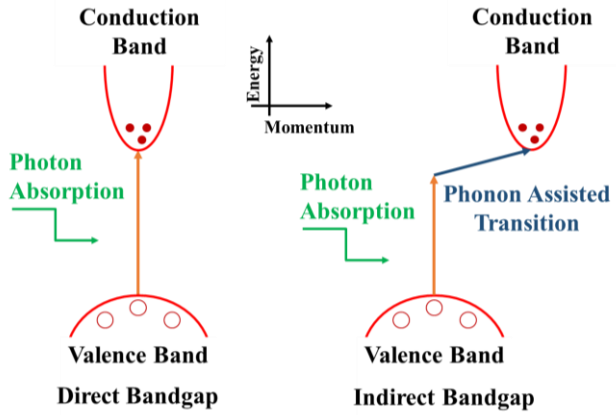

Figure 2-1 Direct (left) and Indirect (right) Bandgap Semiconductor. In the first case an e-h pair is created with same momentum by absorbing a photon, in the second case the e-h can be created if a phonon (blue arrow) is absorbed/emitted to change the electron momentum.

Germanium and silicon are both classified as indirect bandgap semiconductors, with the smallest (indirect) bandgap at 0.66 eV and 1.12 eV, respectively; but a direct bandgap energy at around $E_{\Gamma 1} = 0.8\,eV \approx 1550\,nm$ is found in Ge, as depicted in Figure 2-2a. In silicon instead the smallest direct bandgap is found at $E_{\Gamma 1} = 3.4\,eV \approx 365\,nm$ (Figure 2-2b).

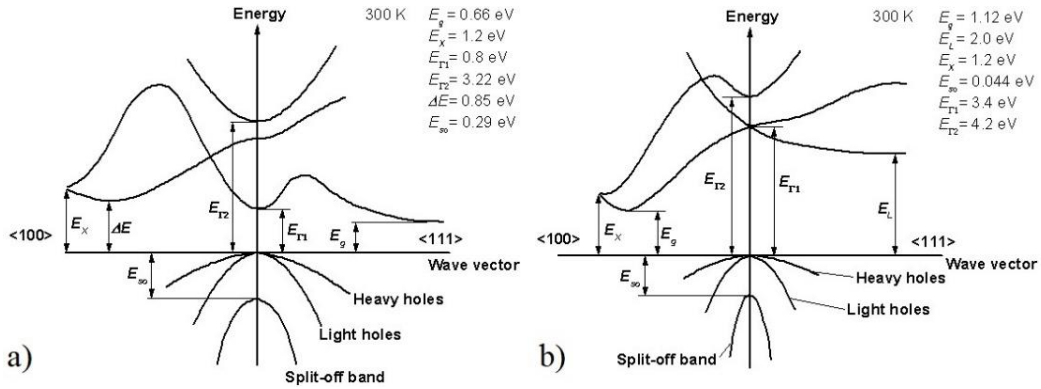

Figure 2-2 Band structure of Bulk Ge (a) and Si (b) [40]. Although classified as indirect bandgap semiconductors, both Si and Ge have a direct bandgap. For Ge the corresponding wavelength is about 1550 nm, hence this material can be used for active devices that interacts with light in the near infrared.

As a consequence, the absorption spectra of those materials differ. In Figure 2-3 from references [41][42], the absorption in the range between 0.6 eV (~2.07 μm) and 4 eV (~0.31 μm) is shown for germanium in red and for silicon in blue, respectively. In the inset, the absorption of Ge between 0.6 eV (~2.07 μm) and 1 eV (1.24 μm) from reference [43] highlights the knee on the absorption spectrum (at about 0.8 eV or 1.55 μm) representing the shift from indirect to direct transitions. As the photon energy matches the Ge direct bandgap Γ_1, absorption (red curve) raises from 100 cm^{-1} to 5000 cm^{-1} (reached at 0.81 eV), making germanium absorbent in the C-band (near infrared). Between 1 eV and 2.2 eV, the absorption raises almost linearly reaching a saturation value of about 1E6 cm^{-1}. Silicon (blue curve), instead, is transparent for wavelength above 1.12 eV (below ~1.1 μm) [44]. Between 1.12 eV and 1.4 eV (~0.89 μm), absorption raises from 1 cm^{-2} to about 500 cm^{-1}. Absorption increases almost linearly from 500 cm^{-1} to 1E5 cm^{-1} between 1.4 eV (~0.89 μm) and 3.2 eV (~0.39 μm). A sharp increase of absorption, up to 1E6 cm^{-1}, is found at 3.4 eV (~0.36 μm) corresponding to the direct bandgap Γ_1 of Silicon. For higher photon energy, the absorption saturates to 1E6 cm^{-2}. The silicon transparency in the near infrared allows to realise waveguide on SOI with low loss, 0.85 dB/cm in the C-band for TM mode (1.09 dB/cm for TE mode) [45] and 1.9 dB/cm for TE mode at λ = 2 μm [46]. At 1.55 μm, however, non-linear effects such as the two-photon absorption (TPA) [47] responsible of an imaginary refractive index of about 10% of the real part [48] and causing conversion of

photons into heat, free-carriers absorbing light and varying the material refractive index, and other non-linear effects, affect light propagation in silicon [49].

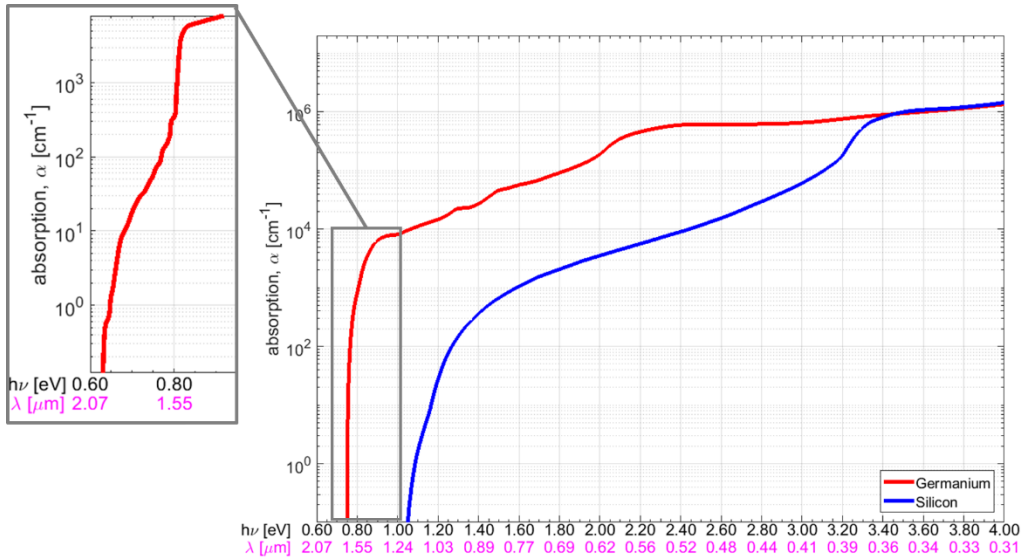

Figure 2-3 Absorption spectra of Si (blue) [41] and Ge (red) [42]. In the inset, a zoom for the Ge absorption coefficient around 0.8 eV [43].

At the communication wavelengths Ge refractive index is higher than that of Si, in reference [50] the refractive index between 0.5 eV and 6 eV has been calculated for a GeSi alloy with a varying content of Ge, from 0 to 1. In Figure 2-4 the refractive index in the photon energy range from 0.5 eV to 1.5 eV increases if the Ge content increases; at 1.55 μm (0.8 eV) the refractive index of Si and Ge are about 3.44 and 4.12, respectively.

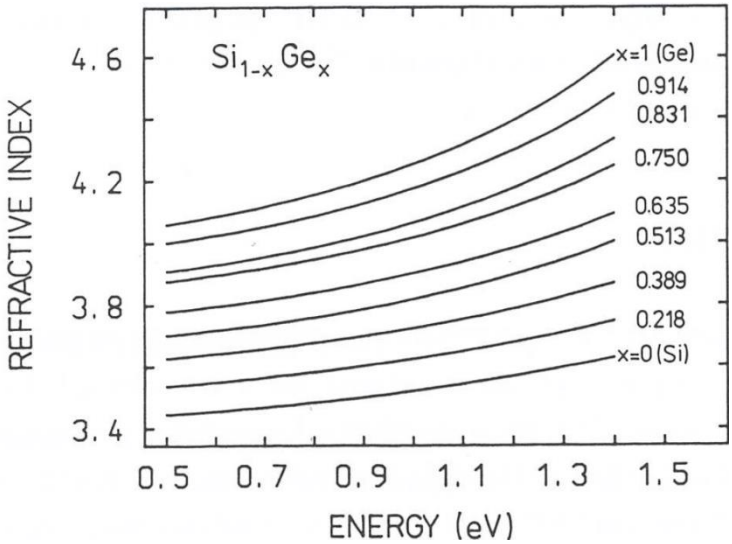

Figure 2-4 Refractive index of GeSi with Ge content from 0 to 1 at different energies, reproduction from reference [50].

Charge-carrier mobility is a key aspect for today transistors; mobility is referred as the constant of proportionality between the average drift velocity of the carrier (electron and hole) and the electric field. Higher mobility is beneficial for CMOS transistors by

increasing the drive current and allowing to fabricate transistor with higher electric RF performances or reduced power consumption thanks to a smaller capacitance. Higher mobility by increasing the diffusion length, defined by the distance carriers move between generation and recombination [51], is beneficial for photonic devices too, allowing to design more efficient photodetectors; CMOS compatible devices made with germanium benefit from its high carrier mobility.

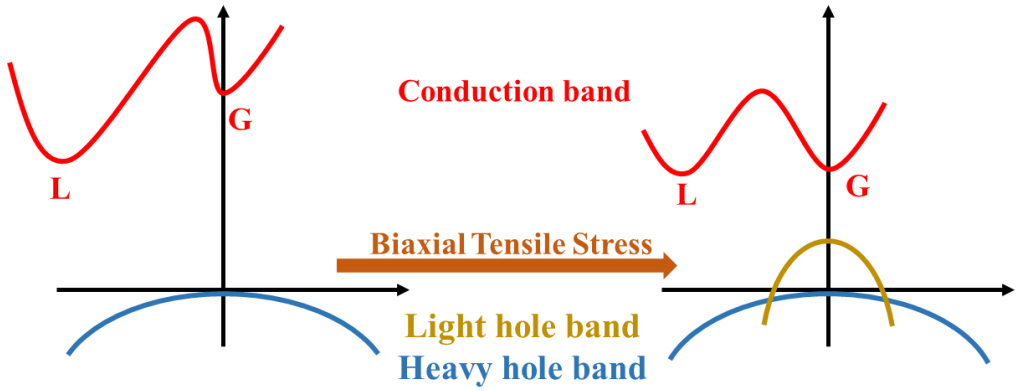

Figure 2-5 Effect of the Biaxial Tensile Strain on the Conduction and Valence Bands. The strain reduces the bandgap between the Γ (CB) and the light hole VB, thus red-shifting the material band-edge.

The lattice constant of Ge ranges between 0.56573 nm and 0.56579 nm whereas for Si it is about 0.5431 nm [52]; the 4% lattice mismatch between the two materials causes strain accumulation and misfit dislocations when Ge is deposited on silicon. If a thin layer of Ge_xSi_{1-x} (with $1<x<0$) is deposited on Si, the lattice mismatch (Figure 2-6a) is compensated at the layers interface in two ways, by straining the Ge_xSi_{1-x} material to match the Si crystal lattice (pseudomorphic growth, Figure 2-6b) or by introducing misfit dislocations at the layers interface (Figure 2-6c) [53].

In the case of pseudomorphic growth (Figure 2-6b), the lattice mismatch is counterbalanced by biaxial strain, compressive strain in the plane of the film and tensile strain in the perpendicular plane of the film [54]. The effect of the biaxial strain is to shift the average position of both VB and CB and cause the splitting of the energy bands, as shown in Figure 2-5. The degeneracy effect due to strain is also found in the CB [55] but it has different nature. In the VB it has an orbital nature, in the CB is spatial [56]. Strain can also be hydrostatic (volumetric), in this case, a shift of the overall energetic position of the band occurs [55][56]. Strain also increases light hole mobility, in reference [57] a hole mobility of 10000 cm^2/Vs with 1% of in-plane strain was calculated.

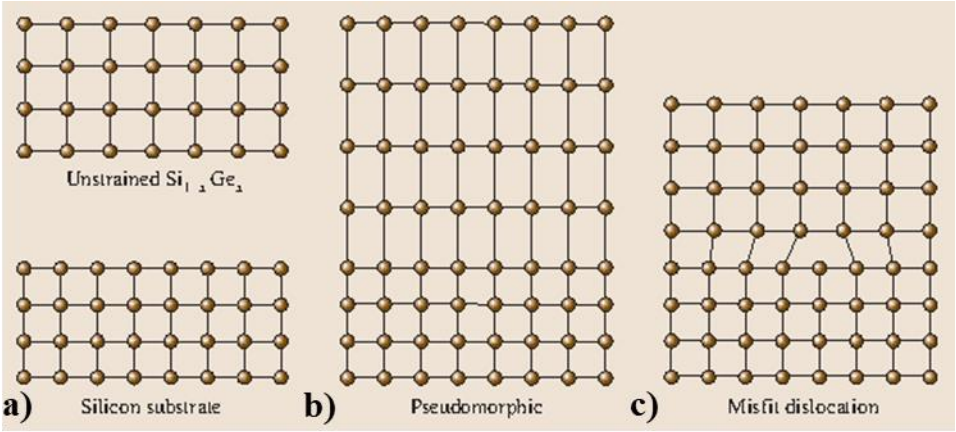

Figure 2-6 (a) Atomic drawing of unstrained Ge_xSi_{1-x} ($1<x<0$) on top and unstrained silicon on the bottom. (b) Pseudomorphic growth of Ge_xSi_{1-x} on Si, the lattice mismatch is compensated by elastic strain. (c) Unstrained growth of Ge_xSi_{1-x} on Si with formation of misfit dislocations, misfit dislocations are formed if the critical thickness is overcome in a pseudomorphic growth. Image reproduced from reference [53].

Introduction of misfit dislocations at the layers interface (Figure 2-6c) [53] can compensate the materials lattice mismatch, allowing the film to be relaxed. Stable misfit dislocations confined at the layers interface are also found in pseudomorphic growth if the growth reaches a specific thickness, dependant from the material composition (4 nm to 10 nm for Ge [58]), called critical thickness. If deposition continues, threading dislocations generate as a by-product of misfit dislocations [59] that propagate through the film until a proper termination is reached [60]. The resulting film is a stack layers of strained and relaxed materials containing a certain quantity of defects that might degrade the film characteristics. Threading Dislocation Density (TDD) should be kept low to avoid poor performances and small time-to-failure of devices fabricated with this film. Threading dislocations, in fact, behave as acceptor-like defects in relaxed Ge with energy level within the material energy bandgap [61], increasing the carrier recombination [62].

Material properties of Ge can be tuned by growing GeSi whose stoichiometric ratio can be varied freely to shift material electro-optic characteristics between those of silicon and germanium. A small quantity of silicon, for example, shifts the band-edge of GeSi to higher energy from the L-band to the C-band, making the material better suited for C-band communication applications. GeSi can be easily grown with Molecular Beam Epitaxy (MBE) [63][64] or with Chemical Vapour Deposition (CVD) in ultra-vacuum (UHVCVD) [65] or Reduced Pressure (RPCVD) [66]. Further details on the RPCVD are given in section 4.2.2.2 being the growth method adopted in this project.

Strain engineering can be exploited to tune electro-optic characteristics of devices made with Ge or GeSi [67][68][69]. Applying tensile strain reduces the bandgap, allowing

to absorb photons at lower energy (redshifting the absorption edge). On the other hand, compressive strain produces blueshift, due to an increment of the bandgap. Compressive (tensile) strain can be obtained by growing the epitaxial layer on a substrate with smaller (bigger) lattice constant and/or applying mechanical stress.

In conclusion, Ge and Si belonging to the same group of the periodic table of elements, are fully compatible; thanks to its direct bandgap, Ge can be adopted in active devices that use the imaginary part of the refractive index to modify the propagating light. Growing GeSi alloy permits to modify the energy band structure for shifting the operation wavelength. Strain, naturally accumulated when growing Ge on Si due to the ~4% lattice mismatch, also plays an important role in determining the material behaviour. Hydrostatic strain shifts the energy level of the VB and/or CB and the biaxial strain degenerates the bands of VB and/or CB; strain, hence, offering another degree of freedom during device design to tune the operation wavelength.

2.2 Optic communication link

A high-speed optical link comprises two fundamental elements: a transceiver and a channel, as illustrated in Figure 2-7.

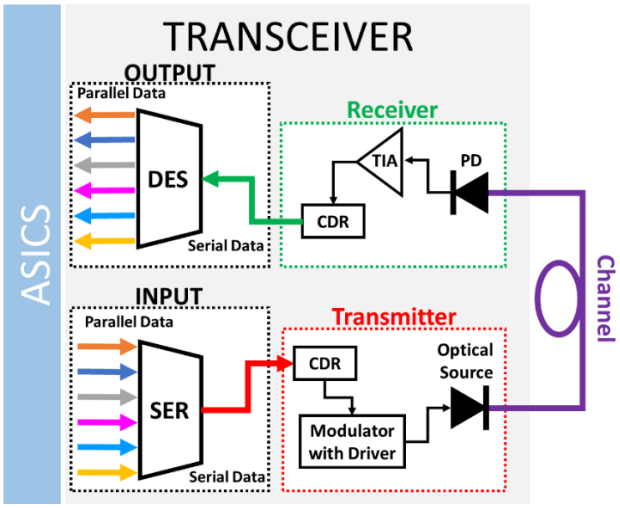

Figure 2-7 Representation of a high-speed optical link. Parallel data from the ASICs are serialised with a SerDes (SER) unit. After Clock and Data Recovery (CDR), the electrical input is converted in a pulsed optic signal by modulating a Laser (Optical Source) with a Modulator with Driver. After propagation through the optic fibre (Channel, in purple), the signal is converted into electric with a Photodiode (PD), the photocurrent is then translated in a usable voltage with a Trans Impedance Amplifier (TIA). A CDR stage precedes data parallel conversion with a SerDes (DES).

Parallel electric data coming from the Application-Specific Integrated Circuits (ASICs) are serialised (SER) and converted in an optic stream with a modulator and a laser (red dotted box in Figure 2-7). The optic signal is then transmitted through the channel, an optic fibre that determines how the data is transmitted. At the receiver (green dotted box in Figure 2-7) the optic signal is converted back into an electric serial stream with a photodiode and a Trans Impedance Amplifier (TIA). The last step is to make the signal parallel again using a deserializer (DES).

2.2.1 Transceiver

Parallel data from the ASICs are serialised using a functional block called SerDes, which provides single line (or a differential pair) for high-speed transmission to minimise the number of interconnects. SerDes generates essentially two kinds of encoded signals, Non-Return-to-Zero (NRZ) also known as Pulse Amplitude Modulation with two levels (PAM-2) and a digital modulation with four levels (PAM-4) [70], a graphical representation is depicted in the Figure 2-8.

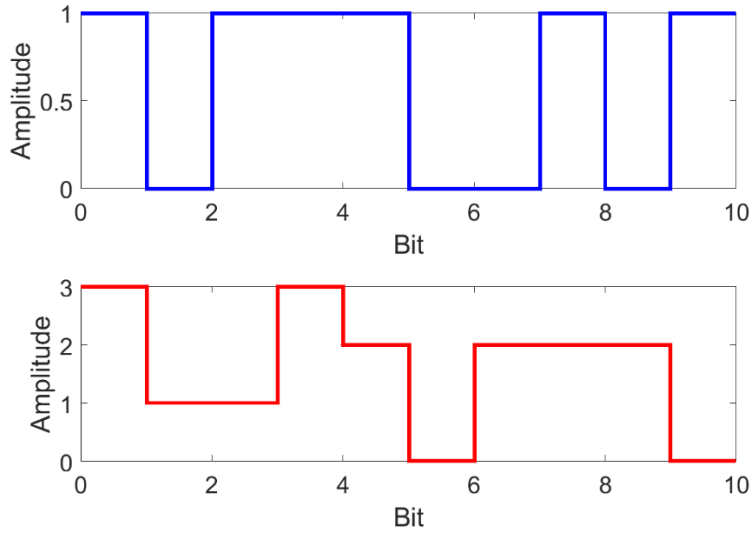

Figure 2-8 (top) NRZ encoding, only two logic levels are available, representing the single bit-0 and bit-1. (bottom) PAM-4 encoding, the four levels from 0 to 3 represent symbols of two bits each using the Grey coding (00, 10, 11, 01).

In the first case (Figure 2-8, blue plot), the bitstream coming from the ASICs is encoded with two signals, a high amplitude signal for bit-1 and a low amplitude signal for bit-0; the gross bitrate (R) [71], defined as the number of bits per second ($R = 1/T_b$), is the system speed. Another PAM-2 encoding often used is Return-to-Zero encoding (shown in Figure 2-9), where the signal always returns to zero after $T_b/2$, making the system stronger against error [72] but more bandwidth demanding, due to the increased number of transitions.

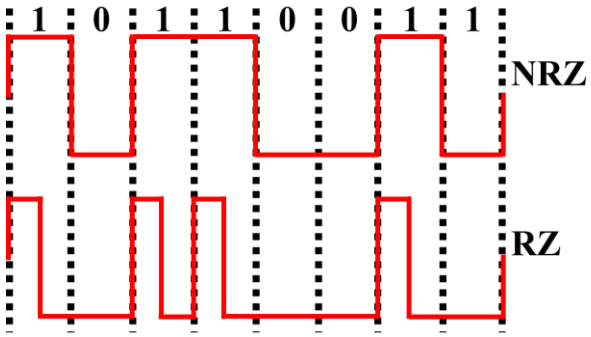

Figure 2-9 In NRZ (top) the logic level occupies the whole timeslot Tb, whereas in RZ encoding the logic level return always to the low level.

In PAM-4 (Figure 2-8 red plot) bits are aggregated in pairs (symbol), the possible bit combinations (Grey code: 00, 10, 11, 01) are coded with 4 different signal levels, as a result, PAM-4 encoding delivers twice the speed of PAM-2 with same bandwidth or same speed with half of PAM-2 bandwidth at cost of more complicated design due to PAM-4 SerDes reduced noise tolerance.

Following the SerDes, a Clock and Data Recovery unit (CDR) [73] recovers the clock and the bitstream before optical conversion, obtained by modulating an optical source (usually a Vertical Cavity Surface Emitting Laser, VCSEL) directly by varying the driving current or with an external modulator [74].

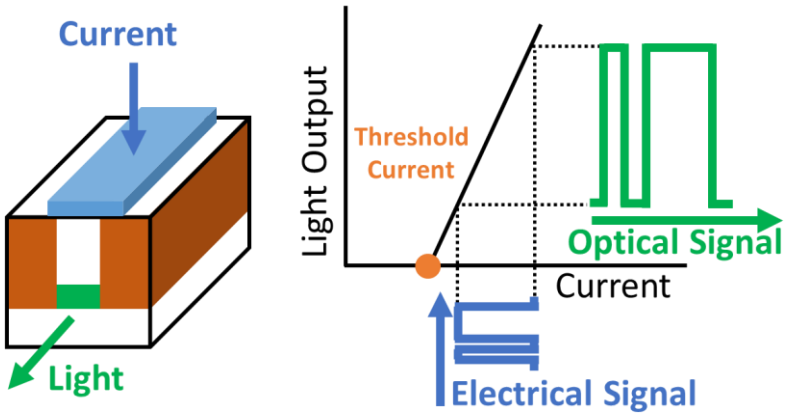

Figure 2-10 (left) Laser diode drawing, if the injected current is higher than the Threshold, the device emits light, (right) by modulating the current an optical replica of the electrical signal is obtained.

In the first case, schematically represented in Figure 2-10, the laser is biased close to the threshold and the encoded signal is applied to the laser driver; in absence of signal (bit-0) the current is below threshold (orange dot in Figure 2-10) and the laser is "off", in the presence of a bit-1, the current is above threshold an optical pulse is generated. This modulation is referred as On-Off-Key (OOK). Interesting results have been accomplished with VCSEL lasers operating at 850 nm, achieving speeds between 50 and 70 Gbps with

NRZ modulation [75][76]. Direct modulated VCSEL operating at 1550 nm have, also, been developed showing speed up to 115 Gbps [77][78]. Amplitude modulation in laser inherits, however, phase modulation and temporal phase variation (chirp) that limit the reach; attempts to reduce and inverse the chirp have been proposed [79]. Another issue of direct laser diode modulation are relaxation oscillations, for which laser power does not reach the steady state immediately after a transition but undergoes to damped oscillations, causing ripples on the transmitted signals, as shown in the Figure 2-11 from reference [80]. Non-linearities and temperature sensitivity are other important limiting factors to the direct VCSEL modulation.

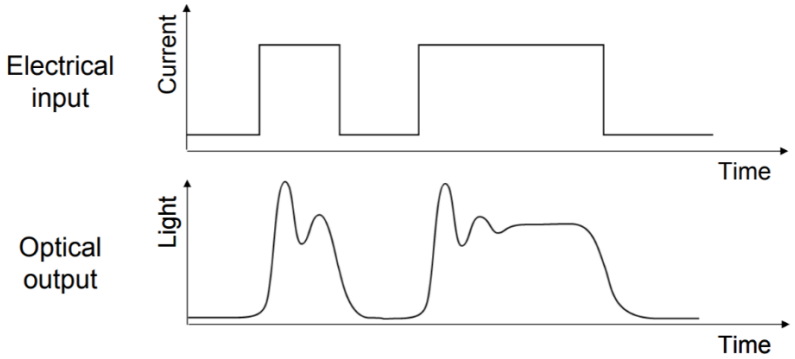

Figure 2-11 Electric signal and modulated optical signals with overshooting caused by relaxed oscillations in the direct modulated laser. Reproduction from reference [80].

In the case of external modulation, the laser is operated in Continuous Wave (CW) and an external device (modulator) modifies the light coherently with the bitstream. Different modulations can be adopted by varying the carrier amplitude, frequency and/or phase; the modulation schemes are called Amplitude-Shift-Key (ASK), Frequency-Shift-Key (FSK) and Phase-Shift-Key (PSK), respectively [74].

ASK is simple to implement but is susceptible to sudden changes in gain and is band-inefficient, FSK and PSK are less susceptible to noise, although FSK requires twice the bandwidth; PSK is bandwidth efficient but coherent detection (clock synchronisation with the transmitter) is needed. Differential-PSK (DPSK) overcomes PSK detection limitations by encoding information using a phase change between adjacent bits. In this case each bit is the phase reference of the following so that direct detection is possible [81].

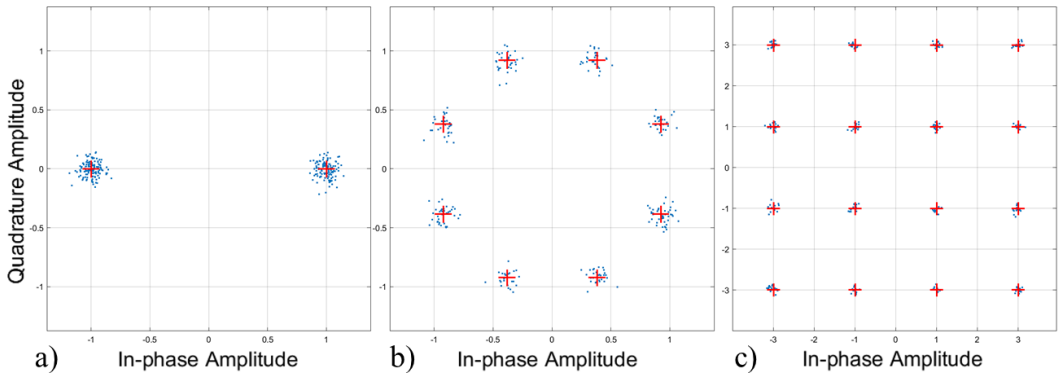

Figure 2-12 Simulation with Matlab® of PSK (also antipodal ASK), 8-QPSK and 16-QAM modulation. Each symbol is represented by points on the constellation plot (red cross). The received samples (blue) are affected by noise and surround the constellation points; the symbol distance depends on M, while M increases, the distance reduces and with that the robustness of the link to errors and noise.

Modern WDM systems often adopt multi-level schemes, such as 2^M-QAM and 2^M-PSK [74], by integrating both amplitude and phase modulation to carry more data with same bandwidth. In those schemes, 2^M signals carry symbols of M bits at symbol rate equal to M times the bitrate. Each symbol, defined by its amplitude and phase, is represented by a point of the constellation diagram on the complex cartesian plot, the greater M the higher the numbers of points on the constellation. In Figure 2-12 are shown three examples, from left to right M is 1 (a), 3 (b) and 4 (c); the total number of points (symbols) goes from 2 (a) to 16 (c) permitting to transmit more data on the same channel. The augmented number of bits per symbol, however, comes with an increased complexity of the transceiver; on one hand the transmitter must generate more distinctive signals and coherent detection is mandatory at the receiver; on the other hand, the error tolerance decreases due to reduced symbol distance, making misinterpretation more probable.

Table 2-2 Comparison between single level and multilevel modulation at 100 Gbps without polarization multiplexing [82]**.**

	Code word [bits/symbol]	Symbol Rate [Gbaud]	Detection	Efficiency [bits/sec/Hz]	Reach [miles]
OOK	**1**	**112**	**Direct**	**0.5**	**< 200**
DPSK	**1**	**112**	**Direct**	**0.5**	**< 200**
DQPSK	**2**	**56**	**Direct**	**1**	**< 500**
QPSK	**2**	**56**	**Coherent**	**1**	**> 1,000**
16-QAM	**4**	**28**	**Coherent**	**1**	**~ 1,000**

Table 2-2 from reference [82] shows common applications for the different modulation schemes based on a 100 Gbps link; OOK (ASK) and DPSK are used for short connection, whereas multilevel schemes are adopted for long haul connections. In optic communication a fourth modulation technique is possible by controlling the light polarisation with an external electric field; this effect known as the Pockels Effect will be discussed later in the chapter. Requiring active polarisation management at the receiver,

polarisation modulators are less common but they can be exploited to increase the spectral efficiency or to implement pseudo-multilevel modulations [81].

The generated optical datastream propagates into the channel, as discussed in section 2.2.2; at the receiver, the optical signal undergoes the reverse process to recover the parallel electric data stream. First, the optical signal is converted in current with a fast photodiode, then the current is converted into a usable voltage with a Trans Impedance amplifier (TIA).

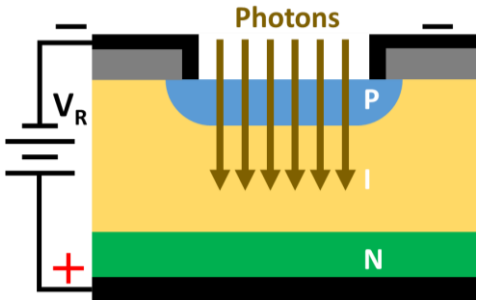

Figure 2-13 PIN Photodiode schematics reverse biased. Photons are absorbed in the intrinsic layer allowing electrons to go to the conduction band. E-h pairs are accelerated by the electric field due to V_R, generating the photocurrent.

Photodiodes are PN or PIN junctions (Figure 2-13), usually reverse biased, that convert the incident light in an electrical signal by exploiting the Photoelectric Effect (PoE), where absorbed photons generate electron hole pairs, that in presence of an electric field generates a flow of carriers or in other words a current, called photocurrent [3].

In a [83] PN junction at equilibrium, a depletion region forms between the P and N doped regions due to diffusions of carriers from a region with higher concentration to a region with lower concentration. At the junction, the excess of electrons of the N-doped region diffuses in the P-doped region and recombines with the holes of the P-doped region. On the same time the excess of holes of the P-doped region diffuses in the N-doped region and recombines with the electrons of the N-doped region. Majority carriers (electrons in the N-doped region and holes in the P-doped region) are, then, depleted at the interface. The positively charged donor atoms at the N-doped region interface and the negatively charged acceptor atoms at the P-doped region interface cannot move, being part of the crystal, forming the depletion region, as shown in Figure 2-14a. In the depletion region an electric field, which opposes to the carrier diffusion, establishes and increases as more carriers diffuse. The electric field eventually stops further diffusion of majority carries, bringing the depletion region to an equilibrium. At reverse bias (p-side connected to the negative terminal, n-side connected to the positive terminal, Figure 2-14b), the majority carriers are pulled away from the junction increasing the depletion region and the electric field (Figure 2-14, right). In a PIN diode, an undoped layer (intrinsic) is between the P and

N doped regions, the depletion region is hence contained almost completely in the intrinsic layer and is larger than the depletion region of a PN diode. PIN diode are extensively used for absorption based photonic devices, photodiodes for example, due to the enhanced volume where e-h pairs can be generated with photon absorption and the reduced junction capacitance that improve the device bandwidth and efficiency.

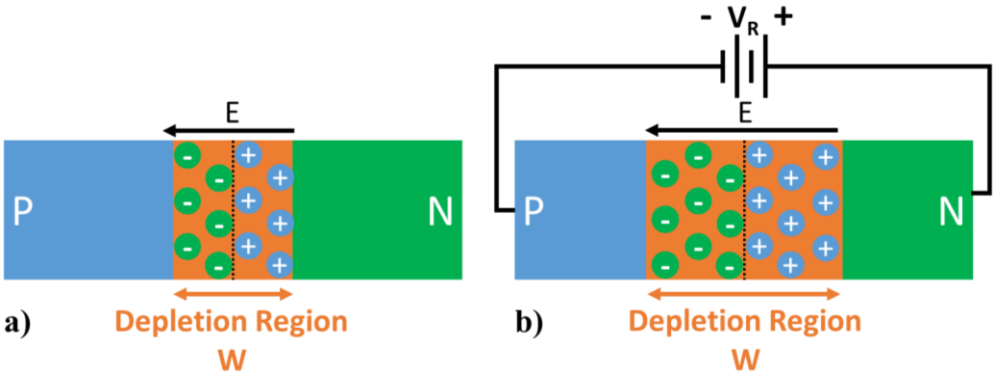

Figure 2-14 PN diode at equilibrium (a) and under reverse bias (b). W is the depletion region width (orange), E the electric field with its direction and V_R the reverse bias. (a) Without bias, an electric field is generated at the interface by attraction of majority carriers to opposite doping and a zone with minority carriers only is formed (W), with a reverse bias (b) more carriers are pulled and the width of W increases.

Photodiodes working in the standard communication wavelength range are available in bulk germanium [34] or quantum wells [35], integrated in SOI waveguides [84] with high-speed performances [85] (above 50 Gbps). Photodiode efficiency is estimated with responsivity, which measures the electrical output per optical input; responsivity approaching 10 A/W was measured on a silicon photodiode with 35 GHz bandwidth operating in a wavelength range from 1100 nm to 1750 nm [86]. III-V photodiodes are also available, offering 42 GHz bandwidth, 0.5 A/W responsivity and able to detect 106 Gbps PAM-4 transmission over 40 km Single Mode Fibre (SMF) without optical amplifier [87].

At the end of the receiver line, a CDR and a SerDes recover the clock/data and convert the serial data stream to the original parallel data stream.

2.2.2 Optic Channel

In the previous section, an overview of a communication system was given; the optical channel, however, needs to be examined further being fundamental for the development of optic modulators. The optic channel essentially consists of an optic fibre, in which propagation is possible thanks to the Total Internal Reflection (TIR) [74].

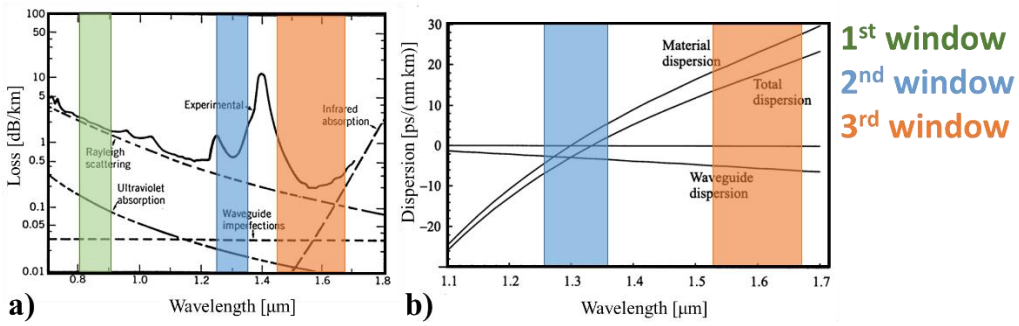

Figure 2-15 Propagation loss [88] (a) and dispersion (b) of the single mode silica optic fibre [74]. (a) The optimum windows are highlighted, the 1st window in green, the 2nd in blue and the 3rd in orange; (b) the dispersion for the 2nd and 3rd windows are highlighted in blue and the in orange, respectively.

From the propagation loss spectrum of single mode silica fibres [88] (Figure 2-15, a), which is the sum of Rayleigh scattering, absorption and waveguide imperfection, three windows for optimum communication are defined. The 1st window between 800 nm and 900 nm (green), mostly used with Multi Mode Fibres (MMFs) and VCSEL operating at 850 nm, the 2nd window also known as O-band (blue) between 1260 nm to 1360 nm and the 3rd window (orange) between 1530 nm and 1675 nm, divided in C-band (1530 nm to 1565 nm) and L-band (1565 nm to 1625 nm).

In Figure 2-15b, instead, the optic fibre dispersion is plotted. In SMFs, dispersion due to material and waveguide affects light propagation in the optic fibre by broadening or shrinking the light pulse and introducing chirp. Material dispersion [89] is a type of chromatic dispersion caused by the dependency of the refractive index to the light wavelength that allows rays at different wavelength to travel at different group velocity. Waveguide dispersion is another type of chromatic dispersion due to partial propagation of light in the cladding at different velocity than that of the core [89]. In MMFs, intermodal dispersion [89] is also found for which different modes propagate with different velocity, distorting the signal and ultimately limiting the reach.

Propagation loss in the O-band is high but no appreciable dispersion is found (Figure 2-15 right, blue region), making this band preferable for short/medium communication systems (<40 km [90]). The C-band exhibits, instead, the lowest propagation loss (< 0.2 dB/km) but suffers from anomalous dispersion, as shown in Figure 2-15 (right, orange region), requiring dispersion management schemes [91]; C-band transmission is commonly implemented for long connections (from 40 km to thousands kilometres) because low loss permits to reduce the number of optical communication repeaters to recover the degraded optical signal due to channel attenuation. Recently, Multi Core Single Mode Fibres

(MCSMF) further improved performances by demonstrating multi-channel transmission over multi-1000 km with Spatial Division Multiplexing (SDM) [92].

In datacentres, optic fibres are fundamental to connect different servers with simple, reliable and fast interconnects, allowing high computational performance with distributed scheme. In Figure 2-16 a diagram from Intel® [93] highlights the internal structure of modern datacentres with current optic fibre technology and future deployment.

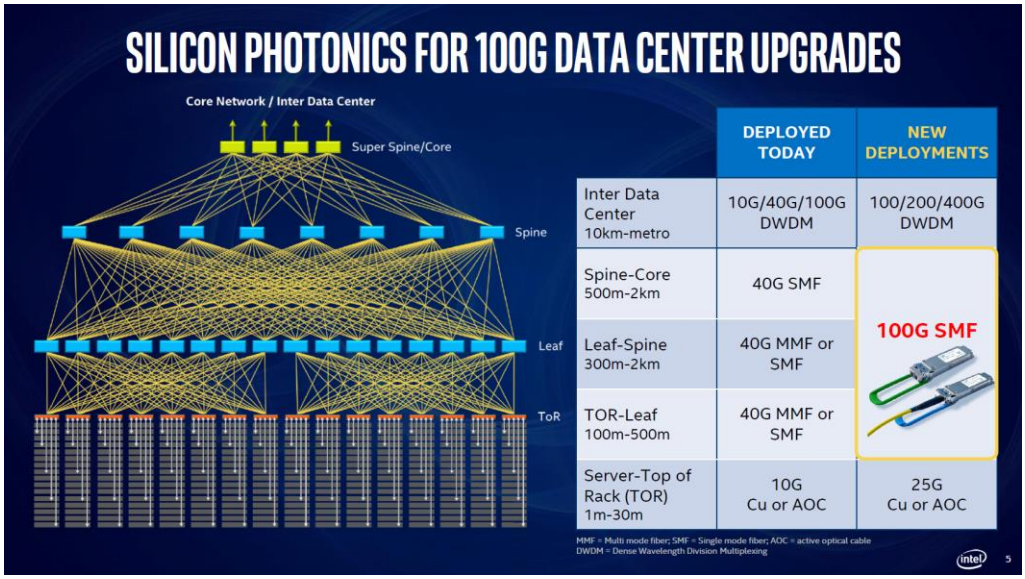

Figure 2-16 Intel® prediction on datacentre upgrades for the >100 Gbps, reproduction from reference [93].

Datacentre hierarchy comprises four levels, the core, the spine, the leaf and the Server Top of Rack (TOR); connections between levels are almost exclusively optical, MMFs and/or SMFs are deployed depending on the distances, only TOR connections are made with copper cables. In small datacentres, VCSEL-based transceivers are used to aggregate four 10 Gbps lasers in 40 Gbps streams, transmitted on MMFs over distances up to 300 m, but in bigger datacentres, implementing leaf-to-spine and spine-to-super-spine interconnects, SMFs are usually deployed, being distances greater than 300 m. Interconnects, however, are evolving as cloud computing advances, promoting a datacentric cloud network with simplified architecture, large bandwidth, low latency and high reliability to replace enterprise private networks [11].

Only a few years ago 100 Gbps interconnect, realised by aggregating four 25 Gbps lasers, was considered bleeding-edge technology. In only a few years these will be replaced by 200 Gbps and 400 Gbps interconnects, promoting single mode transmission also for short connections. MMFs have reach limited to 70 m at 25 Gbps [93] due to modal dispersion and attenuation, incompatible with link distances of modern hyperscale

datacentres. Transmission can be extended in the L-band, systems operating in both C and L band may offer up to 200 channels with 50 GHz spacing [11]. That is why single mode connections are considered future proof by system designers and are being deployed massively by datacentre operators with the result that, in terms of costs, single mode transceivers are now comparable to the multi-mode counterpart.

2.3 Modulation Strategies in the Silicon Platform

In the previous section, the principles of digital communication have been introduced, highlighting the fundamental role of optical modulators as a bridge between electronics and photonics, and the differences between communication platforms. In this section, the physics behind modulation, design and implementation of group IV-based modulators, are presented.

Optical modulators are classified as electro-refractive or electro-absorptive if modulation is obtained, respectively, by varying the real part or the imaginary part of the refractive index with an electric field. In the silicon platform the principal modulation mechanisms are Plasma Dispersion Effect on silicon, Franz-Keldysh Effect and Quantum Confined Stark Effect (commonly adopted with germanium bulk or quantum well, respectively), Pockels effect, Kerr effect and thermo-optic effect by depositing polymers and/or strain layers.

2.3.1 Plasma Dispersion Effect

Plasma Dispersion Effect (PDE) is commonly used for fabricating silicon-based modulators, in this case both real and imaginary parts of the refractive index are changed by a variation of free-charge concentration in the material. Pioneering studies of PDE on silicon for a wide wavelength spectrum were made by Soref and Bennet [94] producing, also, useful expressions to estimate the change in refractive index for a change of free-carrier concentration in silicon at 1.3 μm and 1.55 μm. The variation in free-carrier concentration in silicon can be obtained through [95] carrier accumulation, carrier injection or carrier depletion.

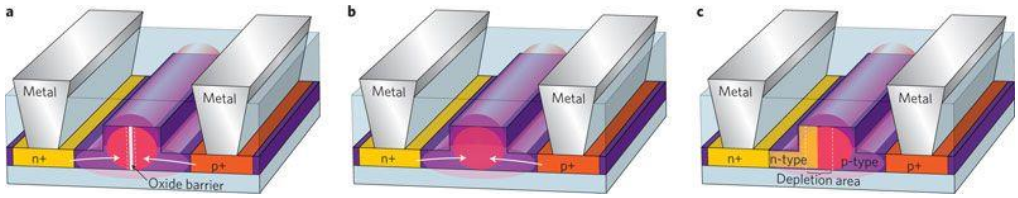

Figure 2-17 PDE modulation with **a** Carrier accumulation (capacitor), **b** Carrier injection (PIN junction in forward bias), **c** Carrier depletion (PN junction in reverse bias), reproduction from reference [95].

In the first case (Figure 2-17a), a capacitor is built using a thin layer of silica in the middle of the waveguide layer, a forward bias is applied for modulation. In the second case (Figure 2-17b), a PIN (highly doped p and n) structure is forward biased, injecting electrons and holes into the intrinsic region. In the third case (Figure 2-17c), a PN diode (lightly doped p and n) is reverse biased, indeed the built-in electric field (see section 2.2.1) increases from the electron-hole removal. Carrier injection modulators have the highest modulation efficiency but are bandwidth limited because speed relies on the slower diffusion of minority carriers with respect to that of majority carriers; pre-emphasis driving circuits can overcome this issue improving the device speed to 12.5 Gbps whilst also reducing the device power budget [96]. Pre-emphasis is often used in communication to boost the amplitude of the high-frequency components of a signal, distorted by the low-pass behaviour of the channel. In the simplest implementation the pre-emphasis driving circuits is a high-pass filter. Carrier depletion [97], instead, is based on majority carriers and limited by the RC constant of the device, offering much higher modulation speeds (> beyond 50 Gbps [98]). Nevertheless, this is at the cost of a relatively low modulation efficiency which increases the device footprint and power consumption. In carrier accumulation modulators, instead, the majority carriers accumulate on the surface of the central insulating layer (silicon dioxide) limiting the device bandwidth, dominated by device resistance and capacitance [99].

Advantages of PDE-based modulators derive from the full CMOS compatibility with standard process and the wide operation bandwidth. In the simplest implementation, a PN diode integrated into the waveguide produces phase modulation; amplitude modulation requires, instead, interferometric structures.

2.3.2 Franz-Keldysh Effect

CMOS Compatible materials have been investigated to implement electro-absorption modulators; Franz-Keldysh Effect (FKE) and Quantum Confined Stark Effect (QCSE), for bulk and quantum well devices respectively.

Theorized independently by Franz [100] and Keldysh [101], The FKE implies a change in the absorption coefficient under the effect of an electric field that tilts the band edges of a direct bandgap semiconductor (whose electron energy maxima and hole energy minima have the same momentum, Figure 2-1), allowing the tails of the Valence and Conduction band wave functions to extend into the bandgap (Figure 2-18); therefore a photon with energy lower than the semiconductor's bandgap can be absorbed by an electron to generate an e-h pair (tunnelling effect), as a result the absorption coefficient becomes proportional to the electric field strength. For photon energies higher than the energy bandgap $h\omega > E_G$ (Figure 2-18a), the overlap between the oscillating wavefunctions in the CB and VB and the excitation energy $h\omega$ (photon) determine the Franz-Keldysh Oscillations (FKO) because of interference of the electron waves in the CB and VB that enhances the transition for some photon energy and reduces for others [102][103].

The FKE is fast. In reference [104] 1 ps electric pulses were detected by exploiting the absorption variation due to FKE on GaAs. Modulators whose speed, limited by the RC time constant, exceeds 50 Gb/s can be fabricated by accurately choose device design.

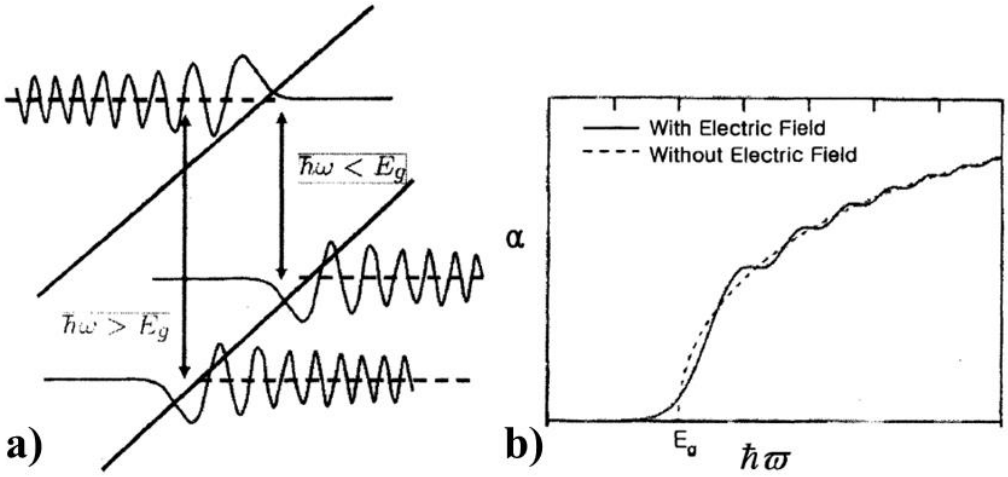

Figure 2-18 (a) The electric field tilts the Band Edges (Franz-Keldysh Effect), allowing photon with lower energy to be absorbed. (b) the Absorption Coefficient curve increases near E_G, for photon energies higher than E_G, Franz-Keldysh oscillations (FKO) due to wave-function interference, appear. Reproduction from reference [102].

A good candidate for using FKE is germanium because of its direct bandgap around 0.8 eV (corresponding to 1550 nm), allowing silicon integration of active devices working in the third window of the communication band. The modulation efficiency can be maximized for the wavelength range needed by growing GeSi alloy with low silicon content and/or by engineering the strain accumulated when the alloy is grown [105][106].

2.3.3 Quantum Confined Stark Effect

The engineering of epitaxial growth techniques allows to deposit Quantum Wells (QW), periodic nanometric thick layers of semiconductor, surrounded by barrier layers with different material composition and/or doping concentration to enable the Quantum Confinement (QC), a condition in which the energy spectrum becomes discrete and inversely proportional to the quantum well size, and excitons (electron hole bounded by Coulomb force) are available at room temperature. In a QW the electrons and/or holes motion is confined in one direction if the layer has thickness close to the size of the de Broglie wavelength of the electron wave function of the material [107]. In Figure 2-19a the diagram of a quantum well is shown, the bandgap energy discontinuity between the $Si_{0.19}Ge_{0.81}$ barriers and the thin Ge layer [108] provides the quantum confinement in the "z" growth direction, the discrete energy levels are shown in the picture with dashed lines. In the other two directions (xy plane), instead, the motion is still free. The discretization along z has three main effects: it shifts the energy band edges to higher energy, it keeps the electrons and holes closer improving the radiative recombination probability and it makes the density of the states independent from the energy [107].

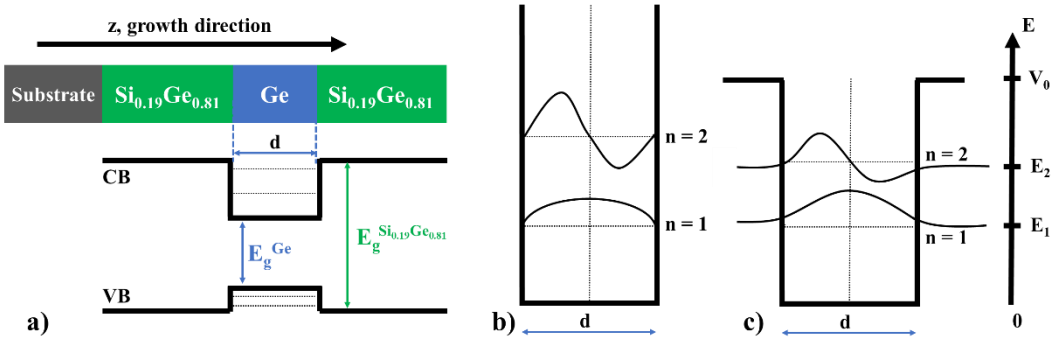

Figure 2-19 (a) Diagram of the quantum well realised using $Si_{0.19}Ge_{0.81}$ barriers and Ge thin layer [108], the resulting band diagram is sketched below. The discrete energy levels are shown in dashed lines. (b) Infinite well and (c) finite well with barriers of height V_0 showing the wave equation for electrons and holes found at discrete energy levels (n=1, 2).

The bandgap energy in a QW depends on the Ge layer thickness (d in Figure 2-19), this is found by solving the Schrödinger equation for electrons and holes in the well:

$$-\frac{\hbar^2}{2m_w^*}\frac{d^2\psi(z)}{dz^2} = E\psi(z) \qquad \text{Eq. 2-1}$$

Considering the simple case of the infinite potential well (Figure 2-19b), the normalised wave equation for electrons and holes is in the form of [109]:

$$\psi_n(z) = \sqrt{\frac{2}{d}} \sin k_n z \qquad \text{Eq. 2-2}$$

with $k_n = \frac{n\pi}{d}, n = integer \geq 1$, d is the well width (Ge layer thickness). The energy E_n is therefore:

$$E_n = \frac{\hbar^2}{2m_w^*}\left(\frac{n\pi}{d}\right)^2 \qquad \text{Eq. 2-3}$$

From Eq. 2-3, the allowed energy level E_n in the potential well depends inversely from d^2, meaning that the smaller the well width is (thinner Ge epilayer), the larger the confinement energy is [107] or in other words the bigger the energy bandgap is. The situation in a real QW is slightly different due to the finite nature of the well barrier, in this case the Schrödinger solution is a superimposition of sinusoidal wave functions inside the well and exponential decaying wave functions outside in the barriers, as shown in Figure 2-19c. The energy levels are smaller than those from the infinite well because the quantum confinement is reduced but they are still inversely proportional to the well width.

A graphical representation of the energy bandgap for bulk material and quantum well is depicted in Figure 2-20, as the nanostructure shrinks the bandgap energy increases (arrows from orange to blue).

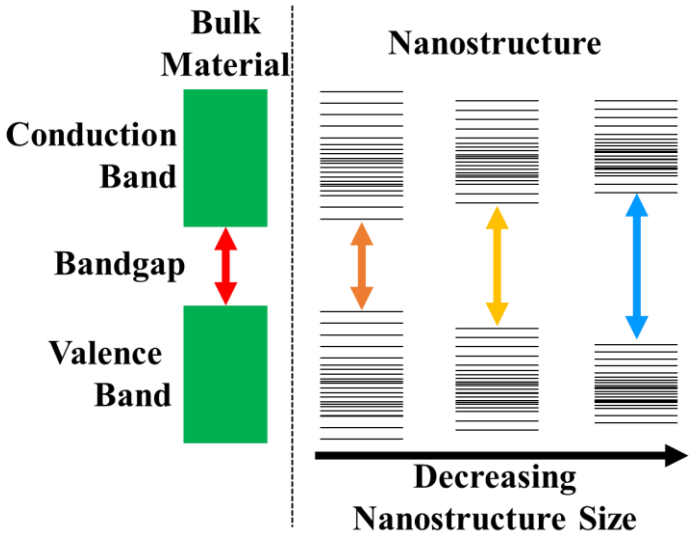

Figure 2-20 Bandgap energy for bulk and nanostructure materials, QC increases the bandgap if the size of the nanostructure reduces.

For direct bandgap quantum wells, in absence of an electric field, electrons and holes occupy discrete states (QC) with symmetric wavefunctions centred in the well (Figure

2-21a), only a set of discrete wavelengths can be absorbed/emitted by the nanostructure. If an external electric field is applied, holes are shifted to lower energy states and electrons to higher energy states; at the same time the related wavefunctions become asymmetric, as depicted in Figure 2-21b.

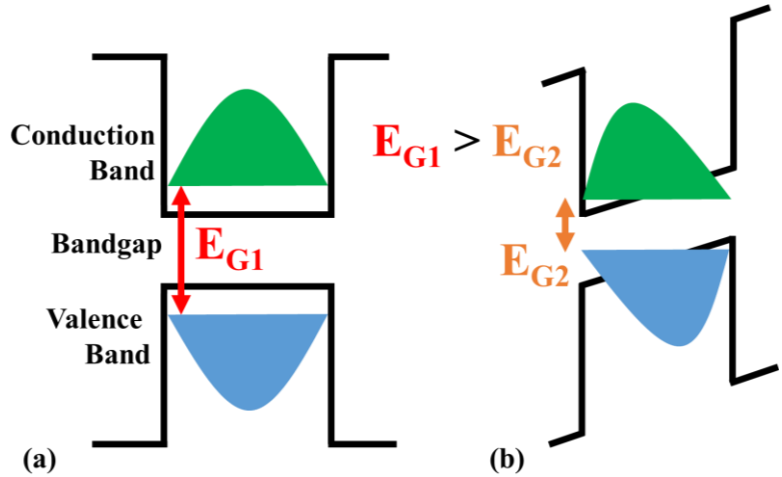

Figure 2-21 QCSE, the reverse bias tilts the discrete energy levels allowing photons with lower energy to be absorbed, similarly to FKE.

The effective bandgap energy reduces (similarly to what seen in the FKE), allowing photons with energy slightly lower than the quantum well energy bandgap to be absorbed; thanks to the discretisation of the bandgap, the so called Quantum Confined Stark Effect [110] is stronger than the FKE of bulk semiconductors. Deposition engineering can be exploited to shift the band edge towards the O-band or the C-band by modifying strain and quantum confinement [111].

2.3.4 Other Non-Linear Effects

The Pockels Effect (PE), a common electro-optic effect in asymmetric crystal-based modulators such as $LiNbO_3$ modulators, can be adopted for amplitude modulation [112] or polarisation modulation [113]. Unfortunately, silicon crystal is symmetric, therefore PE is practically absent in relaxed Si; however, strain can be accumulated in the silicon by depositing layers of SiN on top of the waveguide, thus breaking the crystal symmetry and allowing fabrication PE modulators [114].

The growing attention on modulators whose active layer is obtained by depositing polymers and other compounds on silicon waveguides. In reference [115], a polymer was deposited on a silicon slot waveguide achieving fast phase modulation with high efficiency and compact design; in another study a ferroelectric ceramic compound was used for Pockels modulation [116].

A second order electric effect, the Kerr Effect (KE) changes the refractive index proportionally to the square of the external electric field, in reference [117], a horizontal slot silicon waveguide filled with silicon nanocrystal embedded in silica realised a Kerr modulator.

It is worth mentioning a temperature based modulation technique, in reference [118] the silicon thermo-optic coefficient has been calculated to exploit temperature for phase modulation, in reference [119], instead, temperature has been used to change propagation conditions enabling modulation. The process and power budget of these nonlinear based modulators, however, make their integration in transceivers for communication difficult.

2.4 Common Structures

An Electro-Optic Modulator (EOM) is an active device to control phase, power or polarisation of a propagating mode by means of an external electric field. In silicon platform, modulation can be obtained with several structures, in this section the most common solutions are presented.

2.4.1 Interferometer

A modulation technique widely adopted in silicon is the PDE, implemented with Mach-Zehnder Interferometer (MZI) structures for amplitude modulation.

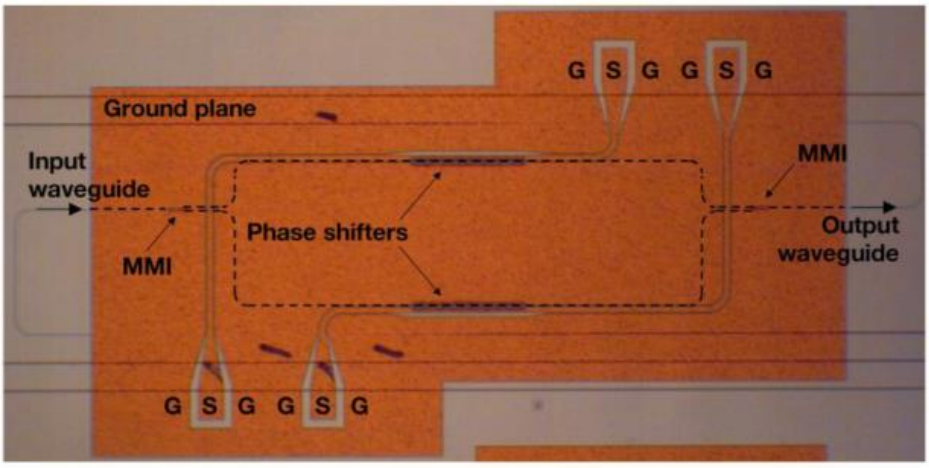

Figure 2-22 PDE MZI top view modulator, reproduction from reference [120]. The area is mostly occupied by the interferometer arms and travelling wave metal pads. The phase shifters, the active area, are about 250 μm long.

Figure 2-22 illustrates the top view of the PDE MZI modulator [120]. The input light is split in two modes using Multi Mode Interference coupler (MMI) that propagate in the two MZI arms. In the simplest implementation a phase shifter is realised in one arm using a PIN junction, the length and doping of the doped wells are chosen to achieve the required phase shift (π for ON/OFF modulation).

At the MZI output, another MMI makes the modes interfere. The output mode has same intensity as the input mode (minus the propagation losses) if the interference is constructive (modes in-phase) or zero-intensity if the interference is destructive (modes π-out-of-phase).

In an intensity PDE MZI modulator, the variation of the relative phase with time in the active arm produces chirp [121], which is detrimental for transmission at high rate and long-distances. The optic fibre chromatic dispersion [74], in fact, induces a spreading or compression of the pulse in time, proportional to the chirp; Push-Pull schemes alleviate this problem (as depicted in Figure 2-22). In this configuration, both MZI arms have phase shifters that work in opposite direction to keep the phase of the output signal constant in time. The ideal condition cannot be fulfilled and a residual chirp, caused by device asymmetries and losses, is still present.

In recent studies [122], PDE MZI depletion modulators with shifted junctions have been proposed to obtain polarisation independency, as depicted in Figure 2-23.

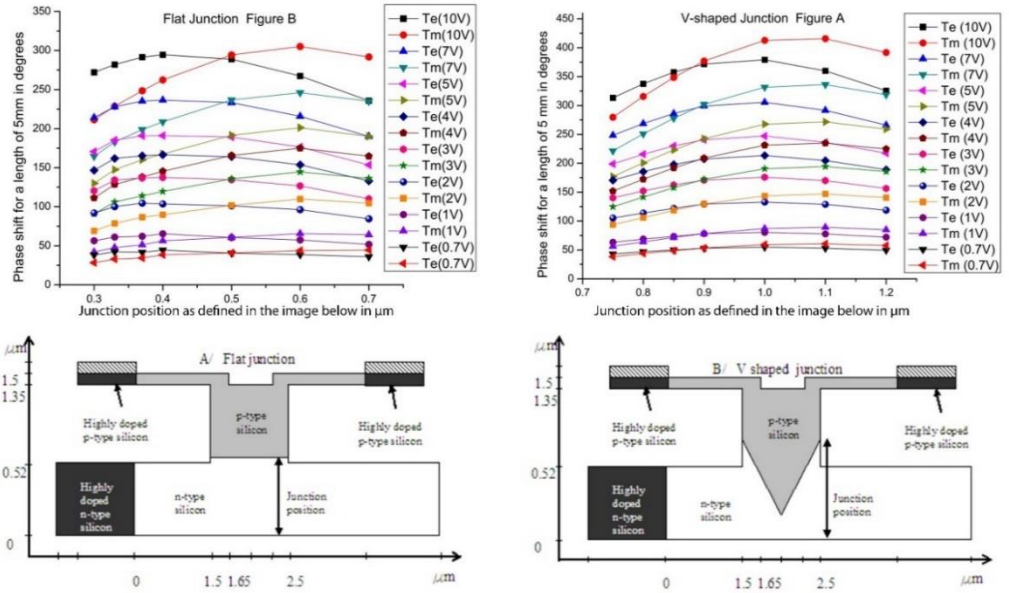

Figure 2-23 Phase shift vs junction position for TE and TM modes for the flat pn junction (left) and the V-shape pn junction (right), reproduction from reference [122]. By engineering the PN junction a similar phase shit vs bias is obtained for both TE and TM.

The main disadvantages of this class of modulators are found in the weakness of electro-optic effect in silicon requiring long phase shifters (~1 mm) with travelling wave electrodes, thus increasing the device footprint (> 1 mm^2) and power consumption (> 1pJ/bit).

2.4.2 Resonant Device

Micrometre modulators have been developed with resonant structures, an example is shown in Figure 2-24 from reference [123]. These devices comprise a straight waveguide and a ring waveguide sufficiently close for evanescent-wave coupling to happen. Inside the ring the light builds up in intensity over multiple round-trip, if the propagation length is a multiple of the wavelength (constructive interference). Some of the power couples back from the ring to the straight waveguide and interferes with the incident light; when resonance is reached, the modes interfere destructively producing a notch filter, where ideally one wavelength is not transmitted (Figure 2-23 right).

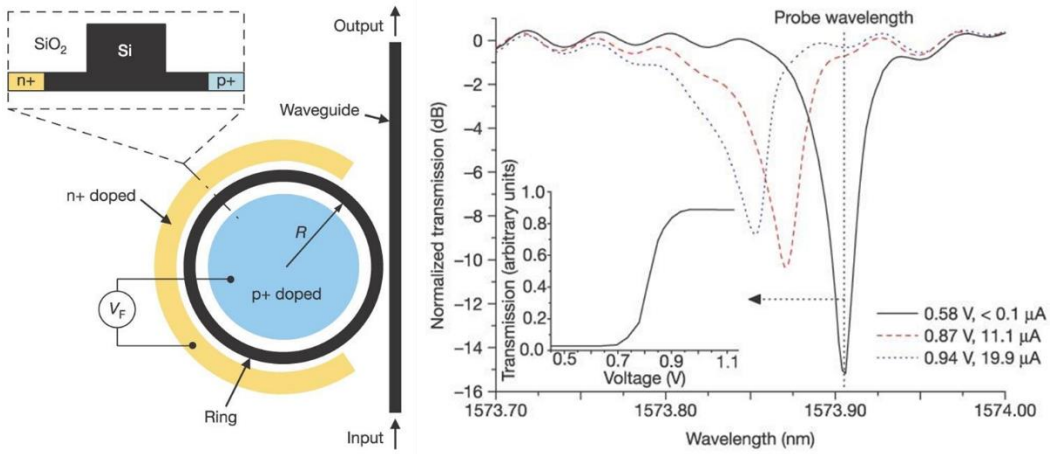

Figure 2-24 (Left) Cross-section and top view of a PDE Ring Resonator Modulator, reproduction from reference [123]. In the region with small gap between the ring and the straight waveguide, evanescence coupling is generated, inside the ring the light builds up if constructive interreference is met, the same port allows part of the light to escape and interfere with the incoming light. As a result, (Right) a Notch Filter response is achieved, the notch is then shifted with a bias.

If the effective refractive index of the ring is changed, the notch can be shifted in wavelength, as shown in the right plot of Figure 2-24, allowing modulation. A common way to exploit this effect is either using PDE or heaters (thermal effect). The main disadvantages of this structure are the narrow operation bandwidth (~100 pm) and the high temperature sensitivity that changes the resonant condition. [121]

2.4.3 PIN Diode

Direct bandgap semiconductors can be exploited to fabricate compact, fast and cheap modulators, thanks to the FKE. In this case, the change in absorption with electric field enables direct amplitude modulation. The device is a PIN diode (Figure 2-25) realised in a fraction (< 100 µm) of the waveguide and driven at reverse bias; there is no need of external support circuit and the standard CMOS process simplifies dramatically fabrication. At zero bias, the built-in electric field causes only a limited electro-absorption effect on the propagating optic mode, whereas at reverse bias the FKE is strong.

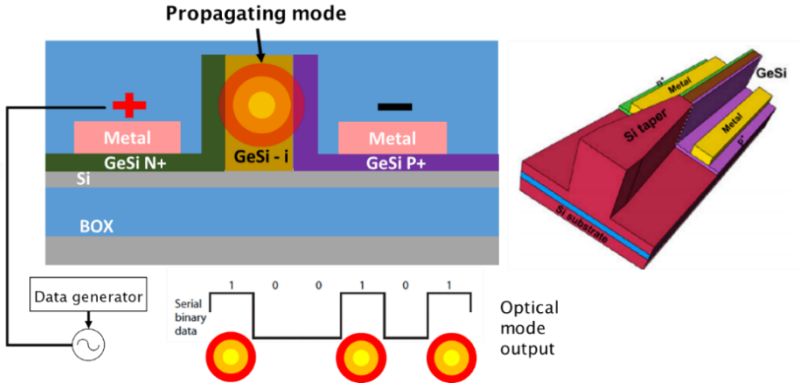

Figure 2-25 PIN FKE modulator cross-section and perspective view, reproduction from reference [30]. The encoded electric signal (bit-1/bit-0) is translated in optic by changing the material absorption with the PIN diode integrated in the waveguide and controlled through the metal pads. The amplitude modulation is obtained directly from the bitstream signal.

The compact device footprint (~60 µm^2), the extremely low power consumption (< 50 fJ), the high rate (> 50 Gbps) and the polarisation independency counterbalance the reduced operation bandwidth (~ 35 nm) intrinsically inherited by the FKE wavelength range and chirp mostly due to weak electro-refraction effect. Engineering the active material [124][125][126] to develop a matrix of devices working at different wavelength to extend the bandwidth while keeping the footprint compact, can be a practical solution.

MQWs allow to exploit the Quantum Confined Stark Effect [127] using PIN diodes, a stronger field effect that can be engineered for operation in the O-band or C-band, at the cost of a more complicated fabrication process (Figure 2-26).

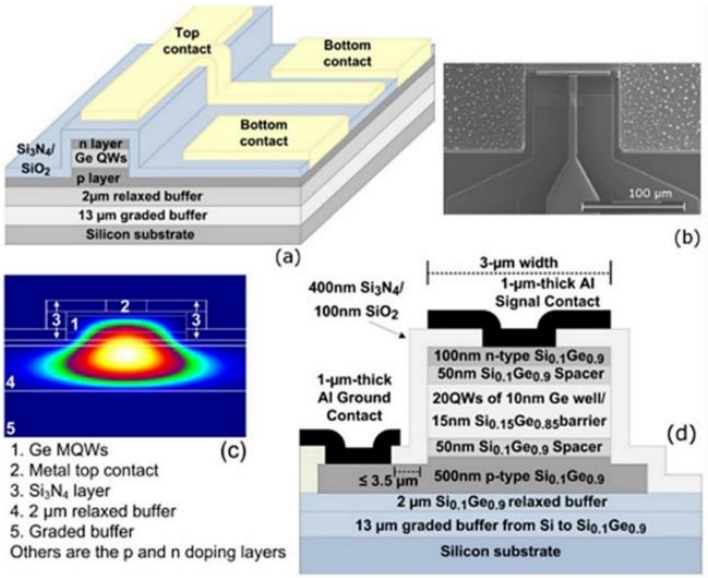

Figure 2-26 (Left) Cross-section and electric field distribution, reproduction from reference [127]. The PIN diode is formed with the vertical QW stack.

2.5 Summary

Following motivations and development of silicon photonics, this chapter focuses on theoretical backgrounds in the attempt to frame the status of current modulation technology. Basic info on group-IV materials compatible with CMOS fabrication lines are discussed. Both indirect bandgap semiconductors, silicon and germanium share the same crystal structure and yet they are very different optically. Silicon, with a direct bandgap at 3.4 eV (0.36 μm) allows to realise waveguides on SOI with loss of about 0.89 dB/cm [45] and 1.9 dB/cm at $\lambda = 2$ μm [46]. Germanium, on the other hand, absorbs light from 1.55 μm, thanks to the direct bandgap at 0.8 eV and thus can be used as the active material in micrometre devices for communication, whose optical characteristics are tuned by varying the alloy composition and/or strain.

The optical link was then examined in its principal aspects, the transceiver and the channel. Belonging to the first one, the SerDes serialise/deserialise information, the transmitter converts the data in to a signal compatible with the channel and the receiver is used to recover the data into its original form. Both transmitter and receiver were analysed in their fundamental components. Part of an optic transmitter, the CDR recovers the clock from the serial electric signal, whereas the optical source and the modulator convert the high-speed (serial) electric signal into optical before transmission in the channel. Part of the receiver, instead, the fast photodiode converts the pulsed light back to electric; the

amplifier (TIA) transforms the photocurrent into a usable pulsed voltage signal and the CDR recovers clock and signal before signal conversion from serial to parallel with a reversed SerDes. Finally, the optic channel was introduced and the communication bands were defined with respect to current applications. The dispersion-free O-band is common for short reach connections and the low attenuation C-band is adopted for long haul. Furthermore, a modern datacentre layout was introduced to point out the necessity of C-band interconnects also for short reach communications to cope with the demand for fast and low latency interconnects.

In the second part, modulation techniques and the commonest devices used in near IR interconnects were investigated. The well-adopted PDE has strengths including, but not limited to, big operation wavelength range, simple implementation, high speed and CMOS compatibility. Its drawbacks are the weakness of this effect in silicon, the big footprint and power budget. Footprint and power are an issue especially for amplitude modulation with MZI structures. Resonant cavities, on the other hand, reduce size and power demand at the cost of operation bandwidth limited to few a picometres. Then, absorption-based modulations were reviewed. The FKE in bulk semiconductors was described, implemented with a simple PIN junction, offering fast modulation with compact footprint and low power consumption, whose limits were found to be the small operation bandwidth and chirp. The QCSE in nanometric structures offers stronger field effect than that of FKE at the cost of a more complicated fabrication process. Other non-linear modulation principles were briefly presented to give a full review of current technology available in silicon photonics.

Chapter 3

Group IV Modulators

The physics behind CMOS optic modulators, and commonest designs have been given in the Chapter 2. In the first part of this chapter, standard metrics are defined, allowing to compare electro-optic and power efficiency of different modulators. Then, recent advances in modulators are presented in a series of tables to highlight advantages and disadvantages of the three main technologies available, PDE, QCSE and FKE; in the last table, the device fabricated for this project has been included to provide an easy comparison with similar devices.

3.1 Standard Metrics

It is important to define common metrics to assess performance of devices that differ in design and operation. The fundamental electro-optic metrics are classified in DC and AC groups. Belonging to the first group (DC) are modulation efficiency $L_\pi V_\pi$ for phase modulators, Insertion Loss (IL), modulation depth or Extinction Ratio (ER) and dark current; whereas in the second group (AC) are Dynamic ER, rise time, power consumption, 3dB Bandwidth.

3.1.1 Modulation Efficiency $L_\pi V_\pi$

In phase modulators, the modulation efficiency defined as $L_\pi V_\pi$ is the product of the voltage by the phase shifter length needed to reach π phase shift in the propagating optic

mode. The design, generally optimises the $L_\pi V_\pi$ to lower the modulator power budget by reducing V_π and/or footprint with shorter L_π. Large modulation efficiency (small $L_\pi V_\pi$) is achieved by maximizing the overlap between the optical mode and the active area [120].

3.1.2 Insertion Loss and Extinction Ratio

Transmission spectra measurements are performed to find the total optic loss (Insertion Loss) between the light source and the detector. IL comprises material absorption, propagation loss, interface loss, surface loss, mode coupling loss and scattering. Mathematically it is defined as the ratio of the received signal power (P_R) over the transmitted signal power (P_T):

$$IL\ (dB) = 10Log(P_R/P_T) \qquad \text{Eq. 3-1}$$

The optical properties of the device are, then, tested while applying the external electric field to evaluate the physical effect involved in modulation. The ER isolates the electro-optic field effect by measuring the ratio of the optical power of the modulated signal in the high (P_0) and low (P_1) level [128]:

$$ER\ (dB) = 10Log(P_0/P_1) \qquad \text{Eq. 3-2}$$

The design tackles low optical losses (IL) and enhancement of the electro-optic effect (ER).

3.1.3 Dark Current

In Figure 3-1a, the cross-section of the Electro Absorption Modulator (EAM) [30] shows the dark current defined by current flowing on surface paths of the device (black) due to poor passivation layer and bulk current (yellow) due to minority carrier recombination in the depletion area and bulk diffusion current [129]. Threading dislocations, by acting as traps and recombination centres in the depletion region, increase the bulk current [61][129] which is proportional to the device area. The surface current, proportional to the device perimeter is, however, the main contribution to the total dark current [129]. High dark current reduces performances and reliability of modulators by increasing the static power consumption.

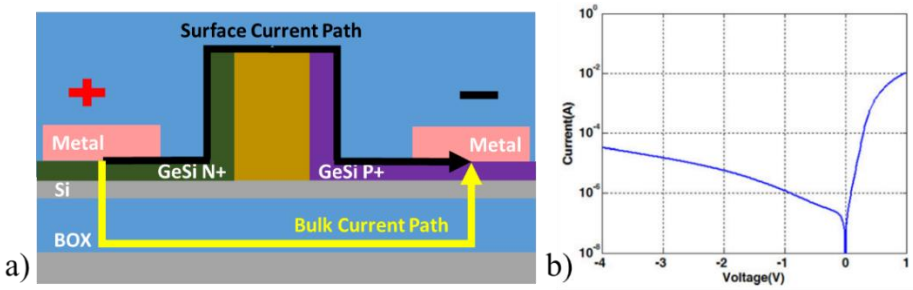

Figure 3-1 (a) Cross-section of the device in reference [30] showing the dark current, mainly due to crystal defects and surface roughness, generates from bulk (yellow) and surface (black) current paths. (b) The IV curve, reproduction from reference [30], is measured from the diode by slowly sweeping the bias.

Electric response to a slowly varying bias, as shown in Figure 3-1b, is used to assess the total dark current at specific bias.

3.1.4 Dynamic Extinction Ratio

Modulation performances are evaluated by sampling the modulated signal coherently with the driver clock. The samples associated to a single bit (or baud if a signal represents multiple bits) are superimposed to generate an eye-diagram [130] similar to that of Figure 3-2.

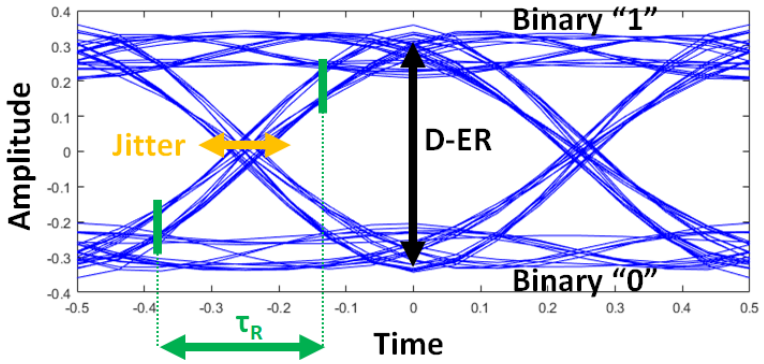

Figure 3-2 Transmission Eye generated with Matlab®. The Eye diagram results from the overlapping of the received signals sampled with same clock as the transmitter, Jitter, ER and Rise Time are defined graphically.

From the eye-diagram (Figure 3-2) it is possible to measure the Dynamic ER (ER-Dyn), which is the modulation depth between the high and low signal level and ultimately defines the quality of the modulator in terms of Bit-Error-Rate and speed. A high ER-Dyn, providing better amplitude separation between the two signal levels reducing the chances of data misinterpretation (BER), permits longer transmissions and/or higher bitrate. The Jitter (deterministic) is the deviation of a transition from the transmission clock, it "closes" the eye diagram (ER-Dyn), hence is detrimental. The transition time of the signal from the 10% to the 90% of its peak is called Rise Time (T_r), the smaller the T_r the faster the device.

3.1.5 Power consumption and 3dB bandwidth

Power consumption and maximum working frequency are found by measuring the Scattering Parameters [131] and evaluating, through simulations, the equivalent small signal electric circuit, which approximates the device with lumped linear elements, chosen to model the current paths in the device. From S-Parameters the input port voltage reflection coefficient S_{11} is measured for a frequency range, then numerical fitting is executed to match its amplitude and phase with those simulated using the equivalent circuit. As an example, in Figure 3-3 the EAM from reference [30] is modelled with six lumped elements, R_S is the junction resistance, C_j the junction capacitance, both modelling the junction current path; R_j models the surface current; R_{Si} and C_{ox} model the silicon substrate and box current paths, respectively. In Figure 3-4(a), the S_{11} curves (solid lines) are fitted (dashed lines) to calculate the lumped element dimensions. The power consumption is, then, found as the energy spent to send a bit: $P = C_j Vpp^2/4\ [fJ/bit]$, with Vpp the voltage swing.

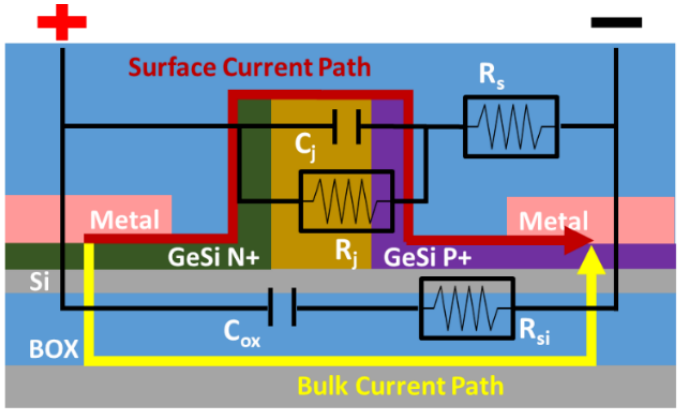

Figure 3-3 Example of small signal equivalent circuit from reference [30], the device is approximated with lumped linear elements to characterise the electric behaviour in frequency, the red and the yellow arrows represent the surface current and the bulk current path, respectively.

The 3dB bandwidth is found from the input port forward voltage gain S_{21}; in Figure 3-4(b) the device 3dB-bandwidth (35Ghz) is highlighted with the purple dashed line. Alternatively, the 3dB-bandwidth can be estimated by the relation $3dB = 0.35/\tau_r$ [132] with $\tau_r = \sqrt{\tau_o^2 - \tau_e^2}$, being τ_e the rise time of the input electric eye and τ_o the rise time of the output optic eye.

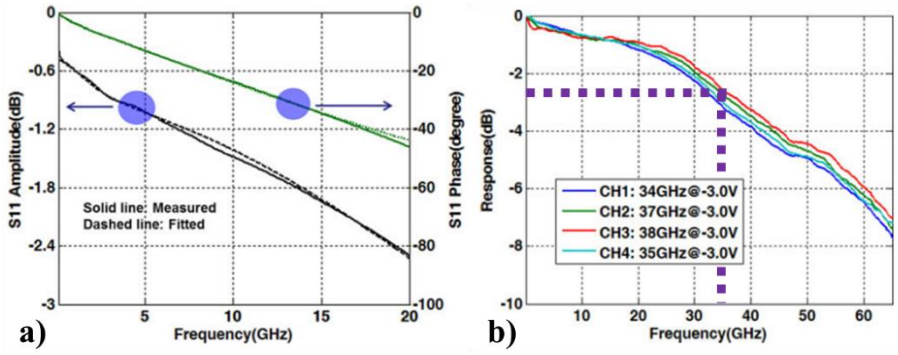

Figure 3-4 (a) S11 measurement reproduced from reference [30]. By fitting the S11 curves using the equivalent small signal cirtuit, the power consumption of the modulator can be estimated. (b) S21 measurement from reference [30], the frequency at which the response is reduced by 3dB defines the highest operating speed in Ghz of the device.

3.2 Literature Review

Three tables are presented trying to summarise the last decade of innovation in the field of optical modulators, using the metrics defined in section 3.1; in Table 3-1 standard silicon modulators based on the PDE are given, in Table 3-2 innovative QCSE based modulators are presented and finally in Table 3-3 the FKE based devices are compared. Although not already discussed, the performances of the first prototype developed in the University of Southampton are included into Table 3-3 for the sake of direct comparison with devices found in literature.

Tables have slightly different parameters depending upon the type of modulator and technology development. Specifically, $L_\pi V_\pi$ can be applied only to phase-based modulators, hence it is only in Table 3-1 and the device speed is missing in Table 3-2 (QCSE), simply because integration is still in development. Dark current measurements were found almost exclusively for the FKE based modulators. Common parameters to all tables are Technology, which describes the adopted design; Wavelength and Dimensions, referring to the operation point and area of the active section, respectively. In the Voltage section, DC bias and voltage swing (Vpp), are reported; similarly, in the ER section both DC (at bias voltage) and Dynamic (ER-Dyn) values are indicated.

3.2.1 Plasma Dispersion Effect Modulators

In the first comparison (Table 3-1), silicon PDE modulators operating in the C-band exhibit high speed (up to 64 Gb/s [133]) and large optical bandwidth [134], O-band operation can be, also, obtained [135].

Table 3-1 Recent progress in Silicon Plasma Dispersion Effect Modulator.

Reference	Technology	Wavelength [nm]	Area [μm²]	3db Band [GHz]	Speed [Gb/s]	Voltage [V]	LπVπ [Vcm]	Energy [fJ/bit]	IL [dB]	ER [dB]
Thomson et al. [136]	MZI	1551.75	0.4 x 3500	-	50	6.5 (Vpp) - 4 (bias)	2.8	4200	7.4	3.1 2.2 (Dyn)
Zhu et al. [133]	MZI	1550	0.9 x 5000	-	64	- 4 (bias)	1.4	7100	8	21
Tu et al. [137]	MZI	1550.17	L = 4000	-	50	1.3 (Vpp) - 4.4 (bias)	2.4	59	4.2	4.44 (Dyn)
Wang et al. [138]	MZI	1550	0.5 x 1000	30	44	5 (Vpp) - 5 (bias)	1.62-2.05	2840	3.9	2.44 (Dyn)
Debnath et al. [134]	MZI	1558.8	0.4 x 500	42	25	6 (Vpp) 3 (bias)	1.53	-	26	20 3.65 (Dyn)
Yong et al. [135]	U-PN MZI	1310	0.7 x 2000	13	24	2.88 (Vpp) - 0.5 (bias)	46	-	2.7	2.2 (Dyn)
Meister et al. [139]	1D-PhC	1592	~15	-	10	3 (Vpp) 0.5 (bias)	-	15	4.5	11 (Dyn)
Baba et al. [140]	Ring Resonator	~ 1548	~ 0.4 x 15	25	50	1.96 (Vpp) 1.2 (bias)	0.28	-	5.2	4.58 (Dyn)
Dong et al. [141]	Ring Resonator	1551.84	15 x 3	11	10	2 (Vpp) -1 (bias)	1.5	50	2	15 6.5 (Dyn)

Mach-Zehnder Interferometer is a very popular choice among research groups, thanks to the well-established, simple and highly customizable process, whose drawbacks are found in the big footprint (~ mm^2), high operation voltage (up to 6.5 V [136]) and power consumption (7.1 pJ/bit [133]). More recently, an all-Si carrier-accumulation lateral MOS-capacitor modulator with a speed of 25 Gb/s (limited by process misalignment) has been demonstrated for the first time [134]. The high IL caused by passive structures, consisting of MMIs, waveguide bends and rib-to-slot waveguide interfaces can be reduced by improving the process. A Photonic Crystal (PhC) Fabry-Perot resonant cavity with a footprint of about 15 μm^2, power consumption of 15 fJ/bit and speed of only 10 Gb/s has been proposed [139], but PhC requires a more sophisticated and less tolerant process than MZIs. Ring resonator modulators are, instead, fast (50 GB/s), compact (footprint ~ 45 μm^2) [140] and very efficient [141]. Hybrid integration [142] and cascades of different sized rings [143] are also a viable solution to integrate transceivers with modulation speed up to 80 Gb/s. The bandwidth, however, limited by the resonance linewidth, is only few hundred of picometres per channel. A 48 μA DC current was demonstrated for the forward biased device in [140] and an extremely low current, less than 1 nA, for the reverse biased pin ring resonator in [141].

3.2.2 QCSE Modulators

In Table 3-2, results from QCSE devices are summarised. Experiments achieved staggering optical bandwidths ranging between the full O-band [144][145] and C-band [146][147] with low power consumption (8.25 fJ/bit [147]) and compact footprint (120 μm^2 [146]); the great advantage of these devices resides in the possibility of tailoring the electro-optic characteristics by varying the nanostructure design (dimension and doping). The absorption mechanism at the core of these modulators can be, also, exploited to realise fast photodiodes using the same design.

Table 3-2 Recent progress in Silicon QCSE Modulator.

Reference	Technology	Wavelength [nm]	Area [μm^2]	3db Band [GHz]	Voltage [V]	Energy [fJ/bit]	IL [dB]	ER [dB]
Rouifed et al. [144]	Ge/GeSi QW	1400	3 x 50	-	4 (Vpp) - 4 (bias)	22	3	4
Chaisakul et al. [145]	Ge/GeSi QW	1433 1444	3 x 90	23	1 (Vpp) - 3, - 4 (bias)	108	5.5 12	10
Edwards et al. [146]	Ge/GeSi QW	1550 1490	0.6 x 200	-	1 (Vpp)	- -	3.5-4.5 6.5-8	6.5 15
Roth et al. [147]	Ge/GeSi QW	1541	225 x 625	-	1 (Vpp) - 1 (bias)	8.25	-	3

Unfortunately to the best of our knowledge, no eye diagram measurements can be found in literature due to waveguide integration being still a work in progress. The only speed measurements found in reference [145] is on the photocurrent, assessing a 3dB bandwidth of 23 GHz.

3.2.3 Bulk Electro Absorption Modulators

Fully compatible with the silicon platform, EAMs can be integrated in Ge [31][148] and GeSi [30][149] where the silicon content shifts the operation wavelength range of Ge diodes from the L-band [30][149] to the C-band [31][148].

Table 3-3 Recent progress in Silicon Franz-Keldysh Modulator.

Reference	Technology	Wavelength [nm]	Area [μm^2]	3db Band [GHz]	Speed [Gb/s]	Voltage [V]	Dark Current [nA]	Energy [fJ/bit]	IL [dB]	ER [dB]
Liu et al. [149]	Pin Gesi	1550	0.6 x 50	1.2	-	3 (Vpp) - 4 (bias)	< 65	50	7.5	10
Feng et al. [30]	Pin Gesi	1550	0.8 x 50	38	28	3 (Vpp) - 3 (bias)	15.4 x 10^3	147	4.8	5.9 4.5 (Dyn)
Lim et al. [148]	Evanescent Pin Ge	1600	16	-	1.25	- 5 (bias)	-	-	9.6	10
Srinivasan et al. [31]	Ge on Si	1610	0.6 x 40	> 50	56	2 (Vpp) - 2 (bias)	< 47	12.8	4.9	4.6 3.29 (Dyn)
Mastronardi et al. [150]	Pin Ge/GeSi	1566	1.5 x 40	56	56.2	4 (Vpp) - 2.7 (bias)	2 x 10^3	44	10.6	5.7 5.2 (Dyn)

In Table 3-3, EAMs show high speed (up to 56 Gb/s), low power consumption (12.8 fJ/s) and low dark current (< 47 nA), while keeping a compact design (down to 16 μm^2

[148]). On the other hand, the optical bandwidth is small, ranging between 14 nm [149] and 35 nm [30]-[31]. In reference [151] a CWDM was implemented with an array of modulators to increase the optical bandwidth up to 80 nm speed which limited the speed to 10 Gb/s and led to power consumption of 5.82 mW per channel. Similarly to QCSE modulators (Table 3-2), EAMs can be used as photodiodes with no change in design process.

EAM FKE modulators in references [30][31][148][149] implement a horizontal diode, which limits the waveguide width to about 0.7 μm to ensure a sufficient electric field strength in the waveguide when the external voltage is applied. By developing an innovative vertical PIN diode, this project proposes a viable solution to bring electric field independency from the rib dimensions in an integrated, compact and fully customisable design, which reaches high speed operation with low power consumption, as highlighted in orange in Table 3-3.

3.3 Summary

This chapter scope was to show the best representatives of the last decade research on group IV optical modulators. Using metrics defined in section 3.1, it was shown pros and cons of three dominant modulator categories for the silicon platform were discussed: the PDE based modulators offer high speed, big bandwidth and footprint [136]. The promising performances of QCSE based modulators, offering operation in both O-band [144][145] and C-band [146][147] with footprint and power consumption comparable with FKE EAMs and the exceptional speed, small footprint and power consumption of bulk EAMs based on the FKE [149] [31]. However, offer in our view the best trade off in terms of compactness and performances for short range C(L)-band integrated silicon photonic transceivers for routing applications in datacentres.

In the pursuit to overcoming the small width-to-height aspect ratio limitation in the FKE EAMs found in literature, inherited by the adoption of a lateral PIN diode, this project developed an innovative wrap-around junction. Modelling, design, fabrication and characterisation are presented in the following chapters.

Chapter 4

Methods

Fabrication of the EAM was mostly accomplished in the Nanofabrication Centre of the University of Southampton (NCUS) on a SOI wafer with 3 μm thick buried oxide and 800 nm thick silicon overlay; the outsourced steps were the active layer deposition and the material doping, only. Material characterisation during fabrication helped in developing recipes and controlling each process step. Device characterisation, instead, was important to assess the device DC and high-speed performances. In this chapter computer-aided design tools are first introduced, then fabrication and characterisation methods are discussed.

4.1 Design Tools

The device was simulated electro-optically to assess modulation performances in relation to device dimensions, doping concentration and alignment. Two software programmes were used together: Silvaco™ TCAD [152] to simulate the fabrication process and electric characteristics of optoelectronic devices and Matlab® [153] to solve the optical mode and evaluate the FKE in DC and high-speed. Additional simulations for designing grating couplers, tapers and evaluating side effects due to etch rate and angled interfaces were performed using Lumerical MODE and FDTD Solutions [154][155]. Once the device design was set, fabrication masks were drawn with Mentor Graphis L-Edit [156]. This section presents the main characteristics of these software, the models and methods applied in the simulations.

4.1.1 Device Process and Electric Simulation in Silvaco TCAD

Silvaco™ TCAD is a software suite that provides semiconductor process and device simulations. In this project three modules have been adopted Devedit™, Athena™ and Atlas™. With Devedit™ [157] device cross-section meshes are defined using a building block approach, regions are implemented as functional blocks with fixed characteristics such as dimension, material, doping. Athena™ [158], on the contrary, is a powerful tool to simulate fabrication processes by defining recipes that mimic the same procedures of a standard CMOS fab. Using masks and lithography steps, the device cross-section is built bottom-up, allowing investigation of side effects (doping diffusion, over etch) during process steps, comprising cavity etch, material growth, doping implantation, annealing and metallization. The device mesh is refined with Devedit™ before calling Atlas™ [159], a device framework engine for simulating the electric field distribution while applying a DC or a transient electrical signal.

4.1.1.1 Deposition method

Different models were used for defining the GeSi layer. In Devedit™ the alloy was defined directly as GeSi by adding the Ge fractional composition. In Athena™, instead, to simulate the effect of Ge concentration on the alloy characteristics such as diffusivity of boron, the alloy was deposited with the MODEL.SIGEC FULL.CPL. In this case the alloy was deposited as silicon with Ge dopant concentration proportional to the silicon undoped atomic density, equal to 5E22 cm^{-3}. For an alloy with 98.5% of Ge, though, the deposit command would include a Ge concentration of 4.925E22 cm^{-3} [160]. In both Devedit™ and Athena™ alloy definition, material properties of GeSi were numerically obtained from Ge and Si interpolation.

4.1.1.2 Etch model

In the case of the Athena™ process, etching steps were considered as geometrical problems simulated at low temperature while impurity redistribution was neglected, the etch region was defined in dimensions and thickness [161] with commands to start the etch in specific regions and stop at specific heights.

4.1.1.3 Implant method

During device definition through the process-oriented engine Athena™, the implantation steps were defined with the command IMPLANT. Controlling input were the dose of dopant, acceleration energy of dopant, tilt and rotation angles and number of ions. The implantation geometry is depicted in Figure 4-1, the tilt angle θ is defined between the incident direction of the implantation beam and the normal to the wafer surface. The rotation angle ϕ is between the implantation plane α and the surface plane Σ taking the wafer major flat as reference. More details on the implant process are given in section 4.2.6. The Crystalline Monte Carlo model [162] also known as Binary Collision Approximation (BCA) [163], was used.

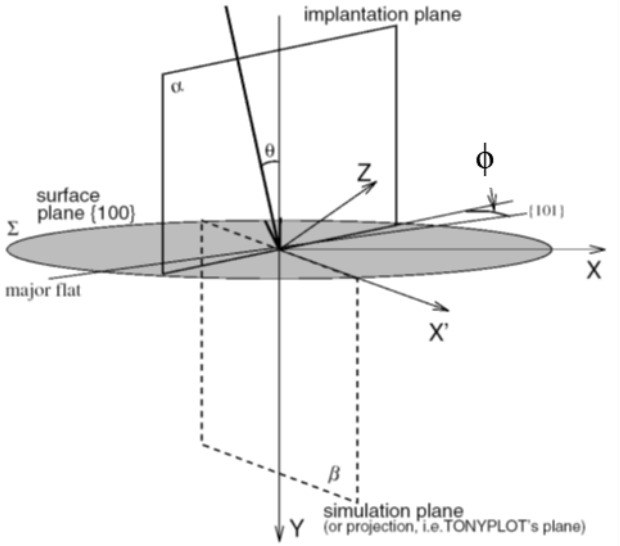

Figure 4-1 Implantation geometry, reproduction from reference [163].

The algorithm permits to simulate ion implantation in non-standard conditions such as structures with many non-planar layers with accuracy close to analytical models for monolayer structures [163]. The ions are launched towards the target, the algorithm follows the velocity decay of ions until they leave the target, or the kinetic energy is below a predefined threshold.

4.1.1.4 Diffusion model

Implanted dopants and defects distribution change if annealing is performed. In Silvaco the DIFFUSE statement allows to simulate the effect of time and temperature dependent diffusion processes [164]. The diffusion simulation uses different models all considering that a dopant atom can diffuse only in the presence of a point defects (lattice vacancy and/or interstitial vacancy). The diffusion simulation follows the continuity

equation for which the rate change of particles in a unit volume is the sum of the particles leaving the volume and those created or annihilated in the volume [164].

4.1.1.5 Bandgap Narrowing Model

In case of highly doped semiconductors (>1E18 cm^{-3}), an effect called bandgap narrowing occurs [165], which reduces the thermal energy required to create an electron-hole pair [166]. In an undoped material at zero temperature, all electron states in the VB are occupied by electron and the smallest energy to form an electron-hole pair defines the material bandgap. In a n-doped material, instead, extra free electrons in the CB can be found due to ionised donors, that interact with crystal electrons. Other interactions might occur within the free electrons and between electrons (or holes) in the VB and the ionised donors or between electrons in the VB and the free electrons. All these interactions affect the electron states in CB and VB, the self-energy [167] of a CB state is negative whereas the self-energy of a VB state is positive. Thus, the overall effect reduces the energy bandgap [168]. In Silvaco, this effect is taken into account by the model BGN [165].

4.1.1.6 Carrier Generation-Recombination Models

Upon perturbation, a semiconductor naturally attempts to return to an equilibrium state with processes involving generation and recombination of carriers [169]; among them for this project it was considered the Shockley-Read-Hall recombination (SRH) and the Auger effect [169] to better simulate the junction electrical behaviour.

In the presence of defects in the crystal lattice or dopant, additional energy states can be found within the material energy bandgap, which mostly account for non-radiative recombinations. During a carrier transition between bands, in fact, those intermediate energy levels in the bandgap might trap electrons with an exchange of energy in the form of lattice vibrations. This effect, called Shockley-Read-Hall recombination [170], [171], is modelled in Silvaco with the SRH command. Since SRH absorbs momentum difference of carriers, it is dominant in indirect bandgap semiconductors and on direct bandgap materials with low carrier density. The dependency of SRH carrier lifetimes on the dopant concentration can be considered [172][173][174] by including the model CONSRH.

In Auger recombination [175] the energy excess from a carrier recombination is given to a third carrier that goes to an excited level within the same energy band; at the end of the process, the energy is released as phonon [176]. Auger recombination may affect

both electronic and photonic devices, in Silvaco this effect is included with the model AUGER.

4.1.1.7 Mobility models

Carriers, accelerated by the electric field, lose momentum due to scattering processes. Carrier mobility is dependent on local electric field, lattice temperature, doping concentration, etc [177]. For simulations, a low-field mobility look up table (CONMOB) was included to relate the low-field mobility at 300 °K to the impurity concentration; to increase accuracy a parallel electric field analytic model (ARORA) [178] that takes into account the silicon electron and hole mobility dependency from the doping and temperature, was used.

Carrier velocities starts to saturate for high electric field strengths. The Caughey and Thomas expression [179] was used to account for any type of velocity saturation effect, the model FLDMOB [180] was used.

4.1.1.8 Impact Ionization Model

Impact ionisation happens when charged carriers loose kinetic energy by means of collisions within the material, generating extra charged carriers. In diodes, in the depletion region at high reverse bias, the accelerated minority carriers can generate other carriers by impact with atoms of the crystal if the electric field is strong and distance between collisions allows carriers to acquire high velocity [181]. Under high reverse bias, minority carriers with enough kinetic energy, in fact, may impact on bound electrons and break the bound, thus promoting them to a conduction state (creating an e-h pair). The extra carriers further generate more electrons from the atom by breaking the covalent bonds leading to an exponential increase of current at reverse bias, called avalanche breakdown. To account for this effect, the Selberherr's Impact Ionization Model [182] was included in the simulations.

4.1.1.9 Newton method

The standard solving method applied in the simulations was the Newton method [183] that finds successively better approximations to the roots of real-valued functions. Each iteration solves a linear version of the non-linear algebraic system; it is a high computational demanding method but it converges after few iterations if the mesh and

initial guess are properly defined [184]. In Silvaco Atlas, this method was implemented to solve the electric field distribution in DC and transient.

4.1.2 Optical Solver

Optical solvers were used to evaluate the TE mode distribution in the device cross-section in electro-optic simulations, assess the FKE in DC and transient, and to evaluate transmission spectra and coupling efficiency in passive devices. For FKE and absorption simulations in passive devices, a Matlab® function was implemented [185]. For coupling and conversion efficiency, Lumerical Mode Solutions [154] was used. For transmission simulation Lumerical FDTD Solutions [155] was adopted. In this section solvers are introduced, while in Chapter 5 their application is analysed in detail.

4.1.2.1 Matlab function

The principal optical mode solver chosen for this project is a Matlab® function (wgmodes [185]) available from Matlab® Exchange that implements the Finite Difference Method (FDM) [185] to calculate the two transverse magnetic field components H_y, H_x of a dielectric waveguide. Other field components can be evaluated in postprocessing. The input is the device cross-section mesh containing the complex refractive index value on each node, whereas the outputs are the magnetic field transverse components (Figure 4-2) and the effective refractive index, for evaluating the opticsl characteristics of the design.

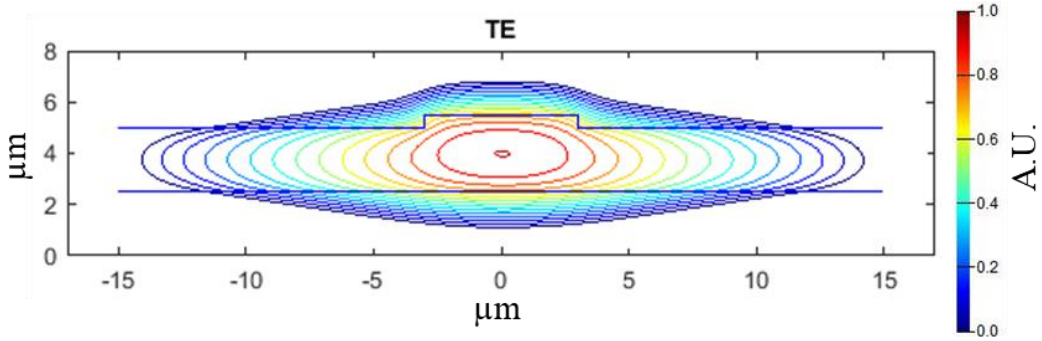

Figure 4-2 TE mode solution calculated with wgmodes [185] in a polymeric waveguide.

4.1.2.2 Lumerical MODE Solutions

Used for conversion efficiency and coupling loss simulations, Lumerical Mode Solutions [154] is a design framework based on an eigenmode solver for evaluating Maxwell's equations in waveguide structures. The electromagnetic fields are decomposed

in a set of local eigenmodes that exist in the device cross-section and are found from the solutions of Maxwell's equations calculated in each local cross-section [186][187].

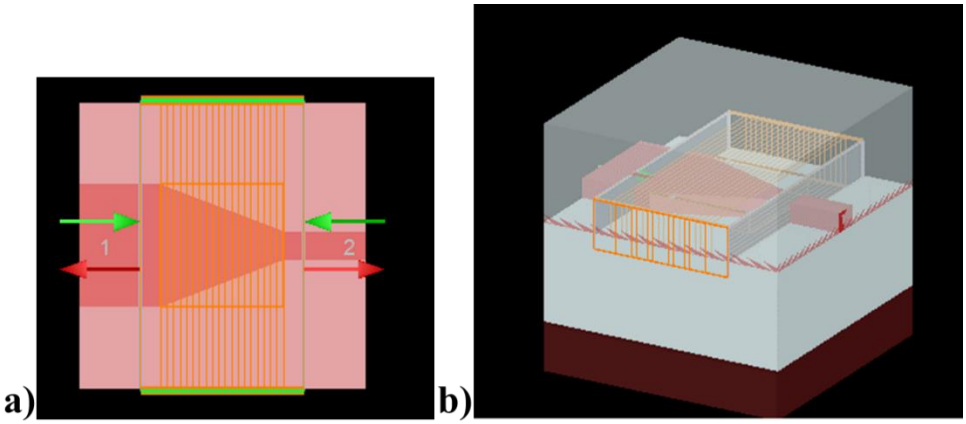

Figure 4-3 Taper simulated in MODE Solutions with EME solver, (a) top-view, (b) perspective view.

Waveguide tapering was required to fabricate single mode TE waveguides and for this purpose, the bidirectional eigenmode expansion (EME) technique available in MODE Solutions was applied [188]. This fully vectoral and bi-directional algorithm solves the Maxwell's equations in frequency, allowing evaluation of light propagation over long distances efficiently (Figure 4-3).

Propagation between waveguides of different materials is accompanied with losses at the interface generated by different refractive index, confinement factor (the power fraction in the waveguide core) and waveguide dimension. In this project devices were fabricated in cavities filled with GeSi and surrounded by Si; waveguides passing through the GeSi cavity were partially made of GeSi and partially of Si, generating a material and dimensional discontinuity due to the higher refractive index [50] and etch rate [189][190] of GeSi with respect Si. In Figure 4-4, the coupling efficiency simulation between a Si waveguide and a GeSi waveguide, is depicted.

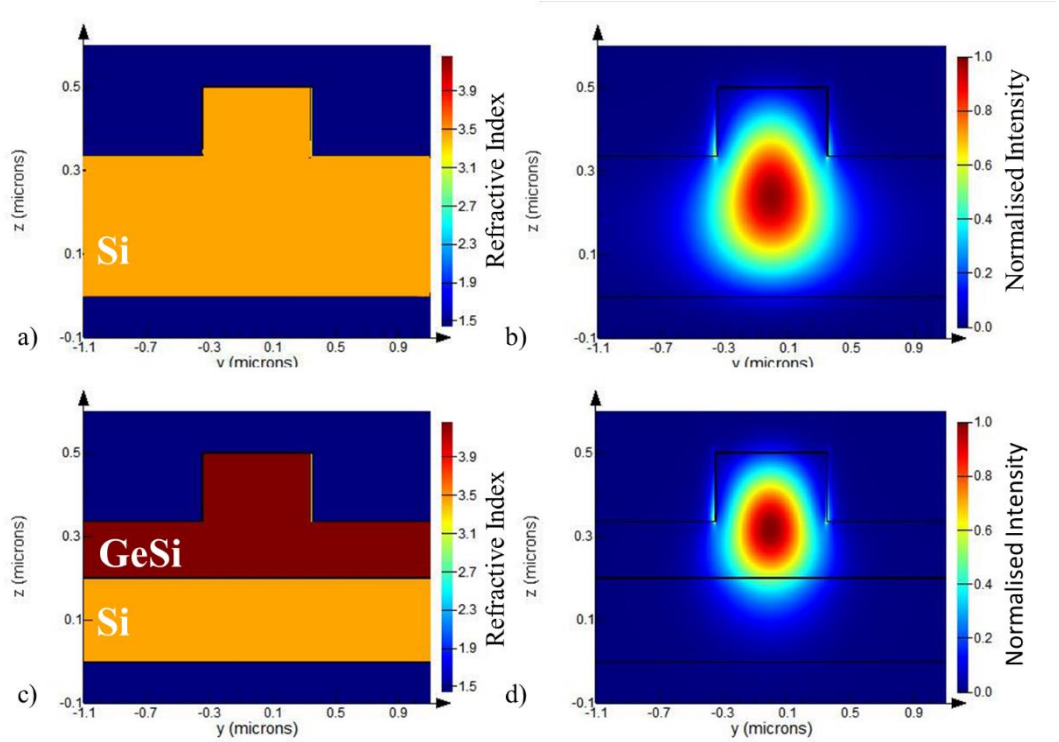

Figure 4-4 Structure definition and TE mode distribution for a Si waveguide (a, b) and a multi-layered waveguide (c, d).

The Si waveguide on oxide is defined (Figure 4-4a) and the mode distribution is calculated (Figure 4-4b), then a multi-layered Si-GeSi waveguide on oxide is defined (Figure 4-4c) and simulated (Figure 4-4d) as well. By applying the overlap analysis whose interface is shown in Figure 4-5, the percentage of optical power when light travels from one waveguide to another (coupling efficiency) is estimated. For this example a coupling efficiency of 0.8 is found (black box in the picture).

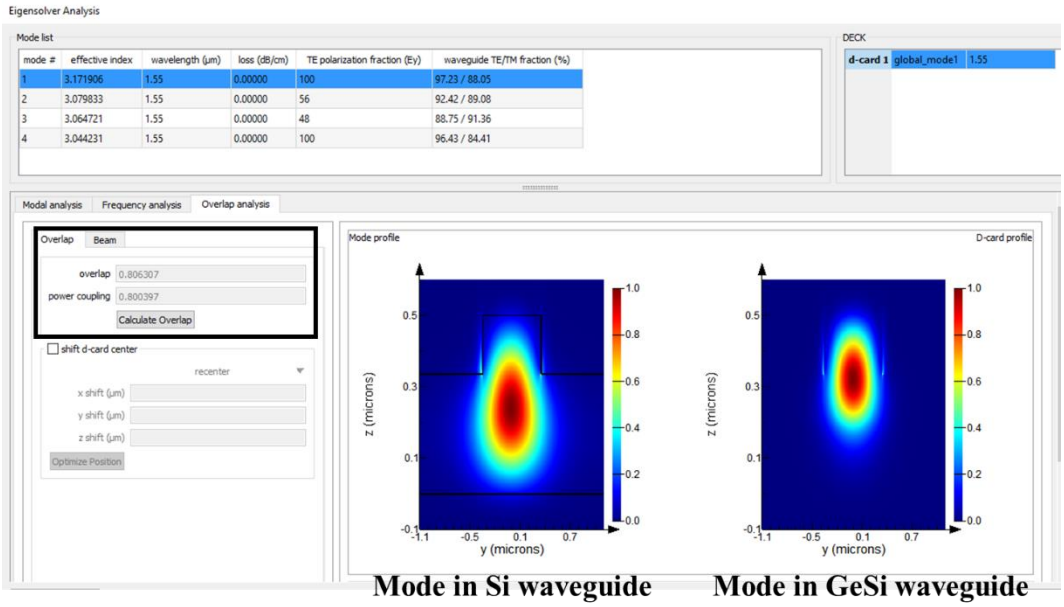

Figure 4-5 Mode overlap calculated in Lumerical Mode Solutions, the mode distribution is found in waveguide sections made in Ge and Si, then by calculating the mode overlap, the coupling loss between the two sections, is estimated.

More details on the simulations carried out with Lumerical MODE Solutions for this project are discussed in section 5.4.

4.1.2.3 Lumerical FDTD Solutions

FDTD Solutions [155], based on the Finite Difference Time Domain (FDTD) method [191] to solve the Maxwell's equations in the 3D space, allows to simulate device response in wavelength with the Fourier transform, taking into account material dispersion. Analysis of mode profile, loss, scattering, radiation, etc. are possible [192]. This method was applied for evaluating the transmission efficiency between angled interfaces and coupling efficiency of grating couplers (GC) used at input and output of waveguides to couple light from and to optic fibres.

Simulation of the fraction of optical power transmitted through the butt-coupled Si-to-GeSi waveguide is possible by building a 3D model, as shown in Figure 4-6. The simulation region is defined with the orange box, different boundaries conditions can be applied, by default the Perfectly Matched Layers (PML) are used. PMLs are fictional absorbing layers for wave equations designed to avoid any reflection at its interfaces when a propagating electromagnetic wave hits the PLM. The PML absorbing boundary conditions have impedance matched with the simulation region and materials [193].

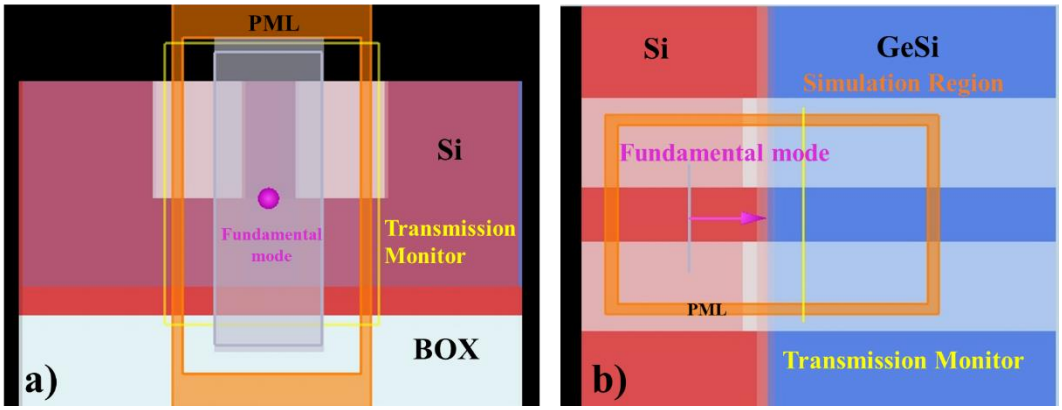

Figure 4-6 Cross-section (a) and top-view (b) of the butt-coupled Si-to-GeSi waveguide.

A propagating mode is defined in the structure (pink arrow in Figure 4-6b), different options are available among those the fundamental mode can be set with its geometry and for a range of wavelengths defining the simulation spectral window. The FDTD engine solves the electromagnetic problem in time and space allowing to evaluate the mode field distribution, the effective refractive index and the mode power in any point of the FDTD region by adding monitors (yellow line in Figure 4-6b), allowing to evaluate the transmitted power (transmission spectrum) from the source to the monitor location.

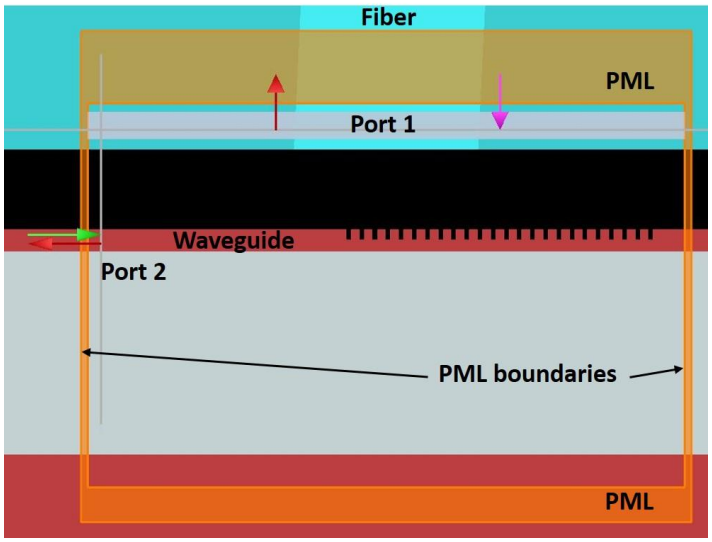

Figure 4-7 Grating coupler lateral view, reproduction from reference [194].

Coupling efficiency between optic fibre and GC can efficiently be evaluated in FDTD. The simulation structure is depicted in Figure 4-7 from reference [194]. Port 1 is the optic fibre that can inject or collect light from/to the GC, port 2 is on the left side of the waveguide that can be also used at input or output port. Design parameters such as waveguide thickness, grating period, duty cycle, etch depth and optic fibre position affect the coupling efficiency. Simulations in wavelength with the FDTD method are then

executed to evaluate the transmission and reflection spectra in order to define the GC design that maximise the power coupling from the optic fibre to the Si waveguide, and vice versa.

Transmission and coupling efficiency simulations with Lumerical FDTD Solutions are presented in section 5.4.

4.1.3 Mask Design Tool

More than ten different process masks have been developed during this project. From the wafer top-view, device and testing structures are realised by overlapping different layouts that define etching and doping regions with nanometric accuracy. In Figure 4-8a, the top view of a simple PIN junction fabricated on Si substrate is defined with four masks (Figure 4-8b), two layers define the doping regions P+ in green and N+ in red, a VIA layer to etch the thick cladding oxide layer deposited after doping wells definition and a final layer to form the metal contacts; the resulting cross-section is depicted in Figure 4-8c.

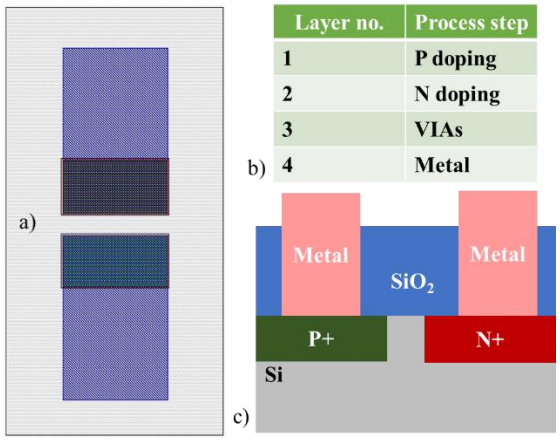

Figure 4-8 PIN diode top-view mask (a) defined with 4 layers (b), the device cross-section is depicted in (c).

The masks for this project have been realised with Tanner L-Edit IC Layout [156] a powerful IC layout software that maximises efficiency thanks to a hierarchical physical layout, support to industry standards, optimised performances with real-time design rule checking and support to macro coding. Exploiting C++ macros, in fact, design time of device variations was optimised by setting a matrix of variations. Details on the mask layout are given in section 5.5.

4.2 Fabrication

Fabrication of an active device requires several process steps, among them, deposition, doping, and etching require high accuracy. Fabrication, usually, starts with lithography, a technique for transferring the mask layout on the wafer. Two main techniques are commonly adopted, photolithography and e-beam lithography. UV photolithography, limited by the light wavelength, has lower resolution than e-beam lithography but is quicker because the whole wafer is exposed on the same time; e-beam, instead, by directly writing the wafer with an electron beam, achieves better resolution at cost of longer exposure time. In this work critical features were defined with e-beam, whereas features requiring only micrometric accuracy with photolithography. Etching with straight profile can be challenging especially for deep etches, in this project plasma etching was extensively adopted, whereas chemical etch was chosen for shallow etches and/or wafer cleaning. Deposition and doping require fine control to enable fabrication of active devices with aspect ratio and material characteristics close to design, epitaxial growth, doping implantation and CMP were the only fabrication steps outsourced. In this section the methods and tools adopted are presented.

4.2.1 Wafer conditioning

During fabrication, wafers were conditioned to remove any residual from a previous step or impurities. Cleaning of the wafers was conducted both/either with Hydrofluoric acid (HF) bath and/or plasma ashing (plasma clean). HF bath is also useful to remove the thin layer of oxide deposited as protecting layer, during fabrication. The Nanofabrication Centre of the University of Southampton (NCUS) is equipped with several wet benches and chemicals to run HF cleaning with any concentration.

Plasma ashing is a dry-cleaning process, in the furnace (asher) monoatomic oxygen ionised gas (plasma) is generated by an RF electromagnetic field in low pressure conditions. At high temperatures, ashing deep cleans the wafer, whereas at low temperatures, the descum process removes residual particles. The NCUS is equipped with the TePla Gigabatch Plasma Asher, a 2.45 GHz plasma asher equipped with O_2 and C_2F_6 gas lines.

4.2.2 Material Deposition

In this project, three material depositions techniques were used, the Plasma Enhanced Chemical Vapour Deposition (PECVD) for growing oxide, the selective Reduced Pressure Chemical Vapour Deposition (RPCVD) for depositing GeSi; and the metal evaporation adopted to deposit the metal contact stack comprising nickel, titanium and aluminium.

4.2.2.1 Plasma Enhanced Chemical Vapour Deposition (PECVD)

PECVD is a standard technique widely used to deposit thin layers of material by mean of chemical reactions with ionised gas (plasma); the working principle is shown in Figure 4-9 from reference [195]. In a low pressure chamber, the wafer is kept at constant temperature while gasses are introduced. DC and RF currents are then injected between the anode on top of the chamber and the cathode on the back of the wafer holder, ionising the gasses. The plasma reacts (chemical process) and/or decomposes on the substrate surface, depositing the required material. For depositing oxide, the chemical reaction in the chamber is [196]:

$$SiO_x{:}SiH_x + N_2O \rightarrow SiO_x\ (+H_2 + N_2)$$

Silane (SiH_x) and nitrogen (N_2O) react to produce SiO_x, chemical residuals are H_2 and N_2.

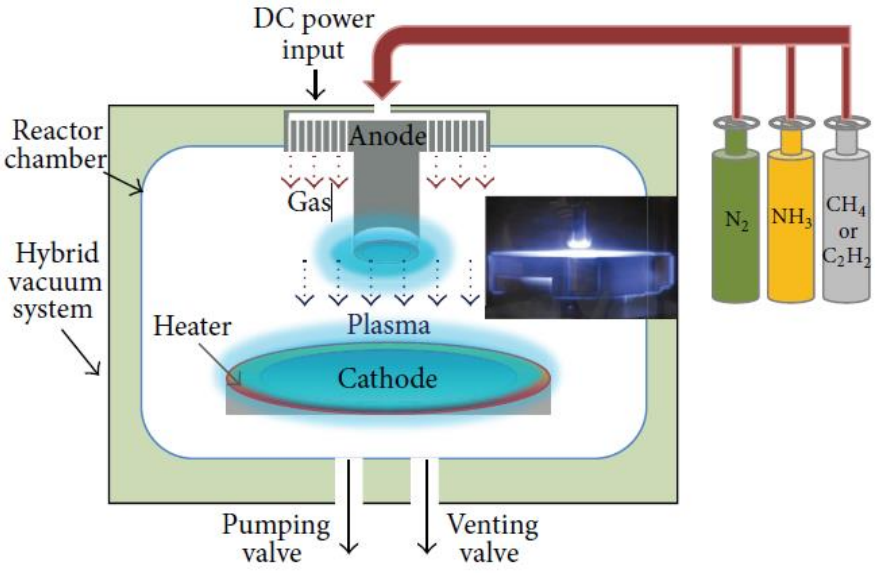

Figure 4-9 PECVD drawing reproduced from reference [195]. In the low-pressure chamber gasses are ionised with an RF current. The plasma reacts with the substrates and material is deposited.

The advantageous lower temperature deposition over other techniques that use high temperature is counterbalanced by an increased number of defects, including silanol (SiOH) and water [197]; substrate temperature, RF power, pressure and gas flow can reduce dramatically the impurity presence if accurately tuned [197]. The resulting layer is no-stoichiometric, with good uniformity and stress free if the RF frequency is varied during the process [198].

Oxide deposited with Oxford Plasma Technology 100 PECVD has been extensively adopted as cap layer (about 20 nm) to protect the surface during processing, as a passivation layer to reduce the surface dark current path improving the device DC and high-speed performances, as discussed in section 3.1 and finally as a thick protecting cladding layer. The various use of the different oxide layers are given in the device process flow in section 7.1.

To deposit SiO_2, the chamber pressure was set to 1000 mT, power to 20 W and temperature at 350 °C while a mixture of SiH_4 (4.2 sccm), N_2 (80 sccm) and N_2O (350 sccm) was flowing in the chamber. The oxide deposition rate was found to be about 1.133 nm/s; therefore, for depositing 20 nm oxide, a deposition time of about 20 s was chosen, for 100 nm oxide time was set to 1 min 14 s and for thicker oxide layer (475 nm) a depositing time of about 8 min was instead used.

4.2.2.2 Selective Reduced Pressure Chemical Vapour Deposition (RPCVD)

The active layer was deposited in cavities realised on the silicon overlay by means of Reduced Pressure Chemical Vapour Deposition (RPCVD) with a two-step growth. CVD technique is generally preferred to Molecular Beam Epitaxy (MBE) method because of the reduced particulate density in CVD reactors, producing films with higher uniformity than those done with MBE, in less time [66]. For this project the selective RPCVD technique was used. The actual recipe details are not known (the growth being outsourced), but the principle (applicable also in Ultra High Vacuum CVD, UHVCVD) is well described in references [65][66][199]. The growing process is depicted in Figure 4-10.

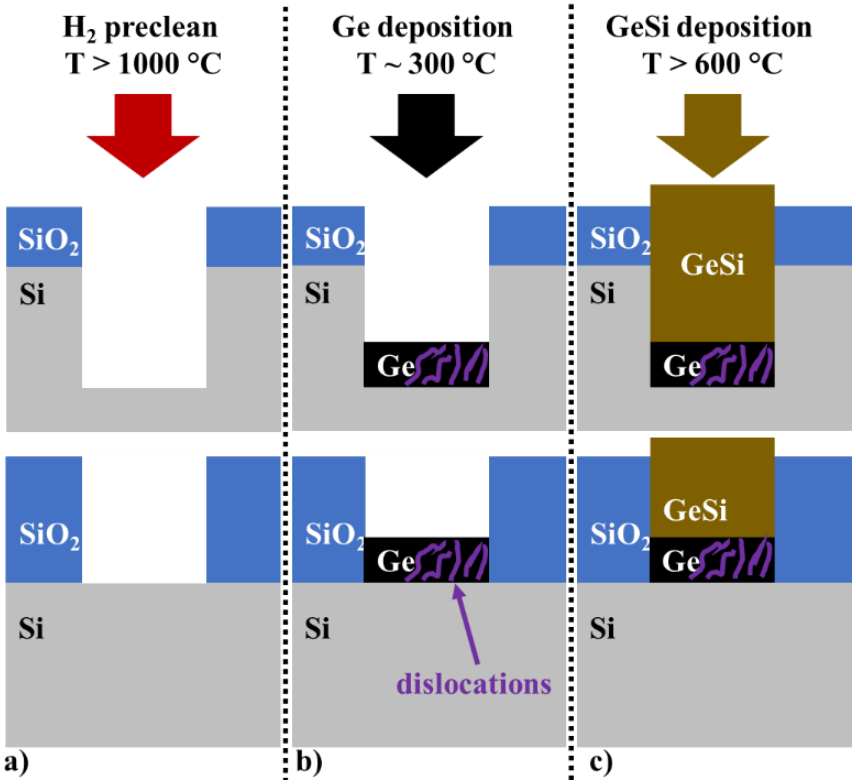

Figure 4-10 Selective RPCVD in trenches etched in Si overlay (up) or realised by depositing thick patterned oxide (down), the growth procedure is the same. Wafers are cleaned in H_2 to remove contaminant and native oxide on the exposed Si areas (a), then Ge is deposited at low temperature (~300 °C) in the trenches only, by tuning the deposition recipe (b). 3D islands are avoided, and a relaxed layer is obtained with dislocations (purple lines in the black Ge box). Finally, temperature is raised >600 °C and GeSi is deposited with lower TDD (c).

Wafers are patterned by etching trenches on the wafer overlay (Figure 4-10 up) or by depositing a dielectric layer (generally SiO_2) etched with patterns (Figure 4-10a down). Wafers are cleaned at high temperature (>1000 °C) to remove any contaminants and native oxide on the Si exposed areas (Figure 4-10a). The precleaning process, done at high temperature, can severely damage the wafer surface creating pits and consuming feature sidewalls if temperature, pressure and time are not set correctly [200]. In Figure 4-11a, from [200], before thermal cleaning the Si surface is smooth, SiO_2 features have sharp sidewalls; after 60 s precleaning at 1000 °C and 1.5E-4 Torr, the wafer surface presents several pits and the SiO_2 sidewalls are consumed.

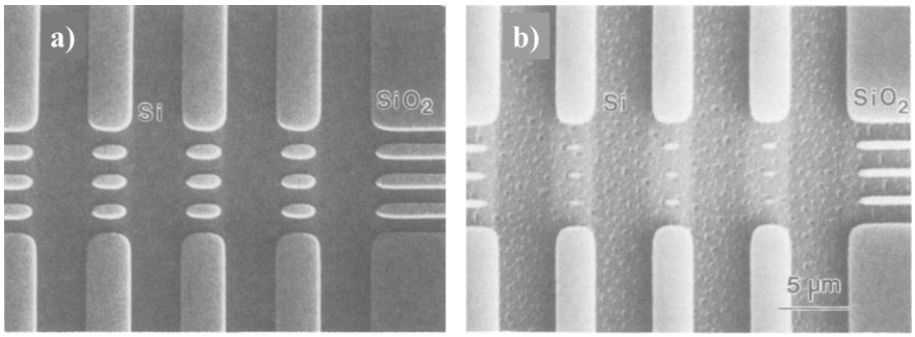

Figure 4-11 Precleaning process executed on Si wafer containing SiO_2 feature. (a) Before thermal cleaning surface is smooth and sidewalls sharp, (b) after 60 s precleaning at 1000 °C and 1.5E-4 Torr, surface damage and sidewall consumption are visible, reproduction from reference [200].

Surface damage, depending on the precleaning conditions, strongly affects the epitaxial growth. In reference [200] it was demonstrated that a correct preclean leads to a smooth and low density defect epilayer, on the contrary the epilayer shows rough surface when preclean is skipped. H_2 cleaning also induces smoothing of the sidewall edges of silicon features, due to self-diffusion of superficial silicon atoms at lower temperature than the silicon melting point (1412 °C at 760 Torr) [201]. In Figure 4-12 from reference [201], annealing in H_2 at 40 Torr for 3 min led to smoothing of sidewalls dependant on the temperature.

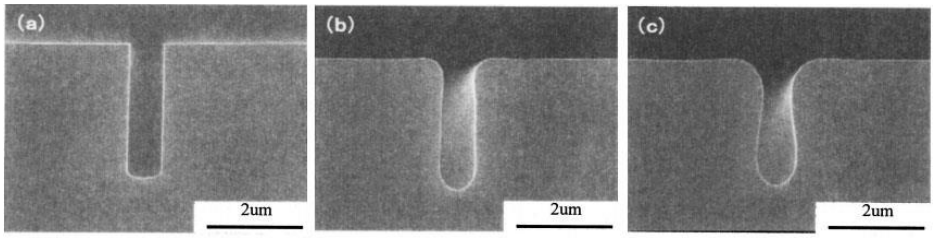

Figure 4-12 SEM of trench before (a) and after H_2 annealing with 40 Torr pressure for 3 min at 1000 °C (b) and 1100 °C (c), reproduction from reference [201].

In reference [202] rib waveguides were thermal annealed with H_2 at different temperature with pressure of 20 Torr for 1 min, resulting in slanted rib sidewalls caused by Si reflow dependant on the annealing temperature. In Figure 4-13a from reference [202], the rib waveguide before annealing is depicted, from (b) to (d) by increasing temperature the Si reflow increases deeply changing the waveguide cross-section. Using a SiO_2 hard mask to protect the rib waveguide, resulted in a reduction of Si reflow [202].

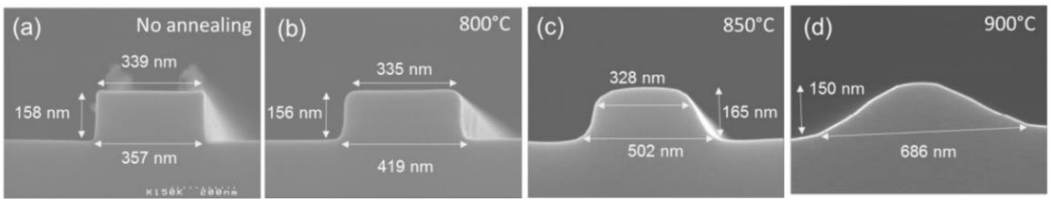

Figure 4-13 (a) Rib waveguide before H_2 annealing, (b)-(d) waveguide after annealing at 800 °C (b), 850 °C (c), 900 °C (d), at pressure of 20 Torr for 1 min. Reproduction from reference [202].

After cleaning, while keeping a low substrate temperature (300 °C), a germanium buffer layer of about 100 nm is grown (Figure 4-10b). A common gas in CVD is GeH_4 (germane) because reaction with SiO_2 generates volatile GeO_2 that is not stable at growing temperature, ensuring growth selectivity on the wafer [203]. Other sources have been tested to replace the toxic and hazardous germane, a liquid organic precursor the iso-butyl germane (IBGe) [204] and germanium chloride ($GeCl_4$) [66], for example. The growth condition is tuned for avoiding 3D Ge islands formation [203], a relaxed layer is obtained with formation of threading dislocations (TD) in the order of 1E7 cm^{-2} or less. In reference [205] TD density of 2.3E7 cm^{-2} for un-patterned wafers (RPCVD) and 2.3E6 cm^{-2} for patterned wafers (selective RPCVD) were obtained by cyclic annealing after Ge growth; in [66] thermal annealing was performed after Ge buffer layer deposition but before GeSi growing, reducing the TD density as low dark current values (~10^{-2} A/cm^2) suggested in IV measurements on diodes fabricated with that epilayer [66]. For this project, TD density between 2E7 cm^{-2} and 5E7 cm^{-2} [206] are expected due to the similar growth technique used in reference [206].

In the second step, growth at higher temperature (>600 °C) is performed to reduce dislocation formation and deposition time, while changing the plasma chemical composition to enable GeSi deposition (Figure 4-10c) [66]. Growth rate and Ge composition controlled by gas flow and temperature are also dependant on the Si coverage (portion of the Si overlay exposed) [207][208]; in reference [209] an extensive study on the relation between Si coverage and growth rate was proposed. The kinetic model of GeSi growth based on the classical boundary layer theory [210] is schematised in Figure 4-14, in which the gas flowing laminarly to the wafer is consumed by dangling bonds on the exposed areas, only after gas molecules diffuse through a stagnant region surrounding the aperture (purple and red semicircles). The stagnant region is due to frictions between the gas flow and the feature on the wafer, it depends directly on the gas viscosity and inversely on the gas velocity. If gas flows faster (lower pressure), the boundary layer moves towards the surface (red semicircle) and the depletion volume reduces so that less molecules are available for deposition, reducing the growth rate; if gas flows slower (increased pressure), the boundary region expands (purple semicircle) hence more molecules can diffuse through the boundary layer and deposit on the layer, increasing the growth rate.

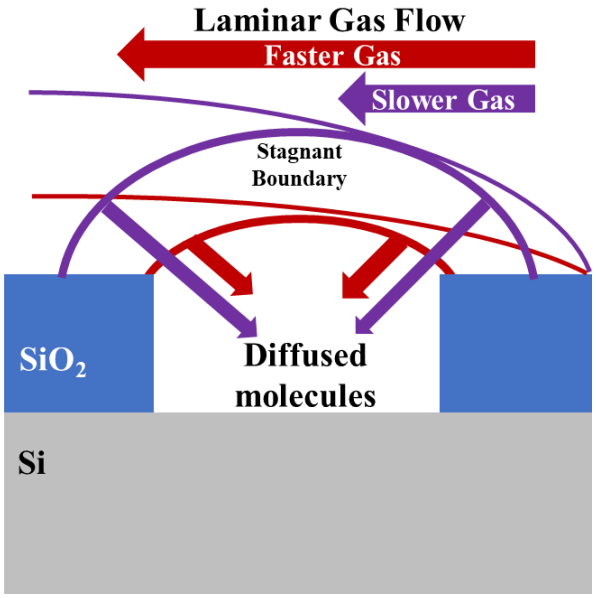

Figure 4-14 Classical boundary layer theory, the gas flows laminarly above the wafer (red and purple arrows), a stagnant boundary region is formed on top of the trench depending on gas velocity (purple and red semicircles). If gas flows slowly (purple) the boundary region (purple semicircle) is bigger, therefore more molecules can diffuse through the boundary increasing the growth. If the gas velocity is high, the stagnant boundary is small (red semicircle) reducing the number of molecules available for deposition, reducing the growth.

In reference [209], it was proved that the growth rate and composition are not dependant on the feature shape or size, only on the total coverage. The interactions between chips with differently sized designs was also demonstrated, suggesting that designing dummy features on the wafer to maintain constant the coverage on the entire wafer, or calibrating the growth with a reference sample containing differently sized features, would improve the layer growth uniformity. For this project, the first approach was chosen to get good uniformity and growth rate.

4.2.2.3 Chemical Mechanical Polishing (CMP)

CMP is a process to planarize surfaces with chemical and mechanical action [211]. In this project it was used after the selectively GeSi growth in cavities to remove the excessive material accumulated on the Si overlay and planarize the cavities. An abrasive and corrosive chemical, called slurry, is deposited on a polishing cloth that rotates; the wafer, held on another rotating support, is pressed against the ring obtaining a planetary rotation. The tool schematic is depicted in Figure 4-15 .

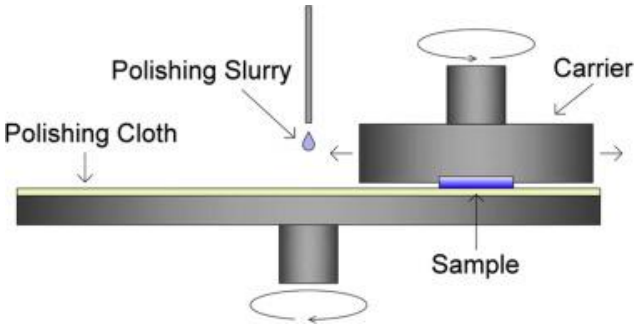

Figure 4-15 CMP schematics reproduced from reference [212], a planetary movement of the sample is obtained with the carrier and plate rotation. Polishing slurry is poured while the tool operates.

Downward pressure, rotation speed and slurry composition determine the material etching rate; however, material thickness and feature size greatly change CMP speed and final result. Sparse features with different dimensions will result in a non-homogeneous CMP with bigger features etched faster than smaller ones, dishing and erosion may also occur [213].

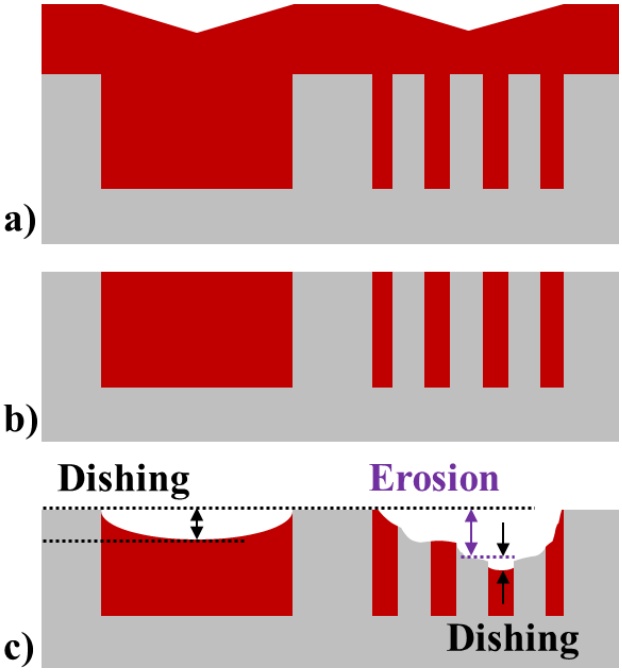

Figure 4-16 (a) wafer before CMP, (b) wafer after CMP in ideal conditions, (c) dishing and erosion in real CMP process.

An example of the CMP process is depicted in Figure 4-16. Material (red) is deposited in cavities with an overgrowth covering the entire wafer (Figure 4-16a) in a non-selective process. After CMP, the ideal situation is shown in Figure 4-16b, cavities are fully filled with materials and the thickness is conformal. In a real CMP, however, the polishing cloth is not completely rigid neither flat so that can bend easily, removing more material in wide features (Figure 4-16c, cavity on the left), this effect is called dishing [214]; when

feature density is high, erosion [214] is likely to happen, for which small gaps under higher pressure are washed away, reducing the height of the trench (right feature of Figure 4-16c).

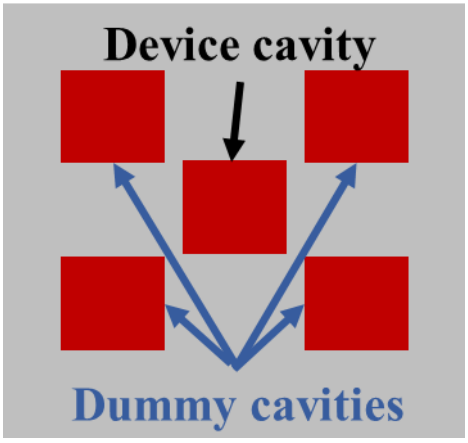

Figure 4-17 Top-view of the wafer with dummy cavities surrounding the device cavity.

Uniform density distribution is sought to prevent or alleviate dishing and erosion by adding dummy features in the layout [213]. In this project, though, cavities were realised on the Si overlay spread on the wafer area to ensure good uniformity growth, each device cavity was surrounded by four dummy cavities to ensure conformal CMP (Figure 4-17). The CMP step was outsourced to the VTT Technical Research Centre of Finland [215].

4.2.2.4 Metal Evaporator

In the final step of the process, a layer of metal is deposited using evaporation; the tool and the physical principle are depicted in Figure 4-18a.

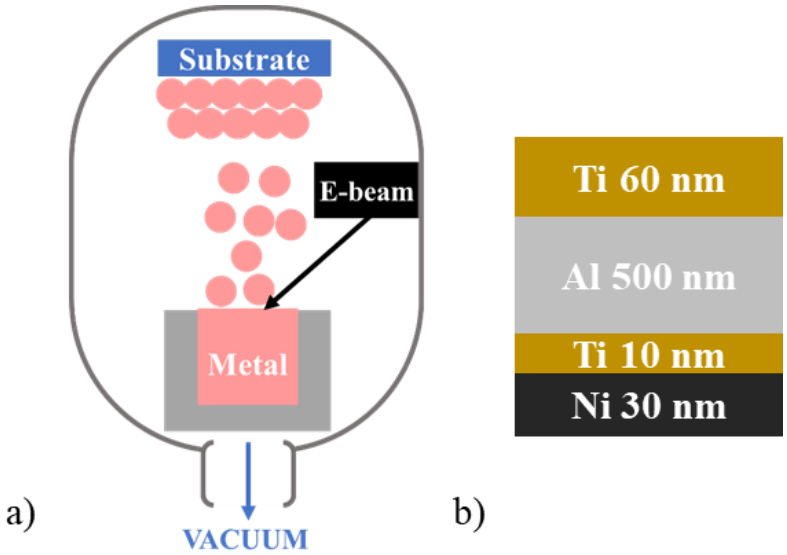

Figure 4-18 (a) Evaporator drawing, the metal is heated up until evaporation through an e-beam gun, metal particles then travel upward where the substrate is located. With pressure below 10^{-5} mBar and smooth substrate surface, an even thin metal film can be deposited. (b) Metal stack deposited in this project, Ni was deposited to form GeNi to reduce contact resistance, Ti was used to avoid metal diffusion and as capping layer, Al was used to reach the surface.

In a furnace kept at pressure below 10^{-5} mBar the metal is heated up with an e-beam source until evaporation; the metal particles, then, deposit on wafers held on the top of the furnace upside down. The film quality highly depends on the pressure, low pressure permits molecules to travel directly to the target (wafer) and deposit evenly, otherwise deviation from the trajectory due to collisions and chemical reactions with air might happen, resulting in a non-uniform and rough film. The tool used was the Leybold LAB700EB Evaporator DV03 to deposit a metal stack, as pictured in Figure 4-18b. A 30 nm layer of nickel was deposited to form germanide (GeNi) to reduce contact resistance [216][217], then 10 nm of titanium was deposited to form TiN alloy for preventing metal diffusion in the epilayer [218], 500 nm thick aluminium layer was deposited to reach the surface and a final 60 nm of titanium was deposited to protect the metal staked layer.

4.2.3 Lithography

Lithography is the process of transferring the process step layout from the mask to the wafer. Several techniques are available, amongst them e-beam and contact photolithography are here presented, due to their extensive use during fabrication.

4.2.3.1 E-beam Lithography

E-beam lithography is a standard technique especially adopted in research environment. By using a focused electron beam, direct writing on compatible resist such as ZEP enables accuracy below 10 nm. The precision, however, comes at price of longer processing time [219]. Figure 4-19 from reference [220] shows the e-beam chamber and the working principle; an electron beam source is focused through a series of lenses, an aperture controls the e-beam spot. When the aperture opens the e-beam travels from the source to the target, passing through deflectors that apply a controlled magnetic field to drive the spot on the desired area. By hitting the target, the beam changes the resist chemical composition, which can be dissolved with suitable solvent.

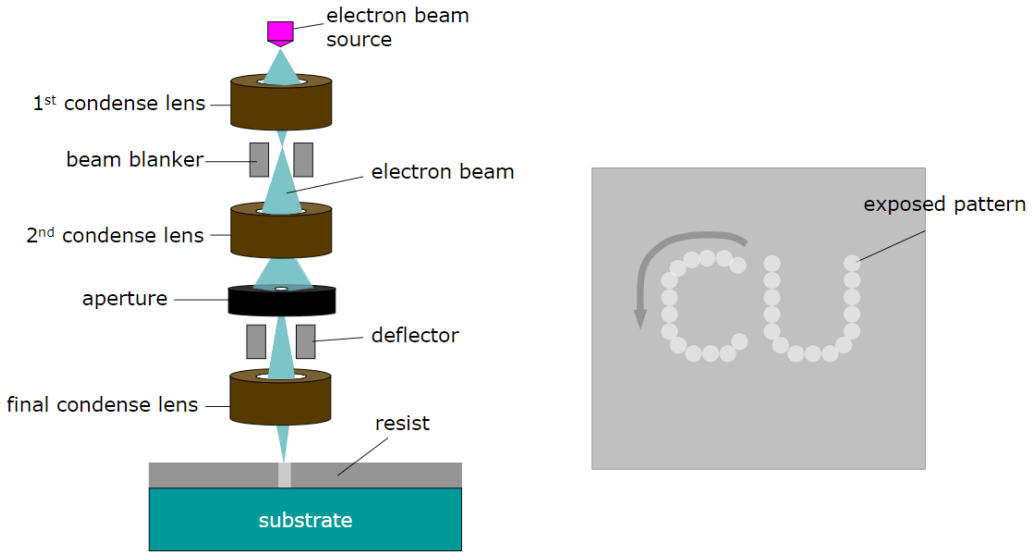

Figure 4-19 E-beam drawing reproduced from reference [220], in (a) the e-beam chamber is depicted showing the beam source, the lenses, the aperture and the deflectors; (b) the exposed patterns is dissolved after development bath in ZEDN50.

In this project e-beam lithography was used to define device cavities where the EAM was realised. Doping wells, waveguides, grating couplers and vias, all those different layers were defined in the process masks with nanometric precision, including features needed for the correct alignment of the electron beam respect the wafer. The process mask, indeed, is defined from the device top-view with a stack of layers, each layer represents a single e-beam step that needs to be aligned to a reference. Details on mask layout are given in section 5.5. The e-beam tool, therefore introduces two alignment errors, the first one is related to the alignment of different layers in different e-beam steps. Depending on many factors such as alignment mark condition on the wafer and tool accuracy, it can be >20 nm. The second kind of alignment error depends on how the e-beam tool works. Large exposed areas are fragmented in fields of 1 mm^2 that are stitched together by moving the stage containing the wafer. Determined by discontinuity at the field boundaries, interfield stitching errors up to 2 nm [221] might occur in dense layouts where the e-beam re-alignment routine is executed after long time and beam deflection is high.

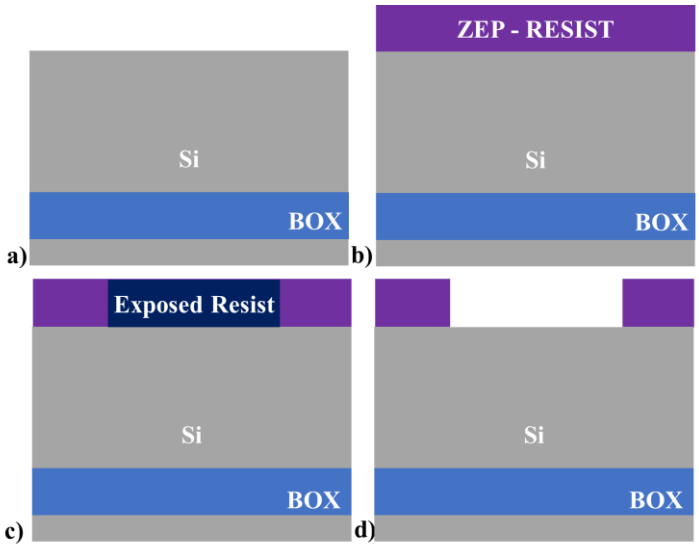

Figure 4-20 E-beam process, (a) dehydration, (b) ZEP spin and bake, (c) e-beam writing, (d) resist developing.

In this project, the adopted resist was the ZEP520A [222], a high resolution positive resist capable of resolving 10 nm sized features with 50 nm pitch [219]; resist etching selectivity to SiO_2 is 1:1, to Si and GeSi instead 1:3. Dr. Ali Khokar oversaw the tool and performed all the writing with the JEOL JBX-9300FS e-beam tool. For each e-beam job, wafers were dehydrated at 210 °C for 30 min (Figure 4-20a), then ZEP (Figure 4-20b) was spun coated with thickness varied according to the process need. For thick etches (cavity etch) 450 nm ZEP was spun at 3370 rpm, for shallow etches (waveguide, gratings, etc.) 265 nm at 6000 rpm, followed by 3 min baking at 180 °C. E-Spacer 300Z was finally spun, a conductive polymer used to coat ZEP over substrates that charge causing beam deflection and pattern distortion. After e-beam writing (Figure 4-20c) with dose 195 $\mu C/cm^2$, patterns were developed in ZED-N50 [222] for 90 s, rinsed in IPA for 30 s and dried with N_2 (Figure 4-20d).

4.2.3.2 Photolithography

In photolithography, a UV light transfers the pattern from a photomask to a photosensitive resist, in Figure 4-21 the whole process is sketched. The wafer is spin coated with photoresist and baked at about 100 °C (Figure 4-21a). Then, (Figure 4-21b) the wafer is transferred in the mask-aligner and aligned with micrometric precision to the mask, a quartz plate containing the layout in a form of metal patterns. Once aligned, an UV lamp illuminates the mask. If the resist is positive (Figure 4-21c in red), only the illuminated areas are removed with a bath in developer, vice versa with negative resist (Figure 4-21c

in green). A final hard bake at 90-140 °C removes all the remaining developer and improves the resist adhesion to the wafer [223].

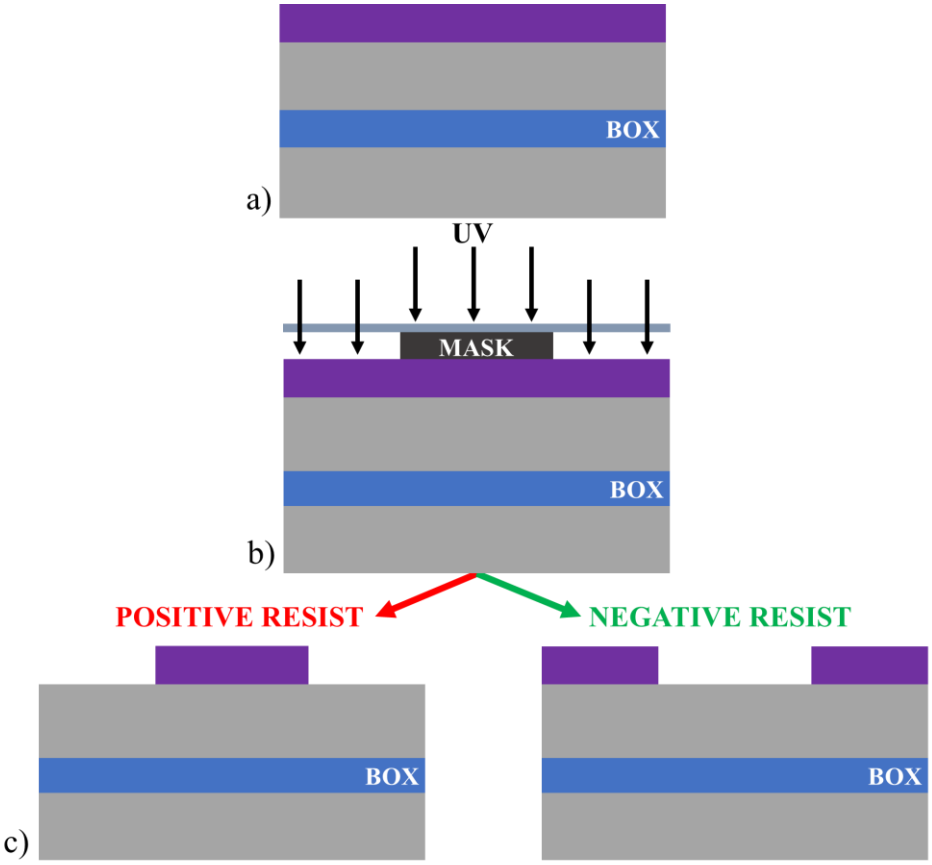

Figure 4-21 Photolithography, (a) the photoresist is spin coated and soft baked on the wafer; (b) after aligning the mask with the wafer, an UV lamp shines the whole wafer modifying the chemical composition of the exposed areas; (c) whether positive (red) or negative (green) resist is adopted, the exposed or the protected areas are finally removed with the developer.

In this work photolithography with the EVG620TB mask aligner was used to open features before GeSi growth for ensuring a homogenous growth of the material on the wafer. Wafers were dehydrated in an oven at 210 °C for 30 min, then S1813 [224] was spun at 5000 rpm and baked at 115 °C for 1 min. Wafers, aligned to the quartz mask, were exposed to UV light for 1.9 s and developed in MF-319 [225] for 40 s, rinsed in DI water and spun dried. Photolithography was also used for metal lift-off as explained in section 4.2.5.

4.2.4 Inductively Coupled Plasma Etching (ICP)

In Inductively Coupled Plasma (ICP), a high-density reactive plasma driven by a RF electromagnetic field, chemically and mechanically etches the exposed substrate (Figure 4-22). The chemical etch is isotropic, whereas mechanical etch due to high-energy ions in

the process is highly anisotropic because ions tend to arrive normal to the target (wafer). The etch rate is high while the surface damage is low. The RF field produces anisotropic etch profile with high verticality if gasses are wisely selected [226].

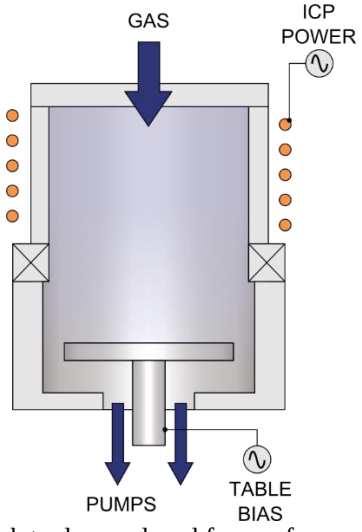

Figure 4-22 Drawing of ICP etch tool reproduced from reference [227].

PlasmaTherm Versaline Deep Silicon Etcher was used to etch the oxide layer, due to better etch verticality and control, whereas the Oxford Instruments ICP 380 system was used for silicon and GeSi. In this project, four etching recipes available in the ICP tools of the NCUS were used to etch Si, GeSi and SiO_2; recipes are summarised in Table 4-1.

Table 4-1 ICP recipes used for Si, GeSi and SiO_2 etch with straight or slanted sidewalls.

	Recipe name	Pressure [mT]	RF [W]	ICP [W]	T [C]	CF_4 [sccm]	SF_6 [sccm]	C_4F_8 [sccm]	Ar [sccm]	CHF_3 [sccm]
Si	ICP-Si	15	50	800	15	-	25	45	-	-
GeSi	ICP-Si	15	50	800	15	-	25	45	-	-
SiO_2	ICP-SiO_2	5	100	400	15	50	-	-	-	-
SiO_2 Slanted	ICPS-SiO_2	10	40	1000	15	-	-	25	18	12

For Si and GeSi (recipe name ICP-Si) a mixture of SF_6 (25 sccm) and C_4F_8 (45 sccm) was used in a 15 mT pressurised chamber with a substrate RF power of 50 W and ionising gas ICP power of 800 W. For etching oxide with straight sidewall (recipe name ICP-SiO_2), instead a pressure of 5 mT, a substrate RF power of 100 W and ICP power of 400 W was used with 50 sccm flow of CF_4; in all etching a temperature of 15 °C was set. A different recipe was used for etching about 500 nm thick SiO_2 with slanted sidewall (recipe name ICPS-SiO_2), needed to avoid cracks in the metal layer deposited afterwards. Chamber pressure was set to 10 mT, RF and ICP powers were 40 W and 1000 W respectively, 25 sccm flow of C_4F_8, 18 sccm flow of Ar and 12 sccm flow of CHF_3 were instead used. Recipes were tested to evaluate the etch rate, for Si an etch rate ranging between 4.7 nm/s and 6 nm/s was measured, for Ge an etch rate from 16% to 30% higher than Si was found,

for SiO_2 an etch rate between 2.4 nm/s and 2.54 nm/s, was measured. Difference in tool conditions, and wafer characteristics affecting the etch rate, were considered during process.

A typical ICP etch subprocess involved up to five steps, summarised in Figure 4-23. PECVD oxide was deposited using one of the recipes defined in section 4.2.2.1, followed by resist spinning, baking (Figure 4-23a) and e-beam or UV contact photolithography. ICP-SiO_2 or ICPS-SiO_2 etch (Figure 4-23b) and ICP-Si etch (Figure 4-23c) were executed in a row to open the thin oxide and etch the underlying layer (Si or GeSi). Resist was stripped with O_2 plasma clean [228] (Figure 4-23d), at the end of the process, the remaining oxide was optionally removed with another ICP-SiO_2 or HF bath (Figure 4-23e).

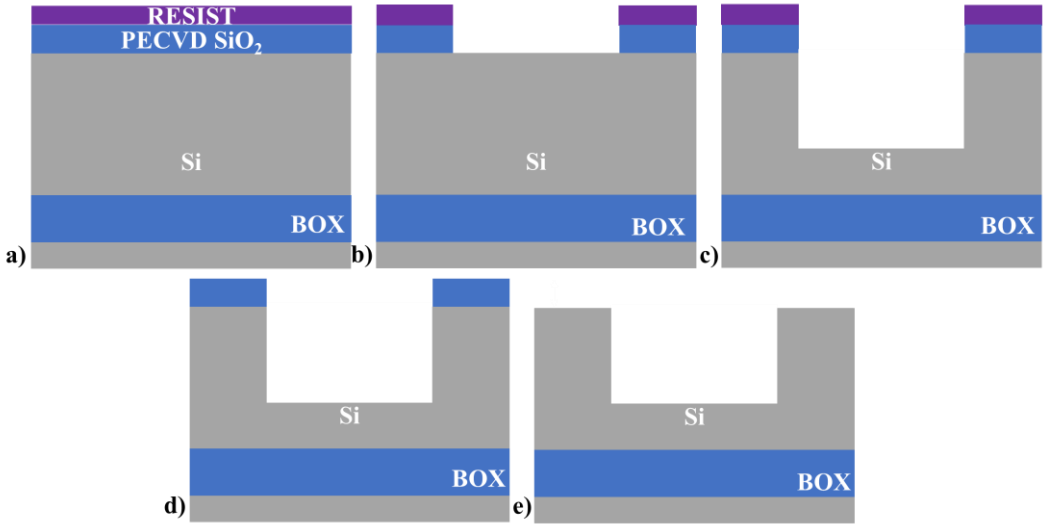

Figure 4-23 ICP subprocess etch: first (a) PECVD oxide is deposited with standard recipe, then resist is spun. Following, (b) lithography (e-beam or UV lithography) and oxide etch (ICP-SiO_2 or ICPS-SiO_2) are performed, thus silicon is etched with ICP-Si (c). The last steps are resist strip (d) and oxide etch (e).

4.2.5 Metal Lift-off

Lift-off process uses a sacrificial material to deposit the target film on the substrate. The sacrificial material, normally photoresist, is etched with a negative mask or a negative resist; then, the desired material is deposited on the whole wafer, covering the opened areas and resist. Finally, the resist is washed away leaving the target material on the wanted areas only. This technique does not require any specific etching tool and avoids direct etching on the wafer; on the other hand, flagging, retention, and ears limit its usability. Flagging refers to irregular patterns torn after lift-off [229] as shown in Figure 4-24a from reference [229], retention instead refers to metal not washed away after lift-off [229] as shown in Figure 4-24b,c from reference [229].

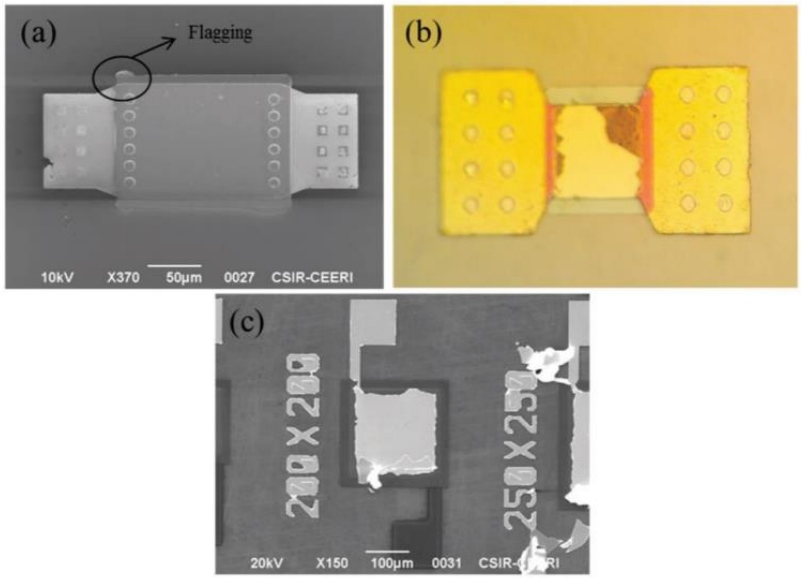

Figure 4-24 (a) flagging of material after lift-off, (b)-(c) retention of metal, reproduction from reference [229].

Ears may form on the sidewalls of the opened resist areas after material deposition producing protruding features on the wafer, as shown in Figure 4-25 from reference [230].

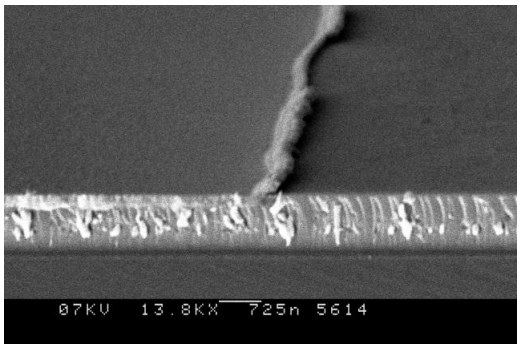

Figure 4-25 SEM picture of a Pt ear protruding from the wafer surface, reproduction from reference [230].

The metal lift-off technique for this project is depicted in Figure 4-26; wafers were spin coated with image reversal resist AZ5214 [231] (Figure 4-26a) spun at 3000 rpm for 40 s obtaining a thickness of about 1.62 µm, then exposed with UV (contact lithography) for 5 s and baked for 30 s at 125 °C to transfer the mask on the resist, as shown in Figure 4-26b in light purple. A second UV exposure for 45 s (Figure 4-26b) was then performed. To remove the resist from the VIA etches (Figure 4-26c) a 15 s bath in AZ400 developer [231] diluted in DI water with a ratio of 1:3 was used; once opened, metal stack was evaporated using the tool presented in 4.2.2.4 (Figure 4-26d). Finally, a bath in acetone to remove the resist underneath and with that the unwanted metal (Figure 4-26e).

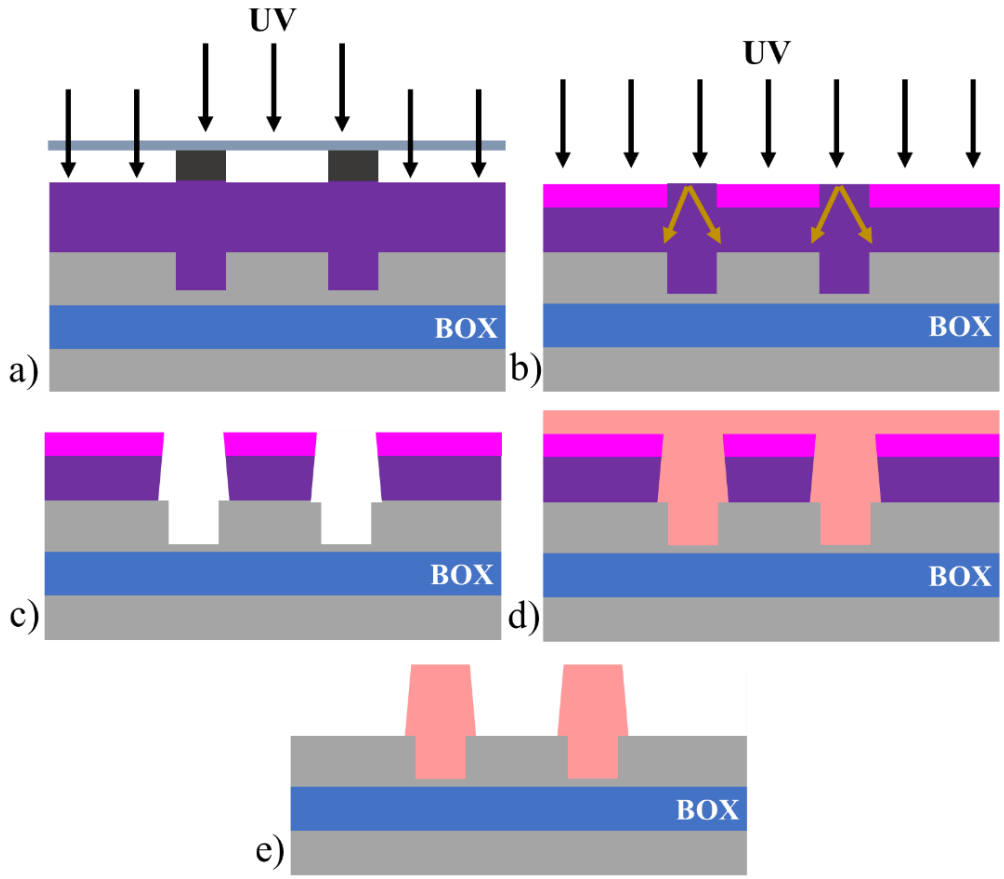

Figure 4-26 Lift-off process. (a) Photoresist (AZ5214 in purple) is deposited on the wafer, a double UV exposure is used to open the features, first a short time exposure to transfer the layout from the mask to the resist as shown in (b) in light purple; the arrow in gold refer to the lift-off profile etch. Then as second longer exposure to open the VIAs using AZ400 developer, as shown in (c). (d) Metal is evaporated filling the apertures (VIAs) and covering the resist. Finally, (e) the resist is dissolved, and the unwanted metal removed.

4.2.6 Ion Implant Doping

Ion implantation is a low temperature and precise process to change physical characteristics and chemical composition of material by introducing impurities [223].

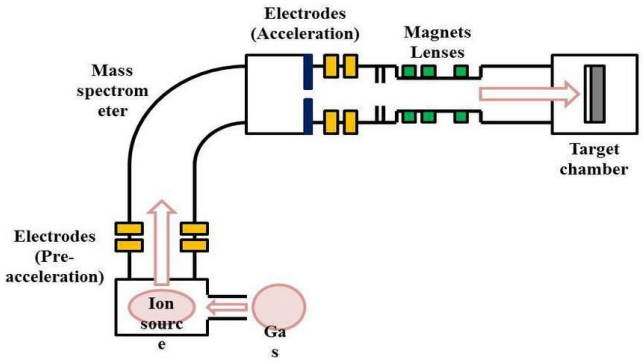

Figure 4-27 Ion implant tool sketch, reproduction from reference [232]. Ions, produced by heating up gases, are accelerated with a series of electrodes and magnets. Ions impinge on the sample penetrating it until the kinetic energy is lost due to collisions with the substrate, electrons and nuclei.

The ion implantation tool is depicted in Figure 4-27 from reference [232]. Gasses are introduced in the ion source and heated up to generate ions of the desired element. Common gasses are diborane (B_2H_6), phosphine (PH_3), difluoroboryl (BF_2). Ions (As, P or B) are filtered and accelerated with a series of electrodes and magnets inside a low pressurised chamber to avoid ion scattering due to collision of ions with gas. Ions, impinging on the surface, lose energy through collisions with substrate, electrons and nuclei, until rest. The propagation depth depends on the substrate material, ion mass, ion kinetic energy, tilt and rotation angles. The doping beam is, in fact, scanned while the wafer is tilted and rotated. In Figure 4-28a, the tilt angle θ is defined between the incident direction of the implantation beam and the normal to the wafer surface; in Figure 4-28b the rotation angle ϕ is between the plane that contains the wafer normal and the beam, and the plane perpendicular to the primary flat (x), which defines the silicon crystal orientation.

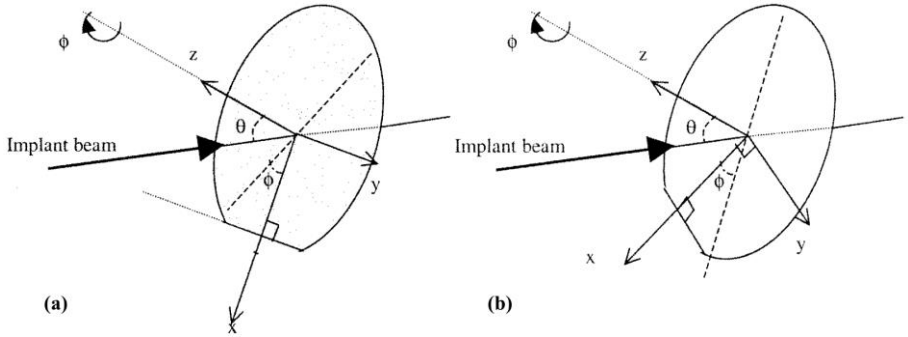

Figure 4-28 (a) the wafer is tilt to an angle θ defined by the wafer normal and the implant beam incident direction. (b) The rotation angle ϕ is defined between the plane containing the wafer normal and the plane perpendicular to the primary flat (x). Image reproduced from reference [233].

Tilt and rotation need to be chosen accurately to determine the doping depth due to channelling effect [234], schematically represented in Figure 4-29; if the direction of the dopant beam (blue arrow) lies close to a major crystal direction (grey dots), small-angle scattering will occur with high probability [235], the dopant (blue dot) will suffer from low energy loss hence will penetrate deeper into the crystal, as depicted in Figure 4-29a. If the dopant direction is not in a major crystal direction, large-scale scattering will occur, the dopant will lose energy quicker, determining shallower penetration, as shown in Figure 4-29b.

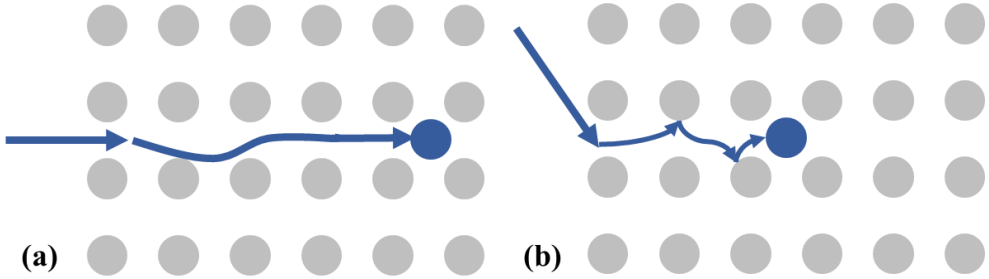

Figure 4-29 Channelling effect, (a) if the incident implantation beam lies close to major crystal directions, ions are suffer a small-angle scattering and penetrate more in the crystal; (b) otherwise, large-scale scattering reduces the dopant penetration.

In this project SOI wafers with major axis aligned to the Si <100> direction were used. Tilt, rotation, and kinetic energy were varied according to the dopant species and required doping depth. Implant collisions ruin the substrate lattice introducing damage that spans from point defects to amorphous layers [162][236]. High temperature annealing (RTA) is executed to restore the crystalline lattice (recrystallisation process [162]) and activate the dopant by moving dopants from interstitial to substitutional lattice sites. For this project the implant step was outsourced to the ion beam centre at the University of Surrey [237].

4.2.7 Rapid Thermal Annealing (RTA)

Rapid Thermal Annealing (RTA) is frequently used to change material composition and as already introduced in the previous section, to activate dopants. NCUS is equipped with JipElec RTA furnaces that permit to quickly heat up and cool down wafers up to 1200 °C by using a halogen lamp. The chamber surfaces are cooled with water, atmosphere is saturated with argon (Ar) and temperature is controlled with a thermocouple located on the wafer holder to accurately measure the wafer temperature. RTA process starts by cooling the chamber with N_2, temperature is raised to the annealing value (ramp up) and kept for a certain period (annealing step), finally temperature is lowered (ramp down).

4.3 Material Characterisation

Material characterisation, to control the process step and tune recipes, is important during fabrication and includes non-invasive and invasive methods. This section gives an overview of the tools used in this work.

4.3.1 Atomic Force Microscope (AFM)

Atomic Force Microscope [238] [239] is a scanning probe microscopy technique to map samples by touching the surface with a cantilever. It is a non-invasive tool, schematised in Figure 4-30 from reference [239].

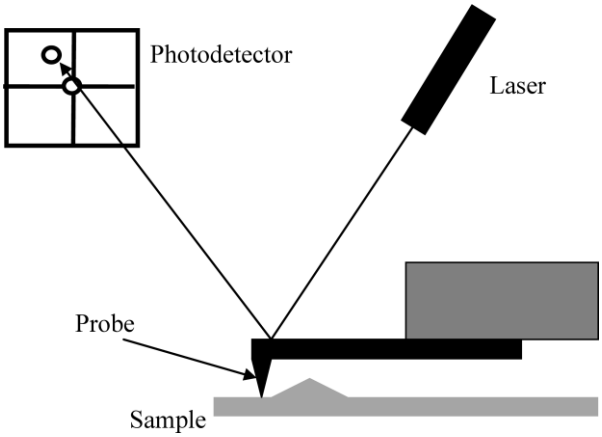

Figure 4-30 AFM working principle, reproduction from reference [239]. A nanometric probe is held on a cantilever which scans the wafer. Forces between the probe and the surface cause the probe to bend. The translation is recorded by using an optic system that shines the cantilever and records the reflected beam with a photodetector. The ray deflection information is then translated in normal displacement.

The cantilever, usually in silicon or SiN, has a curve tip (probe) with nanometric radius and is driven with piezometric elements ensuring precise movements on the sample. When the tip is contacted on the sample, a deflection of the cantilever occurs due to forces between the tip and the sample, the deflection is recorded using an optic readout unit consisting of a laser and a photodiode. The laser shines the cantilever, while the photodiode collects the reflected light, which depends on the cantilever deflection, a feedback control translates the deflection information in normal displacement. The readout operation is executed while the sample is scanned; the raw data is usually converted in roughness measurement by calculating the Root Mean Square (RMS).

4.3.2 Ellipsometry

Material properties of dielectrics such as composition, roughness, thickness and doping can be measured by comparing with a model the change of polarisation of a light after reflection or transmission. In Figure 4-31, from reference [240], the working principle of an ellipsometry tool is depicted. A light source is held at an angle while light is linearly polarised, on the opposite position the reflected light from the sample travels through another polariser and a detector.

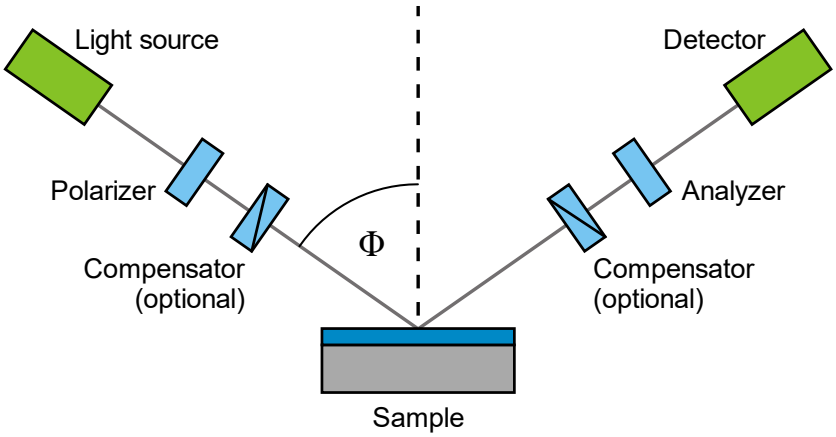

Figure 4-31 Ellipsometry working principle, reproduction from reference [240].

The complex reflectance ratio depends on the amplitude change (Psi) and phase difference (Delta) between transmitted and reflected light; the complex reflectance ratio is calculated by comparing experimental data with a model. Since signal depends on both material properties and thickness, this non-invasive technique permits to accurately characterise thicknesses of single layers or heterostructures [241].

During fabrication, data were collected using the M2000DI ellipsometer and inspected with CompleteEASE software [242], to measure thickness of different layers etched and/or deposited in different steps. As an example, in Figure 4-32 fitting measurements are shown after depositing 120 nm PECVD SiO_2 on a SOI wafer with nominal thicknesses of 3000 nm buried oxide and 500 nm Si overlay. In Figure 4-32a, the Psi (red) and Delta (green) measured from the tool are perfectly fitted with the provided SOI model [243] by adding an extra SiO_2 layer (dashed lines) giving the following thicknesses: 3023 nm buried oxide, 504 nm Si overlay and 125 nm PECVD oxide.

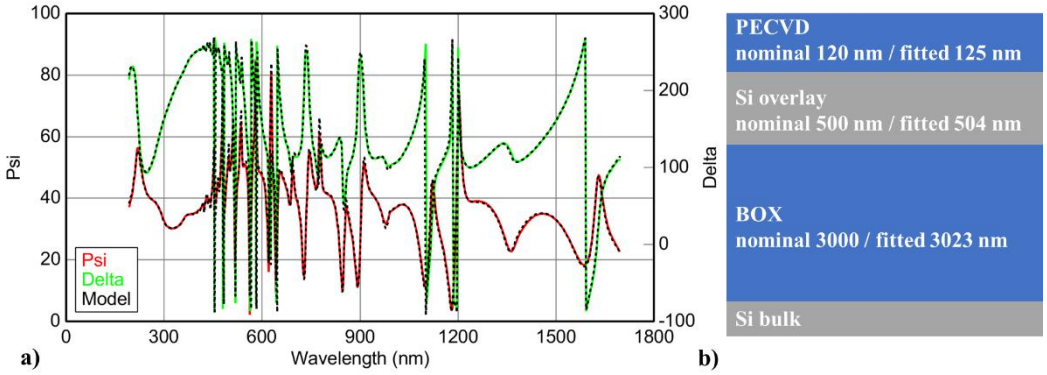

Figure 4-32 (a) Ellipsometry measurement fitting with CompleteEASE, Psi in green and Delta in red represent the amplitude change and phase change measured in the ellipsometry tool while sweeping the light wavelength. In dashed lines, the fitting results using the provided SOI model. (b) layer stack with nominal and fitted thicknesses.

4.3.3 Scanning Electron Microscopy (SEM)

SEM is an analysis technique that uses focused electron beam to accurately reproduce 3D images with a resolution up to 1 nm [244]. Electrons interacts with atoms of the sample producing several signals containing information on composition and roughness; commonly, detection is achieved with secondary electrons emitted by atoms from the surface specimen, excited by the electron beam. Other signals such as back-scattered electron, X-rays and light, absorbed and transmitted electrons may be used for detection, but it is very uncommon that a single machine implements all kind of detection. Large depth of field resulting from the very narrow electron beam is another advantage in SEMs [245]. Due to the Focused Ion Beam (FIB) cut, FIB-SEM is an invasive analysis.

NCUS is equipped a NVISION 40 FIB-SEM, a double column electron microscope that, integrating a Focused Ion Beam, permits to process material and produce accurate 3D images. The FIB is very similar to SEM technique but using ions with high mass such as gallium, ablation and deposition is possible [246]. For this project the FIB was only adopted to cut cross-section of samples inspected with the SEM column to evaluate thickness, roughness and composition of layers, as shown in Figure 4-33.

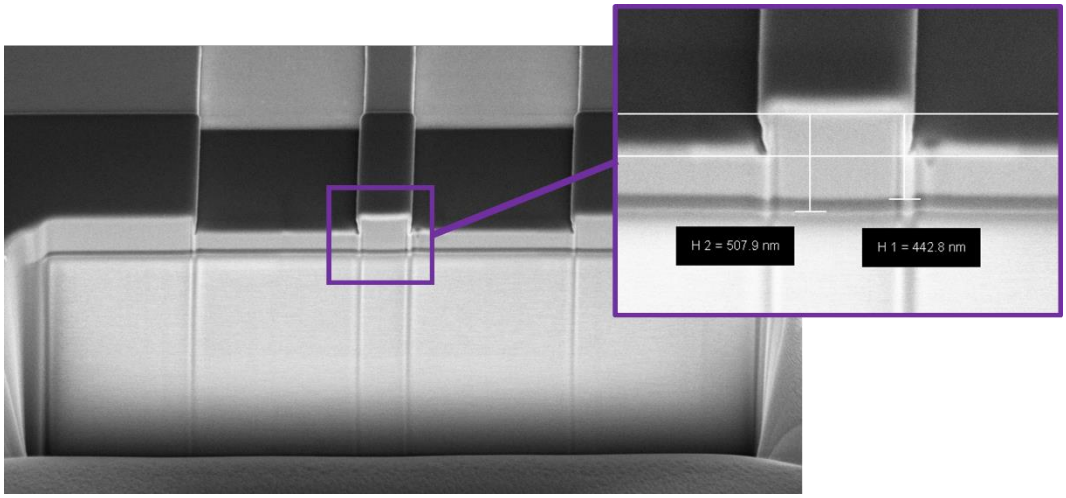

Figure 4-33 FIB-SEM image of a waveguide test etch on 500 nm SOI wafer. FIB is used to cut a cross-section visible as a rectangular hole; in the inset, the closup of the rib with relevant dimensions, different speciemen are distinguishable with grey tones.

4.3.4 Secondary-Ion Mass Spectrometry (SIMS)

Another invasive technique, Secondary-Ion Mass Spectrometry (SIMS) analyses composition of films with a focused ion beam sputtered on the sample. Secondary ions ejected from the sample, are collected and their masses and charges are analysed with a spectrometer to determine elemental, molecular and isotopic composition [247]. SIMS

analysis, for this project, were outsourced to get precise layer thickness, composition and doping concentration, as shown in Figure 4-34.

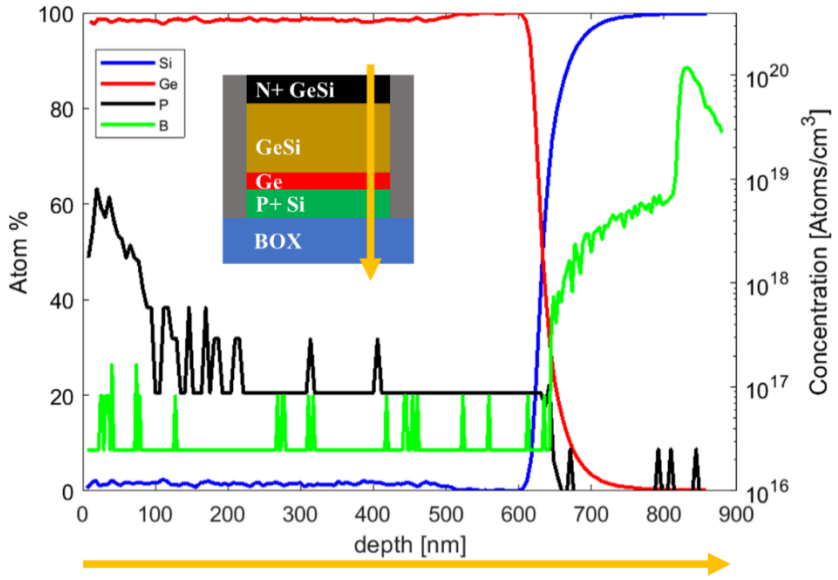

Figure 4-34 SIMS analysis of a testing sample, depicted in the inset, along the depth.

4.3.5 Other methods

Other outsourced analysis conducted during this project were the High Angle Annular Dark Field Scanning Transmission Electron Microscopy (HAADF-STEM) [248], and Precession Electron Diffraction Technique (PEDT) [249][250]. HAADF-STEM is a method for mapping samples with a scanning transmission electron microscope [244] to collect scattered electrons with an annular dark-field detector. It was used to accurately evaluate dislocations in samples. PEDT, instead, is an innovative technique to accurately measure bi-dimensional strain in thin films.

4.4 Device Characterisation

Devices fabricated in the NCUS cleanroom were characterised in two different setups; a DC semi-automatic setup was developed specifically for this project, allowing to carry electro-optic measurements on device batches. The high-speed setup, sharing most of the components of the DC setup, was used on selected devices to assess modulation performances. In the following, drawing of both setups with comments are given.

4.4.1 DC Experimental Setup

The DC setup is sketched in Figure 4-35. The optical section includes the Agilent 8163B Lightwave Multimeter equipped with Agilent 81950A tunable laser (C-band) and 81634B power meter, a polariser and micrometre positioning stages. Polarisation maintaining optic fibre (PM-SMF) and SMFs connect all optical components (black lines in the picture).

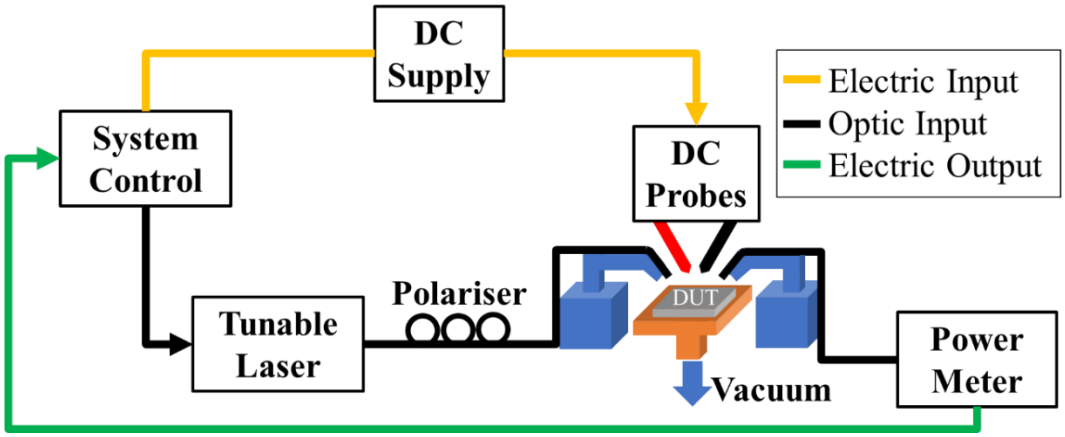

Figure 4-35 DC measurement setup

Light from the laser propagates into to the polariser to reduce as much as possible TM light polarisation. From the polariser, light travels in a SMF whose end has been cleaved to expose the fibre core-cladding tip, held on a movable stage unit (blue drawing in the picture). Microcontrollers on the stage permit precise alignment between fibre tip and DUT input port; the DUT is held on a copper stage using vacuum. Another stage unit holds a second cleaved SMF aligned to the output port of the DUT and connected to the power meter, while titanium needles, connected to DC probes, are lowered onto the device metal pads. A Panasonic GP-KR222 camera on top of the copper stage facilitates alignment of the fibres on the GC. A photo of the stage section is shown in Figure 4-36, highlighting the angled fibre holder (red), the DC probes (yellow) and the camera lens focusing tube (white). In the inset a close-up of the chip surrounded by the fibre and DC needle holders is depicted, reflected from the chip, the exposed optic fibres and DC needles are visible. The electric section, used for electric characterisation (IV curve) and transmission spectra (evaluation of FKE), includes DPP105 Positioner DC probes from Cascade Microtech connected to a Keysight Source Meter SMU 2400.

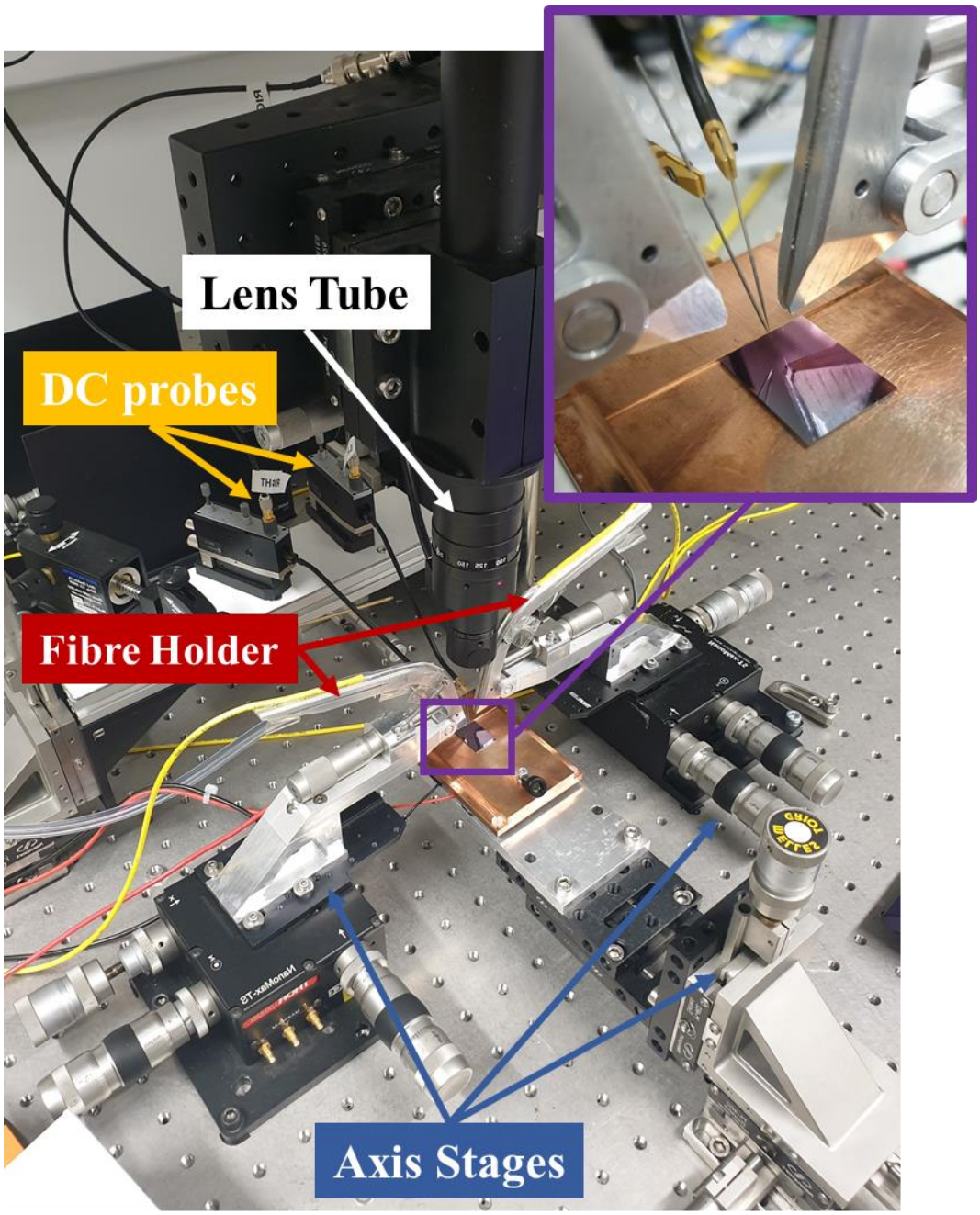

Figure 4-36 Experimental setup, in the inset a chip on the copper stage is characterised in DC with optic fibres coming out from the angled fibre holders and titanium needles attached to the Cascade Microtech DC probes. The high-speed stage setup differs only for the RF probes

Laser, source meter and power meter are controlled through System Control, a software written in Matlab®, allowing batch measurement and analysis; the interface is shown in Figure 4-37. It is possible to select laser power output, wavelength scan range, photodiode sensitivity, bias and current limit. For passive measurements, the routine enables laser scan only; for active measurements, instead, an IV measurement is first executed to ensure the correct connection between dc probes and device metal pads, hence

electro-optic measurements are done at the selected reverse biases. Data are saved in files stored in folders defined by the user.

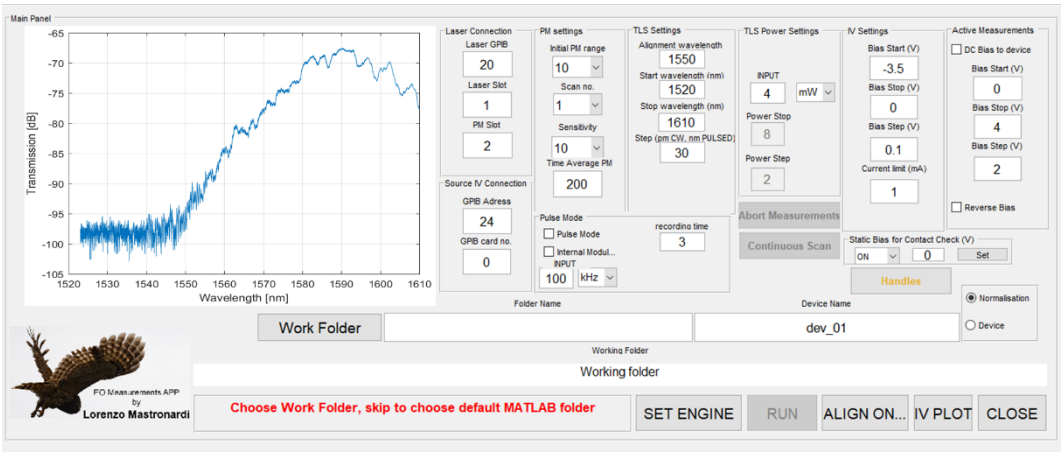

Figure 4-37 Graphical interface of the system control app written in Matlab®.

For DC measurements, the software drives the laser in wavelength sweep mode and collects the photocurrent amplitude from the power meter. Transmission spectra are retrieved from the Server Engine part of the Keysight N7700A Photonic Application Suite [251]. First, measurements on silicon waveguides are performed to evaluate the fibre-waveguide coupling loss, the grating loss and the silicon waveguide loss then, electro-optic measurements are executed on the DUT while applying DC biases. Once both measurements are available, the software analysis routine subtracts the transmission spectra of the silicon waveguide from the device waveguide (normalisation operation) to retrieve the cavity IL. Finally, cavity IL with and without bias are compared to calculate ER and the ER/IL ratio. IV measurements are possible during transmission spectra routine or as an independent test by controlling the DC supply.

4.4.2 High-speed Experimental Setup

High-speed measurements were conducted on a different setup that shares some of the components of the DC setup but the working conditions differ.

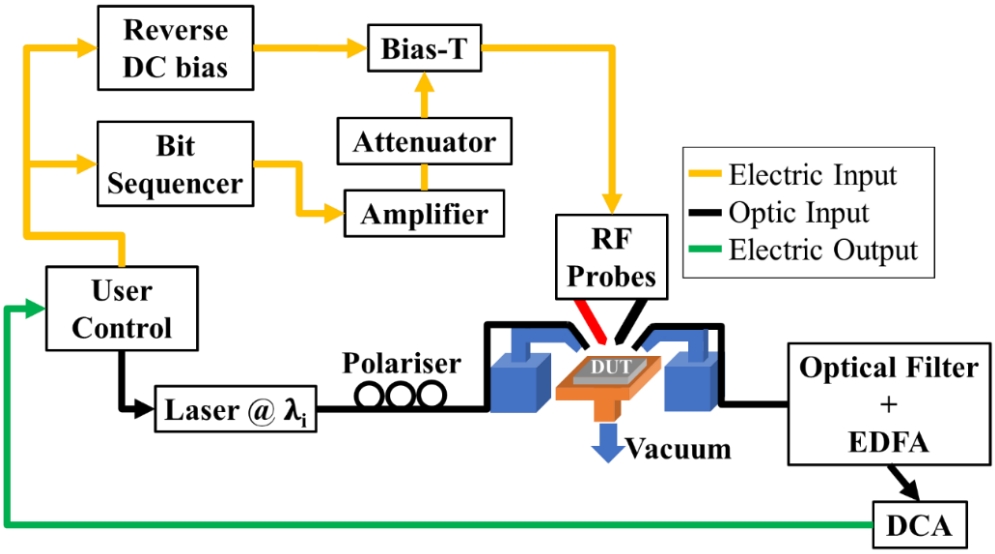

Figure 4-38 High-speed measurement setup.

In Figure 4-38, the high-speed setup uses the same laser, power meter unit, stages, DC supply of the setup shown in the previous section; important difference are found in the electric input system, the output detection unit and operation. RF compatible elements are added to generate the electric modulating signal. For this project a 56 Gbps pseudorandom binary sequence (PRBS) generator coupled with a cascade of RF amplifier and in line RF attenuators was employed to generate a random electric signal with fixed swing voltage. DC and RF electrical signals are mixed with a bias-T. The resulting signal is fed to the device by RF GS probes; the GS probes are not 50 ohms terminated thus electric reflections must be considered in the measurements.

During measurements, the laser is set to a fixed wavelength. At the output an optical filter, an optical amplifier (Erbium Doped Fibre Amplifier) and a Digital Communication Analyser (DCA) are included to remove optical noise, amplify and convert signal to electric and assess modulation performances. The final difference with the DC setup is the absence of the System Control App.

Similarly to DC measurement, the device and grating couplers are aligned to the fibre tips using angled holders, while the RF probes are lowered onto the device metal pads. The laser is turned on and fed to the device after polarisation filtering. At the same time, the RF+DC random electric signal is generated with NRZ coding and fed to the device

through probes. At the output, the modulated light is collected, filtered, amplified and finally converted back to an electric bitstream; the DCA samples both input and output signals and generates the eye diagram plots, whose characteristics (dynamic ER and rise time) are used to evaluate device performances.

4.5 Summary

In this chapter computer aided methods for designing and simulating the EAM were presented, Silvaco TCAD suite for developing the process recipes and simulating the electric field distribution, Matlab® for electro-optic simulations, Lumerical for transmission and coupling loss simulations and Tanner EDA L-edit for mask design. Most of the fabrication was performed in the Nanofabrication Centre of the University of Southampton with standard processes, therefore all fabrication methods and tools employed in this project were examined. E-beam lithography was mostly used, due to its nanometric resolution and accurate control; UV contact lithography, instead, was helpful for steps allowing micrometric tolerances. Etching steps following lithography and requiring control of sidewalls and uniform etch rate was preferably obtained with ICP, whereas wet etch was useful for wafer conditioning and shallow etches. Material deposition and doping implantation were outsourced.

In this chapter characterisation methods were presented: first material characterisation methods adopted to control the process steps and fine tune the step recipes, then device characterisation setups built to test devices and evaluate performances in terms of speed and power consumption. Non-invasive techniques used during and after fabrication were presented. These included AFM microscopy after epitaxial growth to ensure the correct deposition of GeSi in cavities with smooth surface; ellipsometry to estimate material thickness during etch steps and SEM imaging to get precise images of nanometric structures and evaluate aspect-ratio. Often used with FIB, this tool should be considered invasive too. Outsourced invasive techniques were SIMS to accurately measure the material composition in depth, HAADF-STEM for mapping the material uniformity (dislocations) and PEDT to evaluate strain. In the group labs, setups were built to conduct DC and high-speed characterisation; for the DC setup, an app was coded to control all the equipment remotely, improving the measuring efficiency. In the high-speed setup, due to the number of equipment to set for each experiment, a manual approach was chosen.

Chapter 5

Modelling and Designing

The aim of this project is to develop and realise an innovative electro-absorption modulator for short range communication applications, using the Franz-Keldysh (FKE) effect on a GeSi PIN diode. To choose the correct design, an extensive simulation study was needed. Unfortunately, the common available software for photonics devices do not implement neither the FK effect nor GeSi, thus a custom simulation platform had to be made.

Starting from the model found in reference [102], substantial work has been done to complete a set of simulation scripts that defines a custom structure, calculates the electric field distribution for given applied voltages, calculates the complex refractive index applying the FKE for a wavelength range and, by solving the optical mode distribution, ultimately evaluates device performances in DC and transient with analysis parameters retrieved from the mode effective refractive index. The physics involved in such complex device cannot be completely summarized into a single model, but the approximations can be used to compare performances of different designs. This platform employs two approaches. In the first case, fast and yet accurate simulations are obtained by defining the device cross-section with uniform blocks with fixed characteristics. In the second approach, effects such as overgrowth, over-etching, dopant diffusion and concentration are evaluated using fabrication process simulations for the cross-section definition (growth and etching) and junction definition (dopant implantation), hence devices with characteristics close to a real modulator are simulated.

In this chapter, the simulation platform is examined starting from the mathematical model developed in reference [102] that evaluates the FKE in bulk GeSi alloy. The script written for this project is compared with simulations from reference [102] evaluating the FKE on bulk material for different GeSi composition and electric field strengths. Further in the chapter, main characteristics of the whole simulation platform are presented in a series of flow charts and comments to better understand the working principles that drive this software; a real EAM from reference [30] is simulated to validate the simulation environment.

In the second part, five different simulation variables are investigated to optimise the device design. These variables provide device behaviour and performances for doping concentrations, implant recipes, doping alignments and epitaxial stack influence on device spectral efficiency. Then simulations adopted to define GC, waveguide tapers and for evaluating the coupling efficiency between silicon and GeSi waveguides, are shown. Results from simulations are employed to define the design reference with variations included in the mask layout, the details of which are given in the last section.

5.1 Mathematical Model

The mathematical model of the Franz-Keldysh effect has been extensively studied over the last fifty years [29][252][253][254][255], as a result in reference [102] a closed equation is available. The Schrödinger wave equation of an electron-hole pair is used to determine the absorption when an electric field is applied. In the case of a uniform electric field in the z direction (perpendicular direction respect to the device surface) that dominates over the exciton effect (electron-hole interaction), the Schrödinger equation can be arranged as a classical differential equation whose solutions are Airy functions: $Ai(z), Bi(z)$ [256][257], with z the propagation direction. The wave function must decay for $z \to \infty$ [102] (all power absorbed at infinity propagation distance), this implies the solution to be $Ai(z)$. The absorption coefficient equation is derived from Fermi's Golden Rule [258][259], to get the absorption coefficient versus the wavelength for a given electric field:

$$\alpha(\omega) = \frac{\pi e^2 E_p}{12 n_r c \epsilon_0 m_0 \omega} \left(\frac{2m_r}{\hbar^2}\right)^{2/3} \sqrt{\hbar\theta_F}\ [-\eta Ai^2(\eta) + Ai'^2(\eta)] \qquad \text{Eq. 5-1}$$

where $\hbar\theta_F = \left(\frac{\hbar^2 e^2 F^2}{2m_r}\right)^{1/3}$, F electric field, $\eta = \frac{(E_g - \hbar\omega)}{\hbar\theta_F}$, n_r refractive index, m_r effective mass, E_p constant related to the transition matrix element and $Ai'(\eta)$ the derivative of the Airy function $Ai(\eta)$. Equation 5.1 models the electron-photon interaction when an electric field is applied on a direct bandgap semiconductor, so that indirect bandgap transition contributions must be added as a constant. Another limitation of this model is the lack of the exciton effect (change in the bandgap because of electron-hole interaction) but if the photon energy is just below the energy bandgap, the exciton effect is small, and its effect can be neglected. This model is, hence, suitable for calculating the absorption in the weakly absorbing regime where the electric field effect is stronger.

In the case of biaxial strained material, the light and heavy hole bands are non-degenerate [55][56], Eq. 5-1 becomes:

$$\alpha(\omega) = \frac{\pi e^2 E_p}{12 n_r c \epsilon_0 m_0 \omega}\left\{\left(\frac{2m_{r,lh}}{\hbar^2}\right)^{2/3}\sqrt{\hbar\theta_{F,lh}}\,\left[-\eta_{lh}Ai^2(\eta_{lh}) + Ai'^2(\eta_{lh})\right] + \left(\frac{2m_{r,hh}}{\hbar^2}\right)^{2/3}\sqrt{\hbar\theta_{F,hh}}\,\left[-\eta_{hh}Ai^2(\eta_{hh}) + Ai'^2(\eta_{hh})\right]\right. \quad \text{Eq. 5-2}$$

where the subscripts lh, hh stand for “light hole”, and “heavy hole” respectively.

Eq. 5-2 is valid for a strained direct bandgap semiconductor, such as Ge with photon energies around 0.8 eV; this equation is still valid in GeSi, if linear interpolation between Si and Ge is implemented to get material parameters [102] such as deformation potential, refractive index, effective masses and energy bandgap. The light hole, heavy hole and split-off band gaps defined in reference [260] are used to evaluate η_{hh} and η_{lh}.

5.1.1 Analysis Parameters

For EAMs, loss mainly comes from the material absorption in the intrinsic region between the P and N doped layers, where the electric field is present, hence it is useful to define the material insertion loss with and without reverse bias:

$$IL_{ON,OFF}(dB) = -10Log(e^{-\alpha_{ON,OFF}L}) \approx 4.343\alpha_{ON,OFF}L \quad \text{Eq. 5-3}$$

where L is the active layer length and $\alpha_{OFF}, \alpha_{ON}$ are the absorption coefficients with and without reverse bias. In Figure 5-1a the IL_{ON} and IL_{OFF}, depicted in red, have been calculated from Eq. 5-2 for a GeSi alloy with 1.5 % of silicon and 0.2% tensile strain and device length of 50 μm. At 0 V (full red line), to account for the built-in electric field in PIN structures an electric field of 10 keV is considered, the IL_{ON} is high for λ <1.5 μm and

shows the Franz-Keldysh oscillations (FKO) with period dependent on the built-in electric field and caused by the interference of the electron wave function in the CB and VB that enhances absorption for some photon energies and reduces for others [102][103]. For $\lambda >$ 1.5 μm, absorption is only due to indirect bandgap transitions, hence IL_{ON} is lower.

For -2 V bias, the IL_{OFF} spectrum is monotonic, for short wavelengths the damping behaviour is replaced by a smooth curve with reduced loss; in the weakly absorption regime around 1.5 μm, IL increases up to 15 dB thanks to the FKE (dashed red line) overcoming the IL_{ON}. At longer wavelengths ($\lambda >$ 1.6 μm) the IL is once again only influenced by indirect bandgap transitions. To isolate the electric field contribution to the losses, material ER (Figure 5-1a, blue curve) can be calculated as ILs ratio:

$$ER_{material}(dB) = \frac{IL_{OFF}}{IL_{ON}} = -10Log\left(\frac{e^{-\alpha_{OFF}L}}{e^{-\alpha_{ON}L}}\right) \approx 4.343(\alpha_{OFF} - \alpha_{ON})\,L \qquad \text{Eq. 5-4}$$

The material ER spectrum shows a gaussian-like shape, whose peak is centred at the maximum loss difference between the "ON" and "OFF" states, for the following ER and $ER_{material}$ will be used indifferently. Finally, the absorption contrast (Figure of Merit), representing the material electro-absorption efficiency, is the ratio between the Extinction Ratio and the Insertion Loss:

$$FOM = \frac{ER_{material}}{IL} = \frac{\Delta\alpha}{\alpha_{ON}} \qquad \text{Eq. 5-5}$$

This FOM, shown in Figure 5-1b, reaches its peak in the weakly absorption regime for photon energies just below the material direct bandgap where electro-absorption effect is strong (high $\Delta\alpha$) but in absence of reverse bias the absorption is due to indirect transitions only (small α_{ON}). FOM spectra (DC FOM) and a time varying FOM(t) were calculated with simulations at different biases by sweeping the wavelength and in transient by applying an electric square pulse of about 50 ps while keeping fixed the wavelength.

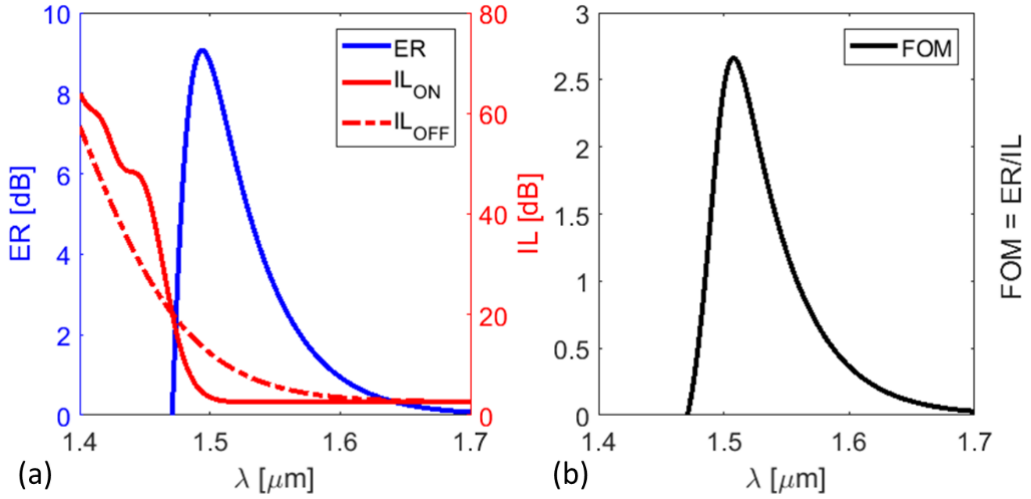

Figure 5-1 Example of (a) IL_{ON}, IL_{OFF}, ER and (b) FOM calculated using the model presented in 5.1 for a 50 μm long GeSi alloy with 1.5% Si and electric field of 10 kV/cm and 100 kV/cm for the ON and OFF state, respectively.

5.1.2 Model Validation

In order to validate the script, a series of simulations are realised with data from reference [102], results are compared and are showing good agreement. It was considered a generic bulk GeSi PIN diode 50 μm long with uniform electric distribution in the cross-section. In the first validation simulation, the absorption contrast for a wavelength range is calculated for different silicon contents. Following the parameter settings in reference [102], the built-in electric field value for the "ON" state is 10 kV/cm, the electric field for the "OFF" state is instead 100 kV/cm. The silicon content is varied from 0.5% up to 1.1% and the simulation is run for λ between 1.4 μm and 1.7 μm. In Figure 5-2, the absorption contrast (FOM) as a function of wavelength and Si content is depicted in a series of curves with colours from blue to yellow. Silicon and germanium are indirect bandgap materials, but around 0.8 eV (1550 nm) Ge has a direct bandgap; increasing the Si content in the GeSi alloy implies the material to become more Si-like, hence the GeSi bandgap increases and more indirect transitions occur, causing a blueshift and a reduction of the FOM peak (from blue to yellow curves). By importing the plots shown in reference [102] for a silicon content of 0.5% and 1.1% (red and black dotted curves), simulation data can be compared showing a good fit of the curves to those from reference [102].

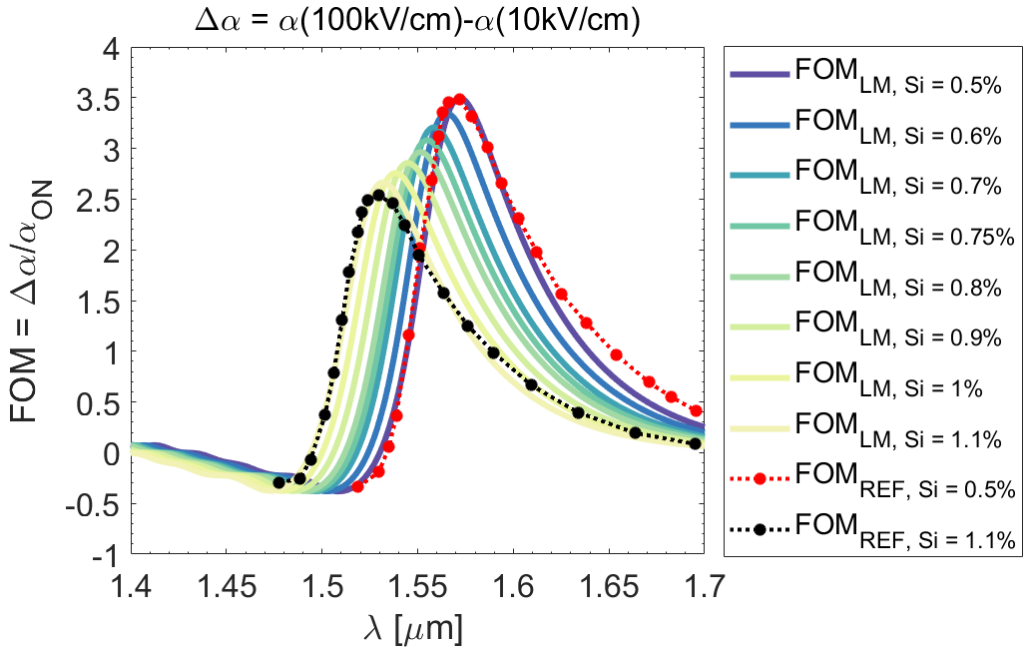

Figure 5-2 FOM vs Si content for wavelength range 1.4 μm to 1.7 μm compared with results from reference [102] (dashed lines) by importing the curves with Si=0.5% (red dot) and Si=1.1% (black dot).

For the second validation simulation, the absorption contrast is simulated with fixed wavelength (1550 nm) and varying silicon content. In Figure 5-3, each dot represents the FOM peak for specific Si content. The simulation result (blue curve) is compared with the reference curve (red) taken from reference [102]. Once again, the difference is small (maximum difference <0.13), both curves show that a silicon content of 0.7% to 0.9% gives the best results in terms of FOM.

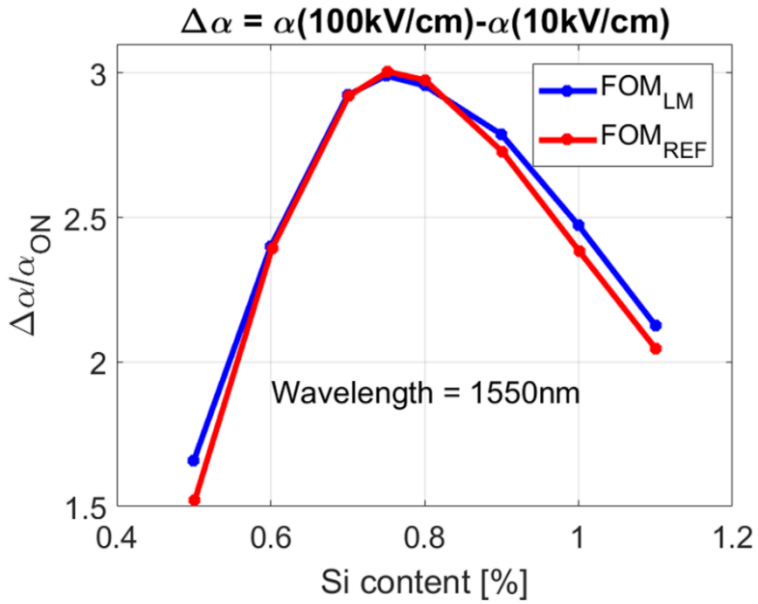

Figure 5-3 FOM peak vs Si content for a fixed wavelength, the script curve (blue) is compared with results from reference [102] shown in red.

Finally, in the third validation simulation the effect of the electric field on the absorption is calculated for a fixed wavelength (1.55 μm) and silicon composition (0.75%). In Figure 5-4, absorption increases almost linearly with the electric field, the maximum electric field value is set as 130 kV/cm, where the breakdown condition is reached [102]. The similarity of the script result (blue curve) with the imported curve from reference [102] (red), confirms the code is implemented effectively.

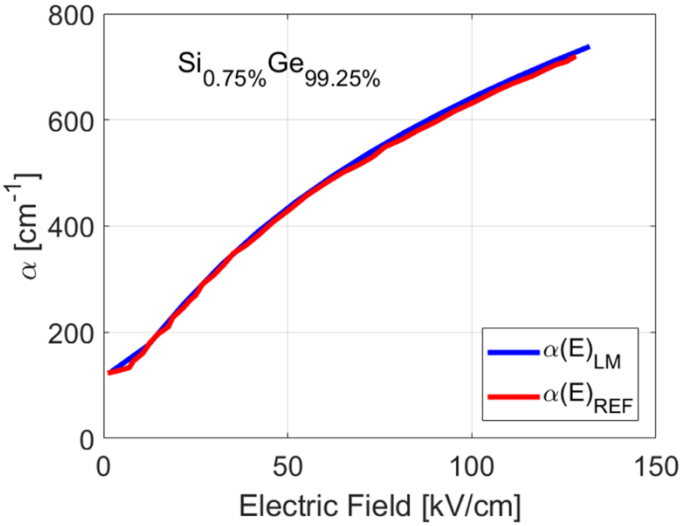

Figure 5-4 Absorption coefficient at 1.55 μm vs electric field, the script curve (blue) is compared with the same simulation from reference [102] (red curve).

5.2 Simulation Platform

Commercially available software implementing the FKE and GeSi material were not available, hence a custom simulation platform was needed. The idea behind this platform is to define cross-sections from a template using a set of "input variables" and run automatic simulations to calculate the electric field distribution and, by matching the correspondent field effect, the optical mode distribution. Analysis parameters, at the end of the simulation run, are handy tools to compare different designs.

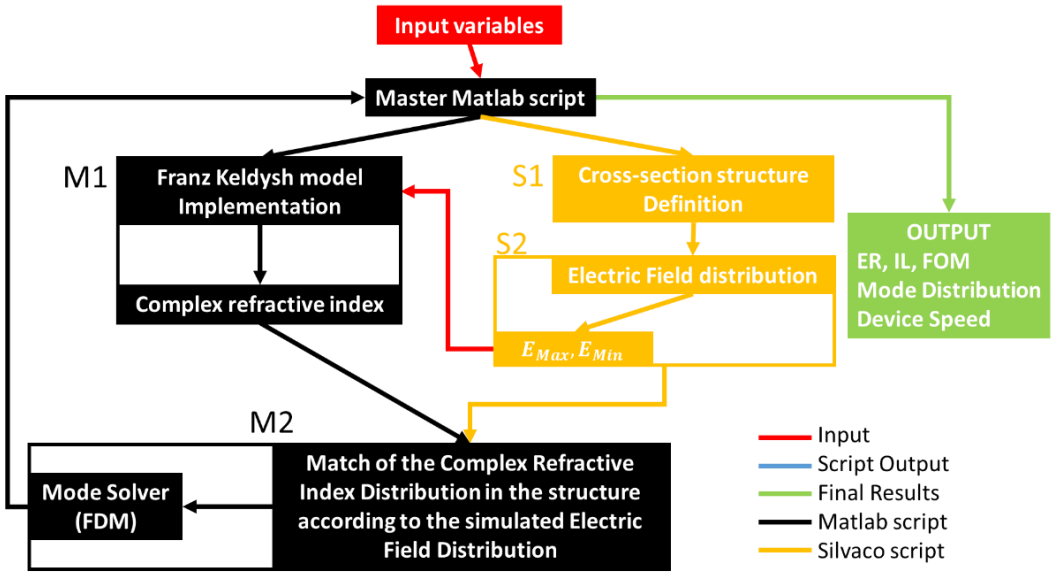

Figure 5-5 Simulation Platform Flow chart. Input are passed to the first Matlab® script to generate the design code and run electro-optic calculations (M1). In yellow the Silvaco code, that builds the device mesh with blocks or simulating the fabrication process (S1) and evaluates the electric field distribution (S2). Output from M1 and S2 are used in M2 to solve the optical mode under DC bias and/or transient time electric signal.

The simulation platform, depicted in Figure 5-5 can be divided in two parts: the structure definition and electric simulation using Silvaco (yellow), on one side; the FKE routine and the electro-optical characterisation with Matlab® (black), on the other side. The Master Matlab® script controls the whole platform by setting the simulation parameters: Si content, strain, doping concentrations, reverse bias, wavelength range. In the structure development section (Figure 5-6 in yellow), the EAM cross-section is defined and built by S1.

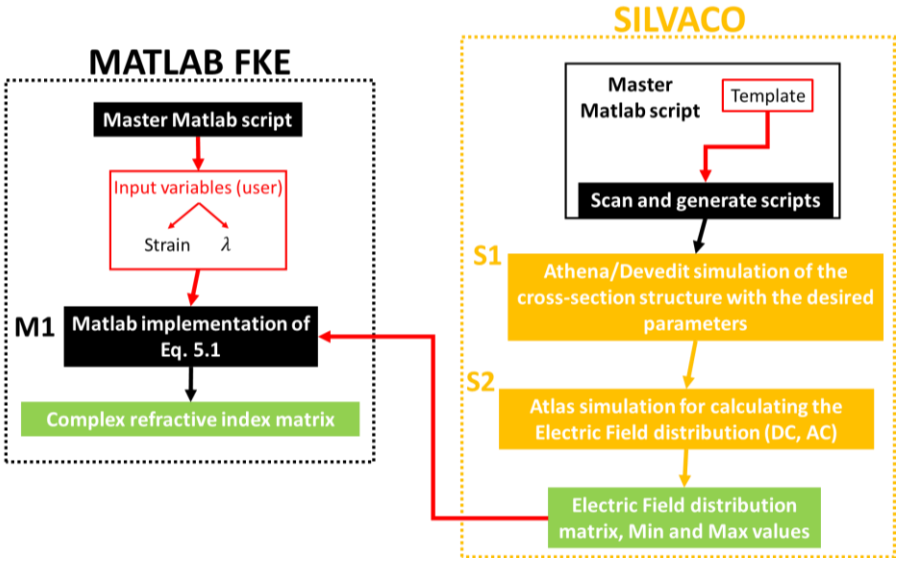

Figure 5-6 Flowchart detail of the structure development section. S1 builds the device cross-section and S2 calculates the electric field distribution with DC and transient electric signals. In black the flowchart detail of M1 the part of the code that implements the FKE.

The cross-section can be built with Devedit™ using building blocks or mimicking the process using Athena™, particularly effective to test dopant implantation recipes. In the first case (Figure 5-7a) each layer has constant characteristics within the box boundaries, allowing faster calculation of both electric field distribution and electro-optic effect while keeping good accuracy; in the second case, the active layer stack is deposited as Ge doped with a varying Si concentration, as shown by the arrow in Figure 5-7b. The advantage of using Athena™ is the introduction of all side effects happening in a real fabrication run, including but not limited to dopant diffusion, over-etching and misalignment. Once the cross-section is ready Atlas™, the Silvaco™ electric solver engine, calculates the electric field distribution by applying a constant reverse bias (DC) or a transient reverse voltage signal (AC).

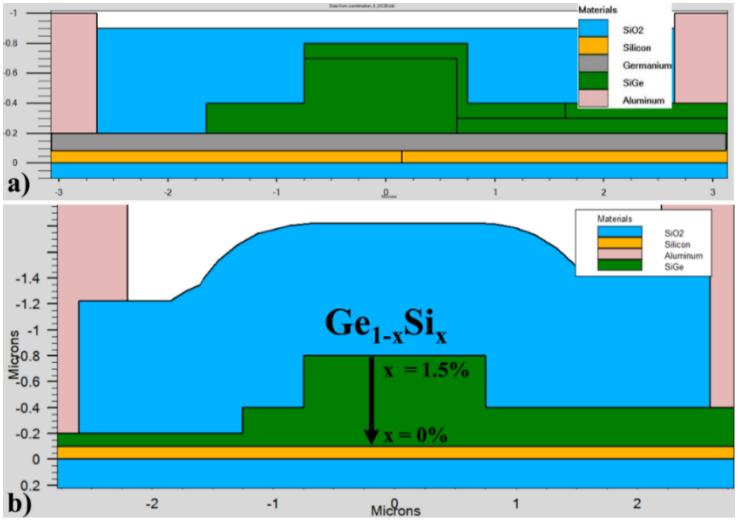

Figure 5-7 Device cross-section (a) built with Devedit™ presents sharp layer boundaries, making the simulation routine faster. (b) The device cross-section is built using the process approach (Athena), the Ge and GeSi layer are defined together by varying the silicon concertation with depth (arrow).

The Franz-Keldysh script examined in section 5.1 is implemented in M1 (Figure 5-6 in black), the electric field values are retrieved from S2 and used as input for M1, this routine calculates the material complex refractive index as a function of wavelength, strain, material composition and electric field. The output from M1 and S2 are, then, combined in M2 to produce a refractive index mesh for the device cross-section at any given reverse bias and solve the modes; a flow chart of M2 is depicted in Figure 5-8. The final output is the mode distribution, the ER the DC FOM and the FOM(t), as defined in section 5.1.1.

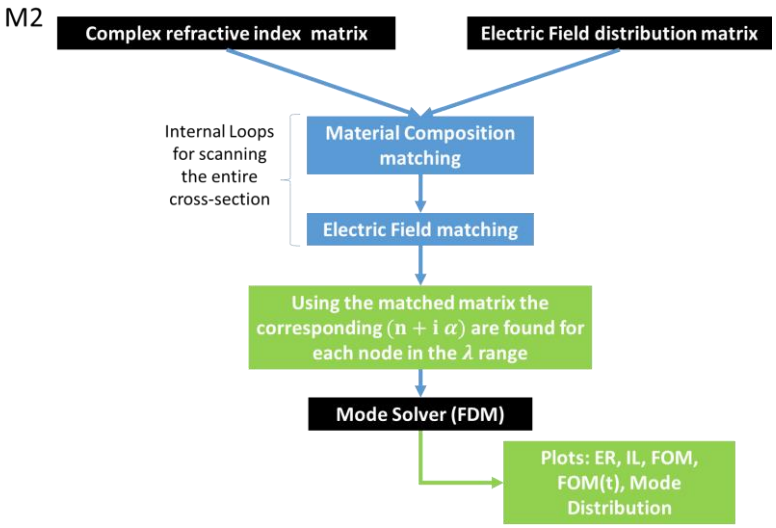

Figure 5-8 M2, Mode solver script Flow chart. The complex refractive map from M1 and the electric field distribution from S1 are interpolated and fed to the mode solver that calculates the modes dependent from wavelength, material composition, device design and applied bias.

M2 applies two routines graphically represented in Figure 5-9, the first routine retrieves the cross-section mesh (red dots) from Silvaco Atlas™ files and maps the material composition in the mesh whose density is varied for finding the best trade-off between simulation accuracy and computational complexity. Finer mesh (spacing of few nanometres) is chosen at material boundaries to better simulate the electric field distribution at the interfaces whereas a coarser mesh (hundreds of nanometres) is chosen were the material is uniform and thus a more uniform electric field is expected. In Figure 5-9 this operation is depicted with a red table showing the device mesh with dots (not in scale). The second routine by applying the FKE model (M1) at each node, calculates the complex refractive index for different reverse biases and wavelengths generating a four-dimensional matrix dependent from material composition, electric field, wavelength and strain (gold table). Once the mapping is complete, the Mode Solver is called.

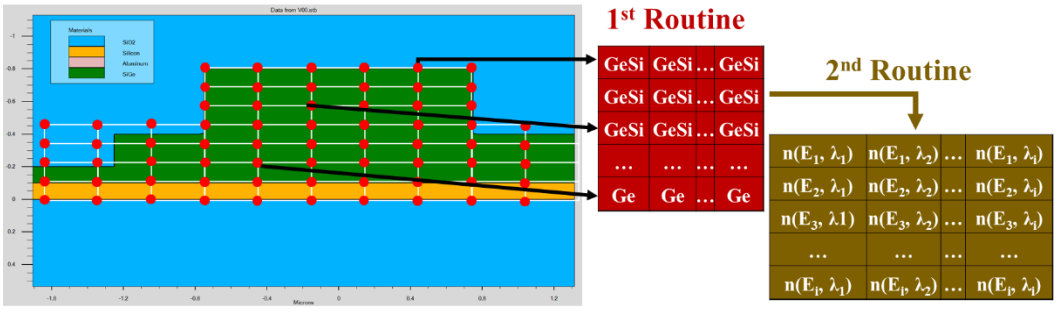

Figure 5-9 M2 routines, for each node the corresponding refractive index is found. The mesh in white is not to scale and is shown as coarse to demonstrate the principle. The routine reads in each node composition (red table) and calculates the complex refractive index for each wavelength and bias (gold table), the result is fed to the mode solver.

The chosen solver, developed by Thomas Murphy and available on Mathworks® File Exchange [185], calculates the transverse magnetic components of the field at each

node (red dots in Figure 5-9) for both TE and TM polarisation; the effective refractive indexes are, then, used to calculate the device IL, ER and FOM. The simulation platform first solves the modes for static voltages, then by selecting the resulting maximum FOM value (Max_{FOM}) and the correspondent wavelength $\lambda_{Max_{FOM}}$, the optical modes are solved in the time domain.

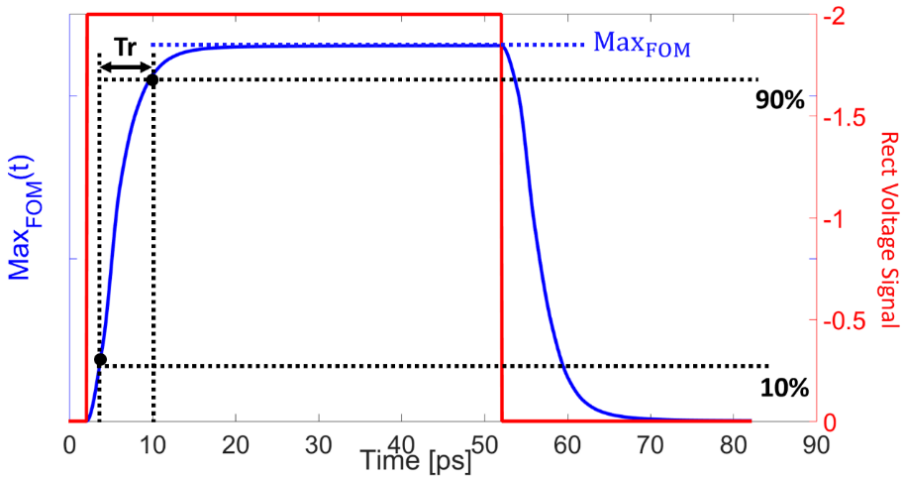

Figure 5-10 In red the transient electric signal applied at the device contacts, in blue the resulting time dependant optical efficiency (FOM against time).

While keeping fixed the wavelength to the $\lambda_{Max_{FOM}}$, the simulator applies a time dependant rectangular voltage signal across the diode contacts (red line in Figure 5-10) and calculates the electric field distribution against time. The modes are then solved in time and the speed of the EAM is calculated as $3dB = 0.35/Tr$ [132], where the rise time Tr is found from the time efficiency response (blue plot in Figure 5-10) by taking the elapsed time for the response to go from the 10% to the 90% of its maximum, as depicted in dashed lines in Figure 5-10.

The simulation platform can simulate multiple designs automatically by setting a matrix of values for one or more "input variables".

5.2.1 Simulation Platform Validation

Simulation validation has been carried out to control the platform accuracy; for this purpose, the device cross-section from reference [30] was simulated and compared with the real device.

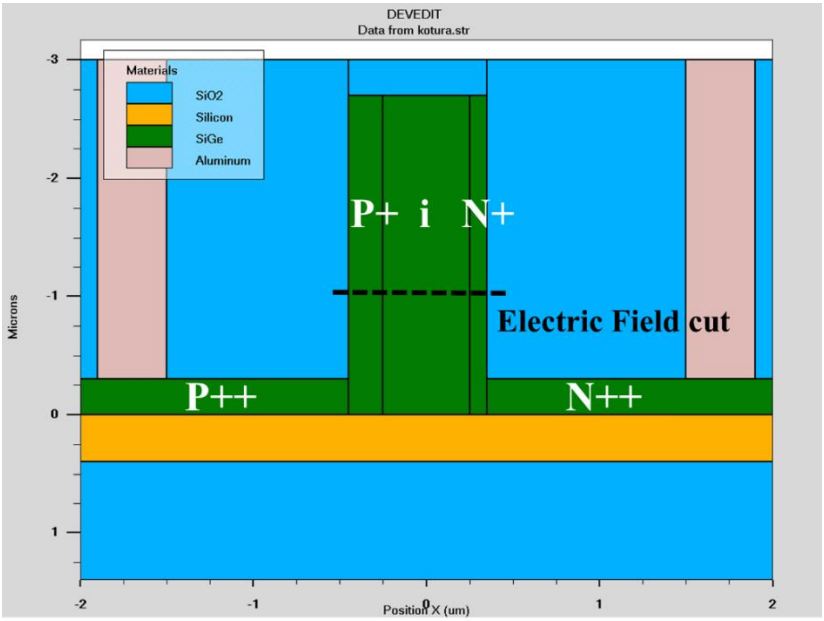

Figure 5-11 Device cross-section simulated in Devedit™ of the device found in reference [30].

The structure is depicted in Figure 5-11, the active layer is made with an alloy of $Ge_{99.15\%}Si_{0.85\%}$, the waveguide width is 0.8 μm and the height is 2.7 μm. The diode P+ doping sidewall is 0.2 μm wide, the N+ one is of 0.1 μm wide, the intrinsic GeSi layer is 0.5 μm wide, the device is 50 μm long.

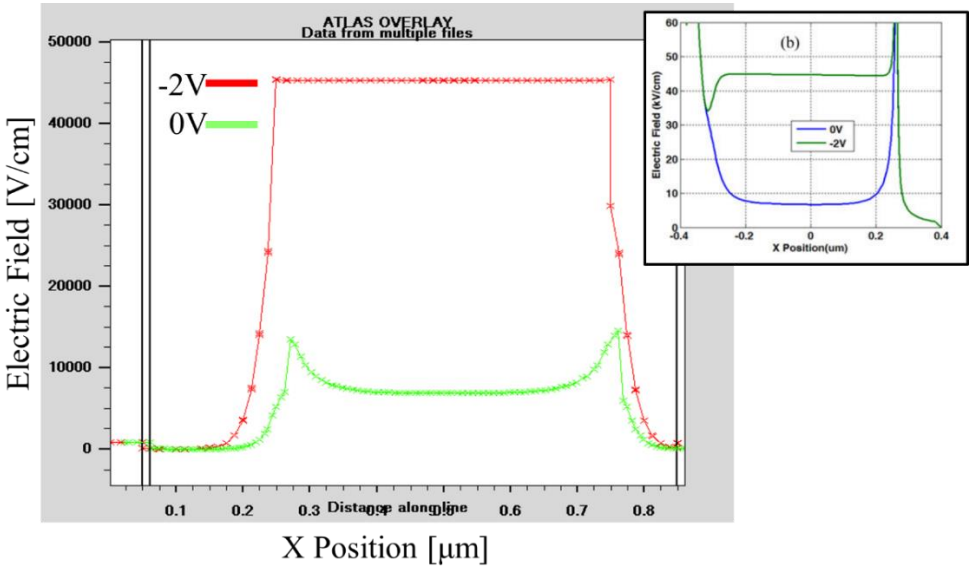

Figure 5-12 electric field cut along the dashed line of Figure 5-11 for 0 V (green curve) and -2 V (red curve) bias, in the inset result reproduced from reference [30].

The electric field distribution is simulated and compared with reference [30] as shown in Figure 5-12; the electric field values are approximately 8 kV/cm for 0 V and 45 kV/cm for -2 V in the region from 0.3 to 0.7 μm, and agree with results found in reference [30] in the region ±0.2 μm as shown in the inset. The simulation platform output is compared with the real device in Figure 5-13, the ER plots from reference [30] are imported

and shown with dashed lines, while the full lines represent the simulation results. In order to centre the ER peaks, the simulation is run with a strain value of 0.05% instead of the 0.2% from reference [102] otherwise a 10 nm redshift is found. The peak values are quite close to the reference with an error of less than 0.5 dB apart for the -3 V case where the difference is above 1 dB probably due to electric field distribution simulation inaccuracy.

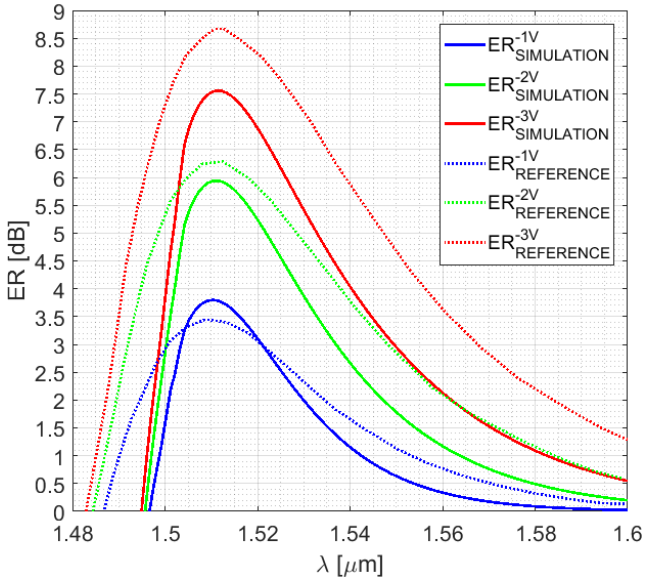

Figure 5-13 ER(λ), in dashed lines the experimental results imported from reference [30] with full lines the simulated device. In this case the silicon content is 0.85% but the strain is reduced to 0.05%, if 0.2% of strain is used the plots are redshifted of about 10 nm.

This comparison, affected by the lack of important information such as fabrication tolerances and implant depth, shows the limitation of the platform found in the constant material composition, strain and constant temperature, which may affect the ER peak position and width. Nevertheless, the platform accuracy is good enough to compare cross-sections with different characteristics, to assess the reference design for this project.

5.3 Device Simulations

Designs were simulated to find the best trade-off between FOM and device speed. In this section simulations are examined. The first set aimed the effect of the junction doping levels (Si P+ and GeSi N+) on the device performance; once the best trade-off was found, the second set of simulations investigated the doping recipes to implement in the first fabrication run. In the third set, doping well alignments with respect to the centre of the device have been studied for defining design variations to include in the process masks.

In the last part, DC simulations for comparing designs with and without a Ge buffer layer, are presented.

In Figure 5-14a, the cross-section template of the device is drawn, a layer stack of 0.1 µm Si (yellow), 0.1 µm Ge (grey) and 0.6 µm GeSi defines the device active region. The rib is 1.5 µm wide and 0.4 µm tall, on the left side, a deeper etch is conceived to realise the P++ contact doping in the Ge layer. In Figure 5-14b the doping layers are depicted, two high doping concentrations (1E20 cm^{-3}) for the doping contacts are realised in the Ge layer on the left slab (1), and on the right GeSi slab (2) with thickness of 0.1 µm. The PIN junction is formed between the silicon slab (3) and the rib (4); silicon is doped P+, the GeSi rib is intrinsic for thickness of 0.5 µm whereas on the top 0.1 µm the N+ doping is realised with a wrap-around shape, needed to contact the doping with the GeSi N++ doping contact (2). Additional low doping layers are defined to consider dopant diffusion from the well to the surrounding layers (6-7). The device length was chosen to be 40 µm.

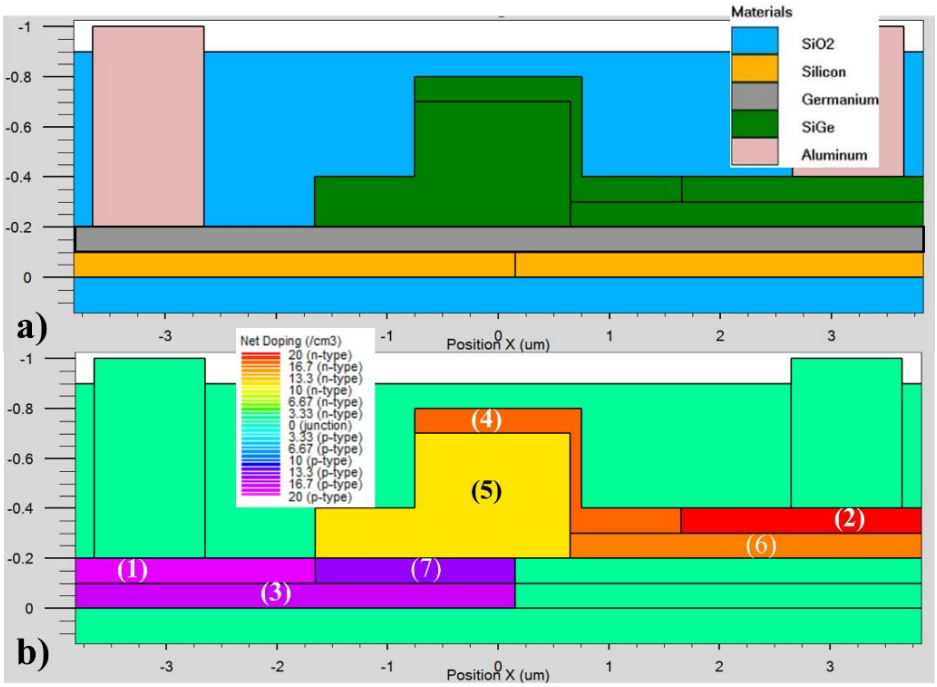

Figure 5-14 Device cross-section built with pre-determined blocks (a), characterised by fixed doping concentration (b). In the doping simulations, doping concentrations in (3) and (4) are varied. (dimensions not in scale)

5.3.1 Doping Simulations

These simulations aim to exploit the dependency of the EAM speed on the junction doping concentrations by calculating the FOM in DC and transient. For this purpose, the structure is drawn using blocks with predetermined characteristics where only the junction doping concentrations (regions 3 and 4 in Figure 5-14b) were changed in the simulation

loop. After mesh definition, the electric field distribution in DC and transient were calculated in Atlas™, the electric field and material distributions were imported in Matlab® and interpolated in space and wavelength. The complex refractive mesh at 0 V and -2 V was calculated in the FKE routine and the modes solved. In Figure 5-15a, the overlay of the electric field distribution at -2 V in rainbow colours and the TE optic mode distribution in grey confirms the quality of this design, the optic mode is well confined in the rib and an electric field up to 45 kV/cm is reached in the wide rib, as shown in the extrapolated electric field along the dashed line of Figure 5-15b (red line); at 0 V, instead, the electric field (blue line) is about 7 kV/cm and thus contributes to the total transmission loss of the device with a small FKE absorption.

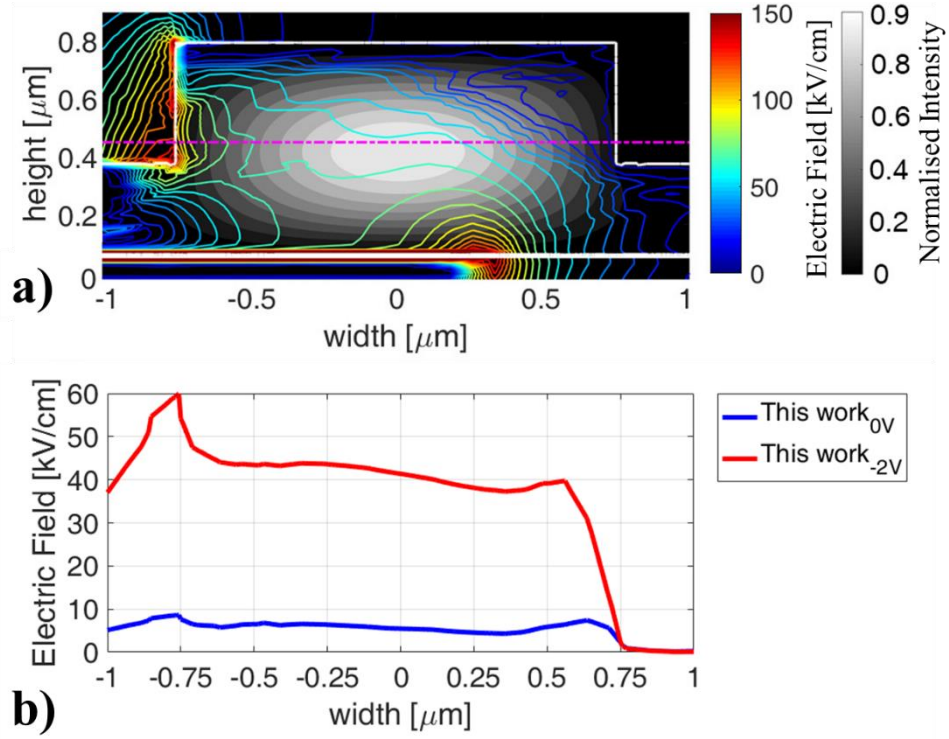

Figure 5-15 a) Overlay of the TE mode distribution (grey contour) and the electric field distribution (coloured contour) at -2 V. (b) The extrapolated electric field along the dashed line.

Three doping levels were chosen for both P and N junction wells, ranging from 1E17 cm^{-3} to 1E19 cm^{-3} (nine combinations); the contact doping distances were kept at 1.5 μm from the centre for avoiding interference on the simulations. In Figure 5-16, the resulting ER and FOM for all combinations are plotted; strain conditions from experimental fitting presented in section 7.4 were used. In Figure 5-16a, the ER peak, found at about 1.54 μm, ranges between 4.3 dB (high doping) and 4.7 dB (low doping); a second peak is also visible at about 1.58 μm due to the Ge buffer layer. In Figure 5-16b the effect of the Ge buffer layer is more evident, the FOM has two peaks. The first peak, related to the GeSi absorption spectrum, is centred at ~1.55 μm; above 1.56 μm the IL is lower, but the ER raises again

because of the Ge absorption contribution, hence the spectral efficiency (FOM) increases again and a second peak comparable with the principal one is found at about 1.58 μm. Even though this effect might be undesirable for modulation in the C-band due to higher loss caused by Ge absorption, it also extends the modulation window in the L-band, making such design desirable for many applications requiring broadband modulation. In Figure 5-16, ER and FOM principal maxima reduce slightly with increasing doping because on one hand the electric field strength at reverse bias does not increase enough with doping concentration to improve the FKE, on the other hand higher losses at 0 V bias are caused by the built-in electric field being directly proportional to the junction doping. The peak due to the Ge layer instead increases for higher doping concentration because a stronger electric field is achieved at all reverse biases, thus enhancing the FKE.

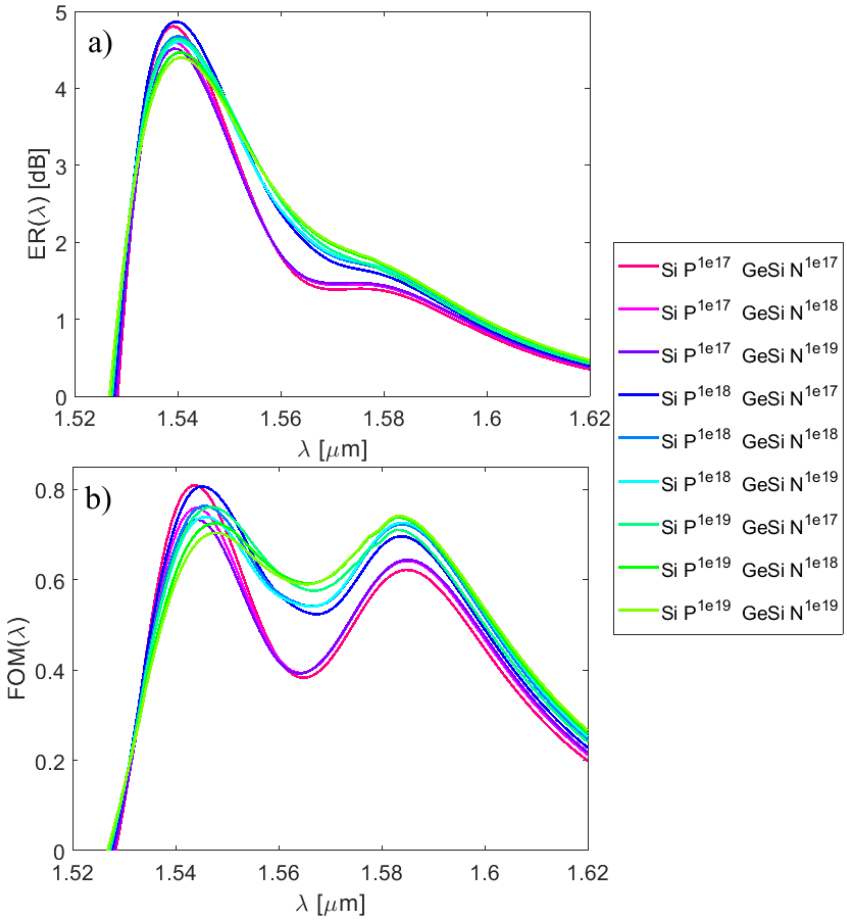

Figure 5-16 ER and FOM for simulated devices, a) ER plots show a double bell shape slightly dependants from the junction doping level; the first peak associated with the GeSi layer, centred at 1.54 μm, ranges between 4.3 dB to 4.7 dB. The second peak (1.5 – 2 dB) is centred at 1.58 μm. In b), the FOM is more affected by the Ge buffer layer, the second peak is comparable to the principal one, extending the operation window of this design to the L-band.

In transient, the time dependant FOM was calculated around 1.55 μm, the output of this simulation set is depicted in Figure 5-17; the efficiency response in time for the

different designs depends on the doping levels, showing that low doping levels dramatically affect the device speed. In Figure 5-17, combinations with silicon P+ doping of 1E17 cm^{-3} (pink curves) do not reach the asymptotic value; for medium P+ doping level (1E18 cm^{-3}), instead, the device speed increases while the FOM peak decreases proportionally to both P+ and N+ doping concentration. High doping concentrations enhance the switching speed due to junction resistance reduction but at cost of higher built-in electric field, hence losses.

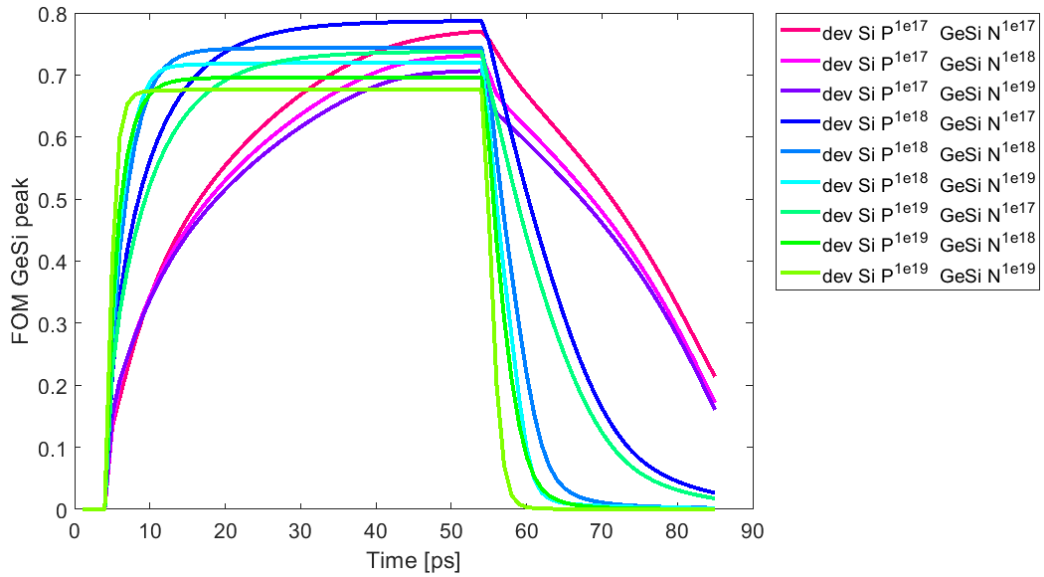

Figure 5-17 $Max_{FOM}(t)$ for different P and N doping levels. For boron concentration below 1E18 cm^{-3} (plots in pink shades), the asymptotic FOM value is not fully reached meaning that the device RC constant is too big for high-speed operation. Higher doping concentrations ensure faster speed at cost of reduced FOM peak (plots from blue to green).

Table 5-1 summarizes the results of Figure 5-17 excluding results from the boron low doping concentration (1E17 cm^{-3}, plots in pink shades) due to asymptotic FOM level not reached, meaning that the device RC is too big for high-speed operation. For medium doping levels (1E18cm^{-3}, curves in blue shades), the device speed is between 29 GHz and 84 GHz, $Max_{FOM}(t)$ reduces from 0.79 up to 0.72. High doping levels (1E19 cm^{-3}, green curves) give the highest bandwidth, up to 198 GHz with a $Max_{FOM}(t)$ ranging between 0.74 to 0.68. If efficiency reduction is tolerable, then, higher doping levels should be selected to fabricate faster devices.

Table 5-1 Doping Simulation Results, the results from the low boron concentrations (pink shades plots in Figure 5-17 have been removed being not reliable.

Doping Concentration [cm^{-3}]		3dB Band [GHz]	$Max_{FOM}(t)$	Max FOM DC
P	N			
1.00E+18	1.00E+17	29	0.79	0.81
1.00E+18	1.00E+18	66	0.74	0.76
1.00E+18	1.00E+19	84	0.72	0.74
1.00E+19	1.00E+17	29	0.74	0.76
1.00E+19	1.00E+18	95	0.70	0.74
1.00E+19	1.00E+19	198	0.68	0.74

From these simulations it can be concluded that the boron concentration in the P side of the EAM junction plays an important role in determining the device switching performances and must be chosen carefully. For the fabrication run high doping concentration for both N+ and P+ doping well was chosen to obtain high-speed performances whilst retaining a reasonably high FOM. In the next section, implant simulations tackling the doping concentrations chosen here, are presented.

5.3.2 Implantation Recipe Simulations

Once the doping conditions were set, doping simulations were made to develop the implantation recipes employing the Athena™ version of the simulator and the Monte Carlo implant simulation model [163] using as inputs the kinetic energy, dopant dose, tilt and rotation angles defined in section 4.1.1.3. In the first set, implantations on bulk material to develop the implant recipes for the highly doped contact wells (Figure 5-18), were simulated for P++ in Ge (a), and N++ in GeSi (b) targeting an active dopant concertation of 1E20 cm^{-3} for phosphorus and boron.

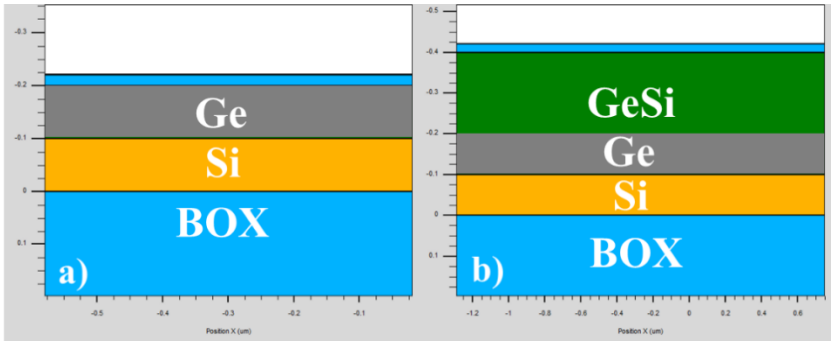

Figure 5-18 Bulk structure used in (a) Ge P++ and (b) GeSi N++ doping implant simulations. In green the target material thickness is 100 nm for Ge and 300 nm for Ge/GeSi, to reflect the targeted thickness in the device.

P++ type doping was simulated in bulk Ge using BF_2 to study the dopant depth profile; the structure implemented is depicted in Figure 5-18a. On standard SOI wafer, 100

nm Ge (grey) is deposited, followed by 25 nm PECVD oxide; the layer thicknesses were chosen to reflect the real device condition (left side slab of Figure 5-14, region number 1). Two simulation matrices are presented, in Figure 5-19a the kinetic energy was 45 keV, in Figure 5-19b the energy was 70 keV, in both cases doping concentration was varied between 1E13 ions/cm^2 (blue curve) and 2E15 ions/cm^2 (cyan curve), the dopant flux was tilted by 5° respect the wafer while the wafer was rotated of 270°; doping peak and uniformity across the whole thickness was assessed with dots highlighting the concentration peak. Differences are found in the doping distribution versus depth, with 45 keV the dopant peak is found at about 30 nm from the surface, then concentration drops quickly (Figure 5-19a). Increasing the energy (70 keV) concentration peak shifts in depth with more uniform distribution (Figure 5-19b) at the surface, however, the concentration is reduced; higher energy, in fact, permit to better penetrate the material.

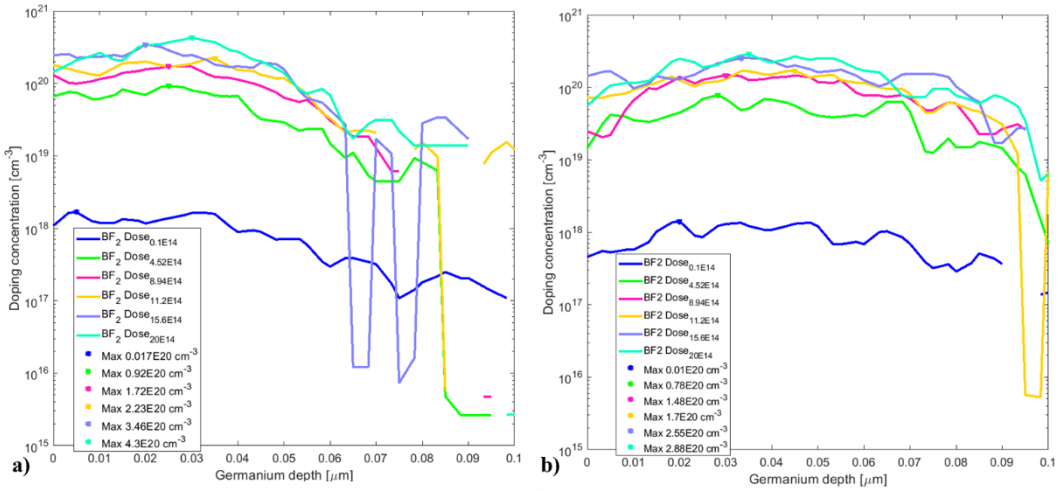

Figure 5-19 BF_2 doping simulation SIMS in Ge, kinetic energy is 45 keV (a) and 70 keV (b) while the dose is varied between 1e13 to 20 e14 ions/cm^2, the doping peak is highlighted with dots.

For N++ doping, implant on GeSi was simulated with phosphorus. The structure used is depicted in Figure 5-18b, also in this simulation, layer thicknesses were chosen to reflect the real device thickness and composition (right side slab of Figure 5-14, region number 2); on standard SOI, 100 nm Ge (green) was deposited, followed by 200 nm of GeSi with 1.5% Si content; the final layer is 25 nm PECVD oxide. The key aspect of this doping was to confine the high doping concentration ideally on the top 100 nm of material with a steep drop of dopant concentration in few nanometres. In the real device, in fact, the slab underneath was designed to be intrinsic. In this case, the kinetic energy was swept between 15 keV and 60 keV, whereas dose was varied from 1E14 ions/cm^2 to 2E15 ions/cm^2, the dopant flux was tilted of 5° respect the wafer while the wafer was rotated of 90°; simulation results are plotted in Figure 5-20 for the (a) low and (b) high kinetic energy, dots highlight the dopant peaks. The doping concentration is proportional to the ion

concentration for a given kinetic energy, a minimum 1E14 ions/cm^2 is required to fulfil the concentration >5E19 cm^{-3}. The kinetic energy impacts on the doping distribution, at low energy (Figure 5-20a) the doping peak is at the GeSi surface, but a considerable concentration drop is found in less than 50 nm. With 60 keV energy (Figure 5-20b), the doping peak is found deeper in the material, and more importantly is wider, giving a more uniform dopant concentration in the whole thickness (150 nm), but the doping concentration at the surface is lower.

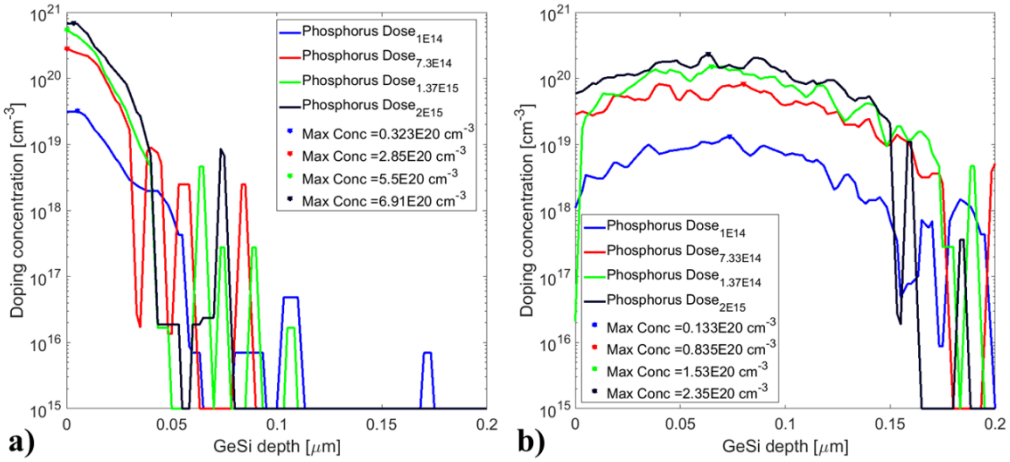

Figure 5-20 Phosphorus doping simulation SIMS in GeSi, (a) kinetic energy is 15 keV, (b) kinetic energy is 60 keV. In both simulations, the dose is varied between 1E14 to 2E15 ions/cm^2; the doping peak is highlighted with dot.

For the first fabrication run, a dual step implant for both P++ and N++ was chosen, an implant with higher energy but lower dose was done first to form a ~100 nm thick highly doped well, followed by a second implant at lower energy but higher dose to improve dopant concentration at the surface for reducing contact resistance.

Table 5-2 Implant simulation summary for the highly doped contacts with the recipes that meet design conditions.

		P++, BF_2	N++, Phosphorus
Material		Ge	GeSi
Target Doping		1E20 cm^{-3}	1E20 cm^{-3}
1st	Energy	70 keV	60 keV
	Dopant dose	1E15 cm^{-2}	1E15 cm^{-2}
2nd	Energy	45 keV	15 keV
	Dopant dose	2E15 cm^{-2}	2E15 cm^{-2}
Tilt		5°	5°
Rotation		270°	90°

In Table 5-2 the implant recipes are summarised. For P++ implant, BF_2 with dose 1E15 cm^{-2} and kinetic energy of 70 keV was first executed, followed by an implant with 2E15 cm^{-2} dose and 15 keV energy. For the N++ doping, in the first implant at 60 keV a phosphorus dose of 1E15 cm^{-2} ions was implanted followed by a 15 keV implant with 2E15 cm^{-2} dose, simulations of the recipes used in fabrication is shown in Figure 5-21. In Figure

5-21a, the GeSi layer has a phosphorus concentration peak of 6E20 cm^{-3} at the surface and a uniform phosphorus concentration of about 1E20 cm^{-3} for the following 100 nm, a doping concentration of 1E18 cm^{-3} is still present at 200 nm of depth. In Figure 5-21b the boron concentration in Ge has a peak of about 5E20 cm^{-3} close to surface, whereas deeper in the layer a concentration between 1E20 cm^{-3} and 1E19 cm^{-3} is achieved. In Figure 5-22a-b the implantation species and orientations are drawn for the GeSi N++ (a) and Ge P++ (b) as they were executed during fabrication, the implantation steps are presented in section 7.1.

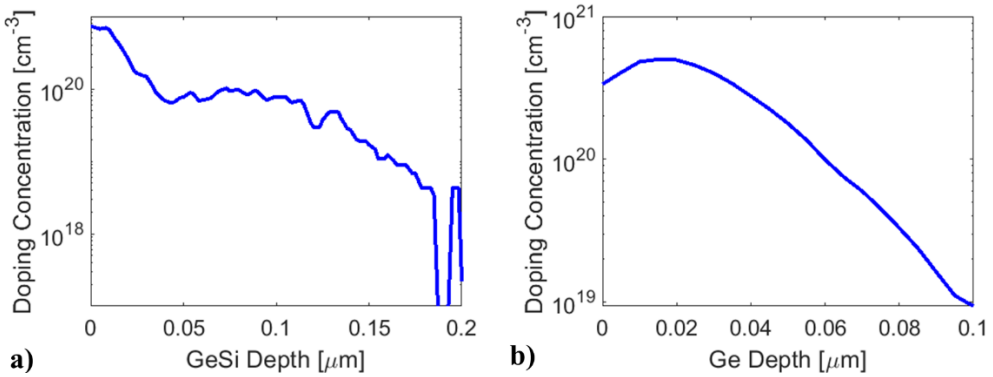

Figure 5-21 Simulation of the dual step implant recipe used in fabrication for N++ (a) and P++ (b).

In the second set of implant simulations, the doping recipes to define the PIN junction were studied by building the structure with Athena™ following CMOS standard fabrication steps.

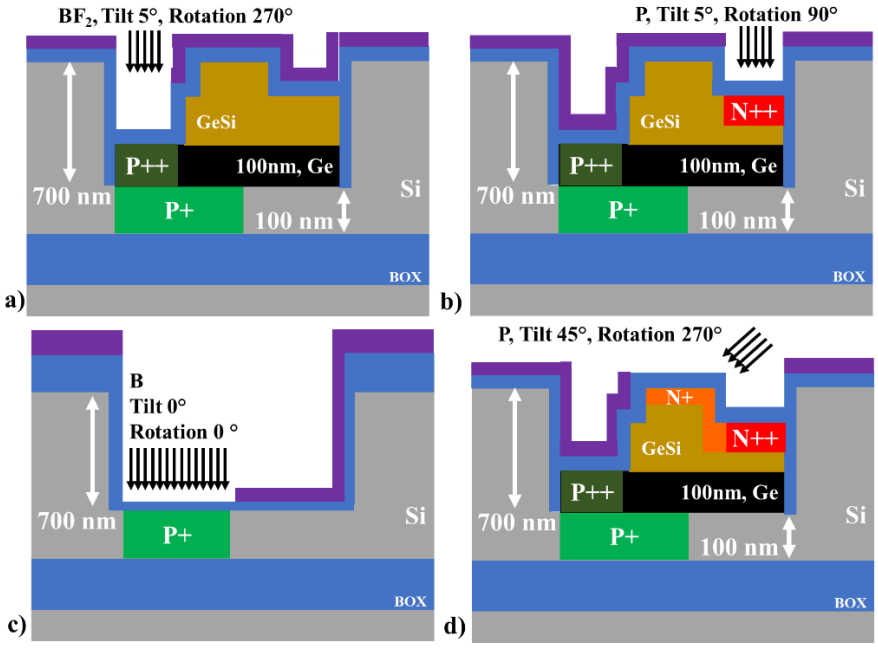

Figure 5-22 Doping implant simulation schematics, (a) BF_2 P++ doping in the Ge layer to form the contact doping and (b) P for the N++ doping in GeSi, in both cases 5° tilt and rotation of 270° and 90°, respectively. (c) Si doped P+ with tilt and rotation angles of 0° to ensure doping confinement in the cavity flat surface. (d) GeSi N+ angled implant with tilt angle of 45° and wafer rotation of 270° to form the wrap-around doping shape.

In Figure 5-22, the Si P+ doping (c) and the GeSi top rib N+ angled doping (d) species and orientations are drawn, the implantation steps are instead presented in section 7.1. For Si tilt and rotation were set to 0° to ensure implant in the silicon bottom layer only; for the top rib waveguide, the N+ implant was conceived with 45° of tilt and wafer rotated by 270° to realise the wrap-around shaped doping. In Figure 5-23, (a) the cross-section for standard design and the resulting doping concertation (b) for high doping recipes, are reported.

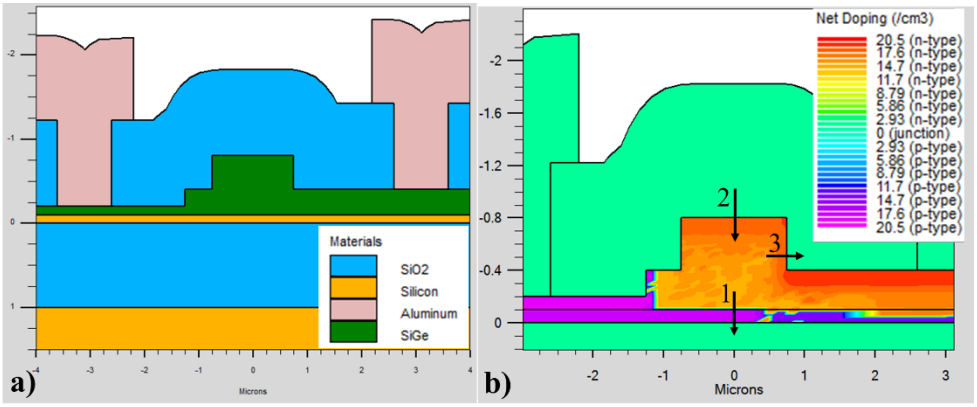

Figure 5-23 Device cross-section used for implant simulations, b) active dopant concentration, in red/orange is phosphorus, in blue/purple boron; intrinsic level is cyan. Arrows show the direction of SIMS analysed in the simulations.

For the thin silicon layer, two boron implants were tested varying the dopant dose between 1.61E14 ions/cm^2 and 3.11E14 ions/cm^2 while keeping fixed the energy to 30 keV. Tilt and rotation were set to 0° because this implant was conceived in the thin Si layer inside the 700 nm deep cavity etch, an angled implant could cause doping of regions outside the targeted one. In Figure 5-24, the boron concentration in the Si layer is depicted along arrow number 1 of Figure 5-23b.

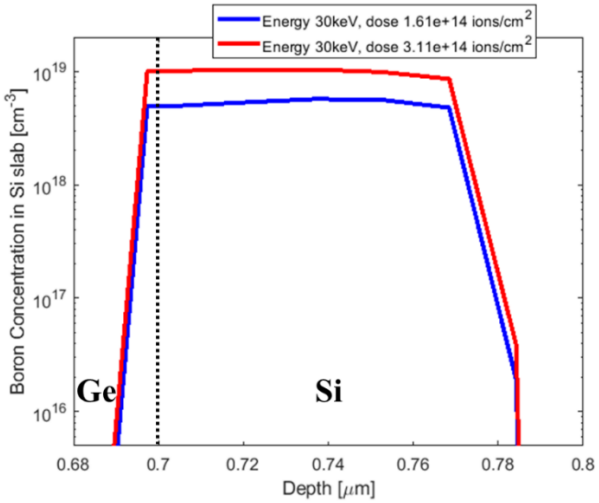

Figure 5-24 Bottom slab Si P+ doping SIMS taken from Figure 5-23b region number 1, in this case only the dose was varied between 1.61E14 ions/cm^2 and 3.11E14 ions/cm^2.

No differences in distribution are found in boron implant recipes, the penetration is uniform across the whole thickness (~0.1 μm), the activated dopant reaches ~4E18 cm^{-3} and ~1E19 cm^{-3} with dose of 1.61E14 ions/cm^2 and 3.1E14 ions/cm^2, respectively. High dopant recipe was selected for fabrication.

It was chosen to exploit six conditions for the N+ doping by varying the implant energy and the dopant dose; due to the wrap-around doping shape, a 45º angled implant was developed with wafer rotation of 270° to ensure a uniform 0.1 μm thick doped layer on the top flat and right side of the rib. In Figure 5-25 SIMS simulation results, along arrows number 1 and 2 of Figure 5-23b, are plotted from the top rib (Figure 5-25a) and rib side (Figure 5-25b) for phosphorus. It was found that lower energy recipes produce high doping concentration at surface with narrow implantation depth, whereas higher energy permit better ions penetration resulting in a flatter doping distribution in depth; the total dopant concentration, instead, depends on the ions concentration. The implant recipe with energy of 60 keV and phosphorus dose of 5E13 ions/cm^2 gives the best results in terms of active dopant concentration (~5E18 cm^{-3}) and depth (~100 nm) for the wrap-around N+ doping; however, recipes with 1E14 ions/cm^2 (pink and yellow curves in Figure 5-25a-b were chosen to ensure a high doping level on the real device.

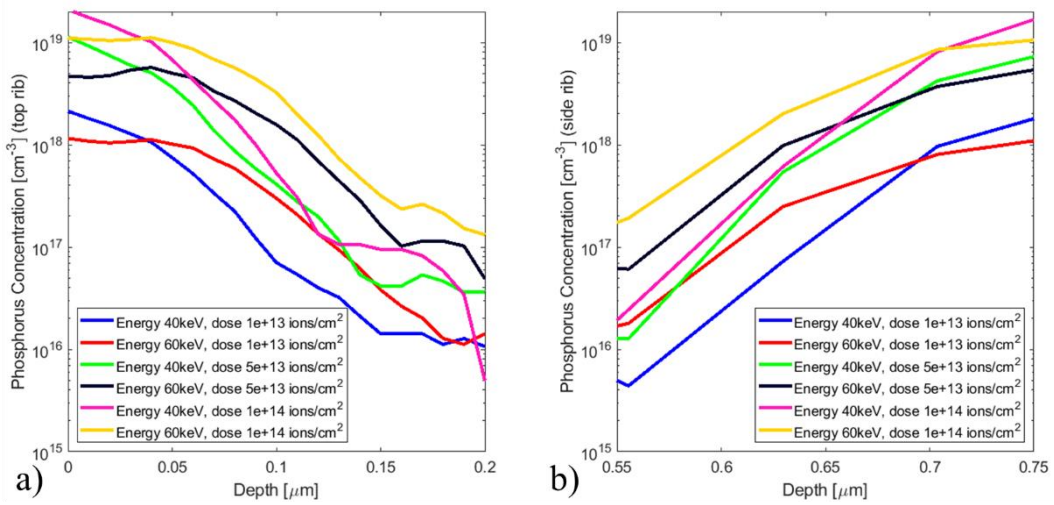

Figure 5-25 SIMS taken from Figure 5-23b for the doping simulations; (a) top rib GeSi N+ doping energy (region number 2) was varied between 40 keV and 60 keV, ions concentration instead were set to be 1E13 to 1E14 ions/cm^2, in (b) the side GeSi rib N+ doping (region number 3), obtained with the angled implant, is shown being the bridge linking the N+ junction doping with the N++ contact doping.

The implantation recipes are summarised in Table 5-3.

Table 5-3 Implant simulation summary for the junction doping with the recipes that meet design conditions.

	P+, Boron	N+, Phosphorus
Material	Si	GeSi
Target Doping	5E18 cm^{-3}	1E19 cm^{-3}
Energy	30 keV	40 keV
Dopant dose	3.108E14 cm^{-2}	1E14 cm^{-2}
Tilt	0	45
Rotation	0	270

5.3.3 Layout Simulations

The simulation platform allows to define custom designs. In this section, simulations exploring device performances linked to doping positions are presented. Athena™ platform version was used to test the process with fixed doping concentration, targeting 5E18 cm^{-3} to 1E19 cm^{-3} for P+ and N+ junction doping. Thanks to this process-oriented method that includes simulations of dopant diffusion and etching, a device cross-section closer to real device can be obtained.

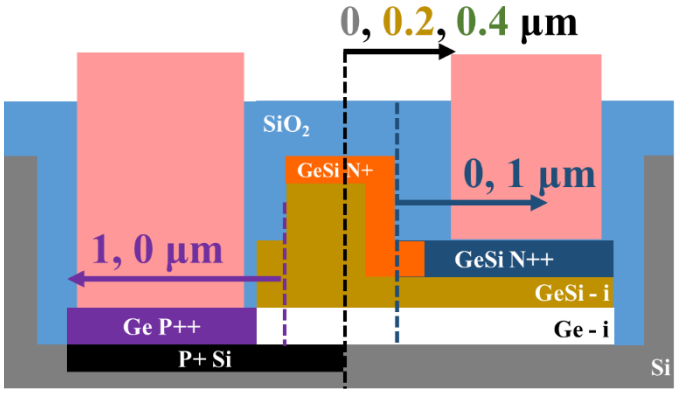

Figure 5-26 Simulations variables shown on the cross-section device from Table 5-4, grey to green for the Si P+ right edge distance from the rib centre, purple and blue for the right and left edge distance from the rib centre of Ge P++ and GeSi N++ well, respectively. Arrows pointing towards the shift direction and distances, are also depicted.

The contact and junction doping were changed according to Figure 5-26, in which arrows point towards the doping edge shift respect the cross-section centre; three combinations are divided in groups (grey, gold and green) referring to the Si P+ right edge position respect the rib centre, ranging from 0 µm to 0.4 µm. For each group, four combinations were exploited by changing the distance between the contact doping edges to the rib centre (purple and blue arrows), from 0 µm to 1 µm. DC simulations were carried out with and without reverse bias (-2 V), consequentially, high-speed simulations were executed. In Table 5-4 all combinations are summarised with relative Max DC FOM and 3dB bandwidth in GHz.

Table 5-4 Simulation results using process approach for different design parameters (shown with different colours), grey refers to Si P+ right edge shifted centred with the rib, gold and green are shifted of 0.2 µm and 0.4 µm, respectively. For each group, the contact doping edge distance from the edge rib from is varied from close (0 µm) to far (1 µm). Max DC FOM and 3dB bandwidth are reported.

Structure	Si P+ [µm]	GeSi N++ [µm]	GeSi P++ [µm]	Max DC FOM	3dB band [GHz]
1 grey	0	0	0	0.72	114
2 grey	0	0	1	0.76	97
3 grey	0	1	0	0.72	76
4 grey	0	1	1	0.77	79
1 gold	0.2	0	0	0.75	98
2 gold	0.2	0	1	0.78	88
3 gold	0.2	1	0	0.73	71
4 gold	0.2	1	1	0.79	72
1 green	0.4	0	0	0.78	86
2 green	0.4	0	1	0.8	76
3 green	0.4	1	0	0.77	62
4 green	0.4	1	1	0.81	63

The impact on both device speed and FOM is mostly determined by the alignment of the bottom P+ doping well (black box in Figure 5-26) and the top wrap-around N+ doping well (orange box in Figure 5-26), which forms the vertical PIN structure.

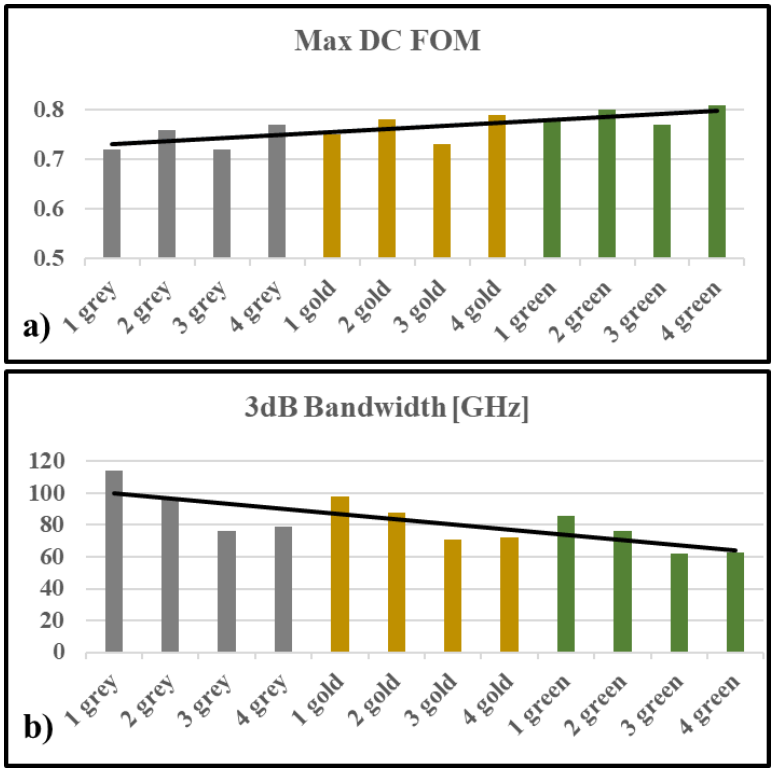

Figure 5-27 (a) Max FOM and (b) 3dB bandwidth performances shown in a graph with trend.

Trends are shown in Figure 5-27 for the FOM (a) and the 3dB bandwidth (b), respectively; increasing the extension of the P+ well over the top N+ well (moving from grey to green set in Table 5-4), improves FOM at the expense of the device speed.

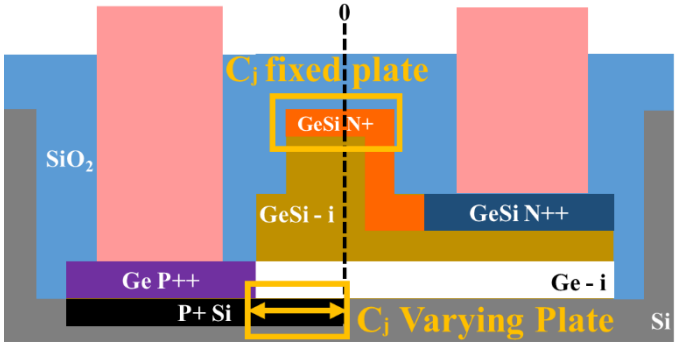

Figure 5-28 The bottom P+ doping width determines the junction capacitance (C_J) by varying the capacitance plate associated with it, shown at the bottom of the junction with an arrow. The top plate, instead, is fixed being defined by the rib width.

When the bottom P+ doping extends more to the right (black box in Figure 5-28), in fact, the vertical junction (yellow rectangles in Figure 5-28) has a bigger area, therefore, the electric field distribution is more uniform, enhancing the FOM peak but the junction capacitance increases as well, reducing the device speed.

Keeping fixed the extensions of the Si P+ doping well (black block) and varying the contact doping positions (P++ in purple and N++ blue colours in Figure 5-26) a small variation of the FOM occurs, mostly dependent from the P++ doping, due to a variation of the built-in electric field. In Figure 5-29 the built-in electric field cut along the rib for different contact doping positions reveals a peak of about 2.6E5 kV/cm on the left side of the rib, when the P++ doping is close to the edge (red and blue curve); for P++ far from the rib edge, the electric field peak disappears (green and cyan curves). On the other side of the rib, the N++ position does not interfere much on the electric field strength and a small peak (1.2E5 kV/cm) is always found. In the centre of the rib, however the electric field is uniform in all cases, so that the overall effect of the doping distance to the DC performances is minimum, up to 4% (green device 1 and 4 in Table 5-4).

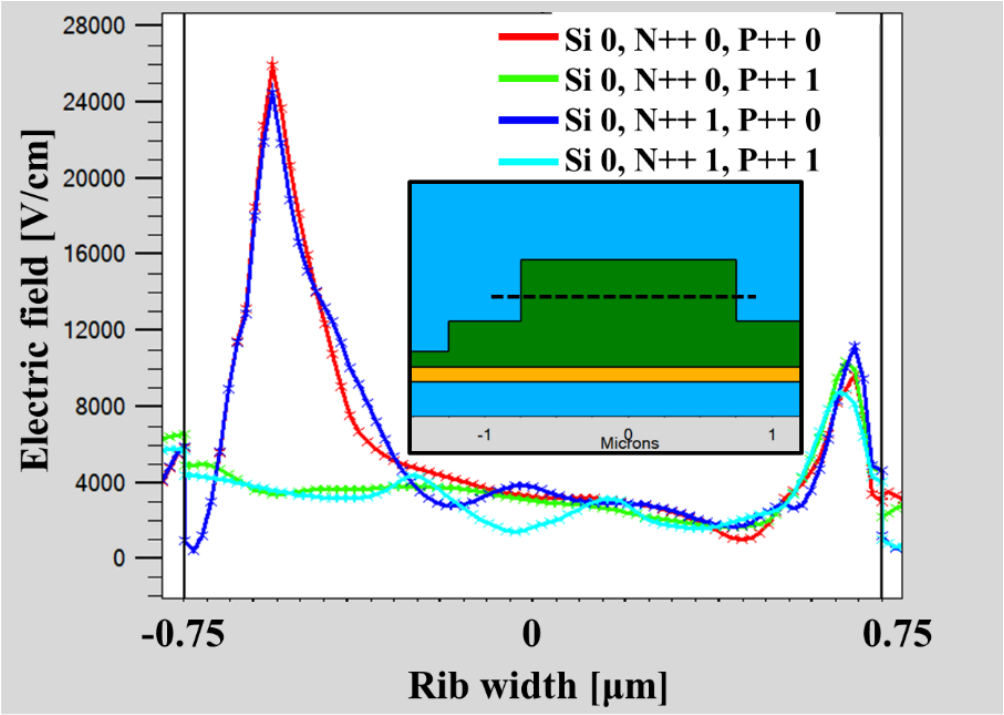

Figure 5-29 Built-in electric field along the rib width (dashed line in the inset) for the grey device group. A peak on the left side is visible for combinations with P++ contact doping close to the edge of the rib, causing a reduction of FOM.

In high-speed, however, contact doping distances are relevant, when the contact doping edges are far from the waveguide edges (dashed purple and blue lines in Figure 5-26), the junction capacitance width increases so the device time constant increases as well, penalising the device speed; vice versa when the contact doping are close to the waveguide. To maximize the FOM and speed design device "1 green" from Table 5-4 was chosen as reference.

Comparison of simulation methods (Devedit™ and Athena™) is possible through device "4 gold" in Table 5-4, being the closest design to that in section 5.3.1, with high junction doping level, contact doping far from the rib and silicon P doping right edge at 0.2 µm from the rib centre. It is found that Athena™ simulation calculates a slightly better FOM DC peak (~9% higher) but more importantly a 3dB bandwidth ~25% lower than that calculated with the Devedit™ version; those differences are linked to the ideal doping conditions (concentration, depth and uniformity) and etching profile of Devedit™ method that generate a PIN junction with constant doping concentration with reduced parasitic capacitance.

5.3.4 Ge buffer layer

In simulations presented so far, designs included the Ge buffer layer needed to grow the GeSi stack, as described in section 4.2.2.1, which might be disadvantageous in terms of efficiency. In this section a comparison with the same device containing a uniform GeSi layer, is proposed.

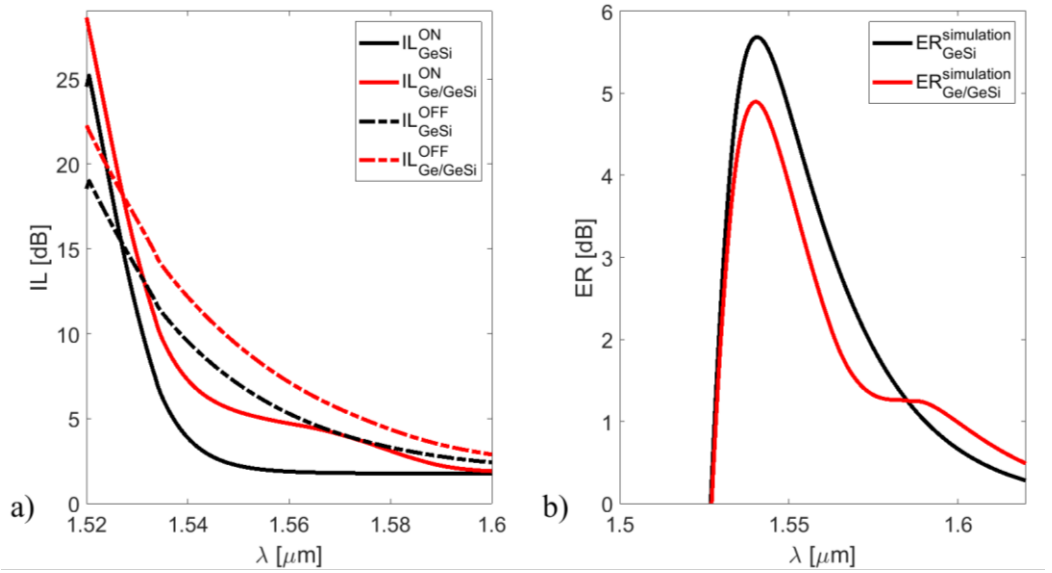

Figure 5-30 (a) IL at different voltages for the device containing the Ge buffer layer (red lines) and the device with uniform GeSi (black lines), showing the lower and monotonic behaviour of the latter; b) ER for the device containing the Ge buffer layer (red line) and the device with uniform GeSi (black line), the second peak is visible in the former design that also reaches a lower principal peak than the device lacking Ge buffer layer.

In Figure 5-30a, the ILs for 0 V (full lines) and -2 V (dashed lines) are drawn for both devices, in red the standard Ge/GeSi epitaxial stack, in black the uniform GeSi epitaxial layer. The first noticeable difference is the reduced ILs for device without Ge buffer layer; the second and more important difference is the monotonic behaviour in wavelength of its ILs. Losses associated to device containing the Ge buffer (red curves) are, instead, higher and the IL for 0 V (full line in red) presents a secondary lobe at about 1.58 μm. For this device (Ge/GeSi), in fact, the IL is not only due to propagation losses, and GeSi absorption but also to absorption linked to the Ge buffer layer, which is shifted over redder wavelength than that of GeSi. The underlying Ge layer, being an inevitable residual of the adopted GeSi growth technique and not a design choice, is then responsible of the second ER peak for wavelengths above 1.57 μm, visible in Figure 5-30b. The Ge buffer layer is also responsible of the principal ER peak reduction of about 1 dB respect the device without Ge (black curve).

A better epitaxial growth recipe that avoids Ge deposition or blends it with Si to form a uniform GeSi layer would improve dramatically the IL, thus improving DC efficiency, as shown in Figure 5-31 where FOM for both devices are drawn. The FOM peak of the device with uniform GeSi (black plot) is four times the standard Ge/GeSi one (red plot); it should be noted, however, that the secondary peak in the Ge/GeSi device extends the device operation window in the L-band range due to a flat FOM spectrum. If lower FOM is acceptable, the efficiency spreading can be exploited in applications requiring operation in both C-band and L-band without varying material composition and/or design.

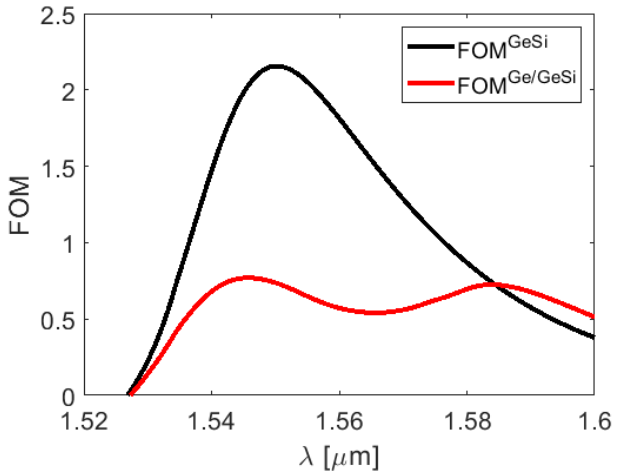

Figure 5-31 FOM for the Ge/GeSi (red) and GeSi (black) device, showing a higher peak of the latter but a flatter behaviour of the device that includes the Ge buffer layer, alloying exploiting this design in the L-band.

5.4 Simulations of Passive Structures

Additional studies were carried out to define grating couplers design with coupling efficiency simulations and taper design by evaluating the conversion efficiency, mode overlap at the Si-GeSi cavity interface to evaluate the power loss due to propagation in waveguides with different aspect ratio and transmission simulations to evaluate the effect of angled cavity sidewalls formed during the H_2 precleaning (section 4.2.2.2).

5.4.1 Grating Coupler and Taper Design

Passive simulations in Lumerical MODE and FDTD Solutions were carried out by Dr. Thalia Dominguez Bucio to design GCs and tapers. Details on the simulation code developed for tapers and CGs are available in reference [261]. Light was coupled into devices through grating couplers realised on a silicon waveguide, to evaluate the coupling

efficiency between optic fibre and waveguide depending on dimensional characteristics and alignment. To define the GC design, FDTD simulations (section 4.1.2.3) were carried out varying GC period and duty cycle for finding the design with the highest coupling efficiency at 1.55 μm for a given etch depth. Gratings, in fact, were realised during the waveguide definition, therefore the etch depth was fixed to 400 nm. In Figure 5-32, the cross-sectional view of the GC realised on an 800 nm SOI wafer is depicted. A coupling angle between optic fibre and GC of 10° was chosen, whereas the grating width was chosen to be 10 μm to ease alignment with the fibre core, being about 11 μm for SMFs. The initial duty cycle, the ratio between the tooth width and the gap between two consecutive teeth, was set to 50%.

Parameter	Value
Teeth number	43
Λ	510 nm
Duty Cycle	30%
Grating Gap	153 nm
Coupling Angle	5°
(1) Cladding Thickness	500 nm
(2) Rib etch	400 nm
(3) Slab thickness	400 nm
(4)BOX thickness	3000 nm

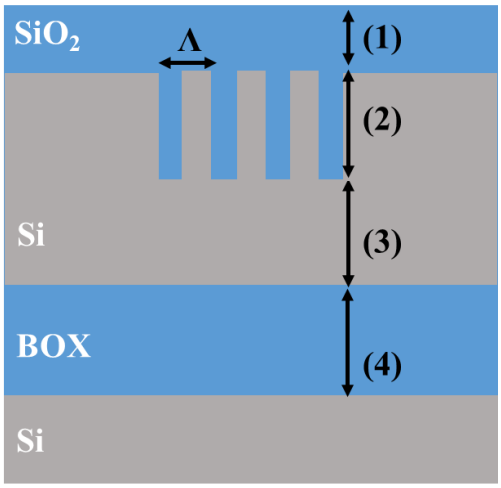

Figure 5-32 Specifications and lateral view of the GC realised on an 800 nm SOI wafer, in the table the optimised parameters to maximise the coupling efficiency at 1.55 μm.

Batch simulations varying period, duty cycle and coupling angle converged to the GC design summarised in the table of Figure 5-32. The total tooth count is 43 with a period Λ = 510 nm and 30% duty cycle, the grating gap is 153 nm, and the coupling efficiency is maximised at 1.55 μm with a coupling angle of 5°. In Figure 5-33 the transmission spectrum is reported. A peak of 0.47 (47% of power coupled from the optic fibre to the waveguide) is found at 1.548 μm, in line with the efficiency (about 50%) of uniform grating couplers found in literature [262].

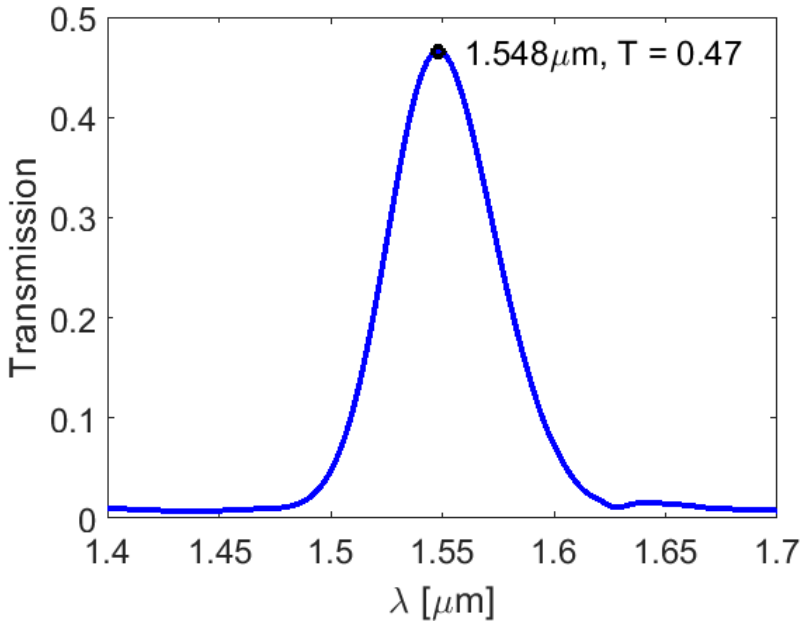

Figure 5-33 Coupling efficiency for the GC defined in the table of Figure 5-32.

Tapers are generally used to couple light in different sized waveguides by modifying the beam spot size/shape of a guided mode by slowly varying the waveguide cross-section. The beam conversion is achieved adiabatically, for which the local first-order mode of the waveguide propagates in the taper with (ideally) no variation to higher or radiative mode [263]. Simulations to evaluate the conversion efficiency as a function of taper length were carried out to select correct design. Details on the waveguide design are given in section 5.5.3.

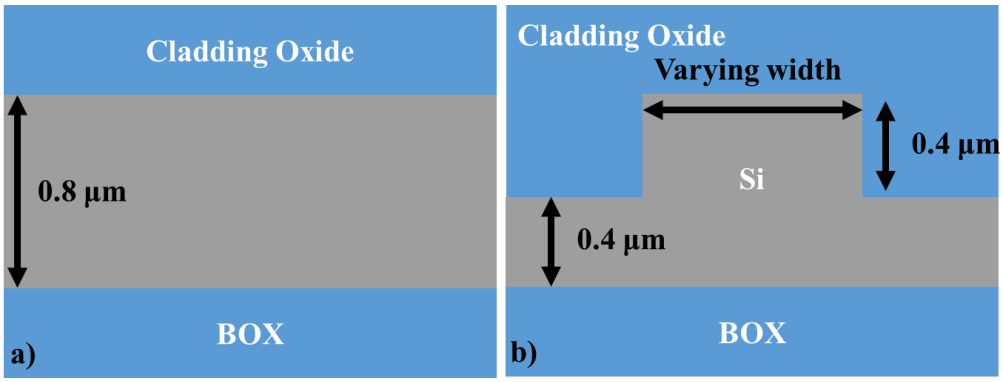

Figure 5-34 (a) Structure to calculate the minimum effective refractive index to support mode propagation in a slab waveguide, (a) waveguide cross-section with varying rib width used to evaluate the effective refractive index for the fundamental and first higher modes for both TE and TM polarisations.

Two adiabatic tapers were simulated, one going from 10 µm to 3 µm width to facilitate alignment between the input/output optic fibre and the GCs at the edge of the waveguide and a "mode filter" taper to prevent propagation of higher modes than the fundamental mode. Dispersion curves of Si waveguide against rib width were simulated

using Lumerical MODE Solutions to define the mode taper. First the cut-off conditions, defined as the minimum effective refractive index that allows guided propagation in a slab waveguide (Figure 5-34a) was calculated, then by sweeping the rib width of the Si waveguide realised on the 800 nm platform (Figure 5-34b), the effective indexes at 1.55 μm for the fundamental and first higher mode for both TE and TM polarisations, were calculated. In Figure 5-35 the dispersion curves are reported, if the rib width is below ~1 μm, only the fundamental mode (TE0 and TM0, in blue and red) have an effective index higher than cut-off (magenta dashed line). That is, by reducing the rib from 3 μm to 0.7 μm (cyan dashed line in Figure 5-35) the "mode filter" taper would ensure that only the fundamental mode propagates in the device waveguide.

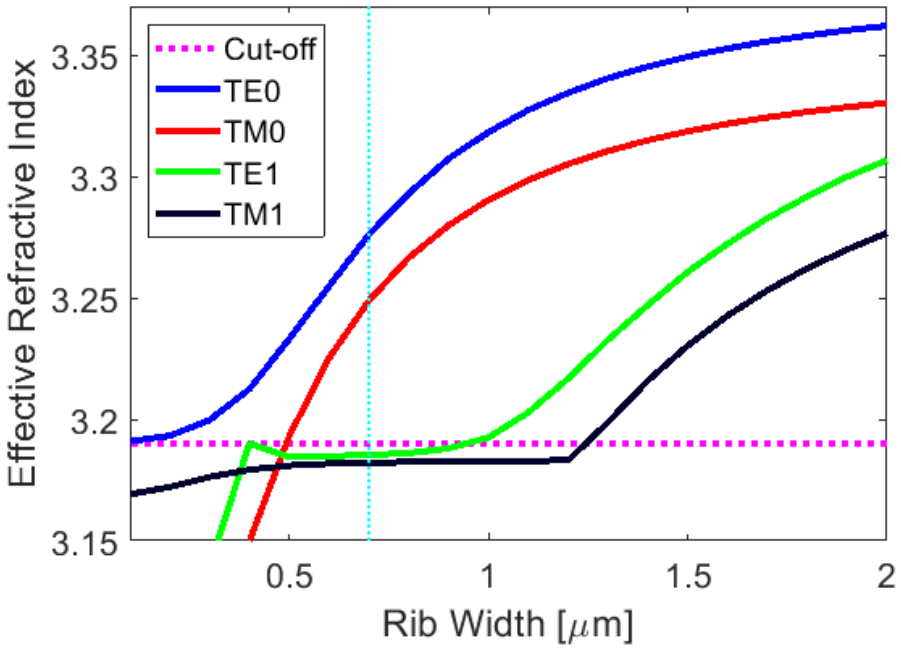

Figure 5-35 Dispersion curves for a Si waveguide, width spans from 0.1 μm to 2 μm. In magenta the minimum effective index that allows mode propagation, in cyan the propagation condition at 0.7 μm rib width.

Tapers were simulated with the EME solver of Lumerical MODE Solutions [188] (section 4.1.2.2), taper length was varied from few micron up to 600 μm to evaluate the conversion efficiency for the fundamental mode, results are shown in Figure 5-36.

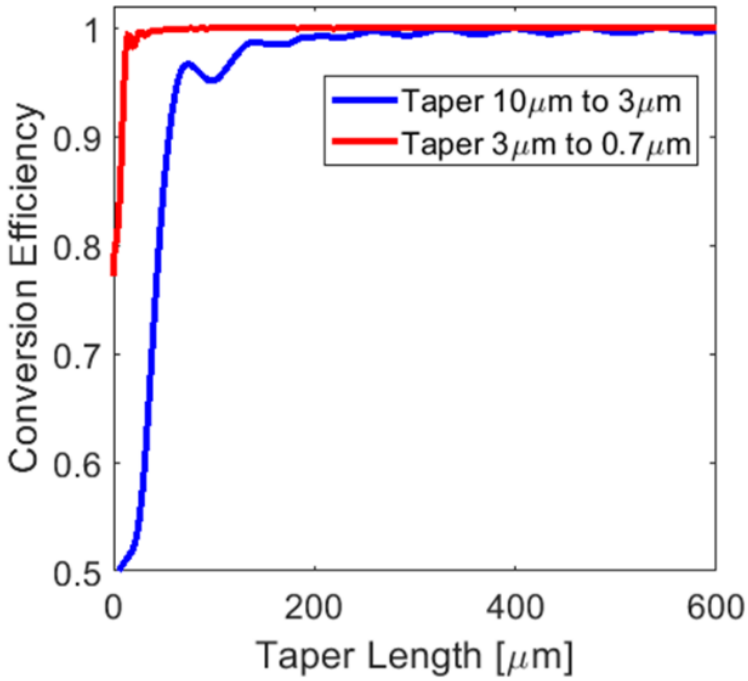

Figure 5-36 Conversion efficiency of the taper from 10 µm to 3 µm and the taper from 3 µm to 0.7 µm evaluated by varying the taper lengths until asymptotic value was reached.

In both tapers a length longer than 200 µm gives conversion close to unity with small oscillations caused by mode beating. In the waveguide design, an additional taper from 0.7 µm to 1.5 µm was also included in the layout to expand the waveguide rib from the mode filter to the device width. In this case, the minimum length required to have full conversion can be taken from the second simulated taper (red curve of Figure 5-36), being those tapers very close in design. To ensure full conversion and no ripples, tapers were designed with a length of 600 µm.

5.4.2 Mode overlap Simulations

Mode overlap simulations (section 4.1.2.2) were carried out by Dr. Thalia Dominguez Bucio on passive devices to evaluate coupling loss at the Si-GeSi cavity interface. For simulations, Lumerical MODE Solutions was used where the overlap analysis engine enables to easily calculate the percentage of power coupled between waveguides made with different materials.

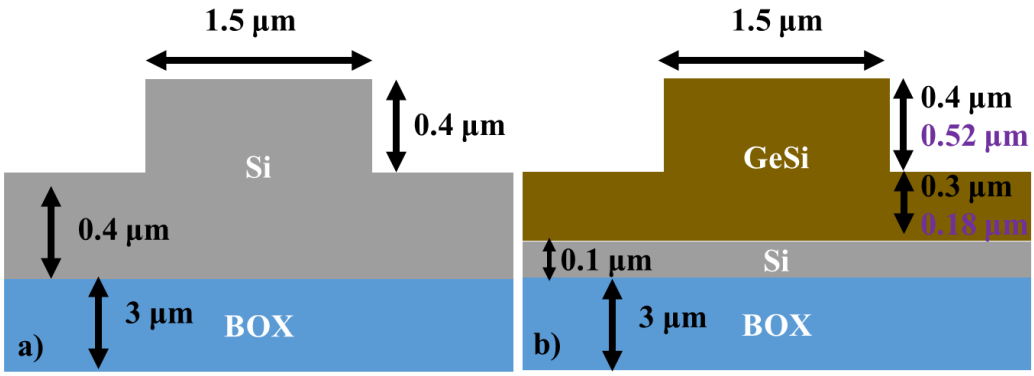

Figure 5-37 Device cross-section of (a) Si waveguide, (b) GeSi waveguide, in purple the over-etched GeSi waveguide.

Two simulations were run, in Figure 5-37 on a SOI wafer with 800 nm Si overlay. Waveguides are realised with Si (a) and with a staked layer (b) comprising 100 nm Si and 700 nm of GeSi. In the first simulation, waveguide cross-sections with rib height of 400 nm, rib width of 1500 nm and slab thickness of 400 nm were considered for both cases. An interface loss was calculated for the TE mode of 0.27 dB. In the real process, waveguides passing through the GeSi device cavities were defined in a single step by etching on the same time Si and GeSi, GeSi etch rate however is faster than Si (up to 30% with the standard etch recipes used in this project) [189][190], thus in the GeSi waveguide (Figure 5-37b) the rib height was set to 520 nm and the slab thickness to 280 nm (purple text in the figure). An interface loss of 0.31 dB per facet was found for the TE mode, suggesting that a small variation in waveguide thickness would not impact on the device IL.

5.4.3 Transmission Simulations of Angled Interfaces

In section 4.2.2.2 it was shown that H_2 precleaning before GeSi growth can lead to Si reflow of the surface atoms at lower temperature than the Si melting point, smoothing the trench sidewalls. In FDTD, transmission simulations (section 4.1.2.3) for evaluating the impact of the sidewalls smoothing to the optical power transmitted at the Si-GeSi interface were carried out. In Figure 5-38, the structure simulated is depicted, (a) the lateral view of the cavity shows on the right side the slanted sidewall defined with an angle $\theta = \tan^{-1}(0.6/0.7) = 40.5°$ defined from the cavity thickness (0.7 µm) and the base (0.6 µm, measured experimentally) of the triangle formed by the slanted wall and the normal to the wafer (Figure 5-38a, dashed line). In Figure 5-38b-c, the rib cross-sections are depicted, (b) outside the cavity the rib has 1.5 µm width and 0.4 µm height, inside the cavity (c) the rib in GeSi has same dimensions of the Si rib, whereas the slab is formed by a 100 nm thick Si layer and 300 nm thick GeSi. The GeSi complex refractive index was replaced with a

real refractive index of 4.12, value interpolated from reference [50] at 1.55 μm, to focus the attention on the effect of the slanted sidewall only.

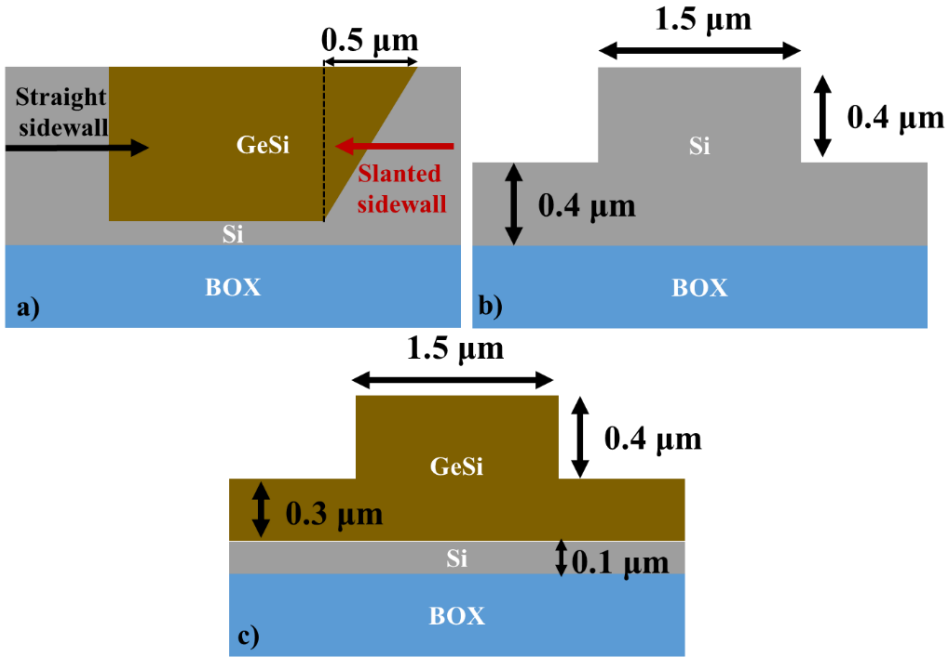

Figure 5-38 (a) Lateral view of the cavity showing the straight sidewall on the left and the slanted sidewall on the right, arrows point to the simulation directions. (b) and (c) show the waveguide cross-section outside and inside the cavity.

Simulations, whose results are shown in Figure 5-39, were run on the straight sidewall first, and on the slanted sidewall afterwards. In the case of straight sidewall (blue curve), transmission was found to be about 98.6% of the total input power, for slanted sidewall instead 96.9% (red curve); with a transmission difference of only 1.7%, the effect of the slanted sidewall was expected to not compromise the device operability.

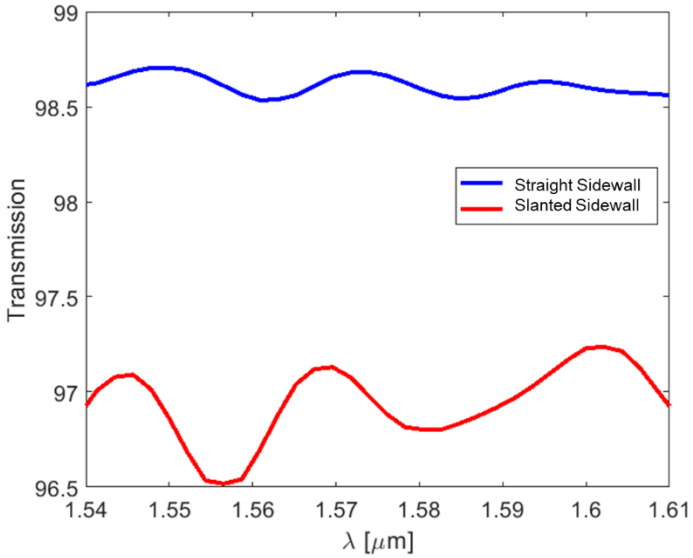

Figure 5-39 Transmission simulation results inside the cavity for the straight (blue) and slanted (red) sidewall. The imaginary part of the refractive index of GeSi was not considered, the real part was set to 4.1.

5.5 Mask layout

Results from simulations (sections 5.3 and 5.4) were used to define fabrication masks, coded in Tanner L-edit. The complete set of masks consists of ten layers to define the device cavity etch with e-beam and dummy cavities etch with UV photolithography, the Si P+ doping, the dual etch step to realise the waveguide rib with GCs, the Ge P++, the GeSi N++ and GeSi N+ doping, the VIAs etch and the final metal lift-off. Mask design followed standard rules derived from CMOS technology, details are given for alignment marks, testing structures, waveguide etch step and device layout. The device design was swept across 21 devices by changing distance of the contact doping from the rib edges, as shown in Figure 5-40.

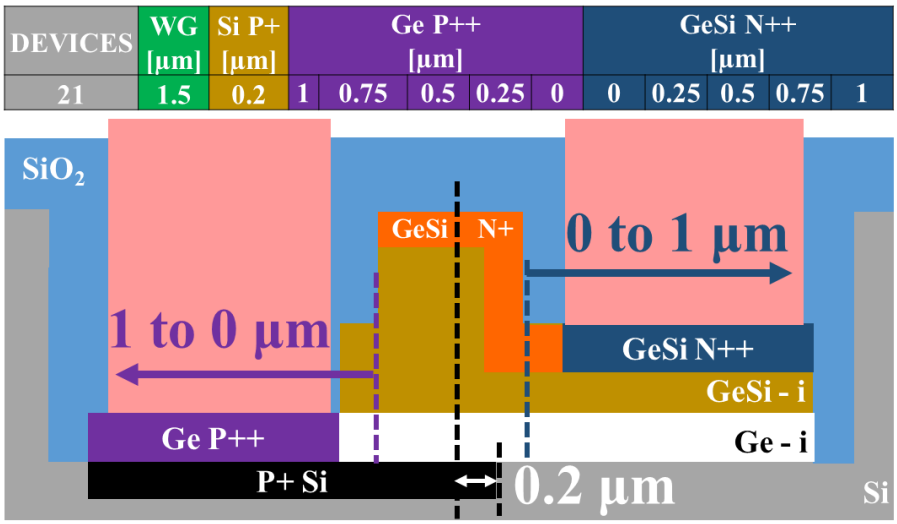

Figure 5-40 Device combinations, the Ge P++ and GeSi N++ well are shifted respect the left and right rib edges between 0 µm and 1 µm in the direction pointed by the arrows, the table on top of the picture summarises all combinations.

The GCs were instead designed with the optimised parameters, found through simulations (section 5.4.1), summarised in Table 5-5.

Table 5-5 GC design parameters.

Grating Design	Teeth number #	Period [nm]	Duty Cycle [%]	Gap [nm]
	43	510	30	153

5.5.1 Alignment Marks

The 6-inch wafer layout, depicted in Figure 5-41, is divided in cells containing devices and testing structures. On the left and right side, wafer scale alignment marks (blue squares) are defined in the first e-beam step (device cavity definition).

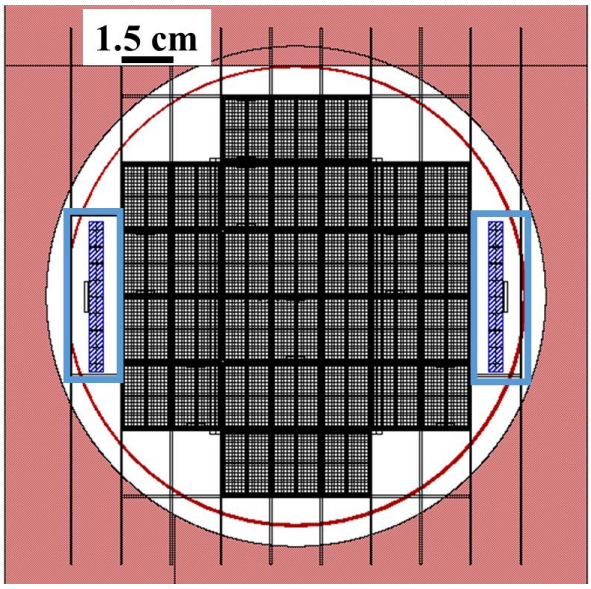

Figure 5-41 Wafer layout, highlighted in the blue squares, the wafer alignment marks for the e-beam and UV lithography.

In Figure 5-42, the wafer scale alignment marks are depicted; the crosses on the right were used for the wafer scale alignment in the e-beam tool in the following e-beam steps. The green square, visible in the close-up of Figure 5-42, is a light feature (clear glass) on the photolithography quartz plate, the yellow cross at the centre is a metal feature (dark field feature). During UV photolithography wafers were aligned to the mask by centring the metal cross on the quartz plate to the e-beam feature (four squares arranged with a gap to form a cross, pointed out by the red arrow in Figure 5-42) written on the wafer in the first e-beam step.

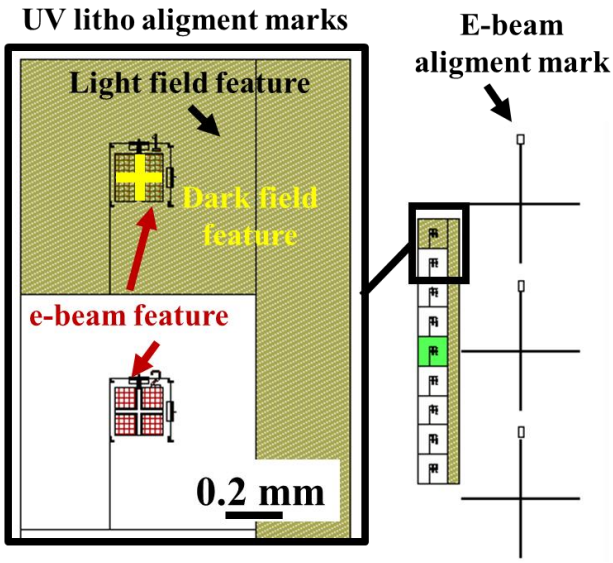

Figure 5-42 Alignment marks detail, on the right crosses written on the first e-beam step were used for wafer scale alignment in the following e-beam steps. In green the light field feature of the photolithography mask, in yellow the dark field cross used to align quartz plate and wafer (e-beam feature in red) during the photolithography process.

Marks at cell scale were included to correctly align the e-beam mask to the wafer portion (cell). In Figure 5-43 the alignment marks, written during the first e-beam step at the four corners of every cell, are depicted in magenta; the crosses were used by the e-beam to finely align electron beam and stage in all axes (x, y, z and tilt).

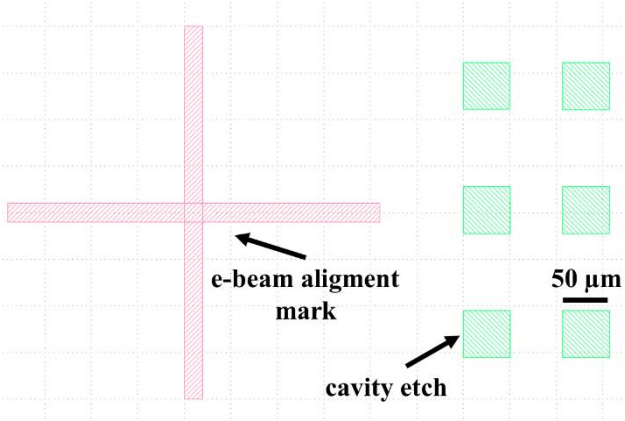

Figure 5-43 In magenta cell alignment marks written in the first e-beam step, in green the cavity etch defined afterwards with UV photolithography.

5.5.2 Testing Structures

In Figure 5-44a, the cell layout is shown, on the right (b) a close-up of the cell highlights different structures repeated on the entire cell.

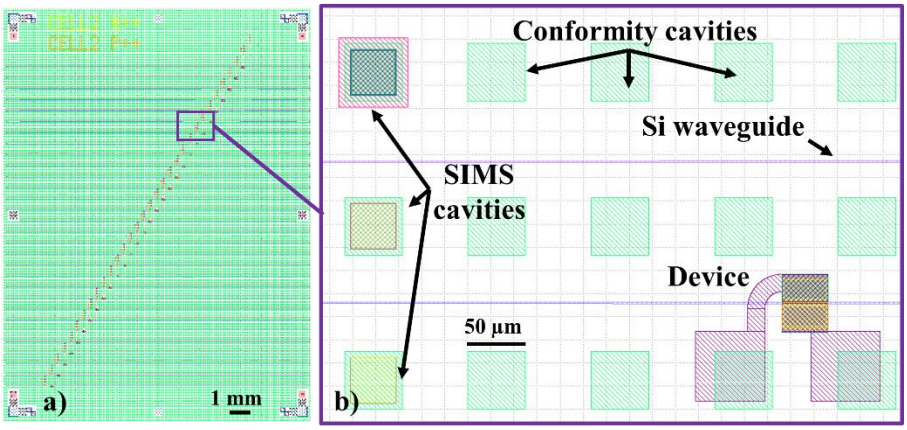

Figure 5-44 (a) Mask layout of the whole cell, (b) close-up showing the device layout, Si waveguide, SIMS and conformity cavities.

Conformity "dummy" cavities (in green) are spread on the entire wafer with a density close to 11%, to control the GeSi growth and composition being both dependant from the Si coverage (portion of the Si overlay exposed) [207][208]. This layer was converted into a photolithography mask because e-beam lithography would have been time consuming and its accuracy an overkill for this etch step.

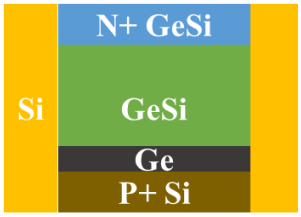

Figure 5-45 SIMS testing structures cross-section, 50x50 μm^2.

Some of these conformity cavities were used for SIMS measurements, for this purpose, additional process layers were added to dope silicon, Ge and GeSi; in Figure 5-45 the SIMS structure layout is shown.

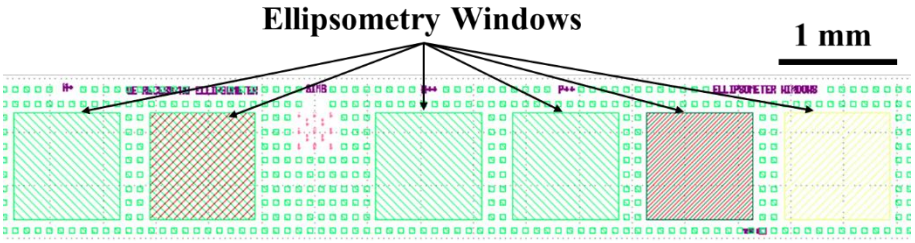

Figure 5-46 Ellipsometry windows for the dummy cavity, device cavity, waveguide and vias etches.

Other testing structures used during the process were the ellipsometry windows. Defined at the cell edges, 1 mm^2 squares (Figure 5-46) were included for all layers to control material thickness during and/or after deposition and etching process steps with the ellipsometry tool described in section 4.3.2.

5.5.3 Waveguide layout

Waveguides were written with e-beam to ensure the sub-micrometric aspect ratio (1.5 μm width and 0.4 μm height) and the long waveguide length (>1 mm) were correctly transferred to the wafer. For this layer, a fine beam spot size was chosen to increase accuracy up to 20 nm. Since the writing time is highly dependent on the layer density and e-beam spot size, waveguides were defined by drawing the rib but in the e-beam tool a Boolean operation was executed to generate patterns along the waveguide length separated by a gap equal to the rib width. By doing that, trenches were written in the ZEP resist so that by etching the exposed areas, waveguide ribs were defined between the trenches. A trench width of 2.5 μm was chosen to ensure mode confinement in the rib (trenches gap). In Figure 5-47, The Boolean operation and the resulting pattern on the resist are shown: (a) waveguide containing the CG is defined by drawing, through C+ macros, a 10 μm wide rib. Features 2.5 μm wide and surrounding the rib layout are grown with a temporary layer (b). A Boolean difference is executed between layers to define the waveguide etch as 2.5

μm trenches around the waveguide rib width (c). In (d), an image taken from an optical microscope of the ZEP resist after development is presented.

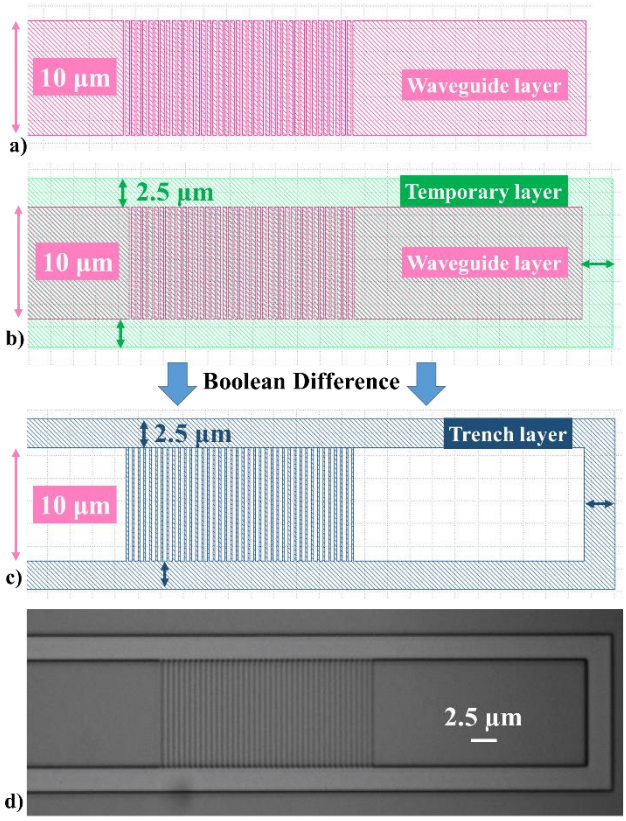

Figure 5-47 Waveguide definition (a) and Boolean operation (b) features that follow the waveguide rib is grown with a temporary layer, (c) a Boolean difference is executed to define the areas to be written in the e-beam and hence etched in ICP; (d) the waveguide definition on the ZEP after resist development.

The waveguide length was set close to the cell width. The rib width was varied along its length to ensure maximum coupling and single mode propagation. In Figure 5-48, the waveguide top-view is sketched (dimensions not in scale); the waveguide is symmetric with respect to the cavity, at the edge of the GC, tailored to support TE mode, is defined on 10 μm wide rib to maximise coupling efficiency with SMF. Two following adiabatic tapers (600 μm long) shrink the rib width to 0.7 μm to ensure single mode propagation by suppressing higher modes that might propagate. A third adiabatic taper brings the rib to the device design width (1.5 μm), this waveguide section passes through the device cavity (black square). On the other side, the tapering order is reversed and another grating on 10 μm wide rib, is defined.

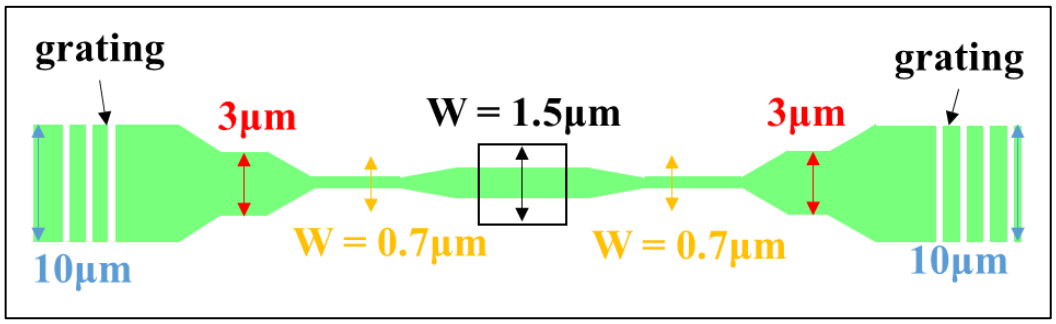

Figure 5-48 Waveguide drawing, from the left: a grating is defined at the edge of the waveguide (10 µm wide), two tapers shrink the rib to 0.7 µm to suppress optic modes different from the fundamental; a third taper brings the rib width to the designed 1.5 µm. At the other side, the design is in reversed order.

In Figure 5-44, the normalisation waveguide is visible above the device; etched on the Si overlay and being an exact replica of the device waveguide. The normalisation waveguide was used to remove the fibre-to-grating coupling loss and the propagation loss in the Si waveguide sections from the device transmission spectra. Si-GeSi interface coupling loss was instead estimated through simulations (section 5.4.2).

5.5.4 Device layout

The device cavity is defined between four surrounding dummies to maximise the layer growth conformity (Figure 5-49), all layers are confined inside the cavity apart from metal pads and waveguide layers. In the cell, devices with different contact doping distances from the rib are designed to prevent strong dopant diffusion from the highly doped wells in the rib that could limit the device performances.

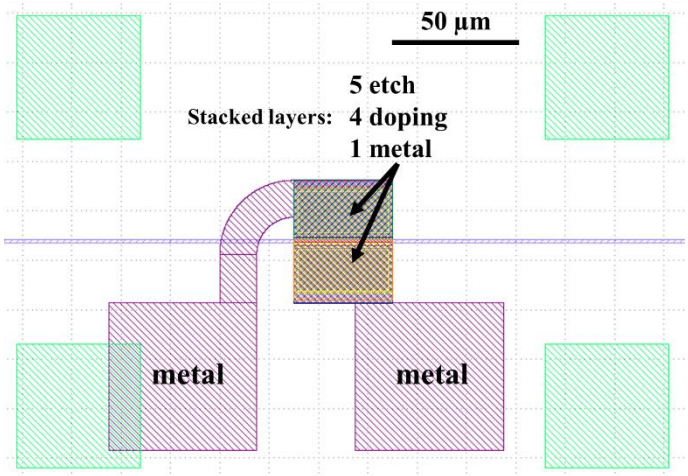

Figure 5-49 Device cavity surrounded by four dummies. 5 etch, 4 doping and 1 metal layers are stacked on each side of the cavity, separated by the rib.

Both N++ and P++ positions have been swept from 0 µm to 1 µm from the right and left rib edge, all the design parameters are summarised in Figure 5-40.

The metal layer, which was developed for lift-off, was converted in another photolithography mask. In Figure 5-49, metal lines, at each side of the waveguide, are connected to 60x60 μm^2 metal pads with a pitch of 40 μm to match the RF probe gap of the high-speed setup.

5.6 Summary

The model from reference [102] calculated with Matlab® has been presented and validated. Subsequently, the work has been focused on realising an automated simulator capable of "building" the PIN diode EAM waveguide cross-section and studying the effects of composition, strain, wavelength and electric field on the optical transmission. Three different parts oversee the structure definition, evaluation of the electric field distribution, calculation of the complex refractive index by applying the FK effect and optical mode solutions allowing to explore devices with different characteristics in an automatic fashion. Validation simulations show that the whole platform is reliable for developing a device candidate design for the first fabrication run.

The Simulator Platform has been used to build matrices of simulations. In the first one, the device was built using building blocks with predetermined dimensions and compositions, while the PIN doping concentrations were varied. The first result was that a Boron concentration of 1E18 cm^{-3} was needed to obtain a fast device. The second result, instead, was that the doping level of both wells changed dramatically the device speed. One can conclude the highest doping concentrations give the fastest device, but at the expenses of the FOM peak. The second simulation matrix investigated the dopant implant recipe development, thanks to Athena™ it was possible to mimic the fabrication process and tune the implant recipe to get the desired concentration and distribution of dopant. The implantation recipes chosen for this project are summarised in Table 5-2 and Table 5-3. The third simulation matrix, instead, focused on doping dimensions while keeping fixed the doping levels. The device was built using a process approach that enables investigation of side effects like etching profile, doping diffusion. The candidate design has been found in device "1 green" from Table 5-4. These simulations, however, confirm that faster device can be achieved if reduction of FOM peak is not an issue. Simulation comparison of devices with and without the underlaying Ge buffer layer show its influence on electro absorption efficiency by reducing the maximum ER achievable. A better conditioned epitaxial growth

that avoids the double step growth or blends the Ge layer would improve the DC optical characteristics of the EAM.

Passive simulations using Lumerical MODE and FDTD Solutions were carried out by Dr. Thalia Dominguez Bucio to define CG design, tapers design and evaluate the coupling efficiency between silicon and GeSi waveguides. An interface loss of 0.31 dB was calculated concluding small variations in waveguide thickness would not impact on the device performances.

To estimate the effect of angled sidewalls at the cavity edges, due to Si reflow [201][202], transmission simulations with Lumerical FDTD Solutions were run. It was found that a reduction in power of about 1.7% resulted for an angle of ~40° and this is considered small and will not cause major issue.

Simulations were used to define the fabrication masks which were generated in L-Edit IC Layout. On the chip, devices with different contact doping (P++ and N++) positions were realised. Unwanted diffusion of impurities in the rib, in fact, would cause a drop of the electric field and increase of optical losses, affecting drastically the device performances. By varying the position of the contact doping, the probability of having working devices was maximised. Details on the mask layout were given for the SIMS structures, the waveguide and the device.

Chapter 6

Material Tailoring

In the early stages of the project, during which the platform characteristics were not chosen, it has been possible to conduct a side study on a 500 nm SOI platform to exploit GeSi bandgap tunability by means of composition variation. GeSi alloy, in fact, can be formed with any concentration of Ge in Si, enabling easy wavelength tuning that together with CMOS compatibility, make GeSi attractive to the communication industry. A tunable material can be exploited for multiplexing purposes, extending the operation window from the E-band to L-band without changing the device design. The alloy can be "tuned" before device definition or after; in a recent work [124], cost-effective process showing the possibility to tune Si content in GeSi using rapid melt growth technique has been demonstrated, providing yet another capability to achieve custom GeSi growth. Although this technique is very promising, work still needs to be done to demonstrate waveguided devices. In this project, an experiment with RTA exploited, instead, the bandgap shift after realising waveguide in GeSi cavities. For this purpose, an SOI wafer with 500 nm overlay was patterned with cavities where a stacked layer comprising 100 nm Ge and 300 nm of $Ge_{98.5\%}Si_{1.5\%}$ was growth with selective RPCVD, as discussed in section 4.2.2.2. Waveguides passing through cavities were etched together with silicon waveguides used for normalisation purposes. Transmission spectra were measured before and after rapid thermal anneal (RTA) to evaluate the direct bandgap shift by means of a semi-graphical method. In this chapter, the analysis method is first presented, then the fabrication process is briefly discussed; measurements of samples before and after annealing showing a blueshift up to 38 nm are evaluated, followed by material characterisation studies performed to evaluate possible causes of blueshift. The chapter concludes with passive

simulations of the device cross-section before and after annealing to analyse the effect of epitaxial stack variation in direct bandgap shift.

6.1 Direct Bandgap Estimation

The evaluation of the direct bandgap is conducted using the Tauc curve, a method proposed by Tauc, Davis and Mott [264][265] for characterizing amorphous and crystalline photonic materials with absorption spectroscopy; according to this method, it is possible to express the absorption coefficient in terms of the net energy between the photon and the material bandgap energies using the relation:

$$(h\nu\alpha)^{1/n} = A(h\nu - E_G) \qquad \text{Eq. 6-1}$$

where h is the Planck's constant, ν is the frequency, α is the absorption coefficient, E_G is the band gap energy and A is a proportional constant. The exponent n denotes the nature of the transition that can be direct or indirect, allowed or forbidden. In basic transitions, allowed transitions dominate for which n = 1/2 or n = 2 refers to direct and indirect transitions, respectively.

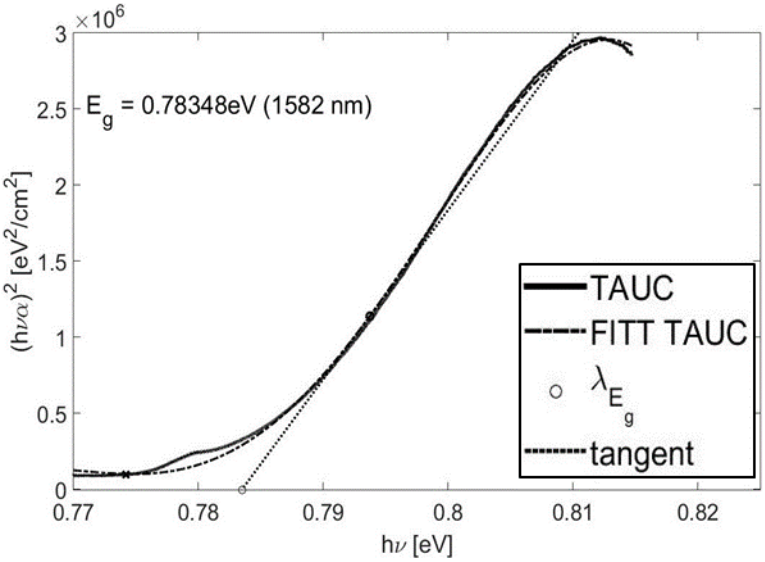

Figure 6-1 Tauc Curve analysis for the passive device realised in a trench containing a $Ge_{98.5\%}Si_{1.5\%}$ alloy. The inflection point is used to trace the tangent by taking the nearest points around it. The E_G is found where the tangent intersects the abscissa.

By measuring the transmission spectrum (Insertion Loss) it is possible to calculate the absorption spectrum and plot $(h\nu\alpha)^{1/n}$ against the photon energy hν, by taking the tangent to its inflection point (tangent passing through two points around the inflection point), the bandgap energy E_G is found where the tangent intersects the horizontal axis. The material

optical characteristics depend on the material energy bandgap and the photon energy. If photon energy is below the material bandgap energy, the material is transparent and photons propagate freely within the material, as the photon energy approaches the bandgap energy, exponential "Urbach Tail" [266], associated with defect states in the material, shows. For photon energy close to the material bandgap, absorption raises linearly with the energy, this linear region is used for the Tauc evaluation. For higher energy, the available transition states saturate and the curve deviates from linearity. The error associate to this method is about 1% respect the absolute value [267]. An example of the Tauc evaluation is shown in the Figure 6-1 for a waveguide with an epitaxial stack comprising 100 nm Ge and 300 nm GeSi alloy with 1.5% of silicon. In this case, a bandgap of 1582 nm is calculated.

6.2 Fabrication Process

Silicon-on-insulator (SOI) wafers with 500 nm Si overlay and BOX of 3 μm have been adopted in this experiment. Recesses with fixed area of 50x50 μm^2 and depth of 400 nm were realised in the Si overlay, then GeSi layer was deposited with a two-step growth technique discussed in section 4.2.2.2, the epilayer stack comprised 300 nm of $Ge_{98.5\%}Si_{1.5\%}$ plus a 100 nm thick Ge layer. The $Ge_{98.5\%}Si_{1.5\%}$ and Si were etched simultaneously to realise butt coupled Si-to-GeSi and GeSi-to-Si rib waveguides; Si waveguides were also realised close to the passive devices for normalization purposes, coupling gratings were etched at the waveguide ends. A thin PECVD oxide layer (~50 nm) was deposited as capping layer.

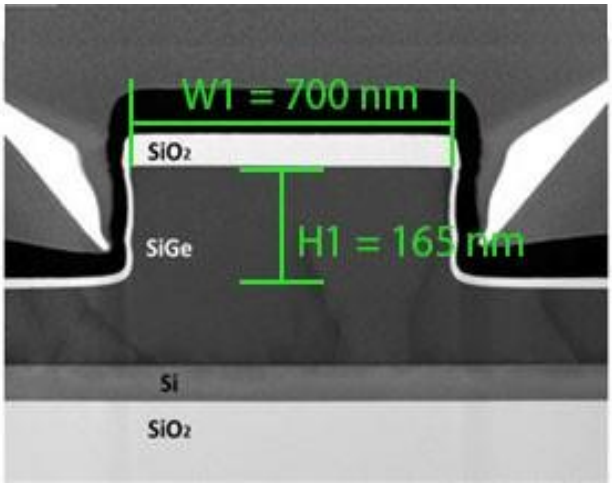

Figure 6-2 Waveguide cross-section TEM image with dimensions.

The waveguide cross-section is depicted in Figure 6-2, the measured waveguide rib is 700 nm wide and 165 nm deep, the material thicknesses in the cavity instead are: 80 nm

for the bottom Si and 420 nm for the Ge/GeSi stack layers, hence close to the nominal values.

6.3 RTA recipe

Before running annealing experiments, it was important to define the correct RTA recipe to control the annealing process. To choose the annealing temperature and time, results from diffusion of Si in germanium in reference [268] were used. In this study, about 600 nm of Ge has been deposited on Si substrate with MBE, during growth Si isotope 28 was added to the epitaxial layer. Diffusion experiments, carried out at different temperatures, allowed to determine experimentally the diffusivity for Si in Ge as a function of temperature. In Table 6-1 values from reference [268] are reported, diffusivity increases with temperature from 3.1E-18 cm^2/s at 600 °C to 2.1E-13 cm^2/s at 900 °C, permitting to greatly varying the diffusion length of Si in Ge with temperature for a given annealing time.

Table 6-1 Experimental results of diffusivity for Si in Ge from reference [268]**.**

Temperature [°C]	Diffusivity [cm^2/s]
600	3.1E-18
650	2.7E-17
750	2.1E-15
800	1.1E-14
900	2.1E-13

The average distance Si atoms can diffuse in Ge called diffusion length D_L, depends on temperature and annealing time and it can be estimated with the relation [269]:

$$D_L = \sqrt{D\tau} \qquad \text{Eq. 6-2}$$

with D diffusivity coefficient calculated in reference [268] and τ the annealing time. In Figure 6-3, D_L from 600 °C to 900 °C (green) have been plotted for τ ranging between 0 s to 2.8 h; in dashed lines the diffusion lengths for 5 min (black), 10 min (magenta) and 20 min (cyan) are highlighted. Below 700 °C the diffusion length is too small to be effective in varying material composition of the 100 nm thick Ge buffer layer, at 650 °C for example (red plot) 5 nm diffusion length requires more than 2 h. Higher temperature, instead, permits faster and longer diffusion of Si in Ge, at τ = 900 °C, for example (gold plot), 10 nm diffusion is achievable within only 10 s. To allow better control of the Si diffusion, it was chosen an annealing temperature of 750 °C, for which the diffusion length ranges between 8 nm and ~20 nm with annealing time from 5 min to 20 min.

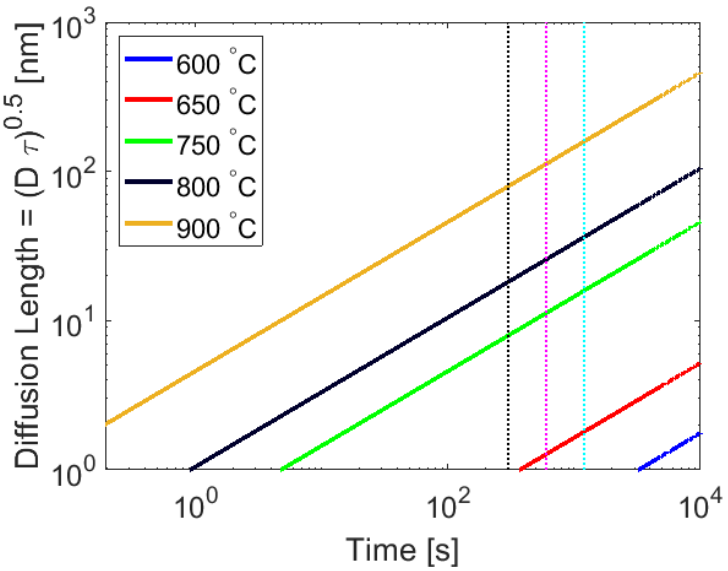

Figure 6-3 Diffusion length for different temperatures, 600 °C (blue), 650 °C (red), 750 °C (green), 800 °C (black), 900 °C (gold). Dashed lines highlighting diffusion lengths at specific RTA times are included for 5 min (black), 10 min (magenta) and 20 min (cyan).

6.4 Measurement analysis

For this experiment the DC setup described in section 4.4.1 was used for measuring devices before and after annealing. A Matlab® script was written to normalize transmission spectra and average measurements from 21 devices. The averaged Insertion Loss spectrum in dB was then used to calculate the absorption spectrum by inverting the IL expression:

$$\alpha = \frac{IL}{4.34\ L}\ [cm^{-1}] \qquad \text{Eq. 6-3}$$

where L is the trench length. From the $(h\nu\alpha)^2$ spectrum, the material direct energy bandgap was evaluated by applying the Tauc method.

Samples were measured before and after rapid thermal annealing in N_2 saturated ambient at 750 °C, the RTA process recipe is depicted in Figure 6-4. The chamber was cooled down with nitrogen and the chamber temperature was set as reference (0 °C), then a ramp up of 10 min was executed to heating up the samples up to 750 °C. Two annealing time were chosen, 5 min (recipe R1, blue curve) and 10 min (recipe R2, red curve). The process ended with a 10 min ramp down to cool down the sample to the reference temperature.

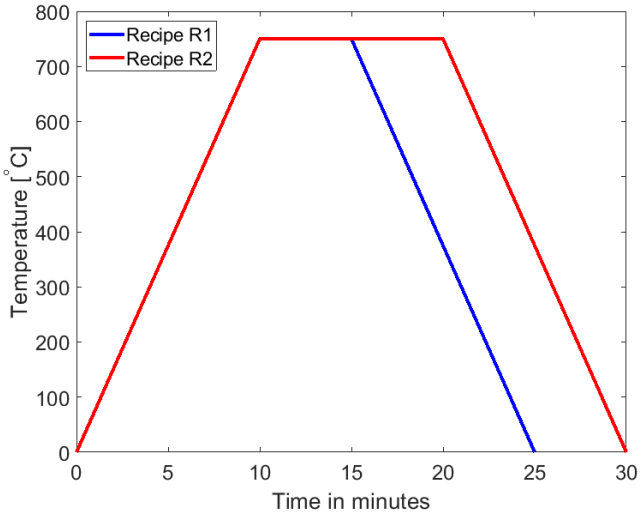

Figure 6-4 RTA recipes R1 and R2 with annealing time of 5 min and 10 min at 750 °C, respectively.

Three samples were annealed, S1 was annealed for 5 min with R1, S2 for 10 min with R2 and S3 was annealed twice by applying the R2 recipe twice, the Tauc method was then applied. As an example, the output analysis for S3 is shown in Figure 6-5, the device direct bandgap is estimated to be 1582 nm before and 1544 nm after RTA.

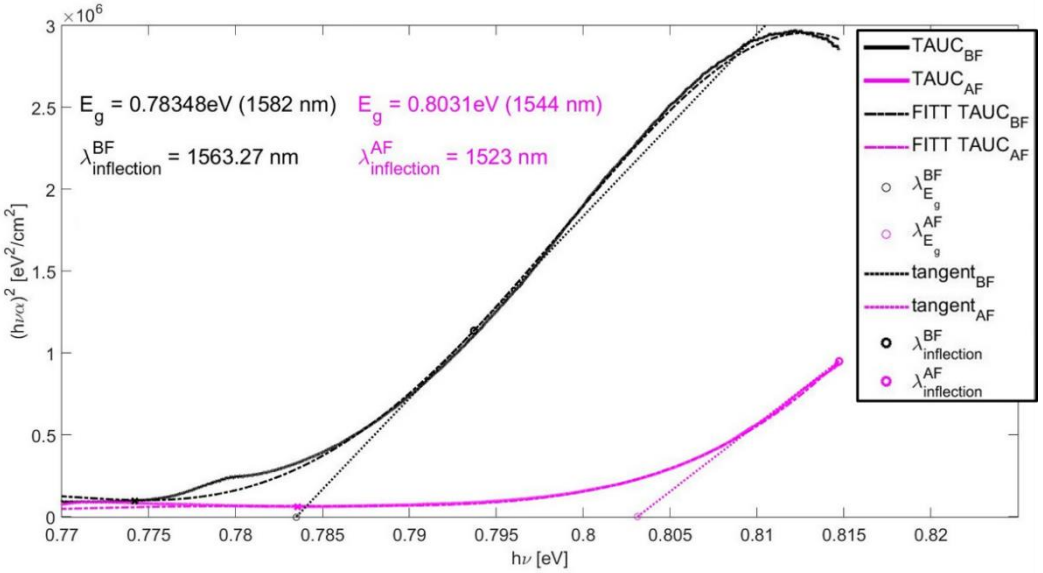

Figure 6-5 Tauc curves of sample S3 before (black) and after (magenta) annealing 20 min. The inflection point is found at 1563 nm and 1523 nm, before and after annealing from which a direct bandgap of 1582 nm before and 1544 nm after annealing is calculated, thus the total blueshift is 38 nm.

In Table 6-2, the sample analysis is summarised with E_G values obtained averaging the cavity loss of different devices, standard deviation for the E_G is calculated to be about 2.5 nm. In S1, bandgap blueshifts from 1582 nm to 1557 nm in 5 min, in S2 instead from 1580 nm to 1542 nm in 10 min and in S3 from 1582 nm to 1544 nm in 20 min. Loss per

unit length also reduces with a maximum reduction in S2 from 0.22 dB/μm to 0.1 dB/μm in 10 min, suggesting a change of material composition in the Ge buffer layer after annealing, the standard deviation is about 0.04 dB/μm.

Table 6-2 Bandgap, bandgap shift and loss as a function of annealing time. Three samples are proposed S1 annealed for 5 min, S2 annealed for 10 min twice and S3 annealed for 20 min.

Time [min]	E_G [nm]			E_G shift [nm]			Loss [dB/μm]		
	S1	S2	S3	S1	S2	S3	S1	S2	S3
0	1582	1580	1582	0	0	0	0.20	0.22	0.20
5	1557	-	-	25	-	-	0.14	-	-
10	-	1542	1552	-	38	30	-	0.10	0.15
20	-	-	1544	-	-	38	-	-	0.16

In Figure 6-6, the bandgap shift (a) and cavity loss per unit length (b) for sample S1, S2 and S3 are shown with average curves in black lines. Shift over shorter wavelength is calculated to be about 25 nm in S1, whereas in S2 and S3 a maximum shift of 38 nm is found. In Figure 6-6a black curve, the average bandgap shift shows almost linear behaviour for the first 10 min with a maximum shift of 34 nm, in the following 10 min annealing the shift saturates to 38 nm. Loss is also affected by annealing, in Figure 6-6b Loss per unit length decreases with annealing, although reduction varies from sample to sample. The highest reduction is found in S2 to be about 55% whereas the lowest reduction, about 12%, is found in S3. In S3 the Loss also increases after the second annealing step, this increment however is only 0.01 dB/μm, therefore it should be intended as no change in the Loss occurred. The mean Loss per unit length curve (Figure 6-6b) is depicted in black, from 0 min to 10 min Loss reduces from 0.207 dB/μm to 0.125 dB/μm almost linearly; above 10 min a constant Loss value is considered to account for the annealing saturation effect. It can be concluded that the loss per unit length has a reduction an average of 40% in 10 min annealing.

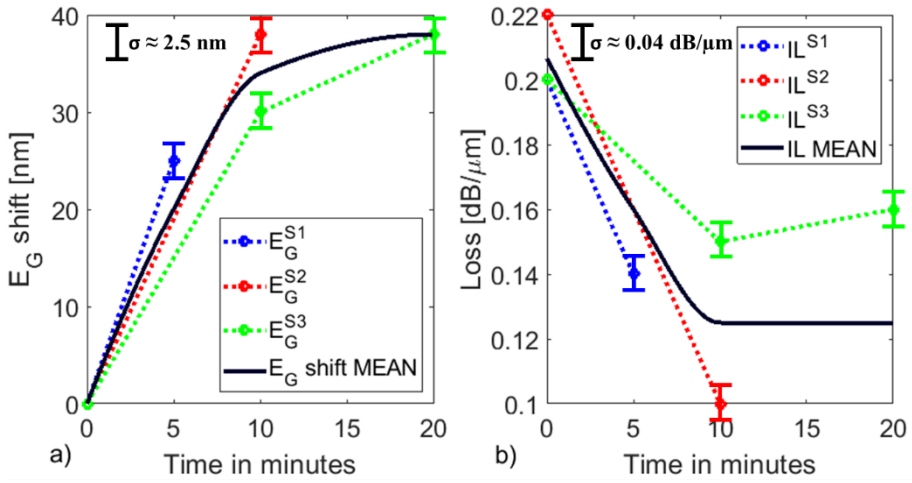

Figure 6-6 Bandgap shift (a) and cavity loss per unit length (b) for sample S1, S2 and S3. Mean curves are added in black lines, the standard deviation (σ) is also shown.

6.5 Characterization

Annealing caused bandgap shift over shorter wavelength up to 38 nm, to investigate the cause of this shift, characterization analysis tackled material composition, strain mapping and dislocation evaluation.

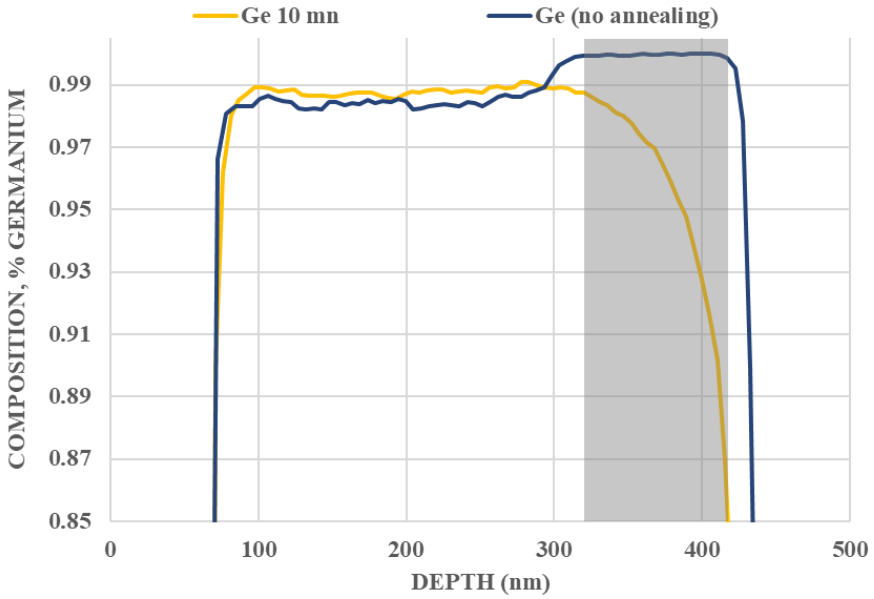

Figure 6-7 SIMS analysis results, before and after annealing. Before annealing a uniform GeSi layer with Si ~1.5% is found for the first 300 nm from the top of the cavity, following 100 nm Ge (blue curve). After 10 min annealing, Si migration varies the GeSi composition (yellow curve) from 100 nm to 300 nm the average Si content is 1.2%, below the Ge buffer layer is replaced by a GeSi alloy with varying Si content between 1.2% to 15% (shaded area).

In Figure 6-7, SIMS study conducted on cavities 50 x 50 μm^2 filled with GeSi and covered by a thin oxide layer (about 70 nm), shows Ge and Si content against depth; two samples were measured, one before and another after annealing (10 min). Before annealing (blue curve) $Ge_{98.5\%}Si_{1.5\%}$ alloy is found between 70 nm and 300 nm, below 100 nm pure Ge layer is measured; further down a sharp transition layer is found with a Si content increasing up to 100% at ~500 nm.

After annealing the material composition changes dramatically, there is a 0.3% increment of Ge from the top cavity to 300 nm deep (yellow curve), the Ge buffer layer between 300 and 400 nm is, instead, replaced by a GeSi alloy whose Ge content reduces with depth from 99% to 85% the average Ge content in this 100 nm layer is about 91.6%. The change in material composition can be attributed to the Si diffusion in Ge as demonstrated in reference [268], silicon diffuses from the top GeSi layer to the Ge buffer layer, additional Si atoms diffuse from the cavity trench to the Ge buffer layer, the average diffusion length therefore is about 100 nm which implies from reference [268] that an annealing temperature of 900 °C, was reached in the cavity. This local temperature

increment is probably due to the lower Ge thermal conductivity of Ge (~0.2 W cm^{-1} $°C^{-1}$) respect Si (~0.5 W cm^{-1} $°C^{-1}$) at 700 °C [270].

Samples were analysed in the nano-characterisation centre of the CEA Leti tech [271] to measure the cross-section strain using the Precession Electron Diffraction Technique [249][250]. Laminar cross-section sheets were cut from two samples one annealed and the other not and analysed with TEM FEI TITAN THEMIS 80-200 kV.

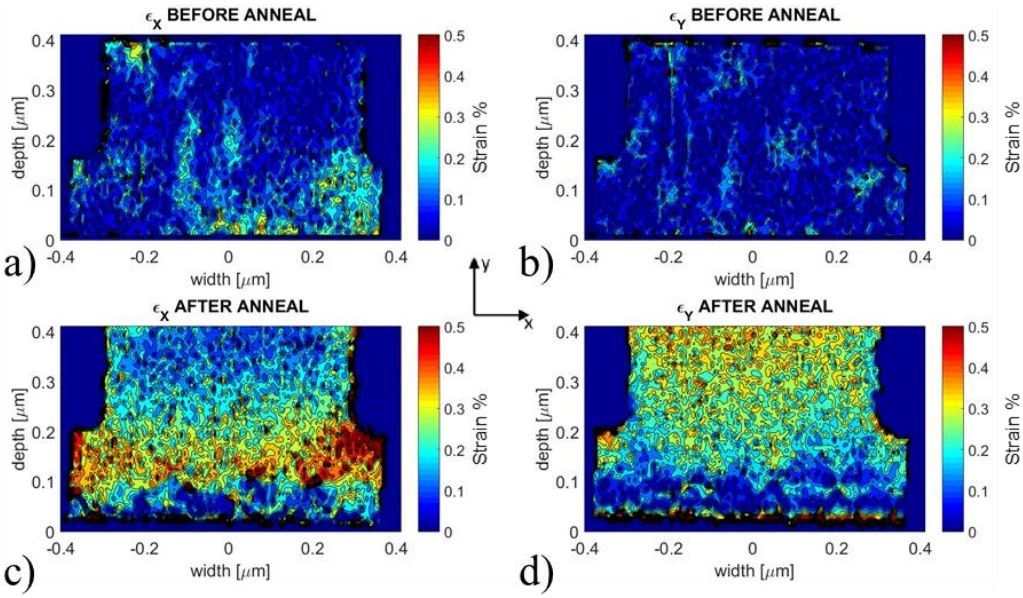

Figure 6-8 Tensile strain on x and y directions before (a, b) and after annealing (c, d). Before annealing, strain is low due to dislocation relaxations; after annealing, a more uniform GeSi stack with strain up to 0.5%, is found.

Analysis results are shown in Figure 6-8, before annealing strain in both x (a) and y (b) directions is low in average. After annealing (Figure 6-8c,d) tensile strain in the waveguide increases up to 0.5%. From the bottom of the cavity, the first 100 nm of material (silicon) is almost strain free both longitudinally (ϵ_x) and transversely (ϵ_y), whereas high longitudinal tensile strain is confined at 100-200 nm of depth (Figure 6-8c), where the Ge buffer layer is found before annealing, longitudinal strain reduces towards the surface. Interestingly, for the transverse strain ϵ_y (Figure 6-8d) the map is reversed, the strain starts to accumulate from 100 nm above the silicon overlay and reaches its maximum value, 0.5%, at the surface.

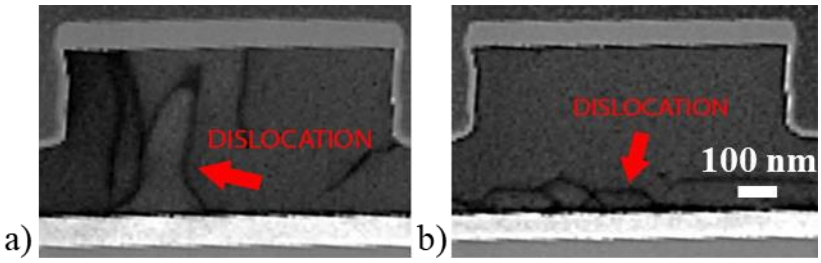

Figure 6-9 Dislocation study in the waveguide before (a) and after annealing (b). Before annealing, dislocations are seen throughout the whole waveguide, whereas after annealing they are confined in the first 100 nm of the stack from the bottom of the trench (white layer).

The strain increment can be explained by analysing the dislocation map measured in CEA Leti labs [271] using the high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) [248]; before annealing (Figure 6-9a), dislocations are found throughout the waveguide allowing strain relaxation [272]. After annealing, dislocations are confined in the first hundred nanometres of material above the Si layer (in Figure 6-9b silicon is the white layer), improving the homogeneity of the material but increasing strain.

Silicon reduction in the rib and strain accumulation after annealing should cause a redshift of the absorption band-edge in contradiction with the measurements presented in Table 6-2. The measured blueshift might be explained by the Si intermixing in the Ge buffer layer after annealing, this would change the device absorption behaviour as the optical mode propagates in the buffer layer. To investigate the device absorption dependency from the underlying Ge layer, two devices were simulated, one containing the Ge/GeSi stack, the other a uniform GeSi stack. A variation of the simulation platform that considers the complex refractive index of Ge and GeSi was used to solve the optical mode distribution in passive structures. The GeSi content before and after annealing was varied accordingly with SIMS results (Figure 6-7), before annealing $Ge_{98.5\%}Si_{1.5\%}$ alloy was used for the 300 nm GeSi epitaxial layer, followed by 100 nm pure Ge; for the device after annealing the top 300 nm layer was replaced with an alloy of $Ge_{98.8\%}Si_{1.2\%}$, whereas the Ge layer was replaced with an GeSi alloy with average composition of $Ge_{91.6\%}Si_{8.4\%}$. The GeSi complex refractive index was interpolated from reference [50] considering the stochiometric content, as shown in Figure 6-10. For the real part (Figure 6-10a) data for pure Ge and $Ge_{91.4\%}Si_{8.6\%}$ alloy were available from reference [50], for the imaginary part (Figure 6-10b) pure Ge and $Ge_{90\%}Si_{10\%}$ alloy (red curves) data were instead available from reference [50]. Using weighted interpolation, the complex refractive spectra for $Ge_{98.5\%}Si_{1.5\%}$ (green curves), $Ge_{98.8\%}Si_{1.2\%}$ (black curves), $Ge_{91.6\%}Si_{8.4\%}$ (pink curves), were calculated.

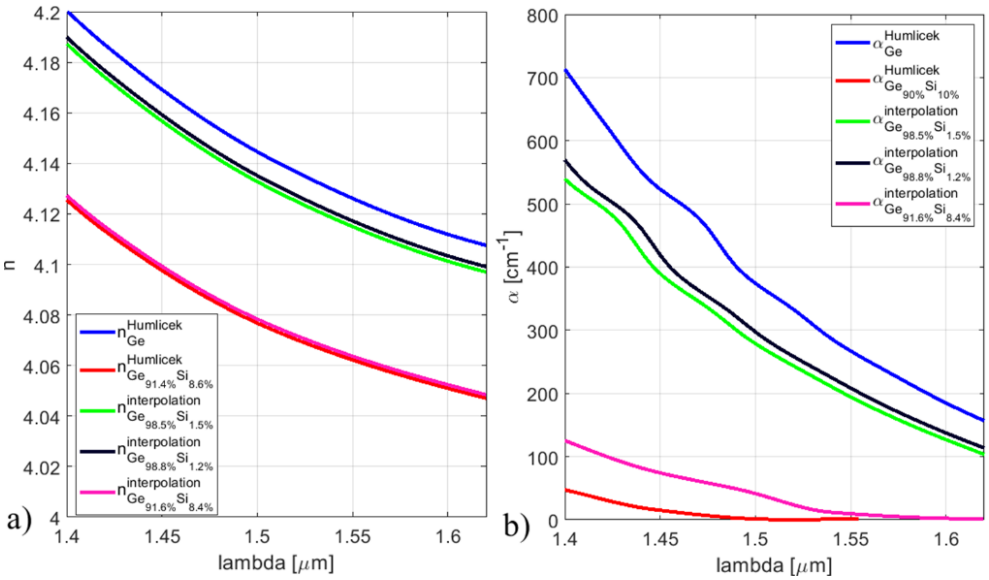

Figure 6-10 Ge and GeSi refractive index (a) and absorption coefficient (b) from Humlicek [50], in blue and red respectively; those curves were interpolated to evaluate the complex refractive index relative to SIMS composition results before and after annealing, $Ge_{98.5\%}Si_{1.5\%}$ (green curves), $Ge_{98.8\%}Si_{1.2\%}$ (black curves), $Ge_{91.6\%}Si_{8.4\%}$ (pink curves).

The modes were solved in both conditions; before annealing the mode partially propagates in the Ge buffer layer (Figure 6-11a) affecting the device absorption spectrum, whereas after annealing the mode propagates in a GeSi alloy with different Si content in depth (Figure 6-11b), varying the absorption characteristics of the device.

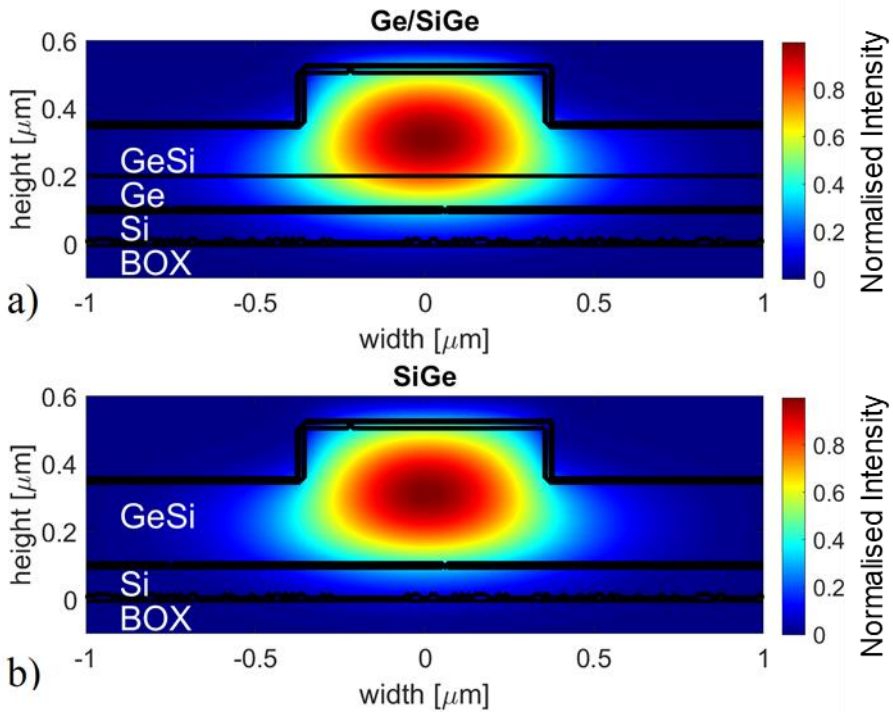

Figure 6-11 TE mode distribution before and after annealing. Before annealing (a), the mode partially propagates in the 100 nm Ge layer, affecting the optical properties of the passive device; after annealing (b), the mode propagates in a uniform GeSi layer with varying Si content.

The Tauc method was applied, in Figure 6-12 the spectra before and after annealing are plotted with relative tangent in the inflection point, permitting to calculate a blueshift of about 0.011 eV (~21 nm) between the two devices. Although the shift is lower than the one measured in the experiment, this simulation offers an indication of the cause of blueshift after annealing.

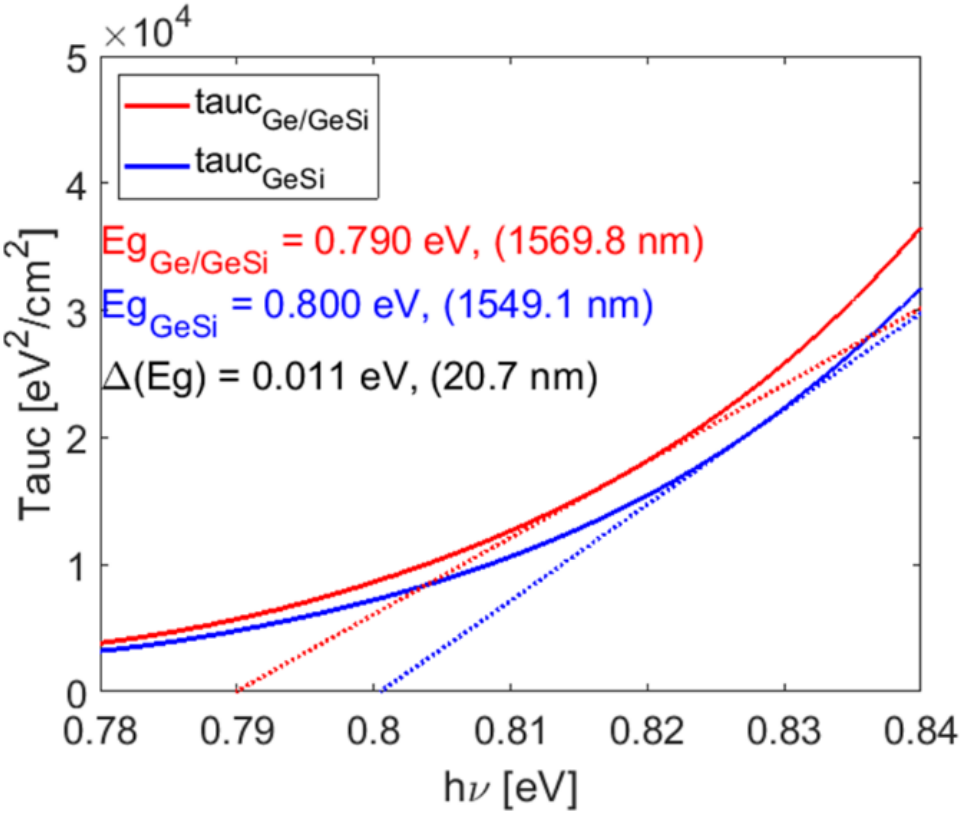

Figure 6-12 Tauc before and after RTA, in red and blue respectively. The effect of removing the Ge buffer layer is to shift towards higher energy the bandgap associated with the direct absorption to about 20 nm, as evaluated with the tangent to the inflection point for both curves.

These simulations are, however, intended more qualitative than quantitative due to use of averaged GeSi stochiometric composition and simple weighted interpolation for calculating the complex refractive index of different alloys; secondary effects related to phonon generation in the Ge buffer layer, not considered here, might account for increased losses and further wavelength shift, in measurement data. Further investigations on material composition and optical behaviour need to be addressed.

6.6 Summary

The band-gap shift of a GeSi layer after annealing was investigated; for this purpose, passive waveguides were realised in sites containing nominal $Ge_{98.5\%}$ $Si_{1.5\%}$ layer growth with selective epitaxy. Transmission measurements were performed before and after annealing, results show a maximum blueshift of 38nm whose causes are then investigated. Composition studies were performed before and after annealing, before annealing the GeSi alloy contained ~1.5% of silicon; after annealing, 100 nm deep silicon migration from the GeSi alloy to the Ge-seed layer was measured, in agreement with results from references [268][269]. It was, also, found that after annealing the material tensile strain increased possibly due to dislocations reduction, as Figure 6-9 suggests. Simulations suggested that the anneal-induced blueshift should be attributed to the change in material composition of the Ge/GeSi stack to a GeSi alloy with varying Si content from 1.2% (100-400 nm) up to 15%. The ability to fine-tune the material bandgap up to 38 nm can be successfully used to fine-tune the operational modulation wavelength of specific wafers whilst retaining the simplicity of only one epitaxial recipe.

Chapter 7

GeSi Photonic Modulator

Scope of this project was to realise and demonstrate a high-speed, compact, CMOS compatible EAM working in the C and L bands; starting from the state-of-the-art and theoretical background, design tools have been developed to define the device aspect-ratio, doping concentration and test process steps. An important milestone has been the realisation of a simulation platform whose results in section 5.3 have been used to define the design reference; in this chapter, the knowledge acquired in the previous studies is summarised in the fabrication of the first prototype in the Nanofabrication Centre of the University Of Southampton. In the first part of the chapter, the fabrication process is fully described with material characterisation studies (AFM, SIMS) performed to assess the alloy roughness, composition, and doping concentrations. Experimental results are, then, examined for different devices starting from dark current and DC performances at chip level to identify trends dependent from variations in the design. The measurement analysis further focuses on devices capable of high-speed operation demonstrating the novelty of the design here proposed.

In the last section of the chapter, a comparison between experimental measurement and simulation results is proposed.

7.1 Device Fabrication Process

Fabrication was mostly done in the Nanofabrication Centre of the University Of Southampton. Involving several steps, including wafer conditioning, lithography, etching, deposition, doping and carried out by Dr. Mehdi Banakar, the only steps outsourced were the epitaxial growth, the dopant implantation, the CMP and SIMS analysis. Details on the tools and recipes adopted have been already discussed in Chapter 4, in this section details on the actual process flow of the first fabrication run is presented; in Figure 7-1, the entire process is depicted.

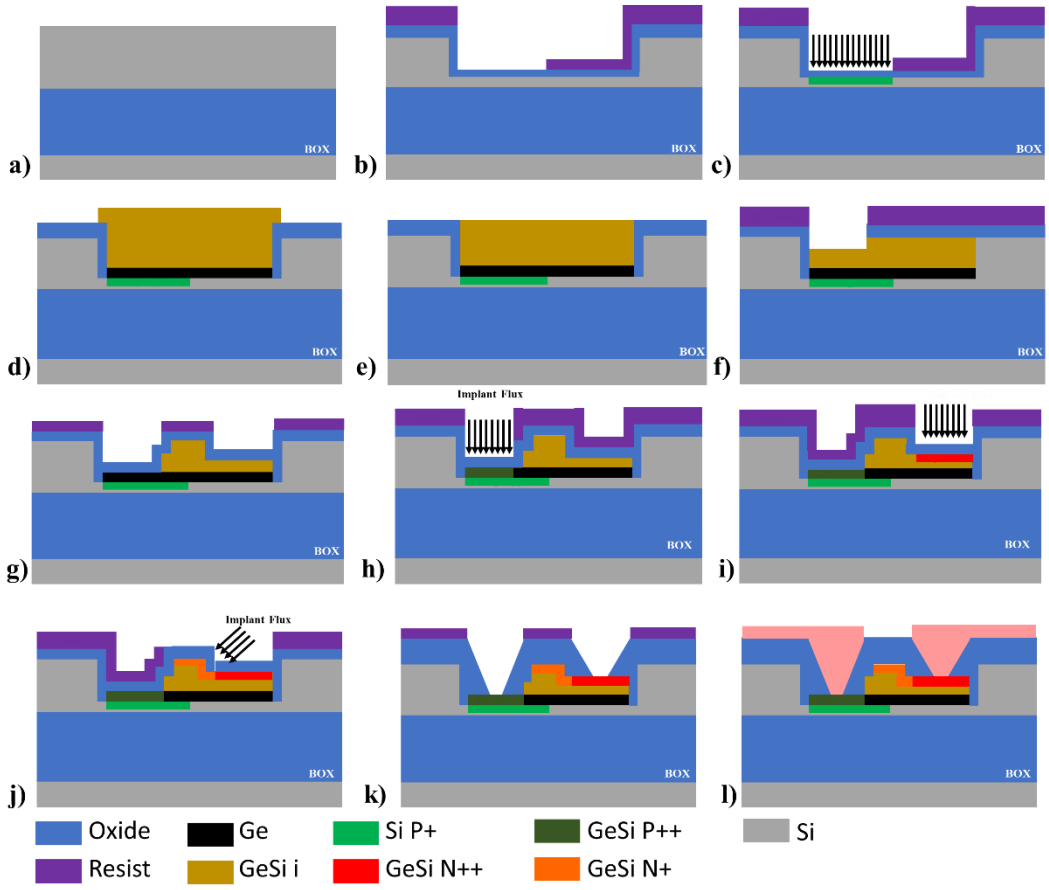

Figure 7-1 Principal steps for the EAM fabrication; from (a) to (l), four etches (b, f, g, k), four implantations (c, h, i, j) and one lift-off (l) are implemented with standard recipes, making this design compatible with current CMOS fabs.

For simplicity the fabrication run is divided in five subprocesses to define the cavity and dope the Si with P+, to etch the waveguide and gratings, to perform the contact doping and the top wrap-around doping implantation and finally to etch VIAs and deposit the metal.

7.1.1 Cavity definition and Si doping

In Figure 7-2 the cavity and Si definition is pictured; about 265 nm oxide was deposited (PECVD) as protective layer (Figure 7-2a), then cavities were defined on the silicon overlay (~800 nm) with a double lithography-etch; with the first e-beam step EAM cavities, alignment marks and ellipsometry window were defined, an ICP-SiO_2 targeting 265 nm, followed.

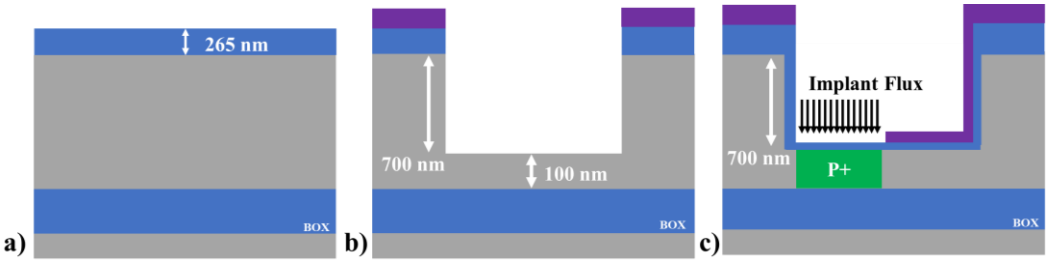

Figure 7-2 cavity definition and Si P+ doping, (a) 265 nm oxide deposition, (b) 700 nm ICP Si etch, (c) Si P+ doping.

The contact lithography, to define the dummy features and relative ellipsometry window, was processed next followed by another 265 nm ICP-SiO_2 to open the oxide. The exposed silicon was then etched to a depth of about 700 nm with ICP-Si, leaving 100 nm thick silicon layer inside the cavity (Figure 7-2b) and prepared for the Si P+ implantation by depositing 20 nm PECVD oxide, followed by e-beam lithography to open the doping wells (almost half of the cavity width) through the ZEP resist. The Si P+ junction well was defined by implanting B with medium/high dose (Figure 7-2c), this step was outsourced to the ion beam centre at the University of Surrey [237]; resist was removed with plasma clean in O_2 and 20 nm oxide was etched (ICP-SiO_2) before the epitaxial growth to remove the oxide in the cavity, while keeping the 265 nm thick oxide layer at the surface of the wafer. The result of this sub-process is depicted in Figure 7-3, the device cavity defined with e-beam is surrounded by conformity cavities realised with photolithography, in orange the region implanted with B (Si P+ doping) using the recipe developed in simulations (Table 5-3); in the picture is also highlighted the test structure for post-fabrication SIMS measurements of the silicon implanted area.

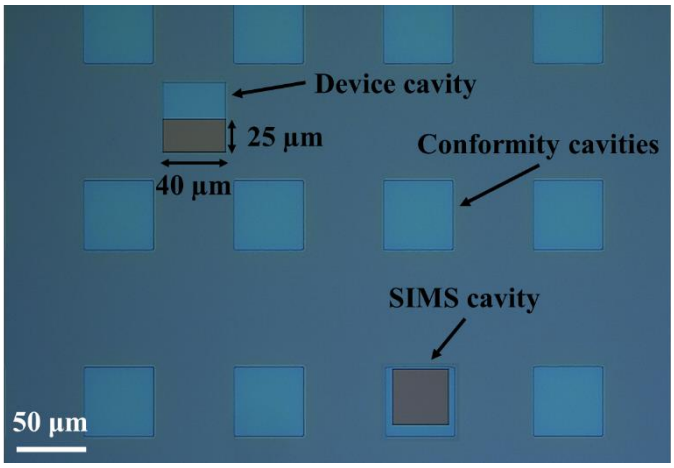

Figure 7-3 Microscope image of the wafer showing the device cavity surrounded by conformity cavities; in orange, the area exposed for boron implant (Si P+).

7.1.2 GeSi growth

The epitaxial stack was deposited with the dual step selective RPCVD deposition discussed in section 4.2.2.2.

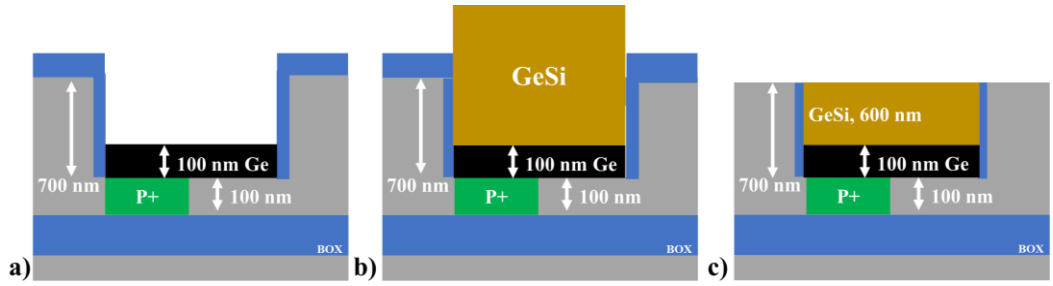

Figure 7-4 GeSi growth, (a) thin oxide etch and Ge deposition, (b) GeSi overgrowth, (c) CMP to planarize the cavities.

Wafers were cleaned at high temperature (above 1000 °C) with H_2 to remove the SiO_2 native oxide, then 100 nm germanium was deposited at 300 °C (Figure 7-4a) followed by GeSi deposition at higher temperature (600 °C) with nominal Si content of 1.5% (Figure 7-4b). Precleaning at high temperature may damage the wafer strongly affecting the epitaxial growth [200] and cause Si reflow [201][202]. In Figure 7-5a-c, pictures from the wafer after deposition showing damage, which can be attributed to precleaning process, are visible. In Figure 7-5d, a FIB cross-section highlights the slanted sidewall at the cavity edges that might be caused by the oxide removal with H_2 leading to Si reflow at the sidewall with diffusion of Si towards the bottom surface [201][202]. The slanted sidewalls effect on the power transmitted through the butt-coupled Si-to-GeSi waveguide simulated in section 5.4.3 accounting for only a reduction of power of about 1.7%, is therefore marginal.

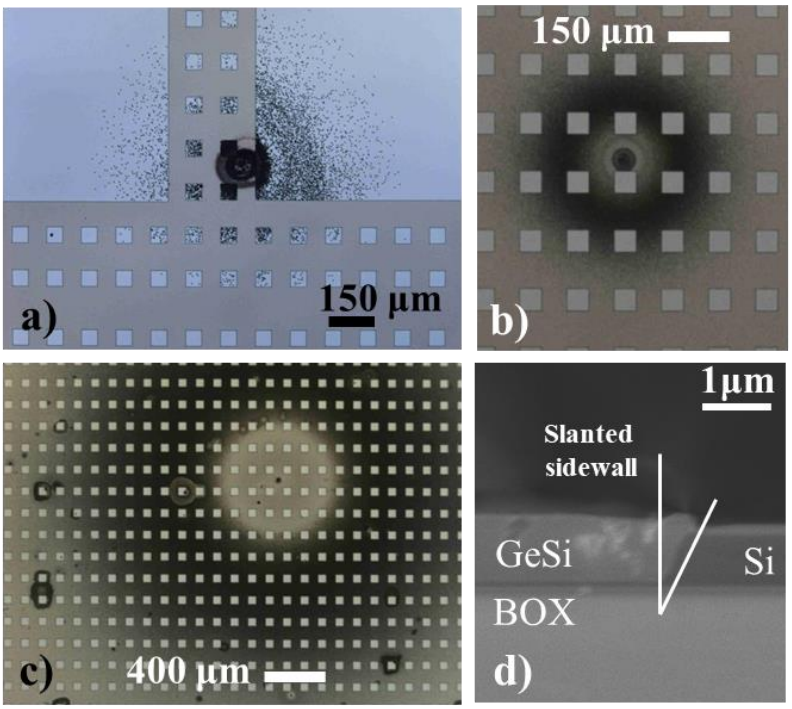

Figure 7-5 (a-c) Pits were found on the wafer during inspection after GeSi growth. (d) FIB cross-section of the lateral view of the cavity realised in the Si overlay and filled with GeSi, highlighted the slanted sidewall.

After selective epitaxy, wafers were inspected and roughness was characterised with AFM. In Figure 7-6, AFM results confirm a successful GeSi deposition with RMS surface roughness ranging between 1.14 nm (Figure 7-6a) and 1.9 nm (Figure 7-6b), thus in line with reported roughness for thick Ge films [273] or GeSi alloy, in reference [66] however it has been reported an astonishing RMS roughness for a GeSi alloy with 0.5% of Si, ranging between 0.2 nm and 0.4 nm thanks to the buffer layer annealing technique adopted in the growth.

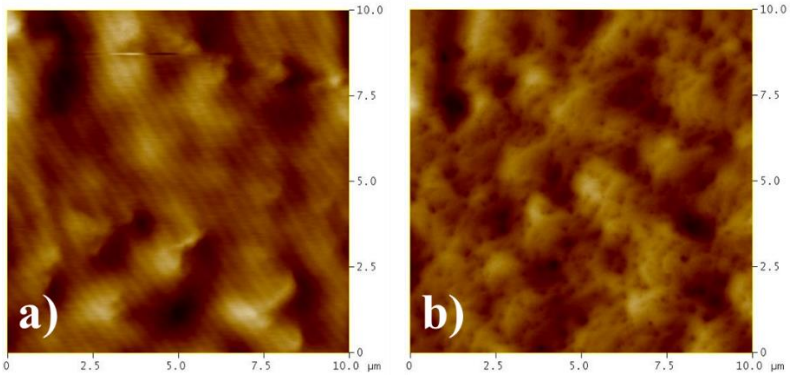

Figure 7-6 AFM roughness measurement, (a) RMS 1.14 nm, (b) 1.9 nm.

Light CMP using the oxide as stopping layer was performed at the VTT Technical Research Centre of Finland [215] to planarize the cavities and remove all GeSi in excess, the procedure was discussed in section 4.2.2.3. Wafer thickness was measured before CMP

on selected regions, it was found a protruding height (GeSi overgrowth) of 144 nm on average. CMP was executed three times with an average GeSi and SiO_2 etch rate of 59.55 nm/min and 24 nm/min respectively. For each step, profilometry analysis, whose results were included in the VTT report, was performed: after the first CMP, the protruding height was reduced by 120 nm, the oxide thickness was measured to be about 161 nm, dishing of about 64 nm was also found. After two other CMPs the protruding features were completely removed with a total over-etch of about 30 nm. The final oxide thickness was found to be about 64 nm, dishing was reduced to 34 nm. After CMP, the remaining oxide was etched in HF 20:1 (Figure 7-4c).

7.1.3 Waveguide and Grating Definition

Waveguides were defined with a self-aligned double etch exposure, 50 nm PECVD oxide was deposited. An e-beam lithography defined the area to be etched first (the left side of the rib), then ICP-SiO_2 was used to open the 50 nm PECVD oxide, followed by another ICP-Si to etch 200 nm of GeSi (Figure 7-7a) resist was ashed, oxide was then removed with a bath in HF 20:1 (20 H_2O, 1 HF). 20 nm of PECVD oxide was deposited, another e-beam lithography defined the waveguide rib and gratings, followed by ICP-SiO_2 to open the 20 nm oxide and another ICP-Si step targeting 400 nm etch depth to form the waveguide rib (Figure 7-7b).

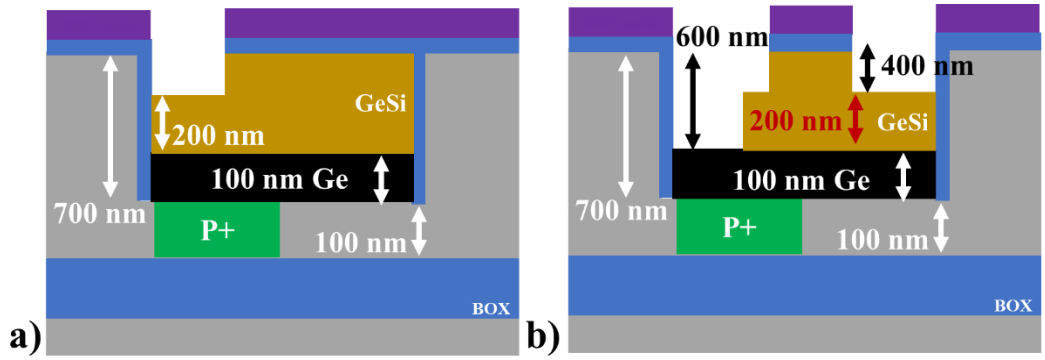

Figure 7-7 Waveguide and grating definition, (a) ICP GeSi etch 200 nm on rib left side, (b) ICP etch 400 nm to define rib and gratings.

As a result, on the left side of the rib the GeSi layer was completely removed, exposing the Ge buffer layer; on the right of the rib, a 300 nm thick layer containing the 200 nm GeSi followed by 100 nm of Ge, was obtained. During the second lithography-etch subprocess, silicon waveguides and CGs were also defined.

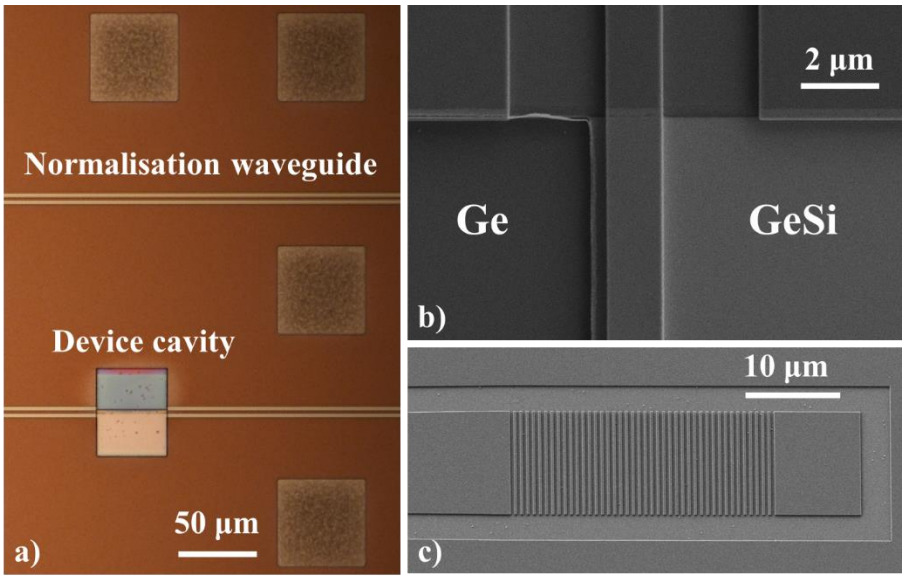

Figure 7-8 (a) Top view of the cavity after waveguide etch, on top the normalisation waveguide and conformity structures, are visible. (b) SEM image of the cavity, showing the trench etch on the left and the rib. (c) SEM picture of the grating coupler.

In Figure 7-8a a microscope image of wafer shows the cavity with the waveguide passing through the device cavity, the silicon normalisation waveguide about 150 µm above, is seen. In Figure 7-8b, the SEM image from the top cavity depicts the GeSi rib with the deep etch (~600 nm) on left and shallow etch (~400 nm) on the right. In Figure 7-8c another SEM picture shows the grating coupler realised on both ends of the waveguide. Thanks to the etch process developed in this project, a single etch is necessary to define the waveguide rib inside the cavity and outside on the Si overlay, giving a huge advantage in terms of alignment and interface loss; the etch rate of Ge, however, is faster than that of Si [189][190], using the ICP-Si recipe a GeSi over-etch from 16% to 30%, was measured with FIB cross-sections. The loss contribution from the over-etched GeSi waveguide, was estimated in the worst case (30% over-etch) through simulations (section 5.4.2) to be 0.31 dB per interface.

7.1.4 Ge and GeSi doping

Three dopant implantations were outsourced to the ion beam centre at the University of Surrey [237] for forming the P++ contact doping (Figure 7-9a), the N++ contact doping (Figure 7-9b) and the N+ junction doping (Figure 7-9c); 20 nm of PECVD oxide was deposited followed by ZEP deposition (450 nm) and e-beam lithography to define the doping wells through the resist while protecting the surrounding area. The implantation recipes used are summarised in Table 5-2 and Table 5-3. After the last implantation, resist

was removed with O_2 plasma clean, PECVD oxide was etched in a HF bath 20:1 and 20 nm PECVD oxide was deposited.

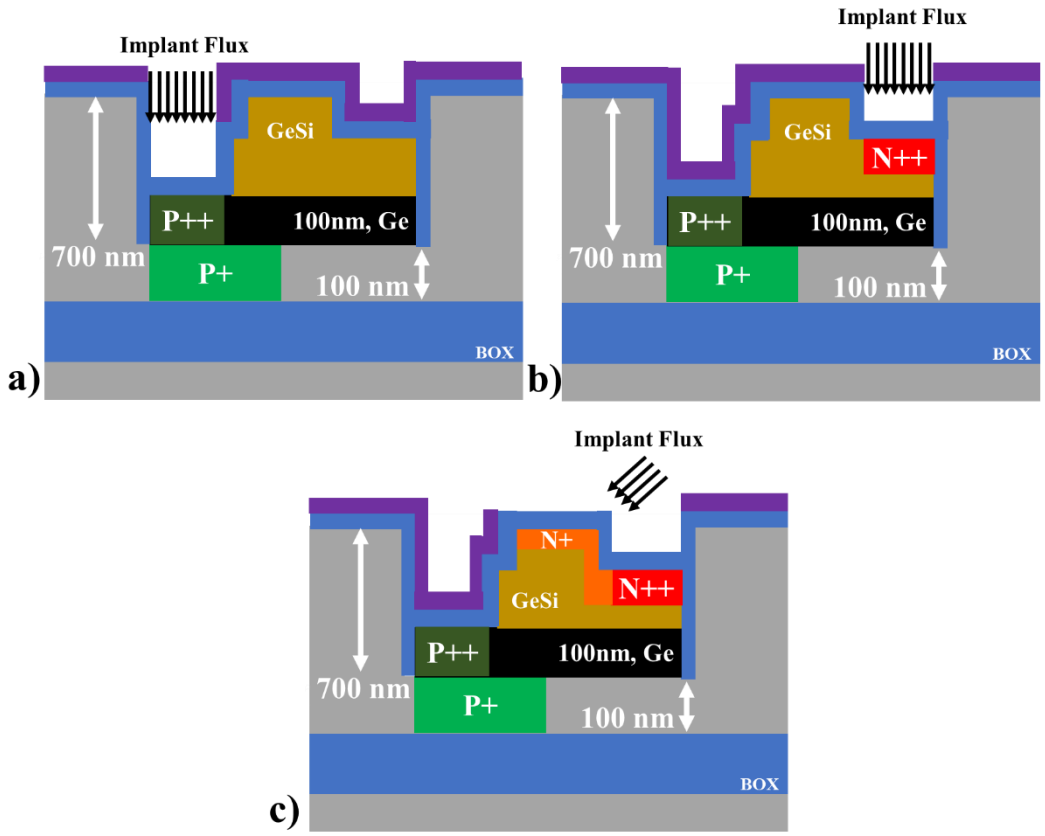

Figure 7-9 Ge and GeSi doping, (a) Ge P++ implant, (b) GeSi N++ implant, (c) GeSi N+ angled implant.

7.1.5 VIAs etch and Metal deposition

A 475 nm thick cladding PECVD oxide was deposited (Figure 7-11a) to separate the metal from the propagation area, VIAs opening were defined with e-beam using the thick ZEP deposition recipe then 450 nm of PECVD oxide was etched with ICP SiO_2 slanted sidewall recipe (ICPS- SiO_2) to avoid any cracks in the metal at the edge of the SiO_2 VIA. The remaining ~50 nm oxide covering the doping contacts was etched in HF 20:1 (Figure 7-11b). Following the VIAs etch the activation and passivation annealing were performed, RTA recipes are shown in Figure 7-10, using standard recipes already available within the Silicon Photonics Group.

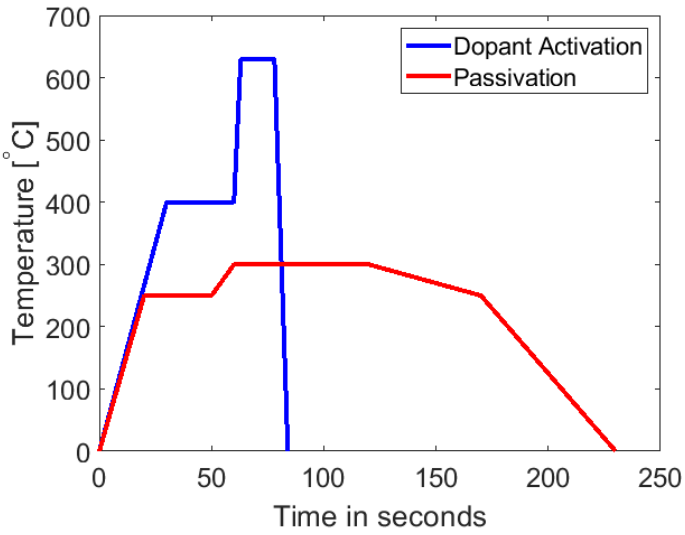

Figure 7-10 RTA recipes for the dopant activation (blue) and the passivation (red).

The dopant activation annealing was conducted as follow (Figure 7-10, blue curve), the RTA chamber was cooled down with nitrogen and the temperature set as reference (0 °C) in 30 s temperature was raised from ambient to 400 °C and kept for 3 s, then in 3 s temperature was raised to 630 °C [274] and kept for 15 s, the annealing was concluded by lowering the temperature from 630 °C to ambient in 6 s. For the passivation layer, RTA in oxygen saturated ambient (Figure 7-10, red curve) was used to form germanium oxide (GeO_2). Due to its solubility in water and being thermally unstable for >450 °C, GeO_2 is usually not desirable, but high quality GeO_2 passivation layers have been demonstrated [275][276]. Temperature was raised to 250 °C in 20 s and kept for 30 s, then it was raised to 300 °C in 10 and kept for 60 s, temperature was so lowered to 250 °C in 50 s and kept for 10 s, finally temperature was brought back to 0 °C in 60 s.

Metal layer lift-off technique was used to define the features (Figure 7-11b), and the metal stack comprising Ni, Ti and Al was evaporated and resist removed (Figure 7-11c); as already mentioned in section 4.2.2.4, 30 nm of nickel was deposited to react with doped germanium for forming germanide (GeNi) and thus reducing contact resistance [216][217], then 10 nm of titanium to stop metal diffusion on the epilayer by forming a TiN alloy [218], a 500 nm thick aluminium layer was deposited to reach the surface and a final 60 nm of titanium as a top protective layer.

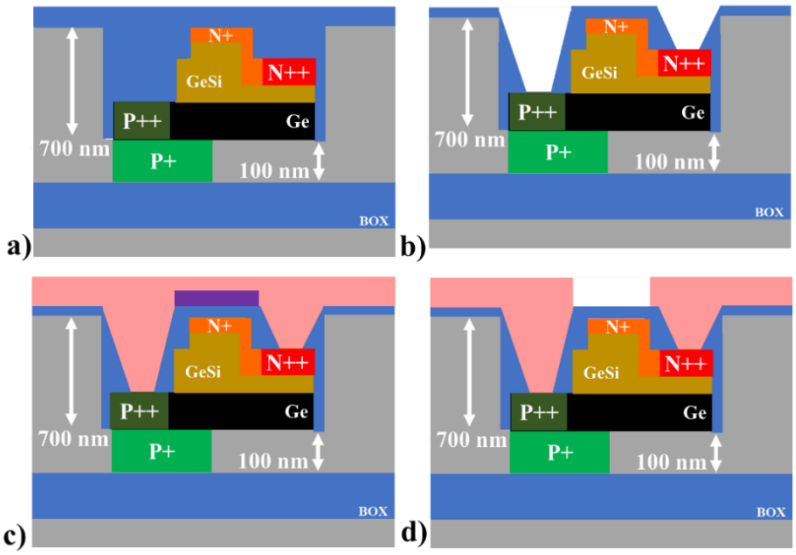

Figure 7-11 (a) Cladding PECVD oxide deposition (475 nm), (b) VIAs definition, (c) metal lift-off, (d) resist removal end of process.

7.1.6 Device Top-View and Cross-Section

In Figure 7-12a, the top view of the device is shown, in light grey the metal pad of the N++ and P++ contact doping; in Figure 7-12b it is reported the FIB-SEM picture of the device cross-section realised providing a wider rib (aspect ratio of W/H = 2.14) than other works [30][31][148][149] for better confining the TE mode and the self-aligned trench etch on the left for realising the P++ contact doping in the 100 nm Ge buffer layer.

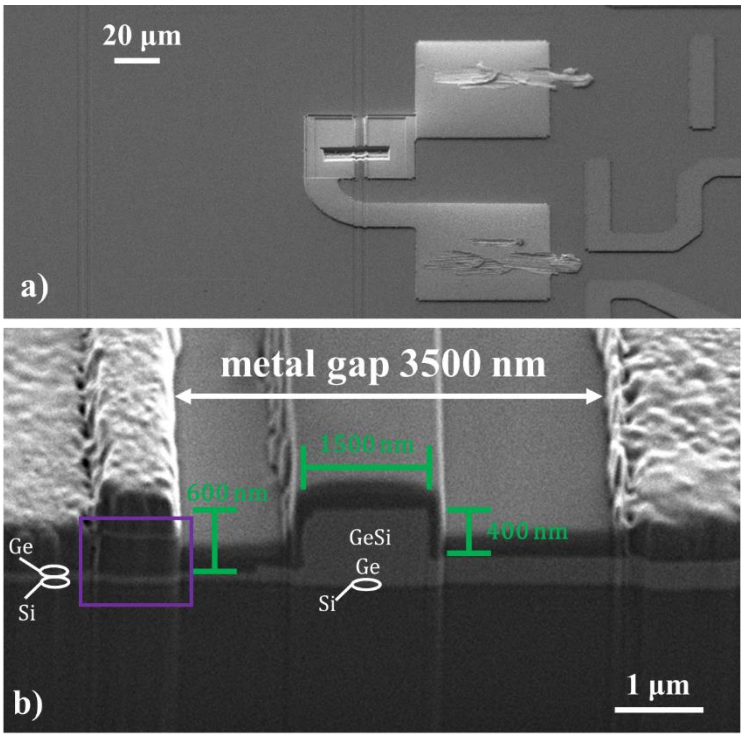

Figure 7-12 (a) SEM picture of the realised device, in the middle the FIB cut is visible. (b) Cross-section of the realised device. In the inset the close-up of the VIA slanted sidewall.

The rib is about 1.5 μm wide and 0.4 μm tall, the deep etch on the left slab is ~0.6 μm, in Figure 7-12b the interface between the Si cavity and the Ge epitaxial layer is not clearly visible due to the low contrast between silicon and germanium.

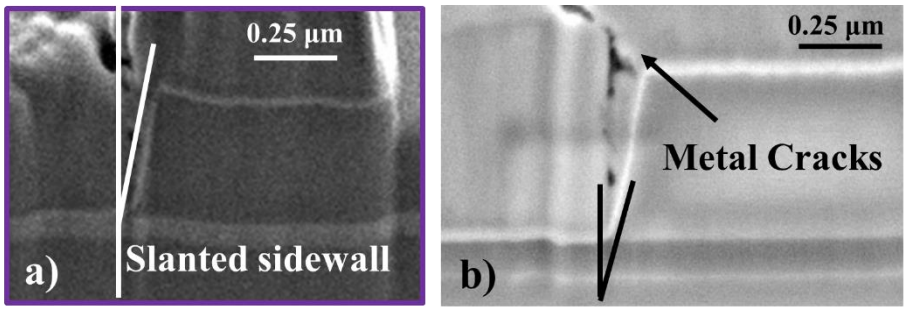

Figure 7-13 VIAS slanted sidewall, (a) inset from Figure 7-12b, (b) small cracks in the metal are visible.

In Figure 7-13a close-up of the vias sidewall from the inset of Figure 7-12b highlights the slanted sidewall achieved with the ICPS-SIO_2 recipes. In Figure 7-13b, another VIA sidewall shows small cracks in the metal that did not affect the device operability.

7.2 SIMS after Fabrication

Fabrication was completed on wafer W4, SIMS study was commissioned to check material and doping conditions on the wafer after fabrication; other wafers were annealed to blend the Ge buffer layer as already discussed in Chapter 6, SIMS measurements on material composition are shown afterwards.

SIMS results are shown in Figure 7-14 for wafer W4 including simulation results from section 5.3.2. Material composition and doping concentration in W4 have good distribution over depth; Si content in GeSi layer varies between 1.5% and 1.2% with an average of 1.3% from the surface to 500 nm of depth, below the Ge buffer layer extends for further 100 nm. A final sharp reduction of Ge concertation is found at about 600 nm replaced by Si whose concentration rises up to 100% at about 800 nm.

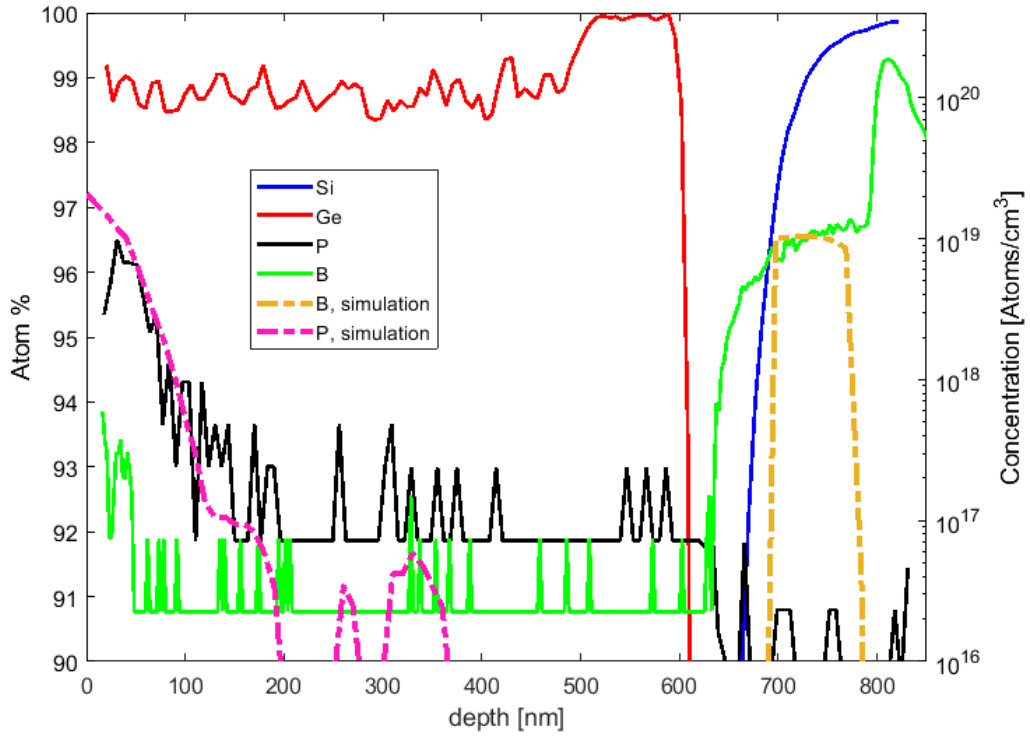

Figure 7-14 SIMS analysis of samples from wafer W4, after doping activation, in red and blue Ge and Si content, respectively; in black and green, phosphorus and boron concentration. Simulations from section 5.3.2 are shown in dashed line, phosphorus in magenta, boron in gold.

The average phosphorus concentration in the first 100 nm of material is about 5E18 cm^{-3} although the concentration peak (1E19 cm^{-3}) is found at 20 nm of depth followed by a fast concentration reduction, due to the high diffusivity of this dopant in Ge [277] that promotes strong migration of dopant in the underlying material. Boron doping in silicon (P+) is, instead, more uniform for the whole thickness (100 nm) with concentration close to 1E19 cm^{-3}. Deeper in the layer (~800 nm of depth), a B concentration spike higher than 1E20 cm^{-3} is visible. Boron in fact is highly diffusive in silicon [278], so that during the high temperature (>1000 °C) cleaning process before Ge/GeSi growth (RPCVD technique details in section 4.2.2.2), boron ions from the Si P+ doping well diffused deeper in the layer accumulating at the Si-oxide interface. Compared to simulations, both doping species are close to design, phosphorus in GeSi (magenta dashed line) has a higher peak than that measured with SIMS (black full line) but the overall distribution matches. Boron simulation in silicon (gold dashed line) is fully in agreement with experimental result (green full line) apart from the high peak at the silicon-oxide interface.

7.2.1 RTA test on the 800 nm Platform

RTA test on a process development wafer (W8) was conducted after waveguide definition in the attempt of reducing the Ge buffer layer contribution to the IL with

annealing and shifting the wavelength operation point towards shorter wavelengths (blueshift), similarly to the experiment presented in Chapter 6. For the RTA a ramp up of 10 min brought the temperature from ambient to 750 °C, wafers were then annealed for 5 min at 750 °C, the process ended with a final ramp down of 10 min. Composition SIMS results are show in Figure 7-15.

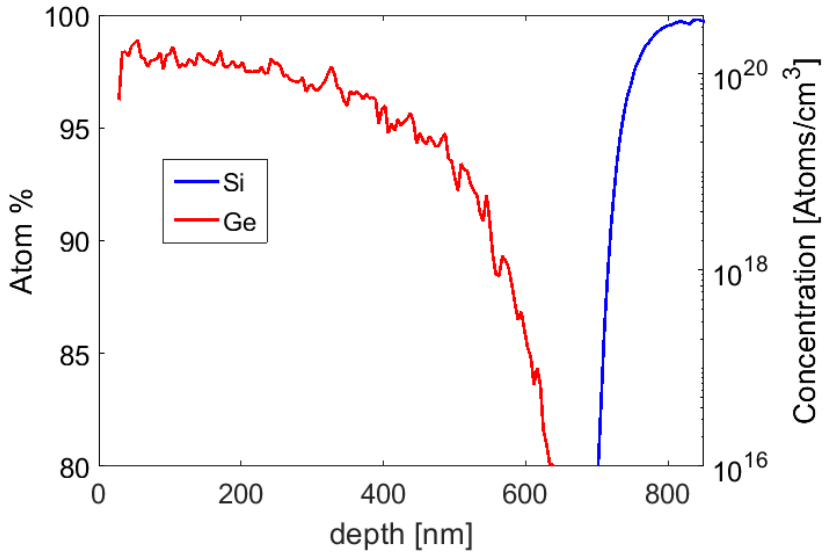

Figure 7-15 SIMS analysis of samples from the annealed wafer (W8), in red and blue Ge and Si content, respectively.

The RTA step was executed for too long and/or at too high temperature, the GeSi alloy has varying composition over depth with silicon concentration up to 13%, extending the transition layer to almost the whole cavity thickness. Due to the high Si concentration, the GeSi alloy behaving as silicon-like, for which indirect bandgap transitions at the communication wavelength have a strong impact on optoelectronic properties [102], would not enable any FKE on devices realised in this wafer.

7.3 Electro-optic Measurements

Fabrication process was successfully completed on W4, which did not go through the RTA step presented in section 7.2.1. In this section, characterisation is discussed for devices from wafer W4 capable of DC and high-speed operation, chip results are presented first, then performances of selected device are further inspected. IV curves are first shown, DC efficiency and high-speed performances, afterwards. Finally, RF electric characterisation is derived for the device that delivered best performances.

7.3.1 IV characterisation

Electric response to a slowly varying bias was needed to evaluate the dark current, originating from surface currents and/or bulk currents dark current reduces performances and reliability of the modulator by increasing the static power consumption, IV characteristics were measured on device from W4, results are shown Table 7-1.

Table 7-1 Dark current at -2 V for devices of W4, device number and contact coping distance combination are also reported.

Device no.	P++ - N++ [µm]	W4 I@-2 V [µA]	Current Density [A/cm^2]
1	1 - 1	14.81	24.68
2	1 - 0.75	10.57	17.62
3	1 - 0.5	5.73	9.55
4	1 - 0.25	14.52	24.20
5	1 - 0	8.41	14.02
6	0.75 - 1	6.45	10.75
7	0.75 - 0.75	7.47	12.45
8	0.75 - 0.5	6.86	11.43
9	0.75 - 0.25	-	-
10	0.75 - 0	3.35	5.58
11	0.5 - 1	12.86	21.43
12	0.5 - 0.75	9.17	15.28
13	0.5 - 0.5	15.51	25.85
14	0.5 - 0.25	15.69	26.15
15	0.5 - 0	10.04	16.73
16	0.25 - 1	38.71	64.52
17	0.25 - 0.75	29.69	49.48
18	0.25 - 0.5	2.06	3.43
19	0.25 - 0.25	-	-
20	0 - 1	89.85	149.75
21	0 - 0.75	274.51	457.52

Dark current ranging between µA and hundreds of µA was measured, by calculating the dark current density, result from device W4-18 can be compared with references [149], [30] and [31] (Table 7-2).

Table 7-2 Current density from different works.

Ref.	I@-2V [µA]	Area [µm^2]	Current Density [A/cm^2]
Liu et al. [149]	0.065	30	0.22
Feng et al. [30]	15.4	40	38.50
Srinivasan et al. [31]	0.047	30	0.16
This work W4-18	2.06	60	3.43

Compared to other works W4-18 shows higher current density than references [149][31] but lower than reference [30], as already discussed in section 3.1.3, the high current density might be explained by a passivation step not fully successful that enhanced the surface current and from high density threading dislocations present in the Ge buffer layer, that increased the bulk current [61][129].

7.3.2 DC Characterisation

Transmission spectra of devices were measured while applying a dc bias ranging from 0 V to -4 V, raw data were normalised with the silicon waveguides, and the cavity loss was found; finally, the electro-optic efficiencies (ER and FOM) were calculated. The measurement results are reported in Figure 7-17 for ER analysis and Figure 7-18 for FOM analysis. Linear interpolation is added to study trends against the contact doping combination. Figure 7-16 shows, similarly to Figure 5-40, the alignment between the contact doping edge (right side for the Ge P++ and left side for the GeSi N++) to the rib edges to facilitate comparison between devices and analyse trends.

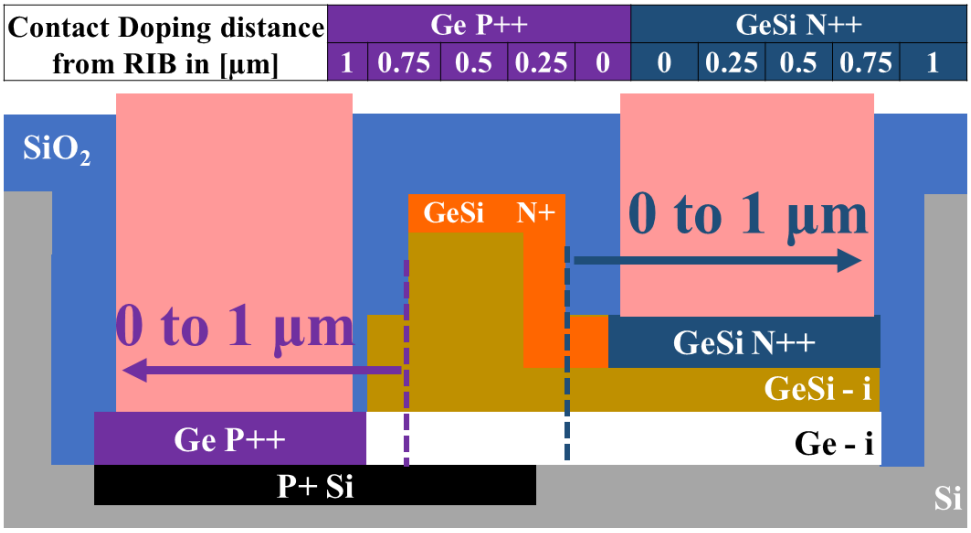

Figure 7-16 Device combinations, the Ge P++ and GeSi N++ well are shifted respect the left and right rib edges between 0 µm and 1 µm in the direction pointed by the arrows, the table on top of the picture summarises all combinations

In Figure 7-17, analysis of devices from W4 is reported with ER principal peaks found around 1.54 µm. Devices are divided in groups (subplot) referring to the contact doping position N++, as highlighted by the plot titles; in each plot, devices differ for the P++ contact doping distance from the rib, written as label on the abscissa, all distances are in µm. It was found a trend proportional to the P++ position; in Figure 7-17a-c (for N++ position from 1 µm to 0.5 µm) for biases from -2 V to -4 V, ER peak increases with increasing P++ distance from the rib edge. The minimum increment is 0.3 dB (Figure 7-17b

black curve ER for -3 V) and the maximum is 4.5 dB (Figure 7-17c magenta curve ER for -4 V). The trend is, instead, almost flat for the spectra at -1 V (red dots and trendline), a small reduction of ER is seen; it should be noted the ER at -1 V is quite low (~3 dB) so that noise could have compromised results.

When the N++ is at distances of 0.25 μm and 0 μm from the right edge of the rib (Figure 7-17d-e), ER shows opposite behaviour at all reverse biases, ER decreases with increasing P++ distance from the rib edge suggesting that the FKE benefits more from the reduced distance of both N++ and P++ than the loss due to the built-in electric field. This assumption is confirmed by the FOM, while in Figure 7-18a-c (N++ between 1 μm and 0.5 μm from the rib edge), the spectral efficiency improves for P++ doping far from the rib, thanks to a reduced IL (lower built-in electric field) in agreement with simulations (Table 5-4 in section 5.3.3); in Figure 7-18d-e for contact doping close to the rib, the FKE overcomes the loss penalty associated to the increased built-in electric field so that the FOM is higher, and vice versa.

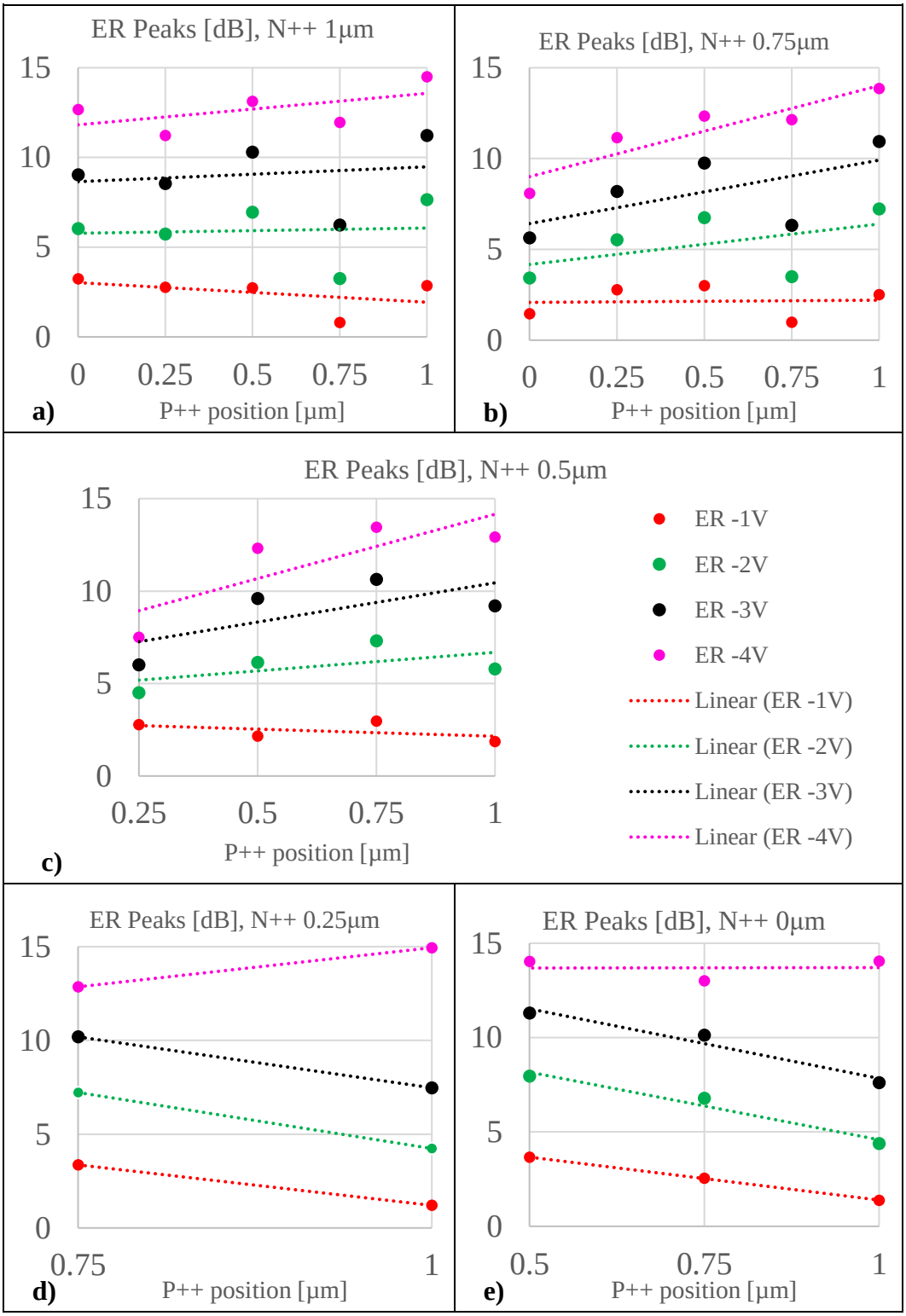

Figure 7-17 ER for devices in W4 divided in N++ positions. In each plot devices differ for the P++ position, written on the abscissa label. Distances in µm, in red ER -1 V, in green ER -2 V, in black ER -3 V and in magenta ER -4 V. Legend shown in c).

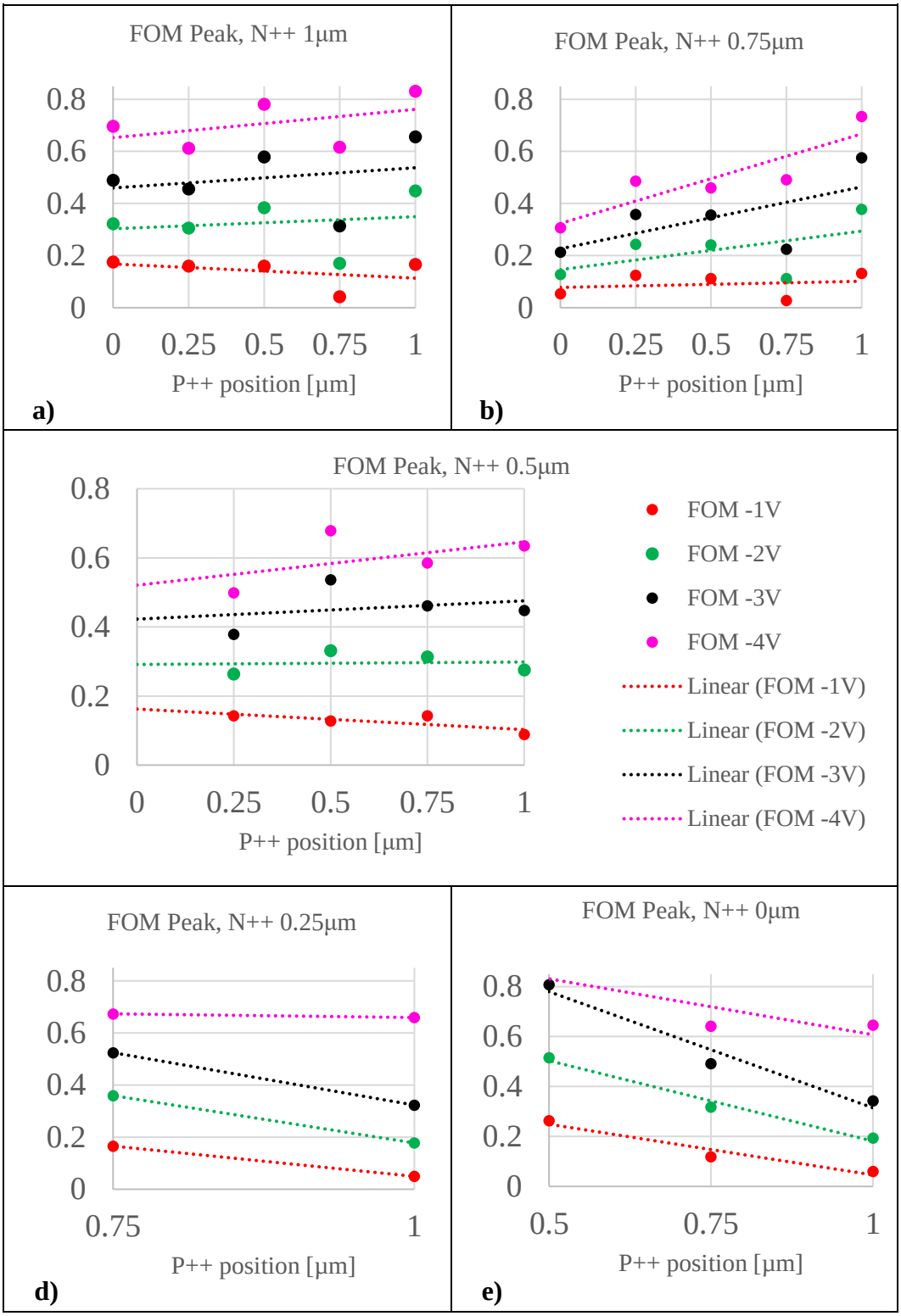

Figure 7-18 FOM for devices in W4 divided in N++ positions. In each plot devices differ for the P++ position, written on the abscissa label. Distances in µm, in red FOM -1 V, in green FOM -2 V, in black FOM -3 V and in magenta FOM -4 V. Legend shown in c).

Spectral efficiencies from device W4-18 in Figure 7-19 confirm the good quality of the epitaxial layer and junction doping.

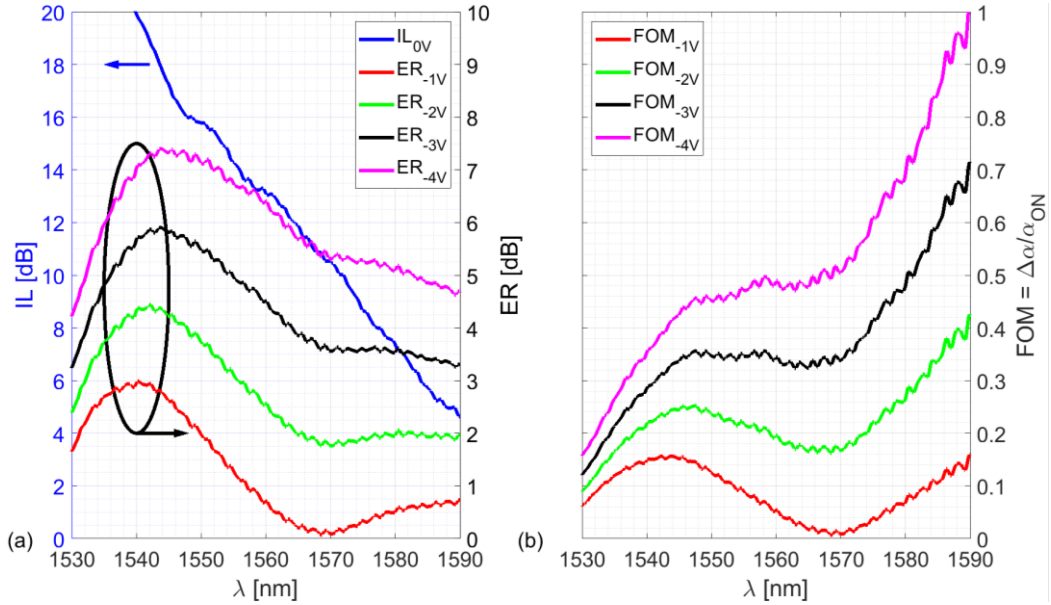

Figure 7-19 W4-18, a) ER and IL of the device achieving the highest modulation speed; b) the resulting FOM at different reverse biases.

ER spectra in Figure 7-19a show two peaks. The first peak around 1.54-1.55 μm has an incremental rate of about 1.5 dB/V reaching ~7.5 dB at 1.545 μm; the second peak, caused by the Ge buffer layer, is up to 5 dB at -4 V for wavelength greater than 1.57 μm. In Figure 7-18b the FOM spectra for different reverse biases are plotted; between 1.53-1.57 μm the absorption related to the GeSi/Ge stacked layers produces a FOM spectrum with a peak up to 0.5 at -4 V, whereas for $\lambda > 1.57$ μm a second peak builds up overcoming the principal peak, thanks to the low IL in this wavelength range; the full spectra, however, are not visible due to the limited bandwidth of laser and couplers.

7.3.3 High-speed Characterisation

The junction capacitance dependence from the P++ doping distance was underestimated in simulations (section 5.3.3), devices with P++ doping distances greater than 0.5 μm (device 1 to 15 in Table 7-1), in fact, were not able to generate an open eye diagram, reducing high-speed compatible devices to only five (device 17 to 21); among them, device W4-18 delivered stable eye diagram.

Device W4-18 was successfully operated at high-speed. In Figure 7-20a, the input electric eye at 56.2 Gb/s, is shown; for this device a DC reverse bias of 2.7 V was adopted confirming the good efficiency of this device, voltage swing of 2.2 V peak-to-peak or ~2.7 V rail-to-rail and laser wavelength of 1.56 μm were set, an electric rise time of 16.8 ps was measured. Figure 7-20b shows the output optical eye diagram, it was measured a 5.2 dB

dynamic ER and rise time of 16.8 ps. It must be said that the speed was not limited by the device itself but by the characterisation kit, capable of delivering up to 56.2 Gb/s.

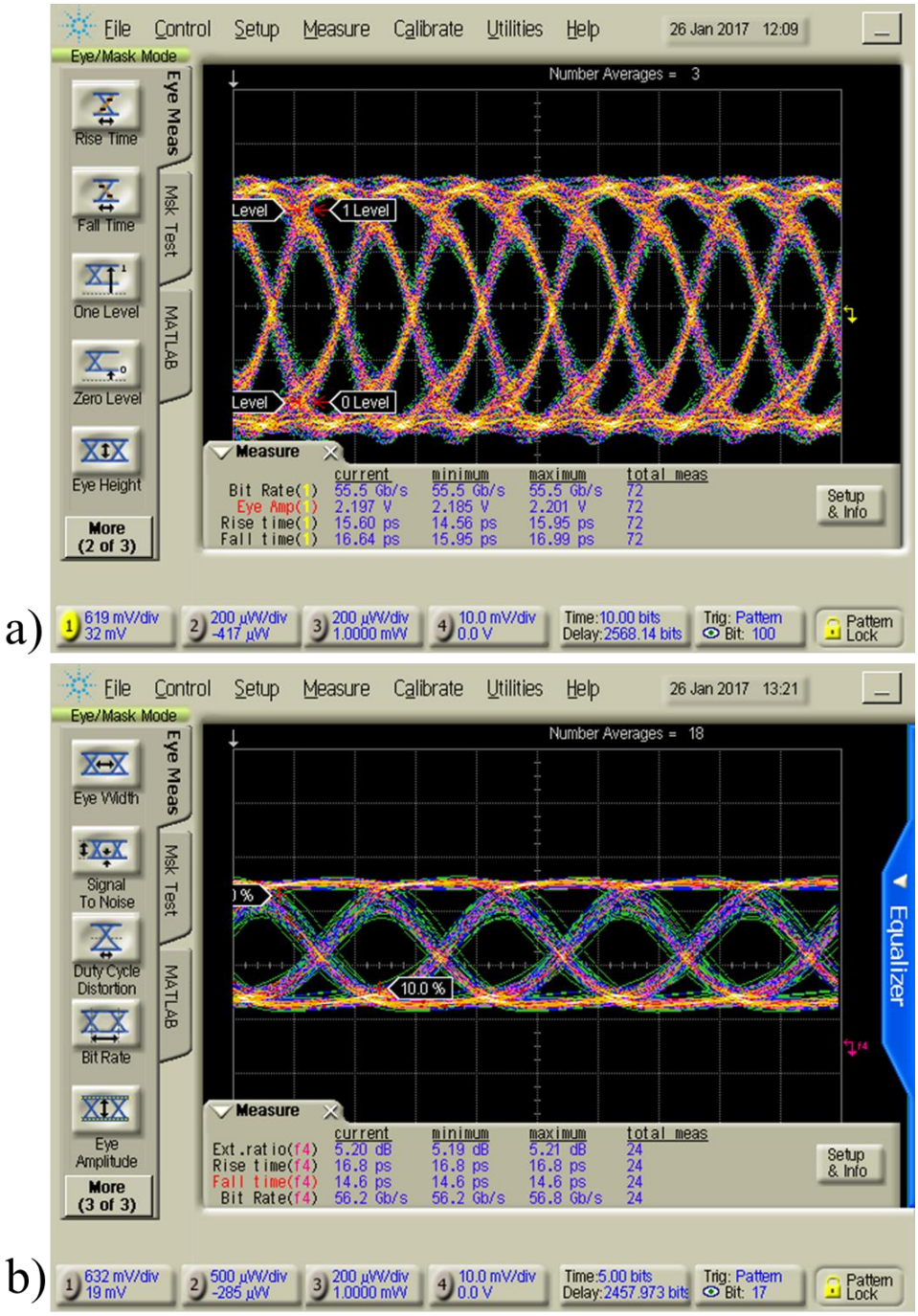

Figure 7-20 W4 device 18, a) input electrical eye diagram with 2.2 Vpp at 56 Gb/s; b) device eye diagram with an ER of 5.2 dB.

From the optic rise time and electric rise time of the device, the 3dB bandwidth was estimated to be 56 GHz.

7.3.4 RF Electric Characterisation

S11 parameters were measured for device W4-18 to evaluate the equivalent circuit shown in Figure 7-21 that includes the pad capacitance (C_{pd}) to better approximate the parasitic elements in the device. S11 magnitude and phase spectra were fitted with the model available in Agilent Advance Design System to evaluate the lumped elements, the experimental spectra and the fittings are shown in Figure 7-22.

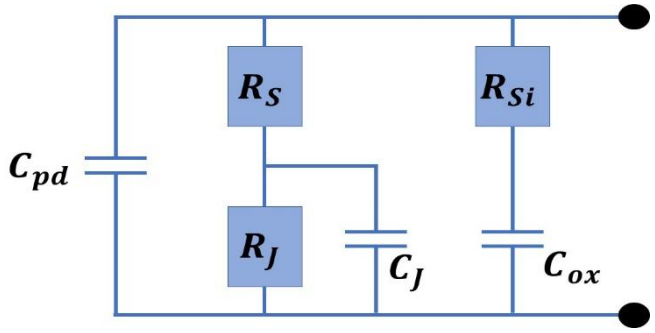

Figure 7-21 Equivalent Circuit

It was found, $C_{pd} = 5\,fF$, $R_s = 150\,\Omega$, $R_J = 1500\,\Omega$, $C_J = 11\,fF$, $C_{ox} = 30\,fF$ and $R_{Si} = 350\,\Omega$. The power of the EAM at 56 Gbps was evaluated to be $C_j V_{pp}^2/4 = 44\,fJ/bit$ considering a swing voltage $V_{pp} = 4\,V$ due to RF reflections caused by GS probes not 50 Ω terminated.

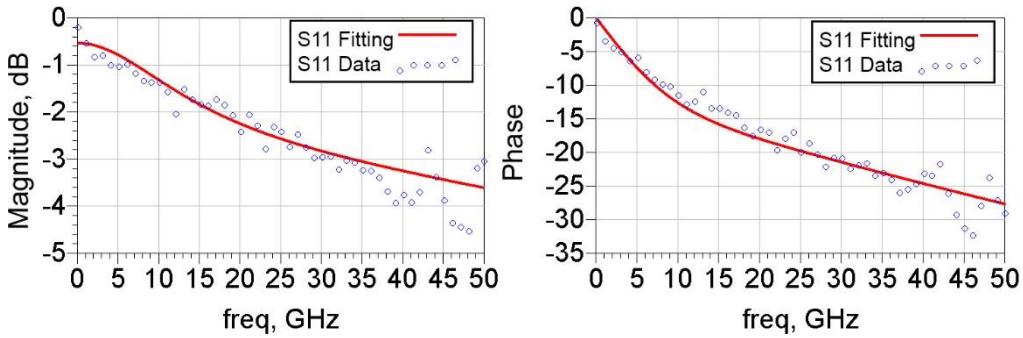

Figure 7-22 S11 Parameter at -3 V; the Magnitude and the phase of the measured device are plotted with circles; the result of the fitting with full line in red.

7.4 Comparison with simulation

Simulations are here compared with experimental data; since the platform only simulates the electro-absorption effect linked with the material, only the ER was considered. The simulation cross-section was defined from SIMS results presented in section 7.2, Si content in the GeSi alloy was set to an average 1.3%, whereas boron and

phosphorus concentration were both set to 1E19 cm^{-3}, the Devedit™ software version was adopted.

It was possible to fit the simulation to the experimental data as shown in Figure 7-23, but some consideration must be done; it was found that the primary ER peaks have good match if 0.47% tensile strain is applied to the GeSi layer, only at -4 V the simulated ER has a lower peak. The secondary peak, instead, can be matched in wavelength if 0.3% tensile strain is applied to the Ge layer, but discrepancy in the amplitude are evident. At -1 V the absorption peak linked to the Ge buffer layer is in line with the experimental data, however for higher reverse biases the peak difference increases, at -2 V the simulation spectrum (full red line) is about 0.5 dB less than the experimental curve (red dashed line), for -3 V (green lines) the difference is about 1 dB, little reduction of the principal peak is also seen. For -4 V the simulated ER, instead, is lower for the whole spectrum, a match with experiment is found only by applying -5 V in the simulation cross-section (magenta curve).

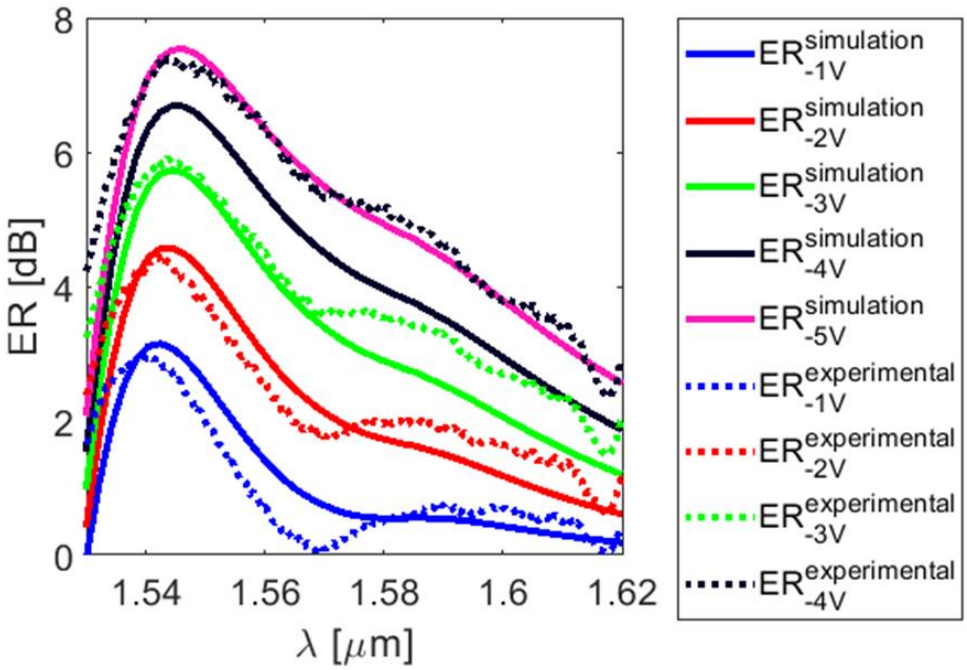

Figure 7-23 Simulation fitting by importing the electric field from Atlas™ output files.

Therefore, considering a multiplying factor (M) for the electric field distribution in the Ge buffer layer, a better match can be found with M = 2 for -1 V and -2 V, and M = 3 for -3 V, for -4 V the simulation is taken at -5 V without any multiplying factor, as shown in Figure 7-24.

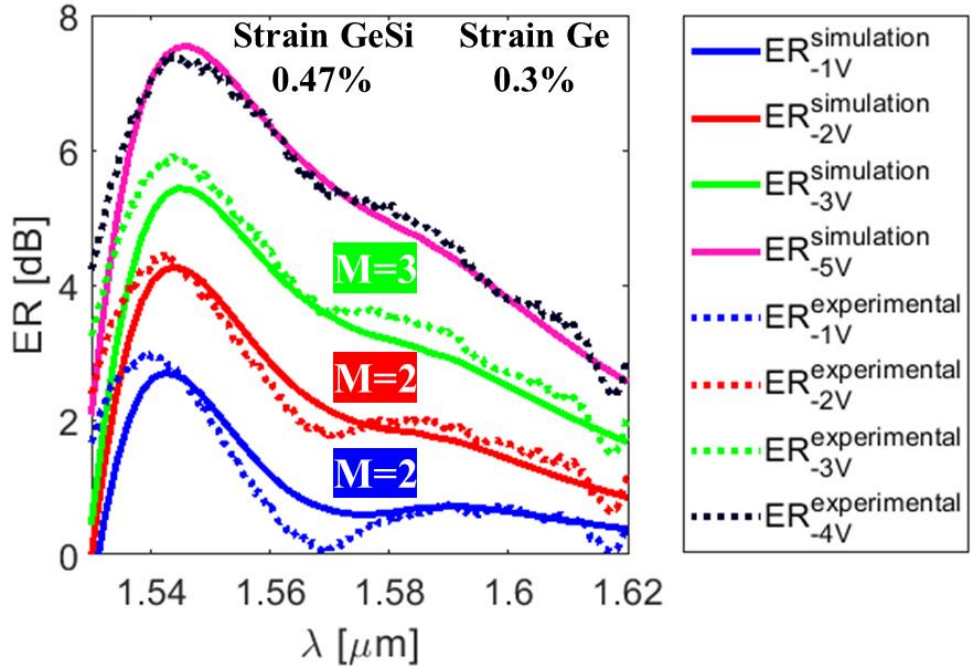

Figure 7-24 Simulation plots (full lines) by using a multiplying factor (M) in the Ge layer to match the experimental results (dashed lines). A factor M = 2 was used for simulations run with DC bias of -1 V (blue) and -2 V (red) and factor M = 3 for simulation run with DC bias -3 V (green). For DC bias of -4V the simulation is run at -5 V (magenta).

7.5 Summary

In this chapter the innovative wrap-around design reviewed in previous chapters, is presented. The process flow is analysed proving the simple fabrication involving five etches and four doping that are all executed with standard and well controlled CMOS techniques, already reviewed in Chapter 4. The first fabrication run was completed on wafer W4. Designs variations were implemented on each wafer by shifting the P++ and N++ contact doping between 0 μm to 1 μm from the rib edges to prevent device failure in the event of dopant diffusion from the highly doped region to the intrinsic rib region.

Results from W4 were promising, SIMS show a slightly lower Si content in the GeSi alloy, 1.3% on average, redshifting slightly the operation wavelength and sharp transition between the Ge buffer layer and the Si wafer overlay. Junction doping concentrations were in-line with design. Unfortunately, SIMS profile on the test wafer used for bandgap engineering through RTA showed strong Si migration in the alloy up to 13% in ~500 nm of thickness, compromising the device operability.

Devices from W4 were characterised, IV measurements revealed a dark current ranging from hundreds of nA to hundreds of μm, suggesting a passivation layer not properly

formed. Thanks to the uniform GeSi layer and good junction doping concentration, good ER and FOM spectra were found for almost all devices belonging to W4. Spectral analysis for different device combinations, revealed a dependency from the contact doping distances, confirming partially results in section 5.3.3. In high-speed, it was found that only designs with P++ doping distances below 0.5 μm from the rib edge could support high-speed operation, due to a junction capacitance more dependent from the P++ doping than that simulated in section 5.3.3; narrowing down the number of high-speed compatible devices to five. Thanks to the good DC ER (>7 dB at -4 V) and limited dark current, device W4-18 achieved high performances at 1.56 μm, supporting 56 Gbps modulation with dynamic ER of 5.2 dB and rise time of only ~16.8 ps, the 3dB bandwidth was calculated to be 56 GHz. Device W4-18 was also electrically characterised in RF by means of S11 measurements, permitting to calculate the elements of the equivalent circuit for small signal and then from the junction capacitance (11 fF), a power consumption of 44 fJ/bit was calculated considering reflections at the device ports that increased the net voltage to about 4 V. In the last section, simulations were compared with experimental results; to fit the data strain of 0.47% and 0.3% were set for the GeSi and Ge, respectively. While the principal ER peak was successfully matched for biases from -1 V to -3 V, the ER peak amplitude linked to the Ge buffer layer was found lower, especially at -3 V and -4 V. By applying a multiplying factor for bias -1 V to -3 V, a better match was found. Experimental ER at -4 V could instead be matched only with a simulation run at -5 V. The cause of this discrepancy is unresolved and will require further investigation.

Chapter 8

Conclusions

The advent of Internet deeply changed the way people communicate; pictures, video, all sort of data is sent at incredibly high speed thanks to a cheap, fast and reliable medium that is the optic fibre. In last decades, while optic fibre technology was improving with deployment of low loss and low dispersion silica fibres, new platforms and devices were developed with the goal of bridging electronics and optics; photonics was born [3]–[5]. Today, optic fibre technology is mature, hollow-core and multi-core fibres opened new paths of development [92]; meanwhile, SMF are replacing MMF fibres also for short range connections, making c-band datacentres preferred to those based on MMF. Datacentre links over 500 m are more common, making impracticable deployment of MMFs, due to high-loss. On the other hand, to cope with new services such as 5G [11], more bandwidth is required; link speed is expected to exceed 1 Tb/s by 2030 [10], making MMF datacentres obsolete, a reliable C-band photonic platform for short range communication distances, is therefore needed. This project, by exploiting the FKE in GeSi, investigates on a vertical modulator PIN design [150] to achieve electric distribution independency from the rib width, better optic confinement and support for both polarisations. In this thesis, Si, Ge and GeSi optic properties were given and compared to demonstrate the CMOS compatibility of germanium-based platforms. The communication link theoretical basis was illustrated to give essential tools to compare modulation strategies and implementations in CMOS platforms.

Comparison of selected works based on group IV materials was proposed with tables; three principal categories were found, the reliable and fast PDE-based modulators

capable of delivering 50 Gbps [136]-[141] at cost of big footprint and power budget, the exceptional spectral efficiency of QCSE-based diodes [144]-[147], for which waveguide integration is still a work in progress; the fast, compact and fully CMOS compatible FKE-based EAMs [30] [31] [148][149], that is a quite mature and yet advanced technology. DC and high-speed performances for the three groups were analysed with standard metrics, comparing advantages and disadvantages of each design, including the wrap-around FKE EAM fabricated in this work, showing high bandwidth with low power consumption, compatible with next-gen datacentre interconnects.

Informatics tools to develop the device design, test the fabrication process and build the fabrication masks, were introduced. Most of the fabrication was done in the Nanofabrication Centre of the University of Southampton, therefore, fabrication techniques and tools were introduced. Material characterisation was fundamental during and after fabrication, all characterisation tools were briefly discussed.

Subsequently, the important simulation platform, developed specifically for this project, was analysed in depth from the cross-section definition using a process approach or fixed boxes with predetermined characteristics, to the calculation of electric field distribution in DC and transient, followed by optic mode solution to evaluate the FKE in both conditions (DC and transient). Three simulation batches were inspected, necessary to study the effects of doping concentration on device performances, develop the doping process recipes and compare device with different doping alignments. From simulation results, device with best trade-offs in terms of speed and spectral efficiency was used to define fabrication masks. Additional simulations showing the Ge buffer layer impacts on spectral efficiency was examined. Simulations in Lumerical MODE and FDTD solutions were presented to define CGs and tapering of the waveguide for the mask layout, to evaluate the coupling efficiency at the waveguide Si-GeSi interface proving that the up to 30% faster Ge etch rate than that of Si would not cause major loss, and to demonstrate a low the impact of the slanted cavity sidewalls to the transmission power of the mode.

Starting from general cell layout, conformity and testing structures were included in the mask layout, due to the importance of having a uniform GeSi growth and the possibility to run SIMS study to verify material and doping quality. Waveguide layout was carefully designed to support only TE mode with coupling gratings; fundamental mode propagation only was ensured with a series of tapering that, by shrinking the width of sections of waveguide to 0.7 μm, would cut-off any higher mode. Important aspects of the device layout were given, the contact doping distance from the rib was swept between 21

combinations to maximise the number of working devices in case of dopant diffusion in the rib and investigate the effect of doping distance to the device performances.

A study on passive devices realised in a 500 nm thick SOI platform was presented, investigating bandgap shift with RTA to extend FKE EAMs operability from the C-band to the full L-band. For this purpose, passive waveguides were realised on cavities etched on the Si overlay and filled with a stack of 100 nm thick Ge and 300 nm thick GeSi with nominal Si content of 1.5%. Transmission spectra of 21 devices were measured and analysed before annealing on three samples; then RTA with different annealing time was performed, S1 was annealed for 5 min, S2 for 10 min and S3 for 20 min. All measurements were studied with the Tauc method [264][265] finding a maximum blueshift of 38 nm, with saturation time of about 10 min and loss per unit length reduction with annealing time. Material characterisation was conducted to understand the cause of blueshift, first SIMS demonstrated silicon migration from the Si overlay to the cavity, modifying dramatically the cavity composition. The 1.5% Si content in the GeSi before annealing reduced to 1.2%, whereas the Ge buffer layer was modified to GeSi with Si varying concentration between 1.2% to 15%. The second material study with innovative techniques to estimate material strain and dislocation mapping found low strain due to dislocations before annealing and strain accumulation after annealing, due to a more uniform layer. Longitudinal strain was accumulated especially in the region were the Ge buffer layer was before annealing; transversal strain was found (up to 5%), instead, in the rib. Simulations of device cross-section before and after annealing was proposed to investigate other plausible cause for the blueshift. Material complex refractive index was interpolated from reference [50] considering the GeSi stochiometric content, then a variation of the simulation platform calculated the mode distribution before and after annealing. The results agreed with the experimental findings, the mode slightly propagates in Ge buffer layer, affecting the device absorption spectrum; after annealing, the GeSi layer that replaced the Ge layer blueshifts the device absorption spectrum. The anneal-induced blueshift attributed to material composition variation, was concluded to be exploitable for tuning the material direct bandgap, allowing fabrication of device matrix with different wavelength operation condition, that would extend the total optic operation bandwidth of EAM modulators.

Fabrication process was reviewed pointing out all important steps, then SIMS results were analysed, for W4 composition and doping distributions were close to design, for the bandgap engineering test wafer W8, instead, the RTA compromised the material composition in the cavity. Dark current results of devices from W4 were reported, proving

a not fully successful passivation step process; then DC characterisation at chip level was inspected. A dependency from the contact doping distances from the rib edge was found for devices from W4, in partial agreement with simulations (section 5.3.3), device W4-18 performances were found compatible for high-speed operation. In agreement with simulations (section 5.3.4) all ER and FOM plots showed a second peak between 1.57 μm and 1.58 μm due to the contribution of Ge to the device absorption characteristics. Device characterisation continued in high-speed, unfortunately the effect of poor passivation layer leading to high dark current and the underestimated effect of contact doping distance to the junction capacitance, reduced the number of devices compatible with high-speed to those with N++ and P++ doping close to the rib edges. Improved masks design including devices with contact doping wells distance to the rib waveguide below 0.5 μm and a better passivation step seeking dark current reduction, need to be investigated. Among the working devices, the best performer was device W4-18, with a dynamic ER of 5.2 dB at 56 Gbps, 3dB bandwidth and power consumption of 56 GHz and 44 fJ/bit at 1.56 μm. W4-18 device proves the novelty of this project design, that brings independency of the electric field strength from the rib width enabling full design customisation while keeping standard process. W4-18 DC characteristics (ER) were also compared to simulations, showing that strain in the Ge buffer layer is lower than that in the GeSi layer and the electric-field is higher respect the field distribution calculated in Silvaco Atlas™.

8.1 Findings

Works on FKE modulators found in literature share a similar horizontal PIN design that limits the waveguide width to assure strong electric field in the rib. This project, by investigating on a vertical PIN diode, seeks to overcome limits linked to narrow waveguide (<1 um) such us optical confinement and losses. Three major outcomes are found:

- Simulations predicted the double peak in ER and FOM spectra, due to the underlying buffer Ge layer and investigated bandgap dependency from material composition, giving a tool for comparing designs with different characteristics (dimension, doping concentration and distribution) helping to define device design that fulfils requirements.
- Device characterisation demonstrated the novelty of the design proposed in this project, thanks to the high dynamic ER (5.2 dB) at 56 Gbps with rise time of 16.8 ps from which a 3dB bandwidth of 56 GHz was calculated;

speed, limited by the experimental kit not by the device, is expected to be higher. This design, therefore, proved to be a good candidate for fast, simple, low cost and fully CMOS compatible EAM for next gen interconnects.

- The third outcome of this project is the absorption blueshift with RTA; the bandgap shift study was successful on the 500 nm platform, the variation of the Ge buffer layer in a GeSi alloy with increasing Si content with depth shall account for the measured blueshift up to 38 nm, as simulations suggest. Other possible cause of blueshift after annealing should be seen in phonon generation, happening before annealing in the Ge buffer layer that redshifts the device absorption spectrum; after annealing the heating effect is avoided enhancing the post annealing blueshift.

8.2 Limitations

The research conducted in this work had a series of limitations:

- The simulation platform was limited in strain and temperature. ER spectra fitting with experimental results in section 7.4 revealed that different strain levels for GeSi layer and Ge buffer layer, should be considered; the fitting also showed an increasing ER mismatch in the Ge layer between simulation and experiment with voltage, imputable to limitation of the simulation platform in calculating the electric field distribution in the Ge layer. By setting a fixed temperature, phonon effects were not included in the model, the temperature-based bandgap shift might be missing in the calculations.
- Fabrication was not flawless; some wafers were lost due to process failure. Other wafers were annealed to reduce the Ge buffer layer contribution to the IL, as experimented in the material engineering study in Chapter 6; unfortunately, over-annealing compromised device performances by strong Si migration in the alloy.
- The passivation step did not work as expected, high dark current in some devices limited high-speed operability.
- While in DC devices with P++ and N++ contact doping at distances greater than 0.5 μm offered better efficiency, in high-speed were unresponsive due to a higher than expected junction capacitance.

- Finally, process development was carried on during fabrication, limiting the total number of available wafers at the end of process.

8.3 Perspectives

The natural evolution of this project is a second fabrication run with improved design, tackling lower IL by growing GeSi directly on silicon or diluting the buffer Ge with annealing. There are, however, other fields of research:

- Material characterisation needs to be addressed to find a full explanation to the stronger absorption due to the Ge buffer layer and blueshift after Ge removal.
- Bandgap shift study gives the opportunity to develop matrix of devices working at different operation wavelength by simple annealing; once the RTA recipe is set correctly, a simple method to extend the operation bandwidth beyond 100 nm, is at easy grasp.
- NRZ has been vastly adopted, but as introduced in the second chapter, PAM-4 modulation is expected to become more common for communication. This device, thanks to the high dynamic ER, is thought to handle PAM-4 without modification on the design.
- Specification of this project was the platform thickness, set to 800 nm to better couple light from the core of the optic fibre to the waveguide and better confine the mode in the waveguide; transferring this design on the widely used 220 nm platform would enable complete customisation to meet all needs although no significant improvement on the performances are expected respect the 800 nm platform.
- Finally, QCSE-based modulators are also very attractive for short-reach communication due to the possibility of tuning the operative wavelength around 1310 nm by tailoring the QWs thicknesses, thus overcoming the intrinsic optical bandwidth of FKE based modulators and enabling O-band operation. So far, high-speed measurements on real devices have not been demonstrated; with a process derived from this project, a fully working QCSE EAM can be fabricated.

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