Surface-modified Silicon Heat Sinks for IC Thermal Management

by

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ABSTRACT

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SURFACE-MODIFIED SILICON HEAT SINKS FOR IC THERMAL MANAGEMENT

by Yichi ZHANG

With fast development of science and technology, integrated circuits (ICs) are asked to work with high performance in a small size nowadays. Due to the rapid increase in the power density of ICs, microscale cooling methods for IC chips have received much more attention today. Heat sinks are a key component for device cooling technology. The project will focus on design, fabricate and characterise silicon micro fin/pin fin heat sinks that would be able to improve the cooling performance of the current available heat sinks. The thermal resistance of the conventional straight fin and pin fin heat sinks have been calculated, as well as of newly-proposed surface-modified silicon chips via analytical and numerical simulation methods. A novel surface-modified all-silicon 3D heat sinks has been proposed to be fabricated with combination of deep reactive ion etching and wafer bonding technologies. Experimental set up for transient thermal property is originally designed by integrating mini wind tunnel with Raman spectrometer to evaluate the cooling capability of the silicon chip with micro pin fin and fin structures. With help of hybrid finite element analysis of the heat transfer and flow dynamics of the system, it is clarified that increase of surface area with micro-structured pin fins is effective to improve the cooling performance of heat sinks both numerically and experimentally. Chip bonding technology to assemble the micro structured silicon chips and small spacers has been explored by developing an original sample holder and optimising process conditions. The idea and technologies developed in this project would be a solid basis of further researches on thermal property control of the system via nanotechnology.
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Declaration of Authorship

I, Yichi ZHANG, declare that the thesis entitled *Surface-modified Silicon Heat Sinks for IC Thermal Management* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published. A list of publications is provided with this manuscript:

Signed:..........................................................................................

Date:.............................................................................................
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Publications

Journal papers (In progress)


International Conference papers


Internal Conference papers


Nomenclature

**ITRS**  International Technology Roadmap for Semiconductors

**HHF**  High heat flux

**UHF**  Ultra-high heat flux

**EHF**  Extreme heat flux

**CHF**  Critical heat flux

**IC**  Integrated Circuit

**PC**  Personal Computer

**FEM**  Finite Element Modelling

**VLSI**  Very-Large-Scale-Integration

**θ_{max}**  Maximum Thermal Resistance

**R_{tot}**  Dimensionless Total Thermal Resistance

**R_{cond}**  Conduction Thermal Resistance

**R_{conv}**  Convection Thermal Resistance

**R_{heat}**  Thermal resistance of coolant absorbed heat

**HRIE**  High Rate Reactive Ion Etching

**DRIE**  Deep Reactive Ion Etching

**ICP**  Inductively Coupled Plasma

**PECVD**  Plasma Enhanced Chemical Vapor Deposition

**SEM**  Scanning Electron Microscope

**LPM**  Litre Per Minute

**TSV**  Through Silicon Via

**TCB**  Thermal Compression Bonding

**PVC**  Polymerizing Vinyl Chloride

**psi**  pound per square inch

**ε**  Porosity, Pitch to Diameter Ration

**\dot{Q}_{cond}**  Heat Transfer Rate by Conduction

**\dot{Q}_{convection}**  Heat Transfer Rate by Convection

**\dot{Q}_{Radiation}**  Heat Transfer Rate by Radiation

**\dot{Q}**  Power Density

**Q**  Thermal energy

**C**  Heat Capacity

**Q_{vh}**  Viscous Heating
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau$</td>
<td>Convection Cooling Time Constant</td>
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<tr>
<td>$S$</td>
<td>Pin Fin Pitch</td>
</tr>
<tr>
<td>$W_p$</td>
<td>Work Done by Pressure Force</td>
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<tr>
<td>$k$</td>
<td>Thermal Conductivity</td>
</tr>
<tr>
<td>$T$</td>
<td>Temperature</td>
</tr>
<tr>
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<tr>
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<tr>
<td>$A$</td>
<td>Surface Area</td>
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<tr>
<td>$A_b$</td>
<td>Exposed Heat Sink Base Area</td>
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<tr>
<td>$A_{fin}$</td>
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<td>Stefan Constant Value</td>
</tr>
<tr>
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<td>Surface Emissivity</td>
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<tr>
<td>$q$</td>
<td>Heat Flux</td>
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<tr>
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<td>Solid or Fluid Density</td>
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<td>Channel Reynolds Number</td>
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<td>Diameter of channel</td>
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<td>Diameter of heat pipe</td>
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<td>$D_p$</td>
<td>Diameter of pin fin</td>
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<td>$D_{pf}$</td>
<td>Diameter of perforated pin fin</td>
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<td>$H_c$</td>
<td>Height of Channel</td>
</tr>
<tr>
<td>$H_p$</td>
<td>Height of pin fin</td>
</tr>
<tr>
<td>$W_c$</td>
<td>Width of Channel</td>
</tr>
<tr>
<td>$W_f$</td>
<td>Width of fin</td>
</tr>
<tr>
<td>$W_w$</td>
<td>Width of wall between two channels</td>
</tr>
<tr>
<td>$b$</td>
<td>Channel Spacing</td>
</tr>
<tr>
<td>$L_f$</td>
<td>Length of fin</td>
</tr>
<tr>
<td>$\Delta P$</td>
<td>Pressure Drop</td>
</tr>
<tr>
<td>$v$</td>
<td>Flow Velocity</td>
</tr>
<tr>
<td>$\dot{Q}$</td>
<td>Dissipated Power</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>( \dot{m} )</td>
<td>Mass Flow Rate</td>
</tr>
<tr>
<td>( \eta )</td>
<td>Fin Efficiency</td>
</tr>
<tr>
<td>( N_g )</td>
<td>Number of Grooves</td>
</tr>
<tr>
<td>( P_{tot} )</td>
<td>Total Power Dissipated</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

1.1 Thermal Issues

Thermal issues become more important in electronic devices and integrated circuits (ICs) with increasing the number of transistors per single chip. Moore’s Law states that the number of transistors have been doubled every two years, indicating the operating power density and internal resistance of ICs have increased very fast and the heat flux from a single high performance chip have increased rapidly with the time. Figure 1.1 shows the transistor scaling down tendency in the gate length, and recently in 2018, IBM reported the successful fabrication of a transistor with a gate-all-around configuration with 5 nm node technology. This is a remarkable breakthrough beyond conventional FinFET design [1].

While the number of transistor per chip keep increasing, the clock frequency is capped around 4 GHz since 2000s as shown in Figure 1.2. A similar trend for the clock frequency and thermal design power can be seen, meaning that with the increase of the number of transistors per silicon chip, the power dissipation is increased rapidly and because of the limitation of the efficiency of heat removal technology with the fan heat sink cooling system. The heat design power is also increases with increasing of the clock frequency. But even with smaller size of transistors and modern fabrication technologies, the operating frequency is capped at 4 GHz in recent year with the traditional fan cooling technology. According to ITRS (International Technology Roadmap for Semiconductors) 2017 [3], the clock frequency under nominal power supply voltage is expected to keep at the same level around 4.2 GHz until 2033 if the heat can not dissipate efficiently. The power density of a high performance chip to be dissipated will expect 100 W/cm$^2$ in 2020 and it will continue to rise to 1000 W/cm$^2$ in future [4]. Thermal issues have become a big challenges due to the increased power density, even with the newest gate-all-around devices, conductance of the heat has been limited due to its confined architecture. In recent years, high heat flux removal technologies have received more attentions due to
the importance of thermal management of the high performance electronic devices, and during the last few decades, researchers around the world have made impressive progress and effort for the better cooling technology. However, this subject is still a big challenge that needs further study and investigation.

The level of the heat flux can be roughly classified into the following categories [5]:
High heat flux (HHF): $10^2$-$10^3$ W/cm$^2$, Ultra-high heat flux (UHF): $10^3$-$10^4$ W/cm$^2$, Extreme heat flux (EHF): $> 10^4$ W/cm$^2$. Various technological methods for the high heat flux removal have been investigated including microchannel heat sink, micro-pin fin heat sink, jet impingement techniques, heat pipes and so on. Among these methods, jet impingement cooling can provide better cooling capacity, but with the huge flowing resistance generated when the fluid flowing within the limited space, it is not suitable for the IC chip cooling [6]. Heat sinks are a key component for the current device cooling technology, and the regular metallic one can be found in the PC or laptop. Using heat sinks combined with forced air flow convection generated by fan is a popular and conventional heat removal method. For example with Intel Pentium 4 processor (3.06 GHz core frequency) generating 62 W/cm$^2$ heat flux where the chip temperature range is around 45 to 65 °C [7], power dissipation rate is reaching the limitation of the conventional heat sink with air cooling technology, which can only provide 1 W/cm$^2$ [5] (or less) heat removable capability. To spread the heat flux from the chips of such higher power dissipation rate, much larger air flow rates is required, meaning that much larger air fan is needed. This is not a good idea to do with as the noise generated by the fans is also a big problem as its level is approaching to human’s limitation. Therefore, a new thermal management technology to cool the chip with high power dissipation has to be explored. According to this, optimizing the cooling performance of the fan-cooled heat sink by modification of a part of heat sinks would be a thing to tackle the serious situation of HHF.

Material and geometry are the two factors which should be considered for the optimization of cooling performance of a heat sink. Therefore, materials with high thermal conductivity should be considered primarily, and the geometry of the heat sink is determined by the shape and the arrangement of the heat sink fins. Recently, development of silicon microfabrication technology opens a new way for alternative microscale cooling methods, showing in same cases, outstanding cooling performance. Materials are either copper or silicon, which has the thermal conductivity of 400 W/m·K and 150 W/m·K, respectively. Thanks to its native material properties, silicon has a relatively high thermal conductivity. Therefore, silicon can be used as a material to make heat sinks for efficient heat exchange. In addition, a big advantage of using silicon is that advanced micro and nanofabrication technology can be applicable to determine the geometry of the heat sink fins. A key technology to be developed is to increase the heat transfer area to achieve higher cooling performance to meet the HHF heat removal requirement.

1.2 Objective

The main objective of this project is to use silicon micro and nanofabrication technologies to modify the heat sink surface area, targeting to increase the heat transfer area to improve the heat sink performance. The most common material to make heat sinks is
metal, like copper or aluminium, because the thermal conductivity of these materials is higher than that of silicon. But as mentioned above, silicon has the thermal conductivity of 150 W/m·K, which is relatively comparable to aluminium’s thermal conductivity of 240 W/m·K. In addition, the recent development of silicon micro and nanofabrication technology can provide further flexibility to determine the optimal geometry of the heat sink fins. Another advantage of using silicon as the structural material to fabricate heat sinks is the potential for integration with IC chips. Figure 1.3 shows a diagram of a wafer level cooling system and the thermal circuit of this system which is shown at the right hand side. The aim is clearly to decrease the thermal resistance of the wafer and heat sinks. The heat sink thermal resistance can be decreased by modifying the surface structure of the fins. All of these optimizations are for increasing the heat transfer area to improve the cooling performance, and this can be realized by using silicon micro and nanofabrication technology. An idea of all silicon heat sinks has come up to my mind based on the aspects described above.

In this project, I will design the silicon heat sinks based on the silicon micro fabrication technologies, prototype the heat sink by using the fabrication facility available in the cleanroom, and then characterise the heat sink by using the evaluation system to be developed here.

1.3 Novelty Statement

After introducing the objective of the project, I want list my novel contributions as follow:

1). A novel measurement system which combines a mini wind tunnel with air flow and Raman spectrometer has been developed for the surface modified silicon chips. By monitoring the temperature obtained from the change of the silicon Raman peak position
after turning on and off the integrated heater, the characteristic time constant of heat spreading has been extracted for each silicon samples.

2). Newly-designed micro-fin and micro-pin fin surface structures has been simulated for both silicon heat sinks and individual silicon chips, the results observed that the increase of the surface area is found to improve the cooling performance efficiently, but a further increase will lead it worse.

3). An original fabrication process has been designed and developed by using DRIE technology for double-side-polished wafers. By adjusting the He flow pressure for wafer cooling during etching, well-controlled double-side deep etching with the etching depth of down to 150 µm has been achieved.

1.4 Thesis Structure

After the overview and introduction of the objective of the project, literature review and background research will be in Chapter 2 which cover the development of most significant types of heat sinks, including microchannel heat sinks, micro-fin heat sinks and micro-pin fin heat sinks, as well as fabrication technologies and experimental station set up, which are referenced for my works shown in the later chapters. Motivation of this work will be introduced based on the literature review. Then theoretical aspects of the heat transfer, fluid dynamics and thermal resistance will be introduced in Chapter 3, together with the analytical equations for estimation. The heat sink thermal resistance is calculated in Chapter 4 for the surface modified one, and systematic FEM simulations are investigated for designed micro fin and micro pin fin heat sinks. In Chapter 5, the fabrication process of surface modified silicon heat sinks is introduced, together with the optimization of the Deep reactive ion etching (DRIE) recipe to achieve double sides deep etching for silicon wafers, and the results of the bonding test for the silicon chips after fabricated. Experimental and characterization will be analysed in Chapter 6, novel experimental system with the combine of the Raman spectroscopy system and the mini wind tunnel under the microscope have been developed to measure the cooling performance of the surface modified silicon chips. Finally, conclusion and future works will be summarized in Chapter 7.
In recent decades, due to decreasing the chip size and increasing the amount of power dissipation, heat dissipation in the electronic systems has been rapidly increasing. To use heat sinks together with forced convection flow is one of the most common methods to dissipate the heat. Numerous investigation has been conducted during the past decades, which includes optimization of heat sink design and enhancement of effects of fluid convection. As the project is focused on the design of the heat sink based on silicon micro fabrication technology and heat transfer of single-phase fluid (flow with single phase, no phase changes from one state to another as a result of external heating), the main part of this literatures review is dedicated to surface modification of the heat sinks and the development of the heat transfer technology, particular with the fabrication technology of deep etching and bonding method. In this chapter, the history of heat sink and heat transfer technology development will be introduced first, and the fabrication technology of the silicon deep etching will be investigated second, together with the bonding technology for wafer level and chip level. Finally, the measurement method of heat transfer will be reviewed as well. Conclusion and motivation will be addressed at the end of this chapter.

2.1 History of heat sink and heat transfer technology development

This review of the heat sink development history mainly focuses on micro fin and pin fin heat sinks, enhancement of surfaces, microchannels and jet impingement. In relation to fluid dynamics, most of the reviews are about the single-phase flow, but variation of fluids such as air, water and some special refrigerants are considered. From the year
Table 2.1: Summary of relevant heat sinks and heat transfer technologies development studies

<table>
<thead>
<tr>
<th>Authors/Year</th>
<th>Geometrical Parameters</th>
<th>Heat Flux Removal (W/cm²)</th>
<th>Heat Removal Technologies</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hc = 302-320 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lazarek &amp; Black (1982)</td>
<td>D = 3.1 mm, semi-circ.</td>
<td>1.4-38</td>
<td>Microchannel, R113</td>
</tr>
<tr>
<td>Chor &amp; Yao (1987)</td>
<td>d0 = 0.429-0.559 mm</td>
<td>10-190</td>
<td>Piezoelectric droplets, water</td>
</tr>
<tr>
<td>Wambsganss et al. (1993)</td>
<td>D = 2.92 mm, circ.</td>
<td>0.88-9.075</td>
<td>Microchannel, R113</td>
</tr>
<tr>
<td>Bower &amp; Mudawar (1994)</td>
<td>L = 1 cm, D = 0.51 mm,</td>
<td>2.8-256</td>
<td>Microchannel &amp; minichannel, R113</td>
</tr>
<tr>
<td></td>
<td>2.54 mm (circ)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tran et al. (1996)</td>
<td>D = 2.46 mm (crinc.),</td>
<td>0.36-12.9</td>
<td>Microchannel, R12, R113</td>
</tr>
<tr>
<td></td>
<td>Dc = 2.4 mm (rect.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P.Teerstra &amp; J.R.Culham</td>
<td>b = 2.18 mm, L = 115 mm, H = 49 mm, N = 15</td>
<td>6-30</td>
<td>Plate fin heat sink, air</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lee &amp; Lee (2001)</td>
<td>Hc = 0.4-2 mm,</td>
<td>0.95-1.58</td>
<td>Microchannel, R113</td>
</tr>
<tr>
<td></td>
<td>Wc = 20 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chien &amp; Chun-Hsum (2001)</td>
<td>H = 1.8, 4.2, 8.2, 10.2 mm, t = 0.2-1.1 mm</td>
<td>0.54</td>
<td>Micro-fin heat sink, air</td>
</tr>
<tr>
<td>Warrier et al. (2002)</td>
<td>Dc = 0.75 mm,</td>
<td>5.99</td>
<td>Microchannel, FC84</td>
</tr>
<tr>
<td></td>
<td>Lc = 433.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Berre &amp; Latennard (2005)</td>
<td>Wc = 230 µm, 500 µm</td>
<td>60-180</td>
<td>Micro heat pipes, Ethanol, Methanol</td>
</tr>
<tr>
<td></td>
<td>Dc = 170 µm, 340 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Lc = 2.7 cm, circ.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dp = 20-100 µm,</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Huang et al. (2005) [21]</td>
<td>d0 = 30 µm, f = 31 Hz</td>
<td>5-50.3</td>
<td>Piezoelectric droplets, water</td>
</tr>
<tr>
<td>Hişhfeld et al. (2006)</td>
<td>channel size: 0.2 x 32 mm², 1 x 3 mm²</td>
<td>14-1430</td>
<td>Microchannel &amp; minichannel, water</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Colgan &amp; R.Schmidt (2007)</td>
<td>W = L = 2 cm, Wc = 65, 75 µm, Lc = 210, 250 µm</td>
<td>460</td>
<td>Microchannel, water</td>
</tr>
<tr>
<td>Brunschwiler et al. (2008)</td>
<td>Dc = 100 µm</td>
<td>74-537</td>
<td>Microchannel, water</td>
</tr>
<tr>
<td>Lee &amp; Mudawar (2009)</td>
<td>Dh = 175.7-415.9 µm,</td>
<td>27-960</td>
<td>Microchannel, HFE 7100</td>
</tr>
<tr>
<td></td>
<td>Lc = 1 cm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Koncar et al. (2010)</td>
<td>dh = 0.6-1.04 mm</td>
<td>401-1262</td>
<td>Jet impingement, He</td>
</tr>
<tr>
<td>Krishnamurthy &amp; Peles</td>
<td>Wc = 200 µm, Hc = 243 µm, Dh = 222 µm</td>
<td>10-110</td>
<td>Microchannel, enhanced surface, HFE 7000</td>
</tr>
<tr>
<td>(2010) [27]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Asthana et al. (2011)</td>
<td>Wc = 100 µm, Hc = 100 µm</td>
<td>143</td>
<td>Microchannel, serpentine water-oil</td>
</tr>
<tr>
<td>Foo &amp; Chin (2012)</td>
<td>Dpf = 8 mm (crinc.),</td>
<td>6</td>
<td>Perforated pin fin heat sink, air</td>
</tr>
<tr>
<td></td>
<td>Hp = 50 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adewumi &amp; Meyer (2013)</td>
<td>Wc = 0.06 mm, Hc = 0.48 mm, Hp = 0.16 mm, Dp = 0.04 mm</td>
<td>100</td>
<td>Microchannel-pin fins hybrid heat sink, water</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yeom &amp; Cui (2015) [31]</td>
<td>Hp = 150-400 µm, Dp = 75-700 µm</td>
<td>h = 250 W/m²K</td>
<td>Cu micro pin fin heat sink, air</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chiu &amp; Yu (2017) [32]</td>
<td>Dp = 0.45, 0.53, 0.66 mm, Hp = 2.5 mm,</td>
<td>30</td>
<td>Al micro pin fin heat sink, water</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ansari &amp; Kim (2018) [33]</td>
<td>Wc = Wp = 250 µm, Hc = Hp = 500 µm</td>
<td>50-900</td>
<td>Microchannel-pin fins hybrid heat sink, water</td>
</tr>
</tbody>
</table>
of 1981s, researchers began to investigate the practical implementation of heat removal technology, which includes the advanced heat sinks and heat transfer mechanism. Table 2.1 summarized the relevant heat sinks and heat transfer technologies with some of the presented literatures over the last 38 years.

In the table, \( D \), \( W_c \) and \( H_c \) are the diameter, width and height of the channel, respectively. \( W_w \) is the width of the wall between two channels. \( d_0 \) is the diameter of the droplet’s nozzle. \( b \) is the gap between the fins. \( t \) is the fin thickness. \( D_h \) is the hydraulic diameter of the channel. \( D_c \), \( D_p \) and \( D_{pf} \) are the diameters of heat pipe, pin fin and perforated pin fin, respectively. \( W_f \) and \( L_f \) are the width and the length of the fin. \( H_p \) is the height of the pin fin.

An idea of the microchannel heat sink as one of the cooling technologies was introduced in 1981 by Tuckerman and Pease [8] for the first time. Multiple microchannels were fabricated on the back side of the wafer that has integrated circuits on the top side of the surface. Because of the direct link of the heat source to coolants through, the wall fins or grooves with large heat transfer area, the best ever cooling performance was demonstrated at that time. This technology has received many attentions for its outstanding performance and its ability to be fit with the scaled silicon VLSI chips. Their report opened up a new way of thermal management, and most of the review papers published in this area have cited this pioneering paper. The compact water-cooled heat sink designed for silicon ICs showed maximum temperature rise of 71 °C above the input water temperature for the input power density of 790 W/cm\(^2\). Figure 2.1 shows the structure of this heat sink.

![Figure 2.1: Schematic view of the heat sink designed by Tuckerman and Peace in 1981. [8]](image-url)
Table 2.2: Tuckerman and Peace’s experimental results with different parameters. All the tests were done for the heat source area of 1 cm$^2$. [8]

<table>
<thead>
<tr>
<th>Expt</th>
<th>$W_c$ (µm)</th>
<th>$W_w$ (µm)</th>
<th>$Z$ (µm)</th>
<th>$P$ (psi)</th>
<th>$f$ (cm$^3$/s)</th>
<th>$\dot{Q}$ (W/cm$^2$)</th>
<th>$\theta_{\text{max}}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>56</td>
<td>44</td>
<td>320</td>
<td>15</td>
<td>4.7</td>
<td>181</td>
<td>0.110</td>
</tr>
<tr>
<td>2</td>
<td>55</td>
<td>45</td>
<td>287</td>
<td>17</td>
<td>6.5</td>
<td>277</td>
<td>0.113</td>
</tr>
<tr>
<td>3</td>
<td>50</td>
<td>50</td>
<td>302</td>
<td>31</td>
<td>8.6</td>
<td>790</td>
<td>0.090</td>
</tr>
</tbody>
</table>

Table 2.2 listed the parameters of the three sets of test and result, where $Z$ is the height of the channels, $P$ is the water pressure drop, $f$ is the water flow rate, $\dot{Q}$ is power density, and the $\theta_{\text{max}}$ is the maximum thermal resistance. The distances between the channels or the width of the walls is a symbol of $W_w$. The table shows that the best performance comes up with the NO.3 experiment, which has the same widths for the wall and channel. The thin-film WSi$_2$ resistor with the thickness of 1 µm was employed as the heat source and the area was designed the same as the base area of the microchannel heat sink, which is 1 cm$^2$. The heat sources were equipped on the front side of substrate instead of actual ICs. For fabrication, thin film was sputtered onto the front surface of the heat sink first and then thermally annealed to form the silicide. The rectangular microchannels with the width $W_c$ and depth $Z$ were fabricated at the back side of the structure. Thermocouples were used to monitor the temperature of the inlet and outlet water flow, and also the surface of the heat source. The cooling performance of 790 W/cm$^2$ was reported under the water pressure of 31 psi, corresponding to 214 kPa. For future design and optimization, they pointed out that reduction of the convection thermal resistance ($\theta_{\text{conv}}$) is an important point to improve the cooling performance of the microchannel heat sinks. This can be achieved by reducing the channel size and add as more channels as possible on a fixed size of IC chip, or making the channel closely to the circuit. But one big problem they also mentioned was how to minimise the pressure drop of the water flowing through the microchannels.

After Tuckerman and Pease’s pioneering work, Lazarek and Black [9] published a new way of cooling in 1982 with boiling of R-113 coolant in a small vertical tube to remove critical heat flux correlation. This was the first report of the two phase change cooling technology where the latent heat of the phase transition was used for cooling rather than just using the heat transfer from the heat sink to the coolant in the single phase technology. They also pointed out that for the two phase change cooling technology, the Nusselt number is a function of the Reynolds number of the coolant. In fluid dynamics, Nusselt number indicates the ratio of the convective heat transfer to conductive heat transfer when the heat transfer occurs at a sold-fluid boundary, Reynolds number is defined as the ratio of the inertia force to the viscous force of the fluid [34]. After the careful experiments, the boiling point with the threshold heat flux around 3 W/cm$^2$ was reported and the heat flux between 1.4 to 38 W/cm$^2$ had been removed as a result. At last, they mentioned that when the liquid coolant changed to vapour, the pressure drop was remarkably reduced compared to the case of the single phase flow. As the first
conception of jet impingement, Choi and Yao [10] employed piezoelectric transducer as the water droplet generator. The principle is to use the transducer to break the water streams into uniform drops in order to flow through the nozzle platforms. A maximum heat flux of 190 W/cm$^2$ was obtained during the experiment.

Wambsganss et al [11] worked on a boiling heat transfer in a horizontal minichannel with the coolant R-113, and the diameter for the small tube was 2.92 mm. They found the boiling heat transfer of R-113 in the small-diameter channels produce a slug flow pattern over a wide range of parameters when compared with large-diameter channels. The effects of high boiling number and slug flow pattern lead to domination by a nucleation mechanism. For the lowest wall superheat, heat transfer was found to be dependent on the heat flux and not on the mass flux. The result shows that it can remove the heat flux around 0.88 to 9.075 W/cm$^2$. Bower and Mudawar [12] did the experiments to find the value of the critical heat flux with both microchannel and minichannel heat sinks. They mentioned that with the lowest pressure drop of $\Delta P < 0.32$ bar, the critical heat flux with the value of 200 W/cm$^2$ can be obtained for both type of heat sinks. Furthermore, the minichannel has lower pressure drop than microchannel and easier to fabricate. Since then, many investigations have been done to improve the performance of the microchannel heat sinks and researchers move their steps back to the single phase water flow as they found that the two phases flow was more complicated than what they imaged and was immature area to solve the existing thermal problem. The water itself is considered the most suitable coolant with its high heat capacity.

Kawano et al. [35] did some numerical studies and experiments for the pressure drop and heat transfer in the microchannel heat sinks. Their design of the heat sink has a $15 \times 15$ mm$^2$ base area and with the 110 microchannels arranged in the area. The width and height of the channels are 57 $\mu$m and 370 $\mu$m, respectively. Water was used as the coolant and they assumed the condition of fully developed laminar flow in the simulations. Their experimental results gave the good agreement with the simulations for the pressure drop, which was for the Reynolds number of $0 < Re < 200$. Within this ranges, the thermal resistance is larger at the microchannel inlet port, and the heat sink has a higher temperature with lower inlet water flow velocity. Beyond this range, i.e $Re > 300$, the pressure drop in simulation was lower than the value obtained from experimental studies.

In 1999, P.Teertstra and J.R.Culham [14] published a paper which focused on the air flow cooling with plate fin heat sinks due to the mainstream cooling method in that time was based on fan with forced air flow. They introduced an analytical model that predicted the average heat transfer rate for forced air flow convection, pointed out that the average Nusselt number was a function of the heat sink geometry and flow velocity, and investigated some formulas to calculate it. Two matching pairs of aluminium heat sinks were configured in a back-to-back arrangement, and two 300 W pencil heaters were press-fitted in between them. The experimental set up of the two heat sinks is
Chapter 2 Literature Review of Heat Dissipation Technology

shown in Figure 2.2. One assumption they made was the temperature of the wall and base plate were equalled to each other, and another boundary condition assumption was adiabatic for both the baseplate and the end of the fins formed by the shroud. These assumptions are convenient to calculate the thermal resistance of the heat sink, and also used in this project. According to the assumption for their theoretical calculation of the heat sink cooling performance, they composited a new module to calculate the Nusselt number. To compare with the predicted calculation results, they did the experiment with the designed test station and obtained that, the results were consistent with each other when the calculation module include the fin efficiency.

Figure 2.2: Back-to-back heat sink prototype assembly (a), and schematic of test apparatus (b). [14]

The result was tested for the fully developed laminar flow with the Reynolds number between $0.1 < Re < 100$, and was compared with the theoretical calculation as shown in Figure 2.3. Note that $Nu_b$ and $Re^*_b$ are the Nusselt number and channel Reynolds number, respectively. The specific definition of the channel Reynolds number in this
article is that Reynolds number of the fluid multiplied by the channel aspect ratio. They pointed out the importance of including the fin efficiency calculation in the analysis, because from the graph we can see that if the calculation of the fin efficiency is not included, the calculation results are largely mismatched with the experimental results.

The number of publications has rapidly increased and the investigation for microchannel, micro fins and micro pin fins cooling reached to a high level since 2000s. As a new method for microchannel configuration, Harris et al. [36] developed a microchannel heat exchanger for the liquid-to-air heat transfer in 2000. Chien and Chun-Hsum [17] presented a novel cooling method that combined the micro pin fin heat sink and air cooling method together in 2001. The material of the heat sink is copper with thermal conductivity of 386 W/m$^\circ$C, the fin array has $22 \times 22$ pin fins and the base size is $35 \times 35 \times 2$ mm$^3$. After estimation of the thermal resistance of the six heat sinks containing six different pin fin thickness and two different fin heights, they found the optimum design among these heat sinks. For comparison, experiment was done by putting the fan and the heater at the top and bottom of the heat sinks, and the results showed a good agreement between the correlation and experimental data. Then in 2002, Judy et al. [37] reported the first experimental data which proved the continuum theory for liquid flows was also suitable for the liquid in microchannels. This was a big breakthrough for researchers who want to understand the liquid flow in the microchannels further. Sharp and Adrian [38] pointed out that the turbulent flow and laminar flow in microchannels are the two different forms, and the laminar flow will be transformed to the turbulent flow when the Reynolds number is almost equal to 2000, which is similar to macroscale channels. Nano fluid was introduced in microchannel heat sinks for the first time by Koo and Kleinstreuer [39], and they provided a conditional list of the cases where the nanofluids can make enhancement of cooling performance for single-phase microchannels in practical implementation. They pointed out that with at least 4% of nanoparticles the thermal conductivity of nanofluids can be improved, and also the heat transfer rate may be increased at the same time, with the nanoparticles adsorbed on the internal walls of the microchannels.

Figure 2.4: Micro pin fin heat sink concept. [20]
One of the most represented papers was published by Y. Peles [20] in 2004 that the forced convection heat transfer across a silicon micro pin fin heat sink was investigated. Very low thermal resistance was achieved and it was comparable with the previous data reported for the microchannel heat sinks. The silicon micro pin fin heat sink they tested is shown in Figure 2.4. It was suggested that the geometrical configurations should meet the following requirements: $10 < Re < 1000$ for the Reynolds number, $2 < L/D < 20$ for the length/diameter ratio corresponding to $200 \, \mu m < L < 400 \, \mu m$ and $20 \, \mu m < D < 100 \, \mu m$, and $0.5 < \varepsilon < 0.9$ for the porosity, a pitch to diameter ratio for the circular pin fins. Both air flow and water flow was tested and then compared to see the difference in their experiments. The relationship between the Reynolds number and $R_{\text{total}}$, the heat sink total thermal resistance for the evenly distributed pin fins with $\varepsilon = 0.65$, for the cases of the air flow and water flow is shown in Figure 2.5. The $R_{\text{total}}$ increases with the increasing Reynolds number, corresponding to increasing the flow rate. The heat convection thermal resistance will further increase when the fin efficiency dominates and it will be reduced at much higher Reynolds number [20]. Another important finding was that the thermal resistance for the water flow is higher than that for the air flow.

![Figure 2.5: Dimensionless $R_{\text{tot}}$ vs. Reynolds number $Re$ with $\varepsilon=0.65$, $C_2=1.953$, $C_3=0.9$, and $w_2/L=25$.][20]

![Figure 2.6: $R_{\text{total}}-\varepsilon$ cure profile for (a) $Re=10$, (b) $Re=100$ and (c) $Re=1000$.][20]
as observed, but not lower than what expected from the fact that the thermal capacity of the water is 4 times higher than that of the air. The author pointed out, although the coolant is an important factor, the heat sink geometry needs to be considered to improve the thermal resistance. The relationship between the total thermal resistance and porosity for the different Reynolds numbers is shown in Figure 2.6. The results show that the thermal resistance increases with reducing the pin fin density, corresponding to increasing the higher porosity ration. At the lower porosity (smaller than 0.7), the total thermal resistance is dominated by the fluid convection, and the dissipated heat will be absorbed by the fluid when it flowing through the heat sink with temperature increase. They also suggested that for the higher Reynolds number \(Re > 900\), the higher density of the micro pin fin is better and for the lower Reynolds number, the lower density is enough for the lower thermal resistance, for example, with Reynolds number of 10, the total thermal resistance is much lower even with the low micro pin fin density, which represented as \(\varepsilon = 0.85\).

Hirshfeld et al. [22] presented a water cooled microchannel heat sink for the accelerator with up to 1 kW/cm². In order to get this level of heat flux, the electron gun was employed as the heat source with up to 20 kW heating power. Both microchannel and minichannel were studied in the experiment, single microchannel with the flow area of \(0.2 \times 32 \text{ mm}^2\) and a set of 25 minichannels with flow area of \(1 \times 3 \text{ mm}^2\). Both of the channels have the same length of 50 mm. Their experiment verified that this cooling capacity can be obtained for both micro- and minichannels with relatively little cost in required pump power. On-chip microchannel cooling gives an outstanding cooling performance compare to the conventional cooling method. But if the microchannel are fabricated separately with the IC chip and bonded with a silicon substrate after that, the distance between the microchannels and the chip increases, so that the thermal resistance of conduction cannot be ignored. However, many discussions were made during the past 20 years based on this point, on-chip or off-chip fabrication? Which is better for the small size chip cooling? In my view, it depends on many aspects like application, performance requirement and cost. For the off-chip microchannel cooling technology, the most representative publication should be Colgan and R.Schmidt’s [23] off-chip microchannel design for high power chips in 2007. They used the fabrication technology at that time, and made a new off-chip microchannel heat sink with stagger fins. They presented a practical implementation of a single-phase Si off-chip cooler, and optimized the performance for very high power chips. Figure 2.7 and Figure 2.8 shows the design and assembly of the microchannel coolers. Two main parts consist the cooler, which are the manifold chip in Figure 2.7(a) and the channel chip in Figure 2.7(b). Both of the chips’ size are \(20 \times 20 \text{ mm}^2\).

Finally, a unit thermal resistance of 10.5 °C/W per mm² was demonstrated with the pressure drop of 5 psi (pound per square inch). Figure 2.9 shows the final result which includes monitoring of the temperature of the inlet water, the difference between the
average chip temperature and inlet water temperature and power with the description of the change of the pressure drop. More than 275 W/cm$^2$ heat flux was applied to the heater resistors, and the power was turned off when the temperature turned to be stable, so the result seems like a square wave in Figure 2.9. In this article, the author compared his design with Tuckerman and Pease’s microchannel, and he pointed out that with more advanced fabrication technologies, such as a high rate reactive ion etching (HRIE), fabrication of Si-based microchannels will be much easier and simpler.
Chapter 2 Literature Review of Heat Dissipation Technology

Figure 2.9: Test results with 250×25 µm staggered blunt fins, and the channel size is 195 µm in depth and 75 µm in width for various flows. [23]

On the other hand, he also explained that it would not be practical to form the microchannels directly on the back surface of the silicon chip. Two main reasons were mentioned: one is the cost, and another one is the limitation of the reduction of the thermal resistance. When a separate microchannel heat sink is integrated with a silicon chip, due to wider space available for the heat sink, it can increase the microchannel heat sink surface area with silicon fabrication technology, resulting in making the thermal resistance as low as possible. The strategy can be more effective rather than fabricating the microchannels directly onto the IC chip substrate with the very limited room. The size of microchannels was made with 75-100 µm in width, and 3 mm in length, and about 180 µm in depth. Another high heat flux removal by using jet impingement technology was presented by Koncar et al. [26] in 2010. With the nozzle diameter range of 0.6 to 1.04 mm, they investigated multiple jet impingement designs to remove high heat flux up to 1262 W/cm² by using helium flow with both experimental and numerical methods. The microchannel heat sink is one of the efficient cooling methods for the rapidly increasing heat dissipation of the microprocessors, and over the last decade, numerous investigations have been done for both the single phase flow and two phase flow with boiling. For the single-phase microchannel cooling technology, the roughness effects or the friction factor between the fluid and the internal channel walls, and the pressure drop problem are two big challenges for researchers. In order to improve the heat transfer, further efforts should be made: for example, optimization of the channel geometries by using silicon micro or nanofabrication technology, and exploring more suitable coolants than water. Nevertheless, other microscale cooling methods have also received many attentions recently. The finned and pin-finned heat sinks are commonly used today for increasing the convective heat transfer coefficients efficiently and reducing the thermal resistance at the same time. According to the advances of
silicon microfabrication technologies, it enables a new structure patterning for the fin and pin fin structures to scaling down the size to micro or nano scale and increasing the surface area extremely for convection heat transfer. Foo and Chin [29] created a new pin fin heat sink structure with perforation on the fins in vertical direction and horizontal surface surrounding. Figure 2.10 shows the schematic diagram of the heat sink structures. With numerical simulation, the heat sinks were studied in a rectangular channel under steady-state forced air flow for their heat transfer characteristics. They presented that with increasing the number of horizontal perforation and the diameters of them, Nusselt number increased significantly, but further increasing the diameters will lead to the thermal dissipation dropped down. This is because of the reduction of the heat conduction along the vertical direction while increasing the perforation. An optimum Nusselt number was obtained from the pin fin array with 5 perforations, and the diameter was 3 mm for both horizontal and vertical perforation. Recently in 2018, Ansari and Kim [33] simulated the performance of a microchannel-pinfin hybrid heat sink with single-phase water flow, and compared with that of a simple microchannel heat sink. Figure 2.11 shows the hybrid heat sink configuration with the micro pin fin heat sink at the center. In order to simulate the hotspot under a microprocessor in real situation, which the size usually varied in the range of 50 to 200 µm\(^2\), the background heat flux under the microchannel heat sink and the hotspot heat flux under the micro pin fin heat sink are different, which are 50 W/cm\(^2\) and 300 W/cm\(^2\), respectively. The total mass flow rate was selected from 0.0015 kg/s (Reynolds number = 200) to 0.0075 kg/s (Reynolds number = 1000), which can make sure the maximum temperature of the heat sink under an efficient performance microprocessor is within the recommended range [40]. The microchannel heat sink without micro pin fin structure in the center was also simulated for comparison. Both heat sinks were simulated for their cooling
limits under the condition of $R_e = 800$, hotspot heat flux increased from 300 to 900 W/cm$^2$ and the background heat flux under the microchannel heat sink was fixed at 50 W/cm$^2$. The computation results showed that the hybrid heat sink could maintain a 30.6% lower temperature rise at the hotspot than the non-hybrid heat sink when the Reynolds number equal to 200, which required a much lower pumping power. When kept the Reynolds number of 800 and varied the heat flux under the hotspot, more than 50% higher heat flux could be applied under the hotspot of the hybrid heat sink to maintain the maximum temperature under the recommended range when compared to non-hybrid heat sink. At last, they mentioned that the diameter and number of the pin fins can be varied to match the cooling requirements and the size of the hotspot.

### 2.2 Review of the fabrication and bonding technologies

Lau et al. [41] developed and designed a fabrication process for the jet impingement microchannel cooling technology. The nozzle array for the jet impingement part was fabricated with through silicon vias (TSV) process, and the microchannel heat sink was fabricated by using deep reactive ion etch (DRIE) process. After that, two silicon chips with nozzles and microchannels were bonded together by using thermal compression bonding (TCB) process together with AuSn as the inter layer, and the silicon chip with nozzles was treated as a lid to generate the microchannels.

The fabrication results of the microchannel chip and the nozzle chip are shown in Figure 2.12. The difference of the top and bottom fin widths are less than 10 µm, which is similar to the nozzle size. The depth of the microchannels were around 250 µm, and for the nozzles’ depth were around 350 µm. They mentioned that the fabrication results
Figure 2.12: Cross section view of fabricated silicon microchannels (a) and silicon nozzles (c) (d), top view of fabricated silicon microchannels (b). [41]

show that the processes they chose maintained the fabrications in good stability and uniformity.

Overviewing the past publications about the silicon high aspect ratio fabrication technologies, deep reactive ion etching (DRIE) is one of the most popular processes and Bosch process is often employed in that system because of the high selectivity to silicon dioxide hard mask. Ayon et al. [42] reported the mechanism of the Bosch process and the profile after etching. The Bosch process named after the company who developed it, which consisting of etching and passivating steps, and appropriate chemistry gas of SF$_6$ and C$_4$F$_8$ are used in etching step and passivating step, respectively. Figure 2.13 shows the etched trenches in ideal and real situations, together with the etching cycles in theory of the Bosch process.

Ideally the side wall and bottom of the trench should be smooth and flat, but in reality the side wall is scalloped and the bottom is shown like a U-shape. That is because of the cyclic nature of the Bosch process which is shown in Figure 2.13(c). They also mentioned that the trench width goes down because the side wall etching would lead to ‘rough’ side walls and the slope $\theta$ of the side wall should be lower than 90° after the Bosch process. Chang et al. [43] modified the normal Bosch process recipe in order to
Figure 2.13: Targeted profile of the Bosch process (a). Real profile after the trench be etched (b). The periodic cycles in the Bosch process (c). [43]

etch sub-micrometer deep trenches and meet the application of anti-reflection structures. According to the periodic etching cycles shown in Figure 2.13(c), they reduced the active times of etching and passivation so that the etching of the amount of silicon for each cycle was decreased, and this can change the roughness of the side wall to a more smoothed one. By reducing the flow rates of the reaction gases and the processing pressure, the anisotropy of the DRIE can be increased, but the etching rate for Si was decreased dramatically. At last, they mentioned that increasing the RF power in the etching steps could remove the passivation layer on the trench bottom efficiently and the anisotropy of DRIE was increased.

In the early 1990s, Schmidt [44] reviewed the wafer bonding methods for micromechanical devices at that time. He summarized the major points of the wafer bonding process: surface preparation, contacting and annealing. The surface preparation means cleaning the wafer surfaces to a mirror-smooth and flat one, which can form a hydrated surface. Then the contacting needs to be happened in a cleanroom environment by pressing the two surface at one point. The annealing step needs the temperature to rise up to 800 to 1200 °C, which can increases the bond strength significantly. He also mentioned that with the temperature beyond 1000 °C, the bond strength equals to the silicon crystal strength itself. Tong and Enquist [45] developed a method to realize covalent bonding
with silicon oxide interlayer at room temperature on the wafer level. What they did was introducing fluorine (F) into bonding oxide layers before bonding, and making the bonding energy equals to silicon fracture energy, which is 2500 mJ/m². The wafers they used were single-side polished 4 inch wafers with surface orientation of 100 and thickness of 525 µm. The thickness of the silicon oxide was generated with PECVD (Plasma Enhanced Chemical Vapor Deposition) process and the thickness was around 1 µm. Two years later, Liang and Bowers [46] reported a covalent bonding process for thermal silicon dioxide to PECVD silicon dioxide at low-temperature deposition, at 260 °C. Then the annealing was processed for 2 hours at 300 °C, leading to the surface energy of 2650 mJ/m². They obtained a record-thin 60 nm oxide interlayer which composed of 30-nm-thick thermal SiO₂ and 30-nm-thick PECVD SiO₂.

2.3 Review of the heat transfer measurements

Figure 2.14: The heat sink structure and dimensions (cm). [47]

Figure 2.15: Geometric configuration of heater block (a), and a real fabricated heater block (b). [47]
Zirakzadeh et al. [47] designed a new combined heat sink structures to test the heat transfer characteristics of miniaturised heat sinks, where Al$_2$O$_3$-water nanofluids are used as a coolant. This nanofluid is the mixture of Al$_2$O$_3$ particles suspended in water, which improves the thermal conductivity of water as it containing solid nanoparticles. The heat sink shown in Figure 2.14 contains a new structure combining the plate fin and columnar pins. The columnar pins are in between the plate fins to enhance the heat transfer area and the heat sink was fabricated from aluminium. The test was performed in the condition to provide a 180 W/cm$^2$ heat flux from the bottom of the heat sink by using a heater block manufactured by themselves, shown in Figure 2.15. Four K-type thermocouples were inserted to measure the temperatures of the heater and the different positions on the heat sink base plate. The other two K-type thermocouples were used to measure the inlet and outlet temperatures of the fluid. For the experimental station set up, they designed a flow loop together with the corresponding components shown in Figure 2.16. Test results were shown for four different conditions: (1) flat plate heat sink without pins among plate fins with water coolant, (2) flat plate heat sink with Al$_2$O$_3$-water nanofluids, (3) plate pin-finned (with pins among plate fins) heat sink with water coolant and (4) plate pined heat sink with Al$_2$O$_3$-water nanofluids. The results of the heat sink thermal resistance as a function of the flow rate is shown in Figure 2.17, and based on the results, they suggested that the Al$_2$O$_3$-water nanofluids increased the overall heat transfer coefficient while decreased the heat sink thermal resistance, and the plate pin-finned heat sink showed a better cooling performance by compared with the conventional plate fin heat sink.

![Figure 2.16: Schematic diagram of the experimental set up.](image)

Yeom and Cui [31] studied the heat transfer characteristics of micro pin fin heat sinks located in a narrow rectangular channel under different air flow rates in 2015. The
material they used for the heat sink is copper, and the dimensions of a micro pin fin are 150-400 µm in length and 75-700 µm in diameter. For the surface with the micro pin-fin structure, the maximum heat transfer performance was enhanced up to 79 % of that with the plain surface. Figure 2.18 shows a schematic diagram of the test station for the heat transfer coefficient. The micro pin-fin plate was placed on a copper block which contains a cartridge heater to generate heat. The width and height of the flow channel are 20 mm and 4.3 mm, respectively. All the micro pin-fin heat sinks tested in this experiment contains the staggered configuration array, as shown in Figure 2.18 in detail. The relationship between the heat transfer coefficient and volume flow rate, is shown in Figure 2.19. The heat sink with its micro pin-fin size of 250 µm in height and 400 µm in diameter shows the highest cooling performance where the heat transfer coefficient of around 250 W/m²·K with the volume flow rate of 60 LPM. They also pointed out
that when the pin fin height is fixed, effects of fluid dynamic become more dominant with increasing of the diameter of fins. This suggests that the enhancing the area of the surface of the micro pin-fin heat sinks can improve the cooling performance efficiently.

For temperature measurement of the heat transfer experiments, various methods can be used, commonly like thermal couple and infrared (IR) camera. For specific materials like silicon, Raman shift spectrum is good to use and has a promising performance. Hart and Benjamin [48] measured the raman spectrum shift of the silicon (111) over the temperature range of 20-770 °K. The Raman spectra were obtained by using argon ion laser with the 5145 Å line and an intracavity prism wavelength selector. The results of the spectra for the temperature of 20, 460 and 770 °K is shown in Figure 2.20.

The shift in frequency and change in amplitude can be observed clearly. The circles present the experimental data, and the triangles represent the frequency shift as calculated by Cowley [49] at 10, 100, 300 and 500 °K relative to the optical-phonon frequency of 525 cm$^{-1}$ at temperature of 0 °K. The results show that the Raman surface scattering is very useful for the study of the heat transfer properties of the silicon. Raman spectroscopy is useful not only for the heat transfer properties, but also for the information about energy dispersion and electronic structures. Iatsunskyi et al. [50] investigated the silicon nanostructures fabricated by using metal-assisted chemical etching process by analysing Raman spectra with one and two-phonon Raman peaks. The Raman spectroscopy was conducted by using the laser with wavelength of 488 nm, 514 nm and 633 nm, and the samples were focused with a 50x microscope lens in room temperature. Finally, clear difference of the Raman shift was observed between the 9 nm structure sample and 14 nm structure sample, suggesting smaller structure gives a smaller shift.
This result strongly suggests that Raman spectroscopy is a promising tool to detect the surface structure of silicon.

2.4 Motivation

As reviewed with the previous works of the heat sinks and heat transfer technologies, various technologies have been developed to remove the heat from the electronics chips effectively. One of the key things is to modify the geometry, in particular the surface structure of the heat sinks. Microchannel heat sink has the outstanding cooling performance for the rapidly increasing heat flux, but the friction factor and the huge pressure drop problem between the fluid and the internal channel walls are the two big challenges to investigate. DRIE microfabrication process is one of the most popular technologies in the MEMS and NEMS research field, but has not been applied yet for the surface patterning for the purpose of improving the heat transfer properties. Generally, most of the previous bonding processes were done with large contact area on the wafer level, and interface materials such as metal or silicon dioxide were commonly introduced. Technologies for chip-level small area bonding without interface materials have not been well investigated. The advances of silicon microfabrication technologies enables to explore a new way of the structure patterning of the fin and pin fin heat sinks, in particular
to scale down the size to micro or nano scale, and to increase the surface area much for enhancing convection heat transfer. For air flow cooling, my idea is to investigate double-side surface modified heat sinks. Figure 2.21 shows a schematic diagram of the surface-modified heat sinks to be developed in this project.

![Figure 2.21: Cross section view of the silicon heat sink after bonding with the spacers and surface modification with fabricated microstructure.](image)

After reviewing relevant literature about methods of heat transfer properties of heat sinks, especially for the micro and nano-structures, analysis of the Raman Stokes peak position shift due to the change of the temperature has found to be a promising method. But the analysis of the combination of Raman spectroscopy and fluid dynamics have not been established yet. With air flow integrated to the micro-Raman microscopy system, a novel measurement system could be developed and the cooling performance of the surface-modified silicon heat sinks should be measured innovatively.
Chapter 3

Theory of Heat Transfer and Fluid Dynamics Mechanisms

In order to investigate the subject of thermal management and improve the cooling performance of heat sinks, fundamental knowledge of heat transfer and fluid dynamics should be studied carefully. The heat transfer is the form of energy transfer essentially, and it takes place between two objects which have temperature difference. There are three different mechanisms of heat transfer, which are conduction, convection and radiation. This chapter will introduce the mechanism of heat transfer first, and then some basic knowledge of fluid dynamics will be presented, including some useful dimensionless quantity numbers, definition of laminar flow and turbulence flow and definition of flow entrance length which is used in the simulation software to define the boundary conditions. The definition of thermal resistance will be introduced later together with some equations used in Chapter 4 to estimate and calculate the cooling performance of the heat sinks.

3.1 Heat transfer Mechanisms

3.1.1 Conduction Heat transfer

This part is mainly referenced from the book written by Rohsenow et al. [51].

The conduction heat transfer happens when the two sides of a material has temperature difference. The materials can be classified as three types, which are metals, gas or liquid and crystalline solid. From the point of view in microscale, the conduction heat transfer will happen through different media when the types of the materials are different and this phenomenon depends on the material itself. Table 3.1 lists the mechanisms of conduction heat transfer in different materials.
Table 3.1: Conduction heat transfer methods in different materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Heat conduction transfer method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metals</td>
<td>Energy transfer between free electrons</td>
</tr>
<tr>
<td>Gas, liquid</td>
<td>Collision and diffusion of the molecules during their random motion</td>
</tr>
<tr>
<td>Crystalline solid</td>
<td>Energy exchange between vibrating molecules in a lattice</td>
</tr>
</tbody>
</table>

Consider a plane wall with thickness of $\Delta x$ and surface area $A$ whose cross section is shown in Figure 3.1. The direction of the conduction heat transfer is labelled in the diagram. Temperatures at the left and right sides of the wall are $T_1$ and $T_2$, respectively. So the temperature difference is $\Delta T = T_2 - T_1$, and the proportionality formula of conduction heat transfer rate can be written as:

$$\dot{Q}_{\text{cond}} \propto A \frac{\Delta T}{\Delta x}.$$  

(3.1)

When a constant $k$ is introduced into the proportionality correlation, the equation can be written as:

$$\dot{Q}_{\text{cond}} = -k A \frac{\Delta T}{\Delta x},$$  

(3.2)

where $k$ (W/m·K) is the thermal conductivity, and the negative sign is a tradition to make $\dot{Q}_{\text{cond}}$ positive if the conduction heat transfer is along the positive $x$ direction. In the limit of $\Delta x \to 0$, the equation above becomes to:

$$\dot{Q}_{\text{cond}} = -k A \frac{dt}{dx},$$  

(3.3)
which is known as Fourier’s law of heat conduction. When transferring the equation of conduction heat transfer to general formula, it becomes:

\[ \dot{Q}_{\text{cond}} = kA \frac{(T_{\text{hot}} - T_{\text{cold}})}{L}, \]  

(3.4)

Where \( T_{\text{hot}} - T_{\text{cold}} \) (K) is the temperature difference between the two sides of the conductor, \( L \) (m) is the thickness of the conductor, corresponding to \( \Delta x \) in Figure 3.1. An idea of the thermal conductivity is similar to that of the electrical conductivity. The lower \( k \) indicates harder to conduct heat and the thermal insulator has much lower value of \( k \).

### 3.1.2 Convection

Convection heat transfer occurs at the interface between the heat sink and the coolant fluid. There are two types of convection heat transfer, which are forced convection and natural (or free) convection. Natural convection means the fluid motion is generated by a density difference due to a temperature difference in it. The main driving force of the natural convection is gravity [34]. The forced convection does not depend on the gravity but on the movement of cold and hot fluids forced by fans or pumps. The difference between them is the source of the fluid motion.

Regarding to Figure 3.2, we can write the equation of convection heat transfer rate as:

\[ \dot{Q}_{\text{conv}} = hA_{\text{conv}}(T_S - T_F), \]  

(3.5)
where \( h \) (W/m\(^2\)-K) is called heat transfer coefficient, \( A_{\text{conv}} \) (m\(^2\)) is the heat convection area and \( T_s - T_F \) (K) is the temperature difference between fluid and surface. This equation is also known as Newton’s law of cooling [34].

The heat transfer coefficient (or film coefficient) is a parameter to indicate the convection heat transfer. The definition of the heat transfer coefficient \( h \) is:

\[
h = \frac{q}{\Delta T}, \tag{3.6}
\]

where \( q \) (W/m\(^2\)) is the heat flux based on the film or surface, and \( \Delta T \) (K) is the temperature difference between the solid surface and surrounding fluid [51]. Note that the thermal resistance of the heat sinks is the inverse of the heat transfer coefficient, which will be shown later with the definition of the thermal resistance.

When considering the transient properties, i.e. temperature as a function of time, the Newton’s law of cooling noted above is described as follows:

Given the total thermal energy \( Q \), the heat capacity \( C \) (J/K), which indicates that with the temperature of the body raise by one unit the amount of heat energy required to provide to the body, and temperature \( T \) of the body, \( Q \) is expressed as [34]:

\[
Q = CT. \tag{3.7}
\]

When \( Q \) is expected to change as a function of time with respect to the temperature difference of the body and surroundings, the differential equation with regard to the time is:

\[
\frac{dQ}{dt} = C\frac{dT}{dt}, \tag{3.8}
\]

and if the temperature of the body is \( T(t) \) at the time \( t \), temperature difference between the body and the surrounding is \( \Delta T(t) \). Then we have:

\[
\frac{dT(t)}{dt} = -\frac{\Delta T(t)}{\tau}, \tag{3.9}
\]

where \( \tau \) is the characteristic time constant of the system, and it can be expressed as:

\[
\tau = \frac{C}{hA}, \tag{3.10}
\]

where \( h \) is the heat transfer coefficient and \( A \) is the heat convection area. By solving the differential Equation 3.9, it gives:

\[
T(t) = T_s + \Delta T(0)e^{-t/\tau}, \tag{3.11}
\]

where \( T_s \) is the temperature of the environment surrounding the body and \( \Delta T(0) \) is the initial temperature difference of the system. With \( \Delta T(t) = T_t - T_s \), Newtonian solution
3.1.3 Radiation

For the radiation heat transfer, it happens under the condition of no medium between the two objects, which have different temperatures and they should facing each other. The heat transfer happens through the exchange of electromagnetic wave or photons [34]. Figure 3.3 shows a case of radiation heat transfer that happens between an object and its surrounding box at the temperature $T_{surr}$, where the object has uniform temperature $T_s$ and with the surface area of $A$.

The equation of radiation heat transfer rate is:

$$
\dot{Q}_{\text{rad}} = \sigma \varepsilon A (T_s^4 - T_{surr}^4),
$$

(3.13)

where $\sigma$ (W·m$^{-2}$·K$^{-4}$) is the Stefan constant with the value of $5.67 \times 10^{-8}$, $\varepsilon$ is the surface emissivity, and $T_s^4 - T_{surr}^4$ (K$^4$) is the temperature difference between the object and the surrounding. The $\varepsilon$ equals to the ratio of the emissivity power of the surface to the emissivity power of a black-body at the same temperature, with the unit of 1. Note that the units of $T_s$ and $T_{surr}$ should be in an absolute units, Kelvin (K) or Rankine (R) [34].

Here I want to introduce the radiation heat transfer coefficient, $h_{rad}$. Equation 3.13 can be transferred to the format of:

$$
\dot{Q}_{\text{rad}} = \sigma \varepsilon A (T_s^2 + T_{surr}^2)(T_s + T_{surr})(T_s - T_{surr}).
$$

(3.14)

When compared with the Equation 3.5, the radiation heat transfer coefficient $h_{rad}$ can be introduced as:

$$
h_{rad} = \sigma \varepsilon (T_s^2 + T_{surr}^2)(T_s + T_{surr}),
$$

(3.15)
then an equation of the radiation heat transfer rate can be written as:

\[ \dot{Q}_{\text{Rad}} = h_{\text{rad}} A (T_s - T_{\text{surr}}). \]  

(3.16)

Here the equation of the radiation heat transfer rate is transferred to a very similar equation to Newton’s law of cooling for the convection heat transfer rate, and it is more convenient to use this equation to calculate the radiation heat transfer coefficient in some situations [34].

### 3.1.4 Heat transfer in solid and fluids

Some equations which used in my simulation works in this thesis will be introduced in this section. The heat transfer interface uses an elliptic partial differential equation to calculate the temperature with the form:

\[ \rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = \dot{Q}, \]  

(3.17)

where \( \rho \) (kg/m\(^3\)) is the density of a solid material, \( C_p \) (J/K) is the heat capacity, \( k \) represents the thermal conductivity and \( \dot{Q} \) (W/m\(^3\)) represents the heat transfer rate of the heat source [52]. For a time-dependent problem, Equation 3.17 is called to analysis. As the study of this project focuses on the stationary condition, Fourier’s law of heat conduction \( \dot{Q}_{\text{cond}} \), which shown in Equation 3.3 is called to calculate the temperature gradient \( \nabla T \) in the heat transfer in solids, when only conduction is considered:

\[ q = -k \nabla T. \]  

(3.18)

The equation of the heat transfer in fluid is shown as [52]:

\[ \rho C_p \frac{\partial T}{\partial t} + \nabla \cdot q = Q + Q_{\text{vh}} + W_p, \]  

(3.19)

where \( W_p \) is the pressure work, due to the work done by pressure force, \( Q_{\text{vh}} \) is the viscous heating, which is generated by the viscous friction during the fluid flow through the channel, and this is usually very small.

### 3.2 Fluid Dynamics

In this section, three basic dimensionless quantity numbers which are used to describe the nature of flow dynamics are introduced. Those are the Nusselt number, Reynold number and Prandtl number. Basic knowledge of laminar and turbulence flow will be described together with some other parameters in fluid dynamics which are used in this project.
3.2.1 Dimensionless quantity numbers

The definition of dimensionless quantity is that a quantity to which no physical dimension is assigned. It is also known as bare number or pure number and the unit of it in the SI is one unit [53]. Dimensionless quantities are widely used in many fields, and the three basic dimensionless numbers in fluid dynamics are very useful and significant.

3.2.1.1 Reynolds Number

In fluid mechanics, Reynolds number is used to predict a pattern of the flow in different situations. It is defined as the ratio of the inertia force to the viscous force, and the laminar flow and turbulent flow are two characteristic flow states which can be indicated by this number. The definition of Reynolds number is:

\[
R_e \propto \frac{\text{inertia force}}{\text{viscous force}} = \frac{\rho v^2/L}{\mu v/L^2} = \frac{\rho v L}{\mu}, \tag{3.20}
\]

where \(v\) (m/s) is the velocity of the object relative to fluid, \(\mu\) (kg/m\(\cdot\)s) is the dynamic viscosity of the fluid, \(\rho\) (kg/m\(^3\)) is the density of the fluid and \(L\) (m) is the characteristic length used in calculation. The \(L\) varies depending on different situation. When considering a flow passing through a flat plate, the characteristic length is the distance that the flow passes. For a flow across a cylinder, the characteristic length is the diameter of the cylinder. There is a specific value of the Reynolds number to distinguish whether the flow is laminar flow or turbulence flow, and different flows have different values. This value is called critical Reynolds number. When a Reynolds number of a specific flow is less than the critical number, the flow is laminar flow. The turbulence flow occurs when the Reynolds number is greater than the critical number [34].

3.2.1.2 Prandtl Number

The Prandtl number indicates how well the molecules of a fluid to transport energy, which can be expressed in the momentum and thermal energy. So it can be defined as the ratio of the momentum diffusivity to thermal diffusivity. The Prandtl number is defined as:

\[
Pr = \frac{\text{viscous diffusion rate}}{\text{thermal diffusion rate}} = \frac{\nu}{\alpha} = \frac{\mu/\rho}{k/(c_p \rho)} = \frac{C_p \mu}{k}, \tag{3.21}
\]

where \(C_p\) (J/kg-K) is the specific heat (or thermal capacity) which is the amount of heat needed to raise the temperature of a certain mass by 1 degree Celsius, \(\nu\) (m\(^2\)/s) and \(\alpha\) (m\(^2\)/s) are momentum diffusivity (or kinematic viscosity) and thermal diffusivity of the fluid, respectively, and \(k\) (W/m-K) is the thermal conductivity.

Note that while the Reynolds number depends on the length scale of the system, no such length scale is found in the definition of the Prandtl number, which only depends
on the fluid state. When the momentum diffusivity dominates, $Pr >> 1$, and when the thermal diffusivity dominates, $Pr << 1$. Gases like air have the Prandtl number of approximately one, meaning the energy generated by molecules in air with momentum and thermal behaviour are comparable. Liquid and metals have very low Prandtl number. Therefore the thermal energy diffusivity is much larger than the momentum diffusivity. Furthermore, oil has a much higher Prandtl number, indicating that the molecules’ momentum is much more effective than thermal diffusion. For most cases, $Pr$ is approximately constant and can be found in property tables together with other conditions, such as the temperature and thermal conductivity [54].

### 3.2.1.3 Nusselt Number

If the convection heat transfer coefficient is converted to a dimensionless format, it is called the Nusselt number and can be expressed as:

$$N_u = \frac{hL}{k}, \quad (3.22)$$

The Nusselt number indicates the ratio of the convective heat transfer to conductive heat transfer when the heat transfer occurs at a solid-fluid boundary. Here I want to show the derivation of Equation 3.22 for better understanding. The heat transfer rate along the y-axis due to convection mechanism is:

$$\dot{Q}_y = hA(T_s - T_\infty), \quad (3.23)$$

where $T_s - T_\infty$ is the temperature of the surface with reference to the temperature of fluid free stream, $T_\infty$. The heat transfer at the surface is also expressed by considering conduction heat transfer:

$$\dot{Q}_y = -kA \frac{\partial(T - T_s)}{\partial y}_{y=0}, \quad (3.24)$$

where $T$ is the fluid temperature. As the convection heat transfer rate along the y-axis is equal to the conduction heat transfer rate, the equations below are obtained:

$$-kA \frac{\partial(T - T_s)}{\partial y}_{y=0} = hA(T_s - T_\infty), \quad (3.25)$$

$$\frac{h}{k} = \left. \frac{\partial(T_s - T)}{\partial y} \right|_{y=0} \frac{T_s - T_\infty}{T_s - T_\infty} \quad (3.26)$$

To make them dimensionless, the representative length $L$ is multiplied:

$$\frac{hL}{k} = \left. \frac{\partial(T_s - T)}{\partial y} \right|_{y=0} \frac{T_s - T_\infty}{L}, \quad (3.27)$$
Here the numerator of the right-hand-side of the Equation 3.27 is the ratio of the surface temperature gradient to the reference temperature gradient, and it is also the ratio of the conductive thermal resistance to the convective thermal resistance of the fluid. Note that similar to the Reynolds number, the Nusselt number also depends on the length scale variable. The Nusselt number is used to measure the increase in heat transfer due to fluid motion, and it is served as a link to connect heat transfer and fluid dynamics together [55] [56].

In order to be convenient to calculate the Nusselt number for the forced convection laminar flow, some useful expressions of Nusselt number under different conditions are summarised in the Table 3.2. For the flow over a flat plate, $N_u_x$ is the local Nusselt number at a distance $x$ from the leading edge of the plate and $\bar{N}_u_x$ is the average Nusselt number with the same distance $x$. For the equation of the Nusselt number with the fully developed pipe flow, $D_h$ is the hydraulic diameter, which will be introduced in the next section.

<table>
<thead>
<tr>
<th></th>
<th>On flat plate [34]</th>
<th>Fully developed pipe flow [57]</th>
<th>Across cylinders [14]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_u_x$</td>
<td>$0.332 Re_x^{1/2} Pr_x^{1/3}$, $\bar{N}_u_x = 2 N_u_x$, $Pr \geq 0.6$.</td>
<td>$Nu = \frac{h D_h}{k_f}$</td>
<td>$Nu = \left[ 1 \left( \frac{Re x}{2} \right)^{1/3} + \frac{1}{(0.664 \sqrt{Re} 10^{0.33} / \sqrt{1+3 Re})} \right]^{-0.33}$</td>
</tr>
</tbody>
</table>

### 3.2.2 Laminar and Turbulent Flow

Every flow should have both driving force and resistance force. The driving force is inertia force in forced convection and buoyancy force in natural convection. The resistance force can be frictional or viscous force. Based on the definition of Reynolds number, when the viscous force is dominated, the flow will be slowed down and presents laminar behaviour, which is called laminar flow. If the driving force is much larger than the viscous or frictional force, the flow becomes fluctuating and disordered, which is called turbulent flow [34]. Note that a flow can be changed from laminar to turbulent from one region to another, due to various reasons such as flow velocity, surface roughness and so on.

Figure 3.4 shows two laminar flows over a cylinder with different Reynolds numbers: (a) a very viscous flow with $Re = 1.54$ and (b) a flow with much higher $Re = 10000$. From Figure 3.4a we can observe that the flow with streamlines stays attached with the cylinder before and after across it, which indicates the flow is still in laminar behaviour after passed through the cylinder. For a flow with $Re = 10000$ shown in Figure 3.4b, we can see the flow is separated and not attached to the surface of the cylinder after passing through it, indicating the flow is changed to turbulence phenomenon. Compared with
Figure 3.4a, the clear streamlines have disappeared and disordered flow with random movement bulk fluid can be observed in the turbulent flow region.

Figure 3.4: Two laminar flows over a cylinder: (a) $Re = 1.54$ and (b) $Re = 10000$. Flow streamlines were made visible by aluminium powders in water [58].

For most situations, laminar flows are steady-state flows which means the flow variables do not change with time. On the other hand, many turbulent flows are transient flows which means they change with time. This indicates that the fluid velocity in a turbulent flow is time dependent and fluctuating with both magnitude and direction [34]. So the analysis for turbulent flow is very difficult and complex.

In the simulation works of this project, laminar flow in steady-state are calculated by solving Navier-Stokes equation:

$$\rho \left( \frac{\partial u}{\partial t} + u \cdot \nabla u \right) = -\nabla p + \nabla \cdot \left( \mu \left( \nabla u + (\nabla u)^T \right) - \frac{2}{3} \mu \nabla \cdot u I \right) + F,$$

(3.28)

where $u$ is the fluid velocity, $\rho$ is the fluid pressure and $\nabla p$ represents the pressure forces, $\rho$ is the fluid density, $\mu$ is the fluid dynamic viscosity and $F$ represents the external forces applied to the fluid [59]. When the laminar flow is applied at the inlet boundary with a constant temperature and velocity, the Navier-Stokes equation will be transferred to:

$$L_{entr} \nabla_t \cdot \left[ -pI + \mu (\nabla_t \mu + (\nabla_t \mu)^T) \right] = -P_{entr} n,$$

(3.29)

where $n$ represents the point at the inlet boundary of the channel domain, $L_{entr}$ is the entrance length of the flow, which should be large enough to make sure that the flow is fully developed before entering to the channel. And $-pI$ is a pressure item, represents volumetric stress when $I$ defined as fluid intensity. In a single-phase fully developed laminar flow, the pressure gradient $\Delta P$ along the flow direction which is caused by the fluid friction is shown as:

$$\Delta P = \rho \cdot \frac{C}{Re} \cdot \frac{Lv^2}{2D_H},$$

(3.30)

where $\rho$ (kg/m$^3$) is the density of the liquid, $C$ is a constant with the value of 64 for a circular tube, $L$ (m) is the length of the channel, $v$ (m/s) is the flow velocity, $D_H$ (m) is the hydraulic diameter [60]. As the flow becomes very complicated when it turns to
a turbulent flow and the Navier-Stokes equation is very hard to solve by the simulation software, the condition with turbulent flow was not considered in this project.

3.2.3 Flow entrance length

Consider a fluid flowing through the channel, which is shown in Figure 3.5 with the whole process: When the flow enters into the channel, the velocities of every point along the vertical direction are the same. And the irrotational flow region is generated initially, where the flow viscous effects and velocity changes are negligible in this region. Along the flow through the channel, the fluid viscosity and the friction of the channel wall start to influence the flow mechanism. Within the entrance length of the developing flow \( L_{e} \), a boundary layer is formed and separates the uniform velocity core from the channel wall, and this boundary layer becomes wider with the fluid flow through the channel. After going through the entrance length, the boundary layer is disappeared and the flow changes to the fully developed flow, where the velocity of the flow remains constant [61]. For the laminar flow, the entrance length is estimated as

\[
L_{\text{entrance}} = 0.06R_{e} \cdot D_{H}. \tag{3.31}
\]

The convective heat transfer coefficient is constant with the fully developed flow, and it is independent of the flow velocity as

\[
h = \frac{N_{u}k_{f}}{D_{H}}, \tag{3.32}
\]

which can be observed from Table 3.2 and the \( N_{u} \) has the value of 3.66 for a constant wall temperature and 4.36 for uniform heat flux boundary condition. \( k_{f} \) (W/m-K) is the thermal conductivity of the fluid, and \( D_{H} \) (m) is the hydraulic diameter [62].
In calculation, different shapes of tubes or channels have to be taken into account. Here I want to introduce the hydraulic diameter and the hydraulic radius for further discussion of the flow in tubes and wind tunnels. The hydraulic radius \( R_h \) is given by:

\[
R_h = \frac{A}{P},
\]  

where \( A \) (m\(^2\)) is the cross section area of the flow, and \( P \) (m) is the wetted perimeter, a portion of the channel’s cross-section perimeter, which is wet.

If the hydraulic radius has a larger value, the channel can carry more volume of fluids to flow through. For the channel with a given width, a deeper channel has the larger hydraulic radius [63].

The formula of the hydraulic diameter is expressed as

\[
D_H = \frac{4A}{P}.
\]  

It is worth noting that Equation 3.34 is not twice of the hydraulic radius, but four times.

For a circular tube, the hydraulic diameter can be calculated with the equation

\[
D_H = \frac{4(\pi D^2/4)}{\pi D} = D.
\]  

Therefore the hydraulic diameter of a circular tube is simply equal to the diameter of the tube.

For a rectangular channel or tube, the hydraulic diameter is calculated as

\[
D_H = \frac{4h_c w_c}{2(h_c + w_c)},
\]  

where \( h_c \) (m) is the height, and \( w_c \) is the width of the channel [63].

Generally, the hydraulic diameter of the most types of the microchannels are simplified as the double of the channel width.

3.3 Thermal Resistance

Based on Ohm’s law, we can write an equation of the current as:

\[
I = \frac{V_1 - V_2}{R},
\]  

The thermal resistance is a key parameter when the cooling performance of the heat sinks is investigated. In order to distinguishing the thermal resistance with the electrical
resistance $R$, we use $R_\theta$ to represent the thermal resistance for general definition:

$$R_\theta = \frac{\Delta T}{\dot{Q}}, \quad (3.38)$$

where $\Delta T$ (K) is the temperature rise of the system with respect to the input coolant temperature (often room temperature), and $\dot{Q}$ (W) is the heat transfer rate.

For a heat conduction happens as shown in Figure 3.1, we can write down the magnitude of the conduction heat transfer rate:

$$\dot{Q}_{\text{cond}} = \frac{kA(T_1 - T_2)}{L}, \quad (3.39)$$

or

$$\dot{Q}_{\text{cond}} = \frac{T_1 - T_2}{L/kA}. \quad (3.40)$$

From Equation 3.40 and Equation 3.37 we can see that there are some similarities between them: (1) temperature difference and voltage difference play a same role to generate heat conduction and current flow, (2) conduction heat transfer rate is defined with the subtraction of the temperature from high temperature side to low temperature side of a layer, which similar to current flow generated from high voltage port to low voltage port of a resistor, (3) the term $L/kA$ in Equation 3.40 plays the similar role of $R$ in Equation 3.37. Based on these common points, we can obtain:

$$R_{\text{cond}} = \frac{L}{kA}, \quad (3.41)$$

which is defined as the conduction thermal resistance and is measured with the unit of $\degree\text{C}/\text{W}$ [34]. This shows that the conduction thermal resistance is proportional to the thickness of the conduction heat transfer layer, and inversely proportional to its surface area and thermal conductivity.

For convection heat transfer and radiation heat transfer, thermal resistance can also be defined in the same way. When we write the Newton’s law of the convection heat transfer rate mentioned in section 3.1.2 as:

$$\dot{Q}_{\text{conv}} = \frac{T_S - T_F}{1/hA_{\text{conv}}}, \quad (3.42)$$

we can obtain the convection thermal resistance:

$$R_{\text{conv}} = \frac{1}{hA_{\text{conv}}}. \quad (3.43)$$

This shows that convection thermal resistance is inversely proportional to the convection heat transfer coefficient and surface area exposed to the fluid [34].
With the definition of radiation heat transfer rate which was introduced in section 3.1.3 and based on the formula shown in Equation 3.16, we can transfer it to:

\[
\dot{Q}_{\text{Rad}} = \frac{T_s - T_{\text{surr}}}{1/h_{\text{rad}}A},
\]

where the radiation thermal resistance is defined as:

\[
R_{\text{rad}} = \frac{1}{h_{\text{rad}}A}.
\]

Note that the same principle as the electronic circuit can be considered when we build thermal resistance networks for parallel, serial and composite connections of the thermal resistance. It is convenient and efficient to use equivalent thermal resistance network to analyse thermal properties of heat transfer systems. One example in the literature [8] is that with a case of water flow through microchannels, the total thermal resistance \( R_{\text{tot}} \) in series connection can be expressed as the sum of three components:

\[
R_{\text{tot}} = R_{\text{cond}} + R_{\text{conv}} + R_{\text{heat}},
\]

where three components are included: (1) the conduction thermal resistance \( R_{\text{cond}} \), (2) the convection thermal resistance \( R_{\text{conv}} \) and (3) the heating thermal resistance \( R_{\text{heat}} \). \( R_{\text{cond}} \) is based on the heat transfer from the circuit to the substrate and the heat sink, \( R_{\text{conv}} \) is the heat transfer from the heat sink to the coolant, and \( R_{\text{heat}} \) shows how much heat is absorbed by the coolant fluid. In general the \( R_{\text{cond}} \) is very small as the heat sink is located very closely to the heat source, and for silicon substrate, with a high thermal conductivity of \( k_{\text{si}} = 1.48 \text{ W/°C-cm} \) at 27 °C, this is negligible [64]. The \( R_{\text{heat}} \) is considered to be very small by using the coolant with a high volumetric heat capacity. For example, water has the heat capacity of 4.18 \text{ J/°C}. Followed by this consideration, the only component we should focus on is the convection thermal resistance \( R_{\text{conv}} \) for designing heat sinks with better cooling performance.

Based on the consideration of the fluid dynamics described in the previous section, the key component of the thermal resistance due to the convection mechanism, \( R_{\text{conv}} \) can be calculated theoretically for the specific designed structures.

According to the literature [20], the total thermal resistance is expressed as

\[
R_{\text{tot}} = R_{\text{heat}} + R_{\text{conv}} = \frac{1}{\dot{m}C_p} + \frac{1}{h(A_b + \eta A_{\text{fin}})},
\]

where \( \dot{m} \) (kg/s) is the mass flow rate, \( C_p \) (J/K) is the specific heat, \( h \) (W/m²·K) is the heat transfer coefficient, \( A_b \) (m²) is the heat sink base area, \( A_{\text{fin}} \) (m²) is the surface area of the heat sink fins, and \( \eta \) is the fin efficiency. From Equation 3.47 the surface areas including base area and fin’s surface area are important parameters for the thermal resistance calculation.
Some general equations to estimate the convection thermal resistance of the heat sinks are listed below [14]:

\[
R_{hs} = \frac{1}{h(A_{\text{base}} + N_{fin}\eta_{fin}A_{fin})},
\]

(3.48)

\[
\eta_{fin} = \frac{\tanh(m \cdot H_{f})}{m \cdot H_{f}},
\]

(3.49)

\[
m = \sqrt{\frac{2 \cdot h}{k_{fin} \cdot t_{fin}}},
\]

(3.50)

\[
h = N_{u} \frac{k_{\text{fluid}}}{b},
\]

(3.51)

where \(R_{hs} \degreeCelsius/W\) is the thermal resistance of heat sink.

From these equations we can see that the key thing to calculate the thermal resistance is the Nusselt number, shown in Table 3.2, which depends on different situations. The other equations are used to calculate the equations for the Nusselt number and the convection thermal resistance, and some of the parameters’ value like \(k_{fin}, k_{\text{fluid}}\) and \(Pr\) can be inquired with specific material.

### 3.4 Raman Thermometry

Since time resolved transient Raman spectroscopy was used to characterize the heat transfer properties in this project, basic knowledge of Raman spectroscopy together with one it’s most significant applications, Raman thermometry, will be introduced in this section.

![Basic Raman Spectroscopy layout](image)

**Figure 3.6: Basic Raman Spectroscopy layout**

Raman spectroscopy is a spectroscopic technique which is most commonly used to determine vibrational modes of molecules, through characterizing the chemical bonding and
solid state structure of materials [65]. The first Raman experiments were carried out by Sir C.V.Raman using focussed sunlight and filters to observe the visual color change from scattered light in 1928 [66]. Modern Raman spectroscopy always employ lasers as the excitation light source. Figure 3.6 shows a typical Raman spectroscopy layout, together with the Notch filter for laser rejection and charge-coupled devices (CCDs) for detection. When a sample is illuminated with a monochromatic light, an interaction will occur between the incident photons and the sample material, this phenomena is called scattering which can be differentiated into two types, elastic and inelastic. Most of the photons are scattered elastically this is know as Rayleigh scattering, however some of the photons interact with the lattice producing a phonon within the material, an inelastic process by nature. This inelastic process is the key principle behind Raman spectroscopy, therefore this type of scattering was named Raman scattering. Figure 3.7 shows a schematic of photons scattering within a material producing the two scattering types.

![Figure 3.7: A schematic diagram of scattering phenomena from incident monochromatic light.](image)

During the Raman scattering, the lattice vibrates releasing a phonon due to the photons from the incident monochromatic light source, this results in the scattered photon shifting to a different energy state, in the form of a change in frequency. If the final energy state of the phonon is higher than the initial state, the scattered photon will shifts to a lower frequency as the total energy of the system must be kept constant. This frequency shift is called Stokes Raman scattering, and if the final energy state is lower than the initial state, the scattered photon will be shifted to a higher frequency, and is known as Anti-Stokes Raman scattering. According to the quantum theory, the energy of a photon is written as [67]:

$$E_p = hv, \quad (3.52)$$

where $E$ (eV) is the energy, $h$ (Js) is the Planck’s constant, which equals to $6.626 \times 10^{-34}$, and $v$ is the frequency of the photon. When the frequency of the phonon is assumed as $v_0$, the measured Raman spectrum is shown in Figure 3.8. Normally the Stokes line has higher output intensity than Anti-Stokes line, so the characterization in Raman spectroscopy is usually based on the Stokes line.
In the field of optical spectroscopy, Raman shift is represented as wavenumber (cm$^{-1}$), which is the spatial frequency of a wave, defined as the number of wavelengths per unit distance. According to Hooke’s law, lattices vibration can be treated as a harmonic oscillator when the temperature of semiconductor material begins to increase due to a laser or external heater. The band length then increases which causes a decrease of the spring constant. The relationship between the phonon frequency and the spring constant is [68]:

\[ v_0 = \frac{1}{2\pi} \sqrt{\frac{k}{m}}, \tag{3.53} \]

where \( m \) is mass and \( k \) is spring constant. As increasing or decreasing of the spring constant causes a change in phonon frequency, this results in a shift of the Raman spectrum peak position. This is the reason why Raman spectroscopy can be used in thermometry to determine the temperature of a material, especially for a semiconductor material such as silicon [65].
Chapter 4

Simulation of Surface-Modified Silicon Heat Sinks

With declaration of the objective and motivation of this project, a series of estimation works have been done to verify the feasibility of the surface modified heat sinks. Two main parts are included in this chapter: one is estimation of the thermal resistance of surface modified heat sinks, and another is Finite Element Analysis by using COMSOL Multiphysics where fluid dynamics and heat transfer are able to be taken into account simultaneously. The equations applied for the simulations were mentioned in Chapter 3. Considering computer resource issues, the simulations for fabricated heat sinks are simplified to one of the single chip with micro fin and pin fin structures on their surface, and all of these simulations are run on the University supercomputer, iridis4. The simulation focuses on the 2×2 cm² silicon chips with different micro structures on one side of the surface. There are three sets of physics calculation modules in this simulation, which are Heat transfer in solids, Heat transfer in fluids and Laminar flow. All of the simulations in this section are under the assumption of the laminar flow, single phase flow, incompressible and continuum fluid, steady state condition, and no slip condition for the wind tunnel walls. The boundary conditions used with the Heat transfer in solids module are same as the Heat transfer in fluids module, which are named as: (1) Initial values, (2) Thermal insulation, (3) Heat source and (4) Out flow in the simulation software. The Initial values assumed the module is operated in a constant ambient temperature. The thermal insulation condition is represented as

\[- n \cdot q = 0, \tag{4.1}\]

which is applied for the wind tunnel boundary except the inlet and outlet part. It indicates that no heat transfer at the outlet boundary of the wind tunnel. The heat source condition is assumed with overall heat transfer rate and the out flow boundary
The boundary conditions used under the Laminar Flow module are (1) initial values, (2) wall, (3) inlet, (4) outlet. The initial values in this physical module is assumed with zero pressure drop as the wind tunnel is under vacuum condition initially. The wall condition is applied to the wind tunnel boundary with no slip condition, except the inlet and outlet part. The inlet boundary is applied with laminar flow, constant inlet temperature and average velocity. The outlet boundary is applied to the outlet of the wind channel, which is used to make sure no fluid from the outlet can flow back to the channel. The values set up to some of the boundaries are listed in Table 4.1.

4.1 Estimation of the thermal resistance of the whole heat sink

Figure 4.1: Calculated thermal resistance in the air flow for micro-fin heat sinks with a different number of grooves on the fins.
In order to evaluate effects of surface modification on the cooling performance of the
heat sink, first we have used analytical formulas for fin-type heat sinks to calculate
the thermal resistance, $R_{hs}$, which are defined in Section 3.3 with equations of 3.48,
3.49, 3.50, 3.51 and the equations of the Nusselt number in Table 3.2. Four heat sink
structures with various total numbers of grooves ($N_g$) on the surface of the fin have been
investigated. The overall size of the heat sinks are approx. $1 \times 1 \times 1 \text{ cm}^3$. For simplicity,
the average fin thickness, $t_{ave}$, and average distance between fins, $b_{ave}$, schematically
shown in Figure 4.1 are used for calculation of the surface-modified structures. Key
parameters varied are summarized in Table 4.2. With increasing the surface area $A_{fin}$,
the thermal resistance decreases, indicating cooling performance is improved with active
surface modification.

Table 4.2: Key parameters used for calculation based on the analytical formula
from section 3.3.

<table>
<thead>
<tr>
<th>$N_g$</th>
<th>$A_{fin} (cm^2)$</th>
<th>$t_{ave} (mm)$</th>
<th>$b_{ave} (mm)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>11.1</td>
<td>1.0</td>
</tr>
<tr>
<td>B</td>
<td>24</td>
<td>12.1</td>
<td>0.7</td>
</tr>
<tr>
<td>C</td>
<td>36</td>
<td>13.1</td>
<td>0.78</td>
</tr>
<tr>
<td>D</td>
<td>60</td>
<td>15.1</td>
<td>0.74</td>
</tr>
</tbody>
</table>

Figure 4.2: Simulation results of surface temperature distribution with 3 m/s
inlet air flow velocity for the heat sink with flat fins ((a) and (b)), with 36 grooves
((C) and (d)), and with 60 grooves ((e) and (f)). The maximum temperature
happens at the position where the heater placed.
Chapter 4 Simulation of Surface-Modified Silicon Heat Sinks

Figure 4.3: Total thermal resistance extracted from simulation results as a function of the surface area for various flow conditions: (a) absolute value and (b) normalized value of the total thermal resistance. The natural cooling is simulated with the heater power of 0.2 W and others are of 10 W.

To confirm this aspect, simulations with COMSOL Multiphysics software are taken into account. Figure 4.2 shows simulation results of the 3D temperature distribution under air flow and the detailed 2D distribution as a cross section for the structure A with flat fins (Fig. 4.2 (a) and (b)), B with 24 grooves (Fig. 4.2 (c) and (d)), and D with 60 grooves (Fig. 4.2 (e) and (f)). Here the equations in section 3.1.4 are used to calculate this simulation result. The heater power $Q$ is 10 W, the inlet flow rate $v_{in}$ is 3 m/s, and the inlet fluid temperature $T_{in}$ is 20 °C. Note that the maximum temperature $T_{max}$, a key indicator of cooling performance decreases from A to B but increases from B to D. The total thermal resistance $R_{tot}$ is estimated as

$$R_{tot} = (T_{max} - T_{in})/Q,$$  \hspace{1cm} (4.2)

from the simulation results.

In order to view more intuitively from the simulation results, the relationship between the fin area and heat sink thermal resistance are drawn corresponding to various flow conditions. Figure 4.3 shows how the $R_{tot}$ is changed with increasing the surface area $A_{fin}$ for various inlet flow rates. While there is less change under the very low flow rate (natural cooling), $R_{tot}$ decreases first and then increases under the air flow with the flow rate of 1-3 m/s. Note that the lowest $R_{tot}$ is observed for the structure with the larger $A_{fin}$ under the higher flow rate in this range. The results suggest that there is an optimum $A_{fin}$ depending on the air flow rate. For the flow rate of 3 m/s, minimum
\( R_{\text{tot}} \) of 9.02 °C/W is obtained at \( A_{\text{fin}} \) of 13.1 cm\(^2\). With normalized thermal resistance curve shown in Figure 4.3 (b), the most sensitively change happens to the inlet flow rate of 1 m/s, which indicates that within the fin surface area range from 10 cm\(^2\) to 16 cm\(^2\), creeping flow with lower velocity is enough to cool down the heat sink. The discrepancy between the theoretical calculations and simulations might be due to lack of consideration of conduction heat transfer in analytical calculation.

### 4.2 Simulation of the fabricated silicon chips with micro structures

In the last section, effects of surface modification have been investigated for the heat sinks which have relatively larger modification structures on the surface of the fins. The simulation results suggest that the effect of the heat conduction in the heat sink cannot be ignored under this laminar flow condition as well as the heat convection at the surface between the surface of the heat sinks and fluid. In the following, microscale surface modification is studied in detail.

#### 4.2.1 Simulation of micro structures with different heights

![Simulation structure of the silicon chip with (a) flat surface, (b) micro fin structure and (c) micro pin fin structure, together with the wind tunnel and heater.](image)

Figure 4.4: Simulation structure of the silicon chip with (a) flat surface, (b) micro fin structure and (c) micro pin fin structure, together with the wind tunnel and heater.

After reviewing the previous fabrication methods for high aspect ratio structures in Chapter 2, DRIE dry etching process has been selected as the silicon surface modification method for the fabrication work of this project. In order to investigate effects of the heat conduction one the heat sinks designed for fabrication, with consideration of computer resource issues, simulations in this section are for a silicon chip with micro-structures on the surface of a silicon wafer. Various microstructures have been designed and the maximum temperatures of the different geometries have been compared with respect to the change of the height of the micro fins and pin fins. Figure 4.4 shows the configuration of simulated models with (a) a flat silicon chip, (b) micro-fin-structured silicon chip and (c) micro-pin-fin-structured silicon chip, respectively. These structures are all supposed
Figure 4.5: Silicon chip with flat surface under the heater power of 3 W and the flow rate of 3 m/s. (a) simulation result of the temperature map and (b) sample structure with heater at the bottom.

to be the same as the silicon chips to be fabricated. The fabrication details will be shown in the later chapter. The thickness of the silicon chip used in the simulation is 650 µm, which is identical to the regular 6-inch wafer. Practically, due to the nature of the etching process, the etching depth of the bonding areas placed in the four corners of the chip and that of the main micro structures would be different. However for simplify, this depth of the bonding area at four corners are fixed to 200 µm for all the simulations.

The wind tunnel is defined on the top of a silicon chip and the heater is placed at the bottom of the chip which is located out of the wind tunnel. The material of the heater is copper with the thermal conductivity of 400 W/m·K.

First, the silicon chip with the flat surface (Figure 4.4 (a)) is simulated and the result is shown in Figure 4.5. The size of the outside wind tunnel is 2.1 cm in width, 2.1 cm in length and 0.1 cm in height, respectively. The dimensions of the heater is 2×2×0.06 cm³. The highest temperature of 76.2 °C is obtained in this simulation and it happens on the surface of the heater. The diagram at the bottom is the cross sectional view along the horizontal line in the middle of the structure.

Table 4.3: Dimensional parameters of micro-fin and micro pin-fin structures used for the simulation of maximum temperature calculations. Symbols in the table are defined in Figure 4.4.

<table>
<thead>
<tr>
<th></th>
<th>$h_{fin}$, $h_{pinfin}$ (µm)</th>
<th>$w_{fin}$, $w_{pinfin}$ (µm)</th>
<th>$g_{fin}$, $g_{pinfin}$ (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>50</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>(b)</td>
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<td>100</td>
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<tr>
<td>(c)</td>
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<tr>
<td>(d)</td>
<td>200</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>
Chapter 4 Simulation of Surface-Modified Silicon Heat Sinks

Figure 4.6: Simulation results of the silicon chips with micro fin structures, and the fin height are (a) 50 µm, (b) 100 µm, (c) 150 µm and (d) 200 µm.

Figure 4.7: Simulation result of the surface maximum temperatures with respect to the height of the fins for the micro fin structures.

The simulations with micro-fin and micro pin-fin structures have been done for the designs with different heights. The dimensional parameters specified in Figure 4.4 (b) and (c) are listed in Table 4.3. First, the simulation results of the silicon chip with micro fin structures are shown in Figure 4.6. The simulations have been conducted under the same conditions of the heater power of 3 W and the fluid flow rate of 3 m/s. Calculated
Figure 4.8: Simulation results of the silicon chips with micro pin fin structures, and the height of the pin fins are (a) 50 µm, (b) 100 µm, (c) 150 µm and (d) 200 µm.

maximum temperatures are also shown in Figure 4.6.

Figure 4.9: Simulation result of the surface maximum temperatures with respect to the height of the pin fins for the micro pin fin structures.

In order to compare the simulation results of the micro fin structures, the maximum temperatures of the surface are plotted in Figure 4.7 with respect to the change of the fin height. The result of the flat surface silicon chip is also plotted at the height of 0
Figure 4.10: Comparison of the simulation results of the micro fin and pin fin structures.

µm. This figure shows that with changing the micro fin height, the surface maximum temperature decreases first towards the height of 50 µm, and then increases under the same air flow rate of 3 m/s. This behaviour is very similar to what was calculated for rather larger surface structures that mentioned in section 4.1. The lowest $T_{\text{max}}$ is observed for the fin height with 50 µm, and the temperature has a slight change for the height range of from 50 to 150 µm, suggesting that there is an optimum height for the lowest $T_{\text{max}}$ in this range. In order to confirm this aspect, a series of simulations have been performed for micro pin fin structures under the same simulation conditions. The results are shown in Figure 4.8. To compare the results of micro pin-fins with that of the flat surface silicon chip again, the calculated $T_{\text{max}}$ of the micro pin fin structures is plotted with the change of the height of the micro pin-fins in Figure 4.9. Similar to the case of micro fins, the $T_{\text{max}}$ decreases first and then increases back to the higher value with the larger pin fin height. The lowest $T_{\text{max}}$ of 71.1 °C is observed at the pin fin height of 150 µm.

In comparison of the simulation results between the micro fin and pin fin structures with respect to the different height, in Figure 4.10, two curves of the change of $T_{\text{max}}$ in Figure 4.7 and Figure 4.9 are plotted together. Tendency of the $T_{\text{max}}$ is similar for these two micro structures, and the lowest temperature appear in the same height range, which are between 50 to 150 µm. One the other hand, the optimum height is different between each other, 50 µm with the temperature of 71.6 °C for the micro fin structure and 150 µm with the temperature of 71.7 °C for the micro pin fin structure. In addition, the
point with 100 µm micro structure height gives the similar temperature values within the "best option" range. This set of simulations suggest that, under the laminar air flow with the velocity of 3 m/s, the cooling performance of the micro fin structures are better than the micro pin fin structures when the height of the micro structure are below 100 µm, while the micro pin fin structures are better when the heights are among the range of 100 µm to 150 µm.

4.3 Simulation of the micro structures with same volume

![Configuration diagram of the micro fin structure with the volume of 14.7 mm³ (a) and simulation result (b).](image)

As discussed before, the objective of this project is to use silicon micro fabrication technology to increase the surface area of the heat sinks to improve the heat sink cooling performance. However, according to the simulation results obtained so far, the cooling performance is not maintained to increase in increasing the surface area of the heat sink. The maximum surface temperature decreases first and then increases back to higher values when the height of the micro structures increases further, no matter which structure of micro fin or micro pin-fin is chosen. This is considered due to decrease of the conduction heat transfer corresponding to the removal of silicon materials for the micro patterns with the etching depth of deeper than 150 µm and beyond in this case. In other words, if too much silicon material is removed by etching, effects of loss of the conduction heat transfer is much larger than gain of the convection heat transfer. Therefore, in this section, simulations will focus on comparing the microstructure patterns where the total volume of the overall fin/pin-fin structures are maintained the same in order to minimize the change of heat conduction and then to extract effects of increase of the heat sink surface area on their cooling performance.

For a 2 cm² silicon chip with an array of a micro pin-fin with the size of 1200×100×200 µm³ and 2100×100×200 µm³, the total volume of the micro pin fins is calculated 14.7 mm³. Therefore, for comparison, an array of micro fins designed has the same top
surface area as the referred micro pin-fin structure has, while the depth are maintained the same of 200 $\mu$m. Figure 4.11 shows the schematic diagram of the designed micro fin structure with the total top surface area of 73.37 $mm^2$, corresponding to the total volume of 14.7 $mm^3$.

Figure 4.11: Schematic diagram of the designed micro fin structure.

Figure 4.12 compares the simulation results of two structures, which are (a) a micro fin structure with volume of 14.7 $mm^3$ and (b) a micro pin fin structure with volume of 14.7 $mm^3$. Note that the simulation conditions are kept consistent as usual, and the only difference is the variation of the fin length, which has marked in Figure 4.11. While keeping the volume of the micro structures the same, the total surface area increases from (a) 390.98 $mm^2$ to (b) 657.09 $mm^2$. From the simulation results, that maximum surface temperature reduced from 76.8 $^\circ C$ in (a) to 75.7 $^\circ C$ in (b), suggesting the cooling performance has been improved when the surface area is increased under this condition.

**Figure 4.12: Simulation results of (a) micro fin structure with volume of 14.7 $mm^3$, (b) micro pin fin structure with volume of 14.7 $mm^3$.**

### 4.4 Summary

In this chapter, first I have focused on the whole heat sink structures close to the commercial ones and then moved to analyze individual, silicon chips with micro fin and pin fin structures on their surface. The designed micro structures are based on the fabrication feasibility via silicon technology. Based on the definition of the thermal resistance and basic equations for analytical calculation that have been introduced in Chapter 3, the thermal resistance of the whole heat sinks have been estimated. The results show that with increasing the surface area of the heat sinks, the thermal resistance always decreases as long as the convection heat transfer mechanism is concerned. Then FEM simulation software COMSOL Multiphysics has been introduced to verify this aspect, and the results show that with increasing the heat sink surface area, the cooling
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performance is improved first but then becomes worse with continuing to increase the surface area. The discrepancy between the theoretical calculation and the simulations is considered by lack of consideration of conduction heat transfer due to the removal of the material of the surface of the heat sinks to obtain larger surface area. To confirm this aspect for micro structures, the individual silicon chips with micro fin and pin fin structures with different heights have been designed and the heat transfer has been simulated under identical conditions of the flow rate, wind tunnel structure and heater power. The similar results have been observed to the simulation results for the whole heat sinks and different optimum height of the structure have been identified between the micro fin and micro pin fin simulation results. It is notable, however, that the range of from 50 $\mu$m to 150 $\mu$m, where $T_{max}$ shows the relatively lower values are similar in both the structures. These results suggest that under the laminar air flow condition, the removal of the material influences the conduction heat transfer, and with excess removal, the domination of the convection heat transfer will be lost and heat conduction will start to play a dominant role. In order to prove this aspect, another set of simulations have been conducted for the individual silicon chips with an array of micro pin fins or micro fins. For this set, the whole volume of the array is kept the same for both the structures to minimize the difference of the heat conduction. The result shows that when keep the volume of the structure the same, the increase of the total surface area can improve the heat sink cooling performance. The aspects that have been verified with this series of simulations will be useful for designing surface modification patterns on heat sinks.

Here I want to suggest some limitations about the COMSOL Multiphysics software during the process of using:

1. Mesh building is an important procedure before going to simulate, while the software provides two options which are Physics-controlled mesh and User-controlled mesh to be put to use, the User-controlled mesh is hard to build when the geometry becomes a little bit tiny and complicate (for example multiple micro-scale structures), and this usually causes calculation errors during the simulation. Although Physics-controlled mesh is much easier to use, simulation results can make a big difference when employing two different types of element size (for example Normal and Coarse mesh), accuracy of the simulation is hard to identify.

2. Resource requirement. With simulating of the micro fin structure which mentioned in section 4.2, it takes almost 2 hours by using the local computer even only one silicon chip and one-side structure are considered. Although university supercomputer Iridis was employed to save time, sample chip with 100 $\mu$m$^2$ pin-fin structure requires 5 to 6 hours to finish the simulation. Huge memory resources will be required for the simulation if the structure size scaling down to 10 $\mu$m$^2$ or nano meters.

3. Geometry build within COMSOL. COMSOL Multiphysics software has powerful function to simulate the finite element model with either single or multiple physics field.
But the CAD geometry building function is less than satisfactory. With simple and large features, geometry drawing is easy to handle by using the software. For complicated and tiny features, geometry building function becomes awkward and hard to control. For the geometries simulated in this project, I prefer to draw the geometries by using the SOLIDWorks software first, and then import into COMSOL to simulate.
Chapter 5

Fabrication of Surface-Modified Silicon Heat Sinks

There are many methods to modify the silicon surface structure in micro and nano fabrication technology. Surface patterning by photo-lithography and growth of nanostructures like carbon nano tubes on the silicon surface are the two common methods. Surface patterning technology by using photo-lithography mask is the method used in this project. According to the simulation results and the definition of the heat sink thermal resistance, the heat sink surface area is a key parameter which could improve the cooling performance, and this also provides an opportunity to collaborate with silicon micro fabrication technology to increase the surface area. To achieve this objective, the main fabrication work of this project is to develop a novel fabrication process in wafer level with double side micro structures etching technology. In addition, bonding technology for stacking the double side etched chips together to generate the 3D silicon surface modified heat sink has been also explored as a chip-level process after dicing the wafers. For micro fin and pin fin structures, dry etching with DRIE (Deep Reactive-Ion Etching) technology has been chosen. Although the DRIE technology has many advantages to achieve vertical and deep trenches, the significant disadvantage is generation of surface roughness on the silicon surface. Wet etching with chemical solution has been also considered to reduce the surface roughness of the dry-etched chips for bonding procedure.

5.1 Fabrication overview

Double-side-polished 6-inch wafers with crystal orientation <100> and p-type doping are chosen for the fabrication. The wafer thickness is 725 ± 25 µm and the resistivity is 1-10 Ω·cm. Figure 5.1 shows a schematic diagram of a rough fabrication idea for the stacked double-side-etched all silicon heat sink. Three different types of heat sinks with
different surface structures are designed: (1) flat surface with no structures, (2) micro fin surface structures and (3) micro pin fin surface structures. The etched surface-modified whole wafer is cut into pieces. The spacers for bonding to build the whole heat sink structures are also designed in the spare spaced in the wafer and cut into the pieces together with the surface-modified pieces. The pieces with micro structures on both the front and back surfaces are bonded with spacers as shown in Figure 5.1 together to generate the whole heat sink with surface modification. Note that the bonding areas are located at the four corners and the etched depth are almost same as the micro structures’ depth, because they were etched together at the same time. The size of the bonding areas are 5 mm and 2 mm for 2 cm$^2$ chips and 1 cm$^2$ chips, respectively. Two different types of bonding spacers were designed for bonding process. Type1 spacer is designed for the flat bonding areas with normal flat surface. Type2 spacer is designed for the bonding area which has a groove etched down at the center, where the extrude pin head on the spacer can embedding in. The size of the etched square hole and pin head of the 1 cm$^2$ chips are 500 $\mu$m$^2$ and 400 $\mu$m$^2$, respectively. For 2 cm$^2$ chips, the size of the hole and the pin head are 1250 $\mu$m$^2$ and 1000 $\mu$m$^2$, respectively.

![Diagram of fabrication process](image)

Figure 5.1: Overview of the fabrication idea with double side polished wafer

Figure 5.2 shows the wafer level layout of different types of structures. The layout is symmetric between the left- and right-hand sides with respect to the axis from top to bottom across the centre to make sure this is applicable for patterning of both the sides. This layout is used for the mask for photo-lithography process. In the layout, two different sizes of pieces are designed as marked in the figure: one set of the pieces with the area of 2 × 2 cm$^2$ and another of 1 × 1 cm$^2$. Two different design of the bonding areas are included. As shown in the figure, most pieces are with flat bonding area at the four corners, which can accept the type1 bonding spacer shown in Figure 5.1. Some
of the pieces have specific design in the bonding areas, which can be fit with the type2 bonding spacer. There are totally five different types of structures designed in a single whole wafer, which are labelled as: (1) 10 µm pin fins, (2) 100 µm pin fins, (3) 10 µm fins, (4) 100 µm fins and (5) flat surface one.

Table 5.1 lists the dimensions of the different structures for more details. The micro pin fin structures are patterned as an assembly of the squares with the same width and length and the gaps between them in both horizontal and vertical directions are also the same. The length of the micro fin patterns are designed in the following manner: for 1 × 1 cm\(^2\) chips the fins' length are same as the chip size, which are 10000 µm. But for 2 × 2 cm\(^2\) chips, the fins were not patterned continually but divided into several sections, which has the length of 2900 µm each and the gaps between two divided fins are same as the width of the fins. The actual structure will be presented later with the optical microscope images.

### 5.2 Fabrication of double side micro fin and pin fin structures

The schematic diagram of the fabrication process is shown in Figure 5.3. In order to depositing silicon dioxide on the both side of the wafers at one time, LPCVD (Low Pressure Chemical Vapor Deposition) technology was employed in the furnace tube under 1000 °C. For the target SiO\(_2\) thickness of 1 µm, the thermal deposition process time was set up to 6 hours and 25 minutes. The thickness was measured by ellipsometer. Figure 5.4 shows the thickness distribution of the SiO\(_2\) on both sides of a wafer after the LPCVD process. From the figure the SiO\(_2\) thickness at the top left and right edges is thinner on side1 and side2, respectively, and thicker part is at the bottom. The thickness differences within the main area except for the notch and edges are less than 10 nm, which was considered as a good uniformity. A photo resist AZ9260 was coated on one side first with the thickness of 7 µm and baking time was 2 minutes at 110 °C. Photolithography was done with the exposure time of 10 seconds after that. Then the mixed solution (AZ400K:water=1:3) was employed for 3-minute development process.
The ICP (inductively coupled plasma) etching process was done for SiO$_2$ to be used as a hard mask. The main reactive gases are: CHF$_3$, C$_4$F$_8$, O$_2$ and He flow. Figure 5.5 shows the ellipsometer measurement results of the dummy wafer which was used for an ICP etching test. The etching rate was observed around 250 nm/min for silicon dioxide, so the etching time for the ICP process was set to 6 minutes by considering 50% over etching of the 1 $\mu$m SiO$_2$ layer. Note that the resist was still remained and the thickness of the resist was reduced to 4 $\mu$m after the ICP process. An optical microscope image of the micro pin fin structure after SiO$_2$ etching is shown in Figure 5.6. The image shows the structure of 100 $\mu$m pin fins with the designed width and length of 100 $\mu$m, shown in Table 5.1. The discrepancy between the measured dimensions and the designed dimensions may come from the fluctuation of the photolithography processes or over etching by ICP process.

Deep reactive ion etching (DRIE) was chosen for the silicon etching after the ICP process, which has the advantages of high etching rate and high selectivity. Ideally the selectivity of the etching can reach to 1:200 for SiO$_2$:Si with the fast speed etching recipe, but it also depends on the recipes and the state of the machine. Note that the photo resist was removed before going to the DRIE process. The etching rate was tested first with the dummy wafer before doing the main process. Figure 5.7 shows the step profiles of a test pattern on the dummy wafer after (a) one minute and (b) two minutes etching. The position of the probe of the profile was located to the bottom of the pattern initially, and then the probe was made move to the top of the pattern. The step that the probe passed
through is the height difference between the bottom and top of the pattern. Figure 5.8 shows a schematic diagram of this procedure in detail. The "St height" shown in the diagram is the height from the bottom to the top of the pattern, which corresponds to the measurement result in the Figure 5.7. Because the thickness of the silicon dioxide layer is also included in the measurement result, the actual etching depth can be obtained by subtracting the SiO$_2$ thickness remained on the top of the pattern. After measuring the thickness of the silicon dioxide layer with the ellipsometer, the etching rate can be
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Figure 5.5: Ellipsometer results of the SiO$_2$ thickness distribution after ICP test with (a) 1 minute and (b) another 1 minute after that.

Figure 5.6: Optical microscope image of the 100 $\mu$m pin fin structure after ICP SiO$_2$ etching.

estimated as $\sim$4 $\mu$m/min and $\sim$25 nm/min for silicon and silicon dioxide, respectively. From this result, we can estimate the selectivity of 1:160 for SiO$_2$:Si.

The etching rate is varied with the size of the structures. In general, etching of larger structures (eg. with 100 $\mu$m gaps) is much faster than that of the smaller structures (eg. with 10 $\mu$m gaps), so the process time needs to be estimated based on the structure which has faster etching rate, to be sure that the silicon structures under the silicon dioxide layer are not etched. After all, the etching time was setting up to 40 minutes for the DRIE machine. The etching was processed for one side first and then for another side. Figure 5.9 shows photo of both the sides of an etched wafer. Note that the Type2 bonding spacers are located around the wafer edge and the smaller Type2 bonding spacers for 1 cm$^2$ chips are located at the bottom part of the layout. The distribution of different structures can be identified by comparing with the wafer layout shown in Figure 5.2.
Figure 5.7: Step profile results of the Si etching depth after DRIE test with (a) 1 minute and (b) another 1 minute after that.

Figure 5.8: Schematic diagram of the step profile process for the DRIE silicon etching.

After the etching process, the structures were checked under optical microscope. There was still around 150-nm-thick SiO$_2$ remained on the top of the patterns. Figure 5.10 shows the optical images of the $10 \times 10 \mu m^2$ pin fin structures formed on a chip with the size of $1 \times 1 \, \text{cm}^2$ under 10x magnification (a) and that of $2 \times 2 \, \text{cm}^2$ under 20x magnification (b). From the figures we can see the dark area at the bottom of the structures. For the pattern with 10 $\mu$m gaps, the SF$_6$ ions in the plasma cannot reach to the bottom area thoroughly, and this mechanism is more significant with further etching. As a result, the etching can generate a rough bottom surface that corresponds to the dark region. The details about this will be discussed later with SEM images. Figure 5.11 shows optical microscope images of the micro fin structures on a $1 \times 1 \, \text{cm}^2$ chip under the 10x magnification microscope. Figure 5.11 (a) shows the fin structure with 100 $\mu$m in width and 1 cm in length and Figure 5.11 (b) gives the one with 10 $\mu$m in width.
Figure 5.9: Pictures of the wafer level view for the DRIE silicon etching result with (a) side 1 and (b) side 2 after 40 minutes.

Figure 5.10: Optical microscope images of 10 $\mu m^2$ pin fins with the chips size of (a) 1 cm$^2$ under 10x magnification and (b) 2 cm$^2$ under 20x magnification.

and 100 $\mu m$ in length. The micro fin structures on $2 \times 2$ cm$^2$ chip are shown in Figure 5.12. The width of the fin is designed the same as the fin structures on a $1 \times 1$ cm$^2$ chip, but the length of 2900 $\mu m$ is different. A much clearer view of the structure with 10x magnification is shown in Figure 5.12 (b). Basically, the design of the fin structures was based on the aspect ratio for fin’s width and length. The aspect ratio of the length to width is equal to 100 for 1 times 1 cm$^2$ chip with the fin width of 100 $\mu m$, which is acceptable. But for the fin width of 10 $\mu m$, if the fin length was designed as the same as the chip’s length, the aspect ratio is increased 10 times larger. Practically such the structure cannot survive during the etching process. So the fins was designed to be cut into sections, as shown in Figure 5.11 (b) and Figure 5.12.

Figure 5.13 shows the optical microscope images of the 100 $\times$ 100 $\mu m^2$ pin fin structures under 10x magnification, with the chip size of (a) $1 \times 1$ cm$^2$ and (b) $2 \times 2$ cm$^2$. Compared with the smaller pin fin structures shown in Figure 5.10, the bottom area can be observed much more brightly than that. While some of the optical microscope
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Figure 5.11: Optical micro scope images of the micro fin structures on 1 cm$^2$ chip with (a) 100 $\mu$m width, 1 cm length and (b) 10 $\mu$m width, 100 $\mu$m length.

Figure 5.12: Optical micro scope images of fin structures on 2 cm$^2$ chip with 100 $\mu$m width and 2900 $\mu$m length under (a) 5x magnification and (b) 10x magnification.

images are listed for each structure, more details about the actual dimensions of different types of structures are summarized in Table 5.2. Compared with the dimensions of the structures on 1 $\times$ 1 cm$^2$ chips, the structures on 2 $\times$ 2 cm$^2$ chips have smaller W and L and larger g, suggesting the structures have been etched further. Refer to the wafer level layout of the structures, we can see that all of the 1 $\times$ 1 cm$^2$ chips are placed at the edge of the wafer. In this case, the etching rate could be a little bit slower than that for the 2 $\times$ 2 cm$^2$ chips which are located at the center of the wafer. For the same structures on the same chips with the same size, the structures with larger designed gaps have been etched more. Furthermore, the fin structures are found to have smaller W and L and larger g when compared with the corresponding pin fin structures.
Figure 5.13: Optical micro scope images of $100 \times 100 \mu m^2$ pin fins on the chips with the size of (a) $1 \times 1 \text{cm}^2$ and (b) $2 \times 2 \text{cm}^2$.

Table 5.2: Table of the actual dimensions for the different structures after silicon etching.

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<th>Chip size ($\text{cm}^2$)</th>
<th>Structures</th>
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<th>Length (L, $\mu m$)</th>
<th>Gap (g, $\mu m$)</th>
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<td>4</td>
</tr>
</tbody>
</table>

5.2.1 SEM images and etching results discussion

In order to investigate the etching rate for different structures and to optimize the recipe for silicon etching, SEM (Scanning Electron Microscope) images of the fabricated structures after etching were taken for the diced pieces. For the silicon etching machine, called as Plasmatherm Versaline DRIE, there are three regular recipes that can be chosen for relevant processes. The recipes are named as "Slow Etching Speed", "Medium Etching Speed" and "Fast Etching Speed". The details of the parameters in each recipe are shown in Figure 5.14, Figure 5.15 and Figure 5.16. From these figures we can see that the main differences that affect the etching speed are found in the step of "Etch B". Firstly, the pressure is set to 40 mTorr and then increased with the step of 20 to 80 mTorr from low speed etching to high speed etching conditions. Secondly, the gas flow rate of SF$_6$ is increased from 150 sccm to 350 sccm with the step of 100 sccm, from the low speed etching to high speed etching. In the Bosch process, the deposition of the chemical passivation layer with C$_4$F$_8$ and the isotropic plasma silicon etching with SF$_6$ correspond to the step of "Dep" and "Etch B" shown in the figures. The "Fast Etching Speed" regular recipe was chosen for my etching process for both sides and the etching time is set to 40 minutes.
Figure 5.14: EP06 Plasmatherm Versaline DRIE machine regular recipe of the "Slow Speed Etch".

Figure 5.15: EP06 Plasmatherm Versaline DRIE machine regular recipe of the "Medium Speed Etch".

Figure 5.16: EP06 Plasmatherm Versaline DRIE machine regular recipe of the "Fast Speed Etch".
Figure 5.17 shows a top view of a $2 \times 2 \text{ cm}^2$ chip with 100-$\mu$m-wide and 2900-$\mu$m-long fin structures taken in the SEM. Here I want to explain disadvantages of using the regular fast speed recipe for my etching process. Figure 5.18 shows a cross sectional view of the same fin structures. Note that the etching was processed from top to bottom. From the figure we can see much roughness at the bottom of the trenches and the shape of the trenches is shown "U" shape. According to the theory of the Bosh process, the passivation layer deposited by introduction of $\text{C}_4\text{F}_8$ can be removed by the plasma etching with introduction of $\text{SF}_6$, and then the silicon at the bottom will be etched in the same plasma process isotropically. But, if the passivation layer is too thick to remove efficiently, the actual etching time for silicon etching at the bottom becomes shorter and shorter with the process going on and finally the "U" shape is formed at the bottom, and the surface of the bottom of the trenches becomes rough. Moreover in Figure 5.18, we can observe that the depth of the trenches formed at the bottom side of the wafer is much shallower than that at the top side. This is due to a technical problem of the etching machine and as a result, the back side etching was stopped on the way of etching at the time of 30 minutes and 40 seconds. This problem was solved by changing the He pressure for wafer cooling. To decrease the He pressure can reduce the amount of the passivation layer to deposit during the etching, and this also can avoid stopping the etching on the way. As a result, the regular fast speed recipe was optimized by changing
Figure 5.18: SEM image of the cross section view of the 100 µm width and 2900 µm length fins on 2 cm\(^2\) chip, with 40 minutes top side etch and 30 minutes bottom side etch. Etched with the gas flow rate of C\(_4\)F\(_8\) 150 sccm, SF\(_6\) 350 sccm and Ar 30 sccm. The ICP power and chamber pressure were setted to 2500 W and 80 mTorr, respectively. The He pressure for backside cooling was set to 4000 mTorr.

Figure 5.19: Optimized recipe based on the "Fast Speed Etch" regular recipe with helium pressure changed to 3000 mTorr.

the helium pressure from 4000 mTorr to 3000 mTorr, and this condition was used to etch the both side of the wafer after all.

The optimized recipe is shown in Figure 5.19, and a cross sectional view of the etched wafer after 40-minute both side etching is shown in Figure 5.20. Compared with Figure
Figure 5.20: SEM image of the cross section view of the 100 \( \mu \text{m} \) width and 2900 \( \mu \text{m} \) length fins on 2 cm\(^2\) chip, with top and bottom side etching time of 40 minutes after the recipe optimization. Both sides were etched with the He pressure of 3000 mTorr for backside cooling of the clamp.

5.17, the micro fin trenches have flatter bottom surface and the bottom shape of the trenches were changed to the wider one, suggesting the removal of the passivation layer becomes more effective after reducing the He pressure drop. Furthermore, thanks to the change of the pressure, the etching depth for both the sides are nearly consistent and the final depth is measured to be 150 \( \mu \text{m} \). The width of the fins is appeared consistent with the designed dimension. For a structure of 100 \( \times \) 100 \( \mu \text{m}^2 \) pin fins on a 2 \( \times \) 2 cm\(^2\) chip, an SEM image of the top view is shown in Figure 5.21. A cross sectional view of the wafer showing the etched structures from both sides is also shown in Figure 5.22. From the image we can see the height of the pin fins on the bottom side is shorter than that of the pin fins on the top side. The height of the pin fins is also a little bit shorter than that of the fin structures shown in Figure 5.20. Considering the fact that the total height of this wafer is also shorter than the others, this shorter height may be caused by thinner silicon dioxide layer at this area. Uniformity of the SiO\(_2\) hard mask layer should be considered seriously for further consistent results.

Figure 5.23 shows the cross sectional view of 10 \( \times \) 10 \( \mu \text{m}^2 \) pin fins on a 2 \( \times \) 2 cm\(^2\) chip. As mentioned before, for the structure with smaller gaps (g), a relatively slower etching rate is expected. From this figure, the etching rate of the silicon can estimated around 3 \( \mu \text{m} \) per minute. Figure 5.24 shows a blow-up of the pin fins on the top side. Compared with the designed width of the pin fins, of 10\( \mu \text{m} \), the result shows 7.5\( \mu \text{m} \).
Figure 5.21: SEM image of the top view of the 100 $\mu m^2$ pin fins on 2 $cm^2$ chip.

Figure 5.22: SEM image of the cross section view of the 100 $\mu m^2$ pin fins on 2 $cm^2$ chip, with front and back side etching time of 40 minutes after the recipe optimization in pin fin width and 9.2$\mu m$ in gap width. Also we can observe that the width of the trenches becomes narrower in the deeper region, and the bottom shape is similar to the...
Figure 5.23: SEM image of the cross section view of the 10 $\mu$m$^2$ pin fins on 2 cm$^2$ chip, with front and back side etching time of 40 minutes after the recipe optimization.

Figure 5.24: SEM image of the cross section view of the 10 $\mu$m$^2$ pin fins on 2 cm$^2$ chip, with more clearly view of the pin fins on top surface.
"U shape" structures shown in Figure 5.18. There should be two reasons for this result. Firstly, as the gaps between the pin fins are narrow and the gas flow rate of the SF$_6$ is fixed, larger amount of SF$_6$ gas flow is required to etch the silicon in these narrower gaps. Particularly in this condition, silicon etching happens before the passivation layer is well deposited to the side walls, which can make the side walls be over-etched slightly. Secondly, as mentioned before, the He pressure is found to influence the amount of the passivation chemicals to be deposited on the side walls. The etching problem for the 100 $\mu$m fin structures was solved by decreasing the He pressure from 4000 mTorr to 3000 mTorr. However, for the structures with 10-µm-wide gaps, it seems that the He pressure of 3000 mTorr is not an optimum pressure for the passivation chemicals to be deposited, lower He pressure down to 2000 mTorr could be tried for future fabrication works. For better etching results, parameters for etching should be optimized separately depending on the characteristic size of the structure. Ideally the 100 $\mu$m and 10 $\mu$m structures should be prepared in separate wafers.

5.3 Bonding process

Following the objective of this project, fabrication of a 3D silicon heat sink which is an alternative stack of the surface modified silicon chips and the spacers is a clear target. The most common and easy method is to use the thermal tapes or glues to bond them together. However, considering the issue of increasing the thermal resistance between the individual pieces and the purpose of this project to develop an all silicon integrated surface modified heat sinks, silicon to silicon direct bonding without any inter layer material between the chips is worth being explored.

5.3.1 Bonding machine and designed chip-bonding mould

In the review of the previous silicon direct bonding methods, the pressure and temperature are found to be two key parameters. Appropriate conditions can be achieved by using the wafer bonding machine. Figure 5.25 shows the bonding machine EVG501 with a 6 inch wafer clamp.

From the figure we can see that the clamp holder of this machine is for 6 inch wafers, and it is obviously not suitable for bonding the small chips. In this case, a stainless steel chip-bonding mould with the diameter of 6 inch has been designed to hold and fix the chips in this machine. Furthermore, the holder can make the bonding spacer be embedded at the four etched corners much easier. Figure 5.26 shows the image of the designed holder that can be placed on the clamp of the wafer bonding machine. The five slots were designed with the same dimension and labelled as shown in the figure, and the small holes at the four corners of the slot are used to make sure that the chip
Figure 5.25: The bonding machine EVG501 for 6 inch wafer.

Figure 5.26: The stainless steel holder designed for bonding with the diameter of 150 mm and the five slots are with the dimension of $22 \times 22 \times 3$ mm$^3$.

can be removed from back side of the holder easily when they get stuck in the slot. The depth of the slot was designed to be fit with the height of the thickness of three chips.

5.3.2 Chip bonding process

Figure 5.27 shows the process to put the chips into the slot of the holder. This test was
performed for two different sets of pieces: one set has two chips with flat surface and four Type1 bonding spacers which are placed at the four corners of the chips, and another set has two chips with $10 \times 10 \mu m^2$ pin fin structure surface and four Type2 bonding spacers. Figure 5.28 shows the two procedures before running the bonding process: (a) a soft graphite disc is covered on top of the stainless steel holder to supply uniform pressure, (b) four valves are used to close the chamber.
5.3.3 Bonding results and discussion

The recipe of the machine is shown in Figure 5.29 with the list of the parameters of the process. Bonding test was started with this default recipe first.

![Figure 5.29: The recipe of the bonding machine, the force of the piston was set to 500 N for the first bonding test.](image)

Figure 5.29: The recipe of the bonding machine, the force of the piston was set to 500 N for the first bonding test.

![Figure 5.30: Bonding results with the piston force of 500 N.](image)

Figure 5.30: Bonding results with the piston force of 500 N.
A detail of the recipe is as follows. First, chamber is preheated at the temperature of 90 °C and then the temperature will be increased up to 350 °C under clamping the top and bottom. The force of the piston was setted to 500 N with in the ”Piston down” option. Note that the test is continued with the increase of the piston force from 500 N to 2000 N with the step of 500 N and this is the key parameter adjusted every time. The process time was 8 hours for each test. Figure 5.30 shows the result that appeared after opening the chamber after using the piston force of 500 N. The result suggests that the bonding was unsuccessful under this condition. The results were basically not changed with increasing the piston force up to 2000 N. To investigate the reason of the failure, the other test set of three flat chips, with no bonding spacers were loaded to the holder when the bonding was run under the piston force of 2000 N. While the sets with spacers were not bonded yet, a set of 3 flat wafers is well bonded under this condition. Figure 5.31 shows the bonding result with the piston force of 2000 N.

As shown in the figure the piston force of 2000 N is too high for the set with the 10 × 10 µm² pin fin structure chip to survive. While the others were survived under this level of pressure, the flat chips with Type1 bonding spacers in between were not bonded yet together. The two flat chips bonded with this process are shown in Figure 5.32.

Based on these bonding tests, piston force of 2000 N and temperature of 350 °C should be the suitable parameters for the chip bonding when using this machine, because the
Chapter 5 Fabrication of Surface-Modified Silicon Heat Sinks

Figure 5.32: The bonded two flat chips without bonding spacers in between.

two flat chips without bonding spacers in between were bonded successfully. For the breakage of the chips in slot 1 shown in Figure 5.31, there are possible several reasons. First, the pressure was too high to bond these types of the sample. Secondly, the bonding spacers in between were misaligned with the etched grooves very well. In particular for the Type2 spacer, the pins and holes formed on the spacers and the four etched square grooves are very tiny so it appeared to be very hard to control. For the samples in slot 3 shown in Figure 5.31, two reasons may cause the breakage: one is the fact that the contact surface area is too small to bond, and another is the fact of that the surface roughness is to high to meet the bonding requirement. The surface of the bonding spacers or the chip is not very uniform and this is also why the structured chips after DRIE etching could not be bonded with the small spacers at the corner. Actually, the roughness control of the plasma-etched surface is a key issue for further development of bonding technology.

5.4 Summary

Original fabrication process has been designed to generate the surface modified silicon heat sinks, which includes the development of double-side silicon wafer etching processes for the target structures and silicon to silicon direct bonding by using the wafer bonding machine. Double-side deep etching of silicon wafers has been successfully completed by optimizing the regular recipe of the DRIE machine. A chip-level silicon-to-silicon direct
bonding technology has been established with the development of the specific chip holder and with the optimization of bonding conditions. As a result, two flat silicon chips have been successfully bonded together. Through the development of this bonding technology, improvement of surface roughness generated after DRIE process is found to be a key thing for future successful bonding of chips with spacers.
Chapter 6

Heat Transfer Property Measurements for Surface-modified Silicon Heat Sinks

In this project, two types of measurement set up have been developed: (1) large wind tunnel integrated with IR thermal camera for characterisation of whole assembled heat sinks, and (2) mini wind tunnel integrated with Raman spectrometer for characterisation of individual surface-modified silicon chips. In this chapter, firstly my effort on developing a customised thermal camera measurement system for assembled heat sinks is briefly introduced. And then a novel mini-wind-tunnel-integrated Raman thermometry set up will be introduced later. Note that, due to time constraint and technical problems for bonding technology shown in Chapter 5, main results of thermal property characterisation are obtained from the Raman thermometry of the surface modified chips. After reviewing relevant literature about methods of heat transfer properties of heat sinks, analysis of the Raman Stokes peak position shift due to the change of the temperature has been found to be a promising method. With respect to its accuracy and a good level of temperature and time resolutions. A novel experimental system has been developed for the temperature measurement of the surface modified single silicon chip by integrating a custom-made mini wind tunnel with existing commercial Raman spectrometer. In this experiment, sample chips with flat surface, $100 \times 100 \, \mu m^2$ pin fin structure, $100 \times 2900 \, \mu m^2$ fin structure and $10 \times 10 \, \mu m^2$ pin fin structure were measured by using 532 nm laser. Experimental details and results will be shown in the following sections.
6.1 Experimental station development of large wind tunnel integrated with Infrared Thermal Imaging Camera

A schematic drawing of the test station designed for characterising assembled silicon heat sinks is shown in Figure 6.1. A wind tunnel, a heater block and air fan are assembled. A removable circular lid with screw thread is used for fixing the anemometer to be inserted into the wind tunnel.

Details of the heater block and a commercial cartridge heater integrated with the heater are shown in Figure 6.2. The thermal insulator foam was filled in the space between the copper cylinder and the outside block to make sure that the heat generated by the heater cannot escape to the outside environment. The outside block is surrounded by plastic glass except for the top plate which is made from ceramic to separate the hot surface of the copper cylinder from the surrounding and to keep the block safe when the top of the copper cylinder becomes very hot.

The actual heater block after produced by the university workshop is shown in Figure 6.3, together with the enclosed variable transformer to control the input power of the heater. Two type K thermocouples were inserted into the ceramic cylinder and integrated at the top and bottom surface of the copper cylinder to measure the temperature and also monitoring thermal uniformity of the cylinder. The discrepancy between the designed copper cylinder and the product are: (1) the ceramic top surface of the block was replaced by a ceramic cylinder and (2) thermal insulator was not filled into the
Chapter 6 Heat Transfer Property Measurements for Surface-modified Silicon Heat Sinks

Figure 6.2: Designed heater block with the integrated commercial cartridge heater.

block but filled between the copper cylinder and ceramic cylinder instead. This change has relatively saved the manufacture time and cost.

Figure 6.3: The fabricated heater block after connected with the power controller and two Type K thermocouples at top and bottom.

The anemometer mentioned above is shown in Figure 6.4. This anemometer is able to detect flow rate with different units such as m/s, LPM or ft/min and to measure the temperature at the same time. For data collection from the thermocouples, data logger with 8 insert ports shown in Figure 6.5 were used. After connecting this data logger with a computer by using a USB cable, temperature data were collected and saved by using an embedded program software.

The designed large wind tunnel is shown in Figure 6.6, together with the integrated air fan and fan speed controller. The wind tunnel with double chambers was designed
in consideration with a thermal insulating layer boundary condition and possible introduction of air in the gap between these two chambers. Figure 6.7 shows the overall configuration of the cooling system after integration of all the components together.

An infrared thermal imaging camera is integrated with the wind tunnel station. The configuration of the experimental station is shown in Figure 6.8. In order to test the
accuracy of the camera, the thermocouple was placed on the heater surface during the
measurement by using camera. The temperature measurement result is shown in Figure
6.9 by applying different voltages to the heater. As we can see there is a big discrepancy
between these two results, which suggests that the camera should be calibrated before
starting to use if acquisition of absolute temperature is required.

Instead, thermal imaging was tested for chosen samples. Some thermal images taken
when heater is turned on are shown in Figure 6.10. The images of (A) an aluminium
commercial pin fin heat sink with the size of $21 \times 21 \times 9$ mm, (B) a ceramic commercial
pin fin heat sink with the size of $19 \times 19 \times 6$ mm, (C) an aluminium commercial pin
Figure 6.8: Experimental station set up with infrared thermal imaging camera, heater and fabricated silicon sample chip placed under it.

Figure 6.9: Heater temperature test results with thermocouples and IR camera at same time, different voltages were applied to the heater.

fin heat sink with the size of $10 \times 10 \times 12.5$ mm and (D) a fabricated silicon chip with the structure of $100 \times 2900 \, \mu m^2$ fin on the surface.

As mentioned at the beginning, this system was not used mainly due to (1) technical issues of the system itself and (2) time constraint for the fabrication of whole heat sinks. For further improvement of the system, the following points should be considered. (a) Uniformity of air flow by considering the shape and size of the wind tunnel, (2) the size of the heater and cylinder to make sure the stable temperature is achieved in a reasonable time scale, (3) accurate calibration of thermal camera to obtain the absolute temperature data.
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6.2 Raman Spectroscopy Experimental Station Setup

The experimental station set up for Raman thermometry for the surface-modified heat sinks is shown in Figure 6.11. The air flow pump is used to generate air flow, which requires the voltage supply of 12 V and its nominal power is 12 W. In operation, the air flow rate of 9 to 15 LPM (Liter per Minute) can be generated with the maximum pressure drop of 150 KPa. The size of the ceramic heater is $2 \times 2 \text{ cm}^2$ with 49 pairs heating resistors inside. The maximum working current and voltage of the heater are 3 A and 6 V, respectively. In order to reduce the heat conduction from the backside of the heater to the microscope stage, a thermal insulator gel sheet with the thickness of 1
mm and with thermal conductivity of 2 W/m·K is placed under the heater, and this is also used to fix the heater in the wind tunnel. Both the air flow pump and the heater are connected to the power supply, which has double output ports with the maximum voltage of 30 V and the maximum current of 2 A. The air pump was connected with the wind tunnel by using a clear PVC (Polymerizing Vinyl Chloride) pipe and an adapter. A photo of the mini wind tunnel integrated with Raman microscope lens is shown in Figure 6.12.

![Figure 6.12: Clearly view of the mini wind tunnel and heater with air flow pipe under the x50 Raman microscope lens.](image)

For stable measurements, the wind tunnel and the pipe are fixed by tape. In the picture we can see the heater is placed in the middle of the wind tunnel base plate, and the test sample chip is placed on the heater and focused by the x50 lens. A diagram of the designed wind tunnel and the details of the dimensional parameters are shown in Figure 6.13.

This wind tunnel was designed according to the size of the wind tunnel in my simulation work presented in Chapter 4 and also according to the very limited space under the Raman microscope. As shown in the schematic diagram, the lid of the wind tunnel consist of two separated glass pieces with semicircle sections, and also they are moveable within the grooves on the two side walls. In Figure 6.12 we can see the x50 lens is adjusted into the hole after being focused. As the distance between the bottom of the lens and the surface of sample chip is less than 1 mm, it is impossible to integrate this type of wind tunnel without using these movable lids. So the lid is designed as it looks like, and for enough spaces and to make sure the lens can be changed safely, the diameter of the circular shape is designed as 40 mm as the x50 lens has the diameter of 32 mm.
Figure 6.13: Explanation of the Raman experimental mini wind tunnel with labelled dimensions in the unit of millimetre. All parts of the wind tunnel were cut from glass chip, which has the thickness of 1 mm.

6.2.1 Characterization and Results Analysis

Figure 6.14: Thermal equivalent time of the heater test with different voltages.

In order to investigate the heat transfer characteristics of different micro structures under Raman microscope system, external heater was placed under the samples and the time to take to be thermal equilibrium after turning on the heater was measured first. Figure 6.14 shows the change of the temperature monitored by the type K thermal couple placed on the surface of the heater with varied supply voltage of the heater. From
this test, the time to reach to a stable temperature in this system is estimated around 5 minutes. In the following experiments, heater voltage was set at 3 V.

A Renishaw InVia Raman microscope with 532 nm laser was used for all the following measurements. The transient measurement mode was used to characterize the heat transfer properties of the surface modified silicon chips. The detailed setting of the measurements are shown in Table 6.1.

Table 6.1: Time resolved Raman measurement of the spectral acquisition setup.

<table>
<thead>
<tr>
<th>Grating scan type</th>
<th>Confocality</th>
<th>Spectrum Range (Raman shift/cm$^{-1}$)</th>
<th>Laser name</th>
<th>Grating name</th>
<th>Detector name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static</td>
<td>Standard</td>
<td>-165.21 to 1132.90 centre 520</td>
<td>532 nm edge</td>
<td>2400 l/mm (vis)</td>
<td>Master: Renishaw CCD Camera</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Acquisition Setting Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exposure time (s)</td>
</tr>
<tr>
<td>-------------------</td>
</tr>
<tr>
<td>2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing Setting Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of acquisitions</td>
</tr>
<tr>
<td>--------------------------</td>
</tr>
<tr>
<td>90</td>
</tr>
</tbody>
</table>

Static grating scan is used for high-speed spectra acquisition. Under the Acquisition and Timing dialogs, exposure time and interval time are set to 2 s and 8 s, which means the sampling time for one point is 2 s and the time between two sampling is 8 s, so that 10 s is taken to sample one point. In this case the number of acquisitions was set to 90 so that it takes 15 minutes (900 s) for each measurement. The laser power was set to 1 % for all of the measurements. A set of the measurements consists of four transient measurements for each sample: (1) Monitoring the Raman shift after turning on the heater without air flow, (2) monitoring the shift after turning off the heater without air flow, (3) monitoring the shift after turning on the heater with air flow, and (4) monitoring the shift after turning off the heater with air flow. All of the measurement time were set to 15 minutes and the current of the air flow pump was set to 12 A. A schematic diagram of the measurement procedures is shown in Figure 6.15.

Figure 6.16 shows the first 8 Raman spectra of a transient sampling measurement for a silicon chip sample with flat surface under no air flow condition. As the material scanned under the Raman spectroscopy is silicon, Raman shift around 520 cm$^{-1}$ is observed. So the data range plotted here is from 475 cm$^{-1}$ to 574 cm$^{-1}$.

As shown in Figure Figure 6.16, the Raman peak position is shifted as the temperature increases, which is observed after turning on the heater at the time when the number 3 data acquisition was completed. For further accurate analysis of the peak position, peak fitting analysis with Lorentz function has been applied for all the spectra taken in the following experiments. As an example, Figure 6.17 shows the result of the Lorentzian
Figure 6.15: Schematic diagram of the time resolved Raman measurement procedures.

Figure 6.16: Measurement results of the first 8 Raman shift sampling of the silicon sample with flat surface.

fitting for the fist sampling point in Figure 6.16, and the Raman shift value of $521.60 \text{ cm}^{-1}$ has been obtained after the fitting.

After fitting all the sampling data, the accurate Raman shift data can be plotted as a function of time. Figure 6.18 shows the time dependence of the silicon Raman peak position for the flat-surface sample under 4 different monitoring conditions: results after the heater turned on (a) with no air flow and (b) with air flow, and the results after the heater turned off (c) with no air flow condition and (d) with air flow.
Figure 6.17: Raman shift and Lorentz fitting results of the first sampling point of the silicon chip with flat surface.

Figure 6.18: Lorentz fitted Raman shift results of the flat surface silicon sample for all measurements. For no air flow condition: (a) with heater turned on and (c) with heater turned off. For air flow introduced: (b) with heater turned on and (d) with heater turned off.

From the figures we can see that when the air flow is introduced, compared with the results under no air flow condition, the peak position has changed faster and then reached
Figure 6.19: Lorentz fitted Raman shift results of the silicon sample with 100 \( \mu \text{m}^2 \) pin fin surface for all measurements. For no air flow condition: (a) with heater turned on and (c) with heater turned off. For air flow introduced: (b) with heater turned on and (d) with heater turned off.

In general, measurement of the temperature change by using micro-Raman spectroscopy is based on the measurement of the change of the Raman peak position. After the Raman shift for each condition is obtained, this shift can be transformed to actual temperature change by using appropriate function fitting methods which have been mentioned in Chapter 2 in Figure 2.20. After transferring a Raman shift value to temperature with the unit in Celsius (\(^\circ\text{C}\)), the time dependent temperature results for the flat surface sample has been plotted as shown in Figure 6.21.

Every Raman shift result taken can be transferred to corresponding temperature in principle. On the other hand, the Raman shift value of the silicon is very hard to be calibrated accurately, therefore I am not focusing absolute temperature value in this study. Instead, as the temperature is found varied in a reasonable range, first the Raman shift is converted to the corresponding temperature by using an equation and then the data are analysed without considering the absolute value. For the analysis of the transient properties and comparison between chips with different surface modifications,
Chapter 6 Heat Transfer Property Measurements for Surface-modified Silicon Heat Sinks

Figure 6.20: Lorentz fitted Raman shift results of the silicon sample with 100 \( \mu \text{m}^2 \) fin surface for all measurements. For no air flow condition: (a) with heater turned on and (c) with heater turned off. For air flow introduced: (b) with heater turned on and (d) with heater turned off.

This method can be applicable. When the air flow is introduced in the wind tunnel, Figure 6.21 (b) and (d) show the temperature is changed in a smaller range and the sample temperature has reached to be stable rather faster. Figure 6.22 and Figure 6.23 have displayed the time dependent temperature results of the silicon samples with 100 \( \times \) 100 \( \mu \text{m}^2 \) pin fin structure and 100 \( \times \) 2900 \( \mu \text{m}^2 \) fin structure, respectively, after the data are converted.

In order to compare the cooling performance between individual samples with different micro structure surfaces, the measurement under the condition of cooling with air flow has been focused. For analysis of the transient temperature change, fundamental theory of the Newton’s law of cooling as a function of time has been mentioned in section 3.1.2, Chapter 3. An exponential decay function is used to fit the transient properties. Corresponding curves are the number (d) in Figure 6.21, Figure 6.22 and Figure 6.23, respectively. The equation used in this study is,

\[
y = A \times \exp(-x/t) + y_0, \tag{6.1}
\]

where \( A \) is the scaling factor, \( y_0 \) is the offset and \( t \) is the decay time constant, which can used to estimate the cooling performance of silicon chip surface with modified microstructures, the smaller \( t \) means the better cooling performance. As an example,
Figure 6.21: Time dependent temperature measurement results of the silicon sample with flat surface.

Figure 6.22: Time dependent temperature measurement results of the silicon sample with 100 µm² pin fin structure.
Figure 6.23: Time dependent temperature measurement results of the silicon sample with 100 $\mu$m$^2$ fin structure.

Figure 6.24 shows the fitted temperature curve of the flat silicon chip in cooling and with air flow, and the $t$ is obtained to be 14.20313 with the standard error of 0.64959 after fitting.

After fitting all the experimental results for all sample chips under the same flow condition, the extracted time constant $t$ are listed in Table 6.2. As we can see from the table,
under the cooling condition, the time constant $t$ of the sample with $100 \times 100 \, \mu m^2$ pin fin surface structure has the smallest value, which means this sample has the best cooling performance. The second best is the flat surface sample, and the $100 \times 2900 \, \mu m^2$ fin sample has the longest time constant, which means its cooling performance is not good. On the other hand, under the heating condition, these three samples have similar values of $t$, but when compared with each other, the $100 \times 100 \, \mu m^2$ pin fin sample still has the largest $t$, indicated the temperature on the surface is hard to be increased, suggesting the cooling performance of this sample is best.

Table 6.2: Fitted time constant $t$ values for all samples under the air flow condition.

<table>
<thead>
<tr>
<th>Sample surface</th>
<th>Heater on</th>
<th>With air flow</th>
<th>$t$</th>
<th>Standard error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flat</td>
<td>Yes</td>
<td>Yes</td>
<td>8.15723</td>
<td>0.60592</td>
</tr>
<tr>
<td></td>
<td>No</td>
<td>Yes</td>
<td>14.20313</td>
<td>0.64959</td>
</tr>
<tr>
<td>$100 , \mu m^2$ pin fin</td>
<td>Yes</td>
<td>Yes</td>
<td>8.67485</td>
<td>0.81547</td>
</tr>
<tr>
<td></td>
<td>No</td>
<td>Yes</td>
<td>12.56281</td>
<td>0.71852</td>
</tr>
<tr>
<td>$100 , \mu m$ fin</td>
<td>Yes</td>
<td>Yes</td>
<td>8.0266</td>
<td>0.53467</td>
</tr>
<tr>
<td></td>
<td>No</td>
<td>Yes</td>
<td>16.499</td>
<td>0.74358</td>
</tr>
</tbody>
</table>

6.2.2 Discussion and Optimization Method

In order to clarify the accuracy and the reproducibility of the experiment data, another measurement was done for all of the samples. As confirmed with the results in the last measurements, temperature becomes stable within 150 s after turning on or off the heater in this measurement system. The next step was to improve the time resolution to obtain more accurate value of the characteristic time for heat spreading. In the following experiment, air flow pump was kept on all the time and two types of measurements are designed. For the first measurement, total sampling time was set to 120 s and for the second one it was kept 900 s, which is the same as in the last time. For the 120 s measurement, the exposure time is changed to 1 s under the Acquisition interface, the interval time was set to 0 s, and as a result the acquisitions was set to 120 under the Timing dialog. This setting offers 120 samplings in total, which will be taken within 120 s. For 900 s measurement, setting of these parameters was kept the same as before. The same laser wavelength of 532 nm with 1% power was used as well as in the last measurement. The measurement results of Raman shift obtained from the chip with flat surface is shown in Figure 6.25.

Figure 6.26 and Figure 6.27 show the measurement results of Raman shift obtained from the chips with $100 \times 100 \, \mu m^2$ pin fin surface and $100 \times 2900 \, \mu m^2$ fin structure, respectively. In each figure, (a) and (c) are taken with the setting for finer time resolution and (b) and (d) are with the same time resolution as before. Then these Raman shifts were converted to the temperature with respect to the time as was mentioned previously.
Figure 6.25: Time dependent Raman shift measurement results under air flow condition of the silicon sample with flat structure for 120 s sampling (a) heater on and (c) heater off, and 900 s sampling (b) heater on and (d) heater off.

Figure 6.26: Time dependent Raman shift measurement results under air flow condition of the silicon sample with 100 µm² pin fin structure for 120 s sampling (a) heater on and (c) heater off, and 900 s sampling (b) heater on and (d) heater off.
Figure 6.27: Time dependent Raman shift measurement results under air flow condition of the silicon sample with 100 µm fin structure for 120 s sampling (a) heater on and (c) heater off, and 900 s sampling (b) heater on and (d) heater off.

Figure 6.28: Time dependent temperature results under air flow condition of the silicon sample with flat surface for 120 s sampling (a) heater on and (c) heater off, and 900 s sampling (b) heater on and (d) heater off.
Figure 6.29: Time dependent temperature results under air flow condition of the silicon sample with 100 $\mu$m$^2$ pin fin structure for 120 s sampling (a) heater on and (c) heater off, and 900 s sampling (b) heater on and (d) heater off.

Figure 6.30: Time dependent temperature results under air flow condition of the silicon sample with 100 $\mu$m fin structure for 120 s sampling (a) heater on and (c) heater off, and 900 s sampling (b) heater on and (d) heater off.
Chapter 6 Heat Transfer Property Measurements for Surface-modified Silicon Heat Sinks

The results shown in Figure 6.28, Figure 6.29 and Figure 6.30 are for the sample chips with flat surface, \(100 \times 100 \mu m^2\) pin fin structure and \(100 \times 2900 \mu m^2\) fin structure, respectively. Then these transient curves of each sample were fitted by the first order exponential function as mentioned before, and the time constant \(t\) was extracted to measure the cooling performance of each micro structure. The extracted time constants are listed in Table 6.3.

Table 6.3: Fitted time constant \(t\) values for all samples with 120 s and 900 s sampling time scale, air flow always applied.

<table>
<thead>
<tr>
<th>Sample with flow</th>
<th>Sampling time</th>
<th>(t)</th>
<th>Standard error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flat</td>
<td>Heating</td>
<td>120 s</td>
<td>6.74214</td>
</tr>
<tr>
<td></td>
<td></td>
<td>900 s</td>
<td>11.94853</td>
</tr>
<tr>
<td></td>
<td>Cooling</td>
<td>120 s</td>
<td>8.51933</td>
</tr>
<tr>
<td></td>
<td></td>
<td>900 s</td>
<td>11.14873</td>
</tr>
<tr>
<td>100 (\mu m^2) pin fin</td>
<td>Heating</td>
<td>120 s</td>
<td>8.52938</td>
</tr>
<tr>
<td></td>
<td></td>
<td>900 s</td>
<td>15.2373</td>
</tr>
<tr>
<td></td>
<td>Cooling</td>
<td>120 s</td>
<td>4.70577</td>
</tr>
<tr>
<td></td>
<td></td>
<td>900 s</td>
<td>8.58356</td>
</tr>
<tr>
<td>100 (\mu m) fin</td>
<td>Heating</td>
<td>120 s</td>
<td>4.89266</td>
</tr>
<tr>
<td></td>
<td></td>
<td>900 s</td>
<td>6.44199</td>
</tr>
<tr>
<td></td>
<td>Cooling</td>
<td>120 s</td>
<td>9.09942</td>
</tr>
<tr>
<td></td>
<td></td>
<td>900 s</td>
<td>12.2177</td>
</tr>
</tbody>
</table>

Thanks to the measurements with finer time resolution, the extracted time constants should be more reliable. Indeed, the standard error of the time constant is around 0.3. The fitting results of the data taken on 120-second measurements has clearly confirmed that the time constant \(t\) of the sample with \(100 \times 100 \mu m^2\) pin fin structure has the smallest value under cooling condition. For the other two samples, the flat surface sample has shown shorter \(t\) compared with the \(100 \times 2900 \mu m^2\) fin structures. Looking at the results under heating condition, both results of 120 s and 900 s monitoring show that the sample with \(100 \times 100 \mu m^2\) pin fin structure has the longest \(t\) value, suggesting of the good cooling performance of this structure. The second best is the sample with flat surface and the sample with \(100 \times 2900 \mu m^2\) scale fin structures have shown the shortest \(t\) value, indicating it has the worst cooling performance among those three samples. The data are confirmed to have has excellent consistency. Including the results of the previous experiments, and a good level of reproducibility of this experimental method has been confirmed.

Compared with the simulation results shown in Chapter 4, experimental results are well consistent with the fact that a micro pin fin structure has the lowest temperature than any other samples with the same height for the microstructures’. Here I would like to mention the results of the transient measurements for the sample with \(10 \times 10 \mu m^2\) pin fin structure on the surface, which was measured under the cooling condition with air flow. The 900 s transient monitoring was applied to the measurement. Figure 6.31 shows the change of temperature with respect to the time under an air flow condition,
together with a exponential function fitting curve. As we can see the data are not stable and have larger fluctuation when the system has reached the thermal equilibrium. This is found to be caused by the losing of the laser focus during the heating and cooling. Due to thermal expansion/shrinkage, the vertical position of the top of a fin/pin fin is moved so that the lens focus is lost during the measurements. Therefore, relatively large fluctuation is observed after 80 seconds, resulting in a higher standard error compared with the data form the larger fins/micro fins.

6.3 Summary

In summary, a novel experimental system has been developed for the temperature measurement of the surface modified single silicon chip. The time resolved transient Raman spectroscopy was used to characterize the heat transfer properties. After fitting the Raman peaks with Lorentzian, the peak positions are converted to the temperature. The change of temperature as a function of time is then fitted with exponential decay functions. The sample chip with $100 \times 100 \mu m^2$ pin fin structure has been found to show the best cooling performance. The results are consistent for both the 900 s sampling time measurement and the 120 s time resolution measurement, and good data reproducibility has been confirmed. The sample with $10 \times 10 \mu m^2$ pin fin structure on the surface can not be measured by this Raman spectroscopy system as the limitation of the focus properties, and also it can not be auto-focused to the surface when the position of the sample surface was changed. Using a laser with different wavelength or changing
to another Raman measurement system with auto-focus functionality may make this sample possible to be measured.
Chapter 7

Conclusions

For better thermal management of future integrated circuits and electronic devices with ultra high power consumption, this project has focused on improving cooling performance of heat sinks by applying silicon micro fabrication technology. Literatures have been reviewed to identify what happens so far and to find the problems what should be optimized. Basic theories relevant to the thermal management have been learned, including the theory of heat transfer, fluid dynamics and the definition of thermal resistance. Through the theoretical study, how to define the boundary conditions in the simulation works is found to be very important, in particular in this type of hybrid simulations. How to calculate the heat sink thermal resistance and also how to extract the thermal resistance from the simulation results have been identified for further applications to various heat sink structures.

The thermal resistance of newly-designed surface-modified silicon micro-fin heat sinks has been calculated and compared with the conventional micro-fin and micro-pin fin heat sink structures. The results show that it is effective to reduce the thermal resistance by increasing the surface area of the heat sinks.

Simulation has been performed by using COMSOL Multiphysics to confirm the effects of surface modification of the heat sink on heat transfer. The calculated thermal resistance decreases first with increasing surface area but then increases with further increase of the surface area. This results suggests that there is an optimum value for the fin surface area to maximize the heat transfer of this system, and the discrepancy between the theoretical calculation and simulations might be due to lack of consideration of conduction heat transfer in analytical calculation. The simulation works have been further extended to calculate heat transfer of individual silicon chip with different micro structures and different height of these structures. Under the laminar air flow condition, the increase of the surface area is found to improve the cooling performance efficiently, but again a further increase is found to lead to worsen the cooling performance, suggesting there exists an optimum point to obtain the best cooling performance. Detailed calculation
has shown that the cooling performance of the micro fin structures is better than that of the micro pin fin structures when the height of the micro structure are less than 100 µm, while the micro pin fin structures are better when the heights is in the range of 100 µm to 150 µm.

To investigate the effects of surface modification on the heat transfer of silicon heat sinks, an original fabrication process has been designed and developed by using DRIE technology for double-side-polished silicon wafers. By adjusting the He flow pressure for wafer cooling during etching, well-controlled double-side deep etching with the etching depth of down to 150 µm has been achieved. For assembled heat sinks, a number of $1 \times 1$ cm$^2$ and $2 \times 2$ cm$^2$ chips with microstructures on their surface, and relevant spacers are designed on multiple double-side-polished silicon wafers and fabricated by using photolithography and etching processes. An original sample holder to realise the direct silicon-silicon bonding on the chip level has been designed and tested with a commercial wafer bonding machine. Although the assembly of the chips and spacers has not been succeed due to time constraint, successful bonding of two flat silicon chips with the newly designed holder and newly-developed recipe is promising for further investigation.

Two types of measurement set up have been newly developed in this project. A measurement station with a large wind tunnel integrated with IR thermal camera for characterisation of whole assembled heat sinks has been designed and developed from scratch. Although actual data acquisition has not been finished with this system due to time constraint and technical issues, the knowledge gained with this building work has been used to design the following Raman thermometry set up. For characterising the heat transfer properties of individual surface-modified silicon chips, a novel measurement system which combine a mini air flow wind tunnel and Raman spectrometer has been developed. The time resolved Raman spectroscopy has been used to study the transient thermal properties of the surface modified silicon chips. By monitoring the temperature obtained from the change of the silicon Raman peak position after turning on and off the integrated heater, the characteristic time constant of heat spreading has been extracted for each silicon chip with a specific surface modification. The results show that the sample chip with $100 \times 100$ µm$^2$ pin fin structure surface have the shortest time constant value, indicating that increasing surface area with micro pin fins are effective to improve the heat transfer from the surface to air under this condition. Having performed the experiments several times for the same sample under the same flow and condition with different time resolution, the data reliability has been confirmed and this method could be extended further for characterisation of the much smaller structures.

### 7.1 Future Remarks

The future work of this project will be divided into three parts:
Chapter 7 Conclusions

1). Fabrication and measurement of the single-side-etched silicon chips with different height of structures which same as the designed structure in the simulation work. Fabrication procedure is roughly same as what described in Chapter 5 and only one side need to be processed this time. As the etching rate of silicon is tested as \( \sim 4 \, \mu\text{m/min} \) in DRIE process, etching time should be adjusted with the optimized recipe to meet the different etching depth requirement. The same measurement procedure should be fellow for the new fabricated samples, and the results can be used to confirm the consistency with the simulation results. Furthermore, much finer time resolution can be applied to obtain more accurate results by changing the setting of exposure time and number of acquisitions.

2). Optimization of the dry etch process for bonding of the silicon chip with small bonding spacers. As discussed, the surface roughness of the bonding area after DRIE etching is important for successful bonding. Improvement of that can be realized by reducing the amount of fluoropolymer film after etching. Several parameters are interested to change based on this optimization, for example, reduce of the C\(_4\)F\(_8\) flow rate, increase of the SF\(_6\) flow rate, or increase of the chamber pressure during etching. Some balance must be obtained as these parameters also influence the etching rate and selectivities. The measurement of the stacked all silicon heat sink can be done after the successful bonding process by using the measurement system which has been developed. After developing this novel experimental system, temperature measurement of the micro structured silicon sample under air flow wind tunnel becomes promising and more accurate thermal properties can be obtained.

3). Silicon chips with much finer (less than 10 \( \mu\text{m} \) patterns) surface structures would be interesting to design, fabricate and characterize. Based on the work done so far in this project, increasing of the surface area of the heat sink is a key to improve the cooling performance, especially for the electronic devices who has ultra high heat dissipation but with very limited package space. Nano scale surface structures could introduce a brand new cooling performance map ever with air flow introduced. The measurement method for this kind of tinny structure should be investigated properly, and also Raman spectroscopy measurement system can be used as an invisible thermal couple, but the issue of lost the laser focus must be solved first considering the heat expansion of the samples.
Appendix A

MATLAB Code for Data Analysis

Thermal resistance calculation of the heat sink with big structures, e.g. 36 grooves:

Nfin=6;
Nslot=3;
tfin=0.001;
b=0.0008;
Hfin=0.008;
L=0.01;
Dslot=0.0003;
Wslot=0.001;
Agroove=Dslot*Wslot;
tmiss=6*(Agroove/Hfin);
teffc=tfin-tmiss;
beffc=b+tmiss;
Afintop=0.00001;
Afin=((2*Hfin*L+2*Hfin*tfin+Afintop+2*Dslot*L*6)-Agroove*12)*6;
Abase=(Nfin-1)*b*L+0.00008;
Across=(0.005*0.001+Agroove*Nslot)*2+5*(b*Hfin+2*Agroove*Nslot)+0.002;
Vin1=1;
Vin2=2;
Vin3=3;
Vin4=4;
S=0.022;
u=1.846e-05;
k=0.024;
kfin=130;
Pr=0.707;
rho=1.205;
Appendix A MATLAB Code for Data Analysis

Gin1 = Vin1 * S;
Gin2 = Vin2 * S;
Gin3 = Vin3 * S;
Gin4 = Vin4 * S;
Vmean1 = Gin1 / Across;
Vmean2 = Gin2 / Across;
Vmean3 = Gin3 / Across;
Vmean4 = Gin4 / Across;
Re1 = (rho * Vmean1 * beffc^2) / (u * L);
Re2 = (rho * Vmean2 * beffc^2) / (u * L);
Re3 = (rho * Vmean3 * beffc^2) / (u * L);
Re4 = (rho * Vmean4 * beffc^2) / (u * L);
Nu1 = ((1 / (Re1 * Pr / 2)^3) + (1 / (0.664 * Re1^0.5 * Pr^0.33 * (1 + 3.65 / Re1^0.5)^0.5)^3))^-0.33;
Nu2 = ((1 / (Re2 * Pr / 2)^3) + (1 / (0.664 * Re2^0.5 * Pr^0.33 * (1 + 3.65 / Re2^0.5)^0.5)^3))^-0.33;
Nu3 = ((1 / (Re3 * Pr / 2)^3) + (1 / (0.664 * Re3^0.5 * Pr^0.33 * (1 + 3.65 / Re3^0.5)^0.5)^3))^-0.33;
Nu4 = ((1 / (Re4 * Pr / 2)^3) + (1 / (0.664 * Re4^0.5 * Pr^0.33 * (1 + 3.65 / Re4^0.5)^0.5)^3))^-0.33;
h1 = Nu1 * k / beffc;
h2 = Nu2 * k / beffc;
h3 = Nu3 * k / beffc;
h4 = Nu4 * k / beffc;
m1 = ((2 * h1) / (kfin * teffc))^0.5;
m2 = ((2 * h2) / (kfin * teffc))^0.5;
m3 = ((2 * h3) / (kfin * teffc))^0.5;
m4 = ((2 * h4) / (kfin * teffc))^0.5;
et1 = tanh(m1 * Hfin) / (m1 * Hfin);
et2 = tanh(m2 * Hfin) / (m2 * Hfin);
et3 = tanh(m3 * Hfin) / (m3 * Hfin);
et4 = tanh(m4 * Hfin) / (m4 * Hfin);
Rhs1 = 1 / (h1 * (Abase + Nfin * et1 * Afin));
Rhs2 = 1 / (h2 * (Abase + Nfin * et2 * Afin));
Rhs3 = 1 / (h3 * (Abase + Nfin * et3 * Afin));
Rhs4 = 1 / (h4 * (Abase + Nfin * et4 * Afin));
x = [Vin1, Vin2, Vin3, Vin4];
y = [Rhs1, Rhs2, Rhs3, Rhs4];
plot(x, y);

Raman Shift results data range cutting from 475 cm\(^{-1}\) to 574 cm\(^{-1}\), e.g. 100 \(\mu\)m\(^2\) pin fin sample heated up with 900 s sampling time:

Inputfolder = ['C:\Users\yz16g13\University of Southampton\Yichi_Yoshi_Working\'];
FileName = ['90sampling_100umpinfin_heatup.xlsx'];
[ndata, text, alldata] = xlsread([Inputfolder, FileName])
A = ndata(:,1);
B = ndata(:,2);
C = ndata(:,3);

A1 = reshape(A, 1011, 120);
A2 = A1(460:538, :)

B1 = reshape(B, 1011, 120);
B2 = B1(460:538, :)

C1 = reshape(C, 1011, 120);
C2 = C1(460:538, :)

Raman Shift results data range cutting from 475 cm$^{-1}$ to 574 cm$^{-1}$, e.g. 100 $\mu$m$^2$ pin fin sample cooling with 120 s sampling time:

Inputfolder = ['C:\Users\yz16g13\University of Southampton\Yichi_Yoshi_Working\'];
FileName = ['120s_sampling_100umpinfin_cooling_withpump.xlsx'];
[ndata, text, alldata] = xlsread([Inputfolder, FileName])

A = ndata(:,1);
B = ndata(:,2);
C = ndata(:,3);

A1 = reshape(A, 1011, 120);
A2 = A1(460:538, :)

B1 = reshape(B, 1011, 120);
B2 = B1(460:538, :)

C1 = reshape(C, 1011, 120);
C2 = C1(460:538, :)

References


REFERENCES


[43] Chienliu Chang, Yeong-Feng Wang, Yoshiaki Kanamori, Ji-Jheng Shih, Yusuke Kawai, Chih-Kung Lee, Kuang-Chong Wu, and Masayoshi Esashi. Etching submicrometer trenches by using the bosch process and its application to the fabrication...


