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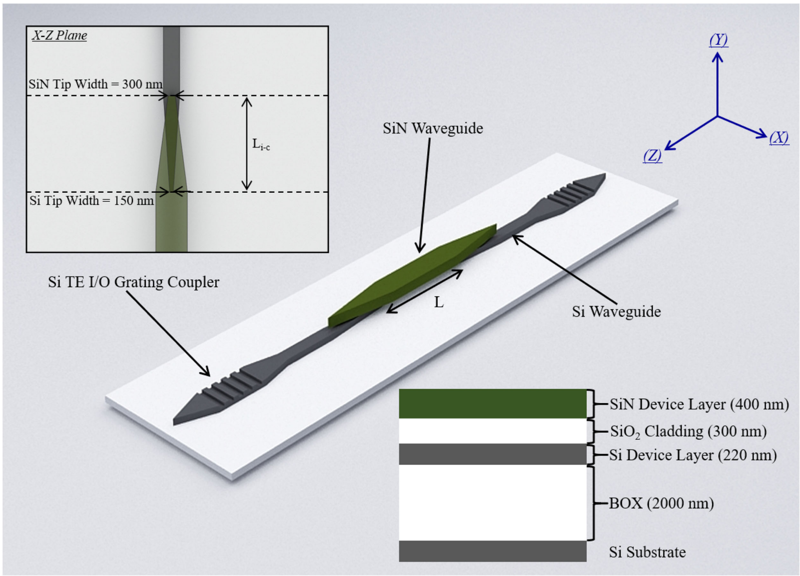
Jia Xu Brian Sia
Wanjun Wang
Xin Guo
Jin Zhou
Zecen Zhang
Xiang Li
Zhong Liang Qiao
Chong Yang Liu
Callum Littlejohns
Graham T. Reed
Hong Wang

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# SiN-SOI Multilayer Platform for Prospective Applications at 2 $\mu$m

**Jia Xu Brian Sia,[1] Wanjun Wang,[1] Xin Guo,[1] Jin Zhou,[1] Zecen Zhang,[1] Xiang Li,[1] Zhong Liang Qiao,[1] Chong Yang Liu,[1] Callum Littlejohns,[1,2] Graham T. Reed,[1,2] and Hong Wang[1]**

[1]Novitas, Silicon Centre of Excellence, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Singapore
[2]Optoelectronics Research Centre, University of Southampton, Southampton SO17 1BJ, U.K.

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**Abstract:** Silicon photonics at the 2 $\mu$m waveband, specifically the 1.9 $\mu$m wavelength region is strategically imperative. This is due to its infrastructural compatibility (i.e., thulium-doped fiber amplifier, hollow-core photonic bandgap fiber) in enabling communications, as well as its potential to enable a wide range of applications. While the conventional Silicon-on-Insulator platform permits passive/active functionalities, it requires stringent processing due to high-index contrast. On the other hand, SiN can serve to reduce waveguiding losses via its moderate-index contrast. In this work, by demonstrating SiN passives and Si-SiN interlayer coupler with favorable performance, we extend the Si-SiN platform to the 1.9 $\mu$m wavelength region. We report waveguide propagation loss of 2.32 dB/cm. Following, trends in radiation loss with regards to bending radius is analyzed. A high performance 3-dB power splitter with insertion loss and bandwidth of 0.05 dB and 55 nm (1935–1990 nm) respectively is introduced. Lastly, Si-SiN transition loss as low as 0.04 dB is demonstrated.

**Index Terms:** Silicon photonics, 2 $\mu$m waveband, silicon nitride, waveguides, photonic integrated circuits

## 1. Introduction

The capability of a computational architecture is largely dependent upon 2 main factors, gate and interconnection-delay. In late 2018, GlobalFoundries, one of the world's 3 largest advanced chipmakers (TSMC, Samsung, GlobalFoundries), ceased further developments at the 7-nm node [1], signaling the end to 50 over years of gate-scaling. Nevertheless, the limiting factor of current multi-core systems lies with interconnect fidelity, rather than transistor size. Silicon photonics has emerged as a scalable and large-bandwidth approach to solve the interconnect conundrum.

Similarly, the optical industry also faces its own set of problems, namely, that of information scaling. The common consensus is that there may not be much headroom left before nonlinear effects sets in with regards to the single-mode fiber (SMF) [2]; Cisco predicts that annual global IP traffic per year could reach 4.8 zettabytes by 2022 [3].

In view of the issues above, the implementation of silicon photonics at the 2 $\mu$m waveband becomes an attractive prospect. The 2 $\mu$m waveband, specifically the 1.9 $\mu$m wavelength region corresponds to the low-loss window of the hollow-core photonic bandgap fiber (HC-PBGF) [4], [5]. On the other hand, the thulium-doped fiber amplifier (TDFA) also enables high small-signal gain and low noise figures in the wavelength region [6], [7]. Besides optical communications, it is of note that the 1.9 $\mu$m wavelength region enables a wide range of technologies such as $H_2O$ spectroscopy [8], optical logic, signal processing [9] as well as enabling the optical Kerr effect [10]. In response to the wealth of applications at the 1.9 $\mu$m wavelength region, encouraging developments have been made in the area of silicon photonics [11]–[15]. However, there has been a lack of multilayer integration in a CMOS-compatible framework. While the high index-contrast ($\Delta n_{Si-SiO2} \approx 2$) of the SOI platform and decent electron/hole mobility of the Si enables passive (i.e., tight bending radius, efficient grating couplers) [16], [17] and active (high-speed electro-refractive induced modulation) [18], [19] optical functions respectively, it comes at a penalty of sensitivity to fabrication and environmental temperature drifts, thereby impacting device performance and stability [20], [21]. SiN, a commonly used material for masking, passivation and strain-engineering in CMOS foundries could serve to supplement the abovementioned shortcomings in Si passive functionalities with its moderate index-contrast ($\Delta n_{SiN-SiO2} \approx 0.5$) and lower thermo-optic effect [21]. Furthermore, SiN can be deposited on various material platforms via plasma-enhanced chemical vapor deposition (PECVD) in a CMOS-compatible process ($T < 400\,^{\circ}$C) enabling increased integration flexibility. The Si-SiN platform can exploit the active functionalities of the Si layer, while leaving the waveguiding to the low-loss SiN layer. In this work, we extend the Si-SiN platform from the near-infrared (NIR) [21]–[23] to the 1.9 $\mu$m wavelength region. The scope of this letter is concerned with the implementation of SiN passives at the 1.9 $\mu$m wavelength region as well as the coupling approach between the Si-SiN device layers. Firstly, SiN waveguides are designed, propagation loss of 2.32 dB/cm is characterized. Following, trends of bending radius on radiation loss is analyzed. A broadband, low-loss 3-dB power splitter implemented on the SiN device layer with a measured operating bandwidth of 55 nm ($\lambda = 1935$—1990 nm) and insertion loss as low as 0.05 dB is presented. Similarly, to the 3-dB power splitter, the designed adiabatic Si-SiN interlayer coupler enables broadband operation, in addition, low transition loss of 0.04 dB is measured.

## 2. SiN Waveguide Propagation Loss and Bend Loss Condition

The 3-D schematic of the Si-SiN platform is illustrated in Fig. 1, together with the coordinates. The Si device layer is utilized for the realization of I/O grating couplers on the 220 nm Silicon-on-Insulator (SOI) platform. The conventional TE-mode grating coupler ($\Lambda = 930$ nm, DC = 0.55, Etch Depth = 70 nm) has a measured coupling loss of ~6 dB. Such an I/O implementation will allow for alignment-tolerant fiber-coupling at the wafer-level and subsequent transition to the lower-loss SiN device layer via the interlayer coupler. The propagation loss of the single-mode TE Si waveguide (Cross-section = $0.6 \times 0.22\ \mu m^2$) is experimentally determined to be 3 dB/cm. Firstly, deep ultra-violet (DUV) immersion lithography and reactive ion etching (RIE) is used to define the Si layer. PECVD is used for blanket deposition of $SiO_2$ followed by chemical mechanical polishing to the desired thickness ($h_{SiO2} = 300$ nm). Following, the PECVD is used again for the deposition of the SiN device layer ($h_{SiN} = 400$ nm). Similarly, to the Si device layer, the SiN device layer is defined using DUV immersion lithography and RIE. Lastly, 1 $\mu$m-thick $SiO_2$ cladding is deposited using PECVD.

Fig. 2 shows the calculated effective indices of the first four eigenmodes (TE00, TM00, TE01, TM01) as a function of waveguide width (W) in a 400 nm thick SiN device layer; electric-field distribution of TE00, TM00, TE01, TM01 together with the corresponding values of W are shown in the inset. Refractive indices applied for the Si, SiN and $SiO_2$ layers are 3.444, 1.962 and 1.444 respectively. The single-mode condition is satisfied for $W \leq 1.5\ \mu$m; the wavelength used for computation is 1970 nm. The TM00/TE01 hybrid point occurs when $W \geq 2.4\ \mu$m.

The cutback approach was used to determine the propagation loss of the fabricated SiN waveguide (Cross-section = $W \times 0.4\ \mu m^2$). Waveguides with lengths(L) of 0.904, 2.134, 4.032 and 6.135 cm are fabricated, and the micrograph images are shown in Fig. 3(a). In Fig. 3(b), (c), we show the measured normalized transmission of waveguides with W = 1.2, 1.4 $\mu$m and lengths

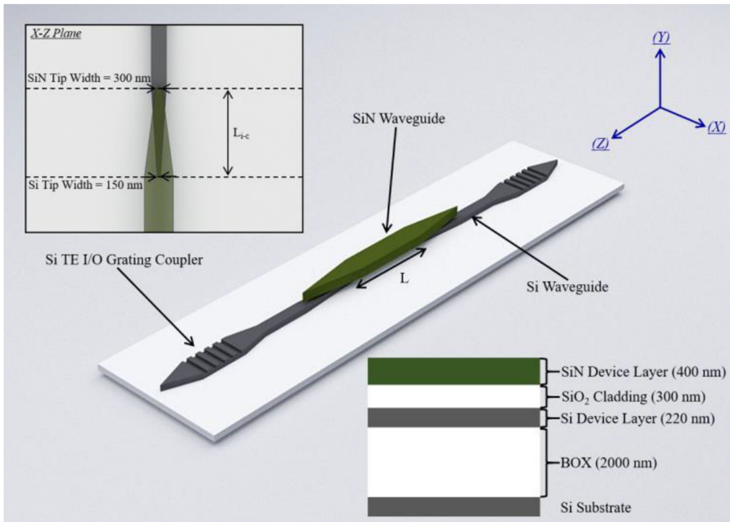


Fig. 1. 3-D schematic of the SiN-SOI platform at the 1.9 $\mu$m wavelength region (directional coordinates indicated); including Si TE grating couplers, waveguide, Si-SiN adiabatic interlayer coupler and SiN waveguide. Inset illustrates the X-Z plane of the Si-SiN adiabatic interlayer coupler.

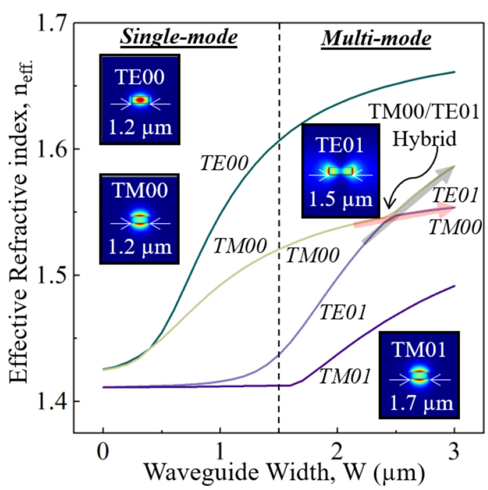


Fig. 2. Theoretical effective indices for TE00, TM00, TE01 and TM01 as a function of waveguide width.

as mentioned above. The measured propagation loss of the waveguides together with its associated error bars, over the maximum range ($\lambda$ = 1935–1990 nm) of our tunable laser (Thorlabs, customized) is shown in Fig. 3(d), obtained through the linear regression with regards to 4 different waveguide lengths (Fig. 3(a)–(c)). In general, it is observed that propagation loss increases at longer wavelengths. At shorter wavelengths, the waveguide propagation (W = 1.2, 1.4 $\mu$m) losses are similar, however, as the wavelength redshifts towards 1990 nm, the propagation loss when W = 1.2 $\mu$m becomes higher in contrast to W = 1.4 $\mu$m. The minimum, maximum measured propagation loss of waveguide when W = 1.2, 1.4 $\mu$m are 2.38, 3.64 and 2.33, 3.35 dB respectively. While we do not have a definitive explanation for the trend, we suspect that at shorter wavelengths, when optical confinement of the waveguides is higher, SiN material absorption plays a relatively significant role in propagation loss values. On the other hand, when wavelength increases, the wider waveguide (W = 1.4 $\mu$m) would be less susceptible to $SiO_2$ absorption and waveguide sidewall roughness

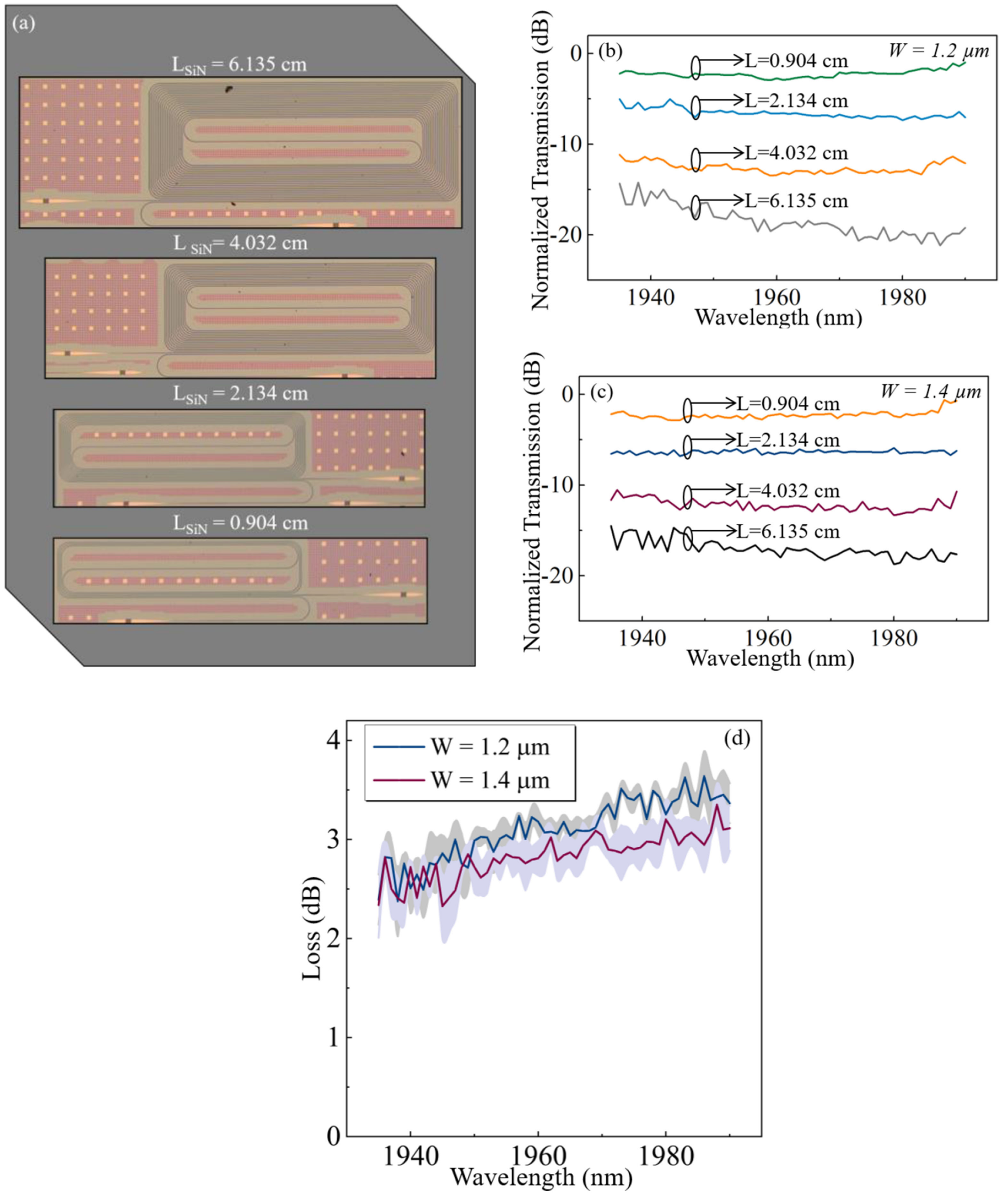


Fig. 3. (a) Micrograph images of SiN waveguides with L = 0.904, 2.134, 4.032, 6.135 cm. (b) Measured normalized transmission of SiN waveguides (W = 1.2 $\mu$m) with L = 0.904, 2.135, 4.032, 6.135 cm. (c) Measured transmission of SiN waveguides (W = 1.4 $\mu$m) with L = 0.904, 2.135, 4.032, 6.135 cm. (d) Measured waveguide propagation loss as a function of wavelength (W = 1.2, 1.4 $\mu$m).

in comparison to the narrower waveguide (W = 1.2 $\mu$m) due to higher confinement of the optical mode, thereby, accounting for the smaller increase in propagation loss as wavelength increases.

Following, the effects of bending radius on radiation loss is also studied. Firstly, Lumerical 3D-FDTD simulation (high mesh resolution) [24] was used to evaluate the critical value of bending radius at $\lambda = 1970$ nm, beyond which radiation loss is trivial for a 1.2 $\mu$m-wide waveguide; when bending radius exceeds 40 $\mu$m, radiation loss becomes negligible (Fig. 4(a)). A single wavelength ($\lambda = 1970$ nm) is used because we did not observe any wavelength dependence (1935-1990 nm) of waveguide bending loss with regards to radius. At the inset of Fig. 4(a), we show the X-Z plane electric-field distribution when R = 5, 40 $\mu$m. The bending loss when R = 30, 40 $\mu$m is characterized

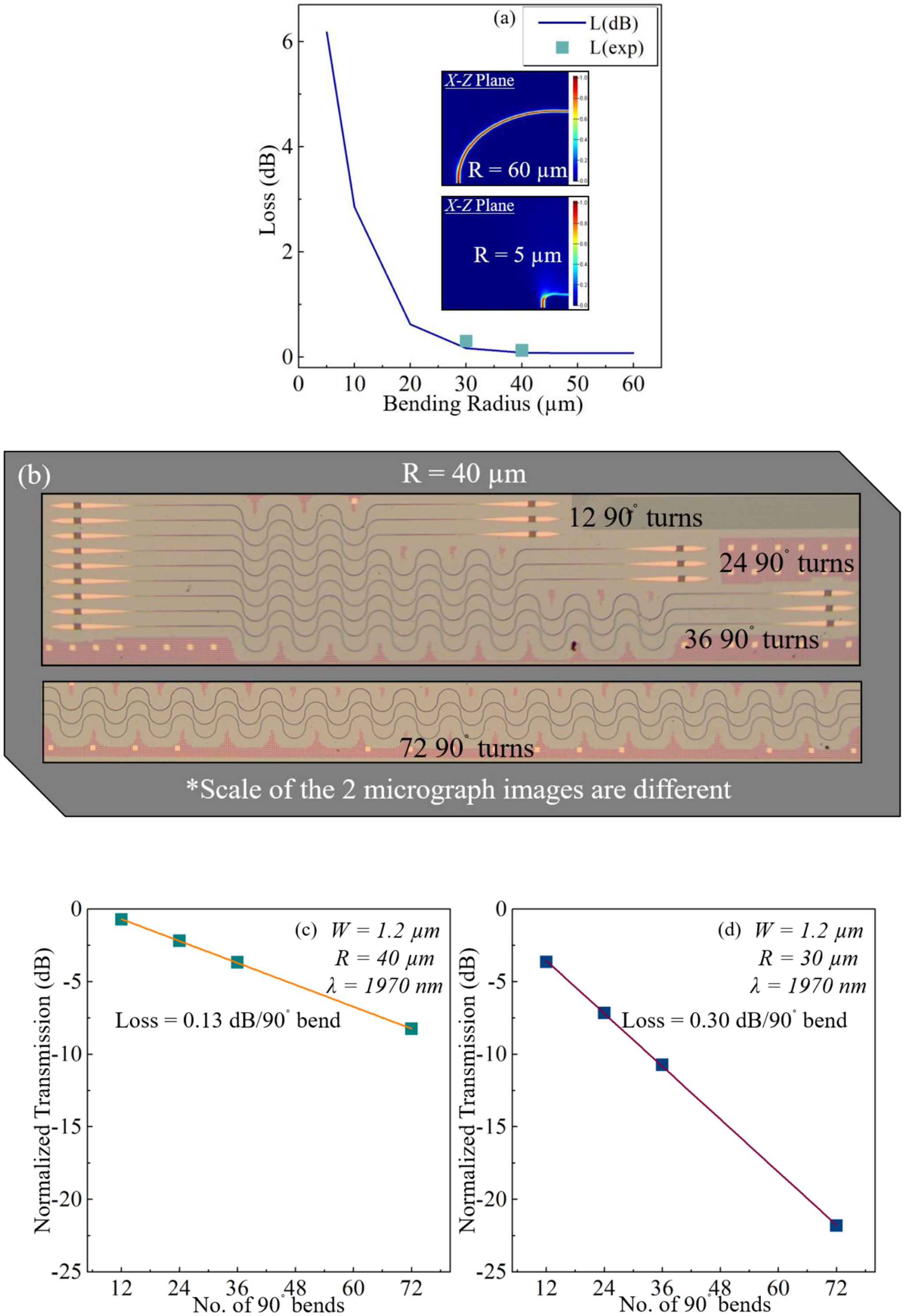


Fig. 4. (a) Simulated SiN 90° bending loss as a function of R. The 2 data points corresponds to the measured SiN 90° bending loss when R = 30, 40 $\mu$m; inset illustrates the electric-field distribution (X-Z plane) when R = 5, 40 $\mu$m. (b) Micrograph images of 12, 24, 36, 72 SiN 90° when R = 40 $\mu$m. (c) Measured SiN 90° bending loss from 12, 24, 36, 72 SiN 90° bends when R = 30 $\mu$m. (d) Measured SiN 90° bending loss from 12, 24, 36, 72 SiN 90° bends when R = 40 $\mu$m.

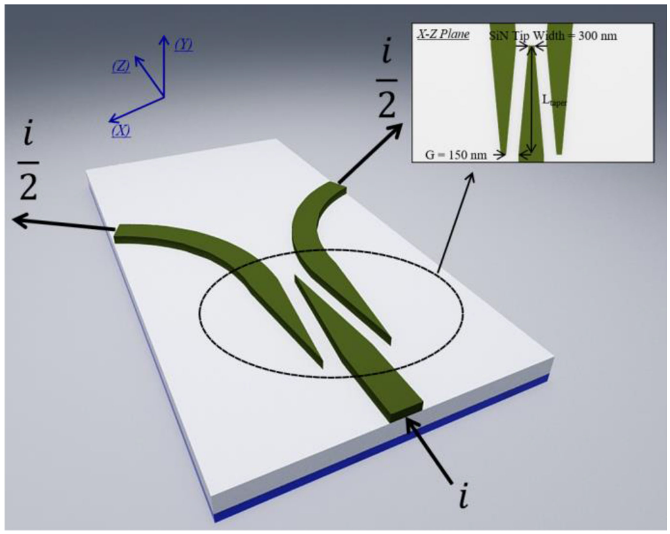


Fig. 5. 3-D schematic of the SiN-based 3-dB power splitter (directional coordinates are indicated). Inset illustrates the X-Z plane of the power splitter.

with the bend-loss test structures (No. of SiN bends = 12, 24, 36, 72); micrograph images when R = 40 $\mu$m are shown in Fig. 4(b). With the wavelength of the light source fixed at 1970 nm, the bending loss per 90° bend is measured to be 0.30 and 0.13 dB when R = 30, 40 $\mu$m respectively (Fig. 4(c)–(d)). As illustrated in Fig. 4(a), there is a close match between experimental and simulated results.

## 3. Highly Efficient 3-dB SiN Power Splitter

The 3-D schematic of the SiN 3-dB power splitter is illustrated in Fig. 5; coordinates are indicated. The power splitter consists of tapering a single-mode TE waveguide (Cross-section = $1.2 \times 0.4\ \mu m^2$), which will be inserted between 2 identical tapers; the 2 output tapers will expand to 2 single-mode TE waveguides, each carrying half of the initial input power ($\frac{i}{2}$).

Through the design methodology elaborated in our previous work [25], the tip width ($W_{tip}$), gap (G), taper length ($L_{taper}$) are designated to be 0.3, 0.15 and 12 $\mu$m respectively. The 3-dB splitter is compact, with a footprint of $3 \times 12\ \mu m^2$. With the design parameters, the electric-field distribution in the X-Z plane is shown in Fig. 6(a); the lightwave in the TE polarization travelling along the input taper will be enhanced in G and coupled into the 2 output tapers. 3D-FDTD simulation indicates negligible insertion loss and wavelength-independent operation over the maximum tunable range of our light source ($\lambda$ = 1935–1990 nm). As means to characterize the splitting ratio and broadband insertion loss, single-stage and 4-stage testing structures are fabricated; the micrograph of the 4-stage testing structure is shown in Fig. 6(b). The measured normalized transmission spectra at port $T_1$, $T_2$, $T_3$ and $T_4$ is shown in Fig. 6(c). Broadband, wavelength-independent 3-dB power splitting, measured from the 4-stage testing structure is experimentally demonstrated from 1935 to 1990 nm in Fig. 6(d). The measured ratios between the 2 output ports in a single-stage testing structure (Fig. 6(e)) indicates a maximum power imbalance ($Imb_{max}$) of 0.05 dB, validating the splitting ratios obtained from the 4-stage testing structure (Fig. 6(d)). The insertion loss of the 3-dB power splitter is obtained via the following approach.

$$\text{Insertion Loss} = \frac{10\log_{10}\left(\left(\sum_{i=1}^{5} T_i\right)/T_0\right)}{4} \tag{1}$$

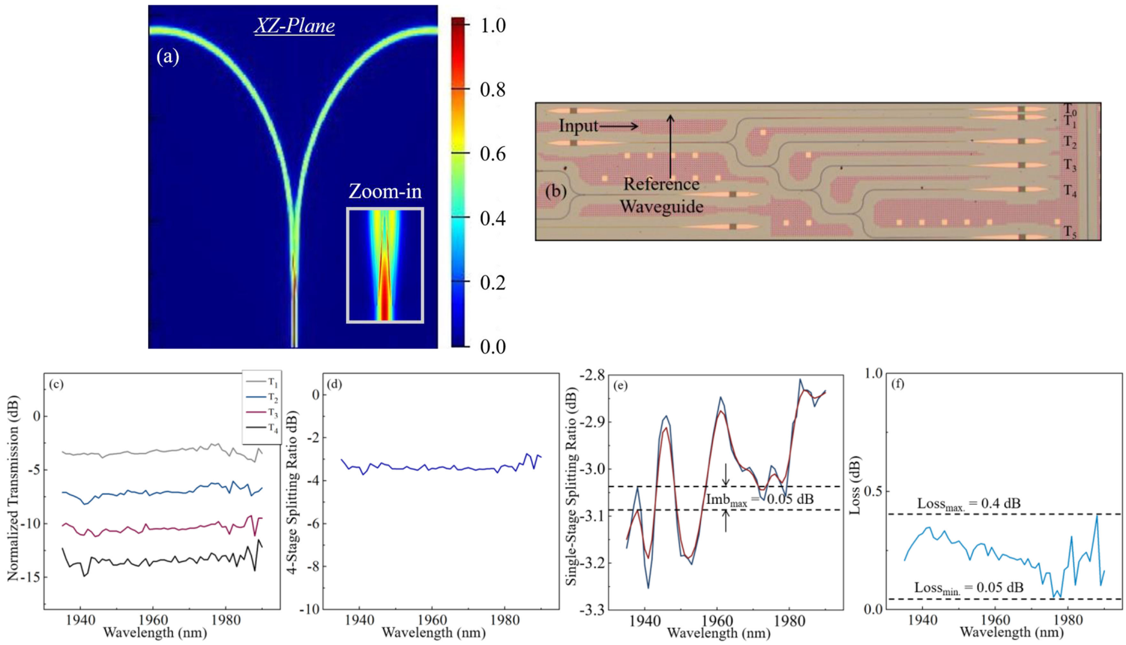


Fig. 6. (a) Electric-field distribution of optimized 3-dB power splitter (X-Z plane). (b) Micrograph image of the 4-stage testing structure; output is labelled for reference. (c) Measured normalized transmission of T1, T2, T3 and T4, obtained from the 4-stage testing structure. (f) Splitting ratio measured from the 4-stage testing structure. (e) Splitting ratio measured from the single-stage testing structure. (e) Experimentally measured 3-dB power splitter broadband insertion loss.

Where $T_{1,2,3,4,5}$ refers to the measured transmission from each of the output ports. $T_0$ refers to the output from the reference waveguide. The factor of ¼ is used in consideration of the 4 stages in the testing structure. Grating coupler insertion loss is factored out via (1). Experimentally determined broadband insertion loss is illustrated in Fig. 6(f); we have characterized a minimum and maximum insertion loss of 0.05 and 0.40 dB from 1935 to 1990 nm respectively. Owing to the field enhancement in G, the insertion loss of the power splitter will be impacted by the extent of sidewall roughness with regards to the taper region [25], [26]. Implementation of the structure on a device layer with moderate index contrast such as SiN will serve to relax processing requirements, thereby, significant reduction in device loss can be achieved as shown in this work.

## 4. Si-SiN Adiabatic Interlayer Coupler

In order to enable low-loss adiabatic transition from the Si to the SiN device layers, a Si-SIN push-pull taper with 300 nm $SiO_2$ gap between the 2 device layers is utilized (Fig. 1). The tip width of the Si and SiN tapers are determined to be 150 and 300 nm respectively (Fig. 1, inset) in consideration of process limitations. Through the eigenmode expansion method, we determine that low-loss adiabatic transition between the Si (Cross-section $= 0.6 \times 0.22\ \mu m^2$) and SiN (Cross-section $= 1.2 \times 0.4\ \mu m^2$) device layers can be achieved when the taper length ($L_{i-c}$) exceeds 40 $\mu$m (Fig. 7a) at $\lambda = 1970$ nm. Bandwidth simulation indicates that the adiabatic interlayer coupler is capable of wavelength-independent operation over the maximum tunable range of our light source. Fig. 7(b)–(f) shows the mode evolution of the of the electric-field distribution in the X-Y plane as the lightwave propagates along a 40 $\mu$m-long Si-SiN adiabatic interlayer coupler. The electric-field distribution of the interlayer coupler ($L_{i-c} = 40\ \mu$m) in the Y-Z plane is illustrated in Fig. 7(g). $L_{i-c} = 20$, 40, 60 $\mu$m-long test structures with 12, 24, 36 and 48 Si-SiN transitions are fabricated; micrograph images are indicated in Fig. 7(h). Via the testing structures, the insertion loss per Si-SiN transition

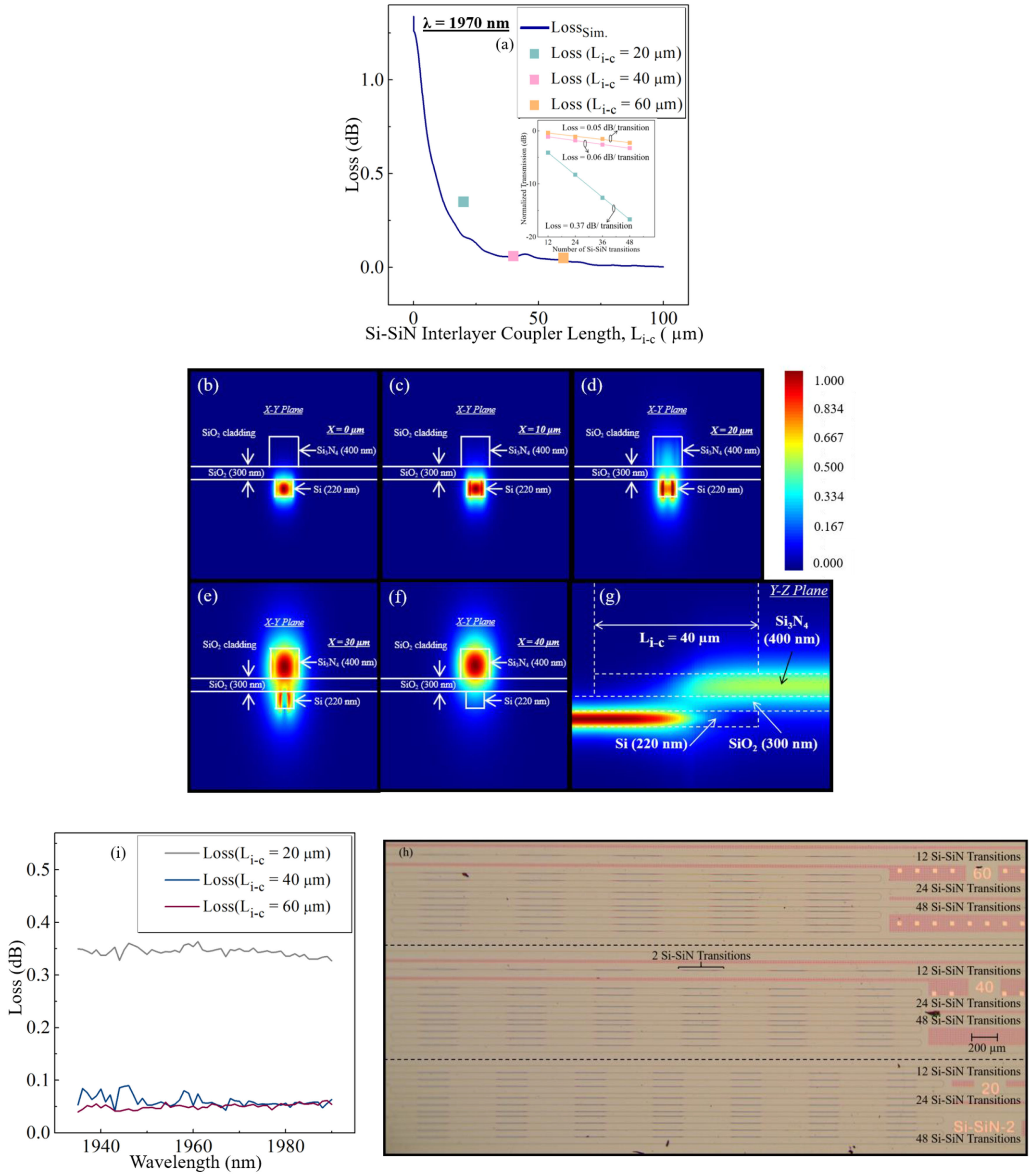


Fig. 7. (a) Simulated insertion loss of the Si-SiN adiabatic interlayer coupler ($\lambda = 1970$ nm). The 3 data points corresponds to the measured insertion loss of the Si-SiN adiabatic interlayer coupler when $L_{i-c} =$ 20, 40 60 $\mu$m ($\lambda = 1970$ nm). (b)–(f) Evolution of electric-field distribution (X-Y plane) as the lightwave propagates along a 40 $\mu$m-long coupler, X = 0, 10, 20, 30, 40 $\mu$m (refer to the coordinates indicated in Fig. 2) (g) Electric-field distribution of the lightwave as it propagates along a 40 $\mu$m-long coupler. (h) Micrograph images of coupler test structures with $L_{i-c} = 20$, 40 60 $\mu$m and 12, 24, 48 Si-SiN transitions. (i) Measured insertion loss as a function of wavelength.

are measured to be 0.37, 0.06, 0.05 dB for $L_{i-c} = = 20$, 40, 60 $\mu$m respectively when $\lambda = 1970$ nm (Fig. 7(a)). Following, the light source is swept from 1935 to 1990 nm characterize the broadband insertion loss of the Si-SiN adiabatic interlayer coupler. Fig. 7(i) demonstrates low-loss operation from 1935 to 1990 nm; maximum and minimum transition loss is found to be 0.06 and 0.04 dB respectively when $L_{i-c} = = 60$ $\mu$m. The experimental data in good agreement with modelling.

## 5. Conclusion

In this work, we extend the CMOS-compatible Si-SiN platform to the 1.9 $\mu$m wavelength region. Broadband (1935–1990 nm), low-loss, Si-SiN interlayer coupler (Insertion Loss = 0.04 dB per Si-SiN transition) and SiN 3-dB power splitter (Insertion Loss = 0.05 dB) are realized. Favorable waveguide propagation loss as low as 2.32 dB is obtained. The extent of radiation loss on bending radius is characterized. While the interest in silicon photonics near 1.9 $\mu$m are ongoing, this letter can act as a basis for future developments at the 1.9 $\mu$m wavelength region on the Si-SiN platform.

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