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FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Electronics and Computer Science

ULTRA LOW POWER CMOS MEDIUM FREQUENCY POWER COLLECTION AND COMMUNICATION CIRCUITS FOR REMOTE SENSOR NODES

by

Teerasak Lee

Thesis for the degree of Doctor of Philosophy

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ABSTRACT

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This thesis presents investigations into a system for the delivery of power and data to low power remote sensor nodes by means of a wide area magnetic inductive coupling, and describes the design and measurement of the essential receiver circuits fabricated in CMOS IC technology. Remote sensors applications require a long-life power supply and data information from the source in order to properly function. An inductive loosely coupled system, in which electromagnetic energy transmitted from the source is collected by many receivers, is a potential candidate for providing a power source and a channel for essential node control data. Moreover, the sensor network can be accurately synchronised by transmitting the modulated timing information carrier to the receivers which removes the risk of data collision, omitting the need for a high accuracy real-time clock in the remote node and its associated power drain. However, the received voltage at the secondary coil may not be sufficient to overcome transistor thresholds and activate the system and begin power transfer. Thus, a rectifier that can operate under the very low input voltage and a high quality factor inductor-capacitor receiver coil are required to maximise the operating range with a reliable start-up voltage. Since the bandwidth of the receiver coil is narrow due to its high quality factor characteristic, an accurate resonant frequency tuning system is needed to optimise the received voltage. Moreover, a phase-shift-keying modulation scheme is chosen for the data transmission since the carrier amplitude and frequency are ideally constant. However, the high quality factor behaviour of the receiver coil distorts the phase-shift-modulated carrier which leads to the failure of the data extraction if the receiver employs a conventional demodulator. A slow phase-shift-keying demodulator is

needed to ensure that the data is extracted without an error when a high quality factor characteristic issued in the signal path.

The design presented in the thesis is an inductive loosely coupled energy harvesting and data demodulation receiver used for wide area wireless sensor network applications. A CMOS rectifier/receiver that can operate with the input voltage below the MOS threshold value with a medium frequency range and provide a DC output voltage delivered to the sensor node load for local storage in a battery or capacitor. In addition, the proposed receiver can extract data from slow phase-shift-keying modulation present on the powering signal. Furthermore, the resonant frequency tuning circuit is implemented to ensure that the receiver operating frequency is matched to the incoming frequency to maximise the received voltage.

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DECLARATION OF AUTHORSHIP

I, Teerasak Lee, declare that this thesis entitled

Ultra low power CMOS medium frequency power collection and communication circuits for remote sensor nodes

and the work presented in it are my own and has been generated by me as the result of my own original research.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;

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Date:.....

List of Publications

Direct project publications:

1. T. Lee, H. R. B. Kennedy, R. A. Bodnar and W. Redman-White, “A CMOS MF energy harvesting and data demodulator receiver for wide area low duty cycle applications with 230 mV start-up voltage,” *2016 IEEE Nordic Circuits and Systems Conferences (NORCAS)*, Copenhagen, 2016.
2. T. Lee, H. R. B. Kennedy, R. Bodnar, J. B. Scott and W. Redman-White, (2016). “Wireless power and network synchronisation for agricultural and industrial remote sensors using low voltage CMOS harvesting and data demodulator IC”, In Proceedings of the *22nd Electronics New Zealand Conference*. Victoria University of Wellington, Wellington, New Zealand, 2016.
3. T. Lee., H. R. B. Kennedy, R. A. Bodnar and W. Redman-White, “A CMOS MF energy harvesting and data demodulator receiver for wide area low duty cycle applications with 230 mV start-up voltage,” in *Analog Integrated Circuits Signal Processing*, 2017.
4. T. Lee, H. R. B. Kennedy, R. A. Bodnar and W. Redman-White, “An MF energy harvesting receiver with slow QPSK control data demodulator for wide area low duty cycle applications”, *ESSCIRC 2018 – IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, Dresden, 2018.

Related publications:

5. H. R. B. Kennedy, T. K. Lee, R. A. Bodnar and W. Redman-White, "Continuous tuning of inductive link antennae with zero voltage switched fractional capacitance," *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Abu Dhabi, 2016.
6. W. Redman-White, H. Kennedy, R. Bodnar and T. Lee, "Adaptive Tuning of Large-Signal Resonant Circuits Using Phase-Switched Fractional Capacitance," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2017.
7. H. Kennedy, R. Bodnar, T. Lee and W. Redman-White, "22.1 A self-tuning resonant inductive link transmit driver using quadrature-symmetric phase-switched fractional capacitance," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, CA, 2017.
8. H. Kennedy, R. Bodnar, T. Lee and W. Redman-White, "A Self-Tuning Resonant-Inductive-Link Transmit Driver Using Quadrature Symmetric Delay Trimmable Phase-Switched Fractional Capacitance," in *IEEE Journal of Solid-State Circuits*, June 2018.

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Chapter 1: INTRODUCTION

1.1 Motivation

Remote sensors for industrial, agricultural and environmental applications demand a long-service lifetime and require a power source that can maintain operation over these periods. However, these applications are often installed in locations where the replacement of the battery is difficult and expensive. For example, multiple sensor nodes installed on a farm to measure the moisture content of the soil may be in locations where changing the battery of each node is occasionally needed, but is hard to achieve in practice. To meet such needs, many designs for ultra-low power circuits and energy harvesting have been published that enable the potential of battery-less applications where battery replacement needs to be avoided.

Scavenging from ambient energy in various environments is challenging since the available energy might not be sufficient for the device to operate [1, 2]. Hence, many energy harvesting applications alternatively harvest from a dedicated electromagnetic source. Example [3] demonstrates a near-field magnetic power transfer where an external power source is used to transmit the energy. In addition, RF energy harvesting is widely used in several radio-frequency identification (RFID) applications where the passive RFID tags harvest the energy from the reader [4]. Therefore, a self-powered receiver that harvests energy from a dedicated magnetic or RF energy source is a potential candidate to replace battery-powered wireless sensor nodes.

Since the energy harvested from an RF energy source or a loosely coupled magnetic wireless link is typically a few µW, a specific circuit that can operate with the ultra-low power consumption is inevitably needed to increase the distance between the transmitter and the receivers. The inductive link coverage area can be extended by using a high-quality factor (Q) narrow-bandwidth resonant inductor-capacitor (LC) circuit. Moreover, reducing the active duty cycle of the receivers can significantly reduce the average power consumption. Although the design of an ultra-low power circuit with the reduced active duty cycle of the receiver can effectively reduce the minimum received energy requirement, the received AC voltage may be insufficient to be converted to DC voltage due to the limited sensitivity of conventional rectifier circuits [5]. Hence, proper designs of the rectifier for supplying the device are needed.

System synchronisation between a transmitter and multiple receivers is needed in order to permit the battery-less remote sensor nodes to only be active at a certain period and avoid the data collisions which occur from simultaneously transmitting the collected data back to the source from

two or more receivers. Thus, the sensor nodes require precise timing information to enable the precise system synchronisation. The accurate timing information can be obtained by either using a high accuracy real-time-clock circuit or transmitting the information modulated with the carrier energy signal from the source to the receivers. The data modulation scheme is preferable due to less power consumption [4, 6, 7]. However, the demodulation of the data in the receiver is not straightforward. A simple amplitude-shift-keying (ASK) demodulation technique, which has power consumption, is not suitable for this work since the average power delivery at the receiver is reduced as the amplitude is shifting according to the data. Moreover, a frequency-shift-keying (FSK) demodulation technique is not appropriate either, since the receiver in the near-field electromagnetic harvesting system has a narrow bandwidth, and deviation from the frequency for optimum power should be avoided. Therefore, a simple phase-shift-keying (PSK) demodulation system with low power consumption is needed.

This work addresses those issues by considering the use of medium frequency (MF) magnetic power delivery from a dedicated distributed antenna system where the application is used for wireless sensor nodes on a farm for agriculture use or in an industrial setting. In addition, the energy harvesting system in this work also allows network timing to be efficiently controlled by extracting the data along with the received energy using the PSK demodulation technique. Moreover, the design of a high sensitivity rectifier and the ultra-low power management for powering the system is demonstrated to deliver operation at longer range from the transmitting antenna system.

1.2 Research Goals and Contributions

The goal of the research is to design and implement a system of battery-less energy harvesting devices that are wirelessly powered by electromagnetic energy from a remote power source. The devices harvest energy from the environment and deliver the power to the remote sensor nodes. Moreover, these devices can also extract data and timing information transmitted from the source to enable communication and synchronisation between a transmitter and multiple receivers without the need for a continuously active real-time-clock.

The proposed system is intended to be used in an area such as a farm or an industrial site where the area could be typically around 100x100m^2. Sensor nodes would be placed in different locations within the field, in locations prohibitive to other power supply methods, and could wirelessly harvest energy and receive instructions from the transmitter.

The design and fabrication of the full custom integrated circuits are undertaken in an 180nm standard CMOS process, available from the Europractice foundry service. This 180nm process is selected, instead of a shorter length CMOS process, as the digital complexity and high bandwidth

switching speed available in more costly smaller geometry processes are not needed for this system. Moreover, smaller geometry processes often have larger off-state leakage that would seriously affect the performance of circuits integrated for a nano-ampere current level. The performance of the energy harvesting functions will be directly affected by the threshold voltage (V_{th}) of the transistors in the chosen process, and those in this 180nm CMOS are suitable for this application. In addition, this project is restricted by the choice of technology shared with another project which means that a near-zero V_{th} process is not an option, although such a process could potentially yield better performances of the energy harvesting circuit.

The following list highlights the research contributions that address these goals.

- Design the MF electromagnetic energy transfer system for wide area wireless sensor network applications with two prototype ICs.
- Design an integrated CMOS switch-over subthreshold voltage rectifier capable of cold starting with the applied input voltage at 200mV which is less than the MOS transistor threshold, and with the switch-over detection circuit to maintain efficient operation (1st prototype IC).
- Design an ultra-low power data extraction system for extracting the phase data modulation (1st prototype IC).
- Design of a segmented rectifier capable of cold starting and with the efficiency adaptive re-configuration over a wide range of input voltage (2nd prototype IC)
- Design an ultra-low power phase data demodulator for extracting the low-speed, slow phase shift modulated data from the MF electromagnetic energy transfer (2nd prototype IC).

All of the work described in this thesis has been done solely by the author, except for the assistance stated in the acknowledgements. In addition to the original contributions by the author, basic ideas developed from several proposed works are given in cited references.

Chapter 2: LITERATURE REVIEW

In this chapter, literature reviews on energy harvesting and data communication are examined. As stated in the previous chapter, this research aims to design a receiver that harvests energy and extracts data from an electromagnetic power source for a remote sensor network for agriculture or industry. Hence, the chapter describes the background of wireless energy harvesting. Furthermore, the principles of an inductively coupled system, including the transmitter and receiver antennas are studied.

2.1 Energy Harvesting Overview

In an environment where various forms of energy such as light or radio frequency waves are present, ambient energy can be extracted and converted into electrical energy. This energy extracting method is called energy harvesting or scavenging. Energy harvesting provides an appealing solution for supplying energy to embedded devices, such as implantable medical devices (IMD) and wireless sensor nodes, where an energy source is required for a long operational lifetime. Compared to the conventional solution where embedded devices are powered by a battery, the capacity of the battery cell is limited and the replacement of the depleted battery may be very inconvenient. Moreover, devices with sufficient battery power for a long operating time may require a larger volume, which might not be practical for remote sensor nodes and IMD.

Several forms of energy extraction by scavenging can be provided from electromagnetic waves, light, heat and vibration. A standard photovoltaic (PV) cell can generate approximately 100mW/cm^2 under bright sunlight and 100µW/cm^3 in an illuminated office [2]. Measurements from Matthews et al. shows that 4mW of power can be harvested by a credit-card-sized PV device in an indoor bright light condition [8]. Heat waste dissipated from machinery in an industrial plant or a small thermal gradient from the human body can be converted into energy by a thermoelectric generator (TEG). A report from Paradiso and Starner [2] states that 60µW/cm^2 can be generated from a TEG in wearable applications. Mechanical vibration from an object such as machinery or a human body can produce energy by means of piezoelectric materials, electrostatic capacitive charging or electromagnetic energy transducers [9]. Ambient radio frequency (RF) waves generated by a cellular base station can typically provide a 1µW/cm^2 to an antenna with the maximum operating distance of 2.5m [10]. Table 2.1 compares the energy harvesting capability of various sources [2].

From Table 2.1, it can be seen that ambient light provides the highest energy density compared to other energy harvesting sources, although with the disadvantage that the available energy is

inconsistent and may fluctuate rapidly. Scavenging energy from heat and vibration may supply stable energy with moderate power density, but on the other hand, a dedicated source such as machinery or a human body is required for each embedded device. Despite the lower energy density powered by an ambient RF wave, the energy can be distributed to multiple devices. Moreover, digital data can also be modulated with the RF wave to enable data communication between the source and the energy harvesting receiver if the receiver is harvesting energy from a dedicated source instead of a base station [6, 7, 11, 12]. An energy harvesting receiver can therefore benefit from having a communication channel as the source can send a *sleep* command to deactivate the receiver in order to reduce the average power consumption of the receiver.

Table 2.1 Energy harvesting capabilities (Table from [2]).

Energy Source	**Performance**
Ambient radio frequency	< 1μW/cm^2 (VHF and UHF band)
Ambient light	100mW/cm^2 (directed toward bright sun) 100μW/cm^2 (illuminated office)
Thermoelectric	60μW/cm^2
Vibrational microgenerators	4μW/cm^3 (human motion-Hz) 800μW/cm^3 (machines-kHz)

As electromagnetic wave energy harvesting is attractive due to the availability of the power distribution to multiple devices and the communication between the source and the receivers, several studies have emphasised far-field RF energy harvesting systems [11-14] or near-field magnetic coupled [3, 6, 15, 16]. However an RF energy harvester operating in the ultra-high-frequency (UHF) band suffers from significant energy loses, such as path loss due to the absorption from walls, or voltage drop from parasitic components [17-19]. While the magnetically coupled energy harvesting system is not affected by such losses since the system is operating at a lower frequency typically below 15MHz, a much larger antenna size is needed for both transmitter and receiver.

Since our work is focusing on a remote sensor network for agricultural or industrial sites, energy harvesting from a dedicated magnetic field is an appropriate solution, since the source must distribute consistent energy to multiple sensors. Moreover, the medium frequency (MF) range (300kHz to 3MHz) is selected for the energy source in order to wirelessly transfer the energy at a relatively large area since the free space path loss is proportional to the frequency [20], and the near-field operating region associated with the transmitting source can be quite large. While the MF band is currently still in use for broadcasting, this is declining and national regulators are opening up this part of the spectrum to some experimentation in very narrow segments [21]. In

addition, the power source can transmit control and timing information to sensor nodes by modulating the data with the magnetic field.

2.2 Medium Frequency Inductive Coupled Energy Harvest

Wireless energy transfer based on near-field magnetic/inductive coupling technique has been extensively used in radio frequency identification (RFID) [4] and wireless implantable medical devices (IMD) [7]. A device can be wirelessly powered by utilizing the magnetic flux loosely coupled between two conductive coils. Figure 2.1 illustrates a model of the proposed MF inductive coupled energy harvesting system. A large loop primary coil, excited by an AC voltage source, generates the time-varying magnetic field. A secondary coil, located within the area under the primary coil, is coupled by the magnetic flux. In consequence, an electromotive force is induced in the secondary coil [22]. As stated in Chapter 1, the application is designed for a sensor network used on a farm or industrial site. A square loop antenna is shown for the primary coil since the loop is probably used in a square or rectangular area defined by the boundaries of a field or an industrial site, and running a conductor around the boundary would be by far the most convenient installation. Furthermore, selecting one large loop, compared with multiple loop antennas for power transmission, is less complex. Only one transmitter circuit is required for a loop antenna, while the synchronisation issues required between multiple transmitters for multiple loop antennae can be avoided.

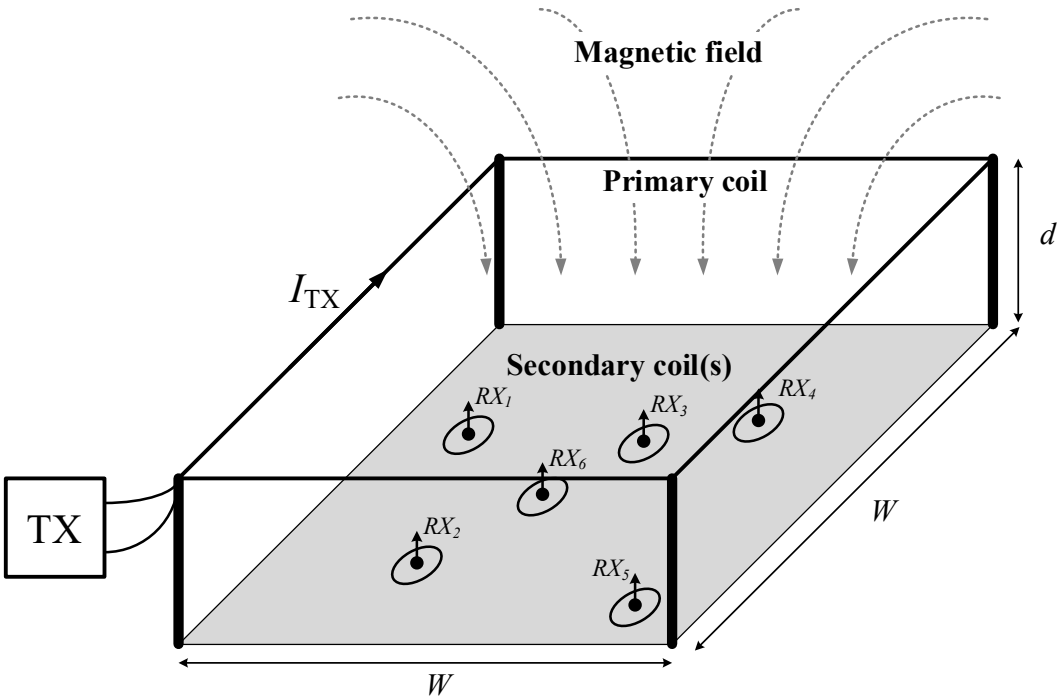


Figure 2.1 Model of MF inductively coupled energy harvesting system.

The MF loosely coupled inductive energy harvesting system can be modelled as an equivalent circuit, as depicted in Figure 2.2. The circuit consists of Ohmic losses R_1 and R_2, self-inductance L_1 and L_2 of the coils and a mutual inductance M_{12} between two coils. From the equivalent circuit

model of the inductive coupling, the relations between voltage and current in the frequency domain can be expressed as

$$V_1(j\omega) = R_1 I_1(j\omega) + j\omega L_1 I_1(j\omega) + j\omega M_{12} I_2(j\omega), \quad (2.1)$$

$$V_2(j\omega) = R_2 I_2(j\omega) + j\omega L_2 I_2(j\omega) + j\omega M_{21} I_1(j\omega), \quad (2.2)$$

where ω is the operating frequency of the system. According to equation (2.2), it is evident that the voltage at the secondary coil (V_2) is generated due to the magnetic coupling between two coils (M_{12}). On the other hand, the voltage at the primary coil (V_1) is affected by the loading current of the secondary coil (I_2). Note that the loading current I_2 that affected the primary coil voltage V_1 is negligible in the loosely coupled inductive links since the value of M_{12} is very small [16].

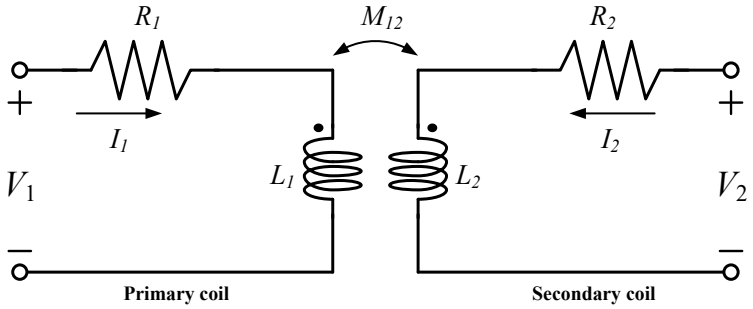


Figure 2.2 Equivalent circuit model for the inductive link coupled between two coils.

From equation (2.1), the equivalent load when multiple secondary coils are placed within the transmitter coil is

$$R_{eq,RX} = j\omega M_{12} I_2 n_{RX}, \quad (2.3)$$

when n_{RX} is the number of secondary coils. Since the magnetic field strength is proportional to I_1 which will be shown later, it is desirable to ensure that the loading resistance due to the multiple secondary coils ($R_{eq,RX}$) does not reduce the primary coil current. Hence, the maximum number of secondary coils used for harvesting the magnetic energy without affecting the primary coil current can be derived by approximating $R_{eq,RX}$ to be much smaller than the primary coil resistance R_1 as

$$R_{eq,RX} = 0.01 * R_1. \quad (2.4)$$

$$n_{RX,MAX} = \frac{R_1}{100 * R_{eq,RX} \omega M_{12} I_2}. \quad (2.5)$$

2.2.1 Self-inductance and Mutual Inductance

The self-inductance L_1 and L_2 from Figure 2.2 is defined by a ratio of the total magnetic flux (ψ) in an enclosed surface of the primary coil to the current which flows in the primary coil (I) [4, 22] which can be expressed as

$$L = \frac{\psi}{I}. \quad (2.6)$$

The total magnetic flux is given by [22]

$$\psi = \mu NHA\,, \tag{2.7}$$

where μ is the permeability of the space in an area of the enclosed surface of the coil, *N* is the number of turns of the coil, *H* is the magnetic field strength and *A* is the area of the enclosed surface of the coil. The mutual inductance *M* from Figure 2.2 occurs when a current is induced by the magnetic flux generated by the primary coil which can be expressed as [22]

$$M_{21} = \frac{\psi_{21}}{I_1}\,, \tag{2.8}$$

where M_{21} is the mutual inductance of the secondary coil excited by the primary coil and ψ_{21} is the total magnetic flux generated by the primary coil that flows through the enclosed surface area of the secondary coil. In addition to the primary coil, the mutual inductance also occurs due to the current that flows in the secondary coil and the magnetic flux coupling in the primary loop. Hence, the mutual inductance is

$$M = M_{12} = M_{21}\,. \tag{2.9}$$

The mutual inductance, which expresses the coupling between two coils, can be normalised in order to intuitively describe the effect of the magnetic coupling between two coils. Therefore, the coupling coefficient *k* is introduced and can be expressed as

$$k = \frac{M}{\sqrt{L_1 L_2}}\,. \tag{2.10}$$

The value of the coupling coefficient of the inductive coupling between two coils is between 0 and 1 (or 100%). In practice, the coupling coefficient of the loosely inductive links for each of the sensor nodes in the proposed system is lower than 0.01 (or 1%) since the size of the secondary coil will be much smaller than the primary coil [16].

2.2.2 Coil Characteristics

The magnetic strength and the inductive coupling coefficient described in section 2.2.1 are dependent on the coil characteristics. In this section, the coil characteristics of both primary and secondary coils that are used in this work are studied. A square single turn loop coil antenna, which is suitable for the practical applications envisaged as mentioned earlier, is chosen for the primary coil, while a ferrite rod antenna is chosen for the secondary coil. The ferrite rod antenna is selected to harvest the wireless energy due to its high Q-factor and its small size. More details are described in the following sections.

2.2.2.1 Square Loop Antenna

A square loop antenna is one of the common structures for a loop antenna. Figure 2.3 illustrates the geometry model of a square loop antenna placed on the origin. From the Biot-Savart law [22], the magnetic field is generated when current is flowing in the loop wire. The magnetic field vector at an arbitrary point of a square loop coil is given by (2.11) [15, 23]. W is half of the length on one side of the loop antenna and I_{TX} is the current flowing in the loop antenna. The derivation of equation (2.11) can be found in Appendix B. It can be seen that the vector of the magnetic field generated by the current flowing in a square loop coil is only in the z-axis, which means that the secondary coil needs to align in the same angular orientation with the primary loop coil to receive the maximum magnetic flux (as shown in Figure 2.1). Moreover, the field strength of the loop is proportional to the transmitter current.

$$
\begin{aligned}
H_z(x,y,z) = \frac{I_{TX}}{4\pi} \cdot \Bigg\{ & \frac{-(y-W)}{(y-W)^2+z^2} \cdot \left(\frac{x+W}{\sqrt{(x+W)^2+(y-W)^2+z^2}} + \frac{-x+W}{\sqrt{(-x+W)^2+(y-W)^2+z^2}} \right) \\
& + \frac{(x+W)}{(x+W)^2+z^2} \cdot \left(\frac{y+W}{\sqrt{(x+W)^2+(y+W)^2+z^2}} + \frac{-y+W}{\sqrt{(x+W)^2+(-y+W)^2+z^2}} \right) \\
& + \frac{(y+W)}{(y+W)^2+z^2} \cdot \left(\frac{-x+W}{\sqrt{(-x+W)^2+(y+W)^2+z^2}} + \frac{x+W}{\sqrt{(x+W)^2+(y+W)^2+z^2}} \right) \\
& - \frac{(x-W)}{(x-W)^2+z^2} \cdot \left(\frac{-y+W}{\sqrt{(x-W)^2+(-y+W)^2+z^2}} + \frac{y+W}{\sqrt{(x-W)^2+(y+W)^2+z^2}} \right) \Bigg\}.
\end{aligned}
\qquad (2.11)
$$

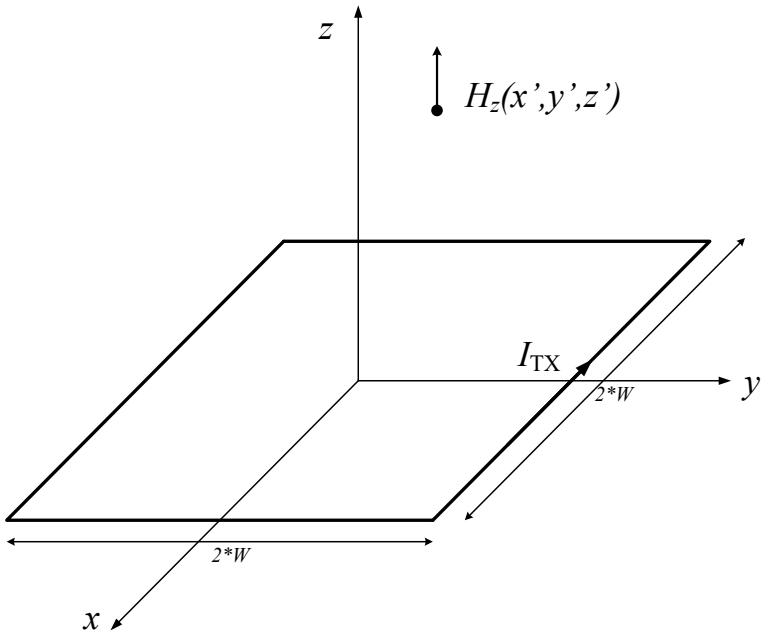


Figure 2.3 Model of a square loop antenna.

Considering the equation (2.11) for the magnetic field in the centre of the loop (x=0 and y=0) with the distance d along the Z-axis, the equation is simplified to

$$H_z(0,0,d) = \left(\frac{2I_{TX}}{\pi}\right)\left(\frac{W^2}{\left(W^2+d^2\right)\sqrt{d^2+2W^2}}\right). \quad (2.12)$$

In this project, the chosen width W is much larger than the distance d. Hence the magnetic field when $W^2 \gg d^2$ and $2W^2 \gg d^2$ can be approximated to

$$H_z(0,0,d) \approx \left(\frac{2I_{TX}}{\pi\sqrt{2}*W}\right). \quad (2.13)$$

The equation (2.13) implies that the distance between the magnetic field strength and the loop is not affecting the magnetic field strength when the width is much greater than the distance. Further, the field strength is inversely proportional to the width of the loop coil. In this project, a square loop antenna is constructed in a large horizontal square area where the side width is between 10m to 100m, while the vertical (i.e., z-axis) distance between the primary coil and secondary coil would typically be between 0m and 2m. Therefore, the reduction of the magnetic field along the distance should not significantly affect the received power at the secondary coil. Note that the vertical distance is selected such that the magnetic field distortion due to the earth is minimised [24-26] if the secondary coils are placed on the ground.

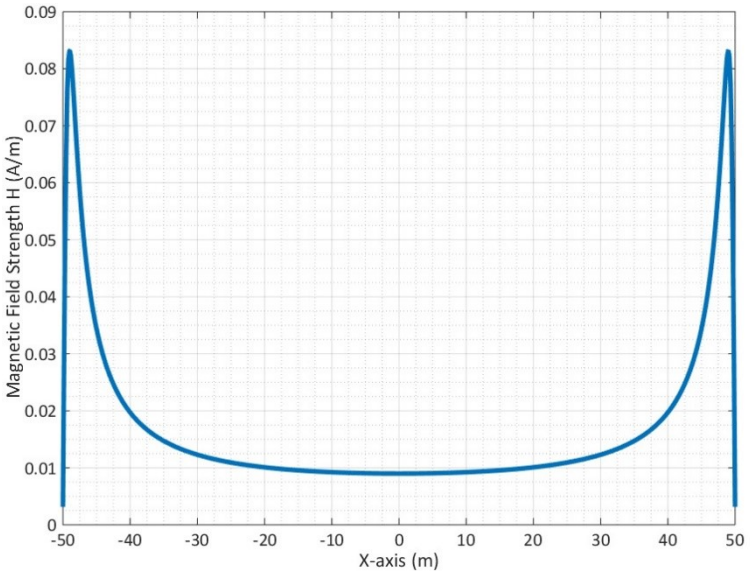


Figure 2.4 Magnetic field strength at *z* = 1m and *y* = 0m for the loop antenna with the side width of *2W* = 100m along the x-axis. The current applied in the coil is 1A.

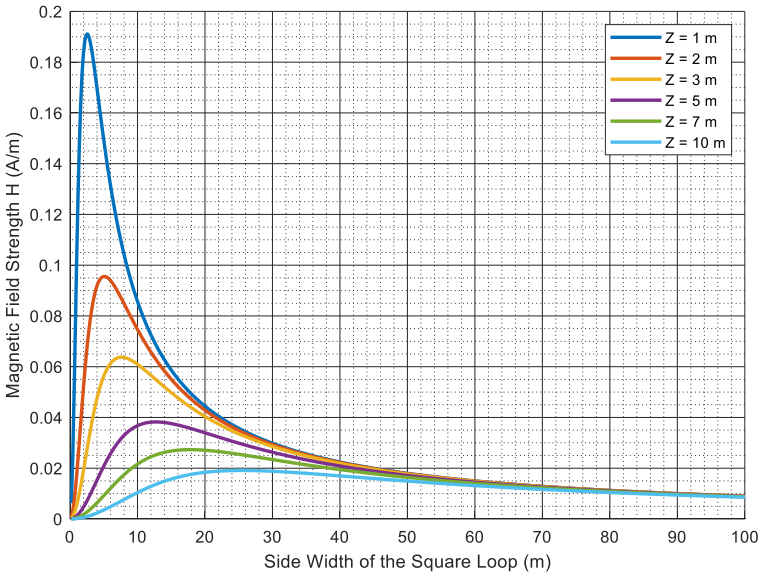


Figure 2.5 The plot of the magnetic field strength at the centre of a square loop antenna (x = 0m and y = 0m) versus the side width of the square loop for different displacements along the z-axis. The current applied in the coil is 1A.

Figure 2.4 plots the magnetic field strength of a square loop antenna of 100m on each side with 1A applied current calculated from equation (2.11) at z = 1m and y = 0m, showing how field strength varies along the x-axis from -50m to 50m. Note that the calculated field is constant as a result of DC passing through the loop, and time-varying field values (as required to generate an induced voltage at the secondary coil) will scale accordingly. It can be observed that the peak of the magnetic field is at the edges inside the square loop. This is because the field strength is inversely proportional to the square of the distance between the point of interest and the conducting wire (or the loop coil) according to the Biot-Savart law [22]. The graph of the magnetic field strength versus the loop antenna side width also varies with different distances along the z-axis is illustrated in Figure 2.5. The magnetic field is calculated at x = 0m and y = 0m when the current of 1A is applied to the coil. It can be seen that the optimum points of the magnetic field strength versus the side width of the loop vary with different distances along the z-axis. Further, it can be seen that the distance that affects the field strength is less impactful when the side width is much larger than the distance, as described earlier.

After the magnetic field of a square loop antenna has been determined, the equivalent circuit of the coil is addressed. Figure 2.6 shows the equivalent circuit of the square loop coil which consists of the square loop loss resistance R_{TX}, and the antenna inductance L_{TX}. Note that the radiation resistance R_{rad} and the internal inductance L_i are omitted since their practical values are negligible compared with their counterpart when the antenna operating frequency is in the MF range. The parasitic elements are given by [27]

$$R_{TX} = \frac{4W}{\pi a}\sqrt{\frac{\omega\mu_0}{2\sigma}}, \quad (2.14)$$

$$L_{TX} = \frac{4W\mu_0}{\pi}\left(\ln\left(\frac{2W}{a}\right) - 0.774\right), \quad (2.15)$$

where *2W* is the side width of the square loop, a is the conducting wire radius, ω is the operating frequency, μ_0 is the permeability of free-space, σ is the conductivity of the wire and λ is the wavelength which is related to the operating frequency ($\lambda = {3 \cdot 10^8}/{f}$). Note that the equations are derived from an assumption that the frequency is very high such that the skin depth of the conductor is very small compared to the cross-section area of the wire. In addition, these equations are valid only when the total length of the square loop antenna is smaller than one-tenth of the free space wavelength λ [4]. Therefore, the maximum operating frequency of the system restricted by the wavelength is given by

$$f_{MAX} = \frac{0.1(l_{TX})}{3\cdot 10^8} = \frac{0.1(4(2W))}{3\cdot 10^8} = \frac{0.8W}{3\cdot 10^8}. \quad (2.16)$$

When l_{tx} is the length of the transmitter antenna (l_{TX} = 4**W*). On the other hand, the minimum operating frequency is constrained by the on-chip coupling capacitor value used in the receiver integrated circuit (IC) since the impedance of the capacitor is inversely proportional to the operating frequency. More details of the on-chip coupling capacitor will be explained later in chapter 3. As a result, the minimum operating frequency is chosen to be at 300kHz.

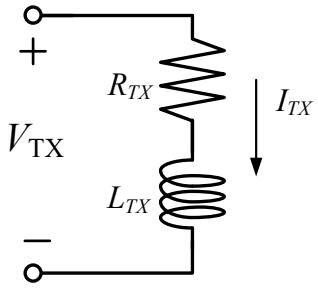


Figure 2.6 Equivalent circuit model of the square loop antenna.

The magnetic field strength of the transmitter loop antenna can be optimised by selecting a small antenna size. However, the minimum size of the antenna is restricted by the wireless sensor network operating distance (e.g., a 70x70m^2 transmitter loop size for a 70x70m^2 operating area of the sensor network). Alternatively, the magnetic field strength of the loop can be increased by increasing the transmitting current, as can be seen in the equation (2.11). In addition, the secondary coil characteristics also affect the received voltage. Hence, enhancing the performance of the loosely coupled inductive system by optimising the design of the secondary coil is an alternative way.

2.2.2.2 Ferrite Rod Antenna

Ferrite rod antennas have been extensively used in broadcast AM radio receivers for several decades [4, 27-29]. The ferrite antenna consists of a loop antenna (the shape is dependent on the ferrite shape) and the ferrite material, as depicted in Figure 2.7. Figure 2.8(a), illustrates the effect of the ferrite rod [30]. By comparing the loop antenna without the ferrite rod and the loop antenna with the ferrite rod, it can be seen that the latter absorbs more magnetic flux through the area within the loop. Therefore, the ferrite rod helps to effectively increase the permeability μ of the secondary coil.

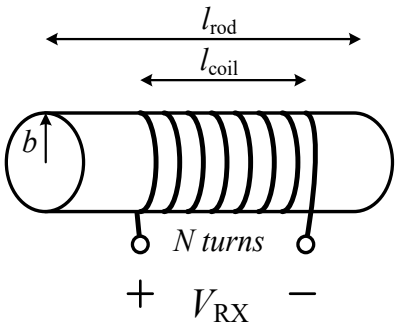
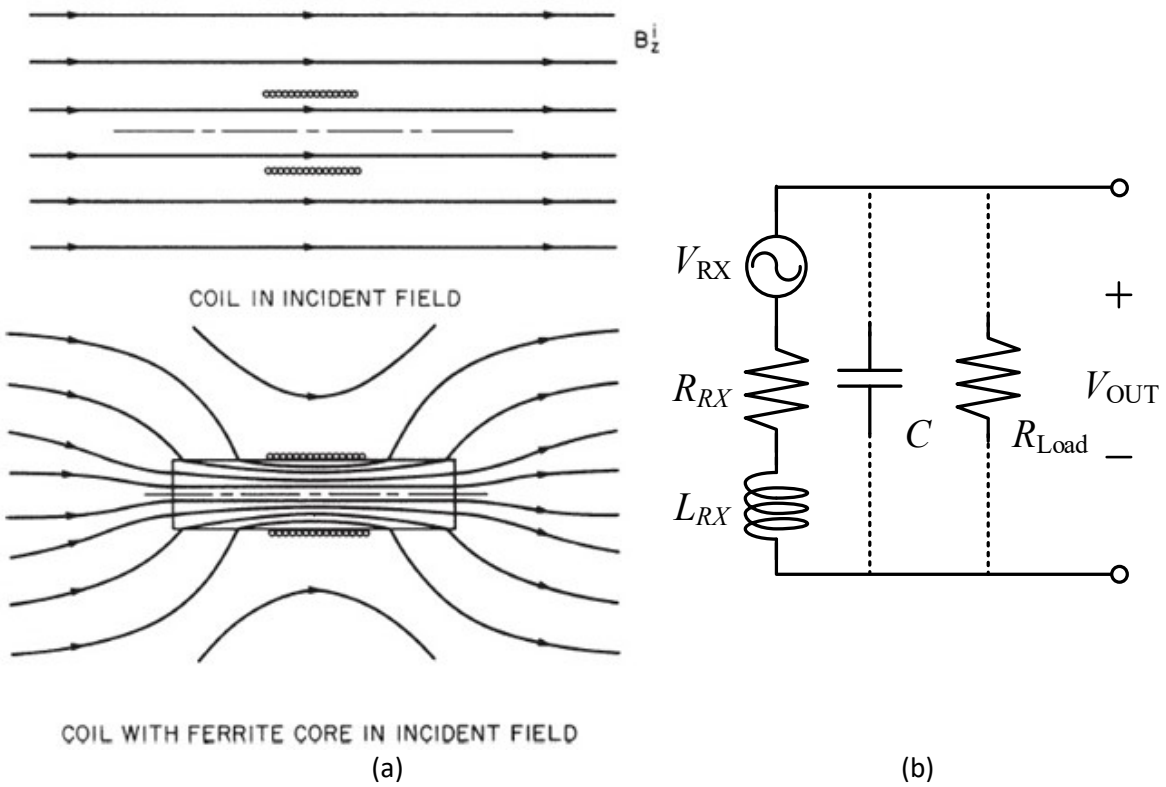


Figure 2.7 Model of a ferrite rod antenna.

The permeability of the ferrite rod is dependent on the initial permeability of the ferrite material and the dimensions of the rod and the coil [30]. Considering the effect on the incident magnetic field depicted in Figure 2.8(a), it can be seen that the magnetic flux along the ferrite rod is maximum at the middle and decreases at the ends of the rod. Hence, a loop coil winding at the middle of the length of the rod could absorb more magnetic flux than a loop coil winding at the end of the length of the rod.

Figure 2.8(b) shows an equivalent circuit of the ferrite rod antenna. By comparing the equivalent circuit of the inductive link in Figure 2.2 to the ferrite rod equivalent circuit in Figure 2.8(b), the induced voltage V_{RX} is related to the mutual inductance M_{12}. Analysing the induced voltage of the secondary coil (V_{IND}) instead of the voltage from the mutual inductive coupling shown in equation (2.1) and (2.2) may be more useful for designing the secondary coil.



(a) (b)

Figure 2.8 (a) The effect of the ferrite rod (Figure from [30].) and (b) equivalent circuit model of the ferrite rod antenna.

The induced voltage due to incident magnetic flux for a ferrite rod antenna is given by [30]

$$V_{IND} = j\omega\mu_{rod} NAB_z , \quad (2.17)$$

where ω is the frequency of the incident magnetic field, μ_{rod} is the relative permeability of the ferrite rod, N is the number of turns of the coil, A is the area of the circular loop ($A = 2\pi b$) and B_z is the incident magnetic field at the ferrite antenna, which is related to the magnetic field strength H as

$$B = \mu_0 H , \quad (2.18)$$

where μ_0 is the permeability of the space. Furthermore, the lumped resistors and inductors shown in Figure 2.8(b) are the loss resistance R_{RX} and the ferrite rod inductance L_{RX} respectively [27, 30]. The expressions of these components are

$$R_{RX} = \frac{Nb}{a}\sqrt{\frac{\omega\mu_0}{2\sigma}} , \quad (2.19)$$

$$L_{RX} = \mu_{rod}\mu_0 N^2 \cdot \frac{A}{l_{coil}} , \quad (2.20)$$

where l_{coil} is the length of the coil, b is the radius of the coil, a is the radius of the loop wire, and σ is the conductivity of the wire.

2.2.3 Resonance

The voltage induced by the magnetic flux from the primary coil V_{RX}, as shown in Figure 2.8(b), can be improved by adding a shunt capacitor at the output terminal of the secondary coil to form a parallel resonant circuit. By applying input voltage at the primary coil with the resonant frequency in the loosely inductively coupled system as

$$\omega_0 = 1/\sqrt{L_{RX}C}, \quad (2.21)$$

the output voltage V_{OUT} is effectively increased by Q times, where Q or quality factor is proportional to the ratio of energy stored to the energy lost per unit time for the sinusoidally excited system [20]. Alternatively, the definition of the Q-factor can also be described as the ratio of a resonant frequency to the bandwidth of a resonant system. By adding the resonant capacitor at the secondary coil, the output voltage is expressed as

$$V_{OUT} = V_{IND}Q, \quad (2.22)$$

where the quality factor of the ferrite antenna is

$$Q = \frac{\omega_0 L_{RX} C R_{Load}}{L_{RX} + C R_{Load} R_{RX}}. \quad (2.23)$$

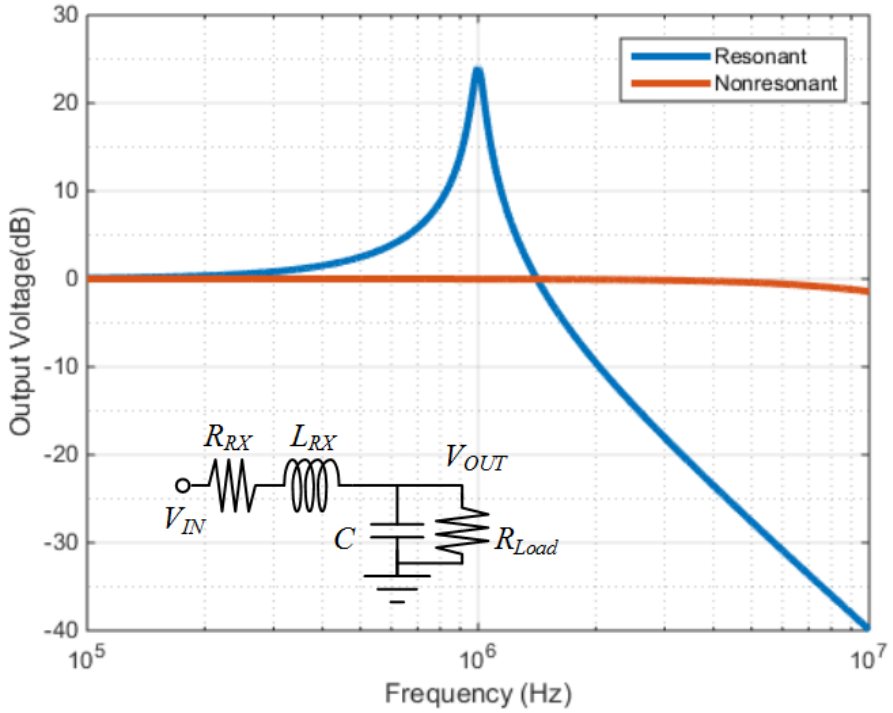


Figure 2.9 Comparison of the normalised voltage across the load (V_{OUT}) between the non-resonant secondary coil and the LC resonant secondary coil. The values of the passive components are L_{RX} = 10µH, C = 100pF, R_{RX} = 1Ω and R_{Load} = 10kΩ.

The derivation of Q is shown in Appendix A. Figure 2.9 shows the simulation result of the non-resonant secondary coil circuit model and the series-LC resonant secondary coil circuit model when the values of the passive components are L_{RX} = 100µH, C = 253pF, R_{RX} = 1Ω and R_{Load} = 10kΩ. From

the figure, the output voltage of the resonant circuit is boosted up to approximately 30 dB when the frequency is operated at the resonant frequency 1MHz. In contrast, the output voltage of a similar ferrite antenna in a non-resonant circuit remains constant at 1V (or 0dB) and gradually decreases when the frequency is greater than 100MHz. In addition, the current I_1 of the primary coil can also be improved by adding an additional capacitor to form an LC resonant circuit similar to the secondary coil.

In addition, the output voltage of the secondary coil can be expressed as a function of the transmitter magnetic field and the receiver coil characteristics by substituting equation (2.17), (2.23) and (2.11) in (2.22), which yields

$$V_{OUT} = \left(\frac{L_{RX} C R_{Load}}{L_{RX} + C R_{Load} R_{RX}} \right) j\omega_0^2 \mu_0 \mu_{rod} NAH_z . \qquad (2.24)$$

While it might seem that the output voltage V_{OUT} can be increased by simply increasing the number of turns N, however the output can possibly decrease if the output load R_{Load} is not sufficiently large. As the inductance L_{RX} is proportional to the square of N, if N is increased such that L_{RX} is much larger than the term $CR_{Load}R_{RX}$ then equation (2.24) can be rewritten as

$$V_{OUT} \cong \left(CR_{Load} \right) j\omega_0^2 \mu_0 \mu_{rod} NAH_z . \qquad (2.25)$$

As a result, the quality factor Q is decreased as the output load is limited by the rectifier (which will be explained in the next chapter). Figure 2.10 depicts the plot of the V_{out} and the ratio of the coil impedance L_{RX} and $CR_{Load}R_{RX}$ when the N is increased with different output load conditions. As expected, the number of turns decreases the output voltage if the output loading resistor is not sufficiently large.

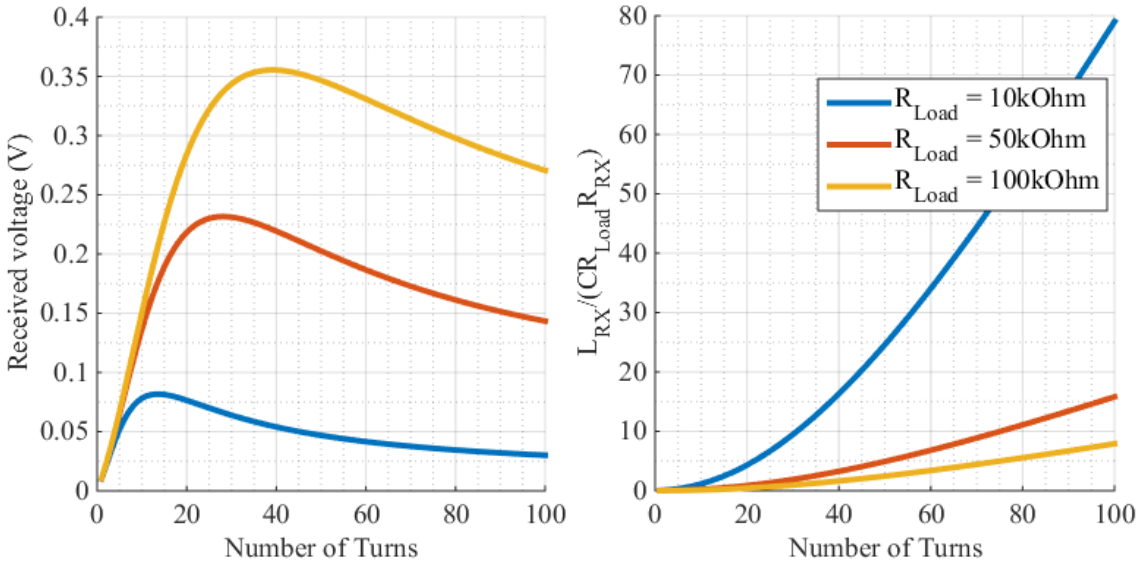


Figure 2.10 The plots of the output voltage V_{OUT} of the secondary coil (left) and the ratio of the coil impedance L_{RX} and $CR_{Load}R_{RX}$ (right) versus the number of turns of the loop antenna with different output load conditions.

2.2.4 Magnetic Coupled Energy Harvest Performance Measures

The power transfer efficiency (PTE) of an inductively coupled system is generally defined as the ratio between the power delivered to the load at the secondary coil R_L and the input power at the source of the primary coil, as shown in Figure 2.11. The PTE, denoted η, is a commonly used indicator of the performance of the design of the power transfer via inductive links. Because our work targets the applications of a remote sensor network with the ability to operate from a cold-start in a wide area, the coupling coefficient between coils is very low. Hence the PTE is limited by the coupling factor [16]. As a result, the optimisation of harvested energy and start-up voltage takes priority over the optimisation of the PTE. However it is still useful to investigate the PTE of the inductively coupled energy harvesting system.

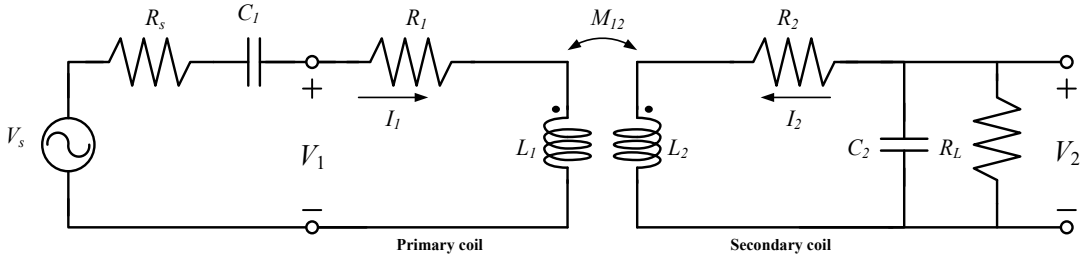


Figure 2.11 Equivalent circuit model of the inductive coupled wireless power transfer.

From Figure 2.11, the PTE is given by

$$\eta \cong k^2 Q_{TX} Q_{RX} . \qquad (2.26)$$

The derivation of the efficiency is shown in Appendix A. It can be seen from equation (2.26) that the PTE is dependent on the coupling coefficient (*k*), and Q-factors of both the primary and secondary coils. As the coupling coefficient of the loosely inductively coupled system is practically lower than 1% [16], the PTE is expected to be very low. However, the energy transfer efficiency can still be improved by employing a resonant circuit on both primary coil and secondary coil. Note that the PTE is derived from the assumption that the inductive link is loosely coupled where *k* is very low.

2.3 Summary

In this chapter, an overview of several energy harvesting methods has been presented. The MF inductive coupled energy harvest is chosen for this project as the system allows a lower power system synchronisation by modulating data with the harvesting energy. In addition, the MF inductive coupled energy harvesting source is independent to the environment compared with other energy harvesting methods.

The mathematic model of the inductive loosely coupled power transfer has been studied. Several equations derived in this chapter have shown how the system can be optimised. The size of the transmitter and receiver antennas can be calculated to maximised the harvested energy. Furthermore, the operating frequency of the system can be selected based on the size of the transmitter antenna. Moreover, the resonant circuit can be used to further increase the received voltage to ensure that the receiver can be powered up with sufficient harvested energy.

Chapter 3: INDUCTIVE COUPLED ENERGY HARVESTING SYSTEM LEVEL STUDY

In this chapter, the system level issues for a medium frequency (MF) inductively coupled energy harvesting system deployed in a large approximately square area, such as a farm or industrial site are studied. An AC-DC receiver/rectifier, which is an important element in the wireless energy harvester design, is explained. The magnetic field generated by the transmitter loop and the output voltage received at the ferrite rod antenna are examined. And lastly, a scheme for system synchronisation of the wireless energy harvest is investigated.

3.1 System Level Overview

The system level of the proposed inductively coupled wireless energy harvesting scheme is shown in Figure 3.1. The system consists of a transmitter and several remotely located sensor node receivers. At the transmitter block, it is comprised of a loop transmitter antenna, typically approximately square or rectangular, a transmitter driver and a radio receiver (at HF/UHF) for a data uplink. The sensor node receiver block consists of a ferrite rod receiving antenna, an AC-DC receiver/rectifier, a data demodulator and a radio transmitter (at HF/UHF). The transmitter magnetic field is modulated with digital data, and is generated by driving a transmitting antenna with the driver, then the magnetic energy received at the secondary coil is converted from an AC signal to DC for energy storage, such as in a large capacitor.

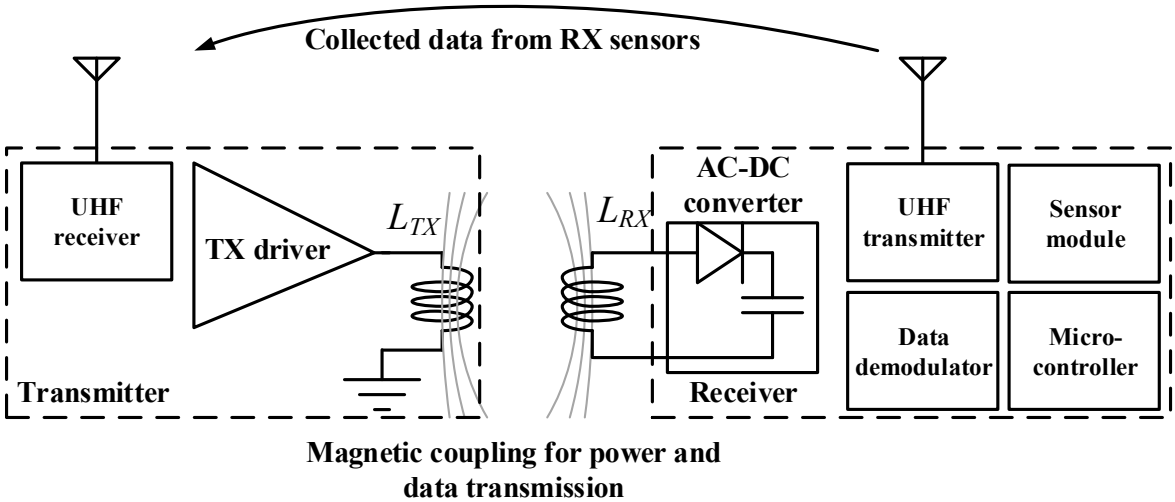


Figure 3.1 System diagram of the inductive coupled wireless energy harvesting.

Moreover, a significant average power consumption, which is caused by the power-hungry radio transmitter and sensor modules, is reduced by activating the modules only when needed. The *active* or *sleep* command is modulated, together with the timing information for the system

synchronisation, through the harvesting energy. A calculation of the average power can be done by using equation (3.1), where *P* is the average power consumption, P_n is the power consumption of the module, t_n is the active time of the module per period and t_T is the total time period. The duration of the active time of the module is constrained by the selected module, on the other hand, the total time period per one cycle of operation can be flexible in order to reduce the average power consumption. For example, if the power consumption of a transmitter module is 1 W and the active time is 10ms then the average power consumption of the transmitter module per 1 hour is 2.78μW. The average power consumption can be reduced to 1.39μW if the transmitter module only activates every 2 hours.

$$P = \frac{P_1 t_1 + P_2 t_2 + P_3 t_3 + ...}{t_T}. \qquad (3.1)$$

As the sensor node collects data, the radio transmitter at the sensor node is used to send the collected data back to the primary source in a suitable RF channel. Because the data transmitted back to the source from several sensor nodes can potentially collide if the timing is incorrect, a synchronisation system is needed. A real-time-clock (RTC) can be used to generate the timing at each sensor node. However, a more accurate RTC consumes more power. On the other hand, the accumulating timing errors of the less accurate but also less power hungry RTC in a long service lifetime sensor node may cause collision or data loss [31, 32]. For example, the RTC shown in [32] consumes very low power at 5.4nW. However, the accumulating timing error of the design is 4.37 seconds per hour. The timing error is calculated by using equation (3.2) where *ppm* is the frequency variation in units of parts per million (ppm) of the clock. Alternatively, system synchronisation with precise timing information and less power consumption at the receiver node can be achieved by transmitting data instructions modulated with the carrier energy signal at the source to the receivers, and then the data can be demodulated at the receivers [7, 11, 12]. Hence the data modulation technique used for the system synchronisation is chosen in this project. The data modulation technique is discussed later in this chapter.

$$t_{delay} = \frac{24 \times 3600 \times ppm}{10^6}. \qquad (3.2)$$

A flowchart of a possible synchronisation protocol for the MF inductively coupled wireless energy harvesting system is depicted in Figure 3.2. The operation can be described as follows. Initially, the sensors start from cold by harvesting the magnetic energy generated from the transmitter. When each receiver is awakened and has sufficient energy stored, an acknowledge signal is sent from each sensor node receiver to the transmitter via the HF/UHF uplink radio channel. If the central source receives acknowledgement signals from all of the sensor node receivers, then the initialisation of the system is complete. Then, in normal operation mode, the sensor nodes are only activated to collect and transmit data back to the source when the nodes receive the *active*

command. As a result, sensor nodes consume less power and the system is precisely synchronised without the need for each node to provide an RTC. Note that this protocol is chosen due to its simplicity. Many other variations are possible with the proposed hardware depending on programmers/users.

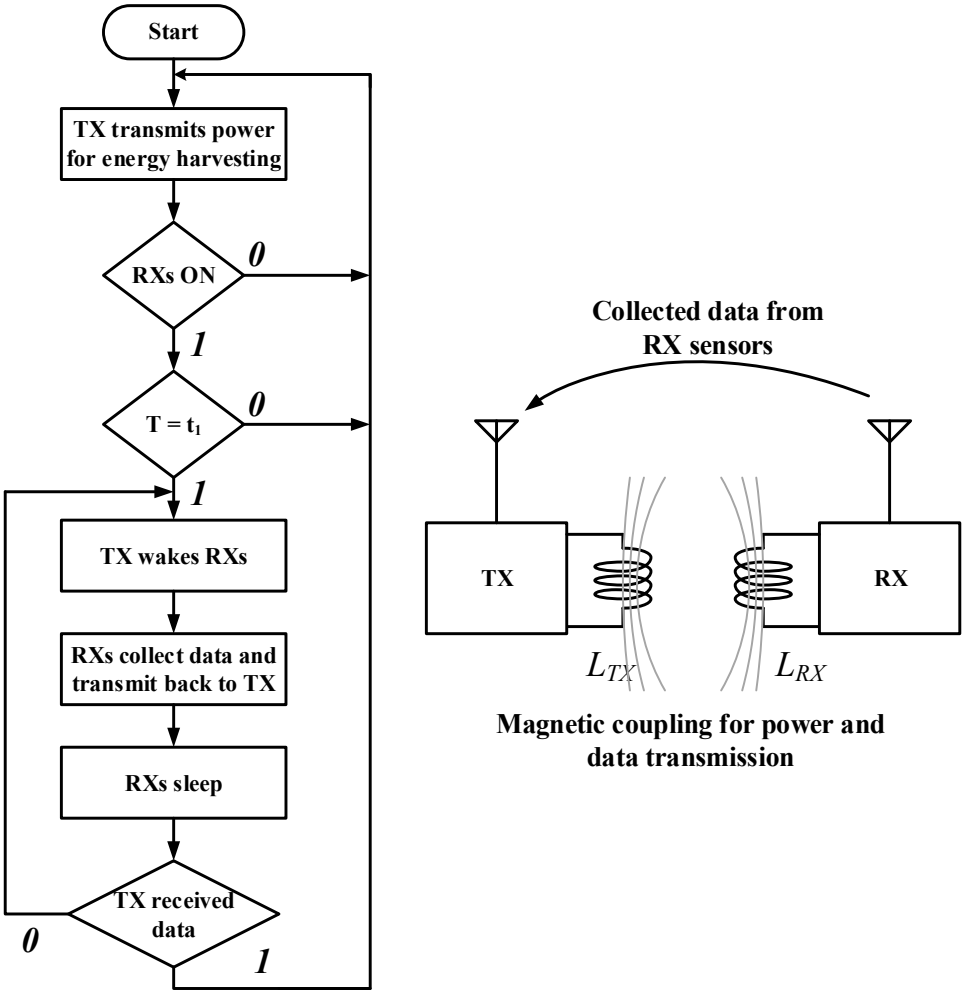


Figure 3.2 Example of the synchronisation protocol for the sensor network.

In the following sections, the AC-DC receiver rectifier used for harvesting the magnetic energy and the data demodulator used for the system synchronisation are studied.

3.2 AC-DC Conversion

For wireless energy harvesting applications, an AC-DC converter or receiver rectifier is an essential element for supplying the power to the applications. The rectifier circuit converts the ambient electromagnetic or magnetic signal received from an antenna to DC voltage. The conventional rectifier consists of a diode and a capacitor where the diode rectifies the incoming AC signal and the capacitor averages the rectified signal to DC voltage. The power conversion efficiency (PCE) of the rectifier circuit is strongly dependent on the forward bias voltage of the diodes used, particularly with very low signal voltages, and also on the losses due to parasitic resistance in the circuit. Furthermore, the leakage during the reverse bias of the diode might also decrease the DC voltage

at the output of the rectifier circuit. In addition, the dynamic power consumption ($CV_{DD}^2 f_{in}$) of the rectifier also degrades the efficiency, especially at high frequencies. A standard CMOS process is chosen for the implementation of the rectifier in this project for cost reasons, as explained in Chapter 1. In a standard CMOS process, MOS transistors are often used in a diode-connected configuration as illustrated in Figure 3.3. The gate and drain of the NMOS M_1 are connected to form a diode, and the diode is operated in forward bias when the input voltage is approximately greater than the threshold voltage (V_{th}) of the transistor. However, the diode-connected transistor fails to conduct if the input amplitude is smaller than the V_{th} of the transistor. In addition, the nominal V_{th} of the target CMOS process is approximately 350mV for NMOS transistor (V_{thn}) and -400mV for PMOS transistor (V_{thp}). In practice, the output current can still be weakly conducting due to the subthreshold leakage but might be insufficient to power the system.

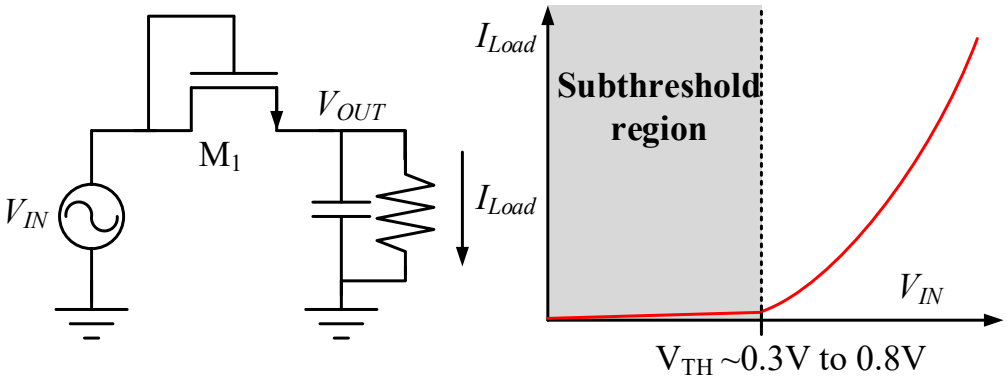


Figure 3.3 Rectifier implemented from the diode-connected NMOS and the load capacitor (left) and the output current behaviour (right).

3.2.1 Power Conversion Efficiency

Before the rectifier is analysed, the PCE of the rectifier circuit must first be introduced. PCE can be defined as a ratio of the power delivered to the load to the total power that is consumed from the source at the input of the rectifier

$$PCE = \frac{P_L}{P_s} \cdot 100 \,. \qquad (3.3)$$

To observe the performance of the rectifier circuit, one can determine the PCE and the converted DC output voltage of the rectifier.

3.2.2 Voltage Multiplier

The conventional voltage rectifier, as depicted in Figure 3.3 including the full-wave rectifier, is not suitable for this application since the rectified output voltage is always smaller than the input voltage in practice. For example, if the input voltage of the rectifier is 500mV_{pk} then the DC output of the conventional rectifier is always less than 500mV, which is not adequate for the CMOS circuit

operating in the saturation region. Therefore, several published works have proposed rectifier circuits that were developed from the voltage doubler/multiplier which can provide a higher output voltage with the same input voltage compared with the conventional voltage rectifier.

The voltage multiplier rectifier circuit used is based on the Dickson charge pump proposed in [33]. Figure 3.4 illustrates the voltage multiplier rectifier that comprises the NMOS M_1 and M_2, the coupling capacitor C_c and the load capacitor C_L. The operation of the circuit is as follows. As an AC signal voltage is applied at the input, when the input voltage is negative, the transistor M_1 is ON while transistor M_2 is OFF. Hence, the negative voltage with respect to ground is stored in capacitor C_c. In the next half period of the input, when the input is positive, the transistor M_2 is ON while the transistor M_1 is OFF. Therefore, the charge in capacitor C_c is pumped to the load capacitor C_L. Eventually, the output voltage is charged to double the input amplitude for an ideal case where the diode forward bias voltage is negligible. By using the same concept, the output voltage can be increased by cascading the voltage multiplier rectifier stages as shown in Figure 3.5 [33].

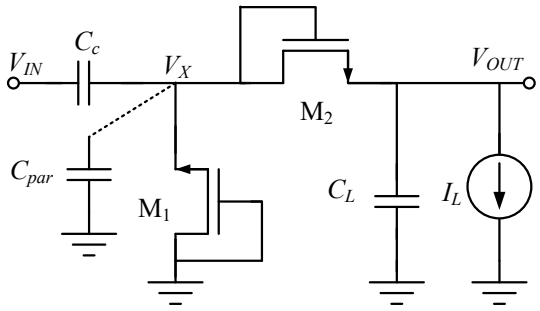


Figure 3.4 Voltage multiplier rectifier implemented from NMOS transistors.

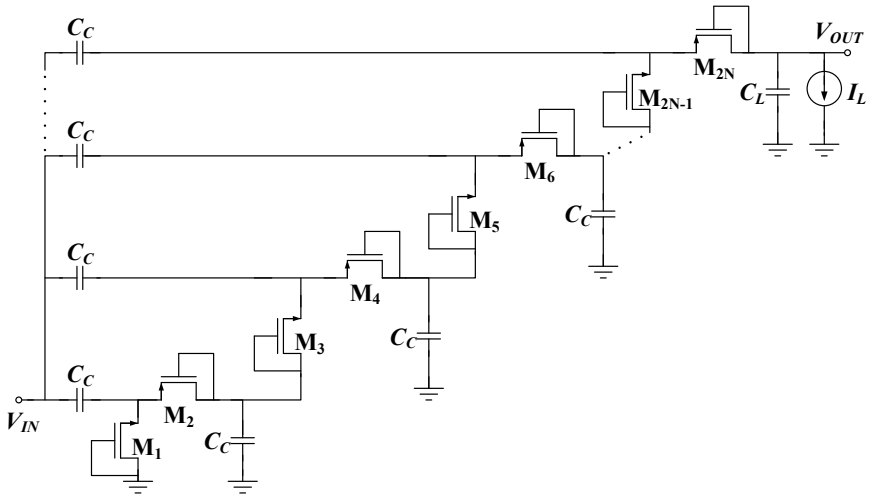


Figure 3.5 N stages voltage multiplier rectifier.

In addition to the circuit, the voltage multiplier can be implemented by three configurations which are the NMOS-only, PMOS-only and the CMOS voltage multiplier. The PMOS-only and CMOS voltage multipliers may benefit from the connection of source and body of the PMOS, which is standard in CMOS processes if deep N-Well is not available. The body-effect of the MOS transistors is exempted in such configurations. On the other hand, the NMOS-only voltage multiplier rectifier

occupies a smaller area compared to the other two configurations. Moreover, the parasitic capacitance of the transistors C_{par} depicted in Figure 3.4 forms a capacitive dividing configuration at node *X*. Therefore, the voltage at node V_X is attenuated by

$$V_X = \left(\frac{C_c}{C_c + C_{par}} \right) V_{IN} . \quad (3.4)$$

Furthermore, the parasitic capacitance at node V_X due to the MOS transistors depicted in Figure 3.5 can be calculated by [17]

$$C_{par} = 2\left(C_{gso}W + C_j WE + 2C_{jsw}(W + E)\right), \quad (3.5)$$

where C_{gso} is the overlap capacitance per unit width, C_j is the junction capacitance per unit area, C_{jsw} is the side-wall junction capacitance per unit perimeter, *W* is the width of the transistor and *E* is a process parameter constant which can be found in the datasheet. The process parameter constant *E* is often five or six times of half of the minimum channel length [17].

The DC output voltage of the rectifier was originally derived by Dickson [33], however the equations are not accurate for radio frequency identification (RFID) rectifier applications which typically operate at higher frequencies than originally envisaged and with micro-power input levels [19]. In the original proposal, the equations are developed from an assumption that the input voltage is relatively large compared with the MOS V_{th}. The forward voltage drop in diodes is also assumed to be linear in the original proposal. For the rectifier in RFID applications, including RF energy harvesting systems, the nonlinearity of the forward voltage essentially affects the output voltage of the rectifier, since the input voltage is often close to the V_{th} value of the MOS diodes. Therefore, a more accurate model for the rectifier for RFID applications is proposed [17-19]. The output voltage of the voltage multiplier rectifier, derived from a simple and accurate model for RFID rectifier, can be expressed as [18]

$$V_{OUT} = 2N\left(V_{IN}\left(\frac{C_c}{C_c + C_{par}} \right) - \sqrt{\frac{2I_L}{\beta}} - V_{TH} \right) - \frac{2NI_L}{f\left(C_c + C_{par}\right)}, \quad (3.6)$$

where β is the gain factor of the transistor ($\beta = \frac{\mu C_{OX}}{n}\frac{W}{L}$), I_L is the load current, *N* is the number of stages of the voltage multiplier and *f* is the frequency of the input signal. Note that this equation is derived from the assumption that the input voltage is larger than the V_{th}. The voltage multiplier rectifier fails to operate when the rectifier input voltage is less or equal to the MOS thresholds.

Figure 3.6 illustrates the equivalent circuit of the voltage multiplier rectifier proposed by [19]. The Thevenin equivalent voltage source and resistance at the output can be expressed as

$$V_{THEV} = 2N\left(V_{IC}\alpha - V_{DIO}\right), \quad (3.7)$$

$$R_{THEV} = \frac{2N}{f\left(C_C + C_{par}\right)} = \frac{2N\alpha}{fC_C}, \quad (3.8)$$

where α is the dividing capacitance of the rectifier ($\alpha = C_C/(C_C + C_{par})$) and V_{DIO} is the forward voltage of the diode-connected MOS transistor ($V_{DIO} = \sqrt{2I_L/\beta} + V_{TH}$). The Thevenin model can be used to analyse the rectifier output loading current, which can be expressed as

$$I_L = \frac{V_{THEV}}{(1 + k_L)R_{THEV}}, \quad (3.9)$$

where k_L is the ratio of the loading resistance to the Thevenin resistance [34]. In addition, the equivalent input impedance of the multi-stage voltage multiplier rectifier consists of the input capacitor C_{IN} paralleled with the input resistance R_{IN}, as depicted in Figure 3.6. The expressions of the lumped equivalent components are given by

$$C_{IN} = 2N\frac{C_c C_{par}}{C_c + C_{par}}, \quad (3.10)$$

$$R_{IN} = \frac{C_c + C_{par}}{NC_c} \cdot \frac{V_{IN}}{4I_L}. \quad (3.11)$$

The derivation of the equivalent input impedance is presented in Appendix C.

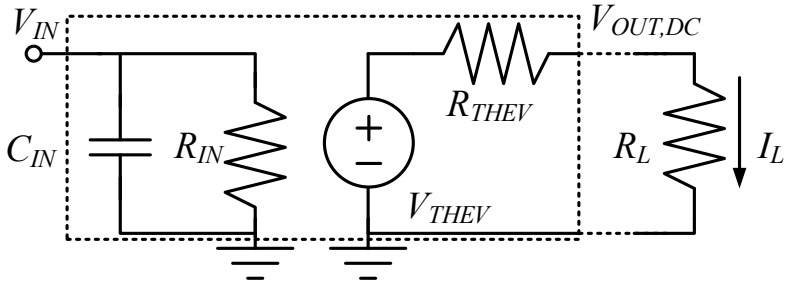


Figure 3.6 Equivalent circuit of the voltage multiplier rectifier.

Equation (3.6) indicates that the output voltage is limited by the MOS diode forward voltage, so the rectifier cannot convert the AC signal into DC voltage if the input amplitude is smaller than V_{th}. Since the received voltage at the secondary coil of the wireless energy transfer system could be of the order of 500mV or even lower, then even with several stages, the output voltage from the voltage multiplier might not be sufficient to power up the system since the multi-stages rectifier also suffers from body effect and loss due to parasitic capacitance. Schottky diodes, although often unavailable in a standard CMOS process, can improve the rectifier circuit since the forward bias voltage can be as low as 200 mV [19]. Moreover, the zero or near-zero-V_{th} MOS transistor, which is available in many deep-submicrometer processes, can also increase the sensitivity of the rectifier [35, 36]. However, Schottky diodes and near-zero-V_{th} MOS transistors also have significant reverse leakage current, which can cause large losses of power when the rectifier input voltage is large.

As has been discussed, the MOS voltage multiplier rectifier could not provide an adequate DC voltage for powering the system. Alternative circuits for the diode-connected MOS transistor to reduce the effective V_{th} will be examined and discussed later. However, the rectified output voltage and the input impedance of the rectifier can still be used for the system level analysis as the components used in the alternative circuits are still similar to the conventional voltage rectifier circuit [5, 37, 38].

3.2.3 Secondary Coil Output Voltage

As the input impedance and the output voltage of the AC-DC receiver rectifier have been studied, the input AC voltage received at the resonant secondary coil antenna of the system (V_{RX}) can be derived by substituting equations (2.23) and (3.11) to (2.22), which yields

$$V_{RX} = \frac{\left(\omega_0 L_{RX} C_0\right)\cdot V_{IND} - \left(2\alpha N L_{RX}\right)\cdot I_L}{C_0 R_{RX}}, \qquad (3.12)$$

where C_0 is the receiver parallel capacitor ($C_0 = C + C_{IC}$) and C_{IC} is the input capacitor of the rectifier shown in equation (3.10). Furthermore, the rectifier loading current can be substituted by (3.9) which yields

$$V_{RX} = \frac{\left(\left(1+k_L\right)\left(2\pi f\right)L_{RX}C_0\right)\cdot V_{IND} - \left(2NfL_{RX}C_C\right)\cdot V_{TH}}{\left(1+k_L\right)C_0 R_{RX} + 2Nf\alpha L_{RX}C_C}. \qquad (3.13)$$

Equation (3.13) can be used to calculate the received voltage at the secondary coil connected to the AC-DC receiver rectifier. However, the equation may be too complex to intuitively explain the system due to the large amount of parameters. By considering equation (3.12) which is less complex, it can be seen that the increase of the loading current I_L of the rectifier output can potentially decrease V_{RX}. This is because the Q-factor of the receiver is affected by the loading current, which eventually decreases the output received voltage. It is important to note that equations (3.13) and (3.12) are derived with the assumption that the rectifier is operating when the input voltage of the rectifier is relatively large compared with the value of the V_{th}.

From the derived equations shown in this section we can summarise that (1) the rectifier requires a voltage that is relatively large compared with the value of the MOS V_{th} and (2) the rectifier output loading current can affect the output voltage of the secondary coil (or the rectifier input voltage in this case). Thus, the design of the receiver antenna in this project is prioritised towards maximizing the received voltage V_{RX} and the rectifier DC voltage V_{OUT} rather than optimising the PTE of the system. The received voltage at the antenna has to be large enough such that the AC-DC receiving rectifier can start-up from cold and generate sufficient rectifier DC voltage.

3.2.4 Rectifier Architectures

The voltage multiplier shown in the previous sections cannot convert the AC voltage into a usable DC voltage supply if the input voltage is close to the V_{th} of the transistor. The diode-connected transistor in the rectifier requires the gate-to-source voltage (V_{GS}) to be greater than the V_{th} to form a conducting channel. Figure 3.7 shows the example state-of-the-art voltage rectifier architectures where the V_{GS} is biased to decrease the effective V_{th} of the transistor. Note that the rectifier architectures in this section are shown in a single-stage form, however, these circuits are also suitable for multi-stage implementation (i.e., with voltage multiplication) as well.

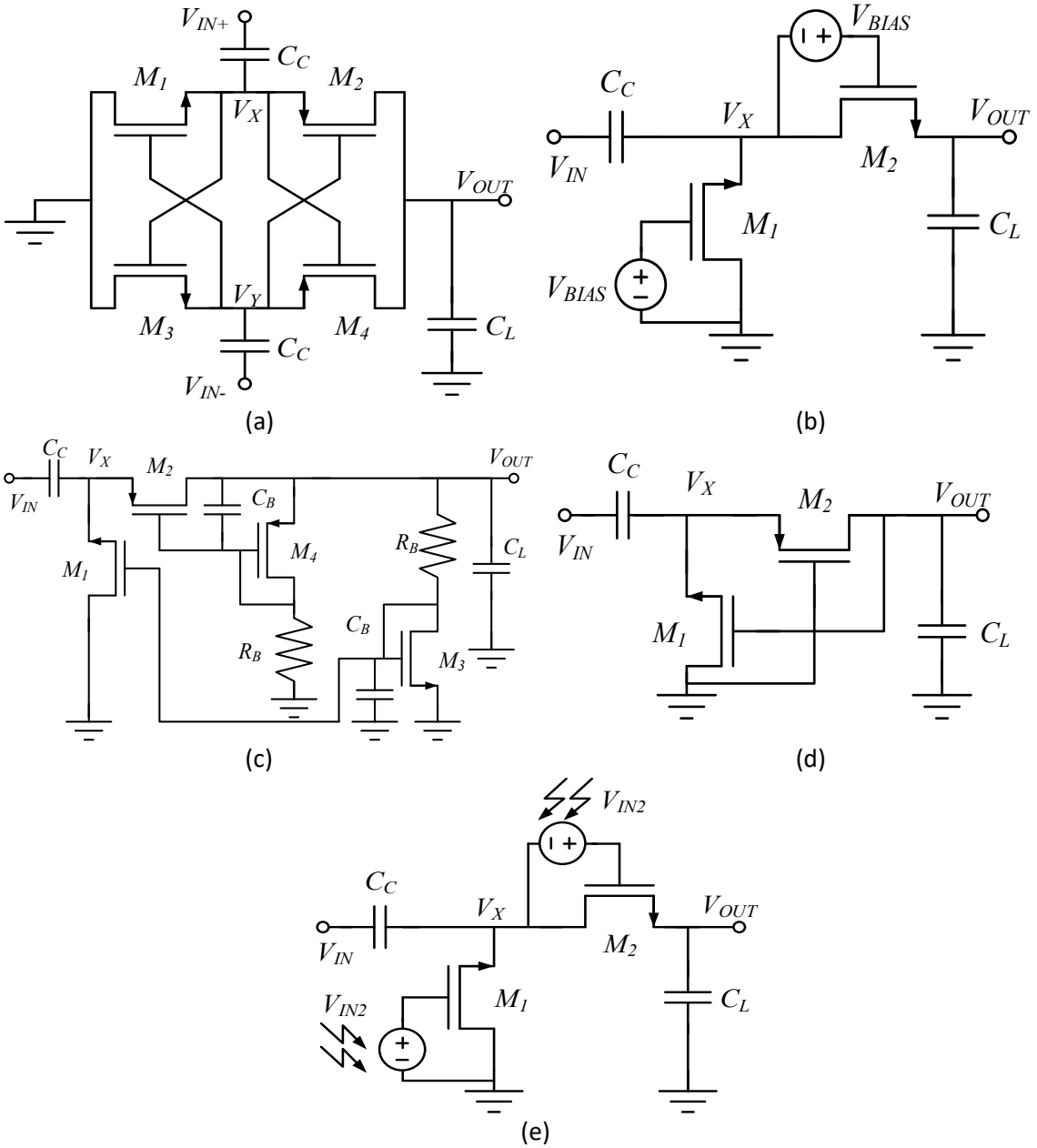


Figure 3.7 Voltage rectifier architectures.

The differential drive rectifier (DD) shown in Figure 3.7(a) was proposed in [13, 39, 40]. The single-stage DD consists of two NMOS (M_1 and M_3) and two PMOS (M_2 and M_4) transistors connected in a

cross-coupled configuration with a bridge structure. The rectifier requires a differential source connected to V_{IN+} and V_{IN-}. The operation of the circuit is as follows. During the positive phase of the input where V_{IN+} is positive and V_{IN-} is negative, transistors M_2 and M_3 are ON while transistors M_1 and M_4 are OFF. Thus, the current flows from V_{IN+} through transistor M_2 to charge the load capacitor C_L and flows back to V_{IN-} through transistor M_3. Similarly, when the input V_{IN+} is negative and V_{IN-} is positive, transistors M_1 and M_4 are ON while transistors M_2 and M_3 are OFF. Hence, the load capacitor is charged by the current flowing through M_4 and M_1. Compared with other proposed circuits, the DD can provide higher efficiency and output voltage when the input is close to the value of V_{th}. However, reverse current leakage significantly increases as the input voltage is increased because the MOS transistors are partially active during the reverse bias phase. Moreover, it can be observed that the circuit requires four transistors and three capacitors for a single stage rectifier which requires a larger size, and potentially adds larger parasitic capacitances with their associated losses. Furthermore, the DD begins to generate a DC voltage only when the peak amplitude input voltage is larger than the value of the V_{th}, this is because the output voltage at cold-start is practically zero, which is not sufficient to bias the DD MOS rectifying transistors.

Figure 3.7(b) illustrates the external V_{th} cancellation rectifier (EVC), which resolves the issue by applying the static voltage across the gate-to-drain terminal of the transistors [37, 41]. By ignoring the load current and the parasitic capacitance, the simplified expression of the output voltage of the rectifier is

$$V_{OUT} = 2\left(V_{IN} - V_{th} + V_{BIAS}\right). \quad (3.14)$$

If the bias voltage is equal to the V_{th}, the limitation due to the insufficient rectifier input below the V_{th} is completely eliminated. The bias voltage of the EVC is distributed by using a switch-capacitor technique to provide the DC voltage [37, 41]. As a result, the effective V_{th} of the rectifier transistors can be reduced to zero if the bias voltage is properly chosen. The circuit can rectify even if the input AC signal is smaller than the MOS V_{th}. However, it appears that the circuit requires an external battery source to supply the voltage to the rectifier. As a result, the circuit is not appropriate for this project since the receiver at the secondary coil must be able to harvest energy from a cold-start. Furthermore, the switch-capacitor biasing generator may consume an additional large area since moderate size capacitors are required for storing the bias voltage.

The internal V_{th} cancellation rectifier (IVC), depicted in Figure 3.7(c), alleviates the insufficient input voltage issue by employing the additional diode-connected transistors M_3 and M_4 to bias the rectifying transistors M_1 and M_2 [42]. In steady state, the DC output voltage of the rectifier (V_{OUT}) provides a bias voltage to the diode-connected M_3 and M_4 where the capacitor C_B is added to filter the high-frequency component of V_{OUT}. Moreover, the large resistor R_B is used to limit the loss current of the bias source MOS diode. Compared to other circuits, the IVC circuit has lower reverse

leakage current when the input voltage is relatively large since the transistors are biased by additional diode-connected transistors such that variations in the V_{th} are compensated. However, since the circuit consists of four transistors, two resistors and four capacitors for a single stage rectifier, the total size of the circuit may be larger compared with other circuits. Note that the IVC fails to start from cold if the rectifier input voltage is lower than the value of the V_{th} since there is no available bias voltage to reduce the effective rectifier MOS thresholds.

The self-V_{th} cancellation rectifier (SVC) proposed in [5, 14, 38] is shown in Figure 3.7(d). As can be seen from the figure, the gate of the input rectifying transistor M_1 is biased by the rectified output DC voltage at the adjacent transistor M_2. Similar to the DD circuit, the SVC rectifying transistors behave as a voltage controlled switch instead of a diode. Since the effective gate bias rises with the input voltage, the NMOS M_1 can become active in both positive and negative input phases when the output voltage is above V_{th}. Similarly, the PMOS M_2 can also become active during the negative input phase when it is supposed to turn off. Therefore, the SVC and DD can exhibit large leakage when the input voltage is relatively large. By comparing this to three previous rectifiers, it can be seen that the area of the SVC is much less since no additional devices are required. Moreover, the effective threshold of the rectifier is reduced by the biasing voltage from the adjacent transistor. In contrast, the PCE of the circuit decreases if the input signal is too large, in a similar way to the differential drive rectifier. Similar to the DD and the IVC, the SVC is not functional when the rectifier input voltage is below the value of the V_{th}.

The hybrid rectifier (HR) is shown in Figure 3.7(e); the circuit rectifies the two dedicated voltage sources V_{IN} and V_{IN2}. The voltage V_{IN} is rectified to supply the main system while the voltage V_{IN2} is generated to provide a bias voltage for the main rectifier. The secondary voltage can be provided by an external source such as a PV cell [43] or a piezoelectric sensor [44]. It can be observed that the circuit configuration is similar to the EVC shown in Figure 3.7(b). By rectifying the two dedicated sources, the HR circuit can convert an AC signal that is lower than the V_{th} similar to the EVC, while other previous rectifiers could not operate with the same input signal. On the other hand, the circuit requires an additional DC source which might not be practical for many applications.

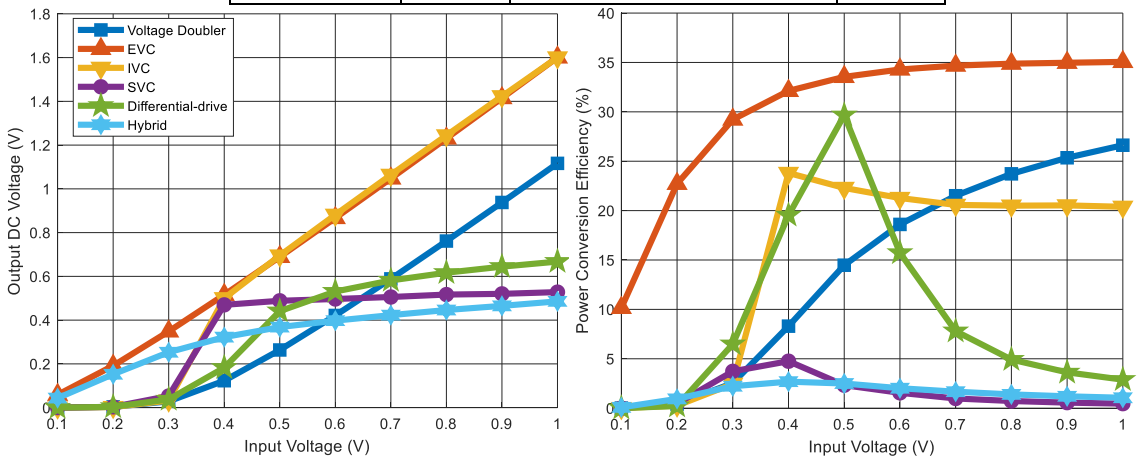
Although an active diode voltage multiplier rectifier could achieve the highest PCE, however, more than a few µW is consumed by the high-speed comparator used for the active diode [45]. Hence, this type of rectifier is often seen only in a near-field strongly coupled inductive link applications, such as implantable medical devices (IMD) [3, 7, 45], where the rectifier input voltage can be between 1V and 3V.

To select a suitable rectifier circuit for the inductive loosely coupling system, the rectifier architectures, investigated in this section, are simulated and compared. The model library of the

180nm CMOS process used for the simulations is extracted from the AMS 0.18µm CMOS process [46]. The V_{th} of the 0.18µm NMOS is 0.35V while the threshold of the 0.18µm PMOS is -0.42V. The LTspice software was used for simulating the rectifier circuits' architectures prior to commencing a final design. The load resistance of 500kΩ is chosen as the output power of 2µW and output voltage of 1V are expected to be a minimum usable level to be delivered to the load. From the system requirements, the dimensions of the transistors for rectifiers are calculated using equations from section 3.2.2. Thus, the parameters of the circuit are shown in Table 3.1. The dimensions of the transistors are realised from the optimization in the simulation after starting from the initial calculations. For the architecture comparisons, the input signal with an operating frequency is at 1MHz and is stepped from 0.1V to 1V. Note that the transistors M_3 and M_4 of the IVC are slightly smaller than the rectifying transistors to minimise the bias current of the diodes MOS M_3 and M_4.

Table 3.1 Parameters used in rectifiers simulation.

Parameters	Value	Parameters	Value
NMOS W/L	10/0.2	Coupling capacitance, C_C	50pF
PMOS W/L	40/0.2	Load resistance, R_L	500kΩ



(a) Output voltage versus input voltage (b) PEC versus input voltage

Figure 3.8 Output voltage and PCE versus input voltage of different rectifier architectures with the operating frequency of 1MHz and a load of 500kΩ.

The output voltage and PCE comparisons of the voltage multiplier, EVC, IVC, SVC, DD and HR are illustrated in Figure 3.8. From Figure 3.8(a), it appears that the converted output voltages when the peak amplitude of the input voltage is high for the EVC and IVC are better than other circuits. On the contrary, only EVC and HR can rectify when the input is lower than $0.4V_{pk}$ which implies that the circuits could operate when the input voltage is below the V_{th} of the CMOS transistors. For the other rectifier circuits, when the input voltage is lower than the V_{th}, the transistors are not activated due to the insufficient voltage at the V_{GS} of the MOS transistors. Observing the result of SVC, DD and HR, it can be seen that the output voltages start to saturate when the input voltage is greater

than $0.5V_{pk}$. Such behaviour occurs because the reverse leakage current increases, as explained earlier.

In addition to the PCE performance shown in Figure 3.8(b), the EVC has the best PCE because the power consumption of the DC biasing generator is not taken into account. (An ideal voltage source is used instead.) Ignoring the PCE result of the EVC, the DD and IVC have the best PCE when the input voltage is low. In contrast, the PCEs of the conventional voltage multiplier and the IVC rectifier are better than the others when the input is high.

In summary, rectifier circuits shown in this section provide different trade-offs. The DD and the SVC appear to be suitable when the input signal is close to the V_{th} of the MOS transistor. On the other hand, the EVC produces the best efficiency when the input voltage is sufficiently large. When the input voltage is lower than the V_{th}, only the EVC and HR are functional for voltage conversion. However, the EVC rectifier requires an external battery while the hybrid rectifier requires an additional voltage source.

For this project, EVC and HR are not suitable since there are no external batteries and secondary harvesting source available. Furthermore, other rectifiers may not be appropriate as those rectifiers cannot operate properly when the received voltage at the secondary coil is lower than the V_{th}, which is likely to occur in this project. Hence, an alternative approach is proposed in the next chapter.

3.3 Magnetic Field Strength and Receiver Output Voltage

As the rectifier circuit model has been investigated, the rectifier equivalent circuit can be used to study the harvested energy of the magnetic loosely coupled energy harvesting system.

The magnetic field strength generated by an ideal square transmitting loop coil and the received output voltage excited at the secondary coil using a ferrite rod antenna are plotted in MATLAB. The parameters used for the calculation are shown in Table 3.2. The width of the square loop is chosen based on the target applications as this project is intended to design the inductively coupled energy harvesting system for a wide area between $10x10m^2$ to $100x100m^2$. Moreover, the conductor wire and the ferrite rod used in this demonstration is based on options available in the market.

Figure 3.9 illustrates the plot of the magnetic field strength generated from the $10x10m^2$ square loop antenna when the centre of the square loop is at the origins (x = 0m, y = 0m) and the vertical distance between the primary coil and the secondary coil is 1m. As explained in section 2.2, the receiver sensor nodes are placed on the ground and the transmitting coil is constructed 0.1m-2m above the ground to minimise the magnetic field distortion due to the ground. It can be seen that

the field strength peaks around the edge of the square area within the loop and decreases when the received point is moving toward the centre of the loop, which is similar to the plot of the magnetic field of the square loop shown in Figure 2.4 from the previous chapter. This is because the magnetic field strength is inversely proportional to the square of the distance between the point of interest and the conducting wire from the Biot-Savart law [22]. Moreover, it can be observed that the field strength falls rapidly outside the perimeter of the loop. As a result, interference from the magnetic energy with another user of the radio spectrum outside the square loop antenna is unlikely.

Table 3.2 Parameters of the square loop antenna and the ferrite rod antenna used for the calculations of the magnetic field strength and receiver output voltage.

Square loop transmitting antenna		**Ferrite rod receiving antenna**	
Parameters	**Value**	**Parameters**	**Value**
Operating frequency	1MHz	Ferrite permeability at 1MHz, μ_r	125+j30
Transmitting current, I_{TX}	100mA	Ferrite rod relative permeability, μ_{rod}	20
Width of the single square loop, *2*W*	10m-100m	Ferrite rod diameter	8mm
Vertical distance between the coils (z-axis)	1m	Ferrite rod length	45mm
Radius of the conductor	0.1mm	Radius of the conductor	0.1mm
TX and RX Coils resistance	0.57Ω/m	Number of turns of the coil	32
		Ferrite rod loading resistance, R_{IN}	50kΩ

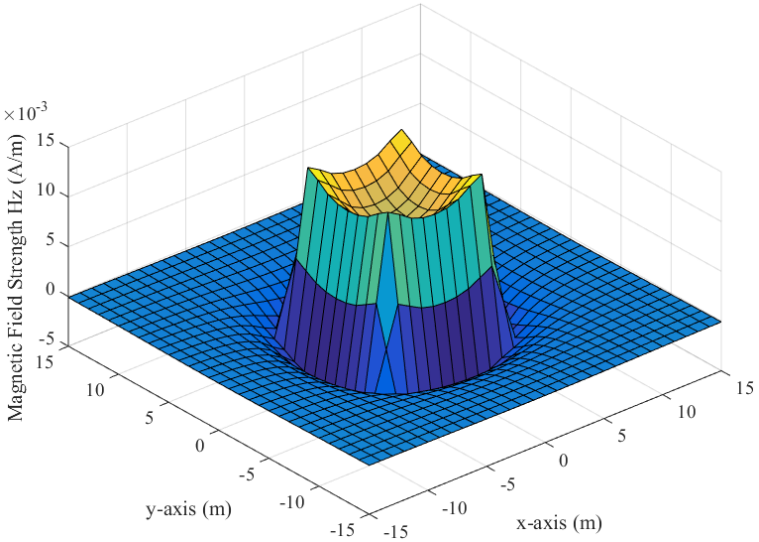


Figure 3.9 Magnetic field strength of the 10x10m^2 square loop antenna at the distance z = 1m when the current I_{TX} is 100mA and the operating frequency is 1MHz.

The plot of the magnetic field strength has shown that the interference outside its perimeter is very low, however it is still important to consider the radiated power caused by the square loop antenna at far-field. The radiation power of the square loop antenna at far-field is given by [27]

$$P_r = Z_0\left(\frac{\pi}{12}\right)\left(k_0(2W)\right)^4\left|I_{TX}\right|^2, \qquad (3.15)$$

where Z_0 is the impedance of free space and k_0 is the wavenumber. In this example, with an excitation current of 100mA, the calculated radiated power from the square loop antenna is 0.192mW or -7.16dBm. Calculating by using the free space path loss equation [27] when the receiving antenna is ideal and the gain is G=1, the radiated power at 1km is reduced to 173pW or -67.6dBm.

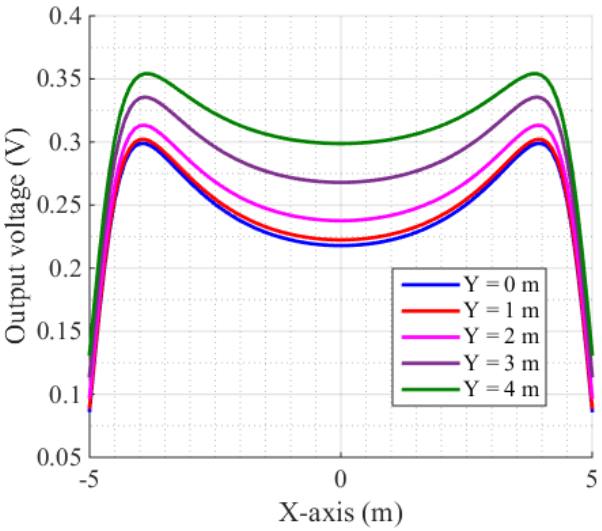


Figure 3.10 Received output voltage of the ferrite rod antenna located within the square loop when the transmitting current is 100mA, the vertical distance (z-axis) between the coils is 1m, the number of turns of the secondary coil is 32 and the loading resistance of the secondary coil is 50kΩ.

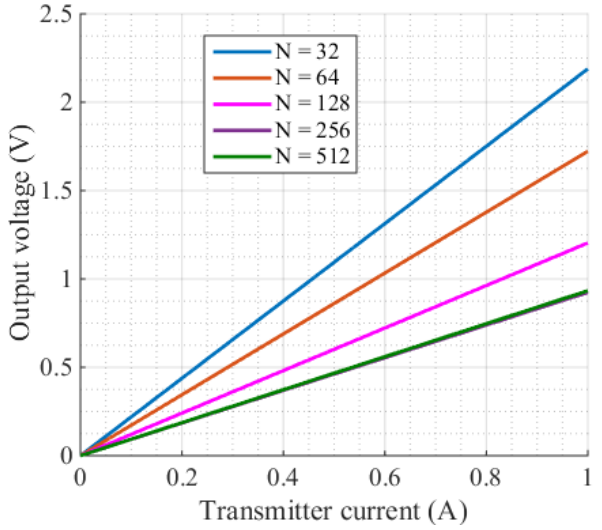


Figure 3.11 Received output voltage of the ferrite rod antenna located at the centre of the square loop when the transmitting current is increasing, the vertical distance between the coils is 1m and the loading resistance at the output of the secondary coil is 50kΩ.

Moreover, the plot of the output received voltage at the resonant secondary coil, implemented from a ferrite rod antenna with the parameters shown in Table 3.2, at different points of interest

(x, y) within the example transmitting square loop coil is depicted in Figure 3.10. It can be observed that the voltage peaks at the area close to the inner boundaries of the square loop are similar to the magnetic field strength plotted in Figure 3.9. In addition, the received output voltage at the coil within the square area varies between 225mV$_{pk}$ to 360mV$_{pk}$. Furthermore, the plot of the received output voltage of the coil versus the transmitter current, with different numbers of turns of the ferrite rod receiving coils, is shown in Figure 3.11. It can be seen that the output voltage is increased when the square loop antenna current increases. This is because the magnetic field strength is linearly proportional to the loop coil current, as can be seen from equation (2.11). Consequently, the output voltage is increased as the magnetic field strength increases. On the other hand, it can be observed from the plot that the optimum number of turns of the receiving coil is at 32, as it was explained in section 2.2.3 that the loading resistance can limit the Q-factor of the secondary coil if the receiver inductance L_{RX} is too large. Note that this calculation assumes that the receiving capacitor at the receiving antenna is tuned to the resonance frequency accordingly, since the number of turns of the receiving coil affects the inductance of the receiving antenna.

3.4 Data Demodulator Requirements for System Synchronisation

As mentioned in section 3.1, the data modulation is used for the system synchronisation. The modulation methods and the demodulator architectures are investigated in this section.

A central issue in the implementation of a communications channel associated with the MF magnetic power supply system is that the data modulation used must be compatible with the main function of energy harvesting. Hence, the modulation should not interfere significantly with the recovery of energy and should also be able to be demodulated with simple ultra-low power circuits.

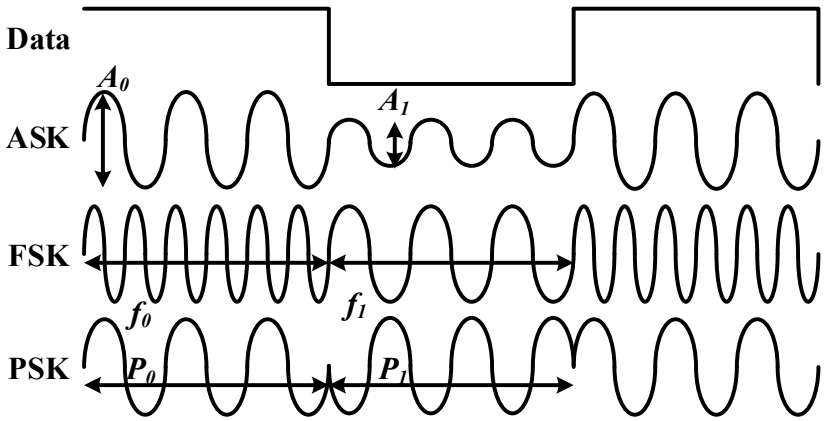


Figure 3.12 The digital modulation techniques of ASK, FSK and PSK.

In recent work, three simple digital modulation techniques are mostly used for wireless data communications of RFID and IMD systems [4, 7]. Such techniques are amplitude-shift keying (ASK), frequency-shift keying (FSK) and phase-shift keying (PSK). Figure 3.12 illustrates examples of the

digital modulation techniques. ASK modulation is done by changing the amplitude of the carrier signal from A_0 to A_1 according to the changing of the data bit stream. The FSK system modulates the signal by changing the frequency of the carrier between f_0 and f_1 as the digital bit changes. For PSK modulation, the phase of the carrier shifts by some defined value (typically a multiple of π/2), when the data bit is changing.

ASK is the most popular method for data transmission used in RFID and IMD applications due to the simplicity of both modulation and demodulation [7]. However, the changing in the amplitude of the carrier signal implies that the transmission power is reduced when the amplitude decreases. The reduced transmission power level might not be adequate to maintain the energy harvesting of the receiver. Similarly, FSK modulation may not be suitable for an inductive loosely coupled wireless power transfer system due to the requirement of a high-Q factor leading to a narrow bandwidth receiver in order to maximise the receiver input voltage, as mentioned in the previous section. As the frequency of the carrier signal changes, the modulated frequency is likely to be attenuated by the antenna LC circuit at the receiver. As a consequence, the receiver may harvest less power when the frequency deviates from nominal. PSK is likely to be the most efficient method for the inductive coupled wireless power transfer, since the amplitude and frequency can be made mostly constant. Hence, PSK could potentially provide the most efficient data rate per available bandwidth and is consistent with maintaining acceptable power transfer compared with ASK and FSK [7, 47]. However, the implementation of a PSK demodulator in the low power receiver might be relatively complex, which eventually causes more power consumption and size compared with ASK and FSK [6, 47, 48].

The PSK modulation scheme is chosen for this project due to the constant frequency and amplitude of the carrier, which is suitable for the wireless inductively loosely coupled energy harvesting system. Several binary phase-shift keying (BPSK) techniques have been proposed [6, 49-51], however, the received voltage at the antenna is likely to be significantly attenuated if the phase of the signal transits from 0 to 180-degree phase shift due to the requirement of a narrow-bandwidth high-Q factor for the receiver coil. Considering the PSK signal during the phase transition, it can be seen that the frequency of the signal during the phase transition period is proportional to the degree of phase shifting since the phase is defined as the rate of change of the frequency over time ($\phi = d\omega/dt$). Hence, the bandwidth of the BPSK signal is wider than the bandwidth of the quadrature-PSK (QPSK) signal. Therefore, the BPSK signal during the phase transition is likely to be attenuated by the narrow-band resonant circuit since the frequency during the phase transition of the BPSK signal deviates from resonant frequency further than the QPSK signal. Figure 3.13 shows the comparison between the amplitude settling time of the BPSK signal and the QPSK signal when Q=33; it can be seen that the QPSK signal requires approximately 15μs to settle the amplitude while the

BPSK amplitude settling time is two times longer. The AC-DC rectified output voltage can be affected by such a slow amplitude response, especially with a higher data rate (i.e., 10kbps) BPSK signal. Therefore, a QPSK modulation is preferable for such applications.

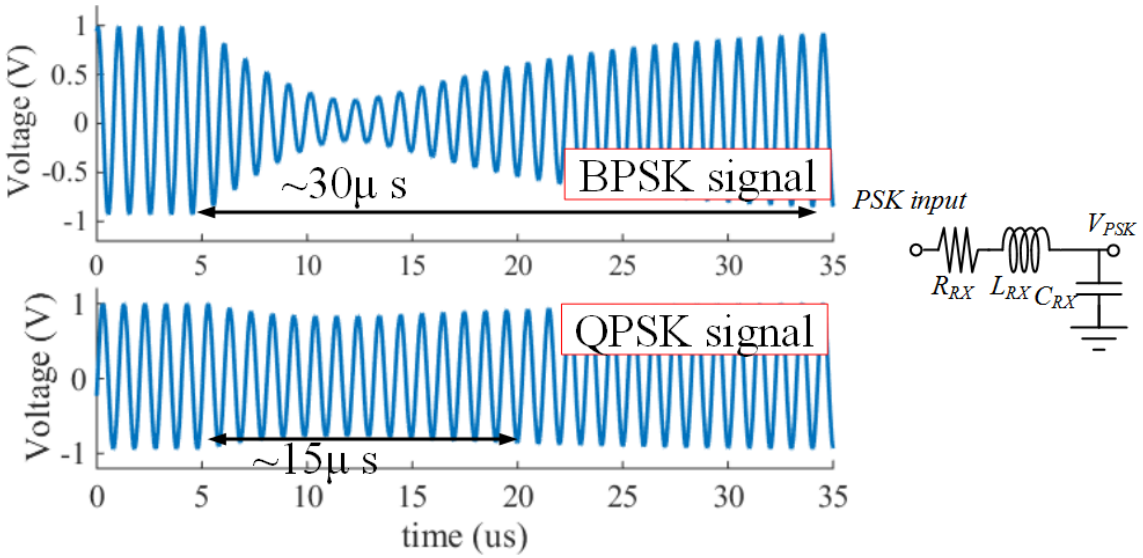


Figure 3.13 Comparison between the amplitude settling time of the BPSK signal and the QPSK signal in the high-Q resonant circuit where Q=33, R_{RX}=10, L_{RX}=53μH and C=478pF.

In the following sections, three practical implementations of the PSK are discussed. Those works might provide some insights in order to design an appropriate PSK demodulator for this project.

3.4.1 Costas Loop PSK Demodulation

Figure 3.14 shows the conventional block diagram of the Costas loop PSK demodulator initially proposed in [52]. The demodulation system consists of three mixer blocks for signal multiplication, which results in subtraction and summation in frequency, a voltage-controlled oscillator, a 90° phase shifter and three low pass filter blocks.

The ideal input data phase modulated signal can be represented by

$$V_{in}(t) = m(t)\sin(\omega_1 t + \theta_1), \qquad (3.16)$$

where $m(t)$ is the modulating data stream. For simplicity in describing the operation, we consider BPSK, such that $m(t)$ can be either 1 or -1, while ω_1 is the carrier frequency and θ_1 is the (arbitrary) phase of the carrier. It can be observed that when $m(t)$ is 1 then the phase is not changing and when $m(t)$ is -1 then the phase of the carrier is shifted by 180°.

When the loop is in a locked condition, the phase differences between θ_1 and θ_2 is close to zero, and therefore the data output at the I Branch is

$$V_{out}(t) = m(t)\cos(\theta_1 - \theta_2) \cong m(t). \qquad (3.17)$$

Hence the digital data bit stream is recovered.

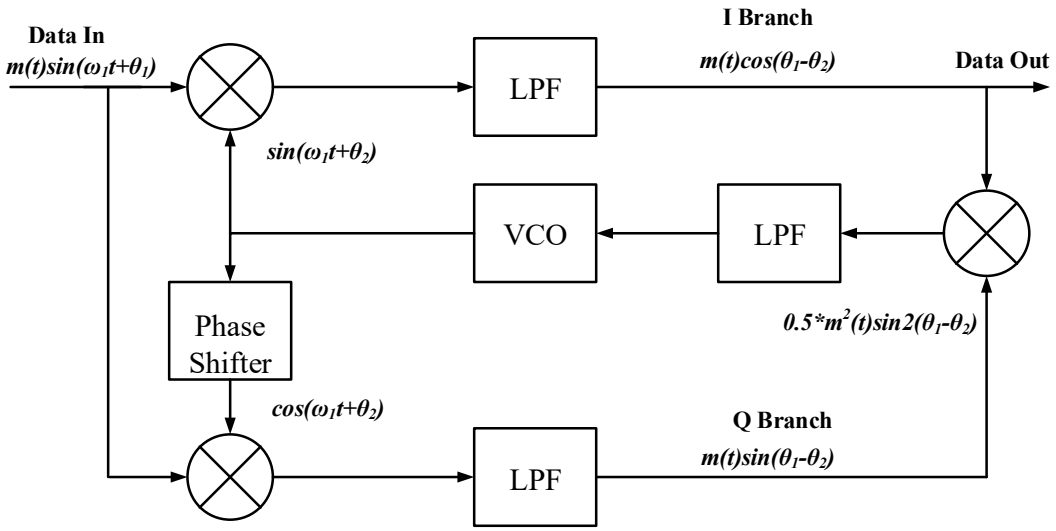


Figure 3.14 Block diagram of the Costas loop PSK demodulator (re-drawn from [52]).

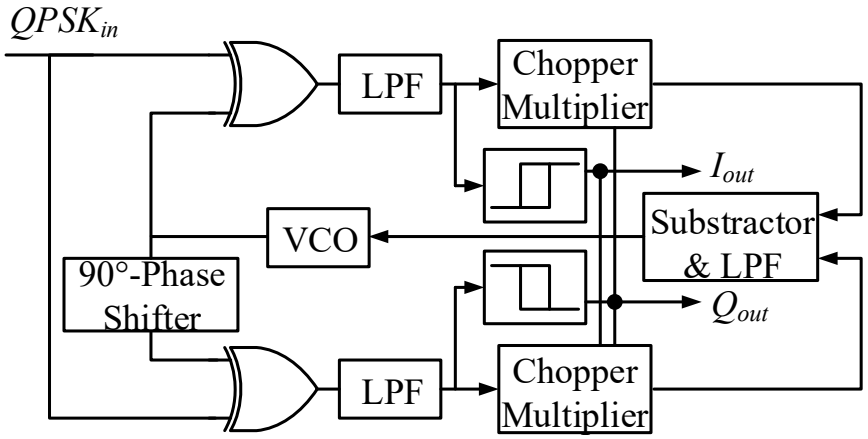


Figure 3.15 The implementation of the Costas loop (re-drawn from [53]).

It can be seen that the original Costas loop requires three analogue multiplier circuits (or switching mixers) and a phase shifter, which are power hungry and complex. Therefore, [6] and [53] proposed the Costas loop where the multiplication and phase shifting are done in the digital domain instead, as depicted in Figure 3.15. Note that the block diagram shown in the figure is the modified Costas loop for QPSK demodulation; two signal multiplication blocks are added to acquire I and Q output data. It can be observed that the received signal is amplified to a digital bit stream where the signals' multiplication is done via XOR logic gates. Moreover, the quadrature generator can be easily implemented from two D-flip-flop circuits.

As the system utilises XOR for phase comparison, the frequency acquisition range is not sufficiently wide. Thus the system employs a conventional phase/frequency detector (PFD), which is commonly used in a phase-locked loop circuit, in order to track the input frequency in the initial state. After the VCO frequency is locked, an ADC converter and an 8-bit register are used to convert and store the VCO tuning input level. As a consequence, the system shifts from using the conventional PFD to the XOR phase detection to demodulate the PSK modulated signal.

3.4.2 BPSK Demodulation using Charge Pump PLL and Trigger and Hold Circuit

Figure 3.16 illustrates the BPSK demodulation proposed by [49], the system utilises the conventional phase/frequency detector (PFD) and a charge pump based phase-locked loop (PLL) to acquire a wide tracking frequency range. The principle of operation of the circuit is described as follows. Initially, the PFD and the charge pump track the input frequency, similarly to a conventional PLL behaviour. When the phase of the input signal is 180° phase shifted, the signal produced by the VCO $CARRIER\_REGEN$ cannot instantaneously track the input phase due to the slow control loop response. In consequence, the XNOR1 detects the phase differences between input signal $BPSK$ and the reference signal $CARRIER\_REGEN$ which results in producing a signal $DATA\_DEMOD$ to switch the path of the PLL loop. As the path of the PLL loop is switched from the non-inverting output of the VCO to the inverting output of the VCO, the phase comparing at PFD becomes zero. Thus, the PLL loop remains in a locked condition. In addition, the data extraction of the system is realised by utilising a trigger and hold circuit to detect the fluctuation of the PLL and hold it for a certain delay defined by the R2-C2 time-constant. It can be seen that this concept can be modified to a QPSK demodulator by generating the I/Q signal used for detecting the incoming signal. However, the data rate used in this system is limited by the slow control loop response. Moreover, the limited loop bandwidth of the system leads to a slow operating frequency lock as a result.

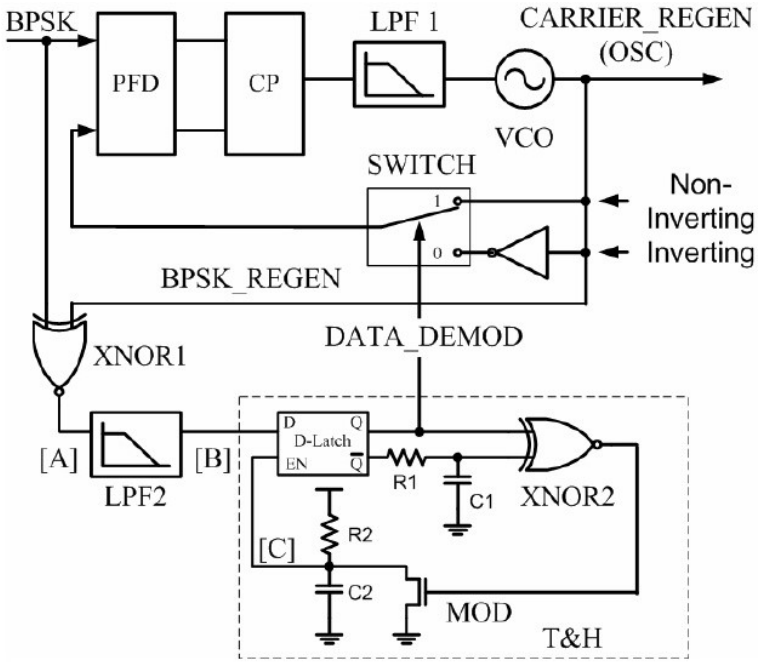


Figure 3.16 BPSK demodulation implemented using charge pump PLL circuit. (Figure from [49].)

3.4.3 PSK Demodulation using Time-to-Digital converter

Figure 3.17 depicts the time-to-digital converter (TDC), which is used to generate a multiple-phase clock for the PSK demodulation. The generated multiple-phase clock is used to sample the incoming

QPSK (or M-PSK) signal, and then a digital state machine control unit can be used to identify the I and Q of the multi-phase clock to match the incoming QPSK signal. In recent state-of-the-art TDC circuit design, the multi-phase clock can be generated by using either a frequency divider [54] or a multi-stage ring oscillator [55]. The TDC frequency-divider-based consumes more power due to the requirement of a higher clock frequency oscillation, thus, the dynamic power ($CV_{DD}^2 f_{in}$) of the system is larger compared with the TDC multi-stage-ring-oscillator-based. On the other hand, the phase accuracy of the multi-phase clock generated by the ring oscillator is process and temperature dependent, hence a larger MOS transistor size may be needed for better accuracy.

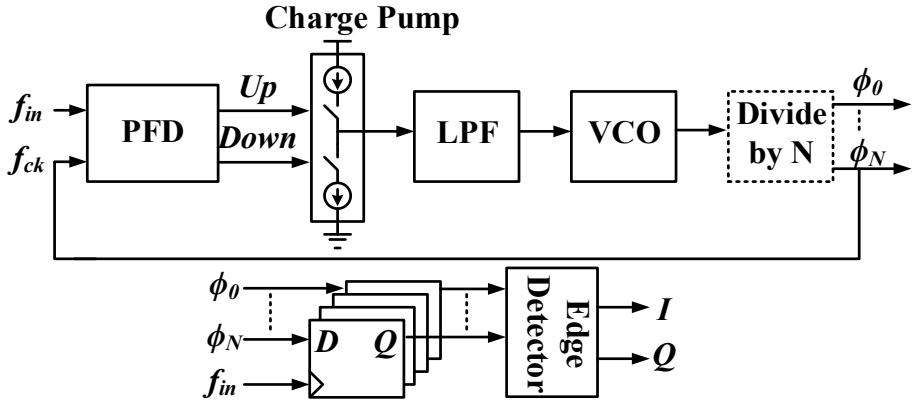


Figure 3.17 Block diagram of the TDC (top) and QPSK signal I/Q detector (bottom).

Table 3.3 Performance of the PSK demodulator.

Work	Costas loop by [6]	Costas loop by [53]	PLL by [49]	TDC by [54]
Process	0.18µm CMOS	0.18µm CMOS	0.5µm CMOS	0.18µm CMOS
Area	0.19mm^2	0.23mm^2	0.1mm^2	2.7mm^2
Frequency	10MHz	13.56MHz	13.56MHz	2.4GHz
Modulation	BPSK	QPSK	BPSK	QPSK
Data rate	1.12Mbps	8Mbps	20kbps	1Mbps
Supply	1.8V	1.8V	3.3V	1.8V
Power	610µW	680µW	3mW	20.4mW
BER	10^{-5}	-	7.58 x 10^{-6}	-

To compare these practical implementations of the PSK demodulator, the performances and specifications are summarised in Table 3.3. By comparing the data rate performance, the implementation of the PSK PLL-based proposed by [49] has the slowest data rate due to the slow PLL control loop response, as explained. It can be seen that the Costas loop PSK demodulation proposed by [6] has the lowest power consumption, which is 610µw. Such power consumption is feasible for the IMD applications as the received power of the implantable devices can be as high as 1mW [3, 7]. However, the received power in this project is potentially in the region of 1 to 100µW. On the other hand, the data rate as high as 100 kbps might exceed the requirements of this work. The data rate of 1 to 10kbps should be sufficient for data communication between the

transmitter and the receiver for this work. Therefore, an alternative system will be proposed in the next chapter.

3.5 Energy Harvesting and Data Demodulator Design Challenges

As the system level of the inductive coupled wireless energy harvesting system has been studied, the design challenges are highlighted as follows:

- Low received voltage at the secondary coil from the ferrite rod antenna might be insufficient for the rectifier to properly start up from cold.
- The magnetic loosely coupled wireless energy harvesting system used for the wireless sensor network requires system synchronisation.
- External modules require sufficient harvested energy to perform tasks.
- The inductance and capacitance values of the receiver LC-tank have to be accurate since the high Q-factor resonant circuit is used to increase the received signal.
- The receiver circuit including the PSK demodulator needs to be ultra-low power since the harvested energy is limited.
- The PSK demodulator needs to be able to demodulate slow transitions limited by the Q-factor of the receiver antenna.

3.6 Summary

In this chapter, an inductive coupled energy harvesting system has been studied. The system synchronisation between the transmitter and multiple receivers allows the receiver to reduce the average power consumption by only activating for a short period. The PSK modulation can be used to transmit the timing information from the source to the receivers which enables the system synchronisation. However, the existing PSK demodulating architectures studied in this chapter consume large power which is undesirable for the low power energy harvesting applications. Hence, the design of the ultra-low power PSK demodulator will be presented in the next chapter.

In addition, the analysis of the AD-DC receiver shows that the loading current of the rectifier can affect the received voltage at the secondary coil. Several rectifier architectures designed to maximise the harvested energy have been studied. The derived equation of the output rectified voltage shows that the rectifier can only start to operate when the input voltage is greater than the diode/transistor forward voltage. As a result, most of the existing rectifier architectures are not suitable in this project since the simulation results of the magnetic energy harvesting system show

that the received voltage can be as low as 250mV_{pk}. Therefore, the rectifier circuit capable of operating with a subthreshold voltage will be proposed in the next chapter.

Moreover, the simulation results of the magnetic field strength and receiver output voltage of the MF inductive coupled energy harvesting system have been presented. The generated magnetic field peaks around its boundary and reduces rapidly when the receiving point moves away from the loop perimeter. The receiver output voltage extracted from the simulation results can be used to define the design specifications of the receiver which will be shown in the next chapter.

Chapter 4: PROTOTYPE WIRELESS ENERGY HARVESTING RECEIVER INTEGRATED CIRCUIT DESIGN

As the system level of the magnetic loosely coupled wireless energy harvesting system has been studied in the previous chapter, several challenges of the system have been highlighted. In this chapter, an integrated circuit (IC) design of the wireless energy harvesting receiver is presented to address those problems. The design specifications of the IC are shown. The system architecture of the IC is proposed and the circuit design of each block is explained.

4.1 Design Specifications

In order to design the energy harvesting receiver, the design specifications are initially defined, as shown in Table 4.1. The minimum amplitude of the input voltage is calculated from the inductive coupling equations that have been demonstrated in section 3.3. Furthermore, the output power delivery required of the energy harvesting receiver is determined from the power consumption of the off-chip external modules which typically comprise a sensor module, a transmitter module and a microcontroller. Appendix D describes the details of the power consumption estimation for each module. In addition, the AMS 0.18µm CMOS process is chosen for this design [46]. As mentioned in Chapter 1, the 180nm standard CMOS process is suitable for this project because of its cost and the transistor threshold voltage (V_{th}).

Table 4.1 Design specifications of the energy harvesting receiver.

Parameters	Value
Minimum amplitude of the input voltage*	250mV_{pk}
Input frequency	500kHz – 2MHz
Output power delivery	34mW for 4ms (Active) 0.2314µW (Idle)

*Calculated from the specifications shown in Table 3.2, section 3.3.

4.2 System Architecture

Figure 4.1 shows the simplified system architecture of the medium frequency (MF) inductive coupled wireless energy harvesting receiver IC. The system consists of a rectifier, a quadrature phase-shift keying (QPSK) demodulator and a power management unit (PMU). The rectifier converts the harvested MF magnetic energy with the frequency between 500kHz and 2MHz to a DC voltage V_{rect} in a range of 0.9V to 1.8V for storage in an off-chip capacitor C_1. Moreover, the data modulated with the harvesting energy is demodulated by the QPSK demodulator to extract the data

for external modules. The demodulator can be activated and deactivated by the power management unit (PMU) depending on the supply voltage level provided by the rectifier. Furthermore, the PMU provides a clean regulated DC voltage V_{DD} to supply the demodulator. Since the voltage provided by the rectifier is not sufficient for typical off-chip external functions such as a microcontroller or a UHF uplink transmitter, a DC-DC converter (charge pump) in the PMU boosts the low voltage V_{rect} to 3V DC output voltage V_{CP} which is stored on the off-chip capacitor C_2.

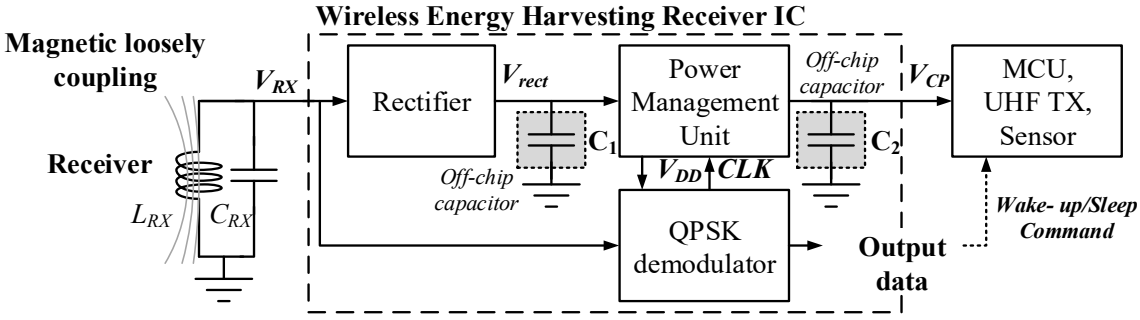


Figure 4.1 Simplified system architecture of the energy harvesting system.

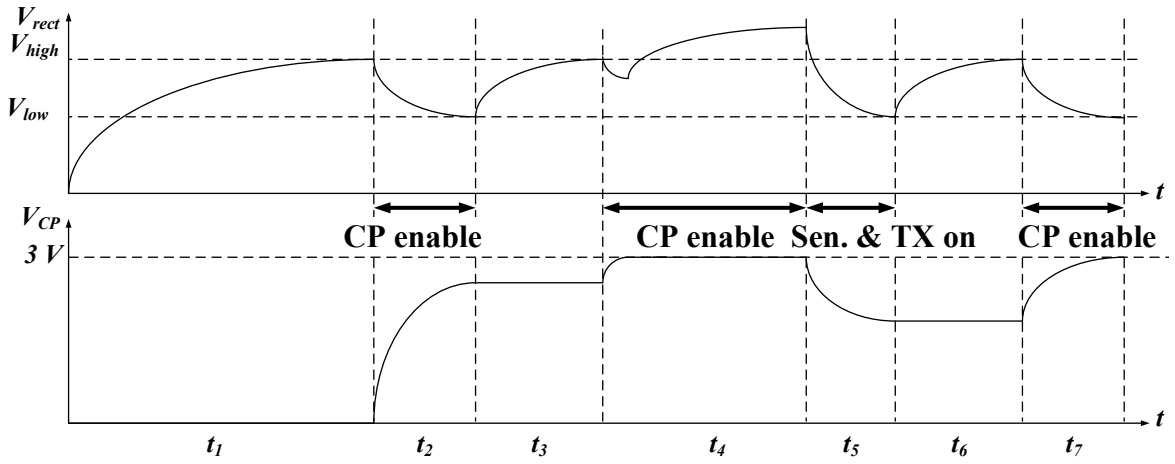


Figure 4.2 Timing diagram of the energy harvesting power management scheme. V_{rect} is the rectifier output voltage storage on the capacitor C_1 and V_{CP} is the DC-DC converted voltage from the power management unit storing energy in capacitor C_2.

The timing diagram of the start-up power supply behaviour of the energy harvesting receiver IC is depicted in Figure 4.2. The diagram consists of the transient behaviour of V_{rect} from the output of the rectifier and V_{CP} from the DC-DC charge pump (CP) circuit of the PMU. The timing diagram can be explained as follows. Initially, the rectifier charges the off-chip capacitor C_1 from cold. Once V_{rect} reaches V_{high}, the PMU enables the DC-DC conversion. As the CP is enabled, a large current is drawn from the capacitor C_1 and the rectifier which may potentially reduce V_{rect}. When the voltage level of V_{rect} drops below V_{low}, the CP is disabled, as shown in the timing diagram between period t_2 and t_3. At t_4, the CP resumes activating as V_{rect} climbs back to V_{high}. When the sensor node is expected to collect the data and transmit the signal back to the source, the current is drawn from the capacitor C_2. Consequently, V_{CP} decreases as in t_5. It can be seen that the reduction of V_{CP} might affect V_{rect}, thus properly chosen capacitor sizes are needed. This is because the rectifier output

needs to provide more power to the CP when the CP output current is drained by external modules, thus V_{rect} may decrease depending on the harvested voltage level at the receiver. Note that V_{low} is defined based on the minimum voltage needed to supply the receiver circuits sufficiently.

The calculation of the size of the storage capacitors is determined from the current consumption and the activation time of the external modules [12]. As shown in Table 4.1, the average current consumption of the external modules is expected to be approximately 11mA for a 4ms period. By using equation (4.1), the capacitance of C_2 is calculated as approximately 115µF. More details of the analysis can be found in Appendix D. On the other hand, the capacitor C_1 can be calculated from the output current provided by the rectifier i_{c1}, the voltage difference between V_{high} and V_{low} and the period t_2.

$$C = \frac{i(t)}{\frac{dv(t)}{dt}}. \qquad (4.1)$$

4.3 Circuit Design

As the harvested energy from the secondary coil of the inductive loosely coupled energy harvest is limited, an ultra-low power circuit design is needed to ensure that the receiver IC can properly operate under the constrained conditions. The circuit implementation of each block presented in Figure 4.1 is briefly explained in the following sections.

4.3.1 Rectifier

In this project, the receiver rectifier is required to convert the input voltage from the antenna coil with the amplitude as low as 250mV$_{pk}$. However, the MOS transistor V$_{th}$ of the chosen process technology is typically at 350mV for NMOS (V$_{thn}$) and 400mV for PMOS (V$_{thp}$). As a result, the conventional voltage multiplier circuit presented in section 3.2.2 is not suitable for the application due to the resulting forward bias voltage issue. Hence, a rectifier operating under the subthreshold voltage condition is presented in this section.

4.3.1.1 Switch-over Cold-start Subthreshold Voltage Rectifier

The proposed subthreshold voltage rectifier is designed based on the concept of a MOS transistor subthreshold operation where the transistor in the subthreshold region can still weakly drain a small nA current depending on the transistor dimensions. Figure 4.3 shows that the PMOS transistor connecting in a self-Vth cancellation rectifier (SVC) configuration can conduct an asymmetrical leakage current when the input voltage is below the MOS V$_{th}$. It can be seen from the simulation result that the output current of the PMOS when the input is positive is larger than the current

when the input is negative, this is because the gate-to-source voltage (V_{GS}) of the PMOS is larger when the input voltage is positive compared with the PMOS V_{GS} when the input is negative. Hence the SVC can generate a small output DC voltage when the input voltage is below the MOS V_{th}.

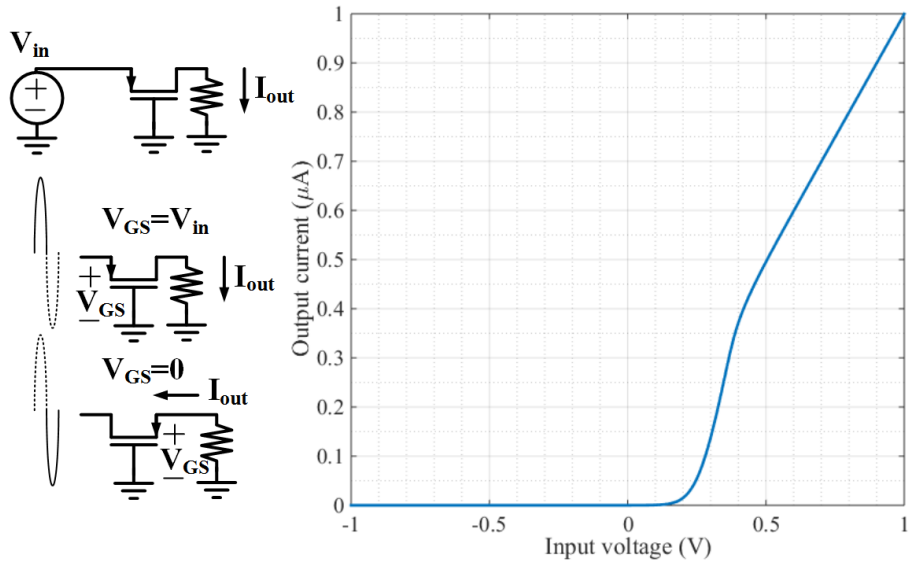


Figure 4.3 Output current versus DC input voltage of the single-stage SVC rectifier.

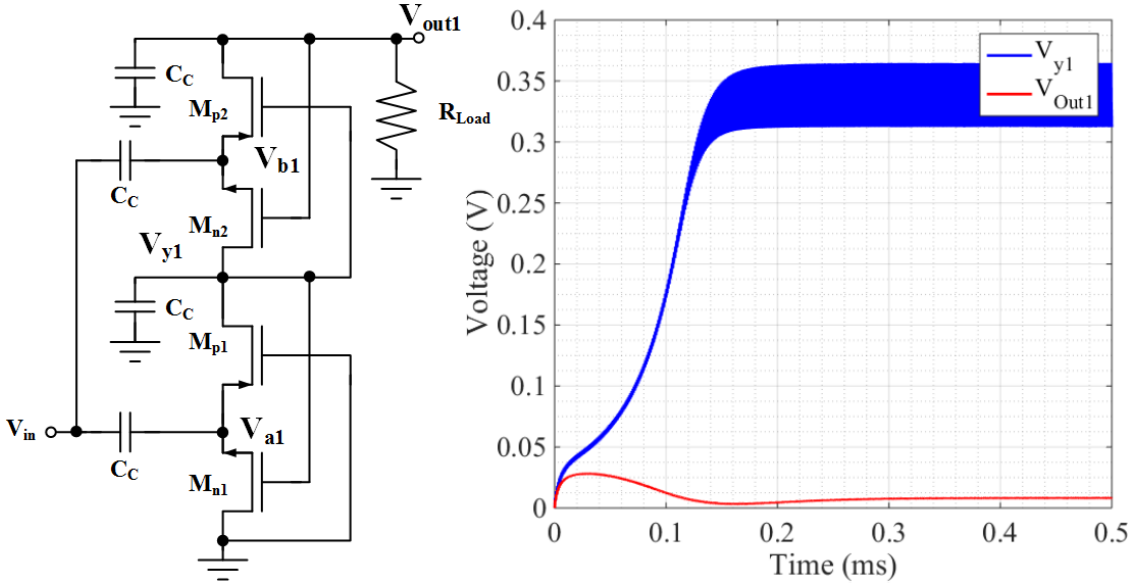


Figure 4.4 Two-stage SVC circuit (left) and the transient simulated voltage behaviour when the input voltage is below the MOS V_{th} (right). The input voltage signal is at 250mV$_{pk}$ while the loading resistance is 500kΩ.

However, the SVC circuit under a subthreshold operation cannot provide a usable DC output voltage to supply the receiver system. Figure 4.4 shows the two-stage SVC circuit and the internal voltage behaviour when the input voltage is below the V_{th} of the transistors. Although the input voltage is not sufficient to fully activate all the transistors, the coupling capacitor C_C at the voltage node V_{y1} at the first stage of the SVC is still being charged by a weak asymmetric leakage current, as described above. Since the node V_{y1} is not loaded by a resistor, the transistors M_{n1} and M_{p1} are biased by the built-up voltage from the leakage current. On the other hand, the output voltage of the rectifier

(V_{out1}) is much lower than the voltage node V_{y1} due to the loading resistor R_{Load}. Consequently, the transistor M_{n2} is conducting in the opposite direction at t=0.1ms (the current is flowing from node V_{b1} to V_{y1} instead) which causes V_{out1} to decrease further as a result.

Figure 4.5 illustrates the proposed subthreshold voltage rectifier circuit developed from the SVC and the internal V_{th} cancellation rectifier (IVC) circuits and its transient simulated voltage behaviour when input voltage is below the MOS V_{th}. The PMOS transistors M_{p1} to M_{p3} are biased by the rectified voltage of the adjacent stages as in the SVC circuit while the NMOS transistor M_{n1} is biased by the DC voltage V_{d0} provided by the diode-connected MOS M_{n2}. Similarly to the SVC, the output voltage V_{y2} at the first stage is initially charged by a net forward leakage current while the output V_{out2} is limited by the loading resistor as expected. However the PMOS transistors are biased by the adjacent voltage nodes that are not connected to any resistors, consequently the output voltage is increased as the effective V_{th} of the PMOS transistor is reduced. As the bias voltage V_{d0} is increased similarly to the output voltage, the effective V_{th} of the transistor M_{n1} is reduced. As a result, the subthreshold voltage rectifier can rectify an input voltage that is lower than the V_{th} of the transistor since the transistors are properly biased. As the proposed rectifier depends on the leakage current to decrease the input start-up voltage of the rectifier, the start-up voltage can be adjusted by increasing/decreasing the MOS dimensions. Note that the number of stages of the proposed rectifier (and thus the voltage multiplication ratio) can be increased by replicating the second stage (M_{p2} and M_{p3}) of the circuit.

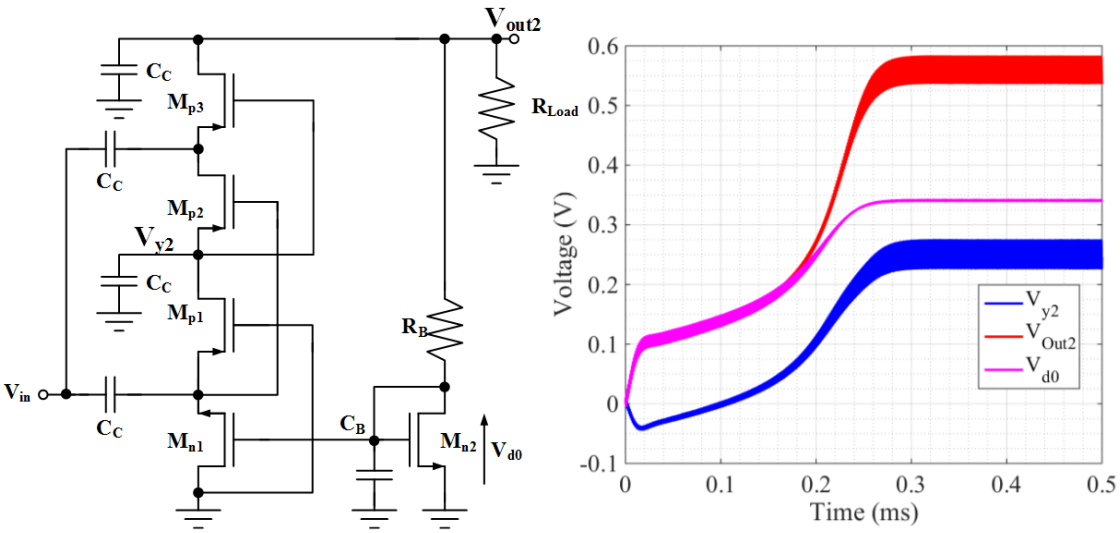


Figure 4.5 Proposed subthreshold voltage rectifier (left) and the transient simulated voltage behaviour when the input voltage is below the MOS V_{th} (right). The input voltage signal is at 250mV_{pk} while the loading resistance is 500kΩ.

The 4-stage implementation of the proposed rectifier with optimised MOS dimensions is simulated using the Cadence CAD tool where the AMS 0.18µm HV CMOS Process [46] is chosen for this design; the optimised transistor aspect ratios are 10/0.2 for NMOS transistors and 140/0.2 for PMOS

transistors. The plots of output voltage and power conversion efficiency (PCE) versus sinusoidal input voltage with the frequency of 1MHz when the output is driving the load of 500kΩ is shown in Figure 4.6. It can be seen that the rectifier can rectify when the input voltage is as low as 250mV$_{pk}$, which is lower than the V_{th} of both NMOS and PMOS of this process (V_{thn}=350mV and V_{thp}=450mV). On the other hand, the PCE result of the rectifier indicates that the efficiency of the rectifier decreases when the input voltage is increased above a given value, which is similar to the behaviour of the SVC rectifier. This is due to the reverse leakage current which starts to increase when the input voltage is too large.

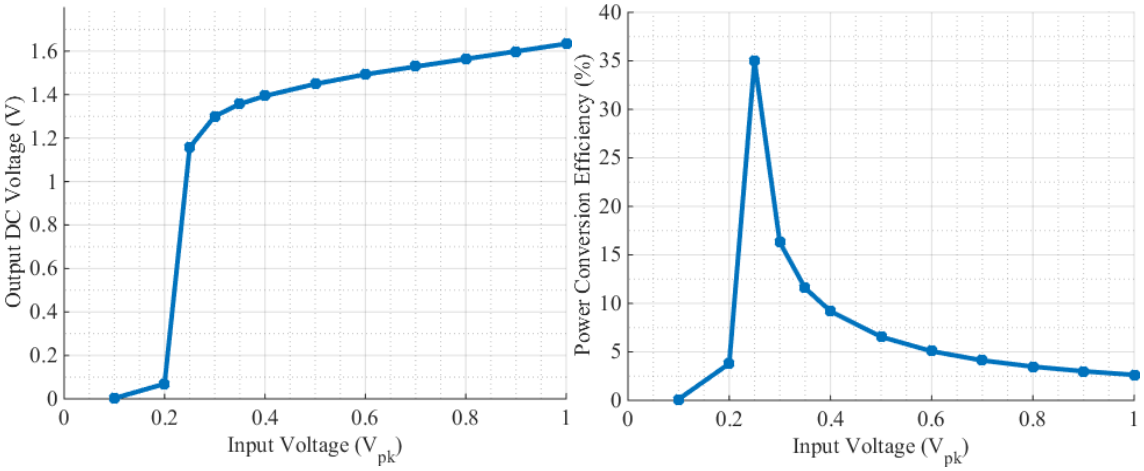


Figure 4.6 Output voltage (left) and PCE (right) versus input voltage of the proposed voltage rectifier when the operating frequency is 1MHz and the load is 500kΩ.

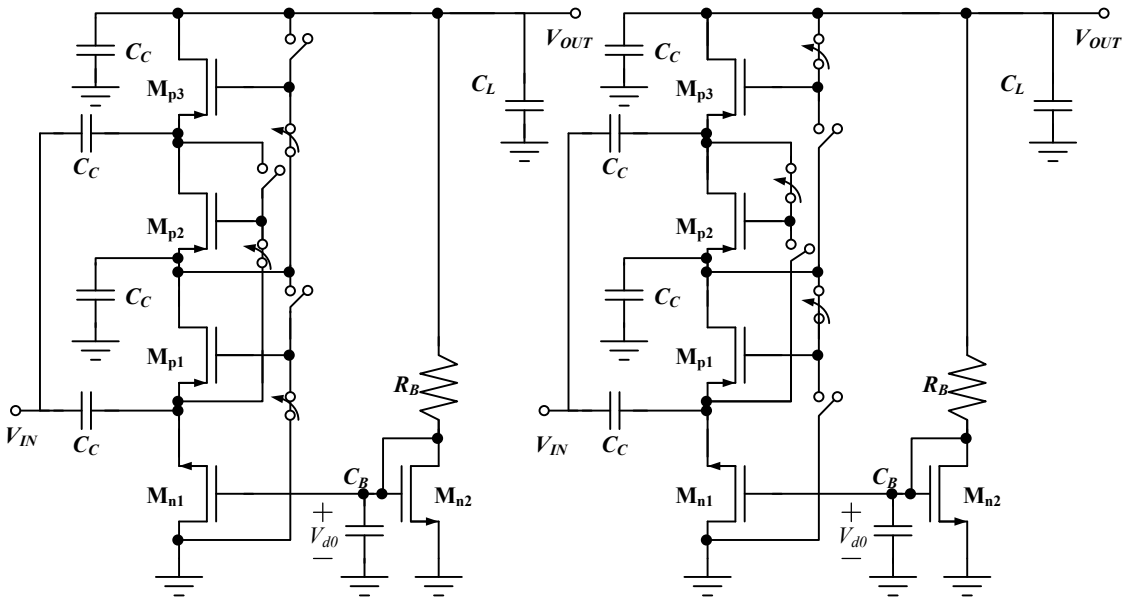


Figure 4.7 A switching between two rectifier circuit configurations of the proposed two-stage voltage rectifier. Left: When the input voltage is relatively low compared to the MOS V_{th}. Right: When the input is relatively large.

The proposed circuit is further developed in order to improve the PCE of the circuit when the input voltage is large. It can be seen from the simulation result shown in Figure 3.8(b) that the PCE of the conventional voltage multiplier is better than other circuits when the input voltage is large. Thus,

switches are added in order to change the gate connection of the PMOS from SVC configuration to voltage multiplier configuration, as illustrated in Figure 4.7. When the input voltage is low, the gate of the PMOS is connected to the adjacent channel to form the SVC configuration. On the other hand, the PMOS is connected to its drain to form the diode-connected configuration when the input voltage is larger [11, 14].

However, the included switches for the rectifier switch-over are not functioning when the system is starting from cold where there is no energy storage in the output capacitor to control the switches. Therefore, an additional capacitor is added in parallel with the switch that is connected between the gate and the adjacent channel of the PMOS, as shown in Figure 4.8. The figure presents the proposed switch-over cold-start voltage rectifier circuit. At cold-start where all switches are OFF, the parallel capacitors C_{SW} connect the gate of the PMOS with the adjacent MOS drain node enabling the circuit to weakly rectify the incoming AC signal under cold-start conditions. When the rectifier DC output voltage V_{OUT} is sufficiently large to supply a comparator used for driving the switches, the switches take over the parallel capacitors and properly operate in order to improve the efficiency of the rectification, as described above.

Figure 4.9 presents the PCE simulation result of the proposed 4-stage rectifier operating in the high voltage input mode compared with the result of the low voltage subthreshold mode shown in Figure 4.6. It can be seen that the efficiency of the rectifier operating in the high voltage mode increases when the input amplitude is increased, as expected.

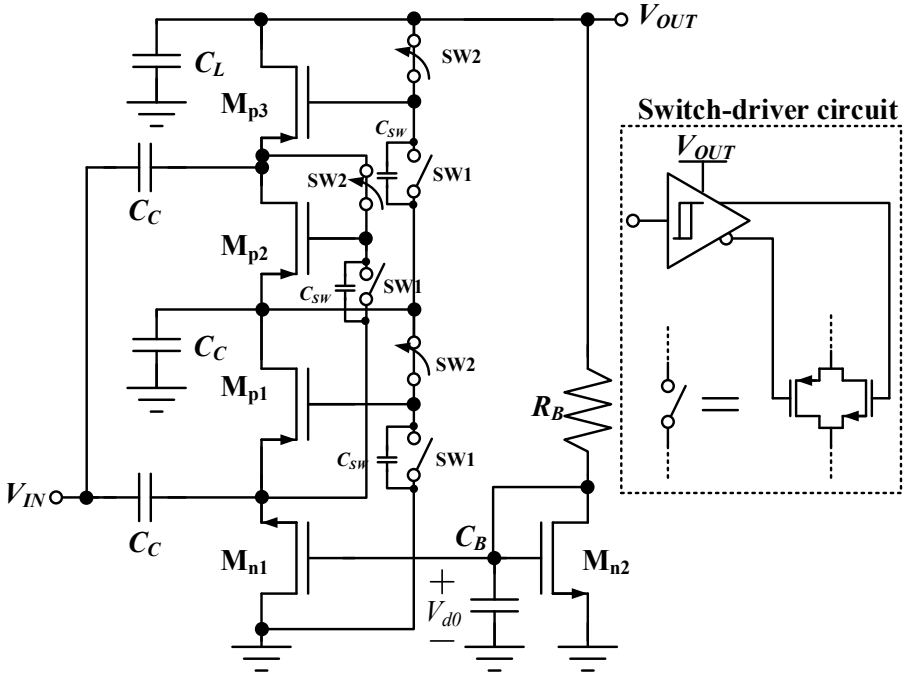


Figure 4.8 Proposed switch-over cold-start subthreshold voltage rectifier.

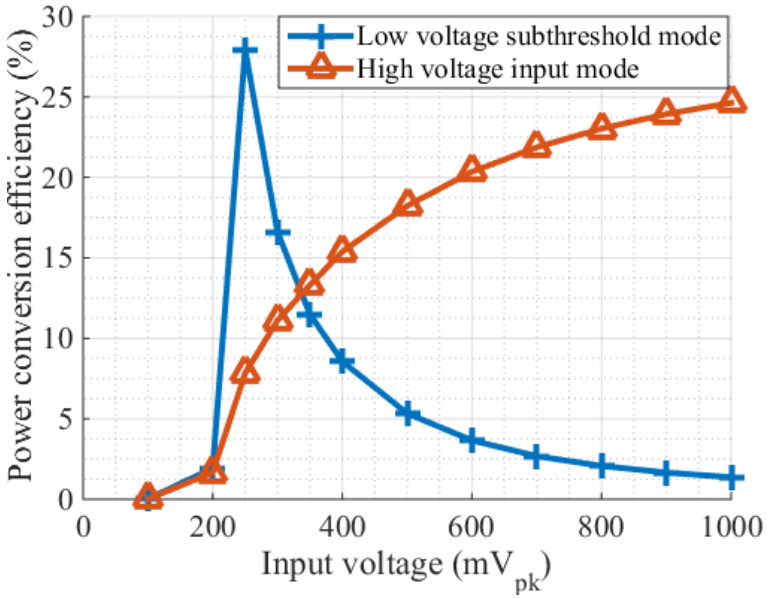


Figure 4.9 PCE versus peak input voltage of the proposed rectifier with two different configurations when the operating frequency is 1MHz and the load is 500kΩ.

4.3.1.2 Switch-over Detection

As the proposed rectifier switches the configuration according to the amplitude of the incoming signal, a voltage amplitude detection circuit is needed in order to make a decision for the switch-over. For simplicity and low power consumption, the proposed switch-over detection circuit depicted in Figure 4.10 is used to detect the incoming voltage amplitude for the switch-over efficiency enhancement. The circuit consists of a dummy rectifier implemented from a simple PMOS diode-connected half-wave voltage rectifier and an ultra-low power comparator supplied by the rectifier output voltage V_{OUT}. The power consumption of the dummy rectifier is negligible compared with the main rectifier since the circuit is unloaded by any resistors. The circuit operates as follows; the input signal is rectified to DC voltage V_{dummy} by the dummy MOS rectifier M_{dummy}. Then the dummy voltage is compared with the voltage produced by the diode-connected V_{d0} of the main rectifier circuit. Due to the forward-bias voltage issue of the dummy rectifier if the input voltage V_{IN} is lower than the PMOS threshold V_{thp}, then the voltage V_{dummy} will likely be smaller than the internal voltage from the main rectifier V_{d0}. Thus, the switches of the cold-start rectifier connect the gate of the PMOS with the adjacent channel to form the SVC configuration. On the other hand, when the input voltage is sufficiently large (i.e., becoming larger than the MOS V_{th}), then the value of V_{dummy} is larger than the V_{d0}. Hence, the switches connect the gate of the PMOS to the drain to form a basic voltage multiplier rectifier.

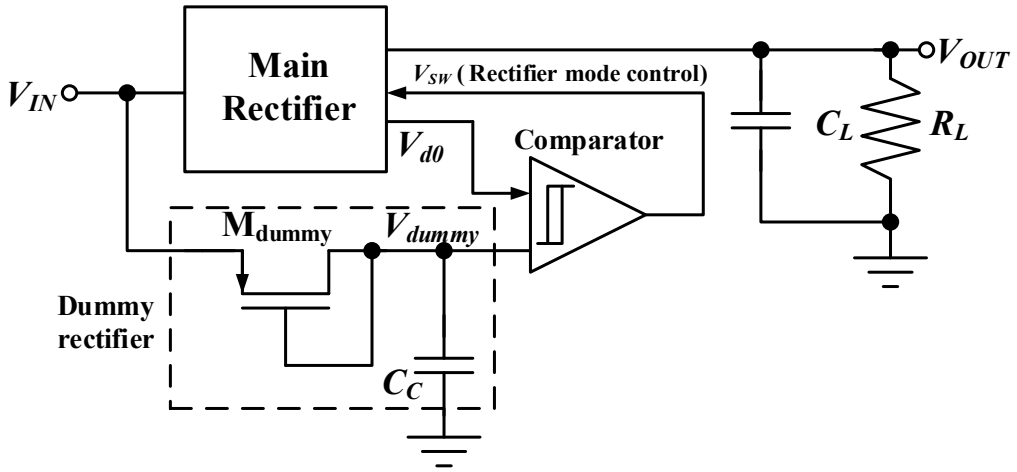


Figure 4.10 Proposed switch-over detection circuit.

Figure 4.11 shows the schematic diagram of the comparator for the switch-over detection circuit. The comparator utilises a positive feedback path to provide a hysteresis characteristic [56] and an inverter at the second stage to provide the inverted output signal. The hysteresis comparator is needed as the inputs of the comparator might potentially be noisy. Furthermore, it can be observed from the figure that the current of the output inverter is limited by the current source I_{REF}. The current limiting of the inverter is needed because the inputs of the NMOS pair V_{in+} and V_{in-} may cause the output to be in the transition region for a significant time, so that it might turn both PMOS and NMOS of the inverter ON and cause a current path from supply to ground through the output inverter. As the circuit supply source is provided by the rectifier circuit which has very high resistance, the local supply voltage may collapse even with a few µA current drain on the supply for a significant time. Moreover, the input is implemented from the NMOS pair since the input voltage may potentially vary from 0.3V to 1.8V. Note that the upper voltage limit 1.8V is limited by the breakdown voltage of the CMOS process used in this project [46]. The 1.8V limiter circuit will be shown later in this chapter. In addition, the current sources of the comparator are implemented from a conventional NMOS current mirror [56, 57] where the current reference I_{REF} is injected from the reference circuit, which will be shown later. The circuits (both comparator and reference generator) can only start to operate when the output rectifier is at least 0.4V which is determined by CMOS process V_{th}.

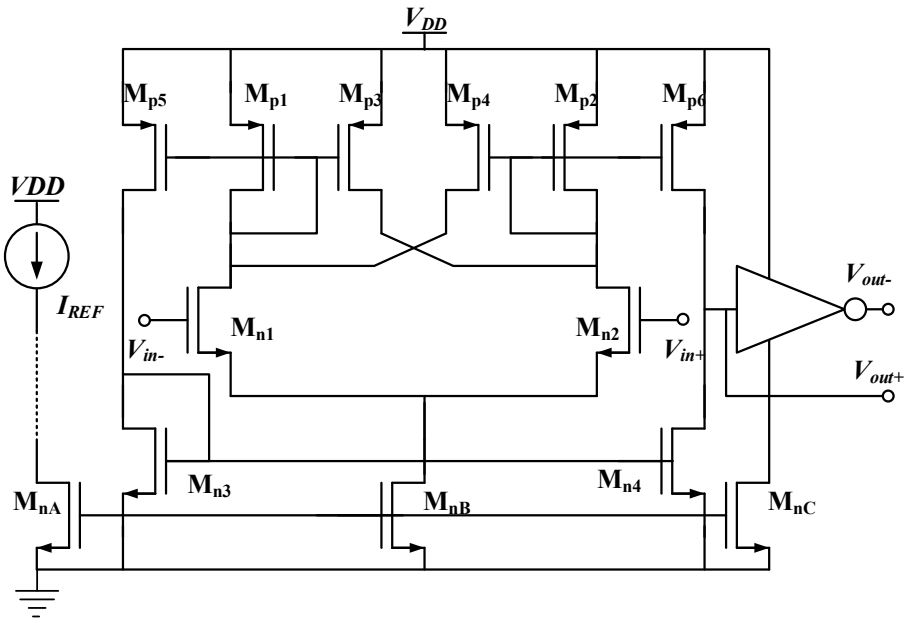


Figure 4.11 Schematic view of the comparator for the rectifier.

The comparator for the rectifier switch-over detection is simulated with transient and DC analysis when the reference current is generated by an ideal current source. The peak of the current consumption during the output transition is approximately 70nA. The current consumption of the comparator for the steady-state condition where the comparator is fully switched is approximately 25nA at the 1V supply voltage. Moreover the hysteresis voltage of the comparator is at 100mV at the nominal condition. As the results can be varied across the process voltage and temperature variations (PVT) for the transistor parameters [56, 57], PVT corners simulation results of the comparator indicate that the variation of the hysteresis voltage is approximately 10mV. In addition, the simulation result verifies that the comparator can operate with the minimum supply voltage of 400mV. The plots of the DC and transient simulations of the comparator can be found in Appendix E.1.

4.3.1.3 Top-level Simulation

The four-stage switch-over cold-start subthreshold voltage rectifier circuit and layout are implemented in the first IC design. The capacitance values of 1nF, 100pF and 12pF are chosen for the loading capacitor C_L, the coupling capacitor C_C and the parallel capacitor C_{SW} respectively. The coupling capacitor C_C is selected such that the impedance ($Z_C = {}^{1}/_{j\omega C}$) of the capacitor is considered to be small for the operating frequency between 500kHz to 2MHz used in this project. On the other hand, the parallel capacitor C_{SW} does not need to be as large since the capacitor is only for the start-up condition; C_{SW} is not needed when the output voltage is sufficiently large to enable the switches. The capacitors are implemented using the metal to metal capacitor (CMIM) structure which provides high capacitance per unit square area in this CMOS process. However the parasitic

capacitance from the metal-to-substrate, which is proportional to the capacitor sizes, is undesirable for the coupling capacitor C_C connecting between the receiver antenna output node (V_{RX}) and the rectifier input. The parasitic capacitance can be removed by connecting the bottom-side metal plate to the antenna output V_{RX} which results in connecting the parasitic capacitor to the LC-antenna instead. Note that the NWELL capacitor could provide more capacitance per unit square area (depending on the shape/dimensions), however it is not suitable for this design since one end of the capacitor is always connected to the substrate. Also, the NWELL capacitor breakdown voltage is much smaller than the CMIM capacitor.

The proposed 4-stage switch-over cold-start voltage rectifier and the switch-over detection circuit are connected together and simulated by applying the input voltage with the frequency of 1MHz stepped from $0.1V_{pk}$ to $1V_{pk}$ when the output load is 500kΩ. Figure 4.12 shows the plots of the output DC voltage and the PCE of the circuit. It appears that the rectifier can start up when the input voltage is as low as $250mV_{pk}$, similar to the previous simulation result for the basic subthreshold rectifier. Moreover, the PCE and the output voltage are improved when the input voltage is large compared with the previous simulation result. It can be observed that the PCE of the rectifier drops at the input voltage between $300mV_{pk}$ and $400mV_{pk}$. This is because the rectifier is operating in the subthreshold mode which causes large reverse leakage current when the input voltage is relatively large. The configuration of the rectifier is switched from the subthreshold mode to the high voltage mode when the input voltage is above $400mV_{pk}$, and thus the PCE rises when the input voltage increases. Note that the efficiency drop of the rectifier when the input is between $300mV_{pk}$ and $350mV_{pk}$ cannot be mitigated by switching the rectifier configuration since the high voltage mode rectifier cannot properly start up due to the insufficient forward-bias voltage of the PMOS transistor, as shown in the previous simulation result from Figure 4.9. In addition, the output voltage of the rectifier will be larger than 1.8V when the input is relatively large, which is greater than the maximum voltage allowed for the thin oxide MOS devices in this process. Thus, a voltage limiter circuit is required in order to protect other building block circuits.

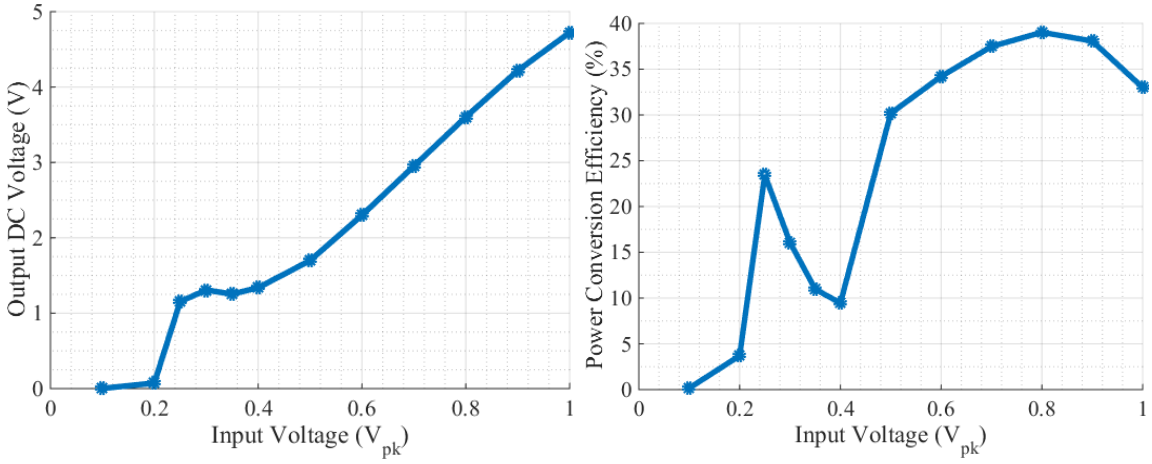


Figure 4.12 Output voltage (left) and PCE (right) versus input voltage of the switch-over cold-start rectifier when the operating frequency is 1MHz and the load is 500kΩ.

4.3.2 Data Demodulator

As mentioned in section 3.4, a QPSK modulation scheme is preferable due to the shorter amplitude settling time that leads to less average signal attenuation of the received signal compared with the BPSK signal. An ultra-low power QPSK demodulator is presented in this section.

Considering the QPSK signal (V_{in}) and the square wave of the sliced QPSK signal (*PLLin*) shown in Figure 4.13, it can be seen that the maximum phase transitions per second of *PLLin* is synchronised with four times the phase transition of the carrier frequency of V_{in}. For instance, if the carrier frequency of V_{in} is 1MHz then the sliced QPSK signal maximum phase transitions rate is 4M pulse-per-second. A clock and data recovery (CRD) system, which recovers a clock signal that is insensitive to missing pulses of the incoming data [20, 58], can be used to create a stable reference square wave signal with the same frequency as the carrier of the QPSK signal called *PLLref*. As a result, the QPSK output data can be extracted from the XOR operation between *PLLin* and *PLLref*, as depicted in Figure 4.13.

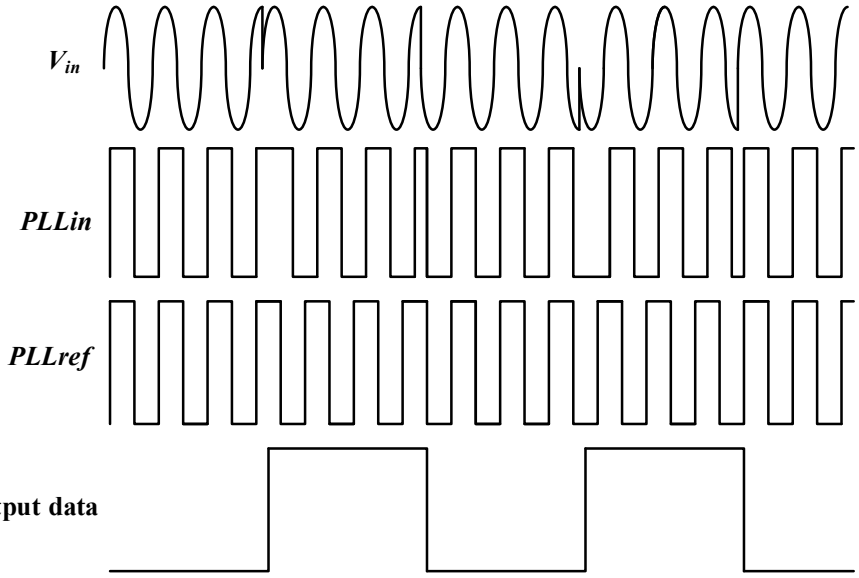


Figure 4.13 Concept of the proposed QPSK demodulator. V_{in} is the incoming QPSK signal, *PLLin* is the amplified input signal, *PLLref* is the reference signal and Output data is the output from the QPSK data extraction.

Figure 4.14 presents the proposed system architecture of the QPSK data demodulator for the wireless energy harvesting receiver. The system has a dual-loop operation that can switch between the phase-locked loop (PLL) mode for the frequency locking and the CDR mode for the data extraction. The proposed system consists of an amplifier, the Phase/Frequency detector (PFD), the Hogge phase detector (PD), the PLL charge pump, a multiplexer, a low-pass filter (LPF), a voltage-

controlled oscillator (VCO), a frequency divider, a lock detection circuit and a data detection circuit. The Hogge PD based CDR PLL detects the incoming pulses (V_{in}) to recover a stable reference clock, however the frequency capture range of this type of PD is not sufficiently large to ensure reliable start up for the system, since the VCO is designed from a ring oscillator which has a very wide output frequency range. Hence the PLL mode is enabled initially for the frequency locking from an out-of-lock condition. In addition, the Hogge PD is chosen because its phase detector gain (K_{PD}) is similar to the K_{PD} of the PFD if the incoming pulses are continuous (The K_{PD} is different for the incoming NRZ signal). The loop stability of the system is thus unlikely to be affected by the transition from the PLL mode to the CDR mode. Note that the VCO clock frequency is locked at four times of the QPSK carrier because the Hogge PD based CDR PLL requires the clock frequency to synchronise with the input phase transitions rate which is four times that of the carrier, as explained earlier.

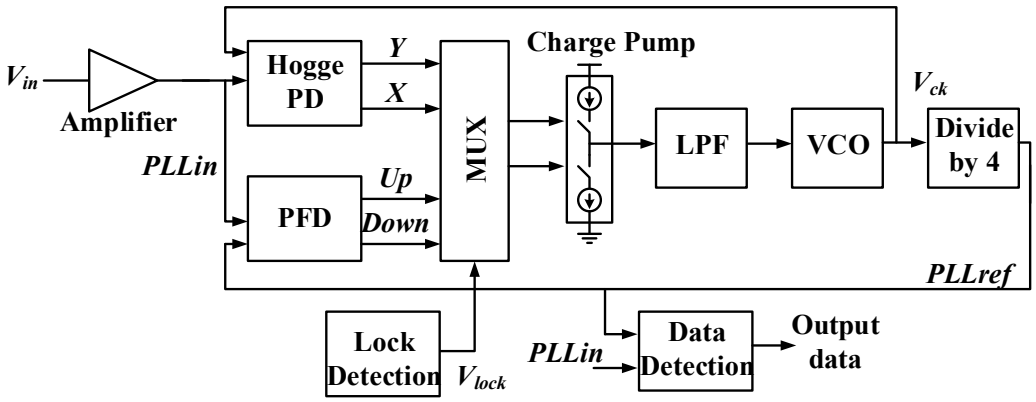


Figure 4.14 System architecture of the proposed QPSK data demodulator.

The data demodulator operates as follows. When the demodulator is enabled by the PMU, the demodulator is initially configured to use the PFD to enable the lock condition to be found. The input amplifier amplifies/limits the incoming signal received from the antenna to a digital level, dictated by the local supply. The amplified signal *PLLin* is initially compared with the VCO output divided by four (*PLLref*) by the PFD. Thus, the frequency of the VCO is four times the frequency of *PLLin*. When the lock detection circuit detects that the VCO frequency is locked to the received signal, the Hogge PD takes over the phase detection of the system. In this case, the Hogge detector takes the VCO output directly at four times the input frequency so that there will be a phase transition in the reference that matches the four possible phase conditions in the QPSK modulated input signal. Similarly to the typical behaviour of a CDR system, the proposed demodulator is not sensitive to missing pulses and will remain in lock despite the imposed QPSK modulation. Therefore, the data detection can sense when the input phase is changed by comparing the signal with the stable phase reference produced by the VCO.

The control loop design of the proposed system is explained in Appendix F. Before the demodulator's circuits are implemented, the demodulator control loop model is firstly verified in

MATLAB to ensure that the loop is stable [59]. In the next section, the operation of the CDR PD used for locking the reference frequency to the incoming "data", in this case in the PSK/QPSK signal, will be explained.

4.3.2.1 Phase Detector

The CDR PD is used to recover a clock signal that is aligned synchronously to the incoming random data such that the rising edge of the lock is at the midpoint of each bit of the input data, which leads to providing a maximum margin for the clock jitter. Moreover, the frequency of the recovered clock must be at least two times the incoming input frequency (or equal to the data rate of the input data, i.e., 1MHz clock frequency for 1Mbps data). To understand how the CDR PD locks the reference frequency to the missing-pulses-incoming-data, we firstly consider a simple PD implemented from a D-type flip-flop (DFF) and an XOR logic gate, as illustrated in Figure 4.15. We assume that a reference clock (*CK*) has a phase transitions rate that is equal to the maximum data rate of the input pulse (D_{in}). It can be seen that the PD can produce an output signal *Y* according to the lag/lead of the reference *CK* to the input data, and then the average voltage of the output signal *Y* (highlighted in grey colour in the figure) can be used to compensate for the phase of the clock using a PLL control loop. Moreover, it can be seen that the average voltage of the output signal *Y* remains unchanged if the random input data transition is missing. Note that this is only true if the input data is random or continuously having a phase transition.

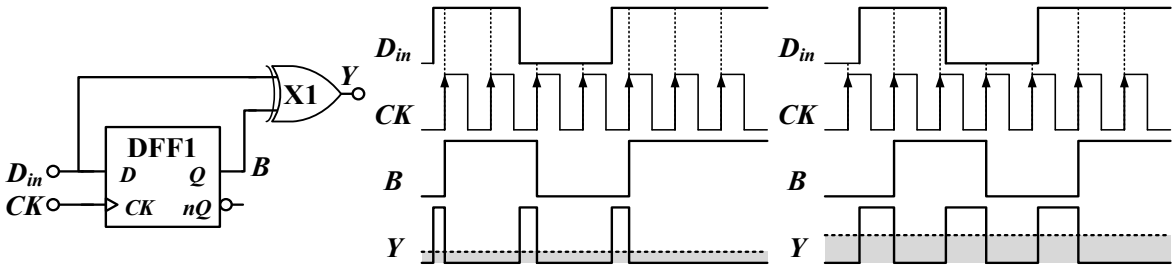
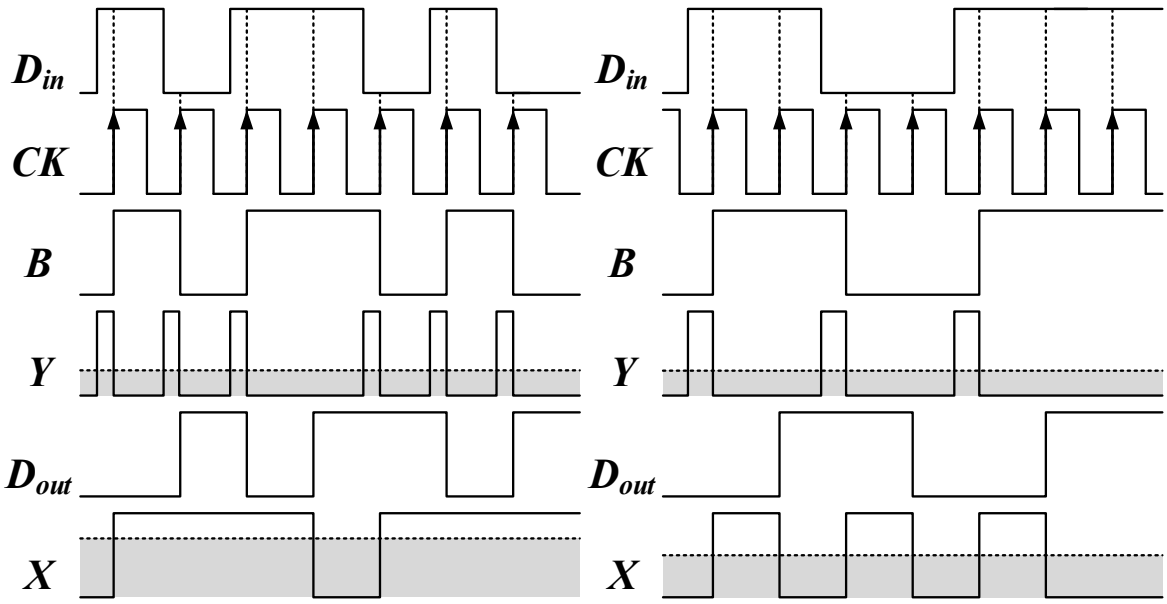


Figure 4.15 Schematic view of a simple PD using a DFF and an XOR gate and its timing diagram.

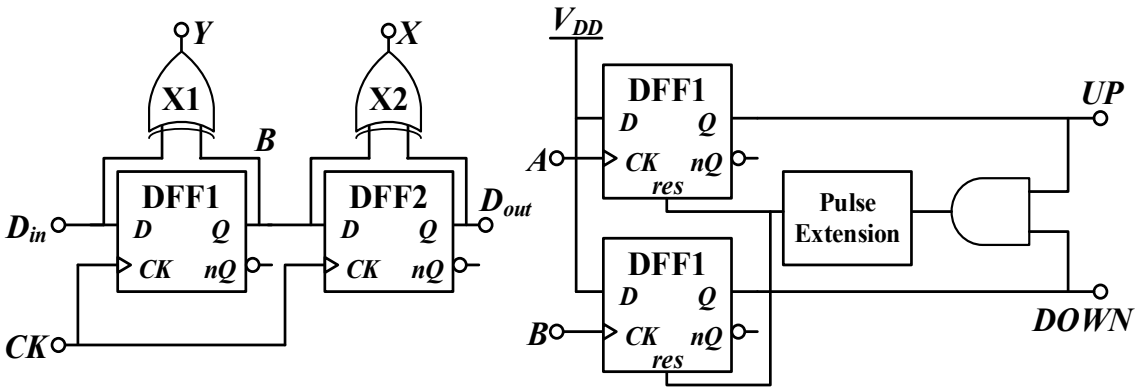


(a) (b)

Figure 4.16 Waveform generated from a simple PD and the Hogge PD.

However, the simple PD shown in Figure 4.15 fails to produce a unique average DC output when the data rate of the random data falls by a factor of two as the pulse width generated by the phase detector rises by a factor of two accordingly. For example; the averaged output *Y* (highlighted in grey colour), generated from the simple PD when the data rate of the random data is faster by a factor of two shown in Figure 4.16(a), is identical to the average output *Y* of the waveform shown in Figure 4.16(b). To produce a unique average output signal *X*, the secondary DFF and XOR gate are cascaded, forming a Hogge PD circuit [20, 58] shown in Figure 4.17(a), to produce a reference pulse clock with the period of $T_{CK}/2$ when T_{CK} is the period of the clock signal *CK*. It can be seen that the average voltage of the signal *X* (highlighted in grey colour) shown in Figure 4.16(a) is different from the average voltage of *X* shown in Figure 4.16(b). The output *X* and *Y* produced by the Hogge PD are consequently subtracted and averaged to control the output frequency of the VCO.

Figure 4.17(b) shows the conventional PFD [20, 59]. The circuit is implemented from two DFF circuits and a NAND gate for resetting the flip-flop. The DFF used in this design required 1ns minimum pulse width as the reset signal, and thus a pulse extension circuit employing a chain of inverters and an OR gate is used for the reset. In addition, the logic circuit cells are obtained from the library provided by the manufacturer [46]. The layout of each logic gate can be cascaded at the adjacent side of the cell since the height of each cell from the library is identical.



(a) Hogge PD (b) PFD

Figure 4.17 Schematic view of the phase detector.

4.3.2.2 PLL Charge pump

The conventional PLL charge pump circuit is susceptible to transient noise due to the charge injection of the MOS switches M_{p1} and M_{n1} [59], therefore a current steering switch and an op-amp used as a voltage follower are utilised as illustrated in Figure 4.18 [60]. The circuit consists of a single-stage op-amp, a PLL charge pump with current steering switch and four multiplexers. The multiplexers are used for selecting two different signals provided by the PFD and the Hogge PD depending on the different operating modes.

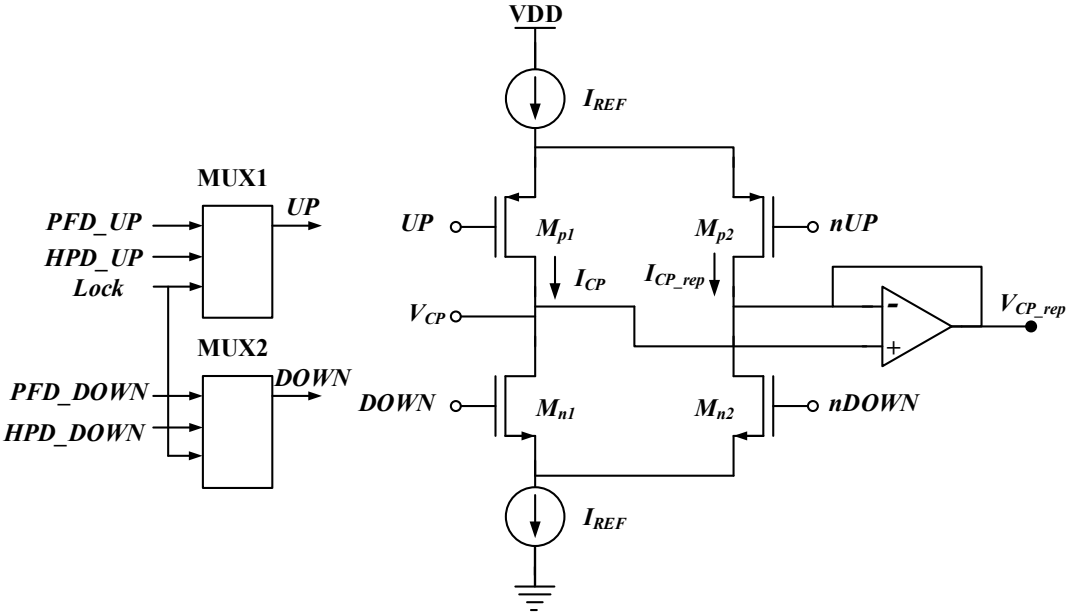


Figure 4.18 Schematic view of the PLL charge pump.

The PLL charge pump is simulated by applying the *UP* and *DOWN* signal (*Y* and *X* signal from Hogge PD) when the voltage supply is 600mV, as can be seen in Figure 4.19. The *integ_icp* shown in the figure (the bottom trace) is the integrated signal of the output PLL charge pump current; the nice shape of triangle implies that the transient noise from the charge-injection at the output current is relatively low.

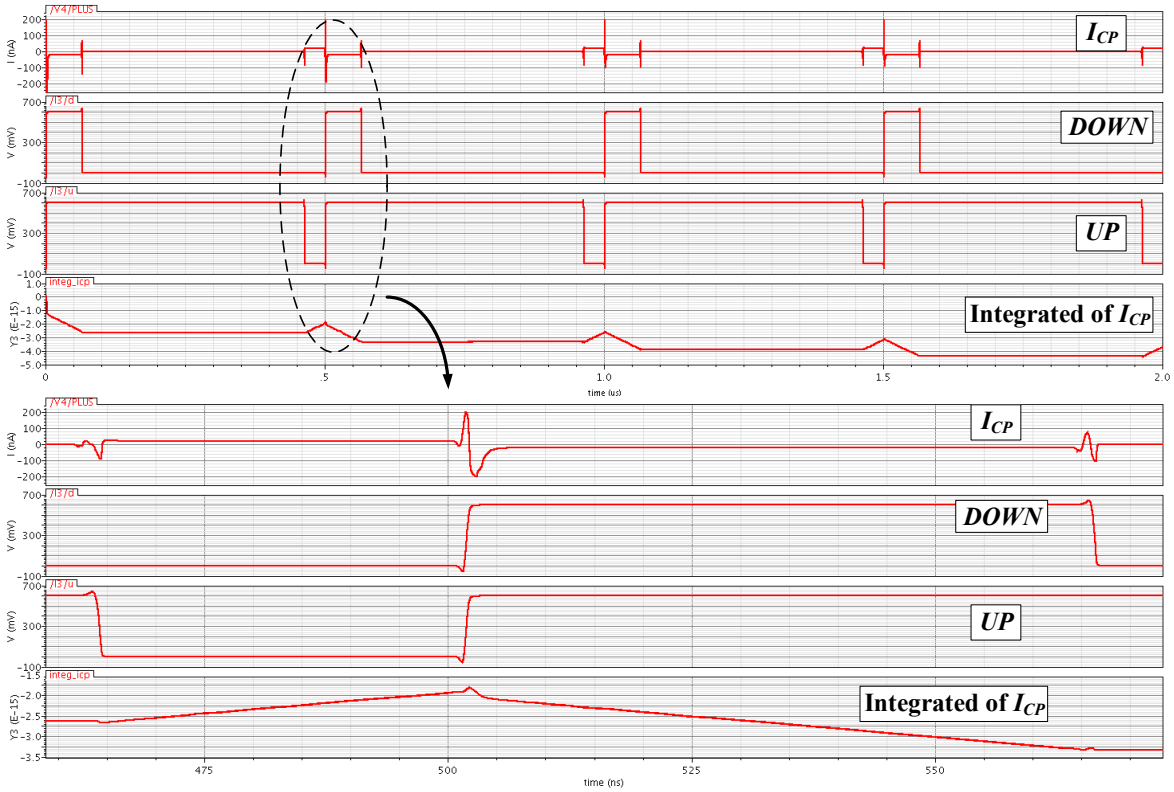


Figure 4.19 Transient response of the PLL charge pump when the supply voltage is 600mV.

4.3.2.3 Voltage-controlled Oscillator and Frequency Divider

The VCO is implemented from the conventional current-starved ring oscillator [61], as illustrated in Figure 4.20. The current-starved configuration is selected in order to acquire a full output voltage swing at all tuning values. In addition, one of the inverters is replaced with a NAND gate in order to enable the sleep mode of the oscillator. Moreover, a simple NMOS (M_n) is utilised for the voltage to current (V-to-I) conversion. In order to improve the linearity of the voltage to current converter, a series resistor (R_S) is connected to the source of M_n to ground which results in a source degeneration configuration [57]. Note that an NMOS switch (SW1) is added to disable the continuous current of the V-to-I converter when the VCO is deactivated. The VCO is designed to generate a clock signal where the frequency range is between 2MHz and 8 MHz since the frequency is divided by four before being compared with the input RF signal. As the VCO generates a high-frequency signal, parasitic capacitors may significantly affect the output frequency of the circuit. Thus, the placement of the chain of inverters in the layout should be very compact.

The post-layout simulation of the VCO is tested by ramping the input voltage of the VCO from the supply (V_{DD}) to ground to control the output frequency. At the nominal condition with the supply voltage of 600mV, the VCO output frequency range is between 100kHz and 14MHz. Moreover, the VCO gain (K_{VCO}) measured from the transient response is 33.5MHz/V, which will be used for designing a PLL system. Furthermore, the simulation of the circuit across the PVT corners with the different power supply has been tested. The maximum frequency of the VCO under the worst-case

condition, with the power supply below 500mV, might not be sufficient for the requirement of the demodulator system. Hence the design of the voltage reference and the voltage regulator that provide the supply voltage, which is above 500mV across the PVT corners, for the demodulator is essential. The simulation results of the VCO are shown in Appendix E.2.

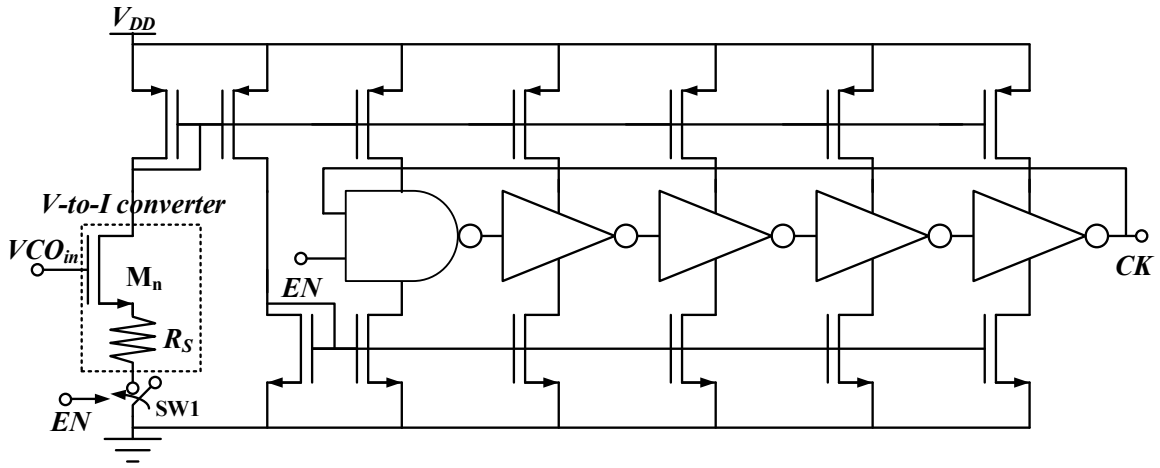


Figure 4.20 Schematic view of the VCO.

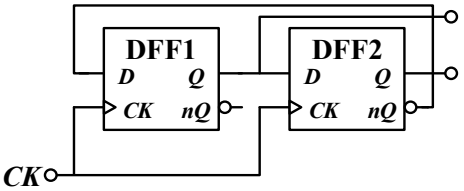


Figure 4.21 Schematic view of the frequency divider.

In addition, a divide by four [59] implemented from two DFF circuits is used as a frequency divider, as depicted in Figure 4.21. The circuit is chosen because it can generate the quadrature outputs (*I* and *Q*) which are required to extract the data using the data detection circuit.

4.3.2.4 Lock Detection

The locked condition detection, implemented from the logic circuit cells from the manufacturer's library, is designed for detecting the locking of the frequency in the proposed QPSK demodulator. When the reference frequency is close to the input frequency then the locked detection sends a signal to switch the phase detection of the demodulator system. Figure 4.22 illustrates the schematic diagram of the proposed locked condition detection. The circuit consists of the N-bit counter and logic circuits, and is developed from [62]. The N-bit counter is used to count the rising edge of input pulses. After 2^N pulses are counted, an overflow output (C_{out}) is toggled in the next rising edge and the N-bit parallel outputs (B_1 to B_N) are reset to zero.

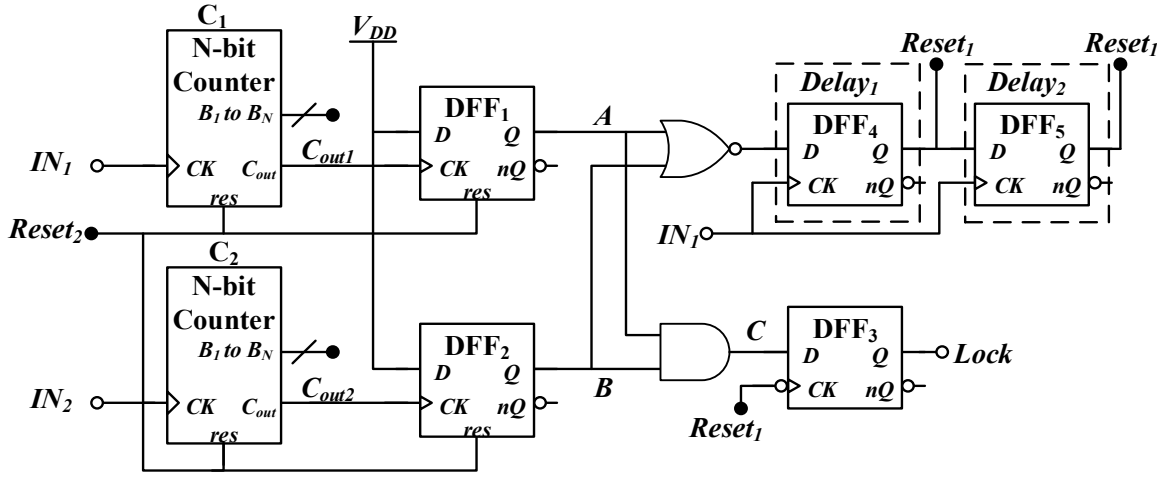


Figure 4.22 Schematic view of the proposed locked detection.

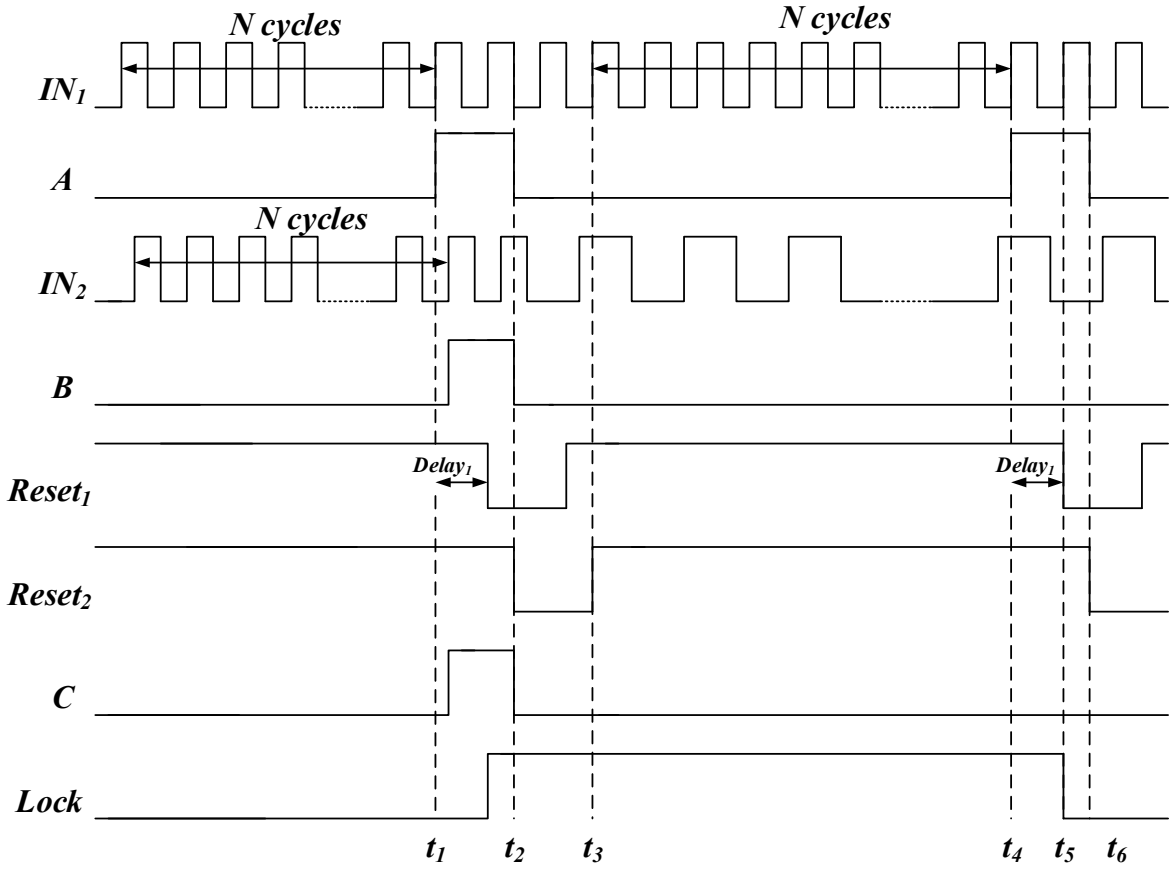


Figure 4.23 Waveform of the locked detection circuit.

Figure 4.23 illustrates a waveform example of the lock detection. Initially, the two input signals with the same frequency are applied to the circuit. At t_1, the counter C_1 finishes the counting and the overflow output C_{out1} from C_1 is high. The D-flip-flop DFF_1 holds the output until it is reset. Before the signal from the first counter is reset, however, the counter C_2 finishes the counting. Sequentially, the output from the logic AND between two counters is high. In consequence, the reset signal $Reset_1$ toggles at the clock input of DFF_2 and the output *Lock* is high. It can be seen that when one of the counters finishes counting, the system waits for another counter for a period of $Delay_1$. When both counters finish counting on time within the delay interval, the output locked

signal then is high, as can be seen in Figure 4.23 at the time between t_1 and t_2. At t_3, the reset signal $Reset_2$ rises and the counters start to count. On the other hand, if the second counter does not finish on time between t_4 and t_5 then the output *Lock* is low. Note that DFF is used to create the delay period of the signal and the FF is toggled by the incoming signal IN_1. In practice, the VCO frequency is likely to start from a low value, hence the incoming frequency is more suitable for toggling the DFF of the delay cells for a shorter and more reliable delay time.

4.3.2.5 Data detection

Figure 4.24 shows the schematic view of the data detection, the circuit is designed to extract the data signal from the QPSK demodulator. The circuit consists of an XOR gate, two DFF circuits and two tri-state buffer logic gates. When the locked detection senses that the frequency is locked, the lock detection enables the tri-state buffer output of the data detection. The QPSK data is extracted by comparing the reference signals *I* and *Q* with the incoming QPSK signal D_{in} using the DFFs.

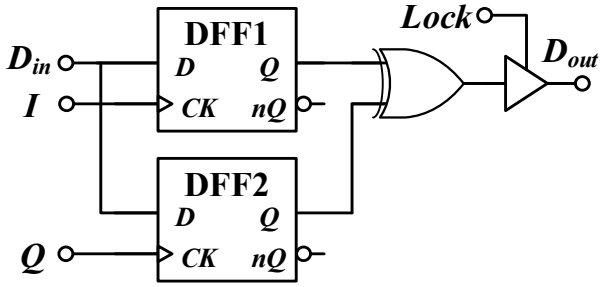


Figure 4.24 Schematic view of the data detection.

The data detection is tested by applying a QPSK modulated signal with the carrier frequency of 1MHz and a reference signal when the supply voltage is 600mV, as shown in Figure 4.25. It can be seen that the data detection can extract the data from the modulated signal. It is important to note that the output data result is the anti-phase of the input data. This is expected for the PSK demodulation system since the system cannot distinguish the recent phase of the signal, whether it is 0-degree or 90-degree before the phase-change. The PSK demodulator can only detect how much the phase is shifted from the previous state (i.e., 90-degree phase lag compared with the previous state). Therefore, a communication protocol is needed for the receiver to identify the correct signal. For example, in two clock cycles if the input data is toggled from high to low or from low to high then the data can be read as “0”, while the data is read as “1” when the input data remains unchanged in two clock cycles; this technique is known as the differential phase shift keying (DPSK) [59].

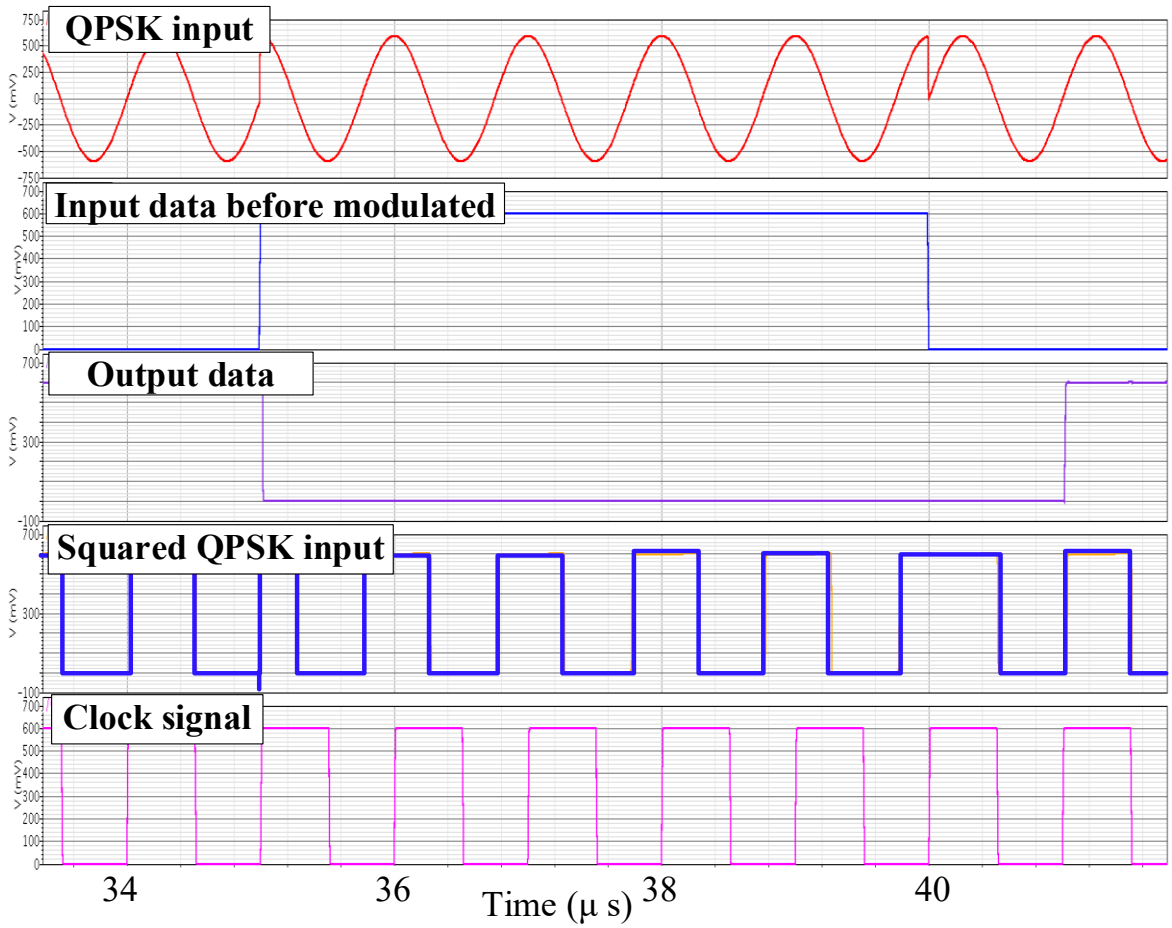


Figure 4.25 Transient response of the data detection when the supply voltage is 600 mV and the frequency of the carrier is 1MHz.

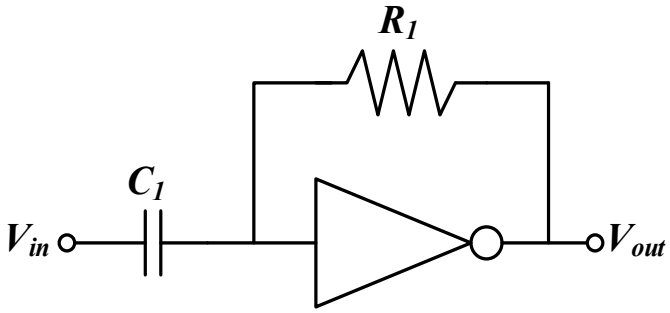


Figure 4.26 Schematic view of the inverting amplifier.

4.3.2.6 Amplifier

Since the incoming signal from the receiving antenna can be as low as 250mV$_{pk}$, the signal may not be sufficiently large to trigger a digital logic gate. Thus, an amplifier is needed to square the input signal. An amplifier is implemented from an inverter biased with a large resistor, as can be seen in Figure 4.26. In addition, a voltage gain of approximately 7.6dB is required, as the minimum incoming signal for the specifications is 250mV$_{pk}$ while the supply voltage and hence logic swing of the logic gates is 600mV. Note that an inverter logic gate used in this project requires at least 380mV to fully trigger the output logic when V_{DD} is 600mV. A 5pF capacitance of the coupling capacitor C_1 is chosen to couple the input signal while an approximately 1MΩ is chosen for the large resistor. The coupling

capacitor for the amplifier is not as large as the coupling capacitor (100pF) used for the rectifier circuit since the input impedance of the amplifier is much higher compared to the rectifier input impedance. The frequency response and the transient response of the amplifier across the PVT have been tested and can be found in Appendix 0.

In this design, we have not discussed the noise, which is an important aspect to consider before designing an amplifier and a data demodulator. However, the amplifier input signal-to-noise ratio (SNR) of the system is very large since the required minimum input voltage (or receiver start-up voltage) is at 250mV. By using the amplifier resistor to calculate the thermal noise at room temperature [57], the SNR of the system is 63dB. Based on the calculated SNR, the calculated bit-error-rate (BER) for the QPSK demodulation can be less than 10^{-8} [59].

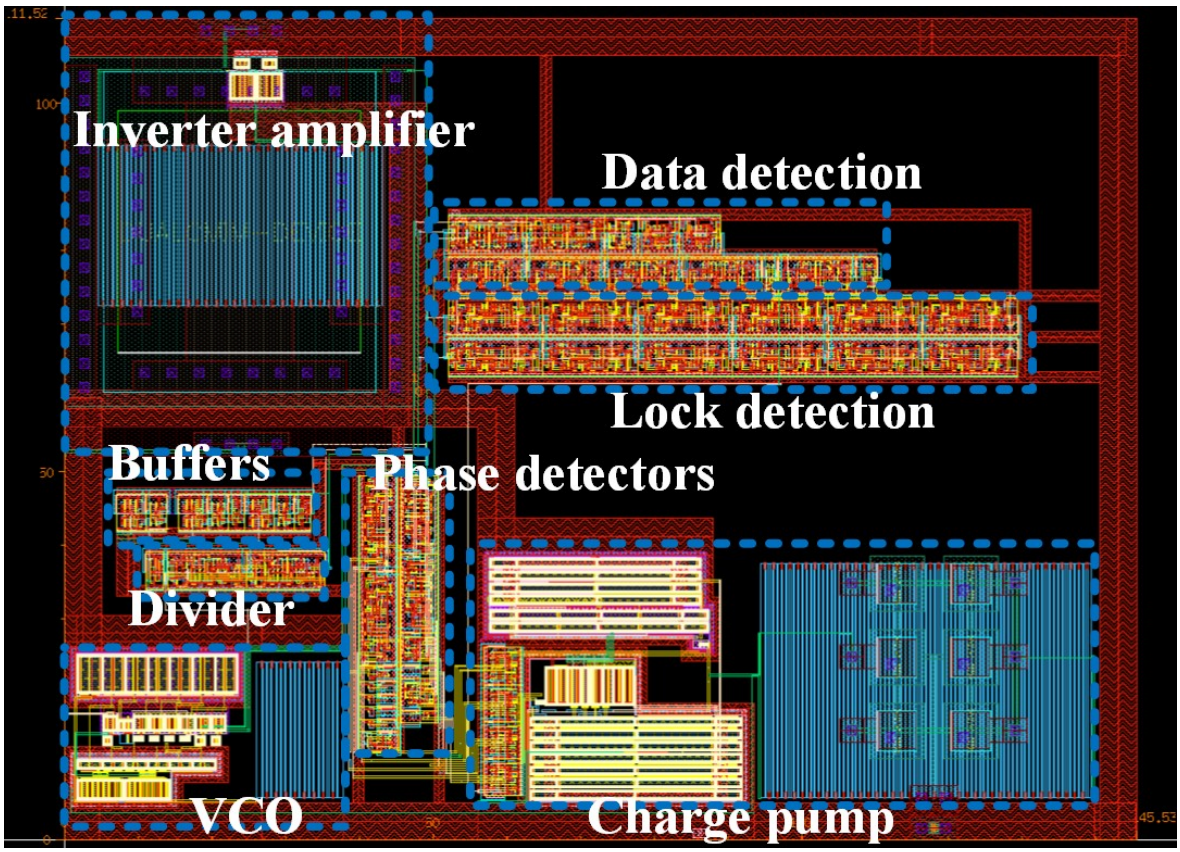


Figure 4.27 Layout view of the QPSK data demodulator. The size of the layout is 112x46µm^2.

4.3.2.7 Top-level Simulation

After the circuit design of each cell of the data demodulator has been completed, the layout of each cell is integrated, as depicted in Figure 4.27. The total area of the layout is 112x146µm^2. The system is simulated by applying a QPSK modulated signal with the carrier frequency of 1 MHz while the input data rate is 100kbps. The power supply of the system is provided by an ideal voltage source ramped from 0V to 600mV, thus the VCO frequency is started from zero. Note that the VCO frequency, in practice, is started from a low value since the system supply voltage is also ramped up from zero to V_{DD} same as the simulation setup. Moreover, the supply voltage used for the data

demodulator has to be as low as possible to minimise the average power consumption of the system, but also sufficiently large for internal circuits to operate properly (e.g., VCO). Hence, the 600mV supply voltage is chosen for the data demodulator circuits. The average power consumption of each block of the data demodulator tested separately is summarised in Appendix E.9.

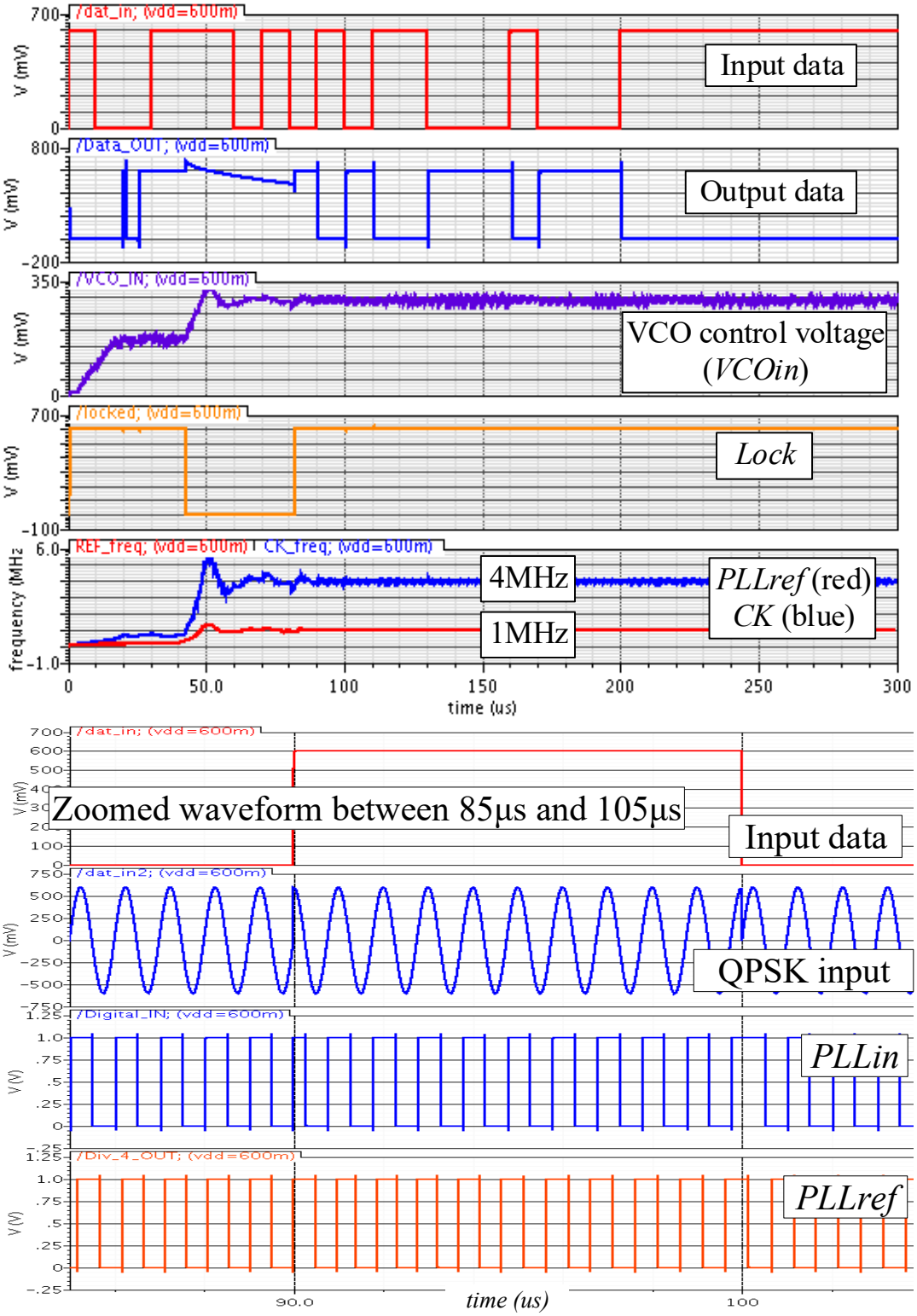


Figure 4.28 Transient response of the QPSK data demodulator when the power supply is ramped from 0V to 600mV and the input signal is an ideal QPSK modulated signal with the frequency of 1MHz frequency and the data rate of 100kbps.

Figure 4.28 presents the simulated time domain start-up response of the proposed QPSK demodulator. It can be seen that initially the signal *Lock* is high, hence the system fails to lock during the period between 0 to 50µs. This is expected, since the VCO frequency is started from cold while the incoming frequency is at 1MHz. After the lock detection circuit detects that the frequencies of the signals are different, the signal *Lock* is low. Consequently, the PLL is configured to use the PFD until the system is properly locked at the approximate time of 80µs, as can be seen from the output signal *Lock*. After the system is locked to the incoming data rate, the demodulator is reconfigured so that the Hogge PD is in the control loop circuit, and the system can successfully demodulate the data signal from the QPSK modulated signal. Although the phase of the output is inverted compared to the input data, a finite-state machine or microprocessor can be used to manipulate the output data later, as described in section 4.3.2.5. In addition, Figure 4.28 also depicts the zoomed waveform of the clock and the input signal amplified by the inverting amplifier. It can be seen that the clock signal is correctly recovered by the demodulator. Moreover, the average power consumption of the data demodulator from the transient response is 690.8nW. It is important to note that although the system can extract 100kbps data from an ideal QPSK signal, the data rate can be as low as 1kbps in practice due to the high Q-factor bandwidth limiting behaviour of the LC-antenna.

In addition, Figure 4.29 displays the transient response of the demodulator when the input is generated from an ideal 180-degree BPSK modulated signal with the 1MHz frequency and 100kbps data rate. It can be seen that the system can also extract the data from the 180-degree BPSK. Note that the test circuit for this simulation does not include the effect of the high-Q LC-antenna circuit.

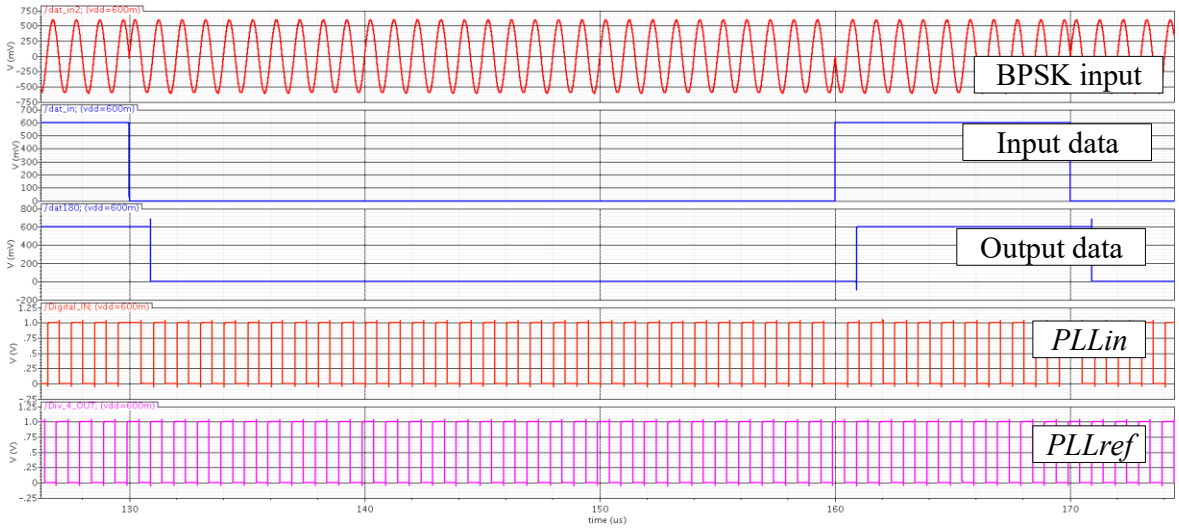


Figure 4.29 Transient response of the PSK data demodulator when the power supply is ramped from 0V to 600mV and the input signal is an ideal 180-degree BPSK modulated signal with the frequency of 1MHz frequency and the data rate of 100kbps.

4.3.3 Power Management

Figure 4.30 presents the system architecture of the PMU for the inductive coupled wireless energy harvesting receiver. The system is comprised of a voltage reference, a voltage regulator, a voltage level detector, a DC-DC voltage converter, the low and high voltage limiter circuits and two off-chip capacitors. The system is designed to produce clean DC voltage sources for internal circuits, including the data demodulator, and external modules.

The output DC voltage from the input switch-over cold-start subthreshold voltage rectifier V_{rect}, in a range of 0.9V to 1.8V, is stored in an off-chip capacitor C_1 to supply the voltage reference, the regulator, the level detector and the QPSK data demodulator. The low voltage limiter ensures that the rectifier output voltage is always below 1.8V for circuit protection. The voltage regulator incorporated with the voltage reference regulates the fluctuating V_{rect} to a stable 600mV DC voltage V_{DD}, then the local supply V_{DD} is provided to the QPSK data demodulator. Since the DC voltage V_{rect} is not sufficient for the off-chip external modules, a DC-DC charge pump (CP) boosts the low voltage V_{rect} to a 3V DC output V_{CP} which is stored on an off-chip capacitor C_2 (or a lithium-ion battery depending on the application system requirements). The clock signal for clocking the CP is generated from the PLL of the data demodulator, which is able to begin running with a very low supply during start-up. Furthermore, the high voltage limiter is used to protect the CP from voltage breakdown while the input signal received from the antenna V_{RX} is limited by the low voltage limiter similarly to the voltage limiter used for limiting the supply voltage V_{rect}. In addition, the level detector controls the active timing of the data demodulator and the CP as described in section 4.1.

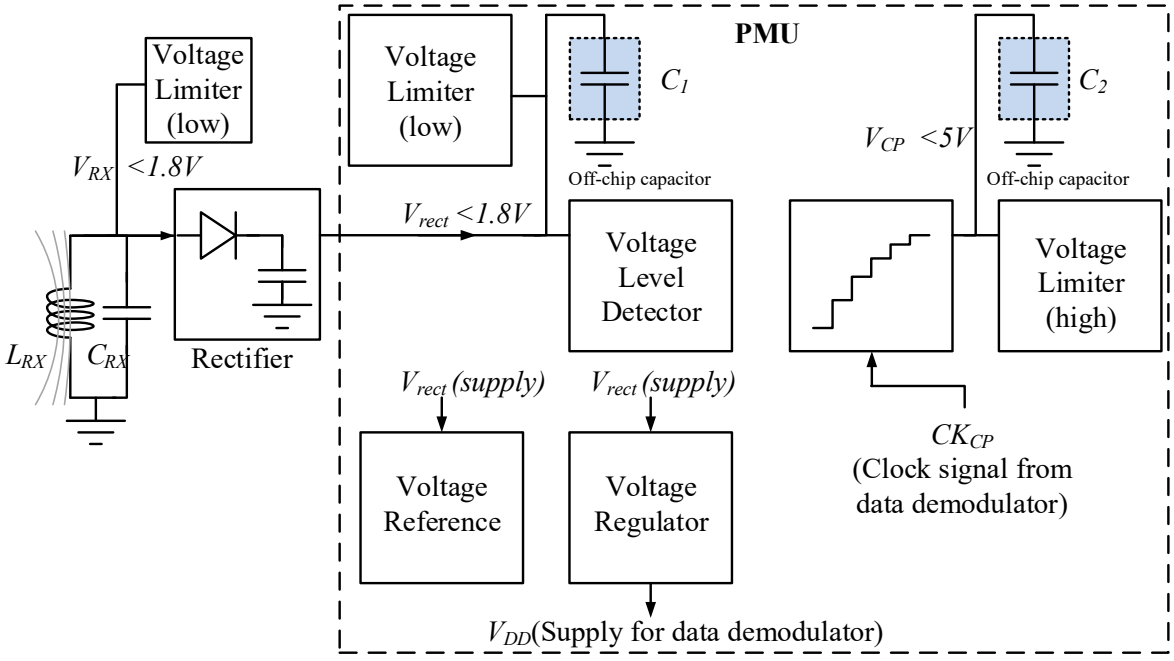


Figure 4.30 System architecture of the power management unit.

4.3.3.1 Voltage Level Detection

Figure 4.31 illustrates the schematic view of the voltage level detection function. The circuit consists of two (different) voltage level detectors V_{low} and V_{high} and logic gates for hysteresis level detection. The circuit is implemented using two identical transistors that are drained by two different values of current (I_{REF1} and I_{REF2}) and are applied by a reference voltage (V_{REF}) at the MOS gate [12]. Considering the PMOS M_{P1}, if the input supply voltage (V_{IN}) exceeds the threshold or $|V_{GS1}| = |V_{IN} - V_{REF}| \geq |V_{thp}|$, then the drain voltage (V_D) of M_{P1} is pulled down to $V_D = V_{IN} - V_{DS}$ where V_{DS} is the drain-to-source voltage of the transistor. The drain voltage V_D can be used to toggle the logic gate when the voltage level exceeds the logic threshold level. Note that the logic threshold level is varied across PVT of the transistor, however this circuit consumes less power than the circuit using an op-amp to compare the input voltage with the reference voltage, which is essential for ultra-low power circuits. In addition, the *nref_ready* signal is generated from the voltage reference circuit when the voltage reference level is ready to enable the voltage level detection circuit using an OR gate. Moreover, the logic circuits are connected to the current source I_{REF3} in order to limit the short circuit current during the output transition, similar to the comparator of the rectifier switch-over detection circuit shown in section 4.3.1.2.

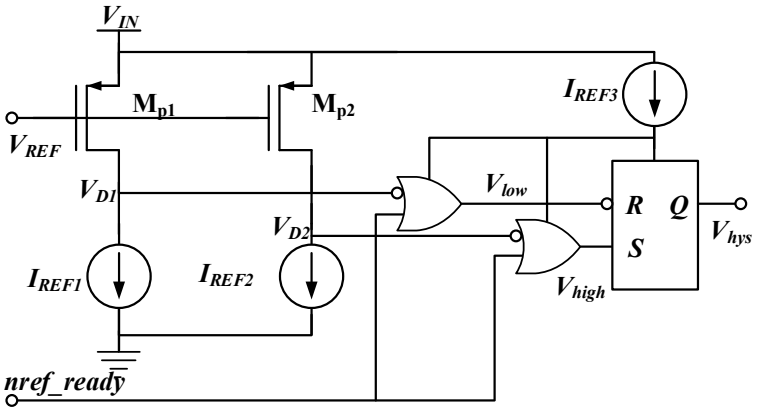


Figure 4.31 Schematic view of the voltage level detection.

Due to the requirement of a hysteresis voltage detection to be able to tolerate a noisy supply signal from the rectifier output (V_{RECT}), a secondary voltage level detector is added by using PMOS M_{p2} and the current source I_{REF2}. As the MOS drain current (I_D) is proportional to V_{DS} when the transistor is operating in the saturation region (and I_D is also roughly proportional to V_{DS} in linear region) [56], two voltage level detection circuits with different voltage levels are created. In addition, the current sources (I_{REF1}, I_{REF2} and I_{REF3}) are implemented from a conventional current mirror circuit where the reference current is generated by the reference circuit which will be shown later.

The hysteresis level detection is tested in both DC and transient simulations; the low voltage level detection V_{low} is 730mV and the high voltage level detection V_{high} is 905mV for nominal PVT. Moreover, the current consumption of the circuit with 1V supply voltage is 120nA. The transient

response verifies that the current spike drained from the level detection circuit which occurred during the output transition is limited to 266nA. The DC, transient and corner tests are shown in Appendix E.4.

4.3.3.2 Voltage Reference

The voltage reference is implemented from the supply independent current reference circuit [56, 57] as shown in Figure 4.32. The circuit is comprised of a reference generator, a start-up circuit and the current mirror that provides the current reference for the analogue building blocks. As the circuit is operating in the subthreshold (weak-inversion) region where the MOS drain current is chosen to be less than 100nA, the expression of the current reference operating in the subthreshold region of the circuit is

$$I_{REF} = \frac{1}{R_1} m V_T \ln\left(\frac{(W/L)_{n2}}{(W/L)_{n1}}\right), \qquad (4.2)$$

where $(W/L)_{n1}$ is the dimension ratio of the transistor M_{n1}, m is the subthreshold slope parameter, and $V_T = k_B T/q$ is the thermal voltage (k_B is the Boltzmann constant, q is the elementary charge and T is the absolute temperature). It can be observed that the reference current is dependent on the resistance R_1, where the resistance of an on-chip resistor is varied across the PVT corners. However, this circuit is chosen because it consumes lower supply current compared with the bandgap reference. The current consumption of the supply independent voltage-current reference can be as low as 10 to 100nA while the current consumption of the bandgap reference can be above 100µA. In addition, the supply independent reference voltage (V_{REF}) from V_{GS} of the MOS M_{n1} can be used as a reference voltage for other circuits in the PMU.

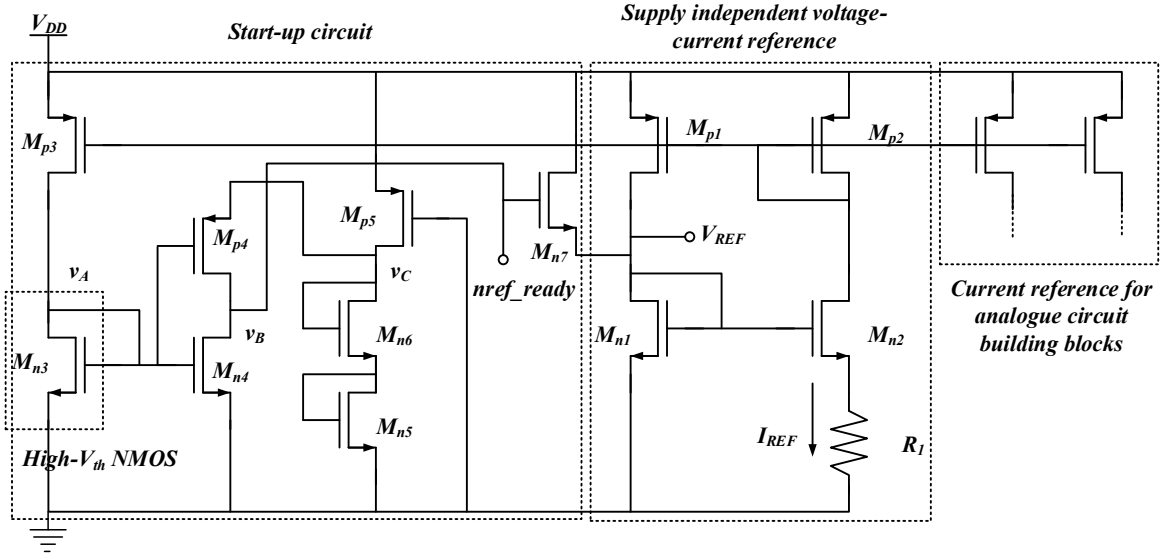


Figure 4.32 Schematic view of the voltage reference.

As there are two conditions that can potentially occur for the reference circuit which are (1) the reference current is conducting and (2) the reference current is zero, hence a start-up circuit is

employed to ensure that the circuit is properly functional. The start-up circuit used in this design is developed from the concept proposed by [63]. From Figure 4.32, the start-up circuit operates as follows. Initially, the reference current I_{REF} is zero, hence the voltage v_A at the gate of the transistor M_{n3} is zero. Consequently, the output voltage v_B of the inverter M_{n4} and M_{p4} is logic high and turns the NMOS switch M_{n7} to conduct. Therefore, the gate voltage of the transistor M_{n1} is pulled up to the power supply and the reference current is starting to conduct. As the current is conducting, the voltage at node v_A is approximately at the V_{th} of the NMOS M_{n3}. Sequentially, the output of the inverter M_{n4} and M_{p4} is logic low and the NMOS switch M_{n7} is turned off. Note that a high-V_{th} NMOS, which is available in the CMOS process used in this project, is selected for M_{n3} to guarantee that v_A is higher than the V_{th} of inverter M_{n4} when I_{REF} is conducting. Moreover, the local supply node of the inverter (v_C) is tied to the diode-connected transistors M_{n5} and M_{n6} and the PMOS resistor M_{p5} to limit the logic high output of the inverter to approximately twice the N-channel V_{th}. If the supply of the inverter is not limited, then the voltage v_A might not be sufficiently high for the inverter to switch to logic low. In consequence, the NMOS switch would always be conducting and the reference circuit would fail to operate properly.

The voltage reference is simulated to verify that the circuit can start up when the supply voltage is as low as 500mV by ramping up the supply voltage from 0V. The circuit generates a DC reference voltage and current approximately at 230mV and 22nA respectively. The voltage reference requires approximately 200µs for the reference signal to be ready for the nominal condition and 500µs for the worst-case PVT corners where the speed of the active devices is limited and the temperature is -20°C. Furthermore, the power supply rejection-ratio (PSRR) of the circuit is approximately at -30dB over the operating frequency region (500kHz – 2MHz). The simulation results can be found in Appendix E.5.

4.3.3.3 Voltage Regulator

Figure 4.33 shows the capacitor-less linear voltage regulator. The circuit consists of a single-stage operational amplifier, a PMOS pass transistor, two resistors for the negative feedback and a comparator. This work employs a simple Miller capacitor for compensation instead of the more sophisticated method that can be found in recent works, since the circuit provides low current consumption and simplicity of the design. As the system requires an ultra-low power circuit, sacrificing an area for a large compensated capacitor rather than a high-power consumption circuit is acceptable. The regulator is designed to provide a 600mV output for a local power supply.

The voltage regulator is tested to ensure that the circuit is stable under the worst-case light load condition [64, 65] where the loading current is 120nA. The minimum loading current is determined from the simulation of the current consumption caused by the data demodulator at sleep mode.

The phase margin of the circuit is approximately 67 degrees while the unity gain bandwidth (UGBW) is approximately 24kHz. In addition, the regulator generates 603mV DC output at the nominal condition. The total current consumption of the regulator at the light load condition is 431nA, thus the quiescent current of the circuit is 311nA. (Assuming the load current is 120nA.) The corner simulation of the voltage regulator confirms that the circuit is stable across the PVT as the phase margin is above 60 degrees while the output voltage varies between 500mV and 780mV, which is acceptable for the demodulator circuit (minimum V_{DD} must be larger than 500mV). The simulation results are shown in Appendix E.6.

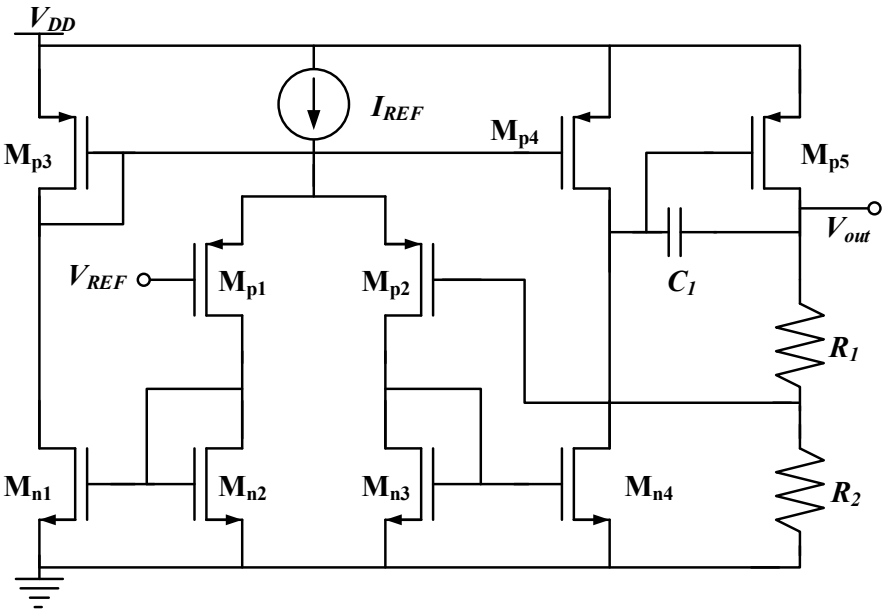


Figure 4.33 Schematic view of the voltage regulator.

4.3.3.4 DC-DC Charge Pumps

The DC-DC voltage converter is shown in Figure 4.34, the circuit consists of a three-stage latched CP [66]. It can be observed that the circuit configuration is similar to the differential drive rectifier mentioned in section 3.2.4, hence the operation of the circuit is similar. Since the CP clock is generated by the PLL which has the amplitude equal to the local supply voltage V_{DD} which is approximately 600mV, a level shifter is needed to shift the amplitude of the clock from 600mV to V_{rect} (rectifier output voltage). Moreover, the NMOS devices of the CP are implemented from the isolated P-well transistors available in this process in order to reduce the body effect. Consequently, the die area of the transistors is much larger than the normal NMOS transistor. Note that the output voltage of the rectifier shown in equation (3.6) can also be used to design the CP since the circuit is developed from the conventional voltage multiplier.

The circuit is tested with the output load of 5MΩ resistance and 500pF capacitance when the supply voltage is 0.9V. The load of 5MΩ is chosen in order to demonstrate that the CP can provide sufficient power to the external modules when they are in idle mode. In active mode, a large current is likely

to be consumed by the external modules in the sensor system which will result in the decrease of the output voltage of the CP. Hence, a large capacitor of, for example, 40µF is selected, as explained in section 4.2. As a result, the output voltage produced by the CP is approximately 3.2V. The corner simulation result of the CP, when the input voltage and the clock signal are generated from an ideal source, is shown in Appendix E.7.

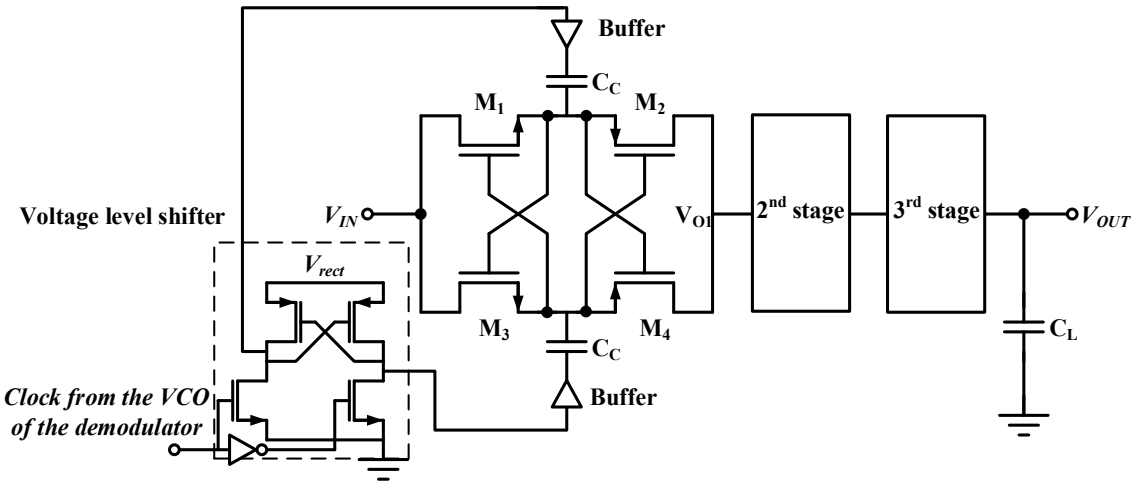


Figure 4.34 Schematic view of the CP.

4.3.3.5 Voltage Limiter

The voltage limiter is used to protect the internal circuits from the breakdown voltage of the 0.18µm CMOS process used in this project. The breakdown voltage of the low voltage CMOS devices is 2V, while the breakdown voltage of the high voltage CMOS devices is 5V [46]. For this design, the incoming signal from the receiving antenna can exceed these voltage ratings. Moreover, the simulation result of the rectifier plotted in Figure 4.12 indicates that the output voltage V_{rect} can rise above the breakdown voltage if the input voltage of the rectifier is greater than $500mV_{pk}$. Hence the voltage limiter is designed to prevent the circuit break down. Similarly, the output voltage of the CP can potentially exceed 5V, and thus the high voltage limiter is needed.

Figure 4.35 illustrates the schematic view of the limiter. Three diode-connected PMOS transistors in series connection are used to detect the input voltage. When the input voltage is higher than approximately three times of the V_{thp} then the parallel PMOS M_{p4} used as a parallel variable resistor starts to conduct. As the input voltage increases, the parallel resistance of M_{p4} decreases. In consequence, the loading current (I_L) of the rectifier or the CP is significantly increased which results in limiting the output voltage of the circuit, as shown in equation (3.6).

The voltage limiter is tested by applying a DC current source in parallel with a 100kΩ resistor. For the low voltage limiter, the input voltage is limited to approximately 1.6V. When the input voltage exceeds 1.6V, then the current conducted through the limiter starts to increase. In addition, the current consumption of the limiter when the input voltage is at 1 V is 38.9nA as can be seen in

Figure 4.35. The measured equivalent resistance of the limiter circuit from the simulation results is less than 4kΩ. On the other hand, the limited voltage of the high voltage limiter is approximately 4.5V. The DC simulation results of the circuits across the PVT are shown in Appendix E.8.

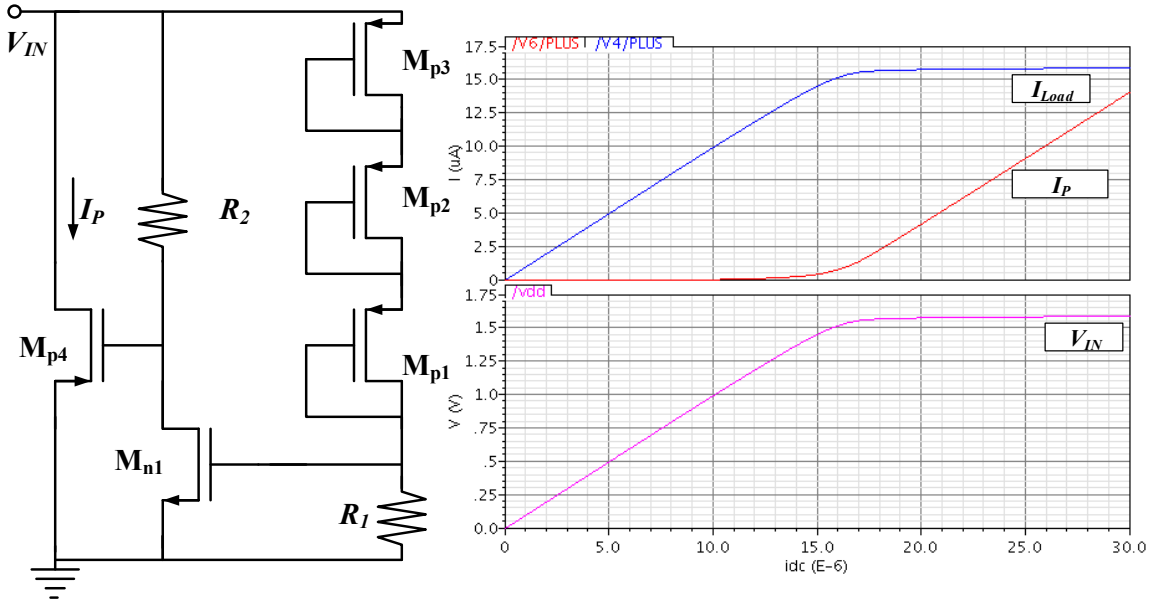


Figure 4.35 Schematic view of the voltage limiter (left) and the simulation results of the low voltage limiter when I_{Load} is the current of the parallel loading resistor.

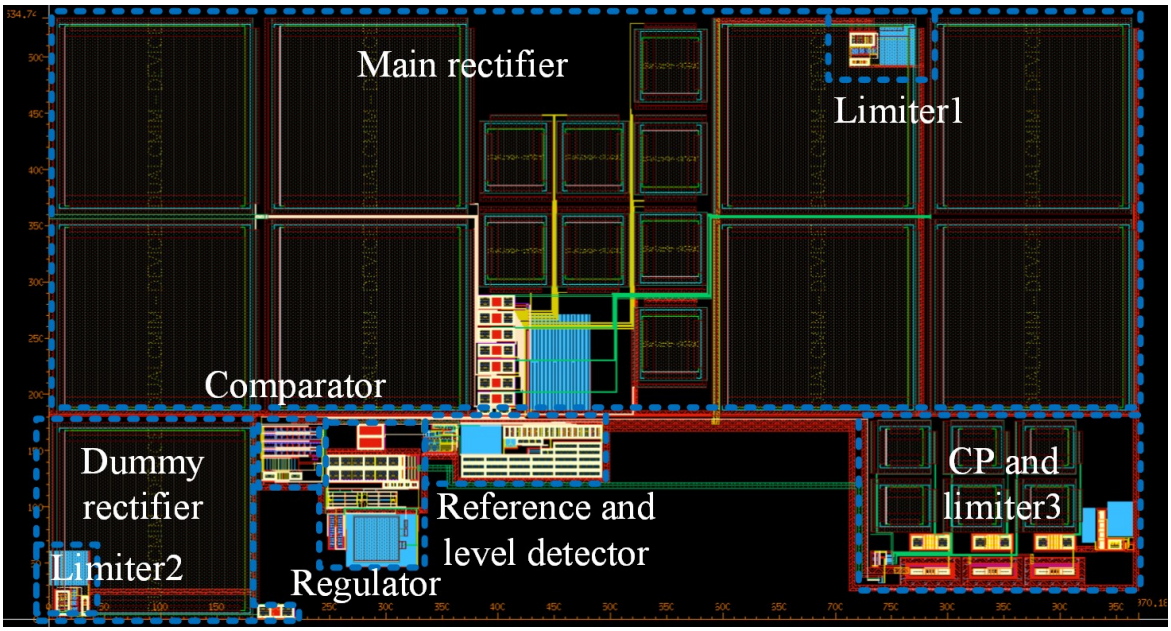


Figure 4.36 Layout view of the rectifier and the power management unit. The size of the layout is 535x970μm^2.

4.3.3.6 Top-level Simulation

The rectifier top-level and the PMU are integrated for the top-level simulation. Figure 4.36 presents the layout of the system where the total area is 535x970μm^2. It can be observed that the layout size of the main rectifier dominates the total area due to the 100pF coupling capacitors (C_C) used in

the rectifier circuit. Moreover, the CP is placed far from other analogue circuits to avoid interference from the noise clock switching of the CP.

As the analogue circuits require moderate accuracy, layout matching techniques are used in circuits that utilise a pair of transistors (e.g., a current mirror) where the transistors are split into a number of fingers for a stack arrangement in order to mitigate the matching effects of the transistor [57, 67]. For instance, the NMOS pair M_{n1} and M_{n2} is arranged as ABBA when A and B represent the fingers of M_{n1} and M_{n2} respectively. Furthermore, several dummy transistors are placed adjacent to both ends of the stacked transistors to improve the process variations. The average power consumption of each block of the PMU simulated separately is summarised in Appendix E.9.

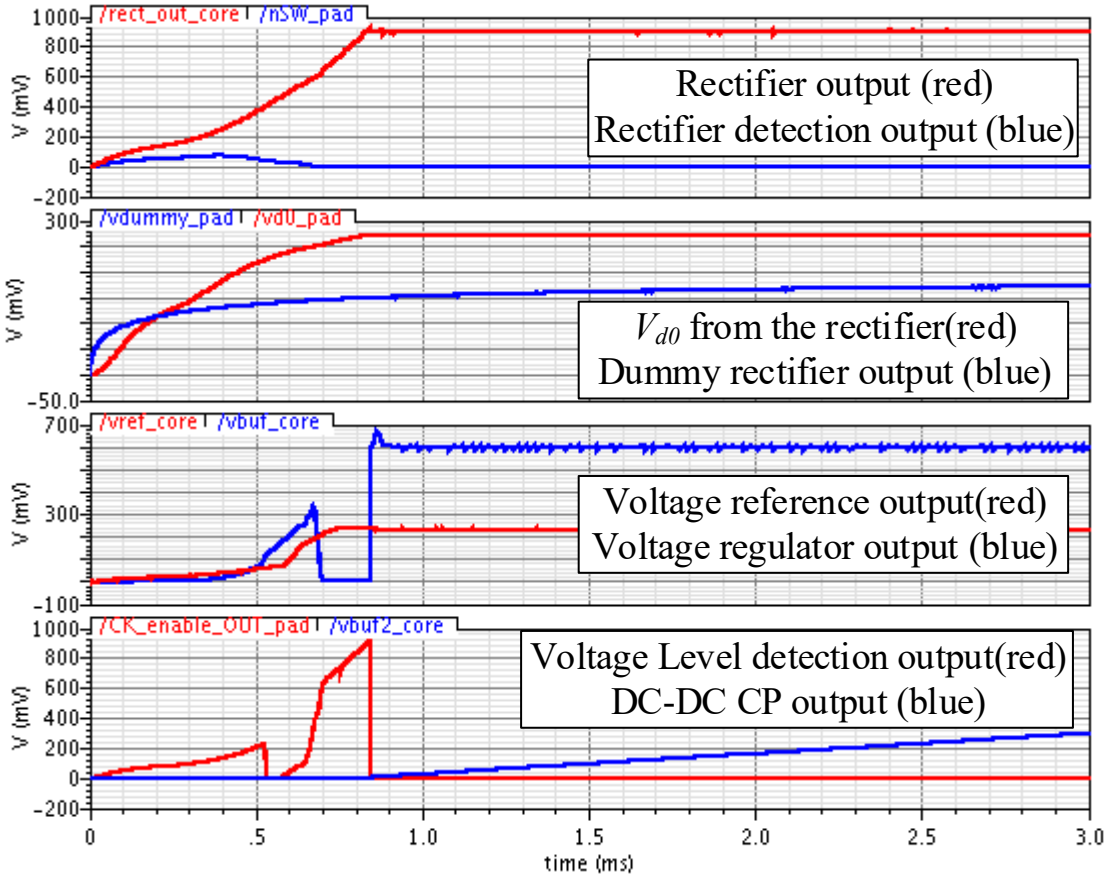


Figure 4.37 Transient response of the PMU when the input is 250mV$_{pk}$ with 1MHz frequency.

Figure 4.37 presents the simulation results of the system when the input is 250mV$_{pk}$ with 1MHz frequency. In addition, the load of 300kΩ, which is equivalent to the loading current due to the QPSK data demodulator (in the nominal condition), is connected to the output node of the voltage regulator. Furthermore, two 1nF capacitors utilised as a storage capacitor are connected to the output node of the main rectifier and the output node of the CP. Note that larger capacitors are used in practice, however the capacitance is reduced to 1nF in this test for shorter simulation time. From Figure 4.37, it can be seen that the rectifier can convert the incoming 250mV$_{pk}$ AC voltage signal to a 900mV DC voltage which is sufficient for the system. In addition, the output of the

comparator is switched to ground when the voltage V_{d0} from the main rectifier is greater than the voltage V_{dummy} from the dummy rectifier at the time of approximately 100µs. Furthermore, the simulation shows that the reference voltage and the regulated voltage are approximately 230mV and 600mV respectively. However, it appears that the local supply voltage generated from the voltage regulator is not smooth because the rectified voltage is not steady due to the frequency carrier noise. Thus, a large capacitor is required at the output node of the rectifier in order to filter the high frequency components from the incoming signal. At 800µs, it can be seen that the output of the level detection is low which enables the DC-DC CP. In consequence, the clock signal generated from an ideal source is connected to the input of the DC-DC CP. Therefore, the output of the CP starts to increase.

4.4 IC Floor Plan

The pad ring is designed to connect the internal nodes of the system to the IC pins. The placement of the pins is arranged such that the unwanted coupling between the adjacent metal traces and the parasitic capacitance are minimised. In addition, the pad ring also provides the electrostatic discharge (ESD) protection to protect the internal circuits. The pin diagram of the receiver IC is illustrated in Figure 4.38, and the pin list of the IC and its functionality are shown in Appendix 0. Note that the IC prototype shown in this chapter was shared with another design (unrelated to this project), thus the pins shown in the figure are only on one side.

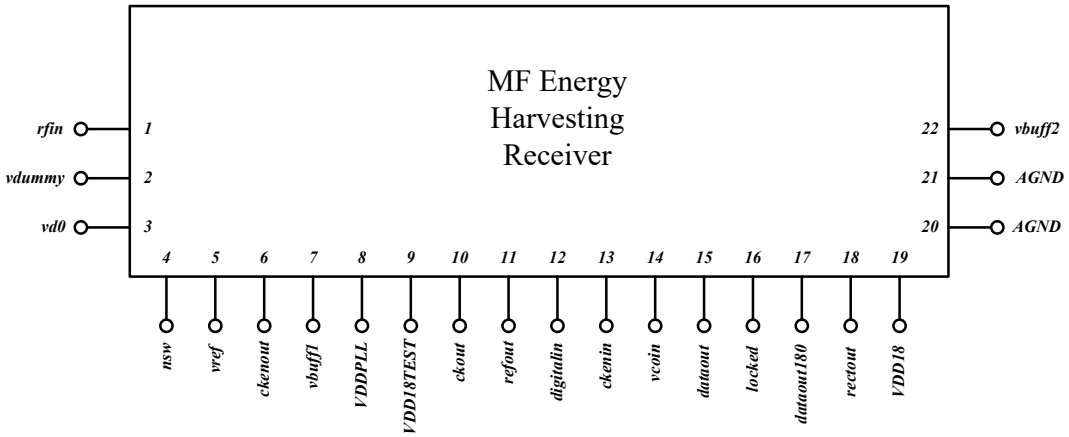


Figure 4.38 Pin diagram of the chip.

Figure 4.39 presents the full chip layout. The total area of the layout is 0.85x2.2mm^2. It can be seen that the gap between the internal circuits and the pad ring is filled with multiple metal traces to pass the minimum metal density design rule. Moreover, the schematic and post-layout extraction of each block have been verified over the PVT corners. The chip micrograph of the wireless energy harvesting receiver IC is shown in Figure 4.40.

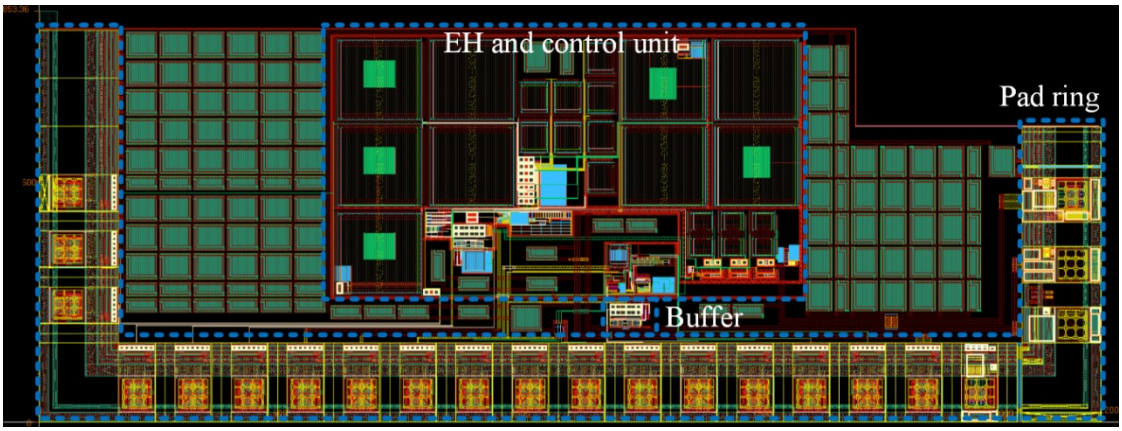


Figure 4.39 Full chip layout. The total layout size is 0.85x2.2mm^2.

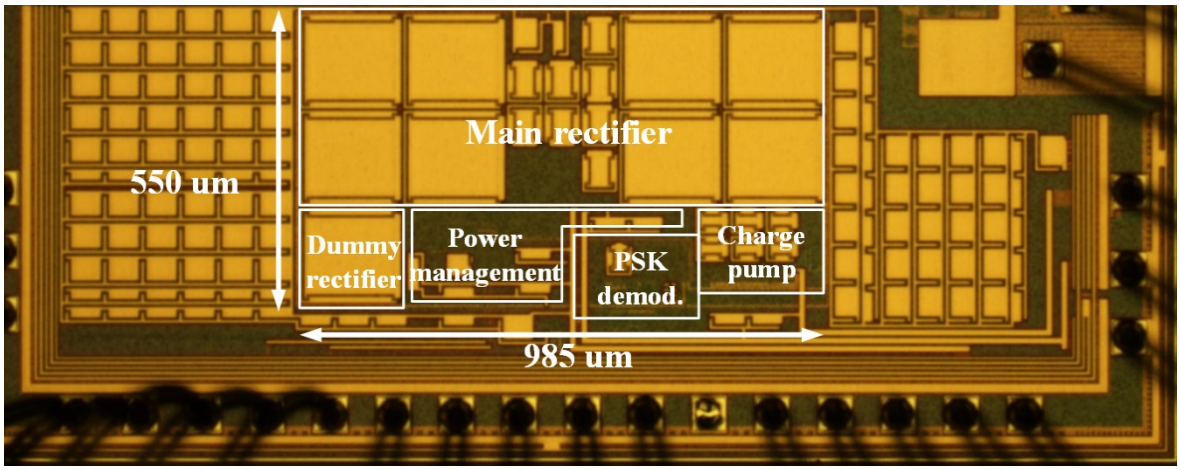


Figure 4.40 Wireless energy harvesting receiver IC micrograph.

4.5 Summary

The MF magnetic loosely coupled energy harvesting receiver prototype IC has been presented in this chapter. The receiver IC is designed to harvest the MF inductive coupled wireless energy to provide a stable supply source to a wireless sensor node. Moreover, the proposed ultra-low power PSK data demodulator of the IC is used to extract the timing information from the incoming signal in order to synchronise the system. The proposed switch-over cold-start subthreshold voltage rectifier is designed to convert an incoming AC signal that can be less than the MOS threshold voltage to a stable DC supply voltage. Furthermore, the switch-over detection circuit is used to improve the rectifier efficiency when the input amplitude is increased. With the ultra-low power designs of the PSK data demodulator and the power management unit, the average power consumption from the simulation results is below 10µW in the typical condition. The low power consumption of the receiver IC is achieved by using a near-threshold supply voltage at 600mV.

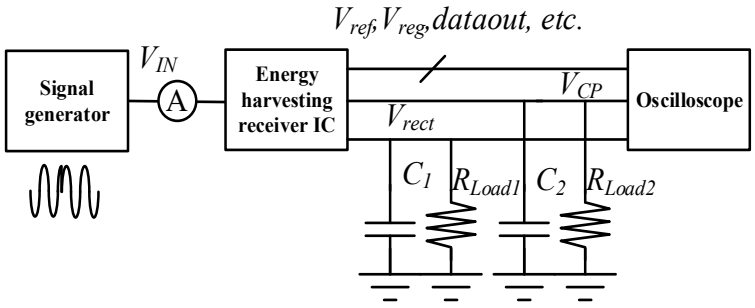
In the next chapter, the experimental result of the receiver prototype IC will be shown.

Chapter 5: WIRELESS ENERGY HARVESTING RECEIVER IC PROTOTYPE EXPERIMENT RESULTS

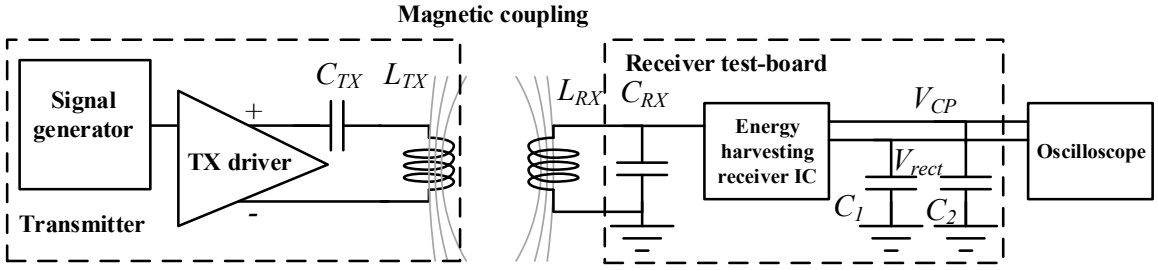
As the inductive loosely coupled wireless energy harvesting receiver IC has been implemented, the laboratory and field measurements of the fabricated IC are presented in this chapter.

5.1 Measurement Setup

Figure 5.1(a) presents the simplified diagram of the laboratory measurement setup of the magnetic loosely coupled wireless energy harvesting receiver IC. A function generator is used to generate the QPSK signal for the receiver IC input. Moreover, a small series resistor connected between the signal generator and the input of the IC is employed to measure the input current of the rectifier for calculating the rectifier power conversion efficiency (PCE). Note that the rectifier and the data demodulator of the chip share the same input pin, as shown in section 4.4. The output ports from the receiver chip are measured by an oscilloscope before analysing the data in MATLAB.



(a) Laboratory experiment setup



(b) Field experiment setup

Figure 5.1 Simplified diagram of the measurement setup of the magnetic loosely coupled wireless energy harvesting receiver IC.

For the field measurement setup shown in Figure 5.1(b), the QPSK signal generated by the signal generator is amplified by a transmitter driver to drive the large square/rectangular loop antenna. Note that the loading resistors (R_{Load1} and R_{Load2}) are not used in this setup, unlike the setup shown in Figure 5.1(a), since those resistors are only used to measure the efficiencies of the rectifier and

DC-DC CP. The transmitter antenna driver is implemented as an H-bridge class-D power amplifier [68] using S8050 for the NPN transistor and S8055 for the PNP transistor. Moreover the capacitor C_{TX} is included to form a resonant circuit at the primary coil to effectively increase the transmitting current. A ferrite rod antenna is used to receive the magnetic energy generated by the primary coil. Similarly, the capacitor C_{RX} is deliberately chosen to match the resonant frequency of the system to increase the received voltage signal. The parameters of the primary and secondary loop coils for the field experiment are listed in Table 5.1. Further, the oscilloscope is used to measure the output nodes of the receiver IC. The photo of the test-board of the wireless energy harvesting receiver IC is shown in Figure 5.2. Moreover, Figure 5.3 depicts the field experiments setup for the inductive wireless energy harvesting system measurement. The system is tested in an electrically quiet environment where in-band medium frequency (MF) interference is not present. Moreover, the 10x10m^2 square loop antenna is attached to the top of non-magnetic poles 2m above the ground level to avoid the loss from earth ground [24-26]. The 2m height of the poles for a large loop antenna is selected to coincide with the practical installation (i.e., fence posts), In addition, while the 10x10m^2 loop antenna is not the largest achievable area for this project, it is still a useful model with the available low power transmit driver, as the results can be scaled by improving the transmitter driver.

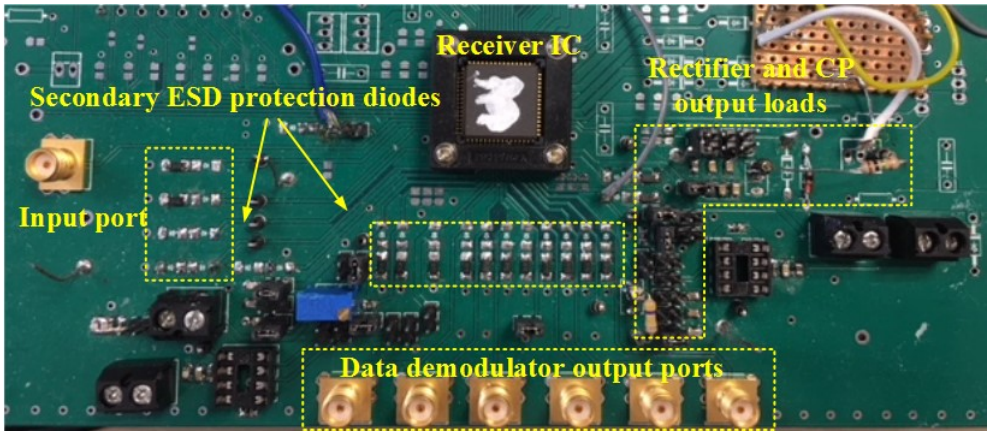


Figure 5.2 Photo of wireless energy harvest receiver IC test-board.

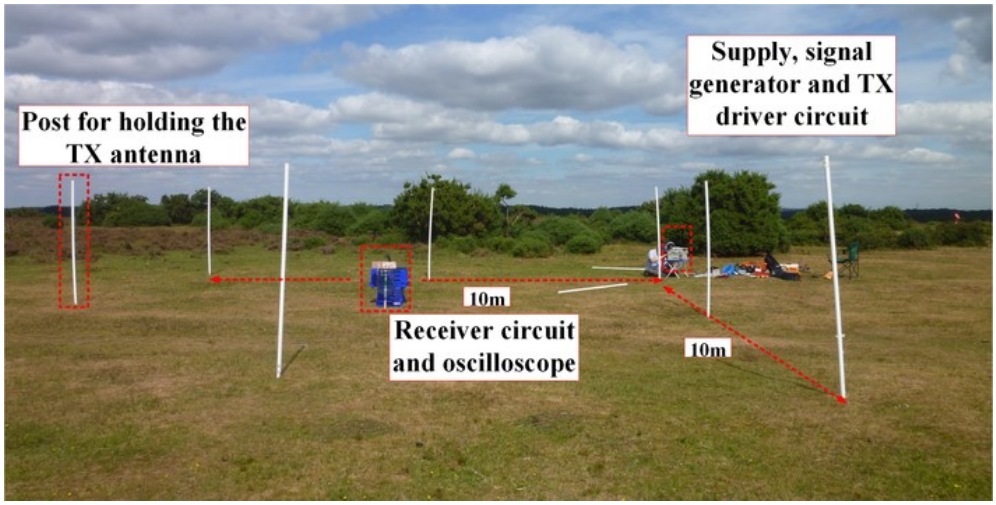


Figure 5.3 Field experiments setup for inductive wireless energy harvesting system measurement.

Table 5.1 Parameters of the large area loop antenna and the ferrite rod antenna used for the field measurement.

Large loop transmitting antenna		**Ferrite rod receiving antenna**	
Parameters	**Value**	**Parameters**	**Value**
Operating frequency	824kHz	Ferrite rod permeability	20
Transmitting current (RMS)	210mA	Ferrite rod diameter	8mm
Width of the square loop	10mx10 m	Ferrite rod length	45mm
Vertical distance (z-axis) between the TX coil and RX coil	0m	Radius of the conductor	0.1mm
Conductor skin depth	71.8µm	Number of turns	32
AC resistance	0.57Ω/m	Conductor skin depth	71.8µm
Inductance	90µH	Resistance	0.826Ω
Resonant capacitance	413pF	Inductance	53µH
Q-factor	21	Resonant capacitance	700pF
		Q-factor	33

5.2 Measurement Results

5.2.1 Laboratory Experiment Results

Figure 5.4 presents the output voltage and PCE measurement results of the rectifier of the receiver IC. The input voltage generated by the signal generator with 1MHz frequency is applied for the rectifier measurement. Further, the loading capacitor of the rectifier used in this measurement is 10µF. It can be seen that the rectifier can start up with the minimum input voltage (V_{IN}) of 200mV$_{pk}$ and the output voltage (V_{rect}) reaches 900mV when V_{IN} is approximately 230mV$_{pk}$ when the loading resistance (R_{Load1}) is 470kΩ. The result implies that the receiver IC can provide 1.72µW power to the system with the incoming input voltage of 230mV$_{pk}$. The rectifier output voltage decreases as the loading current is increased, as expected. On the other hand, the PCE of the rectifier peaks at 25% when V_{IN} is approximately 250mV$_{pk}$ and rapidly falls when V_{IN} is increased due to the reverse leakage current, as discussed in the previous chapter. The rectifier efficiency starts to increase again when the input voltage is above 400mV$_{pk}$ as the rectifier switches to the high-efficiency mode similarly to the simulation result shown in Figure 4.12. The decreased PCE when the input voltage exceeds 500mV$_{pk}$ is caused by the voltage limiter that limits the output voltage V_{rect} at 1.6V.

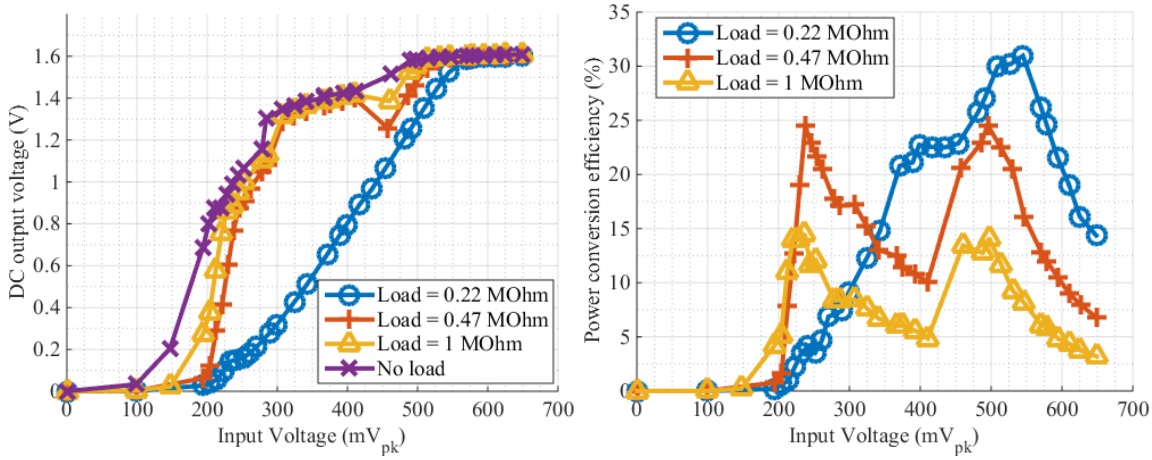


Figure 5.4 IC measurement of the rectifier output voltage (left) and the PCE (right) versus input voltage when the operating frequency is 1MHz shown with different loading resistors.

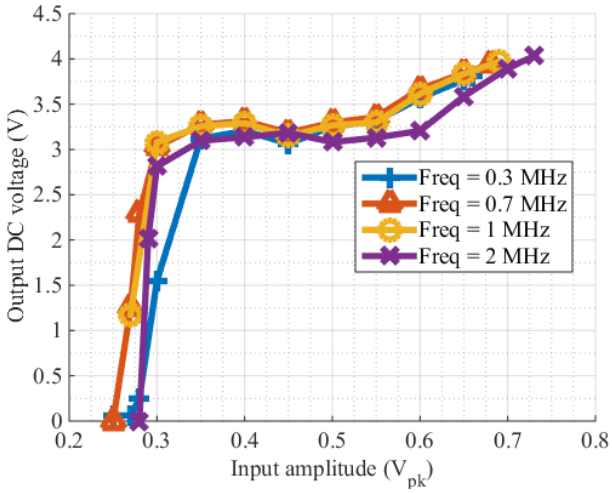


Figure 5.5 DC output voltage measurement of the DC-DC CP in the receiver IC when the loading resistance is 10MΩ shown with different rectifier input frequency.

Figure 5.5 shows the measurement result of the DC-DC CP in the receiver IC when the loading resistance (R_{Load2}) is 10MΩ with different rectifier input frequency. It can be observed that the output voltage is usable when the input voltage of the rectifier is approximately 300mV_{pk}. At the CP start-up voltage of 300mV_{pk}, the CP can deliver 0.9µW to the load which is extremely limited compared with the required power consumption of external modules. But as we mentioned previously in section 3.1, the external modules power consumption from the typical example can be reduced to be less than 0.9µW if the idle mode period is increased. In addition, it can be seen that the CP output voltage is also dependent on the input operating frequency since the CP clock is provided by the PLL reference clock which is recovered from the incoming carrier signal. A local clock generator used for the CP may be needed to improve the circuit.

The QPSK demodulator is tested by applying the 230mV_{pk} input signal (V_{IN}) with 1MHz frequency to the input of the receiver IC. A pseudo-random 1.6kbps data is modulated in QPSK by the signal generator. Furthermore, the receiver IC is self-powered by the on-chip rectifier and PMU. Figure

5.6 presents the waveform from the measurement of the QPSK data demodulator re-plotted in MATLAB. The results show that the 1.6kbps QPSK data demodulation of the self-powered receiver IC is achievable. It can be seen that the reference clock *PLLref* (VCO output divided by four) remains unchanged when the input signal *PLLin* is phase shifted, as expected. In addition, the demodulator power consumption is 1.27µW at 630mV supply voltage.

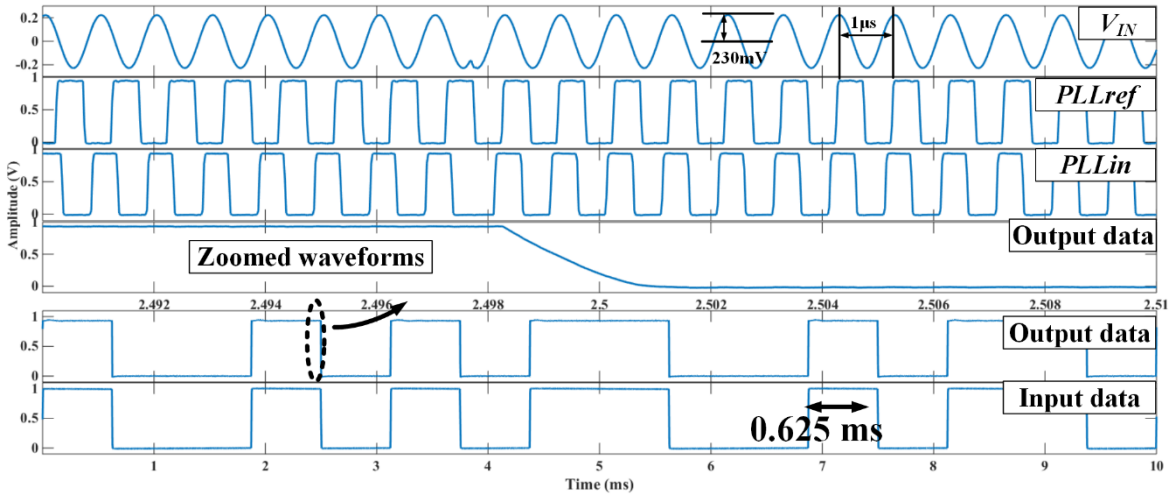


Figure 5.6 Waveform from the measurement of the QPSK data demodulator when the input voltage is 230mV$_{pk}$ with 1MHz carrier frequency and the data rate is 1.6kbps.

Note that an LC-circuit is not used in this measurement. The proposed QPSK demodulator of the prototype receiver IC fails to demodulate the QPSK data when the LC-circuit has a Q-factor larger than 3. This is because the QPSK signal phase transition is distorted by the high-Q LC-circuit which leads to the unstable reference clock generated by the proposed demodulator. More details of the QPSK signal in a high-Q LC-circuit will be explained in the next chapter.

5.2.2 Field Experiment Results

Figure 5.7 shows the comparison of the calculated and measured received voltage at the receiving ferrite rod antenna which is connected to the input of the receiver IC. The receiver IC is tested at different positions within the large area of the transmitter loop antenna where the vertical distance (z-axis) between the transmitter coil and the receiver coil is approximately 0m. The measurement point is moving from one of the edges of the square (x =-5m, y = 0m) to another end (x = 5m, y = 0m). The results are close when the measurement point is far from the large area loop edges, however the deviation between the calculation result and the measurement result is apparent when the receiver is moving toward the edges. One of the main reasons that causes the deviation is that the loading resistance on the receiving coil in the calculation is assumed to be constant while the actual loading resistance contributed by the receiver IC depends on the rectifier input voltage and output current, as explained in section 3.2.

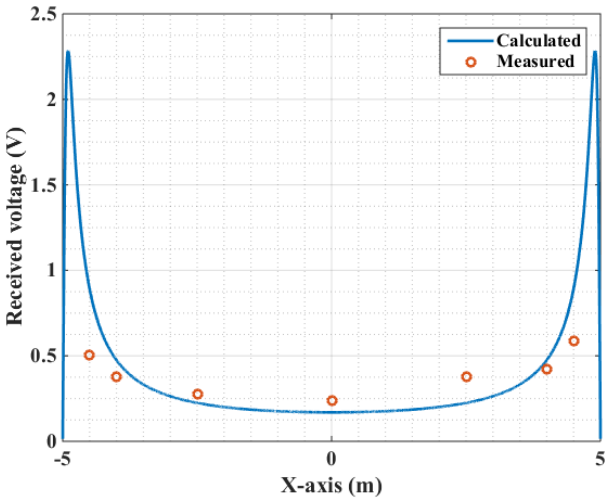


Figure 5.7 Comparison of the calculated and measured received voltage (V_{RX}) at the receiving ferrite rod antenna when y = 0m and z = 0m.

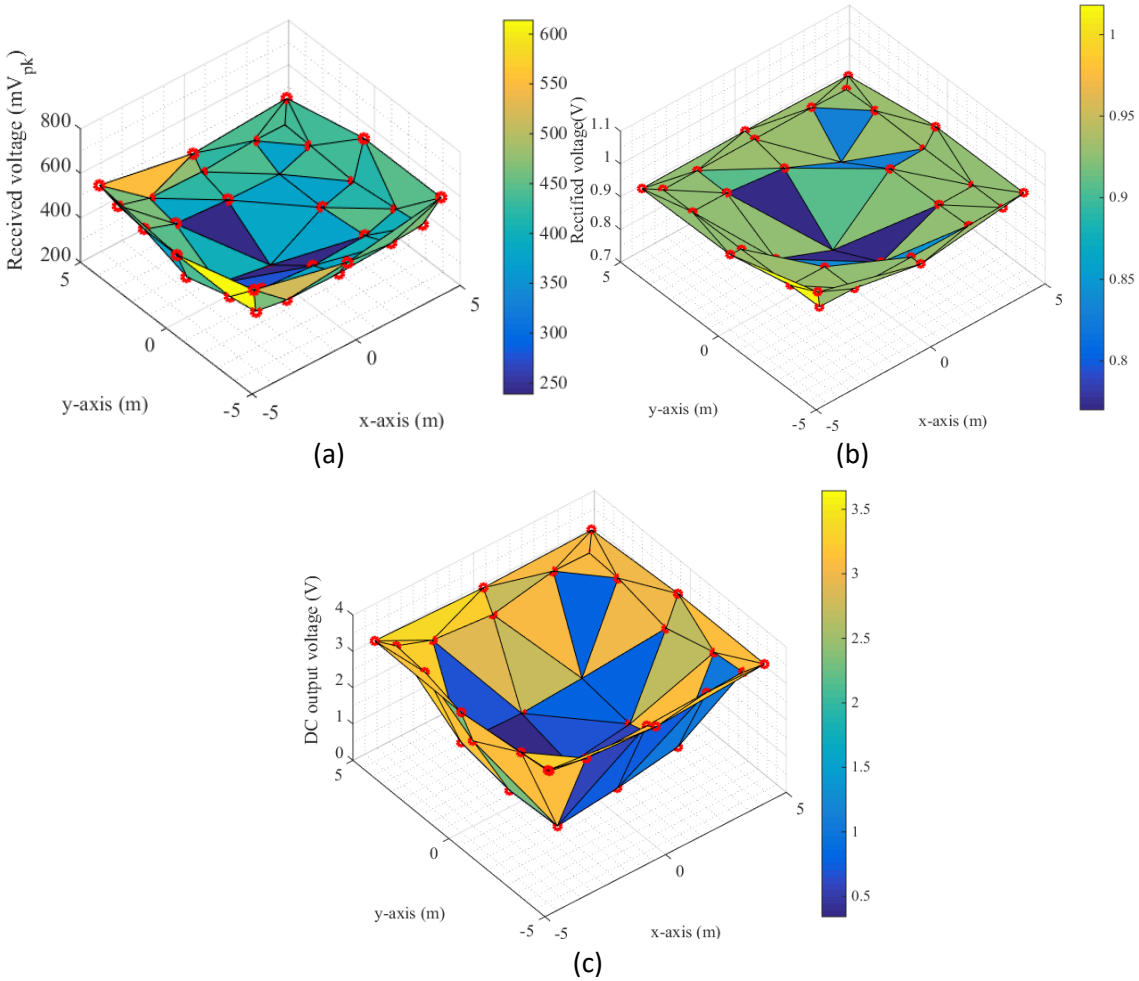


Figure 5.8 Receiver IC field measurement results of (a) the received voltage at the secondary coils (V_{RX}), (b) the rectified voltage at the output of the rectifier (V_{rect}) and (c) the output voltage from the DC-DC converter (V_{CP}).

The measurements of the harvested voltage V_{RX}, V_{rect} and V_{CP} of the receiver IC in a grid where the origin (x =0 m, y = 0m) is at the centre of the loop are presented in Figure 5.8. Similar to the calculated results, the measured received voltage V_{RX} peaks at approximately 600mV$_{pk}$ when the

receiver IC sits near to the boundaries of the transmitting square loop and decreases to approximately 250mV$_{pk}$ when the receiver is placed at the centre of the loop. The measurement result of the rectified output V_{rect} varies between 0.8V and 0.9V, which indicates that the rectifier can operate even when the input amplitude is as low as 250mV$_{pk}$. Further, the maximum output power of 1.33µW with 3V DC output voltage is harvested by the receiver IC when the receiver is close to the boundary of the primary square loop coil (i.e., [x=-4m, y = -4m], [x=4m, y=4m], [x=-4m,y=4m], etc.). However, the received voltage is insufficient to generate a 3V output voltage when the receiver is at the centre of the square loop. We attempted to increase the received voltage by increasing the transmitting current I_{TX} from 210mA$_{RMS}$ to 570mA$_{RMS}$. As a result, the output power of 0.73µW with 2.71V output voltage is harvested from the receiver at the centre of the square loop. The result verifies that the received magnetic energy can be increased to usable levels to power all the systems by increasing the transmitter loop current.

As the proposed QPSK demodulator cannot demodulate the QPSK signal in a high-Q resonant system, the QPSK demodulation field experiment result is not shown in this section. More details about the issue are addressed in the next chapter.

5.3 Design Improvement Requirements of the Energy Harvesting and Data Demodulator Circuits

Most of the design challenges listed in Chapter 3 have been addressed. The measurement results show that the proposed switch-over cold-start subthreshold voltage rectifier can operate under the minimum voltage measured in the field. Further, the ultra-low power circuit design enables the receiver IC to harvest the limited energy to power the internal circuit and external modules. The laboratory result shows that the QPSK data demodulator can be used for the wireless sensor network synchronisation.

However, the proposed demodulator fails to extract data when the QPSK signal is amplified by the high-Q resonant LC tank. Moreover, the accurate tuning of the LC tank for resonant matching has not been addressed. Furthermore, although the proposed rectifier can operate with the low start-up voltage and provide high efficiency when the input voltage is relatively large, however, the rectifier still suffers from the large reverse leakage current occurring at the moderate input voltage level (between 300mV$_{pk}$ and 400mV$_{pk}$). Due to the short-comings found in the first IC prototype, a second IC implementation is required to address these issues. The requirements for the design improvement of the energy harvesting and data demodulator circuits are listed as follows:

- The rectifier circuit needs to provide high efficiency over a wide input voltage range since the harvested voltage can be varied when the receiver is placed in different locations.
- The PSK demodulator needs to be able to extract the QPSK data that has a slow phase transition due to the high-Q resonant circuit.
- The automatic capacitor tuning circuit is needed to match the receiver antenna resonant frequency to the source frequency.

Based on these requirements, the second IC prototype will be presented in the next chapter.

5.4 Summary

Laboratory and field experiments of the magnetic loosely coupled wireless energy harvesting receiver prototype IC have been presented. The laboratory experiment results verify that the proposed rectifier can operate with the subthreshold input voltage to provide a usable DC output voltage. The QPSK data extraction at low data rate has been demonstrated in the laboratory experiment. In addition, the laboratory measurement results show that the receiver IC consumes an ultra-low power below 3μW. For the field experiment, the MF magnetic transmitter coil has been implemented to evaluate the performance of the energy harvesting system. The field measurement of the received voltage shows the expected results where the received voltage peaks at the transmitter loop boundary and decreases when the receiving point is far away from the transmitter loop perimeter. In addition, the field measurement results verify that the receiver prototype IC can be used to harvest the MF magnetic energy and provide a sufficient output voltage.

However, the QPSK data demodulator of the receiver IC fails to extract data in the field experiment due to the high resonant behaviour of the receiver antenna. A few issues including the LC-resonant frequency mismatch and the rectifier efficient drop during a certain input voltage range has not been solved. Therefore, the second prototype IC will be presented in the next chapter to address the remaining issues.

Chapter 6: SEGMENTED RECTIFIER, HIGH-Q QPSK DEMODULATOR AND LC-TUNE CIRCUIT DESIGN

The medium frequency (MF) magnetic loosely coupled wireless energy harvesting receiver IC has been presented in Chapter 4 and 5. The proposed design has solved several design challenges. However, a few problems are still visible. The proposed rectifier still suffers from low efficiency at a certain input voltage range due to the reverse leakage current. Moreover, the proposed demodulator cannot extract the QPSK data from a high-Q receiver antenna. Furthermore, the LC-tuning circuit used for matching the receiver antenna resonant frequency to the incoming frequency has not been presented in the first IC prototype. In this chapter, an improved receiver IC is presented to address the remaining problems.

6.1 System Architecture

Figure 6.1 presents the simplified system architecture of the new wireless energy harvest receiver IC. The system consists of a segmented rectifier, a QPSK demodulator able to deal with a high-Q factor channel path, a tuning binary weighting capacitor circuit, an efficiency tracking circuit and a power management unit (PMU). The rectifier is modified to improve the efficiency performance. A novel technique is added to the previously proposed data demodulator to solve the QPSK demodulation issue caused by the high-Q resonant behaviour. Further, the new tuning capacitor and efficiency tracking control are included to increase the harvested voltage of the receiver IC. The previous PMU is re-used to manage the available power at the receiver. The newly added blocks are described in the following sections.

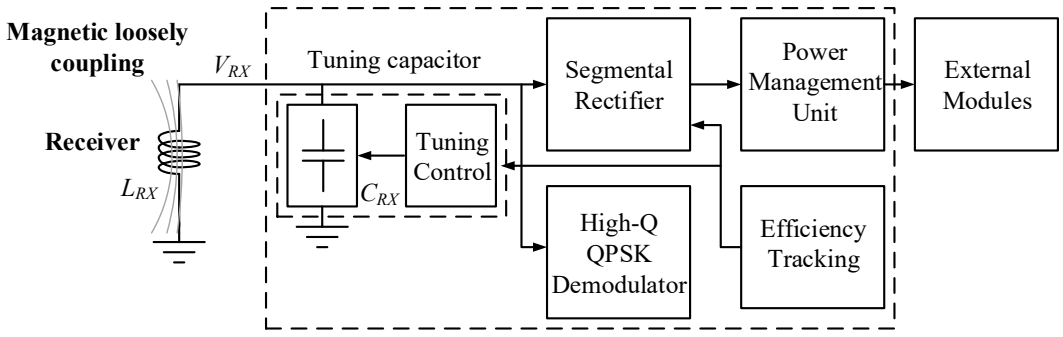


Figure 6.1 Simplified system architecture of the energy harvesting receiver IC.

6.2 Segmented Rectifier

As the received voltage at the receiver antenna from the magnetic coupled wireless energy harvest can be varied depending on the receiver position, as shown in the field measurement results in

section 5.2.2, a rectifier with high power conversion efficiency (PCE) over a wide input range may be useful to maximise the harvested energy. However, the PCE measurement result of the previous rectifier depicted in Figure 5.4 shows that the efficiency drops when the input voltage is between $300mV_{pk}$ and $400mV_{pk}$. This is caused by the reverse leakage current as the rectifier is operating in the subthreshold mode. The PCE will not be improved by switching the rectifier to the high voltage mode as the input voltage is insufficient to fully activate the MOS transistors in basic diode connection configuration.

There are two main reasons that cause the PCE of the rectifier SVC-based to peak only at a specific voltage range; one is the bias voltage in series with the gate-to-source voltage of the diode-connected transistors, and another is the dimension of the transistors. Since the bias gate-to-source voltage (V_{GS}) of the SVC is fixed at a certain range, the reverse leakage current occurs when the input voltage exceeds the certain threshold value corresponding with the fixed bias V_{GS}. Thus, the peak of the PCE can be shifted by manipulating the bias voltage connecting at the gate-to-source voltage of the transistors [11, 14, 41]. Alternatively, the dimensions of the transistor can reduce the reverse leakage current by decreasing the width of the transistors, which results in shifting the PCE since the start-up voltage is also shifted.

[11], [14] and [41] proposed the PCE optimising method by changing the bias voltage V_{GS} of the transistor. In [11] and [14], the V_{GS} bias voltage is increased/decreased by switching the gate of a transistor from one node to another node that provides a different voltage bias. For this method, the circuit implementation is relatively simple. However multiple stages of the rectifier are needed in order to produce a wide PCE range since the number of nodes for switching is limited. As a result, multiple coupling capacitors are used which consume a much larger area. In [41], the bias voltage V_{GS} is provided by the secondary tuneable DC voltage, however the system cannot start from cold due to the requirement of the secondary DC voltage source.

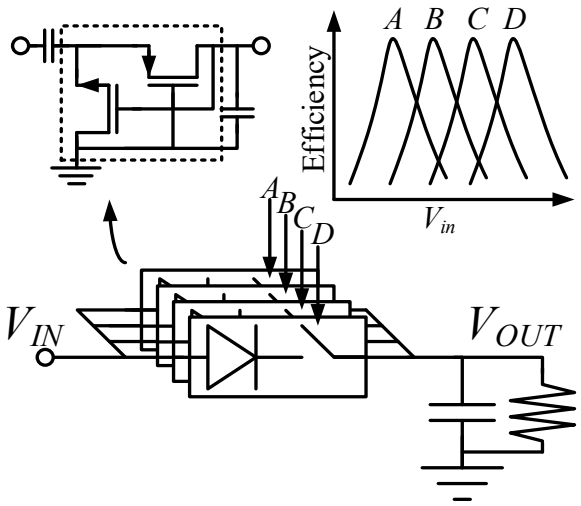


Figure 6.2 Simplified schematic diagram shows the concept of the proposed segmented rectifier.

Figure 6.2 shows the concept of the proposed segmented rectifier. Multiple diodes with different dimensions are selectable. As the reverse leakage current of each diode occurs at different input voltage range, therefore, the wide range PCE can be achieved by switching to the 'correct' diode according to the incoming input signal. Also, multiple stages or an external DC source are not needed.

Figure 6.3 depicts the schematic diagram of the proposed two-stage segmented rectifier with three switchable conditions. At cold-start, the rectifier is connected in the subthreshold mode where the signal is flowing through the parallel capacitor C_{SW} similarly to the previously proposed rectifier shown in section 4.3.1.1. When the output rectified voltage is sufficient, the efficiency control unit switches the mode of the rectifier according to the amplitude of the input signal. The proposed circuit can operate in three modes which are (A) the subthreshold mode when switches *SWA* are closed, (B) the subthreshold mode when switches *SWB* are closed and (C) the high voltage mode when switches *SWA* and *SWB* are opened. The transistor width used in mode A (M_{pAn}) is larger than the transistor width used in mode B (M_{pBn}), hence the PCE of the rectifier mode A peaks at the lower input voltage range compared with the PCE of the rectifier mode B. On the other hand, the PCE of the rectifier mode C peaks at the higher input voltage range since the rectifier is configured in a conventional voltage doubler/multiplier configuration, the same as the previous design. Note that the mode C rectifier is also benefiting from having a wide width transistor M_{PA} as the maximum output current is proportional to the transistor width.

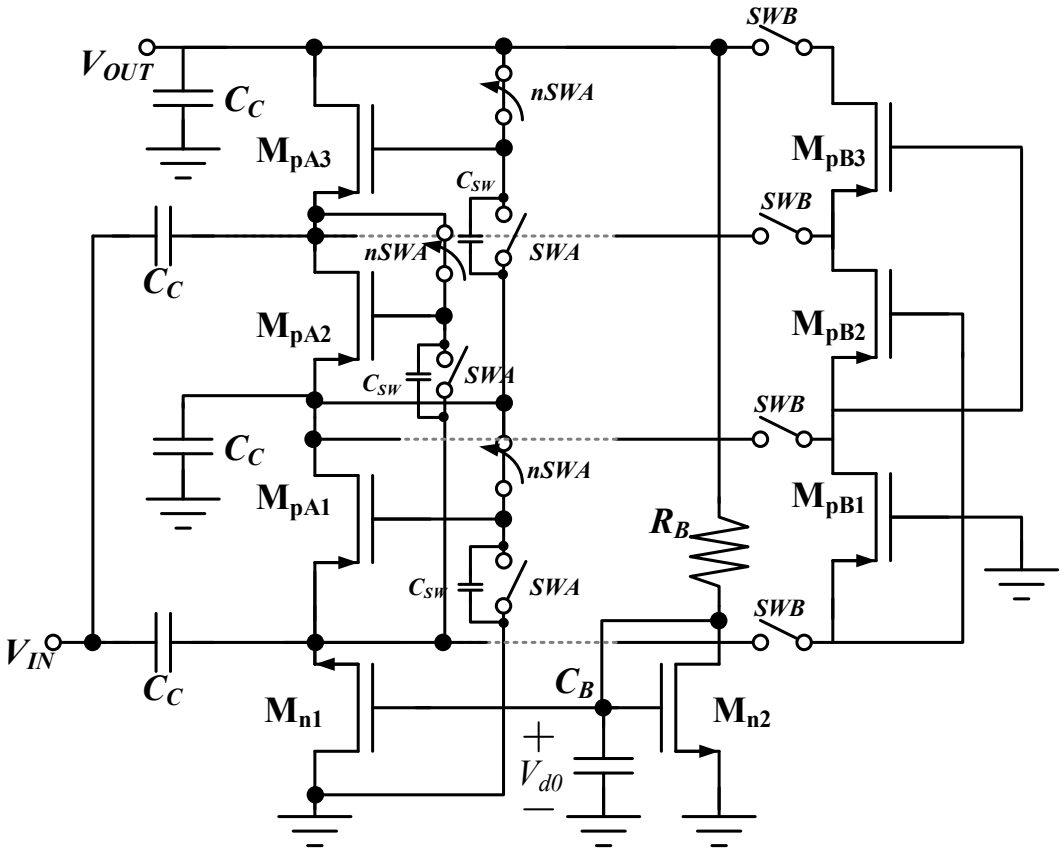


Figure 6.3 The schematic of the proposed two-stage segmented rectifier.

Figure 6.4 shows the simulation results of the segmented rectifier output voltage and PCE operating in three different modes. The input frequency is 1MHz, and the circuit is loaded with a 250kΩ resistor. Moreover, a voltage limiter circuit is used to limit the rectifier output voltage not to exceed 1.8V. It can be seen that the start-up voltage of the rectifier at mode A is lower than its counterparts. Furthermore, the efficiency of each mode peaks at different input voltage ranges at approximately 35%. The overall efficiency of the rectifier is above 25% when the rectifier input is between 250mV$_{pk}$ and 600mV$_{pk}$. It is important to note that the decreased PCE of the rectifier in mode C when the rectifier input voltage is above 500mV$_{pk}$ is due to the voltage limiter circuit.

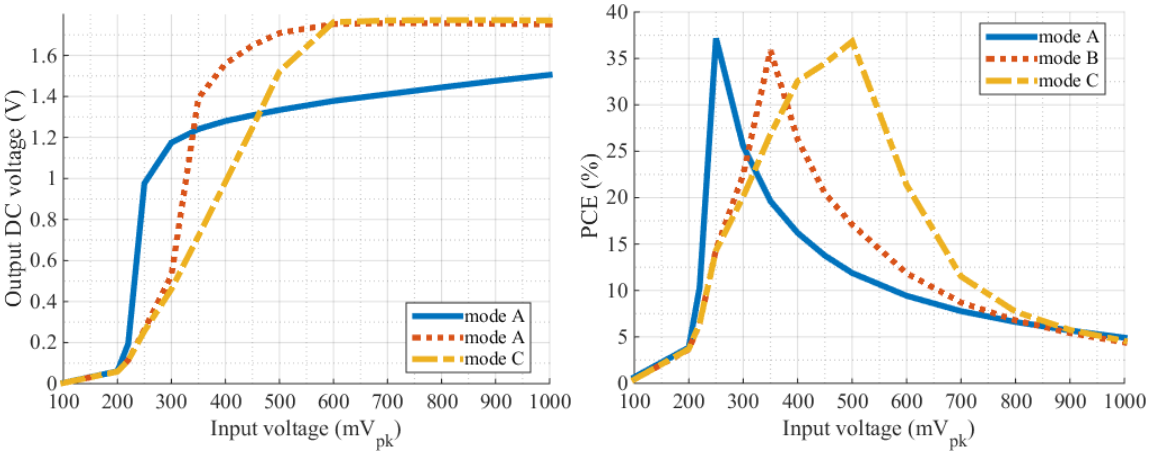


Figure 6.4 Output voltage (left) and PCE (right) versus input voltage of the segmented rectifier with three different configurations with 1MHz input frequency and 250kΩ load resistor.

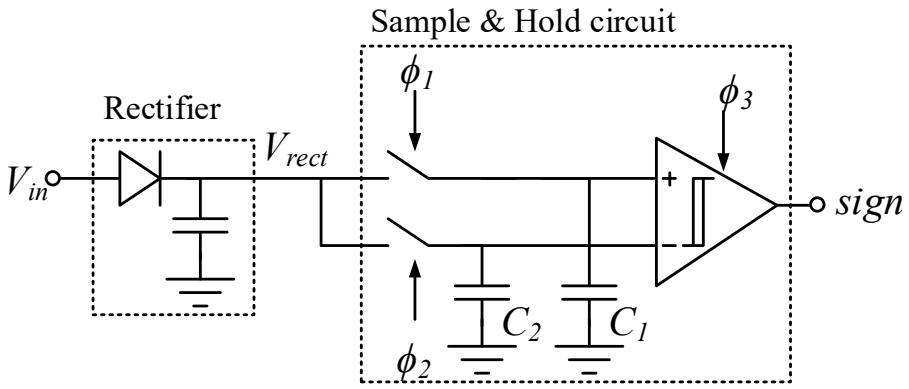


Figure 6.5 Sample-and-hold circuit.

The mode of the rectifier corresponding with the rectifier input signal is controlled by the maximum efficiency tracking circuit which is implemented by a sample-and-hold and a digital control unit [11, 69, 70]. The sample-and-hold circuit, illustrated in Figure 6.5, is used to compare the output voltage from the rectifier (V_{rect}) at different modes while the decision is made by the control unit. In addition, a hysteresis characteristic is added by switching the sampling capacitors C_1 and C_2 according to the comparator output. A StrongARM latch comparator, powered by the rectifier output V_{rect}, is chosen since its power consumption is much less compared with the static

comparator used in the previous design [71]. The schematic diagrams of the hysteresis sample-and-hold circuit and the comparator are shown in Appendix H.1.

Figure 6.6 depicts the control unit state machine and the timing diagram of the segmented rectifier. The signals ϕ_1, ϕ_2 and ϕ_3 are generated to control the sample-and-hold circuit while the signal *sign* is the output logic from the sample-and-hold. Moreover, the *up* and *down* logic signals control the switching mode of the rectifier. As three rectifier modes are possible in this design, the control unit only requires eight clock cycles to complete the evaluation phase. When the evaluation phase is ended, the clock signal *ck* that controls the digital control unit is held and the control unit returns to the idle phase. The duty cycle of the evaluation phase is designed such that the period is much shorter than the idle phase (1% of the idle phase period) to minimise the efficiency overhead. In addition, the clock reference of the control unit, implemented from a saw-tooth generator, is shown in Appendix H.2. Note that a 630mV supply voltage provided by a voltage regulator is used to supply the VCO and the control unit. The control unit is enabled by the PMU when V_{rect} exceeds the threshold voltage which is defined by the minimum supply voltage requirement of the voltage regulator and the data demodulator. More details are provided in section 6.5.

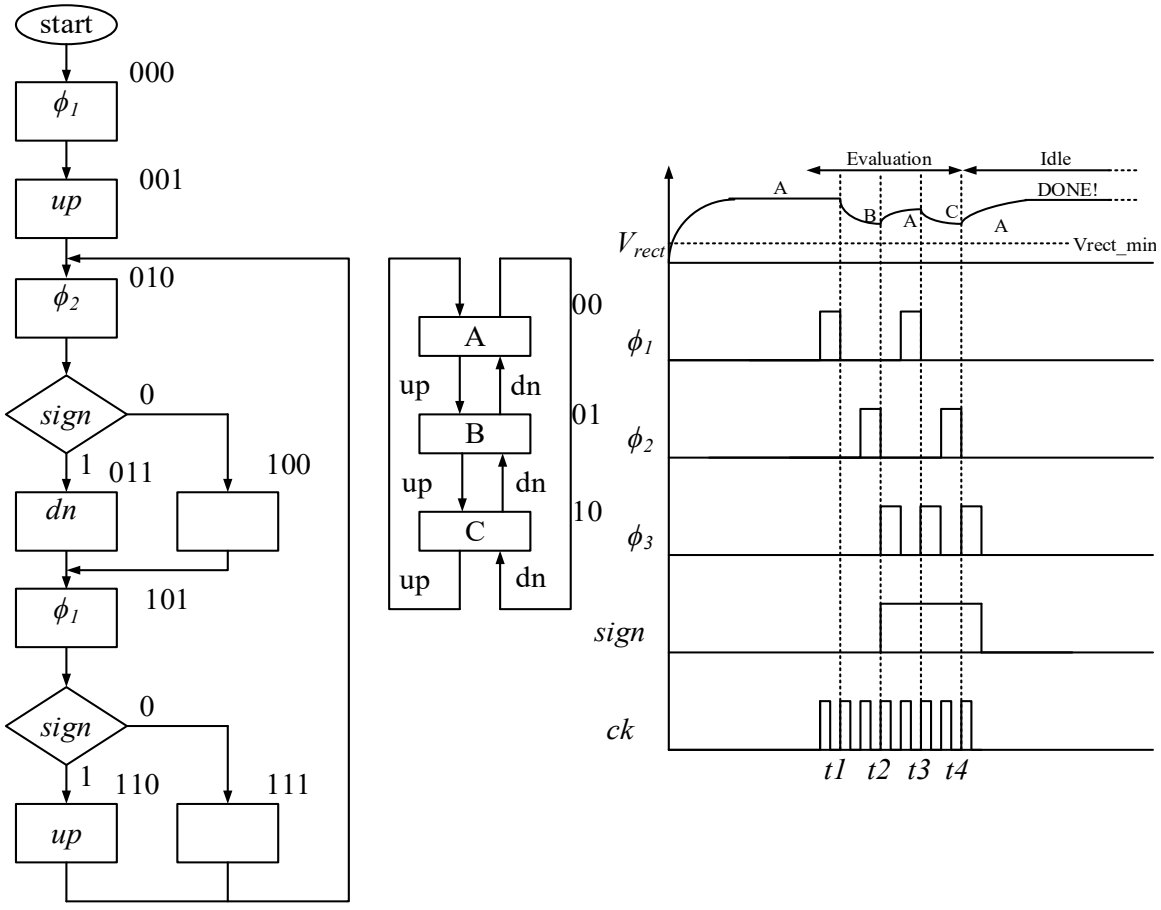


Figure 6.6 State machine of the control unit of the rectifier (left) and its timing diagram (right).

The timing diagram in Figure 6.6 shows an example of how the rectifier operates when the input voltage is relatively low. Initially, the rectifier operates in mode A, starting from cold while the

control unit is in the idle phase. When the output voltage V_{rect} is sufficient to power the system, the clock signal *ck* is generated and the control unit enters the evaluation phase. At *t1*, the rectifier is switched to mode B which consequently decreases the rectifier output voltage. The sample-and-hold circuit identifies that the output voltage of the rectifier in mode A is higher than mode B, hence the control unit reverts the rectifier back to mode A at *t2*. Similarly, the control unit compares the output of rectifier mode A with mode C during the period between *t2* and *t4*. Eventually, the rectifier is switched to mode A and the evaluation phase of the control unit is ended at *t4*.

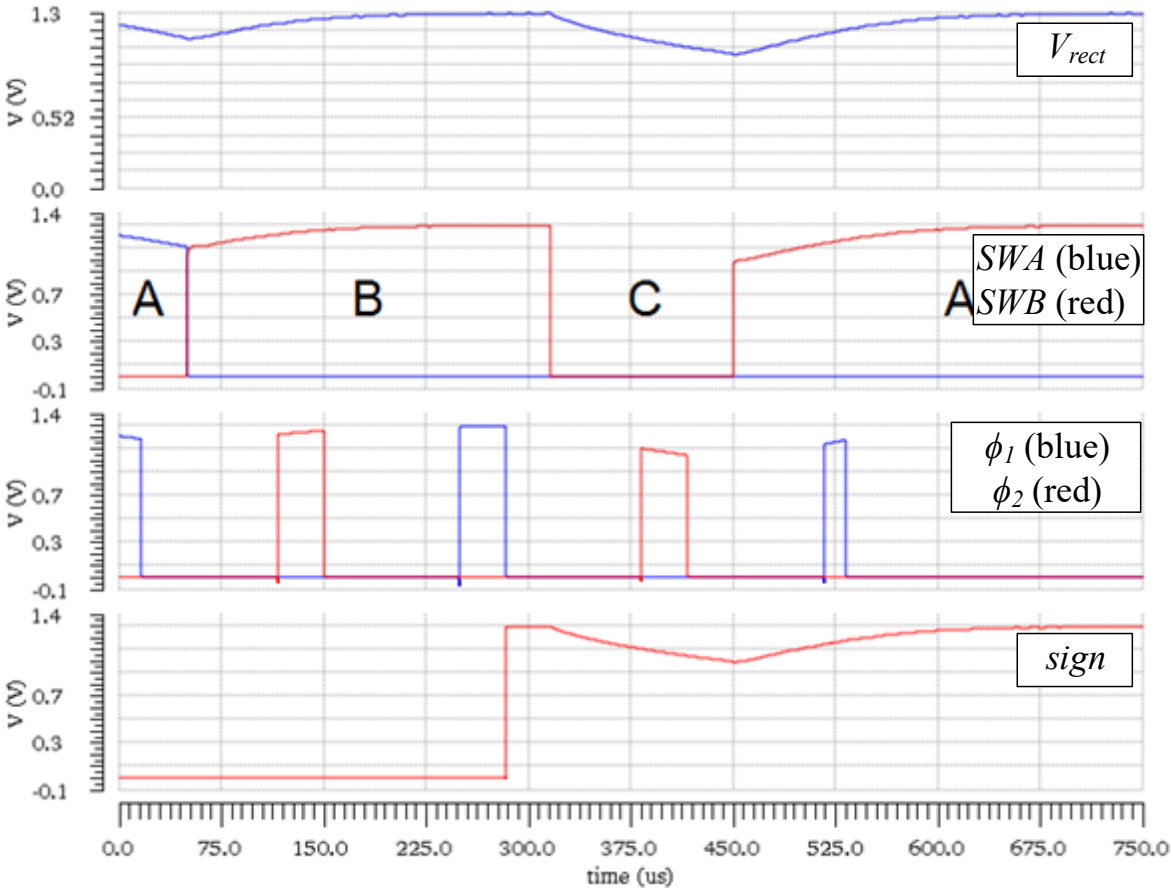


Figure 6.7 Transient response of the top-level segmented rectifier.

The top-level rectifier circuit is simulated to verify the control unit functionality. Figure 6.7 shows the output waveform from the transient simulation result. Initially the rectifier is operating in mode A and switches to mode B at 70µs, as a result; the output voltage is increased. At 320µs, the rectifier switches to mode C which causes the output voltage to decrease. The control unit detects that the rectifier mode B is the optimum mode corresponding to the input voltage, hence the rectifier is switched back to mode B at 450µs and the control unit enters the idle mode. In addition, the simulated power consumption of the sample-and-hold circuit including the reference clock oscillator is 98nW at 1V rectifier output voltage. Note that the sample-and-hold circuit only consumes power when the circuit enters the evaluation mode. Further, the efficiency tracking digital control unit consumes only 4.8nW.

6.3 High-Q QPSK Data Demodulator

The proposed demodulator presented in Chapter 4 can extract data from the QPSK modulator by comparing the stable reference signal with the incoming QPSK signal. However if the PSK voltage signal is boosted by a high-Q resonant LC circuit at the receiver input, the high-Q LC circuit could potentially distort the PSK signal such that the PSK phase transition occurs slowly instead of abruptly. As a result, the demodulator fails to produce the stable reference clock as the phase of the clock follows the slowly drifting incoming PSK phase shift.

Figure 6.8 shows the simulated waveforms of a 1MHz QPSK signal (V_{TX}) applied to a resonant circuit with two different Q-factors varied between Q=1 and Q=15. When the phase shifting occurs at t_1, it can be seen that the phase of the received voltage (V_{RX}) cannot change simultaneously. V_{RX} gradually shifts the phase from 0 to 90-degree in approximately 7 cycles of the voltage when Q=15. On the other hand, V_{RX} for a low Q-factor (Q = 1) almost abruptly changes the phase when V_{TX} is phase shifted. In addition, the data rate of the PSK modulation is limited by the time that is needed for the signal to complete the unit symbol phase transition. For example, the maximum achievable data rate of a 1MHz QPSK signal in the resonant LC-circuit with Q=15 is approximately less than 140kbps ($DR \leq \frac{1}{7cycles} * 1MHz$). The equation used for calculating the number of cycle of the slow phase transition due to the Q-factor will be shown later. Note that the data rate used for the target application is only in a range between 1kbps and 10kbps.

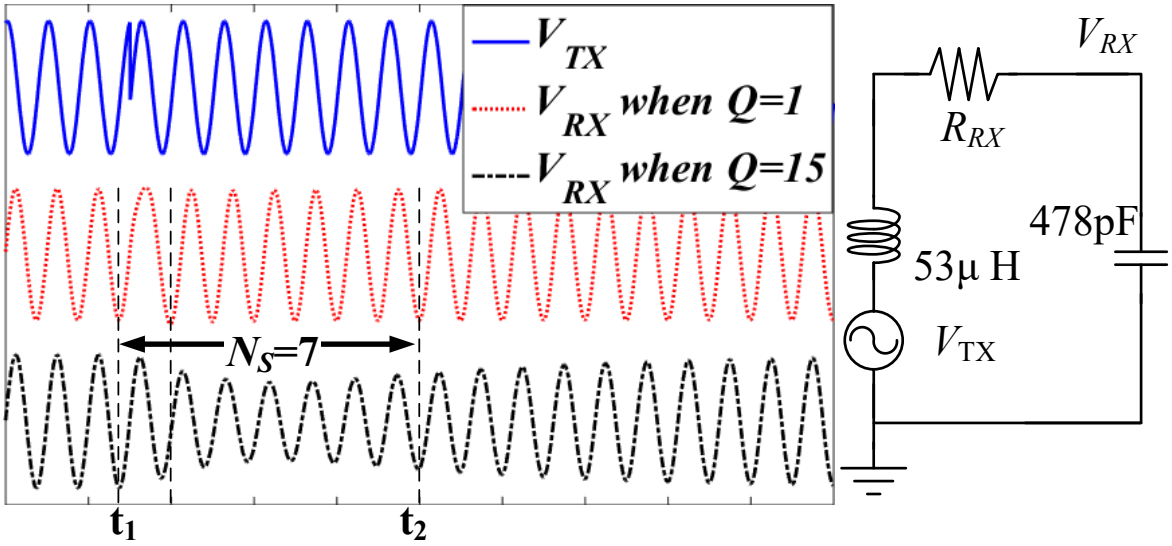


Figure 6.8 Waveforms of the QPSK signal applied to a high-Q resonant RLC circuit.

The settling time derived from the second-order system of the RLC resonant circuit can be used to approximate the settling time of the phase shifted QPSK signal (t_S). A comparison between the simulation and the calculation results has been done to verify that the equation is accurate. Equations (6.1) and (6.2) show the settling time of the RLC resonant LC circuit [72] that can be used to estimate the QPSK phase shift settling time when T_n is the period of the incoming input

voltage and ϕ_r is the acceptable relative phase tolerance for accurate phase change detection. A relative phase tolerance of 0.8 (20% deviated from the ideal phase, i.e., 72° phase shifted for a QPSK signal) extracted from a conventional PSK demodulator simulation result is used in this section. From the equation, it can be seen that the phase settling time t_S is proportional to the Q-factor of the LC-circuit.

$$t_S = -\frac{\ln(1-\phi_r)}{\zeta\omega_n} = -\frac{2Q\ln(1-\phi_r)}{\omega_n} \quad (6.1)$$

$$N_S = t_S / T_n \quad (6.2)$$

Having a gradual phase changing at the received voltage is an issue since the proposed QPSK demodulator presented in section 4.3.2 can only extract the data from near-ideal abrupt QPSK phase shifting ($t_S \approx 0$s). The previous proposed CDR-PLL-based QPSK demodulator generates a constant reference clock where the phase of the clock is insensitive to the missing incoming pulses of the sliced QPSK input signal. However, the distorted slow phase changes of the QPSK affected by a high-Q LC-circuit, which can be considered an input jitter, are transferred to the reference clock generated by the CDR-PLL. Hence, the reference clock using for extracting the data from the incoming QPSK signal is no longer a fixed reference when the input carrier phase gradually shifts.

As the conventional Hogge PD used in the previous design shown in section 4.3.2 is not suitable for such circumstances, a PD that is not sensitive to a gradual phase shifting QPSK is needed for a high-Q inductive loosely coupled energy harvesting receiver. A blind oversampling phase detection CDR may be a potential candidate for the high-Q receiver as the control loop blindly samples the input signal without tracking the input phase [73, 74]. However, the control system requires a multi-phase clock signal in order to perform the oversampling phase detection. As a result, either a much faster or a multi-stage ring oscillator which consumes higher power consumption may be needed. Moreover, the design of the data detection using multiple clock signals phases is likely to be complex and power hungry as well. The input jitter reduction technique presented in [75] can potentially be used to extract the slow phase change QPSK signal, however, the system requires multiple PLL blocks which are likely to consume more power than a single CDR/PLL block.

Instead of using a high-frequency sampling rate to extract the QPSK signal used in a high-Q resonator, we propose an alternative method. Considering Figure 6.9, the sliced QPSK signal (*PLLin*) in the high-Q resonant circuit (i.e., *Q*=5) requires approximately 2 cycles to fully shift the phase. If the QPSK signal is sub-sampled at the fourth rising edge of the signal, then the output result of the sub-sampled signal is not affected by the gradual phase shifting. Hence, the sub-sampled signal can be used as the input data of the previous proposed demodulator to recover the stable reference clock.

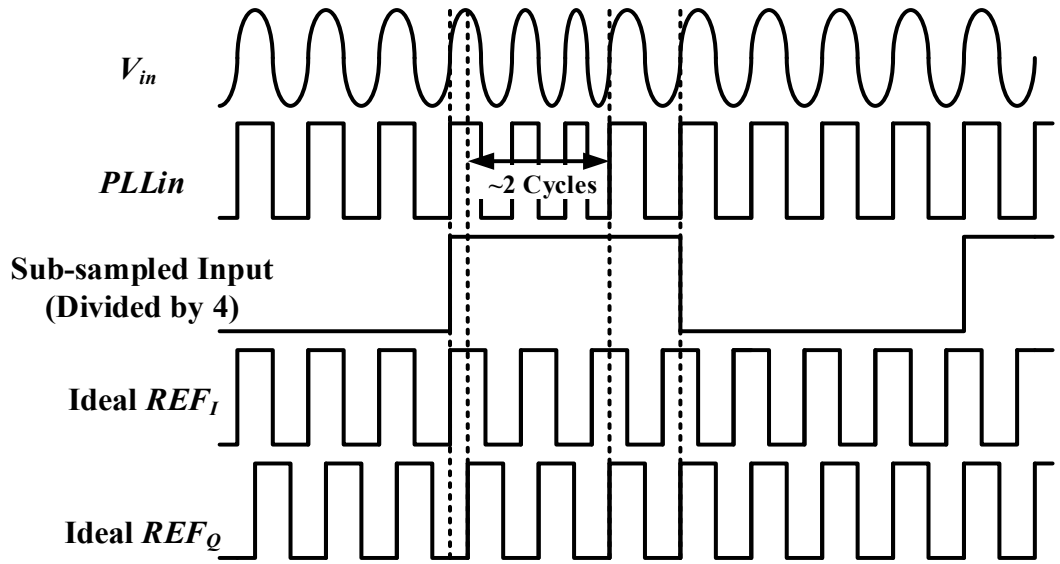


Figure 6.9 Waveforms show the concept of the high-Q QPSK demodulation.

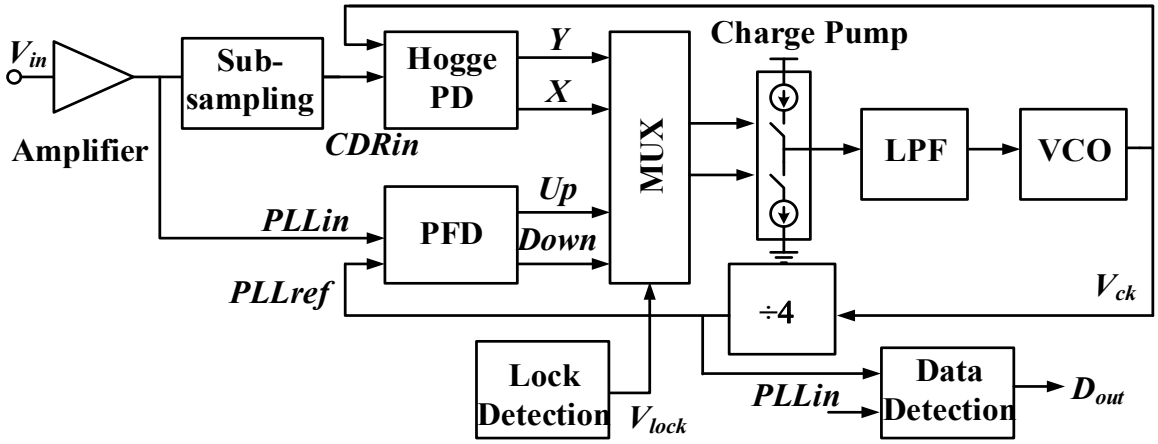


Figure 6.10 Proposed input sub-sampling high-Q QPSK data demodulator.

Figure 6.10 presents the system architecture of the proposed input sub-sampling high-Q QPSK data demodulator. The system is developed from the previously proposed QPSK demodulator where the sub-sampling block is added to extract the QPSK data from the high-Q resonant circuit. The sub-sampling circuit was initially implemented from a frequency divider to produce the *CDRin* signal where the sub-sampling dividing ratio (N_{SS}) is selected from N_S calculated from the desired Q-factor of the transmitter/receiver LC-antenna using (6.2). As the transition rate of the signal *CDRin* is slow, the output signal of the Hogge PD is only updated when the signal *CDRin* is toggled, for example, *CDRin* is toggled every four cycles of the input signal *PLLin* when N_{SS}=4. The frequency tracking of the control loop, when the sub-sampling Hogge PD is operating, is also slow as a consequence. The control loop settling time when operating in the CDR mode can be reduced by increasing the transition rate, thus a multiplexer is used to switch the input signal of the Hogge PD, as can be seen in Figure 6.11. Initially, when the demodulator switches from the PLL mode to the CDR mode, an N-bit clock counter C0 in the sub-sampling block is reset and the multiplexer MUX0 switches the output to the *PLLin* and thus the input dividing ratio is N_{SS}=1. When *N* cycles of the

PLLin are counted, the CDR control loop should be stable and the counter C0 overflow signal (*SSon*) selects the multiplexer output from *PLLin* to *PLLss* as a result.

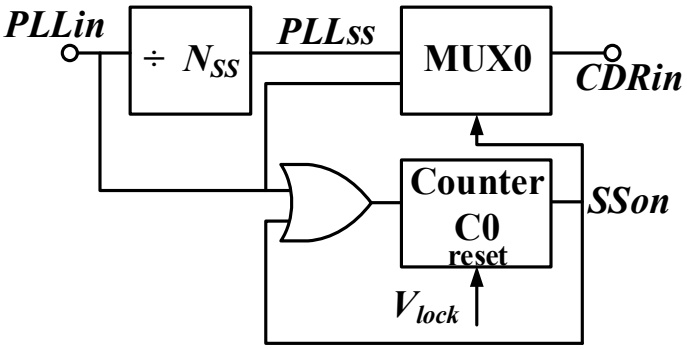


Figure 6.11 Proposed sub-sampling circuit and.

It is important to note that the sub-sampling dividing ratio can limit the data rate of the PSK demodulator. The sub-sampling period must be shorter than the period of the 1-bit data to ensure that the minimum bit period data is not overlooked by the slow sub-sampling rate ($t_{SS} < t_{data}$). As the data rate used in this project is intended to be less than 10kbps, the dividing ratio is more flexible. In addition, the frequency dividing ratio used in this project is configurable manually (N_{SS}=1, 4, 8, 16) for a more flexible Q-factor of the receiving LC-antenna. In practice, the receiver Q-factor can be estimated and thus N_{SS} can be chosen in an early stage of the circuit implementation without the requirement of a selectable N_{SS} of the sub-sampling circuit.

Moreover, the practical Q-factor of the secondary coil LC circuit is limited by the rectifier, as mentioned in Chapter 4. As the calculated input resistance of the rectifier is between 10kΩ and 100kΩ, the practical Q-factor of the receiver antenna is likely to be less than 100 when loaded. It has been shown in section 2.2.3 that the Q-factor of the receiving LC-antenna can be significantly reduced if the antenna loading resistor (which is the rectifier input resistor) decreases. For example, an unloaded LC-antenna with Q=333 (L_{RX}=53H, C_{RX}=478pF and R_{RX}=1) is reduced to 27.55 if the LC-antenna is loaded by a 10kΩ loading resistor. Note that the Q-factor of the receiving LC-antenna is initially high at cold-start since the rectifier has not drained a large input current (and hence the loading resistance is large). However, the PSK demodulator is only activated when the rectifier provides a sufficient supply voltage, hence the Q-factor is decreased when the PSK demodulator begins its operation since the rectifier is draining current from the LC-antenna. In this project, the calculated maximum achievable Q-factor of the proposed sub-sampling QPSK demodulator is approximately 70 using equation (6.2).

The proposed demodulator is simulated by applying a QPSK modulated signal with the carrier frequency of 1MHz and 100kbps data rate to the resonant LC circuit tested with different Q-factors. The resonant inductance and capacitance are 53µH and 478pF respectively. Figure 6.12 shows the

simulation result when the Q-factor of the LC tank is 33.33 and the sub-sampling dividing ratio is 16. It can be seen that the data can be extracted from the QPSK signal in the high-Q resonant circuit. Moreover reference clock *PLLref* remains constant as can be seen from the zoomed waveform from the simulation result shown in Figure 6.13. In addition, it can be observed that the phase of the recovered retimed output of *PLLin* from the Hogge PD abruptly shifts 90 degrees as expected. Further, the proposed demodulator power consumption from the simulation result is 612nW. Note that the power consumption of the demodulator used in this chapter is slightly lower than the power consumption of the previous demodulator shown in Chapter 4 since the internal circuit blocks (i.e., amplifier, VCO) are further optimised to reduce the power consumption.

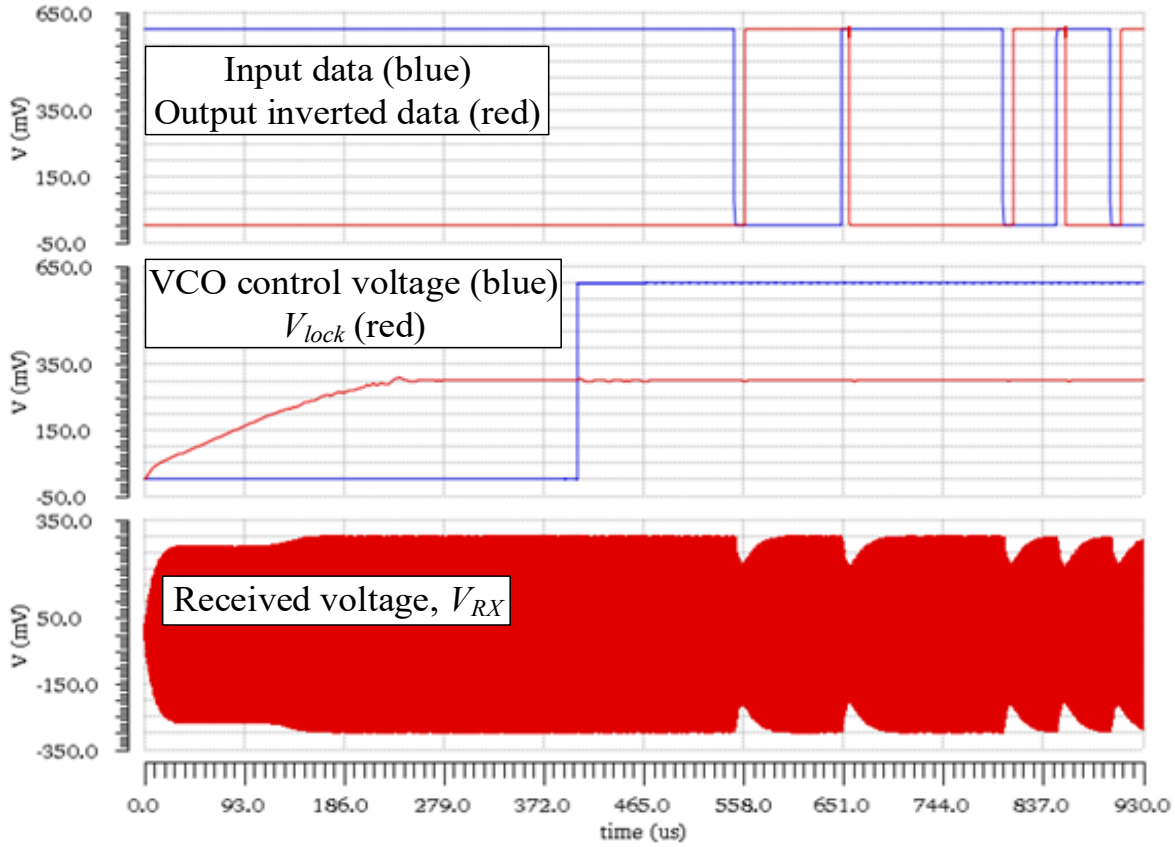


Figure 6.12 Transient simulation of the sub-sampled high-Q QPSK demodulator when the dividing ratio is 16 and the resonant Q-factor is 33.33.

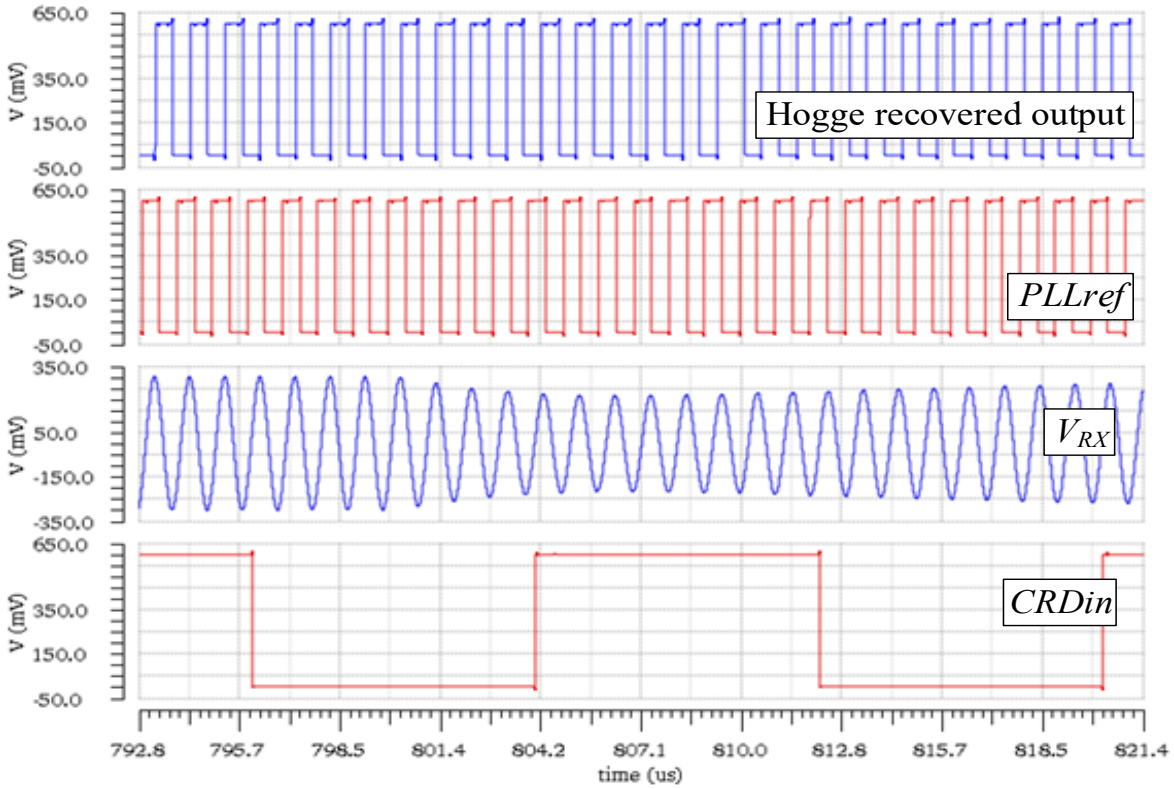


Figure 6.13 Zoomed waveform from the transient simulation of the sub-sampling high-Q QPSK demodulator shown in Figure 6.12

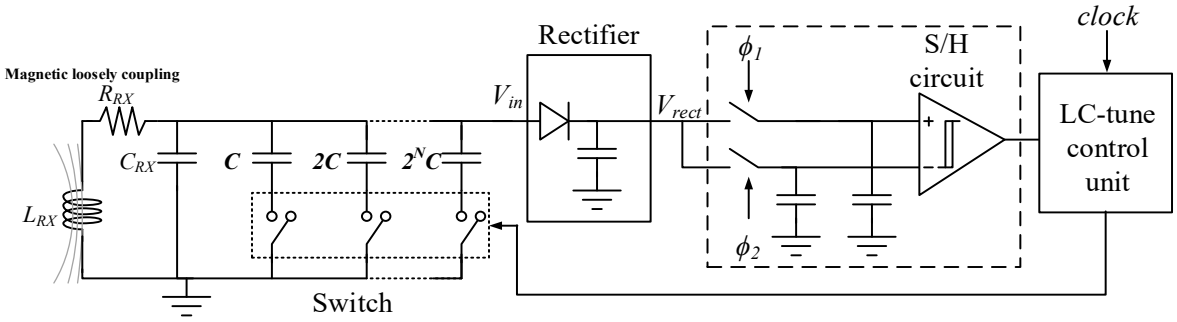


Figure 6.14 LC-tune circuit implemented from the binary weighting capacitor.

6.4 LC-tune

As stated earlier, the resonant frequency of the receiver LC-tank must be matched with the incoming signal in order to maximise the received voltage V_{RX}, hence a binary weighting capacitor system [76-78] is implemented to tune the receiver resonant frequency. Figure 6.14 presents the top-level LC-tune circuit where the sample-and-hold is used to compare the output voltage of the rectifier to detect the optimum output voltage, in a similar way to the segmented rectifier efficiency tracking. An N-bit UP/DOWN counter is used to control the capacitor switches in order to sequentially increase or decrease the capacitance of the LC-tank. Figure 6.15 shows the example of the LC-tuning sequence. When the control unit detects that the output voltage is decreased after

continuously rising, then the counter reverses the direction of the counting for one step (i.e., 0b110 to 0b101) and the evaluation phase is ended. The state machine of the LC-tune control unit can be found in Appendix G.

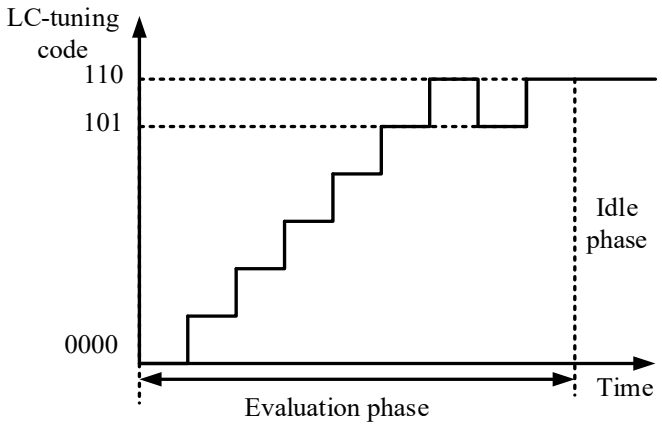


Figure 6.15 Example of an LC-tuning sequence.

The number of capacitors determines the accuracy and the bandwidth of the resonant LC-tuning, hence it is ideally preferable to maximise the N-bit capacitors to the highest possible number. However, the capacitor uses more space if it is on-chip and more pins if it is off-chip. As the operating frequency in this work is in the MF range, a 7-bit binary capacitor is chosen for this design. The unit capacitor C and the maximum resonant frequency capacitance C_{RX} can be calculated from equations (6.3), (6.4) and (6.5). The unit capacitance C must be chosen such that the tuning resolution $d\omega$ is less than the 3dB bandwidth of the high-Q resonant circuit.

$$\omega_{0,\max} = 1/\sqrt{L_{RX}C_{RX}} \qquad (6.3)$$

$$\omega_{0,\min} = 1/\sqrt{L_{RX}\left(C_{RX} + C\sum_{1}^{n} 2^{N}\right)} \qquad (6.4)$$

$$d\omega = \frac{1}{\sqrt{L_{RX}}}\left(\frac{1}{\sqrt{C_{RX}}} - \frac{1}{\sqrt{C_{RX}+C}}\right) \qquad (6.5)$$

The top-level LC-tune circuit is simulated to verify the functionality by applying a 1MHz sinusoidal signal to the LC-tank. The inductance, capacitance and resistance of the LC-tank are 53µH, 350pF and 100mΩ respectively; the values inductance of resistance are defined based on the receiving LC-antenna implementation for the field experiment shown in section 5.1. Furthermore, the unit capacitance of the binary weighting is 10pF. Thus the minimum and maximum tuneable resonant frequency of the LC-tune circuit are 543kHz and 1.17MHz respectively. Moreover the resolution of the frequency tuning is 16.34kHz, as a result, the maximum Q-factor that the circuit can tolerate is approximately 50. As the LC-tank is connected to the rectifier, the Q-factor in this test is varied between 15 and 60 based on the calculation results using equation (2.23) by assuming the rectifier input resistance is between 5kΩ and 20kΩ. Figure 6.16 shows the transient simulation result of the

circuit. The rectifier is started from cold when the resonant frequency of the LC-circuit is approximately 1.17MHz, and the LC-tune control system is enabled between 1.9ms and 3.8ms. It can be seen that the amplitude of the rectifier input voltage V_{RX} and the output rectified DC voltage V_{rect} are increased from 300mV to 450mV and 0.64V to 1.5V respectively. Moreover, the average power consumption of the LC-tune control circuit is 115nW during the evaluation phase. Note that in the practical implementation, the receiving LC-antenna Q-factor can initially be as large as 100 to 150 at cold-start where the rectifier has not drained any input current. Thus, the operating frequency of the energy harvesting system is swept across a certain range (i.e., 500kHz to 2MHz) to ensure that the operating frequency is close to the resonant frequency of the receiving LC-antenna and the received voltage is sufficient for the rectifier to start-up from cold, as explained earlier in section 3.1, Figure 3.2.

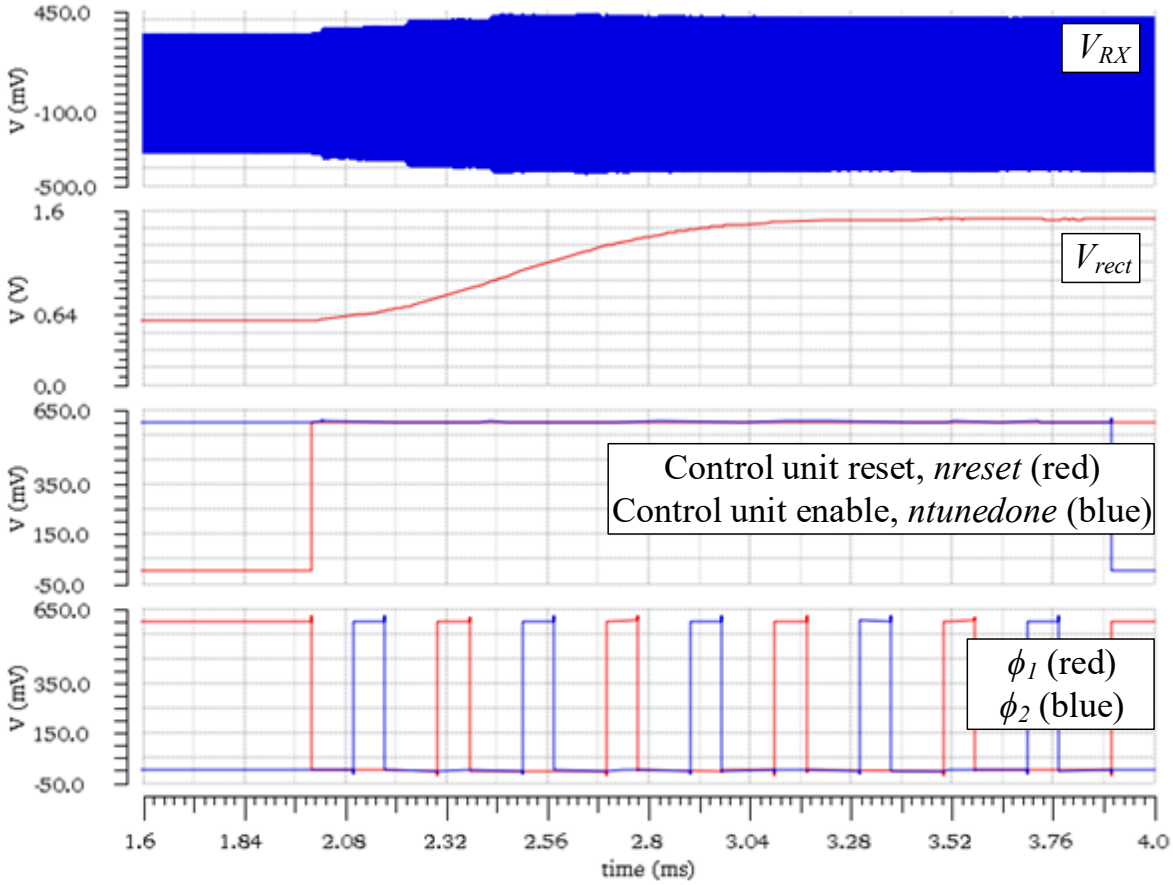


Figure 6.16 Transient simulation of the top-level LC-tune circuit when the input frequency is 1MHz.

6.5 Power Management Unit

The implementation of the PMU is similar to the previous PMU used in Chapter 4, however a digital control unit and a high voltage level detector circuit are added, as depicted in Figure 6.17. The proposed system architecture is comprised of three sub-systems which are the rectifier, the demodulator and the LC-tune; a PMU is designed to control these sub-systems sequentially.

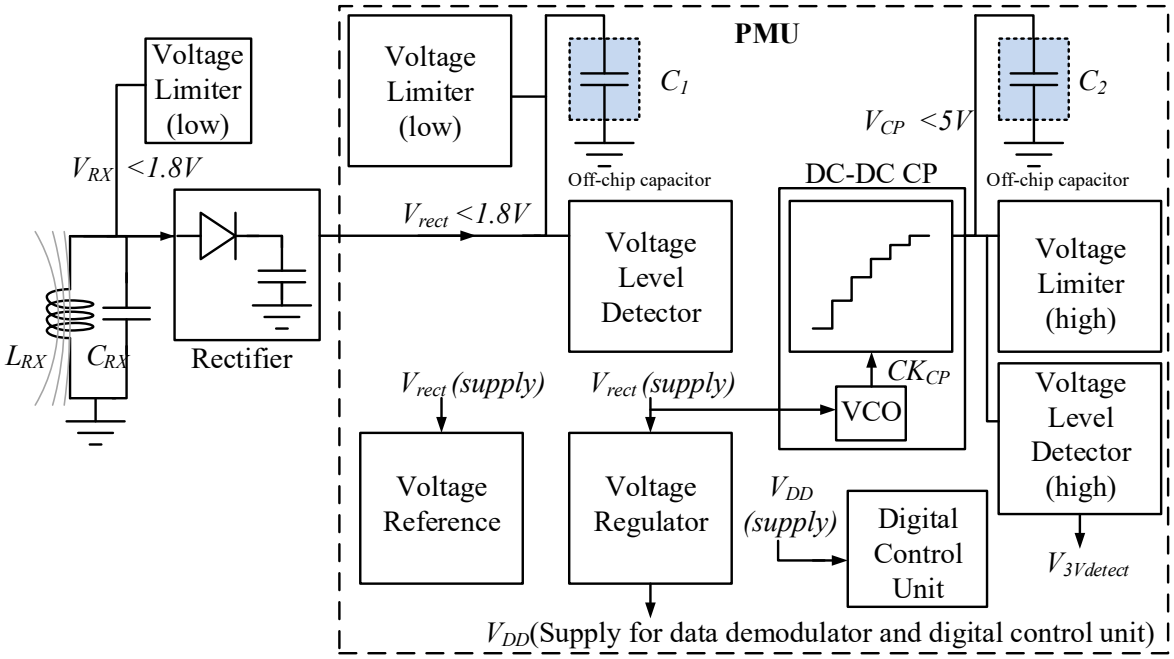


Figure 6.17 System architecture of the PMU.

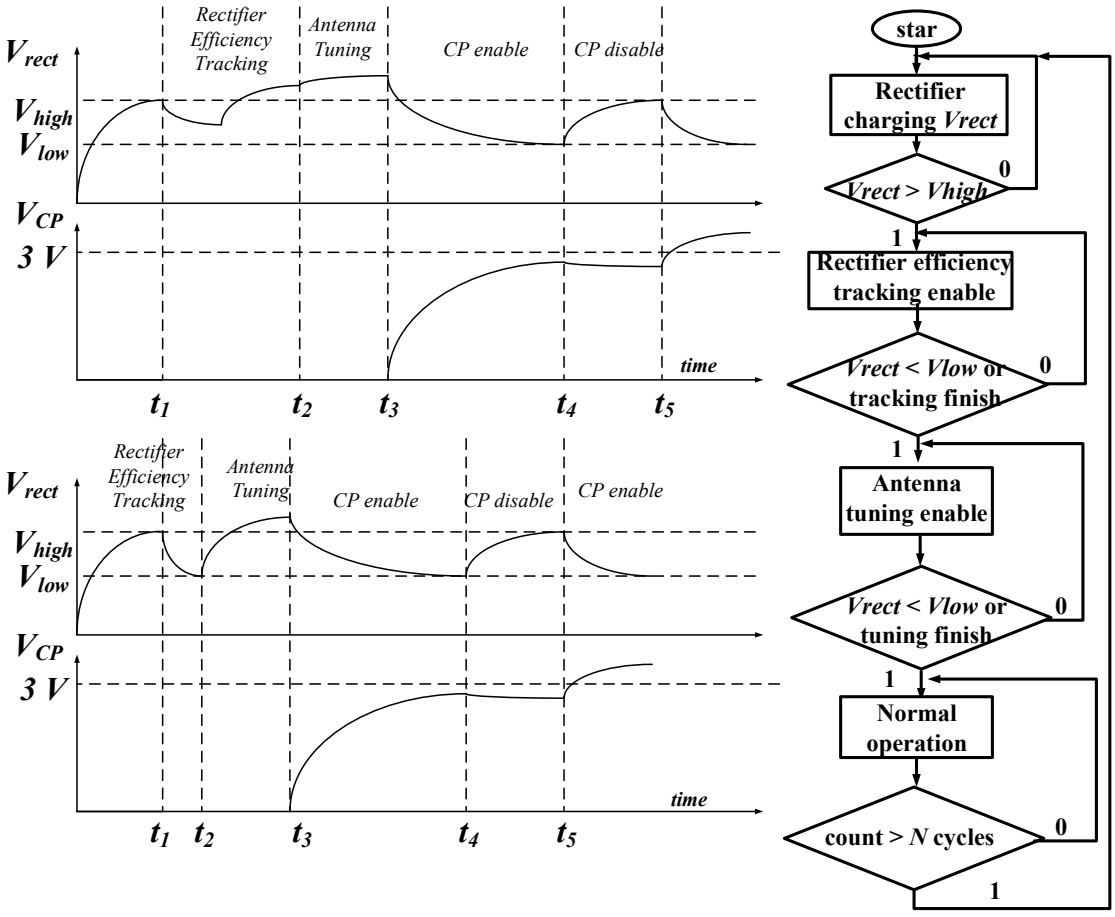


Figure 6.18 Timing diagram and state machine of the PMU.

Figure 6.18 shows the timing diagram and the state machine of the digital control unit of the PMU. The operation is described as follows. Initially, the rectifier is charging an output off-chip storage capacitor/battery C_1 at node V_{rect} from cold-start. When the rectified output voltage reaches V_{high}, the efficiency tracking of the rectifier is enabled at t_1. At t_2, the rectifier control loop enters the idle

phase while the LC-control unit begins the evaluation phase. The LC-tune returns to the idle phase when the operation is finished at t_3, while the data demodulator and the DC-DC CP are enabled. Between t_3 and t_4, the DC converted output V_{CP} is increased which results in decreasing the output rectified voltage V_{rect} since the rectifier loading current is increased. The CP is disabled when the voltage V_{rect} is below V_{low} to enable the rectifier to re-charge the output voltage back to a useable level at t_5.

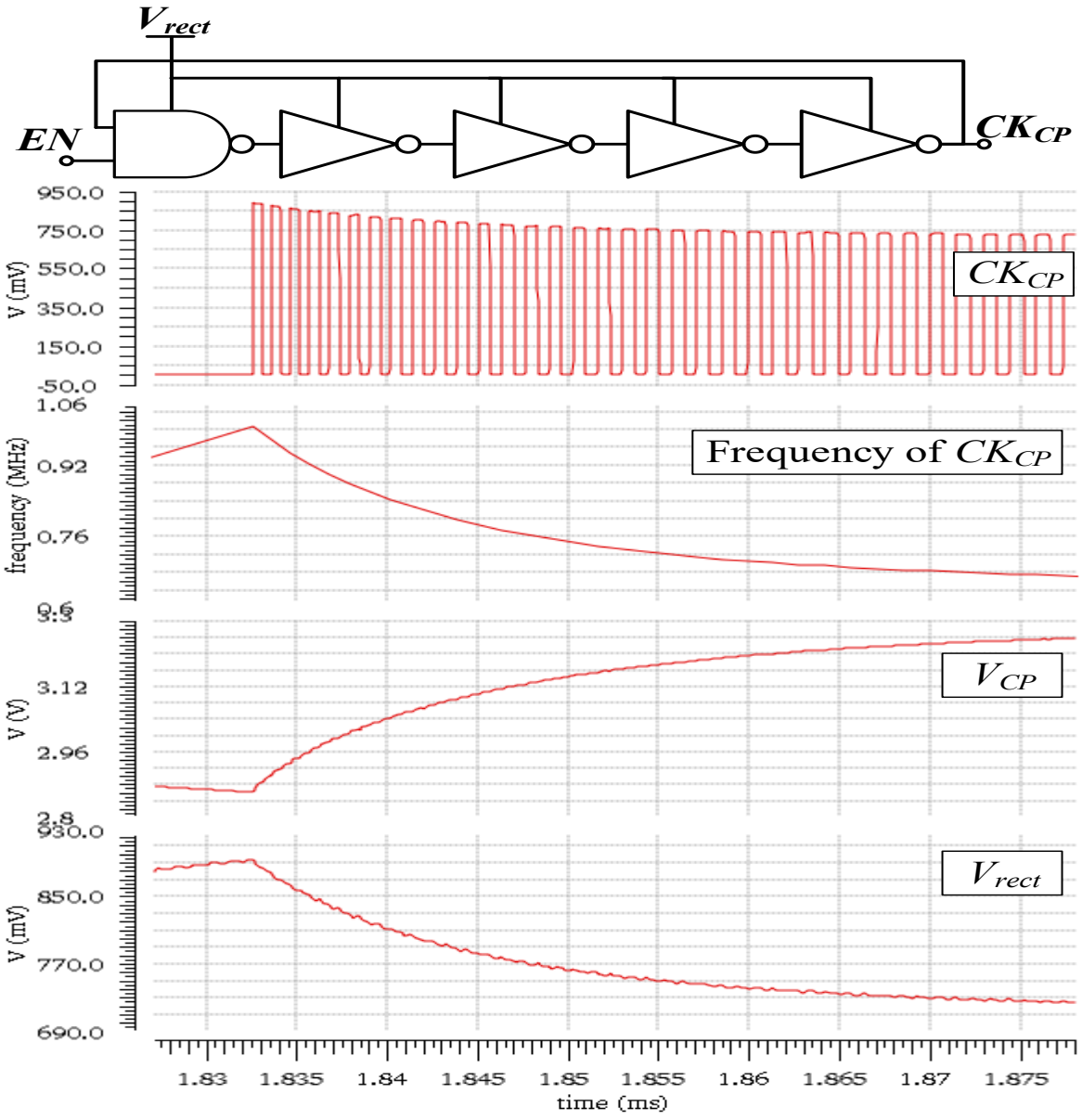


Figure 6.19 VCO for DC-DC CP circuit (top) and the transient simulation results (bottom).

The DC-DC CP used in this chapter is improved by adding a VCO shown in Figure 6.19 implemented from a ring oscillator used as a clock signal for the CP. This is to improve the output voltage performance, as shown in the simulation result when the 1MHz and 250mV$_{pk}$ input rectifier voltage is applied (Figure 6.19). When the rectifier output voltage V_{rect} exceeds V_{high} at t=1.832ms, the CP clock is enabled and the CP output voltage V_{CP} is charged. As V_{rect} is decreased due to the loading current caused by the CP, the frequency of the CP VCO is reduced and hence the power

consumption of the CP is reduced as a result. If the fixed CP clock frequency is used instead similarly to the previous CP shown in Chapter 4, then the fixed clock CP power consumption may prevent V_{CP} from increasing due to the insufficient CP output current/power. In addition, the previous CP output voltage is reduced when the input carrier operating frequency decreases while the CP circuit presented in this chapter is not dependent on the incoming frequency.

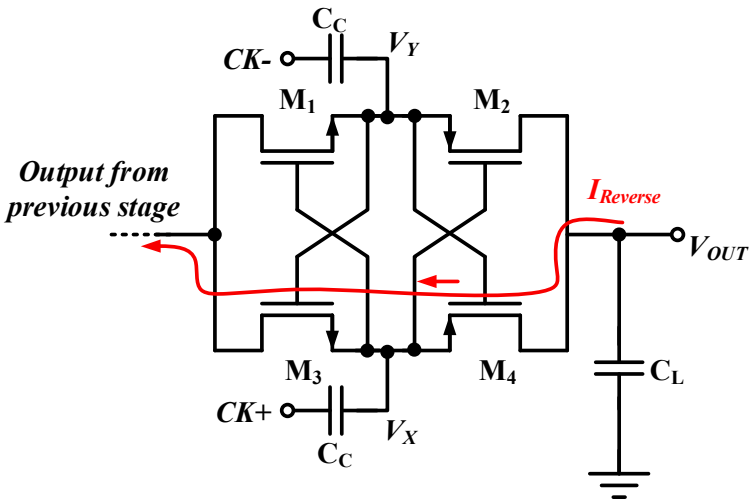


Figure 6.20 Reverse leakage current when CP is disabled.

Since the PMU disables the CP when the supply voltage from the rectifier is below the threshold V_{low}, a reverse current in the CP circuit is likely to occur, as can be seen in Figure 6.20. When the clock signal *CK* is held to disable the CP, the voltage at the gate of the PMOS transistor V_X (or V_Y) is likely to be lower than the CP output voltage V_{OUT} such that the gate-to-source voltage of the PMOS transistor M_4 is larger than the transistor V_{th}. Therefore, the PMOS transistor is still activated and the reverse leakage current is drained from the CP output. The reverse current can be easily avoided by connecting a diode in series with the output storage capacitor, however the output voltage at the storage capacitor is lower than the CP output due to the diode forward voltage. In this project, an off-chip low forward voltage Schottky diode is used to prevent the CP reverse current, which will be shown in the measurement result. Note that the CP reverse leakage current issue is presented exclusively in this chapter because more internal circuits (i.e., LC-tune, efficiency tracking unit, local oscillator, etc.) are used in this receiver IC implementation which leads to greater internal circuits' power consumption. Hence the PMU is likely to disable to the CP of the receiver IC presented in this chapter more often compared with the CP from the previous IC implementation.

Figure 6.21 shows the 3V DC voltage level detector which is used to detect the output voltage level of the DC-DC CP. The voltage V_{CP} is detected by using a switch-capacitor to sample the DC voltage and the voltage dividing capacitor *C1* and *C2* to divide the CP output voltage. The divided voltage V_2 is then compared with a reference voltage (V_{ref}) from a voltage reference circuit using a StrongARM latch comparator, the same as the comparator used in the efficiency tracking control

unit. In addition, the clock signal used for sampling the CP output voltage is generated by the reference clock used in the efficiency tracking control unit. As the circuit only consumes current when the clock signal ϕ_1 is toggled, thus the power consumption from the simulation result is approximately 10nW. Note that this circuit can only be used when a clock signal is available. Hence, the clocked level detection circuit cannot be used as a low voltage level detection since the clock signal is not available at cold-start. Alternatively, a clock signal frequency-divided from the input carrier can be used for the clocked low voltage level detection. However, this method is not suitable for the ultra-low power circuit since the rectifier output voltage is the only available supply voltage for supplying the frequency divider circuit instead of the 600mV regulator voltage (the regulator is enabled by the low voltage level detector). Thus, as a result, the power consumption of the frequency divider circuit is likely to be larger than the previous low voltage level detection shown in section 4.3.3.1.

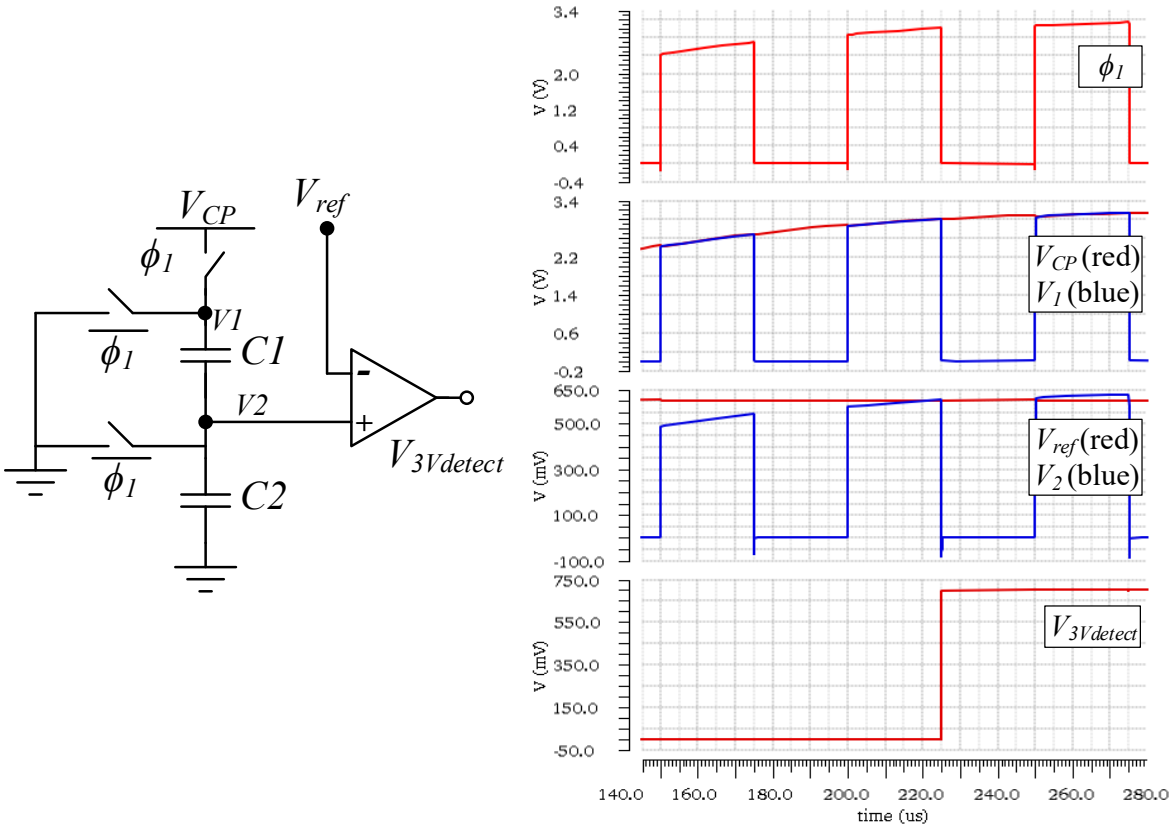


Figure 6.21 3V DC voltage level detector circuit (left) and the transient simulation results (right).

6.6 IC Floor Plan

The building blocks of the wireless energy harvesting receiver have been presented. Each circuit block of the receiver has been simulated separately and summarised in Appendix H.3. Further, the pad ring is designed to connect the internal nodes of the system to the IC pins similarly to the pad ring shown in section 4.4, where the pins placement is arranged to minimise the unwanted parasitic coupling capacitance between the metal traces. Figure 6.22 illustrates the pin diagram of the

receiver IC, and the list of the pins' functionality is shown in Appendix H.4. Figure 6.23 presents the layout of the active area of the chip. The total area of the active area layout is 0.77x1.16mm^2. The die micrograph of the receiver IC is shown in Figure 6.24.

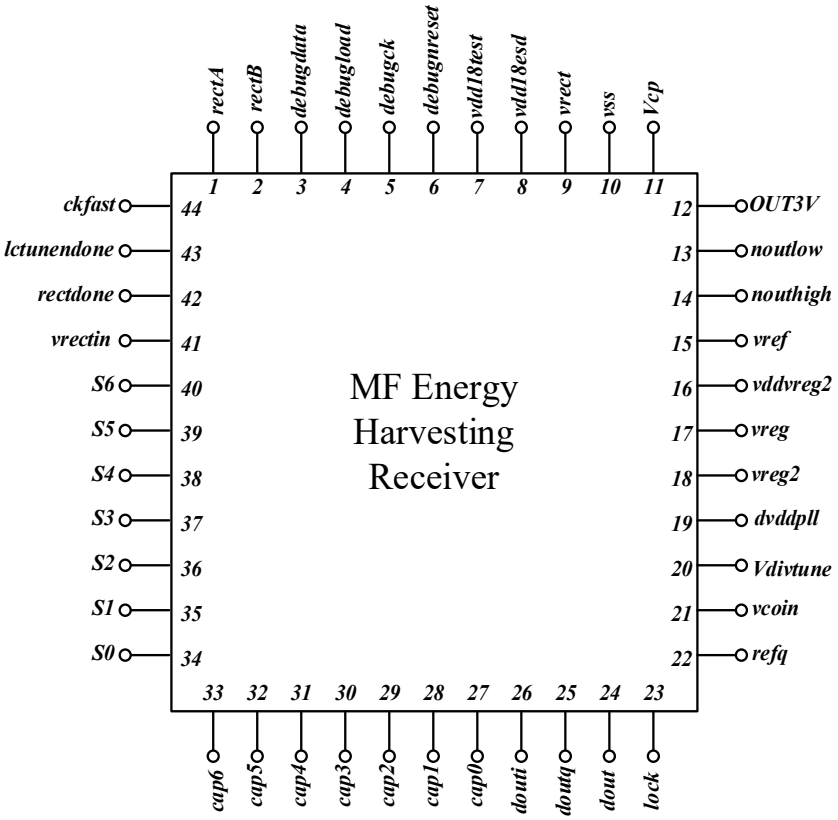


Figure 6.22 Pin diagram of the chip.

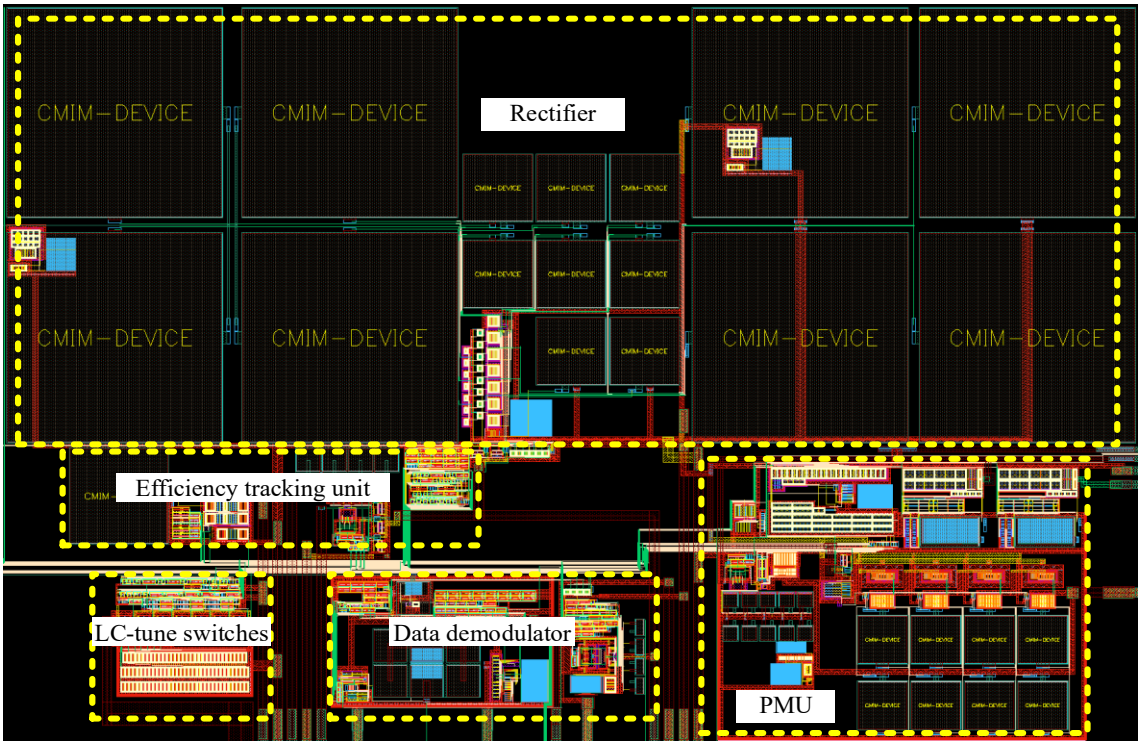


Figure 6.23 Top-level layout. The layout size is 0.77x1.16mm^2.

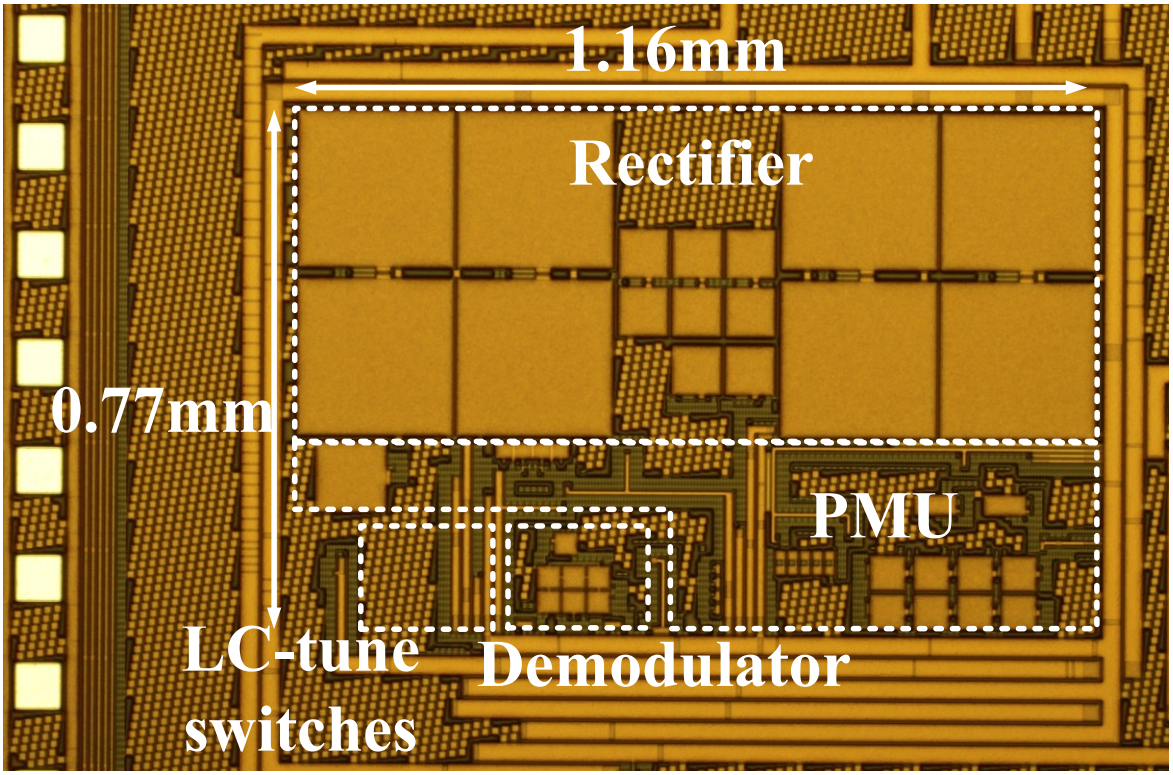
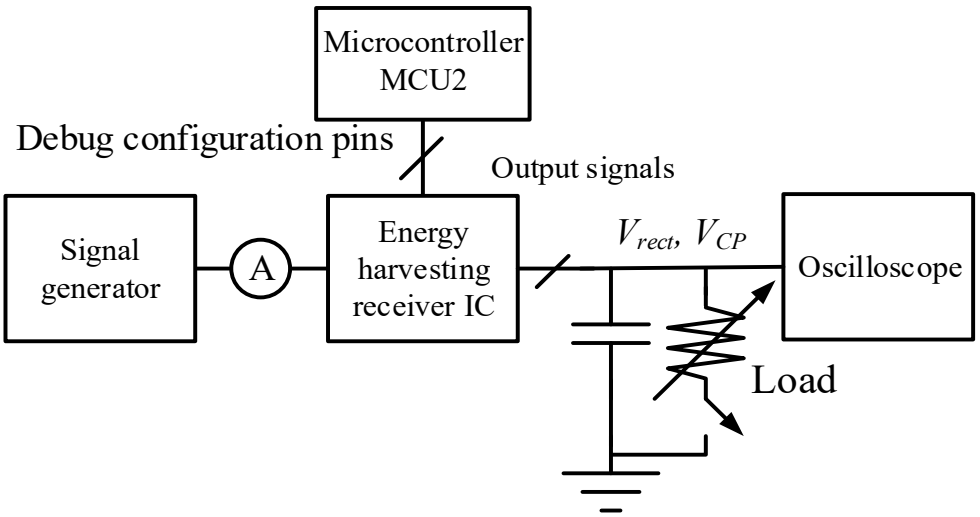


Figure 6.24 Wireless energy harvesting receiver die micrograph.

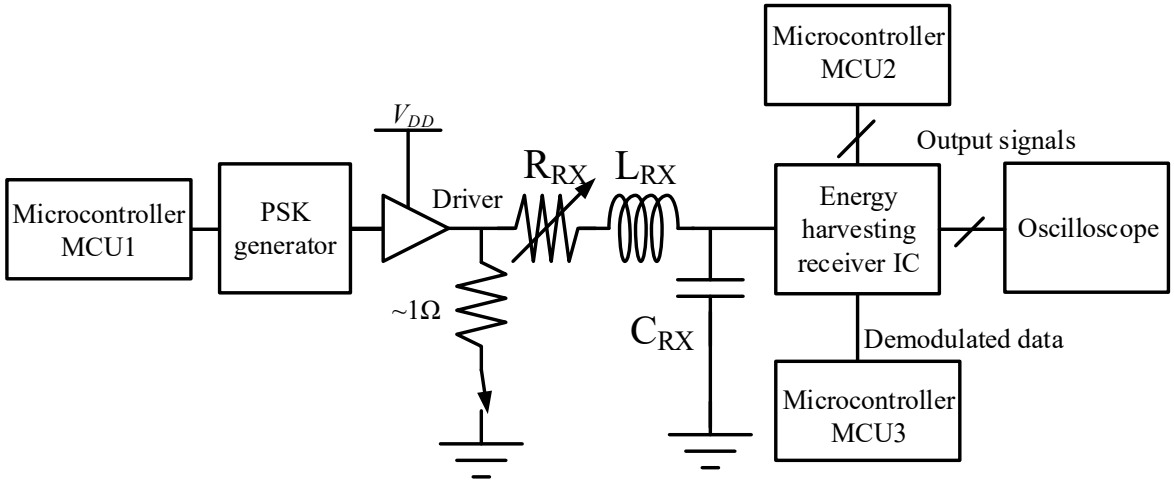
6.7 Measurement Result

6.7.1 Measurement Setup

Figure 6.25 shows the measurement setup for the laboratory measurement of the energy harvesting receiver IC presented in this chapter. For the rectifier and the DC-DC CP measurement setups shown in Figure 6.25(a), selectable loads are connected at the rectifier and CP output nodes for the output voltage measurement and a series resistor is connected between the signal generator and the rectifier input for the rectifier input current measurement similarly to the measurement setup shown in section 5.1. In addition, the microcontroller MCU2 is used to configure the operation of the circuits in the IC, such as selecting the rectifier mode or disabling the LC-tuning control unit. Figure 6.25(b) depicts the QPSK data demodulator and LC-tuning measurement setups where the variable resistors R_{RX} are used to select the Q-factor of the LC-circuit. A 1Ω resistor coupled to ground at the PSK driver output is used to minimise the driver output resistance since the output resistance of the driver circuit can affect the LC-circuit Q-factor. Moreover the microcontroller MCU1 generates pseudo-random data for the QPSK modulation, and the demodulated output data from the IC is compared with the input data to measure the bit-error-rate (BER) of the PSK demodulator by the microcontroller MCU3. Figure 6.26 shows the photo of the wireless energy harvest receiver IC test-board.



(a) Rectifier and DC-DC CP measurement setups



(b) QPSK data demodulator and LC-tuning measurement setups

Figure 6.25 Simplified diagram of the laboratory measurement setup of the energy harvesting receiver IC.

Similarly to the previous field measurement setup shown in Figure 5.1(b), the QPSK signal is amplified by the transmitter antenna driver, which is implemented from the H-bridge class D power amplifier using the TC4431 MOSFET power driver IC that can provide 1.5A maximum output current. In this measurement setup, the 1x1m^2 large loop transmitter antenna is constructed to provide the magnetic field to the ferrite rod receiver antenna, as shown in Figure 6.27. From the figure, it can be seen that the diameter of the receiver antenna is 8mm which is much smaller than the side width of the transmitter antenna. The 1x1m^2 transmitter antenna size in this measurement, which is different from the size of the transmitter antenna shown in the previous measurement in Chapter 5, is chosen to verify that the measurement results are not restricted only in a single case antenna size. Moreover, the magnetic field strength of the transmitter loop antenna has been measured when the transmitter antenna is moved and rotated to ensure that the generated magnetic field is not affected by environments. Table 6.1 shows the parameters of the large loop transmitter

antenna and the ferrite rod receiver antenna. By using the ferrite rod, the effective area of the receiver antenna is increased from $0.05x10^{-3}m^2$ to $10^{-3}m^2$.

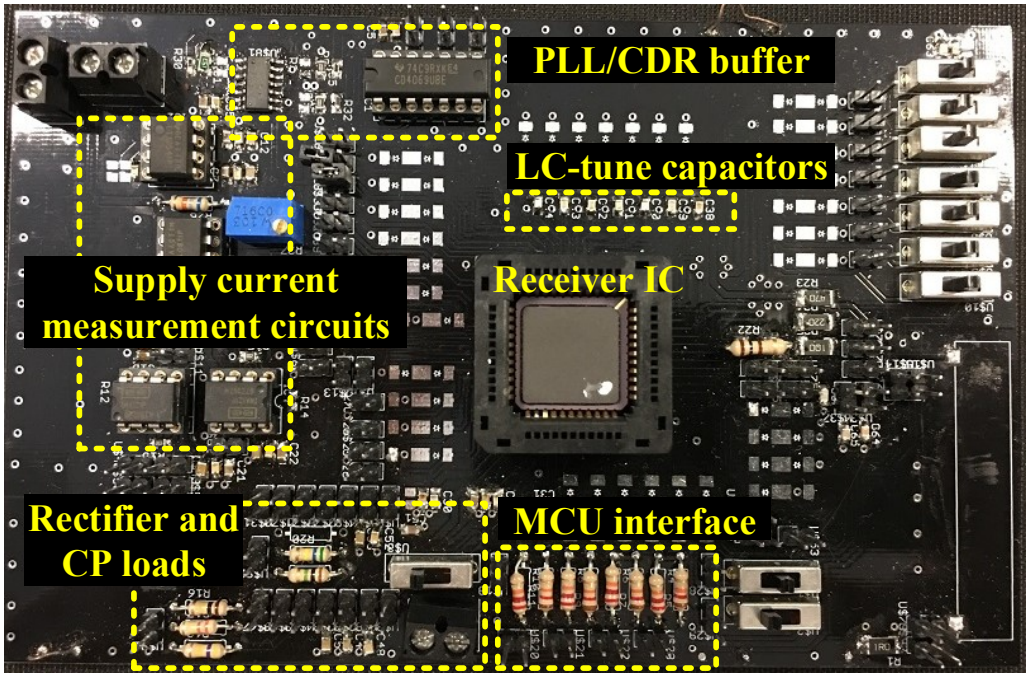


Figure 6.26 Photo of wireless energy harvest receiver IC test-board.

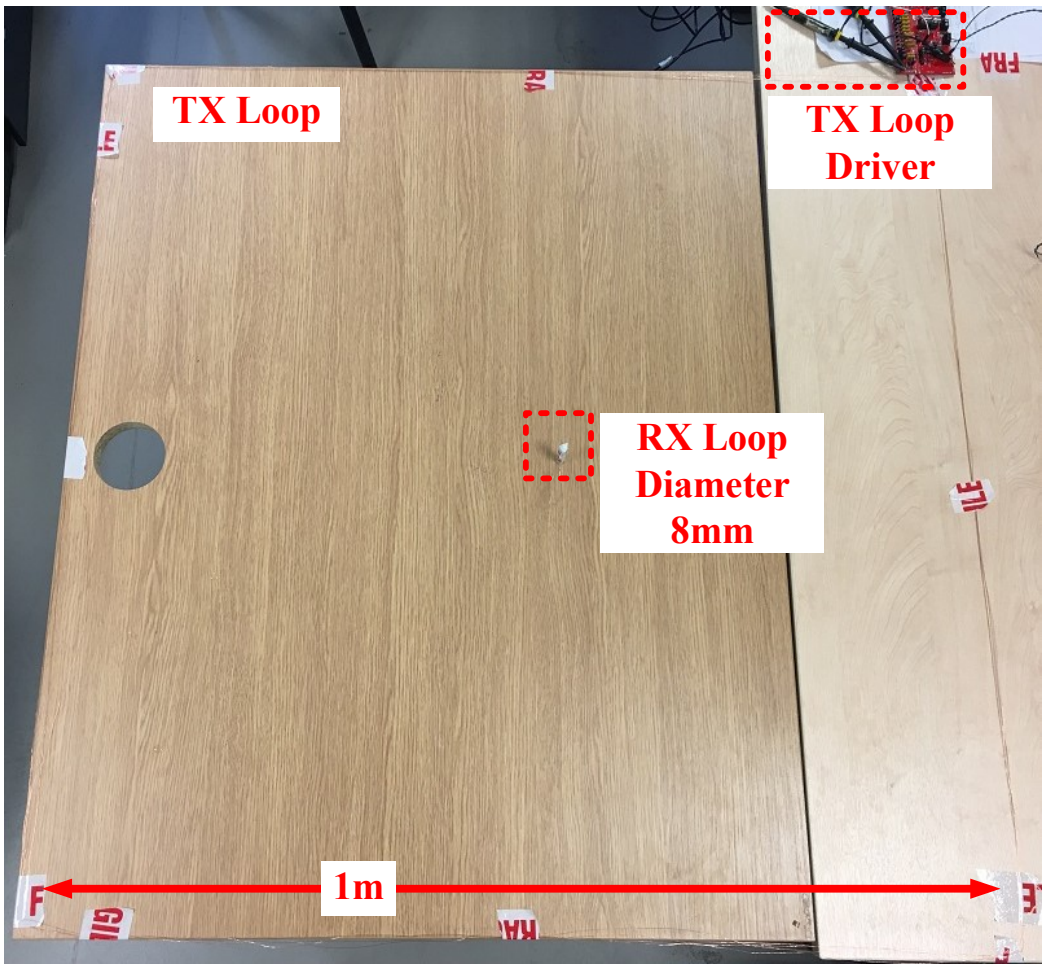


Figure 6.27 Field experiments setup for inductive wireless energy harvesting system measurement.

Table 6.1 Parameters of the large area loop transmitting antenna and the ferrite rod receiving antenna used for the field measurement.

Large loop transmitting antenna		**Ferrite rod receiving antenna**	
Parameters	**Value**	**Parameters**	**Value**
Operating frequency	500kHz	Ferrite rod permeability	18
Width of the square loop	1mx1m	Ferrite rod diameter	8mm
Vertical distance (z-axis) between the TX coil and RX coil	9.5cm	Ferrite rod length	45mm
TX number of turns	4	Ferrite rod effective area	$10^{-3}m^2$
Conductor skin depth	92µm	Radius of the conductor	0.11mm
AC resistance	0.46Ω/m	RX number of turns	24
TX Inductance	115µH	Conductor skin depth	92µm
TX Resonant capacitance	881pF	RX Resistance	0.33Ω
Measured Q-factor	7.7	RX Inductance	29µH
		RX Resonant capacitance	3.5nF
		Measured Q-factor	24

6.7.2 Laboratory Experiment Results

6.7.2.1 Segmented Rectifier Measurement Results

Figure 6.28 presents the output voltage and PCE measurement results of the automatic-mode-configuration segmented rectifier of the receiver IC. The input voltage generated by the signal generator with 1MHz frequency is applied for the rectifier measurement. It can be seen that the minimum rectifier start-up voltage is approximately $200mV_{pk}$ and a 900mV DC output voltage is generated when the rectifier input voltage is $250mV_{pk}$ for the 220kΩ load. Moreover, the PCE of the rectifier peaks at 47% when the load is 220kΩ and maintains above 25% over a wide input range between $250mV_{pk}$ and $700mV_{pk}$ for the 100kΩ load. Note that the decrease of rectifier efficiency when the input voltage exceeds $700mV_{pk}$ is due to the voltage limiter that limits the rectifier output voltage at 1.8V.

Figure 6.29 presents the PCE measurement results of the manual-mode-configuration segmented rectifier of the receiver IC where the efficiency tracking control is disabled. It can be seen that the rectifier efficiency of each mode peaks at different input voltage ranges similarly to the simulation results shown in Figure 6.4.

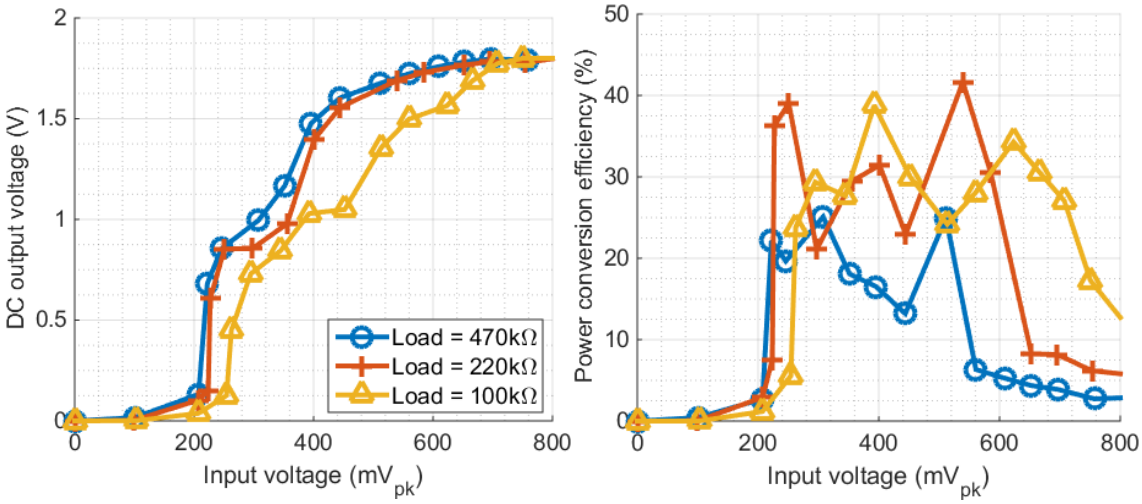


Figure 6.28 IC measurement of the segmented rectifier output voltage (left) and the PCE (right) versus input voltage with different loading resistors when the rectifier efficiency tracking unit is enabled.

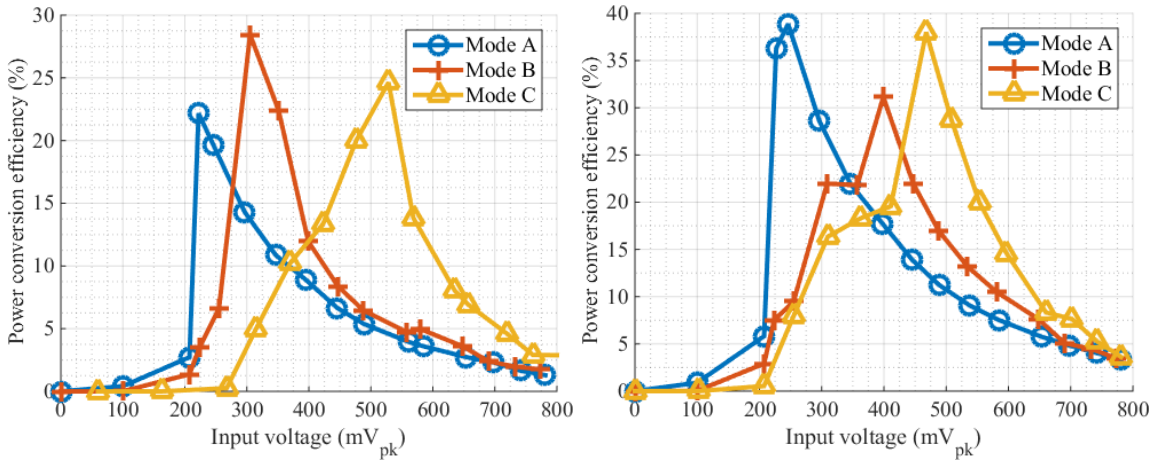


Figure 6.29 IC measurement of the segmented rectifier PCE versus input voltage with the 470kΩ (left) and 220kΩ (right) loading resistors when the rectifier efficiency tracking is disabled.

6.7.2.2 High-Q QPSK Data Demodulator Measurement Results

For the demodulator measurement, pseudo-random data at 1.94kbps, 5.47kbps, 15.6kbps and 26.4kbps data rate generated by the microcontroller MCU1 is QPSK modulated with the 1MHz carrier signal. Figure 6.30 presents the BER measurement results of the high-Q QPSK data demodulator with different LC-antenna Q-factors and sub-sampling dividing ratios. It can be seen that the demodulator can extract the data with the data rate up to 26kbps and the Q-factor up to 25. The BER measurement results show that the BER is improved when the Q-factor is decreased, for example the 10^{-6} BER is achieved when Q is 10 while the BER is $5x10^{-4}$ when Q is 25 at 15.6kbps. Moreover, the BER of the same Q-factor can be reduced when the sub-sampling dividing ratio is increased, for example the $5x10^{-4}$ BER at N=4 is decreased to 10^{-6} when the dividing ratio is increased to N=8. Furthermore, the measured BER is improved when the input voltage of the carrier

signal is increased. This is because the increase of the input voltage leads to the decrease of the LC-antenna Q-factor since more current is drained at the input rectifier circuit which is connected to the LC-antenna. Note that the demodulator BER when N=16 is worse than the BER when N=8. This is because the PLL/CDR control unit is designed for the fixed sub-sampling dividing ratio, hence the control loop internal noise source (i.e., noise from VCO) can cause an error when the dividing ratio is increased. Figure 6.31 shows the simulation result of the QPSK demodulator with different sub-sampling ratios when a noise source is deliberately injected into the control loop. It can be seen that errors occur when the dividing ratio is higher.

Figure 6.32 presents the waveform measurement results of the high-Q QPSK demodulator when the carrier frequency is 1MHz, the data rate is 15.6kbps, the Q-factor is 25 and the sub-sampling dividing ratio is 8. The results show that the demodulator can extract data from the slow QPSK signal when the demodulator is self-powered by the rectifier circuit and the demodulator power consumption is 2.28µW at 630mV supply voltage. Note that an external supply voltage is used in this measurement for the buffer circuits which are used only for experimental purpose.

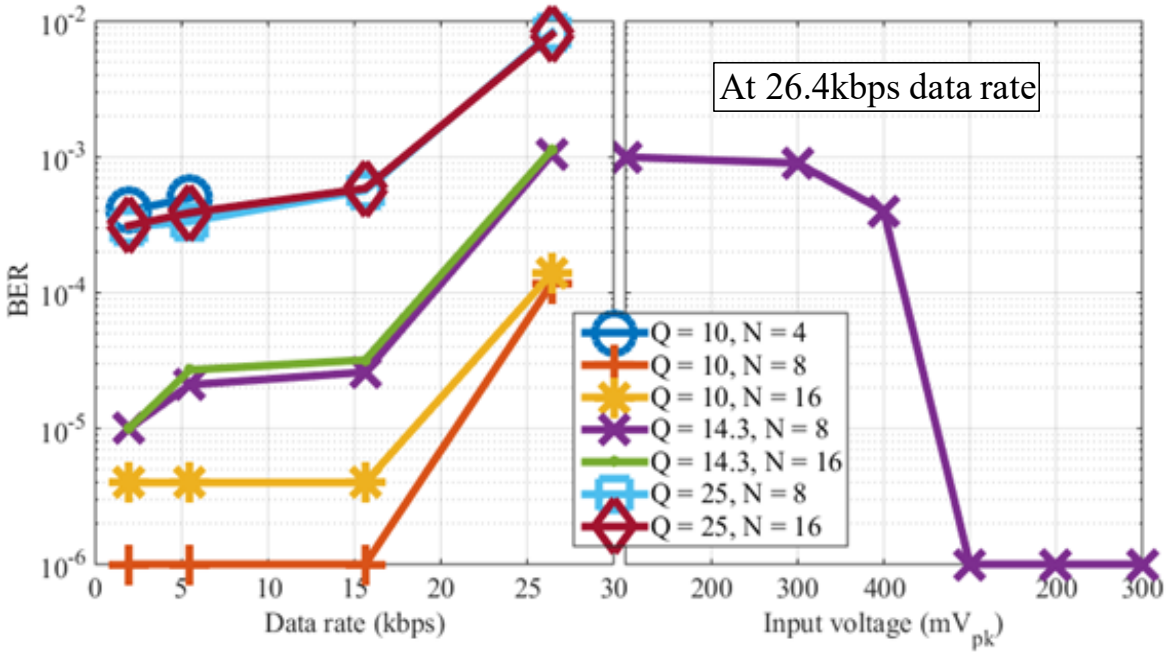


Figure 6.30 BER measurement of the high-Q QPSK data demodulator versus the input data rate (left) and the input voltage of the receiving antenna (right) with different LC-antenna Q-factors and sub-sampling dividing ratios.

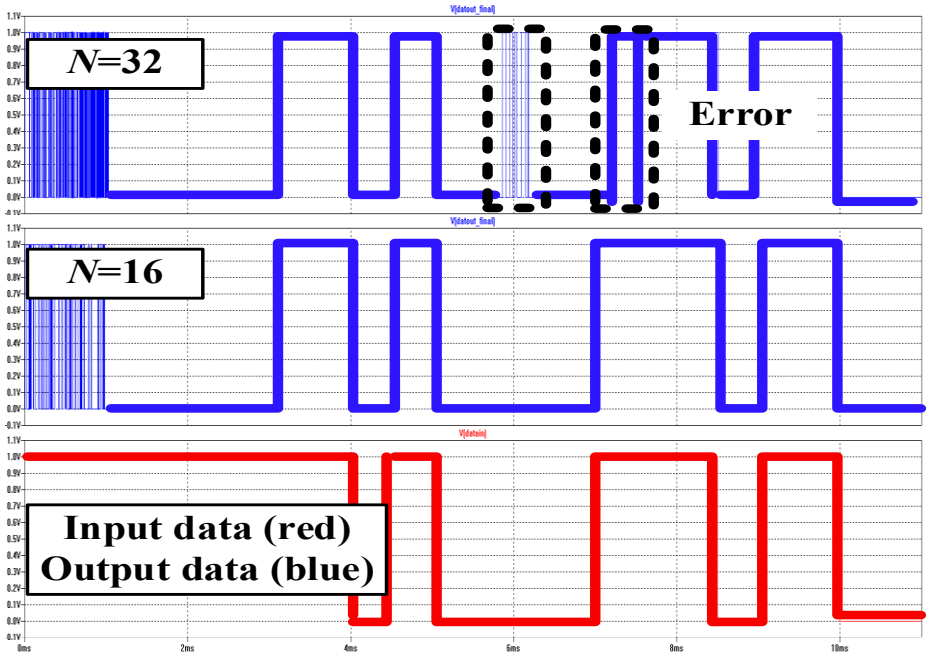


Figure 6.31 Simulation results of the high-Q QPSK data demodulation with two different sub-sampling dividing ratios N_{SS} when the input data rate is 1kbps, the antenna Q-factor is 22 and the VCO input control voltage is injected by a white noise.

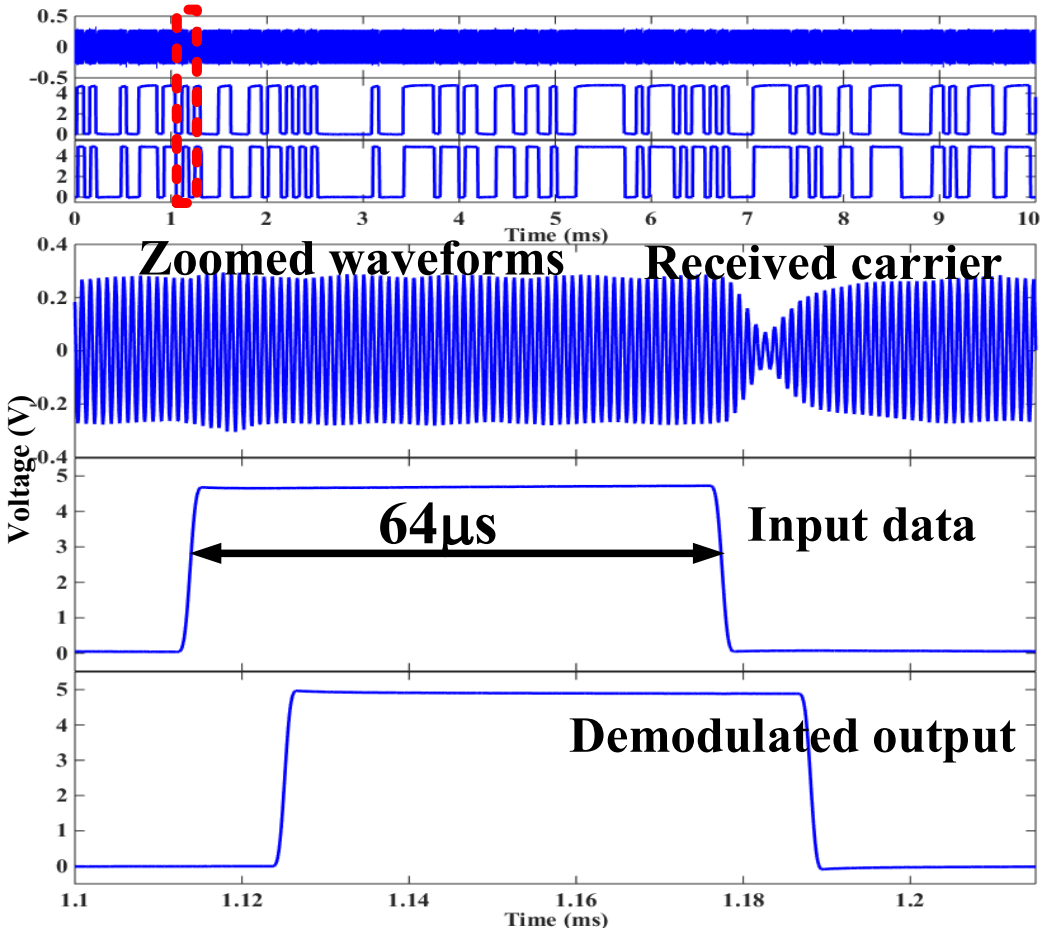


Figure 6.32 Waveform from the measurement of the high-Q QPSK data demodulator when the input frequency is 1MHz, the input data rate is 15.6kbps, the antenna Q-factor is 25 and the sub-sampling dividing ratio is 8.

6.7.2.3 Power Management Unit Measurement Results

As mentioned previously, the reverse current is drained from the DC-DC CP when the circuit is disabled, hence, a low leakage MMDL770T1 Schottky diode with the 0.3V forward voltage and the 9nA reverse leakage current is connected in series with the CP off-chip storage capacitor *C2* to prevent the reverse current. Figure 6.33 illustrates the output waveform of the rectifier and the CP connecting with the diode when the operating frequency is 1MHz and the rectifier output capacitor and CP output capacitor are 57µF. It can be seen that the DC-DC CP can charge a large capacitor 57µF from cold with 220mV$_{pk}$ input voltage.

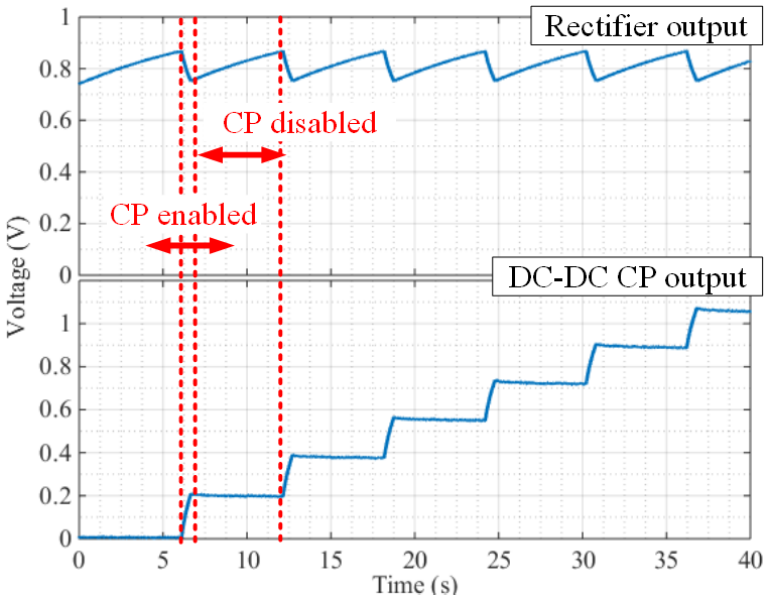
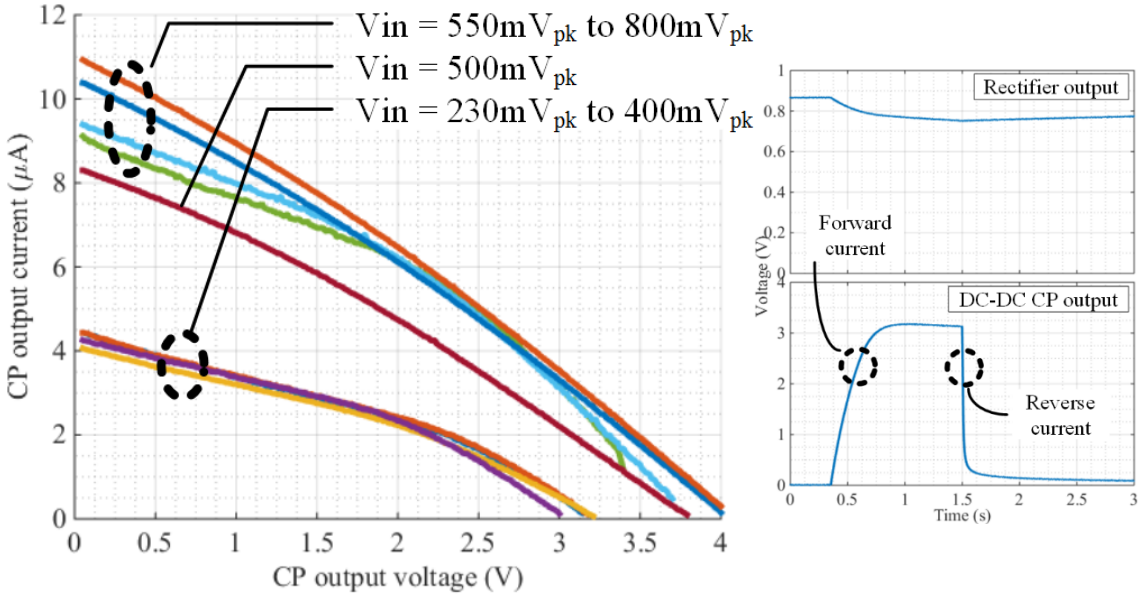


Figure 6.33 Output waveform of the rectifier and the DC-DC CP with the diode from the IC measurement when the input voltage is 220mV$_{pk}$, the operating frequency is 1MHz, the rectifier output capacitor is 57µF and the CP output capacitor is 57µF.

Figure 6.34(a) presents the output current of the CP without the diode versus CP output voltage with different input voltage levels between 230mV$_{pk}$ and 800mV$_{pk}$. The current is derived from the derivative of the CP output voltage waveform shown in Figure 6.34(b) using the equation $I = C\frac{dV}{dt}$. From the output current plot, it can be seen that the CP output can be modelled as a voltage source with an equivalent resistor in series that is approximately at 2MΩ at the input between 230mV$_{pk}$ and 400mV$_{pk}$ and 500kΩ at the input voltage of 800mV$_{pk}$. The output current results can be used to estimate the charging time of the storage capacitor used in practical applications from a simple RC model connecting with a voltage source.

It can be seen from Figure 6.34(b) that the CP output without the diode falls off rapidly, which implies that the reverse current is larger than the CP output current. Figure 6.35(a) depicts the reverse current of the CP during disable when the input voltage is between 230mV$_{pk}$ and 400mV$_{pk}$.

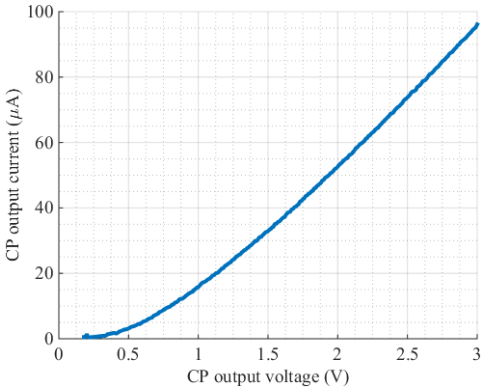
Note that the CP reverse current plots are the same across the input voltage range between 230mV$_{pk}$ and 400mV$_{pk}$, since the reverse current is not dependent on the input voltage. It can be seen from the graph that the reverse current characteristic is the same as a MOS transistor drain current versus gate-to-source voltage characteristic. As explained previously, the reverse current is drained due to the PMOS transistor in the CP being always activated by the bias voltage at V_{GS} when the CP is disabled. The CP output duty cycle at the given input voltage is shown in Figure 6.35(b). Since the CP reverse current is much larger than the forward current, the output of the CP without the diode cannot reach 3V when input voltage is between 230mV$_{pk}$ and 400mV$_{pk}$ since the duty cycle is less than 90%.



(a) (b)

Figure 6.34 (a) Output current of the DC-DC CP without the diode versus CP output voltage with different input voltage levels between 230mV$_{pk}$ and 800mV$_{pk}$ and (b) output waveform of rectifier and CP when the input voltage is 220mVpk, the operating frequency is 1MHz, the rectifier output capacitor is 47µF and the CP output capacitor is 331nF.

From the duty cycle and CP forward voltage, the charging time of the storage capacitor can be estimated. For example, as shown in Appendix D, if the external modules active current is 11mA with 4ms active time then the 440µF storage capacitor is needed to ensure that the supply voltage is maintained above 2.9V when the initial voltage is 3V. At the minimum charging current between 2.9V and 3V is 0.5µA at 230mV$_{pk}$ input voltage, the required charging time is approximately 88 seconds. And from the given duty cycle of 3.5%, the total period required to charge the storage capacitor from 2.9V back to 3V is 42 minutes. Hence, the designer can estimate the receiver idle period from the measurement results. Note that the idle current of the external modules and the leakage current of the storage capacitor/battery must be negligible compared to the charging current.



(a)

$V_{in}(mV_{pk})$	CP Output duty cycle(%)
230	3.49
250	3.52
300	8.26
400	58.31
550	99.24
600	100

(b)

Figure 6.35 (a) Reverse current of the CP during disabled versus CP output voltage when input voltage is between 230mV_{pk} and 400mV_{pk} and (b) the CP output duty cycle versus input voltage.

Figure 6.36 shows the IC measurement of the DC-DC CP output voltage and the charging time of a 10µF storage capacitor. It can be seen that the DC-DC CP start-up voltage with the diode is at 230mV_{pk} input voltage and can provide 3.18V DC output. Since the CP reverse current is much larger than the CP forward current, it can be seen that the CP output without the diode is below 1V when the input voltage is between 230mV_{pk} and 500mV_{pk}. This is because the duty cycle of the CP is below 90% when the input voltage is below 550mV_{pk}. Moreover, the maximum time required for charging an off-chip storage capacitor from cold up to 3V is approximately 2 minutes at 230mV_{pk} input voltage and the charging time less than 10 seconds when the input voltage is greater than 550mV_{pk}.

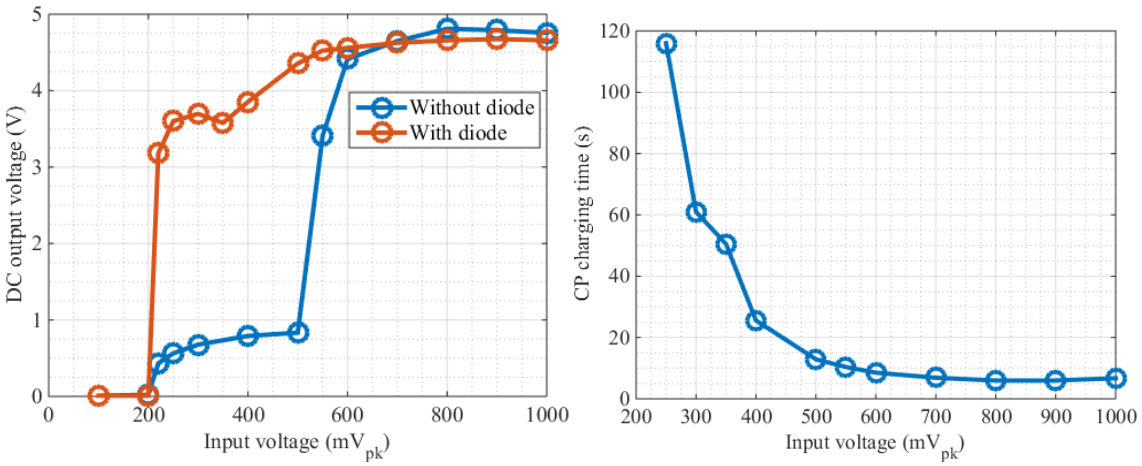


Figure 6.36 IC measurement of the DC-DC CP output voltage (left) and DC-DC CP charging time of 10µF capacitor (right) versus input voltage.

Figure 6.37 presents the waveform measurement of the magnetic loosely coupled wireless energy harvesting receiver IC when the input frequency is 1MHz. It can be seen that the rectifier can start-up from cold to charge the off-chip capacitor, and the rectifier efficiency tracking control unit is enabled when the output rectifier voltage V_{rect} reaches the minimum threshold at t=60ms. After the

rectifier is configured to mode B where SWA is low and SWB is high at t=120ms, the LC-tuning efficiency control is enabled sequentially. The results show that the input voltage at the antenna (V_{RX}) is increasing during the time period between t=120ms and t=250ms when the LC-tuning control is enabled. The LC-antenna resonant frequency is tuned from 1.57MHz to 1MHz. Note that if the Q-factor is high, such that the incoming frequency is out of the band of the LC-antenna resonant frequency, then the receiver IC cannot start to operate from cold. Hence the input frequency sweeping protocol is needed, as explained in section 3.1. Moreover, the DC-DC converter and the data demodulator are enabled after the efficiency control unit enters idle mode as can be seen from the indication signals $rectDONE$ and $\overline{lcDONE}$ at t=250ms.

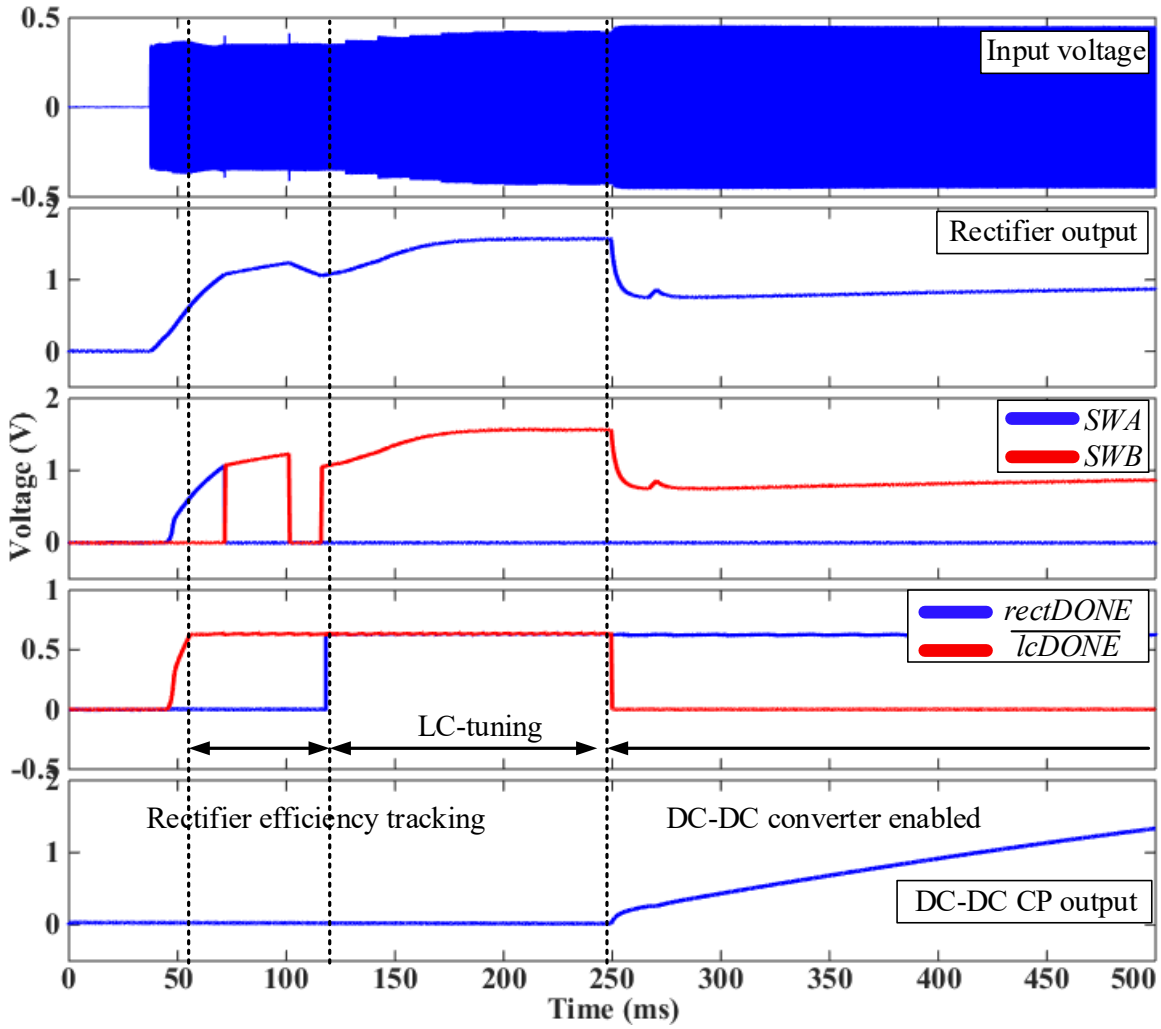


Figure 6.37 IC measurement of the energy harvesting receiver IC when the input frequency is 1MHz. Signals SWA and SWB indicate the rectifier configuration mode while signals $rectDONE$ and $\overline{lcDONE}$ are the enable signals of the efficiency control unit.

6.7.3 Field Experiment Results

As shown in section 6.7.1, the 1x1m^2 large loop antenna provides a stable magnetic field which is modulated with the QPSK data. The output QPSK data from the receiver IC is measured to verify

that the data demodulator can demodulate the QPSK signal from the magnetic field source. Moreover, the rectifier output voltage and the CP output voltage of the IC are measured to verify that the receiver IC can harvest energy from the magnetic field provided by the transmitter antenna.

Figure 6.38 shows the high-Q QPSK data demodulator measurement waveform of the receiver IC at input data rate of 26.4kbps; the Q-factors of the transmitter and receiver antennae are 7.7 and 24 respectively and the demodulator sub-sampling dividing ratio is 8. It can be seen that the QPSK data can be demodulated. Moreover, the receiver IC can provide the 0.85V rectifier output voltage and 3.5V CP output voltage at 704mV$_{pk}$ input to supply the receiver circuits.

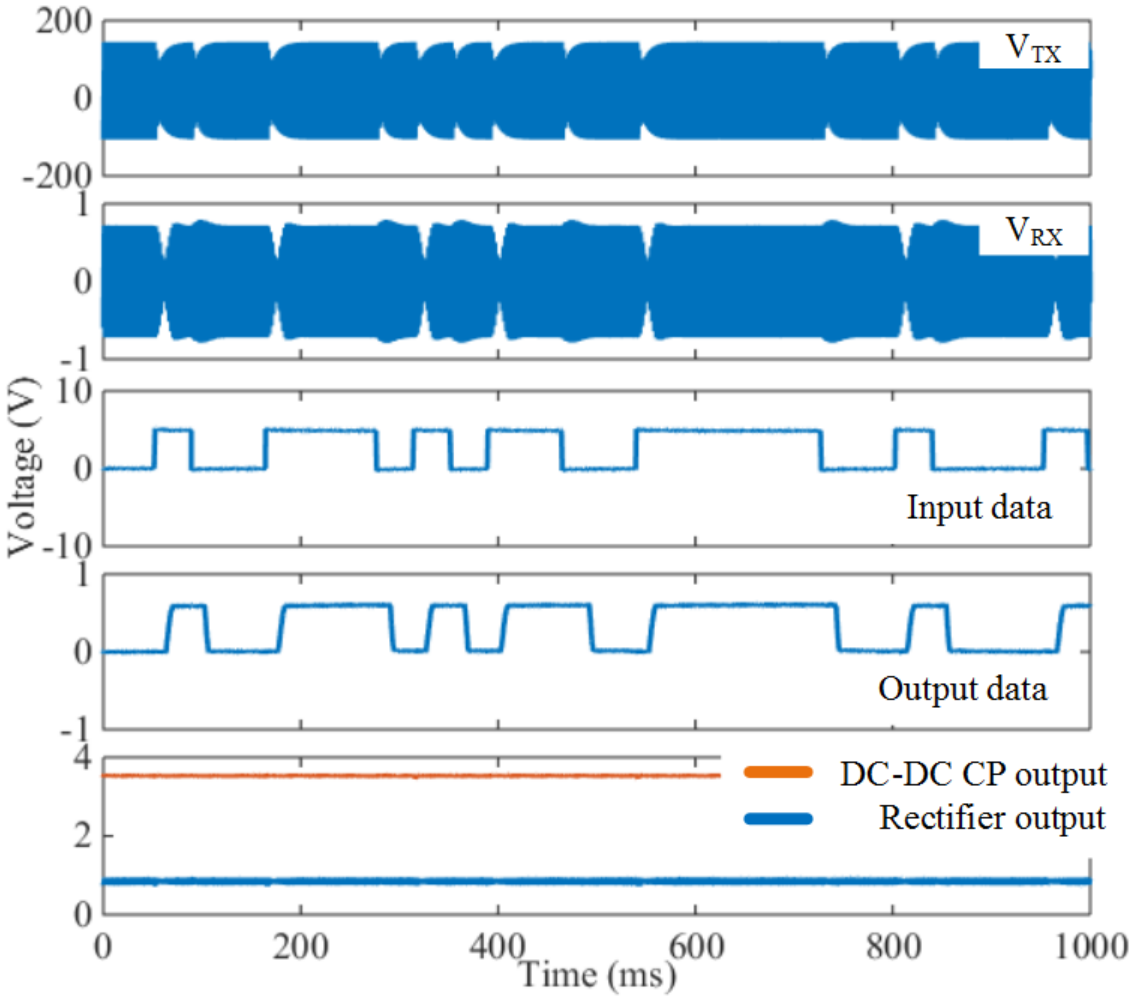


Figure 6.38 Waveform from the field measurement of the high-Q QPSK data demodulator when the input frequency is 500kHz, the input data rate is 26.4kbps, the TX antenna Q-factor is 7.7, the RX antenna Q-factor is 24 and the sub-sampling dividing ratio is 8.

Figure 6.39 presents the field measurement of the received voltage at the antenna V_{RX}, the rectifier output voltage V_{rect} and the DC-DC CP output voltage V_{CP} versus the magnetic field strength generated by the 1x1m^2 transmitter large loop antenna. The transmitter magnetic field strength is derived from the transmitter current using equation (2.11) shown in section 2.2.2.1. From the

received voltage V_{RX} measurement plot when the receiver antenna is unloaded and loaded by the receiver IC, it can be seen that V_{RX} is linearly proportional to the magnetic field strength when the receiver coil is unloaded as expected and saturated at $0.8V_{pk}$ when the receiver coil is loaded by the IC. This is because the loading current at the receiver antenna, which is drained by the rectifier and the DC-DC CP, is increased when V_{RX} increases. In consequence, the loading current limits the receiver Q-factor and the received voltage V_{RX}. Furthermore, it can be seen that the loaded received voltage V_{RX} when the magnetic field strength is below 0.2A/m is slightly larger than the unloaded V_{RX}. This is because the LC-tune of the receiver IC tunes the receiver LC resonant frequency to match the incoming frequency. In addition, the rectifier and DC-DC CP output voltage measurement results show that the receiver IC can harvest the magnetic energy from the stable magnetic field between 0.1A/m and 0.6A/m to provide 1V rectifier output and 4.25V CP output.

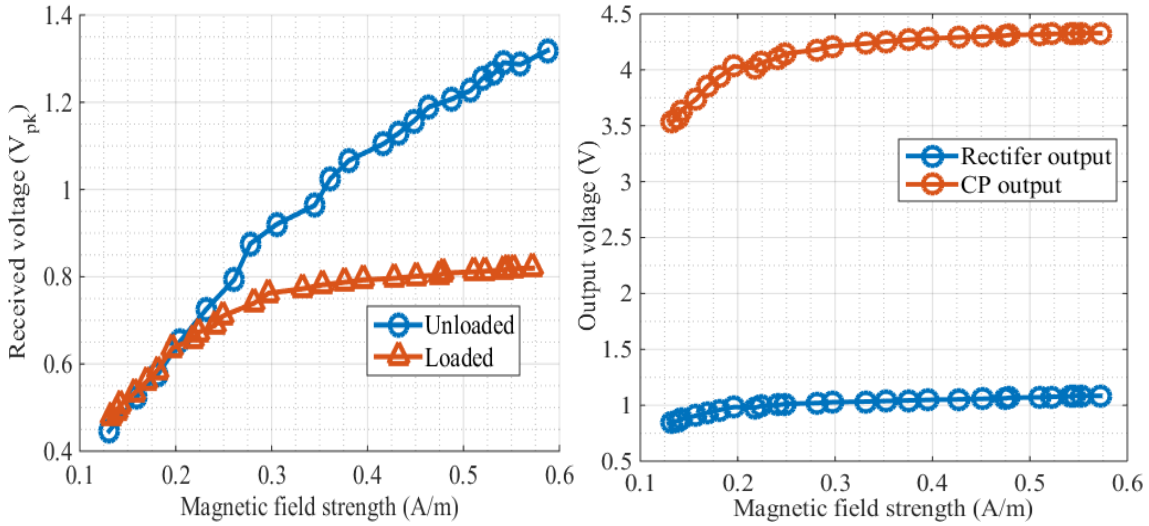


Figure 6.39 Field measurement of the received voltage at the antenna V_{RX} (left) and the harvested output voltage from the rectifier and the DC-DC CP (right).

From the field measurement results, the minimum transmitter current required to start up the receiver IC can be determined by comparison with the calculation results using equations shown in section 2.2. Figure 6.40 shows the magnetic field strength of a single-turn square loop antenna (N_{TX} = 1) at the centre of the $1x1m^2$ square loop antenna (x = 0m, y = 0m, and z = 9.5cm) versus the side width of the square loop ($2W$) when the transmitter current is 100mA. Since the receiver IC requires $250mV_{pk}$ minimum received voltage to provide the 3V output for external modules, the required minimum magnetic field is 0.07A/m. In comparison with the plot from Figure 6.40, the magnetic field strength of the $10x10m^2$ is 0.018A/m when the transmitter current is 100mA and can be increased to 0.07A/m when the transmitter current is 388mA (calculated from equation (2.11)). Hence, the minimum transmitter current required to start up the receiver IC is listed in Table 6.2. Furthermore, the required transmitter current can be reduced by increasing the number of turns of the transmitter loop antenna N_{TX}.

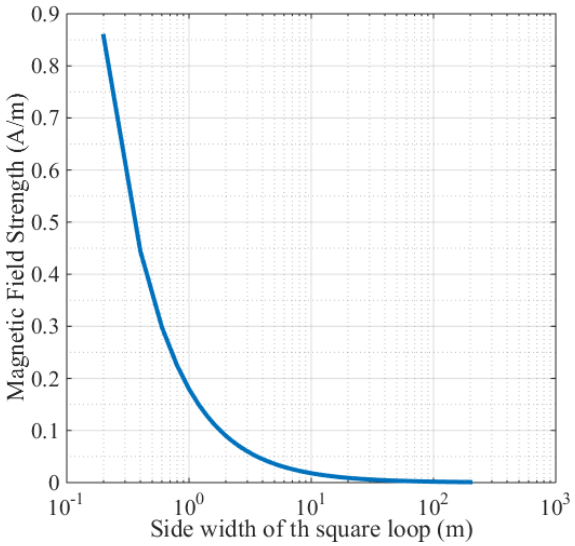


Figure 6.40 Magnetic field strength of the single-turn (N_{TX}=1) square loop antenna with the 100mA transmitter current versus side width of the square loop (*2W*).

Table 6.2 Required minimum transmitter current to start up the receiver.

Side width of the square loop	Magnetic field strength (A/H) at 100mA TX current	Required minimum transmitter current			
		At N_{TX}=1	At N_{TX}=2	At N_{TX}=3	At N_{TX}=4
1m	0.18	39mA	19mA	13mA	9.7mA
10m	0.018	390mA	190mA	130mA	97mA
100m	0.0018	3.9A	1.9A	1.3A	97mA
200m	0.0009	7.8A	3.9A	2.6A	1.9A

The required transmitter current can be reduced by the transmitter loop number of turns N_{TX}, however, the inductance of the square loop antenna is increased by a factor of N_{TX}^2 which leads to the reduction of the resonance capacitance. Table 6.3 shows the required resonance capacitor at the given large loop size and number of turns. It can be seen that the required transmitter current can be reduced to 97mA for the 100x100m^2 transmitter loop antenna if the number of turns is 4, however the resonance capacitor at 500kHz operating frequency is reduced to 2.6pF, which can be smaller than the parasitic capacitor from the transmitter driver or the circuit board. Hence, the designer may need to choose a fewer number of turns of the loop antenna and a lower operating frequency to ensure that the required resonance capacitor is larger than the parasitic capacitor.

Table 6.3 Transmitter square loop antenna parameters.

Number of turns	Side width of the square loop	Square loop inductance	Resonance capacitance at 500kHz operating frequency	Resonance capacitance at 1MHz operating frequency
1	1m	7.2µH	14.1nF	3.52nF
	10m	90µH	1.13nF	281pF
	100m	1.1mH	93pF	23pF
	200m	2.3mH	44pF	11pF
2	1m	29µH	3.5nF	880pF
	10m	360µH	281pF	70pF
	100m	4.4mH	23pF	5.8pF
	200m	9.2mH	11pF	2.7pF
3	1m	65µH	1.6nH	391pF
	10m	810µH	125pF	31pF
	100m	9.8mH	10pF	2.6pF
	200m	21mH	4.9pF	1.2pF
4	1m	65µH	1.6nF	391pF
	10m	3.2mH	31pF	7.8pF
	100m	39mH	2.6pF	0.65pF
	200m	83mH	1.2pF	0.3pF

Note that the required transmitter current is derived from the measurement results when the ferrite rod antenna with the number of turns of 24 is used as a receiver antenna, as shown in the parameters listed in Table 6.1. The required transmitter current can be further reduced by improving the receiver, such as by increasing the size of the ferrite rod or reducing the rectifier and DC-DC CP start-up voltages.

In addition, the magnetic field is measured when the ferrite rod receiver antenna is perfectly aligned with the transmitter loop antenna. The angular misalignment between the transmitter and receiver coils can reduce the received voltage V_{RX}. In practical applications, the designer may use

three receiver antennas with different orientations (e.g., 60° coil angle different between each coil) for magnetic field energy harvesting to minimise the effect of the misalignment of the antenna coils.

Table 6.4 compares the power density of the existing energy harvesting methods summarised by [2] with the power density of the proposed MF magnetic loosely coupled wireless energy harvesting system from the measurement results shown in this section where the parameters used for the measurement are as listed in Table 6.1. It can be seen the magnetic coupling wireless energy harvesting method can provide more power density than the radio frequency energy harvesting method. Although the energy harvesting sources from the ambient light, thermoelectric and vibrational microgenerators can provide more power density than the proposed method, such methods are dependent on the environment and may require an additional power hungry receiver module to enable the system synchronisation. In addition, the power density of the proposed system can be increased by increasing the transmitter current or the transmitter loop antenna number of turns, as mentioned earlier. Note that the power density from the proposed system shown in the table is not the total harvested energy since the power consumption from the subsystems is not taken into account.

Table 6.4 Comparison of energy harvesting method from [2] with the proposed MF magnetic loosely coupled energy harvesting system.

Energy Source	**Power Density**
Ambient light	100mW/cm^2 (directed toward bright sun) 100µW/cm^2 (illuminated office)
Thermoelectric	60µW/cm^2
Vibrational microgenerators	4µW/cm^3 (human motion-Hz) 800µW/cm^3 (machines-kHz)
Ambient radio frequency from cellular base station	< 1µW/cm^2 (VHF and UHF band)
Proposed system*	38µW/cm^2 (at 0.5 A/m magnetic field strength)

*Parameters (i.e., TX loop size, current) from the specifications shown in Table 6.1.

6.8 Summary

The second prototype receiver IC for the magnetic loosely coupled energy harvesting system is further developed and verified in this chapter to solve the remaining issues from chapter 5. The proposed segmented rectifier incorporated with the efficiency tracking control unit is designed to provide an output DC voltage with high efficiency over the wide input voltage range. In addition, the efficiency control unit is also used for tuning the resonant frequency of the receiver antenna LC circuit to match the incoming frequency. As a result, the harvested energy of the receiver IC is automatically optimised by the control unit. Moreover, the proposed high-Q QPSK data demodulator can extract data from the carrier with the slow phase transition due to high-Q LC resonant circuit. The laboratory measurement results of the QPSK demodulator show that the moderate BER data extraction is achieved at high-Q with ultra-low power consumption. Furthermore, the field experiment of the MF magnetic coupled energy harvesting system has been presented. The receiver IC can demodulate the QPSK data under the field experiment setup. In addition, the laboratory and field experiment results show that the energy harvesting performance of the second prototype receiver IC has been improved and can be used for self-powered wireless sensor network applications.

Chapter 7: CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

This thesis has presented the design and implementation of a magnetic loosely coupled energy harvesting receiver for wireless sensor network applications starting from the system requirements, the system level development, the analogue IC architecture design and the IC verification.

In wireless sensor network applications, the magnetic loosely coupled energy harvesting method allows multiple receiver nodes to be wirelessly self-powered from the magnetic field energy harvesting source. As a result, the need for the battery replacement of each receiver node is avoided. The magnetic field energy harvesting source is independent to its environments while the available energy from other existing harvesting sources, such as a light source, is varied depending on its environments. A medium frequency operation is suitable for the magnetic energy harvesting system used for the wireless sensor network applications. This is because the harvested energy operating at the medium frequency does not suffer from losses due to a long-distance operation (path loss) and the parasitic losses that are visible at higher frequencies. Moreover, since the size of an antenna is proportional to the wavelength of the operating signal (to achieve the optimum results), hence the size of the transmitter antenna for the medium frequency operation can be much larger than the transmitter antenna size for the high frequency operation. Note that the receiver antenna size can be much smaller than the transmitter antenna size since a ferrite rod antenna is used to increase the effective area to maximise the received magnetic flux generated from the source. In addition, the magnetic energy source can also be modulated with data to enable the system synchronisation between the source and several receivers, removing the need for an accurate power-hungry real-time clock. By allowing the transmitter to communicate to the receiver node using the modulation scheme, an active/sleep command signal can also be transmitted along with the timing information to the receiver which leads to the reduction of the receiver's average power consumption.

The transmitted magnetic field can be amplified by increasing the transmitter current and the number of turns of the transmitter loop. However, the transmitter loop inductance is increased by a factor of the square of the number of turns which leads to the requirement of a very low resonant capacitor, such that the capacitor might be unavailable in practice. At the receiver side, a ferrite rod antenna is more preferable as a receiver antenna than a circular loop antenna due to the improvement of the effective area from the ferrite material. Both transmitter and receiver

antennas rely on using a high-Q resonant circuit to improve the transmitter current and the received voltage, hence a resonant frequency tuning circuit is implemented to ensure that the resonant frequency of the antenna matches the source frequency. An efficiency tracking control unit is used to periodically tune the receiver resonant frequency during an evaluation phase. After the receiver frequency is matched, the control unit enters the idle phase to reduce the power consumption.

A frequency tuning protocol at the initialisation phase is needed to ensure that the high-Q narrowband receiver can start up from cold since the resonant frequency of the receiver might be much different from the source frequency. At cold-start, where there is no available storage energy at the receiver, the LC-tuning circuit cannot operate since it requires a supply voltage source. The transmitter may need to slowly sweep the input frequency to allow the receiver to harvest the energy. After the receiver is woken up from cold, the LC-tuning circuit can then be enabled to tune the resonant frequency to boost the received voltage. Note that the designer has the freedom to choose the desired system protocol since the prototype IC is not restricted to the given example system protocol.

Besides the improvement of the transmitter magnetic field strength and the receiver induced voltage for extending the wireless sensor network operating distance, the network coverage area can be further increased by reducing the receiver input start-up voltage (or increasing the receiver sensitivity). The subthreshold voltage rectifier, used for converting the incoming magnetic energy to a DC voltage, has a start-up voltage below the transistor threshold voltage (V_{th}) which can improve the input sensitivity of the receiver node. Moreover, the segmented rectifier architecture allows the rectifier to tune the efficiency according to the input by changing the transistor dimensions. Therefore, the segmented rectifier can provide high efficiency over a wide input voltage range, which is very beneficial since the harvested voltage at the receiver antenna is varied across the operating distance. Furthermore, the rectifier efficiency control unit is only enabled briefly and enters the idle period to save the power, the same as the LC-tuning control unit.

Furthermore, the DC-DC charge pump (CP) is used to convert the DC voltage from the rectifier output to a larger DC voltage that can supply external modules of the receiver such as a sensor module or a microcontroller. The harvested power from the DC-DC converter may be low (typically a few μW), but the harvested energy can still sufficiently supply external modules if the active duty cycle of the external module is much lower compared with its inactive duty cycle. However, the harvested energy at the receiver antenna may be very low such that the CP must be disabled briefly to allow the rectifier to re-charge the storage capacitor/battery to a sufficient level. As a consequence, the reverse current is drained by the disabled CP which decreases the DC-DC output

voltage. This can be fixed easily by adding a diode connecting between the CP output and the storage capacitor/battery, but such a solution adds more cost.

The QPSK data demodulator is used for the system synchronisation as the QPSK signal strength and the operating frequency are fixed, hence the harvested energy can be stable. However, since the high-Q resonant circuit is used to increase the received voltage, the phase transition of the received QPSK signal is slow due to the narrow-bandwidth high-Q LC characteristic. The input sub-sampling QPSK demodulator is designed to extract data from the slow phase QPSK signal. As a result, the slow phase shift QPSK data demodulation is achieved at moderate bit-error-rate (BER) performance with a low data rate for a high-Q factor LC-circuits. Note that a low data rate between 100bps and 10kbps is sufficient for the system synchronisation of the wireless sensor network applications. In addition, the proposed data demodulator presented in this project only consumes a few µW power which leaves enough harvested energy for further use. However, the BER achieved by the demodulator is poor when the Q-factor is increasing. This is because the chosen sub-sampling dividing ratio is insufficient to under-sample the high-Q slow phase transition QPSK signal. The sub-sampling QPSK demodulator design offers an ultra-low power solution with moderate BER performance which is enough for this application. However, if high performance is to be expected, then a more power-hungry demodulator circuit may be needed.

The system level studies and simulations allow us to identify the requirements of the system including the specifications of the receiver building blocks. Besides the rectifier and data demodulator, several basic cells were developed for this project with the improvement of the circuit power efficiency to ensure that the receiver circuit can operate at ultra-low power. While the first IC prototype can perform energy harvesting at a low start-up voltage and QPSK data demodulation from a very low Q-factor circuit, however, a few short comings are still visible. The switch-over subthreshold rectifier still suffers from an efficiency drop at a certain input voltage range. Moreover, the QPSK demodulator from the first prototype fails to extract data from the slow phase shift QPSK signal in a high-Q circuit. Furthermore, the LC-tuning circuit has not been implemented in the first design. Therefore, the second IC prototype is developed to resolve the remaining issues.

The IC evaluation of the wireless energy harvesting receiver conducted in laboratory and field experiments demonstrates the feasibility of the magnetic coupled wireless energy harvesting system for wireless sensor network applications. The receiver system is suitable for integration in a standard CMOS technology without the requirement of additional masks in the fabrication process which reduces overall costs. The external modules (i.e., a radio transmitter, a sensor module and a

microcontroller) can be further integrated into the receiver IC to reduce cost and reduce the circuit power consumption to improve the receiver sensitivity.

7.2 Future Work

The project has so far addressed all the system requirements of the wireless sensor network applications, but there are many areas of continuing work that can be further developed. This section describes the potential aspects that can be considered.

In practical applications, the coverage area of the wireless sensor network can be as large as 200x200m^2 which leads to the need for a large transmitter current for generating the minimum required magnetic field strength. Instead of increasing the transmitter current or the number of turns of the transmitter loop antenna, the large loop transmitter can be divided into several smaller loop coils to provide the magnetic field energy harvesting source. For example, the 200x200m^2 transmitter loop coil can be divided into four transmitter loop coils with the sizes of 50x50m^2. Hence the magnetic field strength of the smaller loop can be larger compared with the larger loop at the same transmitter current level, and the field strength can be further improved by increasing the number of turns of the transmitter loop since the required resonant capacitor may still be feasible. However, the magnetic signal from one of the smaller loop coils is likely to couple with other adjacent loop coils which can cause signal interference. This issue may be resolved simply by choosing a different carrier frequency for each loop coil. Since the transmitter and receiver antennas in this application employ a high-Q LC circuit to maximise the harvested energy, the signal interference from the inductive coupling may be less impactful if each loop operates at a different carrier. The system level of the multiple transmitter antennas must be studied, and the data communication and protocol for system synchronisation may need to be further developed.

The receiver antenna coil induces maximum voltage when there is no angular misalignment between the transmitter coil and the receiver coil, however the misalignment of the coils may occur in practice. As mentioned earlier in Chapter 6, two or more coils with different angular orientations can be used to receive the magnetic energy to ensure that the transmitter and receiver coils are perfectly aligned. However, the receiver circuits (i.e., the voltage rectifier, the LC-tuning circuit) for each coil with different angular orientation are needed to tune the resonant frequency and convert the harvested energy to a usable power source. This leads to the requirement of more components such as an array capacitor or a receiver IC. Further research can be explored which only uses a single receiver IC that can switch between the input antenna coils.

As stated in the beginning, the standard CMOS process is chosen in this project due to its cheaper cost, however the rectifier circuit can be further improved to enhance the receiver input sensitivity

by selecting a more expensive CMOS process. Since the rectifier input sensitivity is dependent on the transistor V_{th} which is technology dependent, near-zero-V_{th} transistors can be used to reduce the rectifier start-up voltage. However, it is important to note that the rectifier implemented from near-zero-V_{th} transistors suffers from a reverse leakage current which is more serious than the proposed subthreshold rectifier due to its lower V_{th}. The proposed segmental rectifier concept can be incorporated with the near-zero-V_{th} rectifier to improve the rectifier efficiency.

Several basic circuits implemented in the power management unit in this project consume ultra-low power but sacrifice the accuracy of the reference signal and have less PVT tolerance than the state-of-the-art power management unit. Such results are acceptable for the system requirements in this project. However, if the receiver system is fully integrated with the sensor interface, the transmitter radio module and the microcontroller into a single chip, then a high precision power management unit that operates at ultra-low power is needed.

It has been shown that the BER of the proposed high-Q QPSK demodulator is worst when the Q-factor of the system is increased, the demodulator can be further developed by improving the sub-sampling circuit. From the waveform measurement results of the QPSK signal demodulation, it can be seen that the amplitude of the signal drops shortly during the input signal phase transition. An envelope detection may be used instead of a clock recovered PSK demodulation technique to extract the data. However, the signal voltage drop only occurs in a high-Q resonant circuit.

The DC-DC CP used in this project requires a diode to prevent the output reverse current drain when the CP is disabled. However, the output voltage of the CP with the diode suffers from the forward voltage which can lower the receiver start-up voltage. Further research can be undertaken to prevent the CP output reverse current without using an additional diode. An on-chip power switch may be used to prevent the CP reverse current drain, however, the leakage from the power switch and the biasing circuit must be minimised.

The system synchronisation protocol of the wireless energy harvest shown in this thesis can be further developed to maintain the reliable communication sharing, cooperative processing between sensor nodes, improve the energy efficiency of the sensor nodes and reduce the synchronisation time of the network. Since the choice of protocol is not restricted by the proposed receiver design, a further study of the synchronisation protocol can help improve the system.

Appendix A Resonant circuit and power transfer efficiency of the inductive loosely coupled system

Figure 7.1 shows the circuit model of the inductive coupled wireless power transfer from section 2.2.4, the output voltage V_2 and the power transfer efficiency of the circuit are derived as follows.

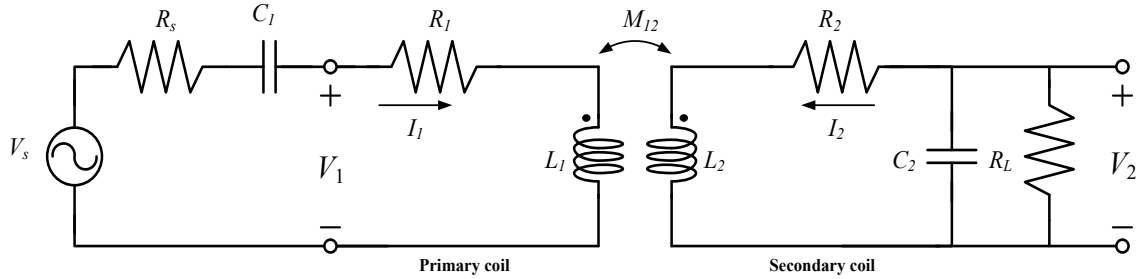


Figure 7.1 The circuit model of the inductive coupled wireless power transfer.

From the circuit depicted in figure 7.1, the Q-factor Q_L corresponding with the inductor L_2 and the Q-factor Q_R corresponding to the capacitor C_2 of the secondary coil are

$$Q_L = \frac{\omega_0 L_2}{R_2}, \qquad (7.1)$$

$$Q_R = \omega_0 C_2 R_L, \qquad (7.2)$$

where ω_0 is the resonant frequency which is given by

$$\omega_0 = \frac{1}{\sqrt{L_2 C_2}}. \qquad (7.3)$$

From equation (7.1) and (7.2), the product of the equation is

$$Q_L Q_R = \frac{R_L}{R_2}. \qquad (7.4)$$

The current I_2 at the secondary coil is

$$I_2 = -\frac{V_2(1 + j\omega C_2 R_L)}{R_L}. \qquad (7.5)$$

If the system is operated at resonant frequency $\omega = \omega_0$, the equation can be substituted by Q-factor from equation (7.2) as

$$I_2 = -\frac{V_2(1 + jQ_R)}{R_L}. \qquad (7.6)$$

By substituting the current from equation (7.6) in (2.2) from section 2.2, the voltage at the secondary coil is

$$V_2 = -\frac{V_2(1 + jQ_R)}{R_L} \cdot R_2 - \frac{V_2(1 + jQ_R)}{R_L} \cdot j\omega_0 L_2 + j\omega_0 M_{12} I_1, \qquad (7.7)$$

$$V_2\left(1+\frac{1+jQ_R}{R_L}\cdot R_2+\frac{1+jQ_R}{R_L}\cdot j\omega_0 L_2\right)=j\omega_0 M_{12}I_1\,, \qquad (7.8)$$

$$V_2\left(1+\frac{1+jQ_R}{R_L}\cdot R_2\left(1+\frac{j\omega_0 L_2}{R_2}\right)\right)=j\omega_0 M_{12}I_1\,, \qquad (7.9)$$

substituting with equation (7.1)

$$V_2\left(1+\frac{(1+jQ_R)(1+jQ_L)}{Q_L Q_R}\right)=j\omega_0 M_{12}I_1\,, \qquad (7.10)$$

$$V_2\left(\frac{1+j(Q_L+Q_R)}{Q_L Q_R}\right)=j\omega_0 M_{12}I_1\,, \qquad (7.11)$$

$$V_2=\frac{j\omega_0 M_{12}I_1 Q_L Q_R}{1+j(Q_L+Q_R)}\,, \qquad (7.12)$$

the magnitude of the voltage is

$$|V_2|=\frac{\omega_0 M_{12}I_1 Q_L Q_R}{\sqrt{1+(Q_L+Q_R)^2}}\,, \qquad (7.13)$$

since the Q-factor of the circuit is usually large where $(Q_L+Q_R)^2 \gg 1$, hence

$$|V_2|\cong\frac{Q_L Q_R}{Q_L+Q_R}\cdot\omega_0 M_{12}I_1=\omega_0 M_{12}I_1 Q\,. \qquad (7.14)$$

It is important to note that *Q* from equation (7.14) represents the Q-factor the secondary coil where

$$Q=\frac{Q_L Q_R}{Q_L+Q_R}\,. \qquad (7.15)$$

$$Q=\frac{\omega_0 L_2 C_2 R_L}{L_2+C_2 R_L R_2}\,. \qquad (7.16)$$

The power transfer efficiency of the circuit is given by

$$\eta=\frac{P_L}{P_s}=\frac{V_2^2/R_L}{V_s^2/(R_s+R_1)}\,, \qquad (7.17)$$

where P_L is the power delivered to the load, V_s is the voltage source and R_s is the losses resistance at the source. Furthermore, the load voltage V_2 in equation (7.14) can be substituted with (7.17) if the system is operated at the resonant frequency as

$$\eta=\frac{(\omega_0 M_{12}I_1 Q)^2/R_L}{V_s^2/(R_s+R_1)}\,. \qquad (7.18)$$

Since the system is operated at the resonant frequency, the impedance of capacitor C_1 and inductor L_1 cancels each other out. Hence the current is

$$I_1=\frac{V_S}{R_S+R_1}=\frac{V_S}{R_{TX}}. \qquad (7.19)$$

By substituting the voltage in equation (7.18) with (7.19), the PTE is

$$\eta = \frac{(\omega_0 M_{12} I_1 Q_{RX})^2 R_{TX}}{R_L V_S^2}. \quad (7.20)$$

The simplifier PTE equation can be derived by substituting the coupling coefficient $M = k\sqrt{L_1 L_2}$ and $Q_{TX} = {\omega_0 L_1}/{R_{TX}}$, which yield

$$\eta = \frac{\left(\omega_0 k\sqrt{L_1 L_2} I_1 Q_{RX}\right)^2 R_{TX}}{R_L V_S^2} = \left(\frac{\omega_0 L_1}{R_{TX}}\right)\left(\frac{\omega_0 L_2}{R_L}\right) k^2 Q_{RX}^2, \quad (7.21)$$

$$\eta = Q_{TX}\left(\frac{\omega_0 L_2}{R_L}\right) k^2 Q_{RX}^2. \quad (7.22)$$

By substituting one of the Q_{RX} with equation (7.4) and (7.15), the PTE is

$$\eta = k^2 Q_{TX} Q_{RX} \frac{Q_L Q_R}{Q_L + Q_R} \frac{Q_L}{Q_L Q_R} = k^2 Q_{TX} Q_{RX} \frac{Q_L}{Q_L + Q_R}. \quad (7.23)$$

Since the loading resistance tends to be much higher than the resistance of the secondary inductor, hence the Q-factor Q_L is much larger than Q_R. This is because the load resistance in this system is the input resistance of the rectifier as discussed in chapter 4, which has the typical value between 10kΩ and 100kΩ, while the resistance of the secondary inductor is practically less than 100Ω. Hence, $\frac{Q_L}{Q_L + Q_R} \approx 1$ and

$$\eta \cong k^2 Q_{TX} Q_{RX}. \quad (7.24)$$

Appendix B Derivation of the magnetic field of the square/rectangular loop

The expression of the magnetic field generated by the square loop shown in equation (2.11) can be derived as follows [15, 23]. Consider the model of a square loop antenna depicted in figure 7.2, if the overall length of the square loop is relatively small compared with the wavelength of the input signal, the square loop can be considered as four identical small dipoles. Thus, each dipole can be separately analysed. From the Biot-Savart law, the magnetic field generated from the dipole CD is

$$\boldsymbol{H_{CD}} = \frac{I_{TX}}{4\pi}\int_C^D \frac{\boldsymbol{dl}\times\boldsymbol{r}}{r^3}, \quad (7.25)$$

where the vectors are given by

$$\boldsymbol{l} = (-W\cdot t, W, 0), \quad (7.26)$$

$$\boldsymbol{dl} = -W(1,0,0), \quad (7.27)$$

$$\boldsymbol{r} = (x + W\cdot t, y - W, z). \quad (7.28)$$

Thus, the cross product of the vector is

$$\boldsymbol{dl}\times\boldsymbol{r} = \big(0, W\cdot z, -W(y-W)\big). \quad (7.29)$$

Substituting the product of the vectors into equation (7.25) yields

$$\boldsymbol{H_{CD}} = \frac{I_{TX}}{4\pi}\int_{-1}^{1} \frac{W\cdot z\boldsymbol{y} - W(y-W)\boldsymbol{z}}{[(x+W\cdot t)^2+(y-W)^2+z^2]^{3/2}}\,dt. \quad (7.30)$$

Equation (7.30) can be mathematically substituted in order to simplify the equation for integrating. By substituting $t' = W\cdot t$ and $dt' = W\cdot dt$, the equation is simplified to

$$\boldsymbol{H_{CD}} = \frac{I_{TX}}{4\pi}\int_{-W}^{W} \frac{z\boldsymbol{y} - (y-W)\boldsymbol{z}}{[(x+t')^2+(y-W)^2+z^2]^{3/2}}\,dt'. \quad (7.31)$$

Since the square loop is symmetrical, it can be observed from figure 7.2 that the magnetic field in X and Y directions cancel each other out. In consequence, the equation of the magnetic field of the dipole can be reduced to

$$\boldsymbol{H_{CD}} = \frac{I_{TX}}{4\pi}\int_{-W}^{W} \frac{-(y-W)\boldsymbol{z}}{[(x+t')^2+(y-W)^2+z^2]^{3/2}}\,dt'. \quad (7.32)$$

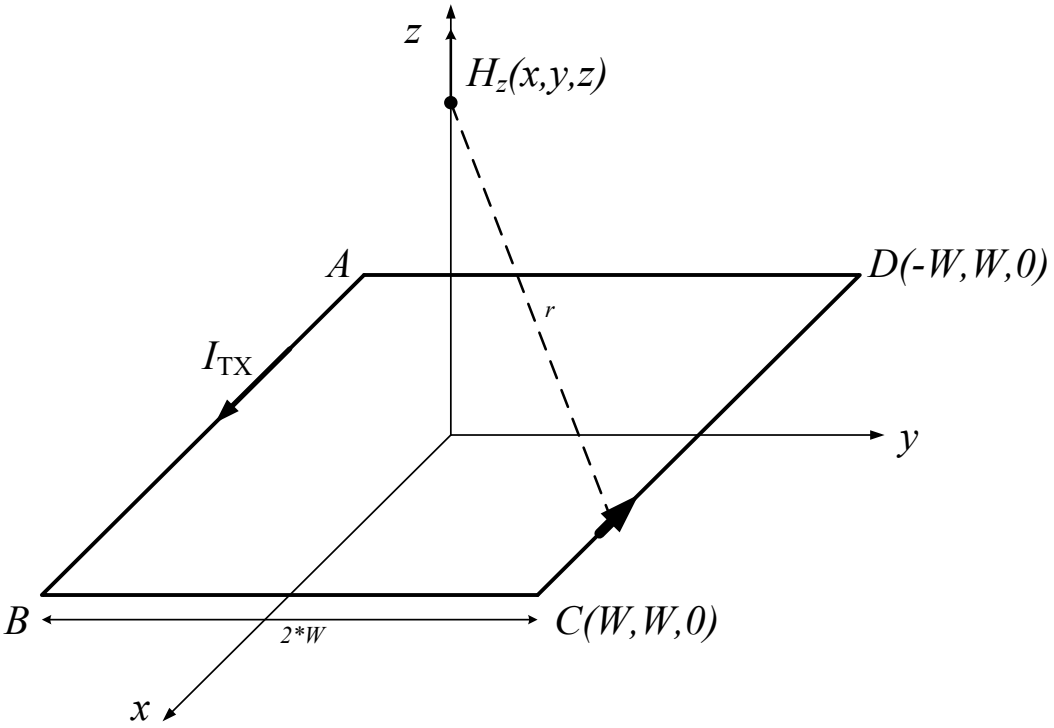


Figure 7.2 Model of a square loop antenna.

Equation (7.32) represents the integral equation of the magnetic field generated by the dipole CD. The integration can further be simplified to

$$H = \int_{-W}^{W} \frac{dA}{[(X+A)^2+k^2]^{3/2}}. \quad (7.33)$$

After the magnetic field of a single dipole is modified to equation (7.33), the integration is demonstrated as follows. Firstly, the equation is substituted by $B = A - X$ and $dB = dA$ which results

$$H = \int_{-W+X}^{W-X} \frac{dB}{[B^2+k^2]^{3/2}}. \quad (7.34)$$

Note that the limits are modified as well. Secondly, the formula is further replaced by $C = {}^{B}/_{k}$ and $dC = {}^{dB}/_{k}$ as

$$H = \frac{1}{k^2} \int_{\frac{-W+X}{k}}^{\frac{W-X}{k}} \frac{dC}{[C^2+1]^{3/2}}. \quad (7.35)$$

Thirdly, the substitution of the trigonometric forms $C = \tan D$ and $dC = \left({}^{1}/_{\cos^2 D}\right) dD$ returns

$$H = \frac{1}{k^2} \int_{\tan^{-1}\frac{-W+X}{k}}^{\tan^{-1}\frac{W-X}{k}} \cos D \, dD. \quad (7.36)$$

Fourthly, the simplified integral equation (7.36) can be easily integrated to

$$H = \frac{1}{k^2}\left[\sin\left(\tan^{-1}\left(\frac{W-X}{k}\right)\right) + \sin\left(\tan^{-1}\left(\frac{W+X}{k}\right)\right)\right]. \quad (7.37)$$

Adopting the Pythagorean identity formula

$$\sin h = \frac{\tan h}{\sqrt{1+\tan^2 h}}, \quad (7.38)$$

therefore equation (7.37) is simplified to

$$H = \frac{1}{k^2}\left[\frac{\frac{W-X}{k}}{\sqrt{1+\frac{(W-X)^2}{k^2}}} + \frac{\frac{W+X}{k}}{\sqrt{1+\frac{(W+X)^2}{k^2}}}\right], \quad (7.39)$$

$$H = \frac{1}{k^2}\left[\frac{W-X}{\sqrt{(W-X)^2+k^2}} + \frac{W+X}{\sqrt{(W+X)^2+k^2}}\right]. \quad (7.40)$$

By comparing equation (7.32) and (7.40), the result of the magnetic field due to dipole CD is expressed by

$$\boldsymbol{H_{CD}} = \frac{I_{TX}}{4\pi} \cdot \frac{-(y-W)}{(y-W)^2+z^2}\left[\frac{W+x}{\sqrt{(W+x)^2+(y-W)^2+z^2}} + \frac{W-X}{\sqrt{(W-x)^2+(y-W)^2+z^2}}\right]. \quad (7.41)$$

The remain three dipoles are similarly computed, therefore the final equation of the magnetic field is expressed as

$$\begin{aligned} H_z(x,y,z) = \frac{I_{TX}}{4\pi} \cdot \Bigg\{ & \frac{-(y-W)}{(y-W)^2+z^2} \cdot \left(\frac{x+W}{\sqrt{(x+W)^2+(y-W)^2+z^2}} + \frac{-x+W}{\sqrt{(-x+W)^2+(y-W)^2+z^2}} \right) \\ & + \frac{(x+W)}{(x+W)^2+z^2} \cdot \left(\frac{y+W}{\sqrt{(x+W)^2+(y+W)^2+z^2}} + \frac{-y+W}{\sqrt{(x+W)^2+(-y+W)^2+z^2}} \right) \\ & + \frac{(y+W)}{(y+W)^2+z^2} \cdot \left(\frac{-x+W}{\sqrt{(-x+W)^2+(y+W)^2+z^2}} + \frac{x+W}{\sqrt{(x+W)^2+(y+W)^2+z^2}} \right) \\ & - \frac{(x-W)}{(x-W)^2+z^2} \cdot \left(\frac{-y+W}{\sqrt{(x-W)^2+(-y+W)^2+z^2}} + \frac{y+W}{\sqrt{(x-W)^2+(y+W)^2+z^2}} \right) \Bigg\}. \end{aligned} \quad (7.42)$$

Appendix C Derivation of the input impedance of the voltage multiplier rectifier

Figure 7.3(a) illustrates the voltage multiplier rectifier circuit. The derivation of the input impedance of the circuit is shown as follows. The equivalent circuit of the rectifier is depicted in figure 7.3(b); the capacitor C_{par} is the summation of the MOS capacitance and the parasitic capacitance. Moreover, the resistance of the diode-connected is computed from the dividing of the voltage across the diode V_X and the current of the diode [19]. In this chapter, we only analyse the input impedance of the rectifier (Figure 7.3(c)) as the LC-antenna circuit is mainly affected by the rectifier input impedance. Moreover, the output behaviour of the rectifier has been discussed in section 3.2.

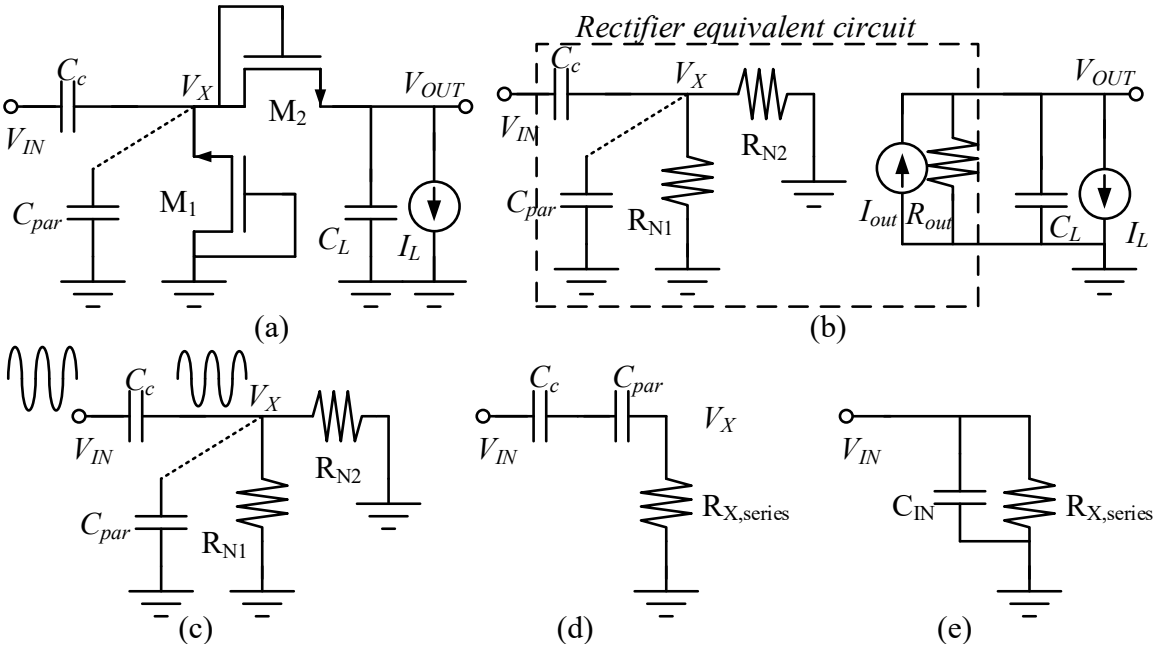


Figure 7.3 Impedance transformation of the voltage multiplier rectifier.

From [19], the diode current can be approximate by the fundamental frequency of the current. The fundamental component computed from the Fourier series is given by [19]

$$I_{fund} = \frac{2}{T}\int I_D(t)\cos(\omega t)dt \cong \frac{2}{T}\int I_D(t)dt = 2I_L . \quad (7.43)$$

Thus, the diode resistance is

$$R_N \cong \frac{V_X}{I_{fund}} = \left(\frac{C_c}{C_c + C_{par}}\right)\frac{V_{IN}}{2I_L} . \quad (7.44)$$

Since the diode-connected NMOS devices are identical, the node *X* resistance is the paralleling resistance

$$R_X = \frac{R_N}{2} . \quad (7.45)$$

Moreover, the parallel capacitor and resistor shown in figure 7.3(c) can be transformed to series capacitor and resistor as illustrated in figure 7.3(d). The values of the series lump components are

$$C_{par,series} \cong C_{par}, \tag{7.46}$$

$$R_{X,series} \cong \frac{R_X}{Q_X^2}. \tag{7.47}$$

Q_X is the quality factor of the parallel capacitor and resistor at node *X* which can be expressed as

$$Q_X = 2\pi f R_X C_{par}, \tag{7.48}$$

where *f* is the operating frequency of the circuit. Furthermore, the series capacitors C_c and $C_{par,series}$ are added to

$$C_{series} \cong \frac{C_c C_{par}}{C_c + C_{par}}. \tag{7.49}$$

Finally, the series capacitor and resistor can be transformed to parallel input impedance as shown in figure 7.3(e). The input impedance can be expressed as

$$C_{IN} \cong C_{series} = \frac{C_c C_{par}}{C_c + C_{par}}, \tag{7.50}$$

$$R_{IN} \cong Q_{IN}^2 R_{X,series} = \frac{C_c + C_{par}}{C_c} \cdot \frac{V_{IN}}{4I_L}, \tag{7.51}$$

where Q_{IN} is

$$Q_{IN} = \frac{1}{2\pi f R_{X,series} C_{series}}. \tag{7.52}$$

Equation (7.50) and (7.51) are the input impedance of the single stage voltage multiplier rectifier. As discussed in section 3.2.2, the output voltage can be increased by a factor of *N* by increasing the stages of the rectifier to N stages. The input impedance components of the N-stages voltage multiplier rectifier is therefore divided/multiplied by a factor of *N* as given by

$$R_{IN} = \frac{C_c + C_{par}}{NC_c} \cdot \frac{V_{IN}}{4I_L}, \tag{7.53}$$

$$C_{IN} = N\frac{C_c C_{par}}{C_c + C_{par}}. \tag{7.54}$$

Appendix D Calculation of the output power delivery requirement

The output power produced by the energy harvesting unit discussed in chapter 4 is intended to be delivered typically to three off-chip modules which are (1) a sensor module, (2) a transmitter module and (3) a microcontroller. Typical examples of application system modules are shown in Table 7.1. Note that the calculations in this section only valid for these particular modules. Other applications would have different demands on the sensor, transmitter and microcontroller.

Table 7.1 Part numbers of the example modules.

Module	Part number
Sensor node	SHT25, Humidity and Temperature Sensor IC [79]
Transmitter	MICRF112, QwikRadio UHF ASK/FSK Transmitter [80]
Microcontroller	PIC12F1612, 8-Pin 8-Bit Flash Microcontroller [81]

Table 7.2 Power consumption of the modules.

Module	Current supply	Voltage supply	Power consumption	Active time (per hour)	Energy consumption (per hour)
Sensor node	350µA	3V	1.05mW	130.2ms	136.71µJ
Transmitter	10.5mA	3V	31.5mW	4ms	126µJ
Microcontroller	365µA (Active) 11nA (Idle)	3V	1.095mW (Active) 99nW (Idle)	200ms	219µJ (Active) 356.4µJ (Idle)

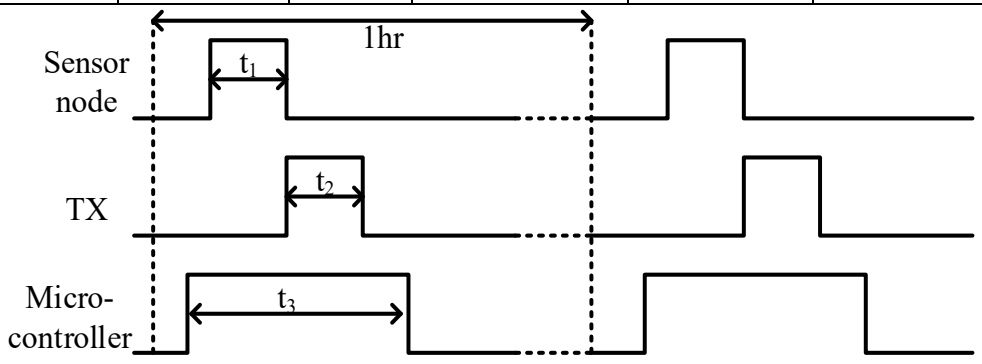


Figure 7.4 Example timing diagram of the external modules operation.

The microcontroller module is used for controlling the activation time slot of the sensor module and the transmitter module. As the sensor module and the transmitter module are only activated in a certain period, the total power consumption is effectively reduced. Table 7.2 shows the power consumption of each module, the active time of the modules is determined from the datasheet of

the module. It can be seen that the power consumption of the microcontroller module shown in the table is separated into active mode and idle mode since the microcontroller is activated only when it collects data from the sensor module and transmits the acquired data via the transmitter module. Figure 7.4 illustrates the example timing diagram of the external modules operation.

From table 7.2, the total energy consumption per hour is

Total energy per hour = 136.71μJ +126μJ + 219μJ + 356.4μJ = 838.11μJ.

The total power consumption of the external modules is

$$P = E/t = \frac{833.11\mu J}{3600s} = 0.2314\mu W .$$

Therefore, the average power consumption of the external modules is 0.23μW while the peak power consumption is approximately 34mW.

In addition, the buffer capacitor can be calculated using equation (4.1) shown in section 0 as

$$C = \frac{i(t)}{\frac{dv(t)}{dt}} = \frac{11.33mA}{\left(\frac{3.3V - 2.9V}{4ms}\right)} = 113.3\mu F ,$$

when the peak current is 11.33mA, the out voltage is decreased from 3.3V to 2.9V and the active period is 4ms. Note that an external voltage regulator is not needed if the external modules can tolerate such a supply voltage range.

Appendix E Wireless Energy Harvesting Receiver IC Simulation Results and IC Floor Plan

In this chapter, the simulation results of the prototype wireless energy harvesting receiver from chapter 4 are shown. Note that the terms worst-case power and speed are referred to the process parameters of the active devices (MOS transistors). The worst-case power means that the current flowing in the MOS channel is very large which leads to a large power consumption. On the other hand, the worst-case speed means that the MOS current is very low which leads to a slow circuit time response.

E.1 Rectifier Switch-over Detection Comparator

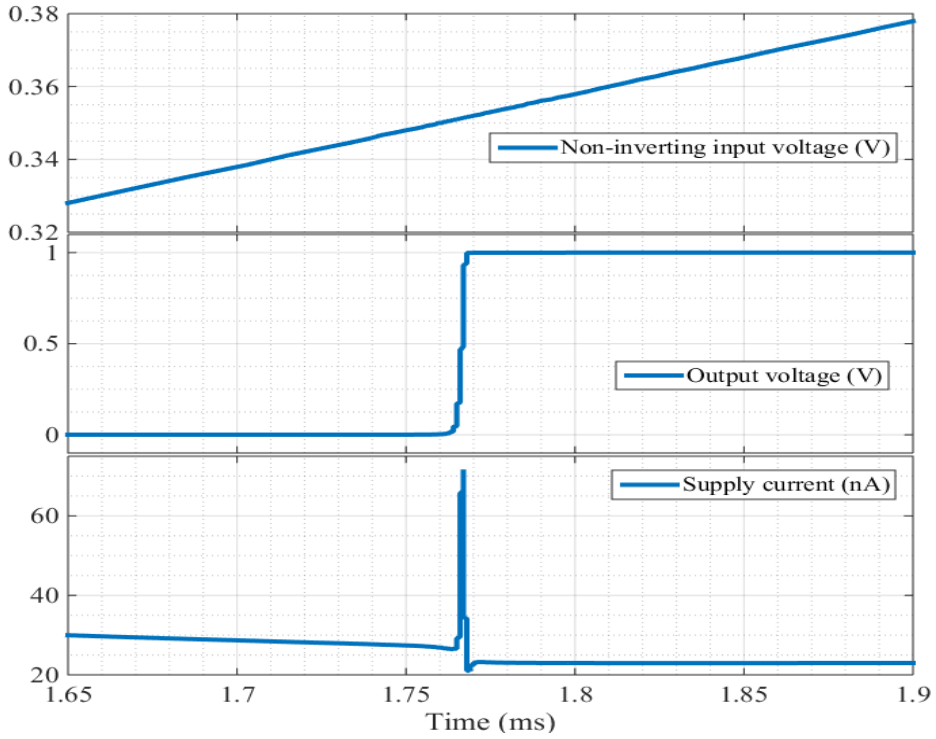


Figure 7.5 Transient response of the comparator for the rectifier. (Corresponding to Figure 4.11)

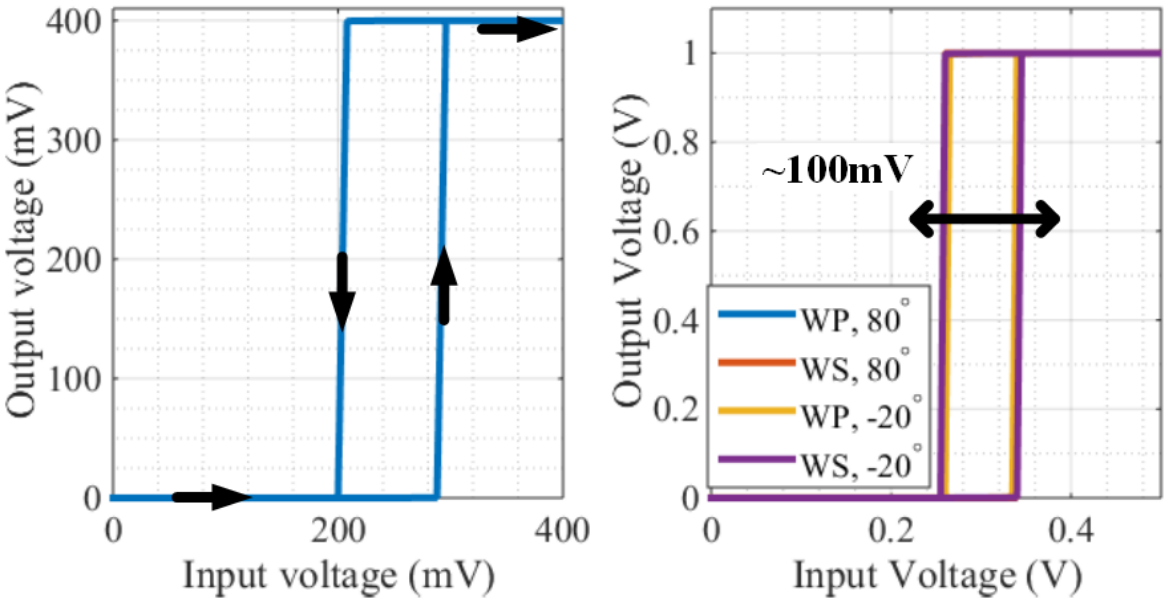


Figure 7.6 (Left) DC response of the comparator for the rectifier when the input voltage V_{in+} is swept from 0 to 400mV when V_{in-} is 250mV and the supply voltage is 400mV, and (Right) the process voltage and temperature (PVT) corners DC response of the comparator when the reference voltage is 300mV and the supply voltage is 1V. (WP=Worst-case power, WS=Worst-case speed) (Corresponding to Figure 4.11)

E.2 Voltage-controlled Oscillator used in the Data Demodulator

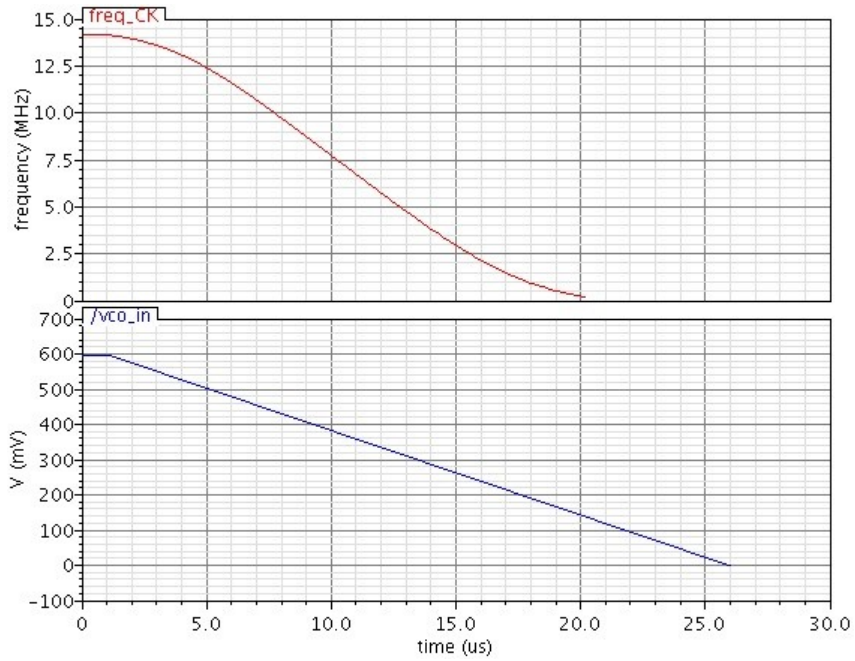


Figure 7.7 Transient response of the VCO when the supply voltage is 600mV. Top: Frequency generated from the VCO. Bottom: Input voltage control frequency of the VCO. (Corresponding to Figure 4.20)

Table 7.3 Output frequency range of the VCO (before being divided by four) with different supply voltage.

Supply voltage	Maximum frequency	Minimum frequency	KVCO
400mV	2.44MHz	354kHz	8.08MHz/V
500mV	7.62MHz	435kHz	21.8MHz/V
600mV	14.2MHz	240kHz	33.5MHz/V
700mV	21.1MHz	720kHz	42MHz/V
800mV	28MHz	561kHz	48MHz/V

Table 7.4 Corner simulation of the VCO when the supply voltage is 600mV.

Condition		Maximum frequency	Minimum frequency
Nominal	Temp. = -20°C	10.6MHz	504kHz
	Temp. = 27°C	14.2MHz	240kHz
	Temp. = 80°C	19.3MHz	782kHz
Worst-case: Speed	Temp. = -20°C	7.66MHz	270kHz
	Temp. = 27°C	10.5MHz	211kHz
	Temp. = 80°C	14.6MHz	640kHz
Worst-case: Power	Temp. = -20°C	14.3MHz	159kHz
	Temp. = 27°C	18.7MHz	531kHz
	Temp. = 80°C	24.9MHz	870kHz

E.3 Data Demodulator Input Amplifier

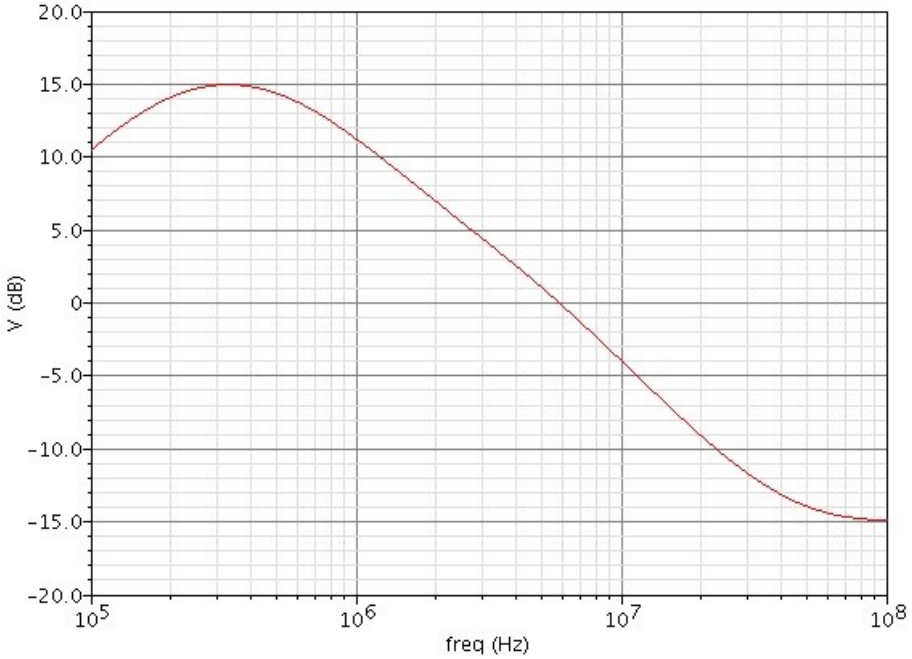


Figure 7.8 Frequency response of the inverting amplifier when the supply voltage is 600mV. (Corresponding to Figure 4.26)

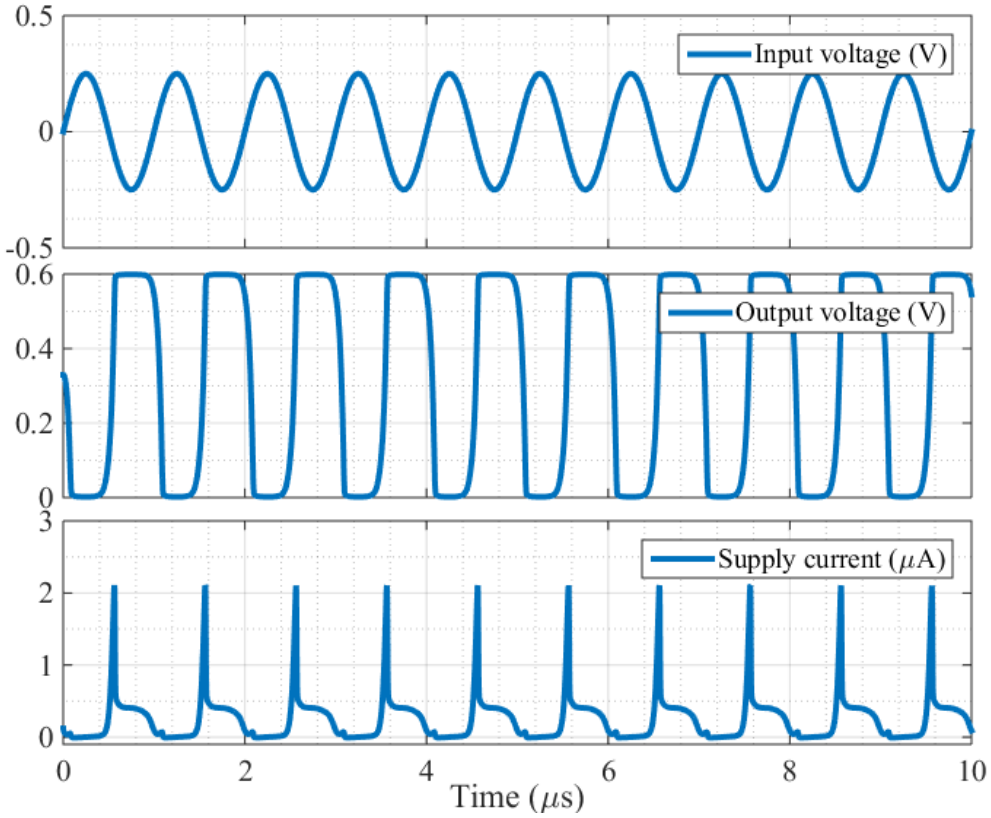


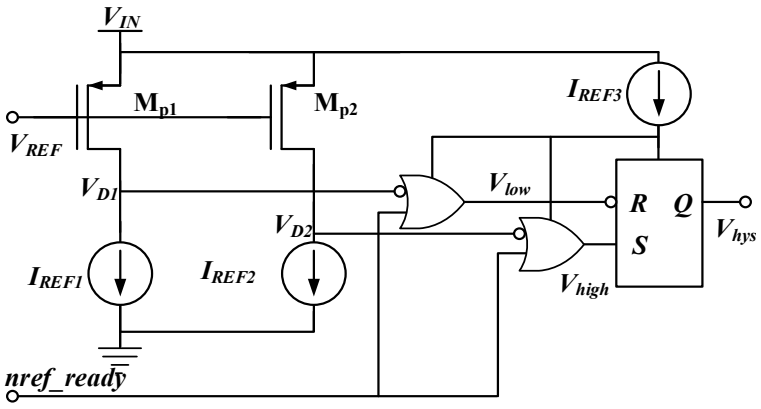
Figure 7.9 Transient response of the inverting amplifier when the supply voltage is 600mV. (Corresponding to Figure 4.26)

Table 7.5 Corner simulation of the inverting amplifier when the supply voltage is 600 mV.

(Minimum gain required is 3.6dB for 250mV$_{pk}$ input voltage)

Condition		Gain at 1 MHz	Power consumption
Nominal	Temp. = -20°C	-4.912dB	133nW
	Temp. = 0°C	3.337dB	141nW
	Temp. = 27°C	11.28dB	153nW
	Temp. = 80°C	21.65dB	193nW
Worst-case: Speed	Temp. = -20°C	-17.13dB	115nW
	Temp. = 0°C	-8.266dB	122nW
	Temp. = 27°C	2.867dB	132nW
	Temp. = 80°C	16.19dB	160nW
Worst-case: Power	Temp. = -20°C	5.281dB	155nW
	Temp. = 0°C	11.37dB	164nW
	Temp. = 27°C	17.7dB	181nW
	Temp. = 80°C	24.73dB	247nW

E.4 Voltage Level Detection used in the PMU



(Voltage level detection from Figure 4.31.)

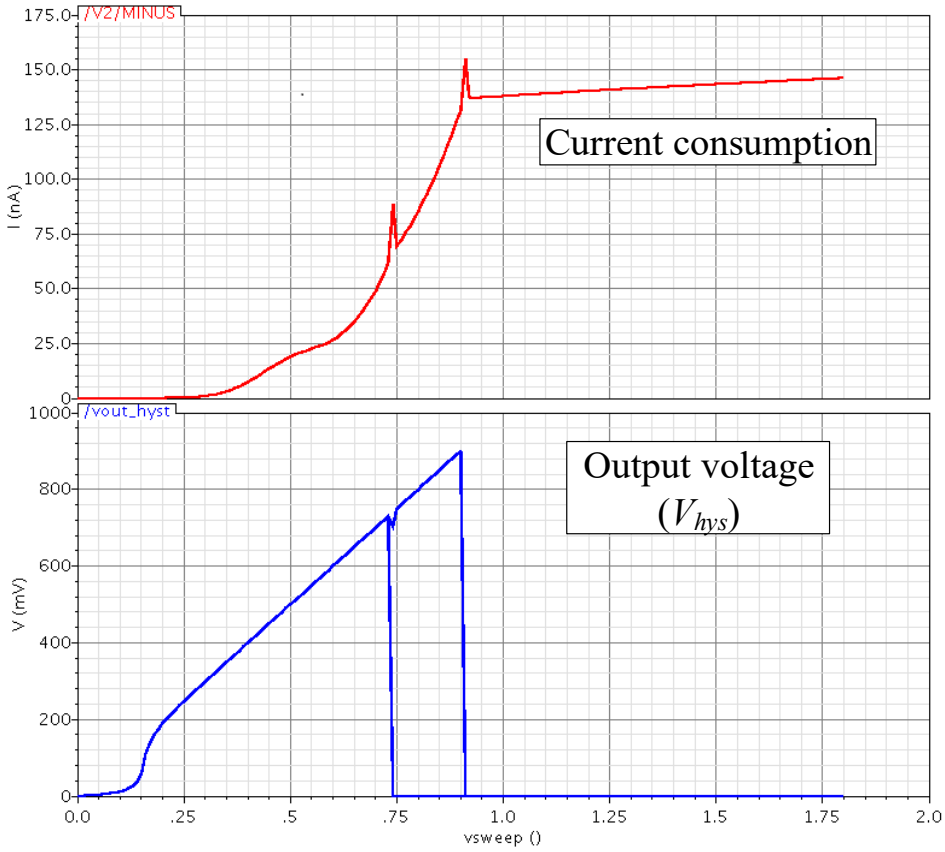


Figure 7.10 DC response of the level detection. Top: Current consumption, Bottom: Output voltage.

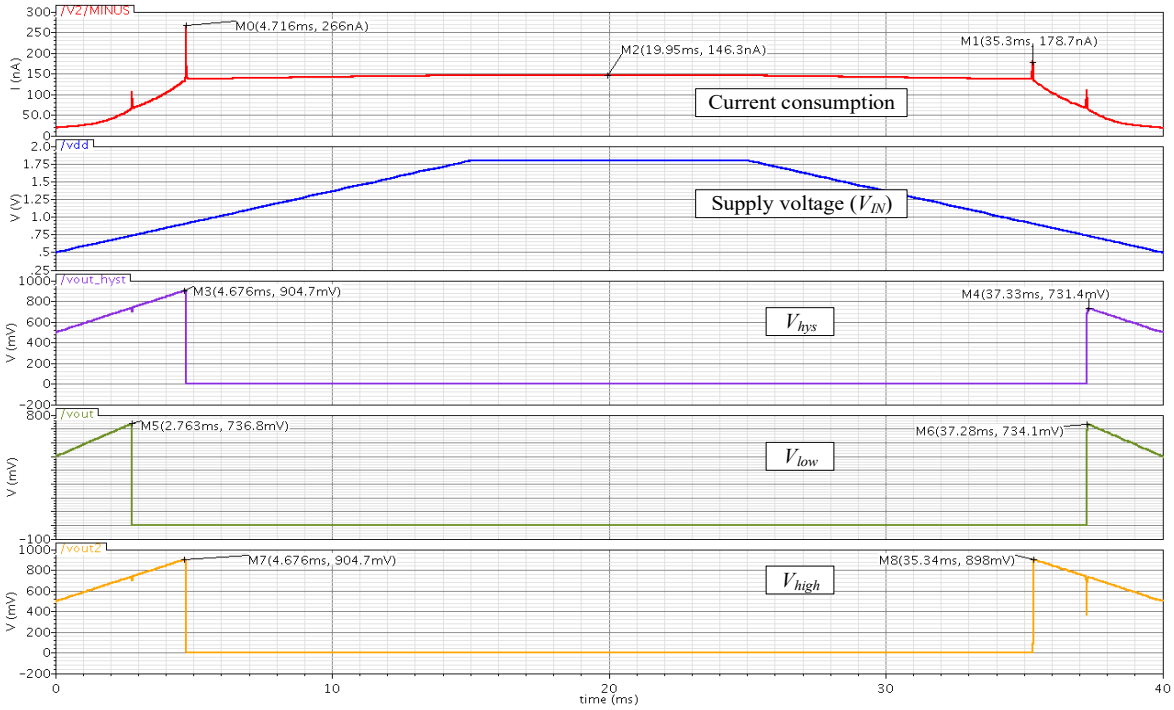
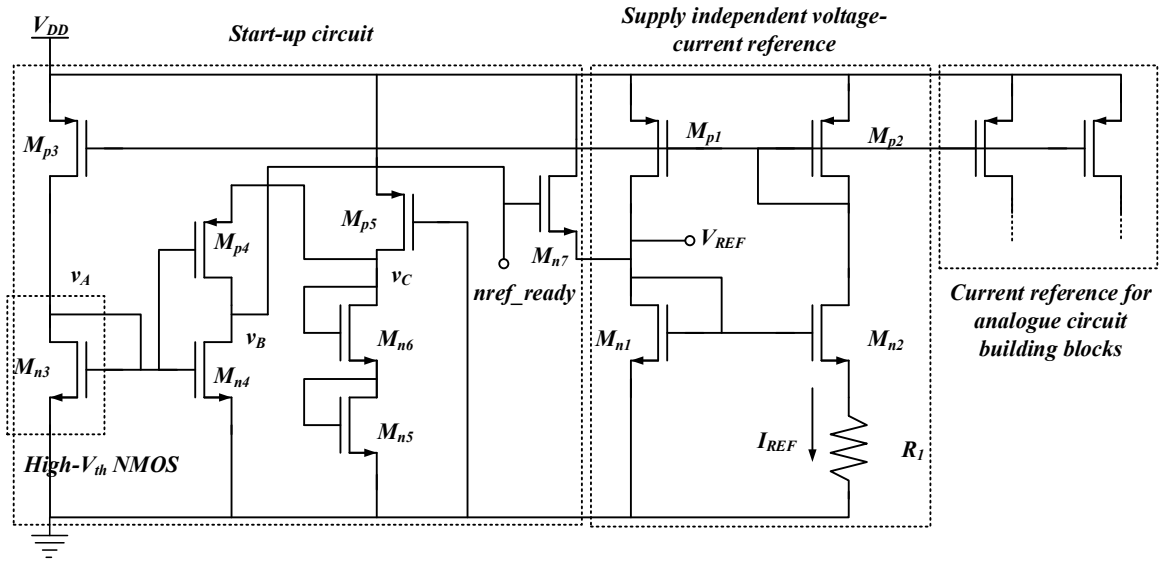


Figure 7.11 Transient response of the level detection.

Table 7.6 Corner simulation of the level detection.

Condition		V_{low}	V_{high}
Nominal	Temp. = -20°C	770mV	915mV
	Temp. = 0°C	755mV	910mV
	Temp. = 27°C	730mV	905mV
	Temp. = 80°C	690mV	910mV
Worst-case: Speed	Temp. = -20°C	825mV	970mV
	Temp. = 0°C	805mV	965mV
	Temp. = 27°C	780mV	955mV
	Temp. = 80°C	735mV	950mV
Worst-case: Power	Temp. = -20°C	740mV	855mV
	Temp. = 0°C	720mV	880mV
	Temp. = 27°C	700mV	875mV
	Temp. = 80°C	675mV	900mV

E.5 Voltage Reference used in the PMU



(Voltage reference circuit from Figure 4.32.)

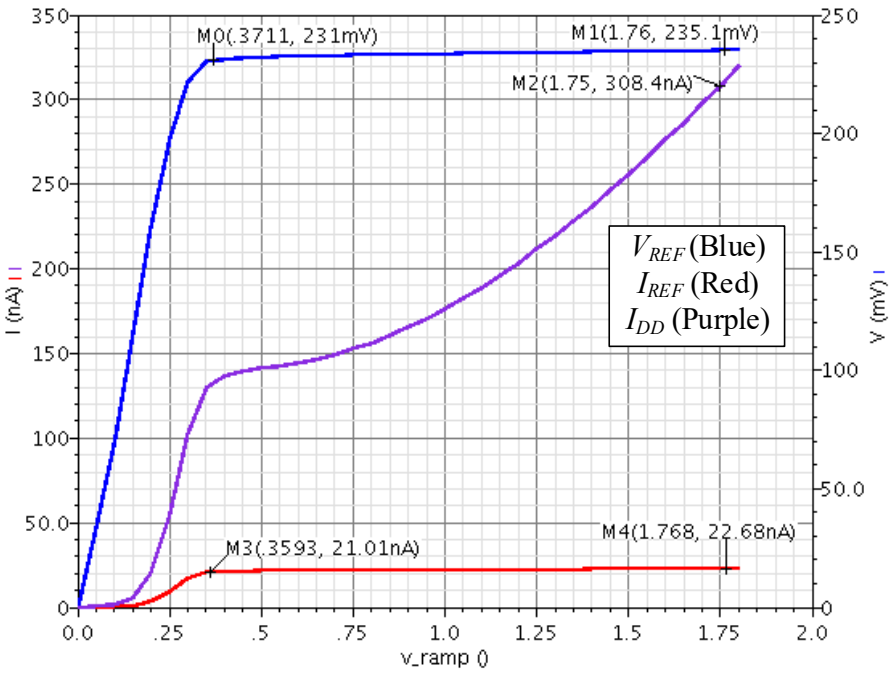


Figure 7.12 DC response of the voltage reference when the supply voltage is swept from 0 to 1.8V.

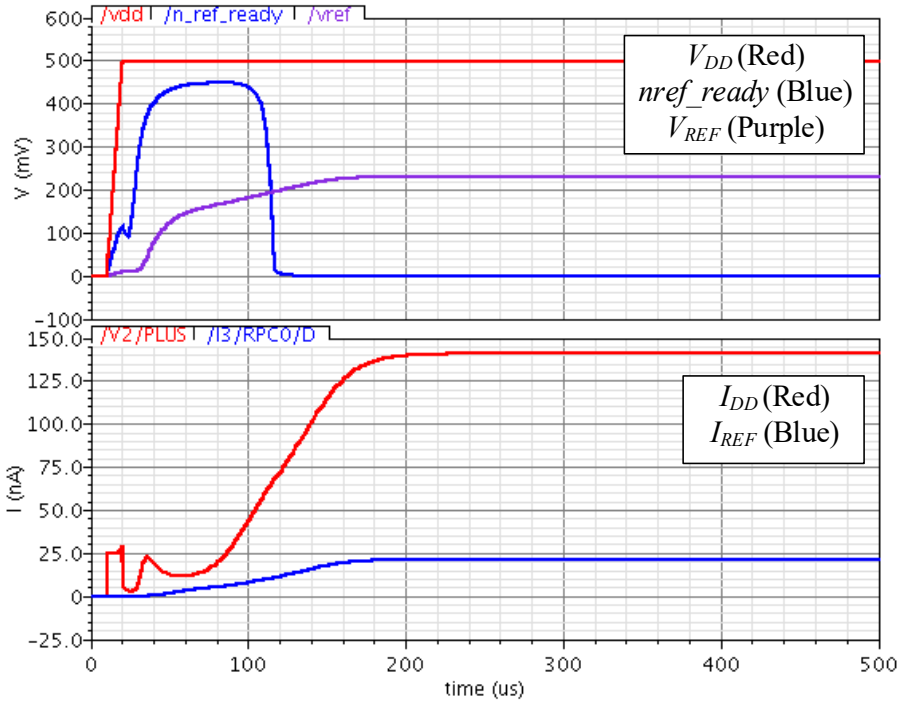


Figure 7.13 Transient response of the voltage reference when the supply voltage is risen from ground up to 500mV.

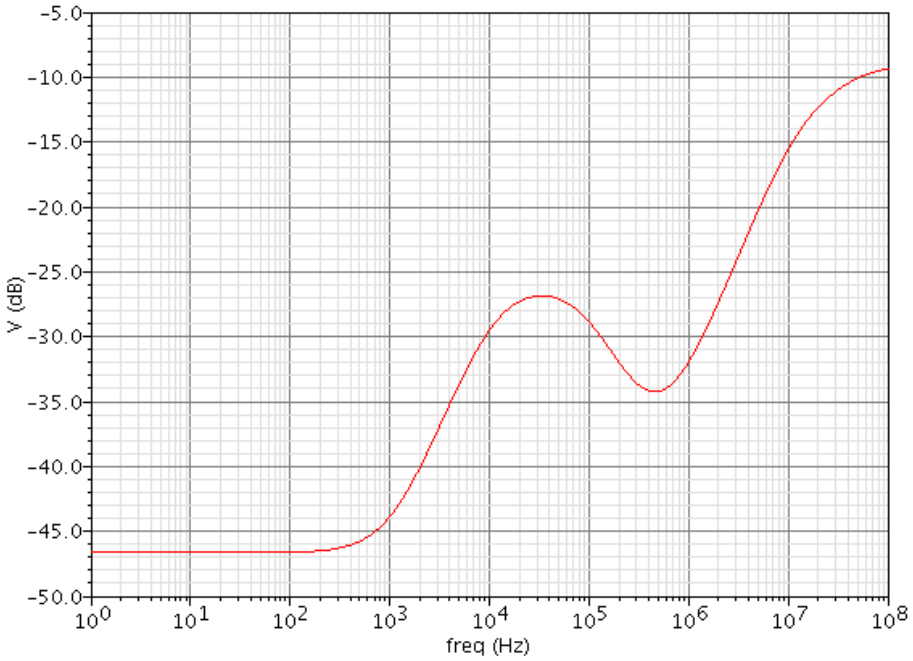
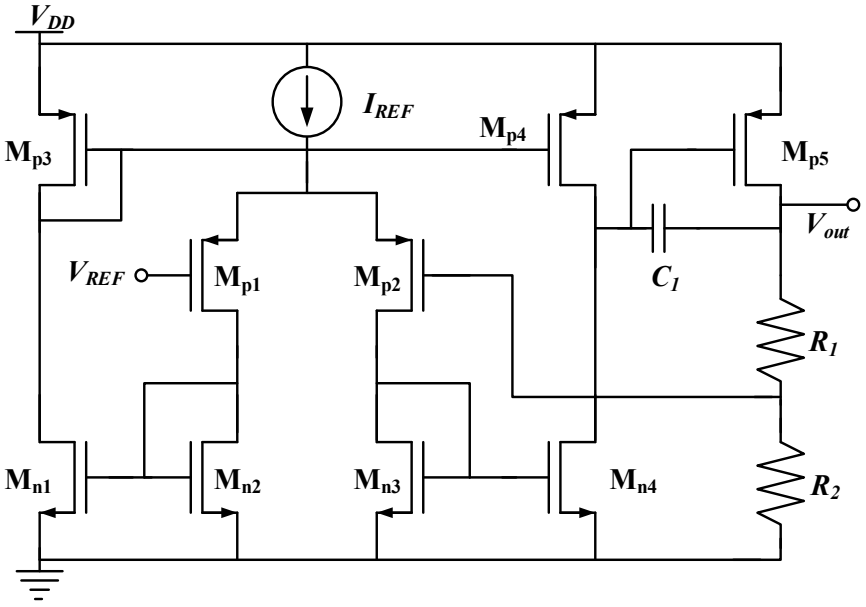


Figure 7.14 PSRR of the voltage reference.

Table 7.7 Corner simulation of the voltage reference.

Condition		$\boldsymbol{vref}$ **at** $\boldsymbol{VDD = 0.9}$ **V**	$\boldsymbol{iref}$ **at** $\boldsymbol{VDD = 0.9}$ **V**
Nominal	Temp. = -20°C	268 mV	17.58 nA
	Temp. = 0°C	253 mV	19.21 nA
	Temp. = 27°C	232 mV	21.5 nA
	Temp. = 80°C	189 mV	26.48 nA
Worst-case: Speed	Temp. = -20°C	296 mV	15.7 nA
	Temp. = 0°C	280 mV	17.17 nA
	Temp. = 27°C	259 mV	19.24 nA
	Temp. = 80°C	214 mV	23.65 nA
Worst-case: Power	Temp. = -20°C	250 mV	20.26 nA
	Temp. = 0°C	235 mV	22.15 nA
	Temp. = 27°C	214 mV	24.83 nA
	Temp. = 80°C	172 mV	30.59 nA

E.6 Voltage Regulator used in the PMU



(Voltage regulator circuit figure from Figure 4.33.)

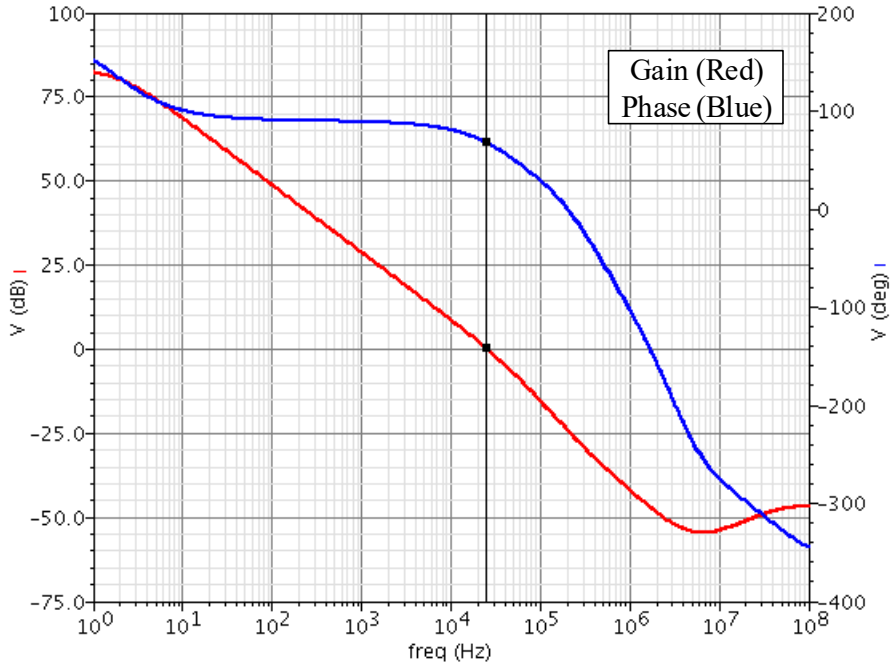


Figure 7.15 AC response of the voltage regulator at the light load condition when the supply voltage is 900mV.

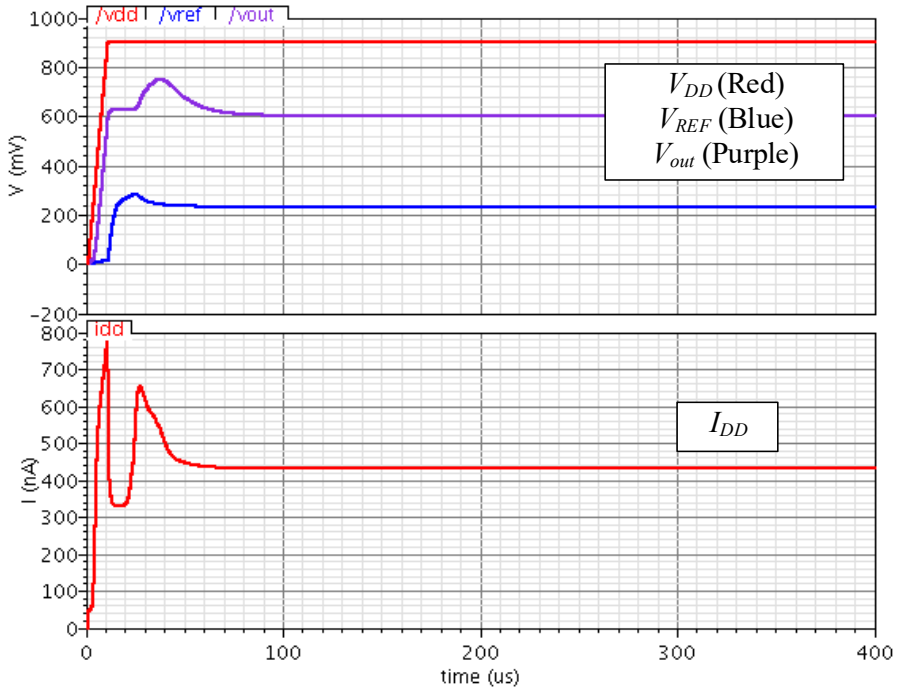


Figure 7.16 Transient response of the voltage regulator when supply voltage is increased from 0V to 900mV.

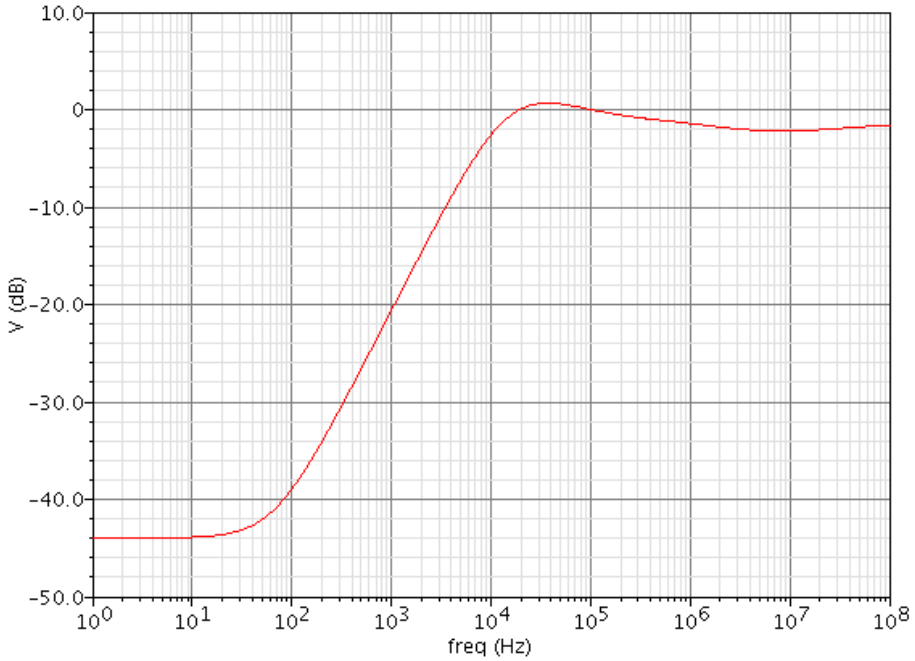


Figure 7.17 PSRR of the voltage regulator.

Table 7.8 Corner simulation of the voltage regulator when the supply voltage is 0.9V.

Condition		Output voltage	Phase margin
Nominal	Temp. = -20°C	696 mV	66.79 deg.
	Temp. = 0°C	657 mV	67 deg.
	Temp. = 27°C	603 mV	67.25 deg.
	Temp. = 80°C	491 mV	67.55 deg.
Worst-case: Speed	Temp. = -20°C	767 mV	67.72 deg.
	Temp. = 0°C	727 mV	67.93 deg.
	Temp. = 27°C	672 mV	68.17 deg.
	Temp. = 80°C	557 mV	68.52 deg.
Worst-case: Power	Temp. = -20°C	648 mV	65.75 deg.
	Temp. = 0°C	610 mV	65.97 deg.
	Temp. = 27°C	557 mV	66.22 deg.
	Temp. = 80°C	448 mV	66.43 deg.

E.7 DC-DC Charge Pump

Table 7.9 Corner simulation of the CP when the load is 5MΩ and the supply voltage is 0.9V.

Condition		Output voltage
Nominal	Temp. = -20°C	3.303 V
	Temp. = 0°C	3.293 V
	Temp. = 27°C	3.253 V
Worst-case: Speed	Temp. = 80°C	3.332 V
	Temp. = -20°C	3.321 V
	Temp. = 0°C	3.265 V
Worst-case: Power	Temp. = 27°C	3.263 V
	Temp. = 80°C	3.248 V
	Temp. = -20°C	3.179 V

E.8 Low and High Voltage Limiter Circuits used in PMU

In this section, the PVT corners simulation results of both low and high voltage limiter circuits are shown. A DC current source is applied to a 100kΩ resistor in parallel with the limiter circuit.

Table 7.10 Corner simulation of the low voltage limiter.

Condition		**Limited voltage**	**Current of the limiter when $V_{DD} = 1$ V**
Nominal	Temp. = -20°C	1.804 V	7.63 nA
	Temp. = 0°C	1.717 V	16.3 nA
	Temp. = 27°C	1.59 V	38.9 nA
	Temp. = 80°C	1.308 V	175 nA
Worst-case: Speed	Temp. = -20°C	1.947 V	3.11 nA
	Temp. = 0°C	1.859 V	7.19 nA
	Temp. = 27°C	1.732 V	19.1 nA
	Temp. = 80°C	1.451 V	91.6 nA
Worst-case: Power	Temp. = -20°C	1.701 V	15.5 nA
	Temp. = 0°C	1.615 V	30.6 nA
	Temp. = 27°C	1.49 V	67.1 nA
	Temp. = 80°C	1.209 V	307 nA

Table 7.11 Corner simulation of the high voltage limiter.

Condition		**Limited voltage**	**Current of the limiter when $V_{DD} = 3$ V**
Nominal	Temp. = -20°C	4.883 V	5.44 nA
	Temp. = 0°C	4.782 V	13 nA
	Temp. = 27°C	4.478 V	34.1 nA
	Temp. = 80°C	4.316 V	126 nA
Worst-case: Speed	Temp. = -20°C	4.478 V	1.72 nA
	Temp. = 0°C	4.378 V	4.56 nA
	Temp. = 27°C	4.233 V	14.1 nA
	Temp. = 80°C	3.913 V	71.8 nA
Worst-case: Power	Temp. = -20°C	5.205 V	33.9 nA
	Temp. = 0°C	5.108 V	62.2 nA
	Temp. = 27°C	4.966 V	117 nA
	Temp. = 80°C	4.654 V	271 nA

E.9 Simulated Power Consumption of the Prototype Energy Harvesting and Data Demodulator IC

Table 7.12 shows the average power consumption of the circuit building blocks of the data demodulator powered by a 600mV supply voltage in the nominal condition when the incoming frequency is 1MHz. It can be seen that the major power consumption is from the VCO. This is mainly because the VCO runs at four times the input frequency while most of the circuits run at lower frequency. The estimated total power consumption of the data demodulator system is approximately 0.8µW.

Table 7.12 Power consumption of the circuit building blocks tested at nominal condition where the power supply is 600mV.

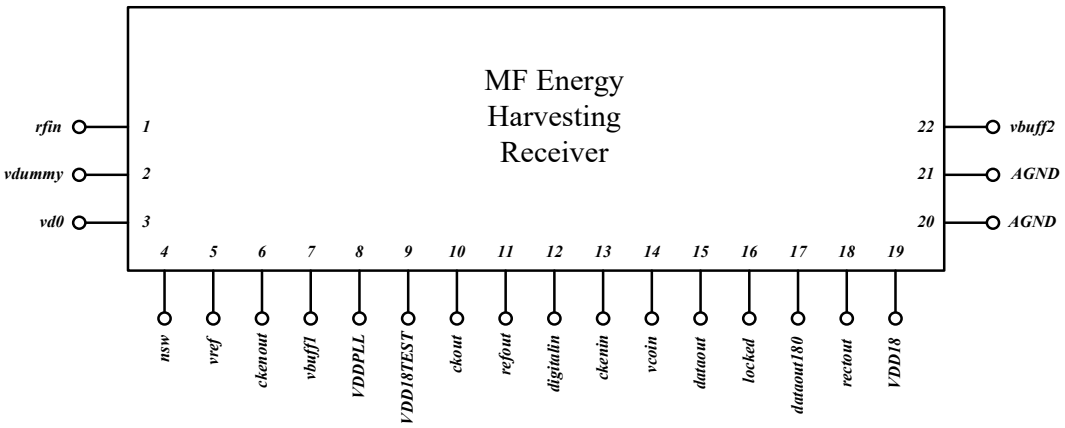
Circuit	Power consumption	Circuit	Power consumption
Amplifier	152.8nW	VCO	369nW
PFD	38.1nW	Charge pump	57.8nW
Hogge PD	60.31nW	Locked detection	48.2nW
Divide by four	44.26nW	Data detection	16.3nW

Table 7.13 summarises the power consumption of the PMU circuit building blocks tested at nominal condition where the power supply is 900mV for low voltage circuit at 3V for the limiter for high voltage. It can be seen that most of the circuits only consume few hundreds nW. On the other hand, the power consumption of the CP DC-DC charge pump from is as large as 4µW. However, the CP is only enabled in a certain period to reduce the average power consumption of the system. In addition, the total power consumption of the blocks in PMU excluding the CP is 691.37nW when the supply voltage is 900mV. Assuming the harvested power is 2µW, approximately 1.2µW is left for the data demodulator and the CP DC-DC charge pump.

Table 7.13 Power consumption of the circuit building blocks tested at nominal condition where the power supply (output from rectifier) is 900mV.

Circuit	**Current**	**Power**	**Circuit**		
Comparator	43nA	38.7nW	CP	-	4μW
Level detection	120nA	108.54nW	Limiter	38.86nA	34.97nW
Voltage reference	141nA	126.9nW	Limiter for high voltage (Tested at V_{DD} = 3V)	34.12nA	102.36nW
Voltage regulator	311nA	279.9nW			

E.10 IC Floor Plan of the Prototype Energy Harvesting and Data Demodulator IC



(IC pin diagram from Figure 4.38)

Table 7.14 Pin list of the IC.

Pin name	Type	Description	Pin name	Type	Description
VDD18TEST	Power	1V supply for digital testing buffers	vbuff1	Output	Regulator output
VDDPLL	Power	600 mV supply for control unit	vbuff2	Output	DC-DC converter output
VDD18	Power	Supply for ESD protection blocks	dataout	Output	Output data from the control unit
AGND	Power	Global ground	ckout	Output	Clock signal from the VCO
rfin	Input	RF input signal from the antenna	refout	Output	Reference clock from the control unit
rectout	Output	Rectifier output	vcoin	Output	Input voltage of the VCO
vd0	Output	Reference voltage from the main rectifier	locked	Output	Output from the locked detection
vdummy	Output	Reference voltage from the dummy rectifier	digitalin	Output	Output from the amplifier in the control unit
nsw	Output	Comparator output for controlling the rectifier	ckenin	Input	Control signal to enable the VCO
vref	Output	Reference voltage	dataout180	Output	Alternative output from the control unit
ckenout	Output	Output from level detection			

Appendix F Control Loop Design of the Data Demodulator

A block diagram of a conventional second-order PLL [59] shown in Figure 7.18 is used to design the proposed demodulator system shown in section 4.3.2 since the system initially operates in the PLL-mode when the input frequency is not yet locked. The frequency response of the system can be expressed as

$$H(s) = \frac{\frac{I_{CP}K_{VCO}}{2\pi C_{CP}}\left(R_{CP}C_{CP}s+1\right)}{s^2+\left(\frac{I_{CP}}{2\pi}\frac{K_{VCO}}{M}R_{CP}\right)s+\frac{I_{CP}}{2\pi C_P}\frac{K_{VCO}}{M}}, \quad (7.55)$$

when I_{CP} is the PLL charge pump current, R_{CP} and C_{CP} are the LPF resistance and capacitance respectively, K_{VCO} is the VCO gain defined by the ratio of the output frequency difference by input voltage difference and M is the dividing ratio of the frequency divider. Moreover the natural frequency, the damping factor and the loop bandwidth of the system are given by equations (7.56), (7.57) and (7.58) respectively.

$$\omega_n = \sqrt{\frac{I_{CP}}{2\pi C_{CP}}\frac{K_{VCO}}{M}}, \quad (7.56)$$

$$\zeta = \frac{R_{CP}}{2}\sqrt{\frac{I_{CP}C_{CP}K_{VCO}}{2\pi * M}}, \quad (7.57)$$

$$\omega_{-3dB}^2 = \left[\left(2\zeta^2+1\right)+\sqrt{\left(2\zeta^2+1\right)^2+1}\right]\omega_n^2, \quad (7.58)$$

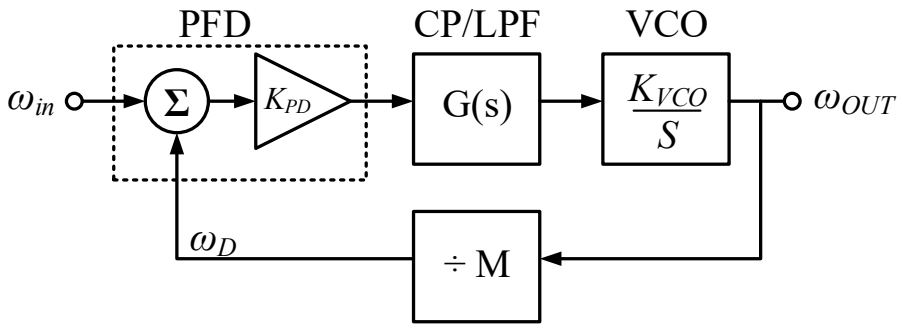


Figure 7.18 Block diagram of the demodulator shown in the frequency domain.

The design procedure can be described as follows:

1) Select the loop bandwidth ω_{-3dB} to be one-tenth or less of the input frequency.
2) Obtain the K_{VCO} from the design of the VCO.
3) Select a desired PLL charge pump current.
4) Calculate the PLL charge pump LPF from the equations by selecting the desired damping factor ζ.

The desired loop bandwidth of the system is selected and the parameters shown in the equations are calculated in order to design the data demodulator system.

Appendix G LC-tune Control Unit State Machine

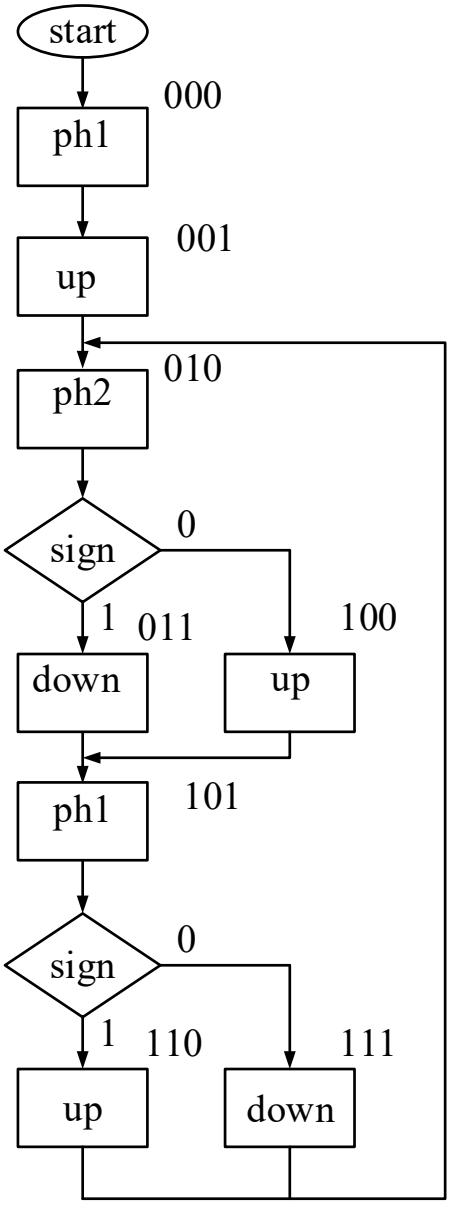
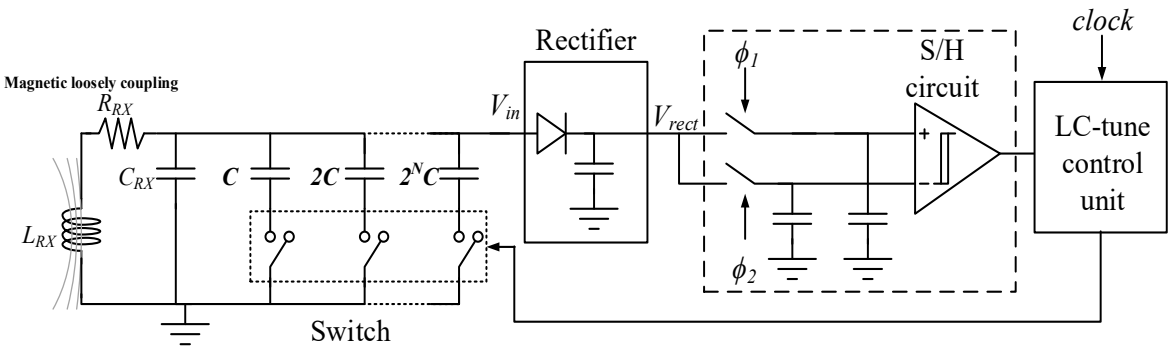


Figure 7.19 State machine of the LC-tune control unit. (Corresponding with Figure 6.14)



(LC-tune circuit from Figure 6.14.)

Appendix H Schematic Diagrams and IC Floor Plan Corresponding with Chapter 6

H.1 Sample-and-hold Circuit

Figure 7.20 shows the hysteresis sample-and-hold circuit where the comparator is implemented from the StrongARM latch comparator depicted in Figure 7.21. The hysteresis characteristic is added by changing the sampling capacitance of each comparator input according to the output result of the comparator.

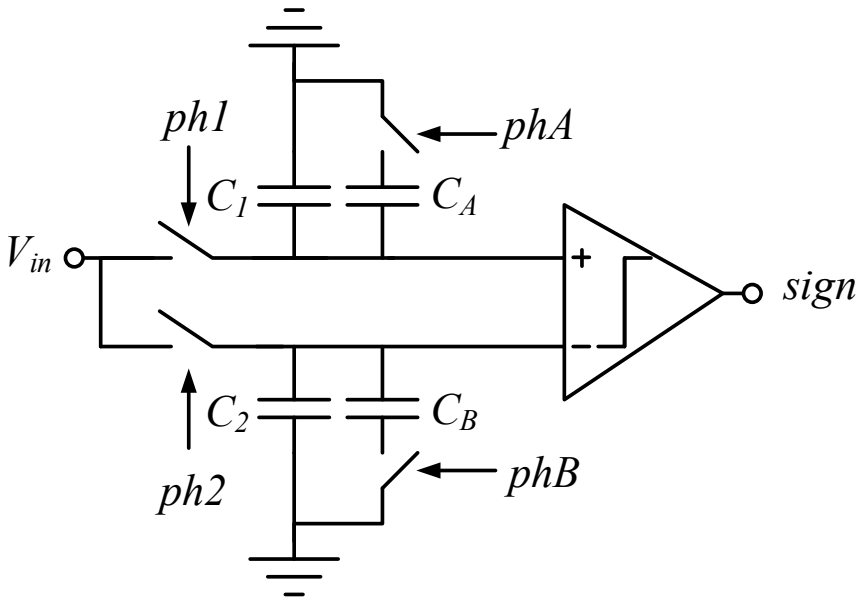


Figure 7.20 Sample-and-hold circuit. (Corresponding to Figure 6.5)

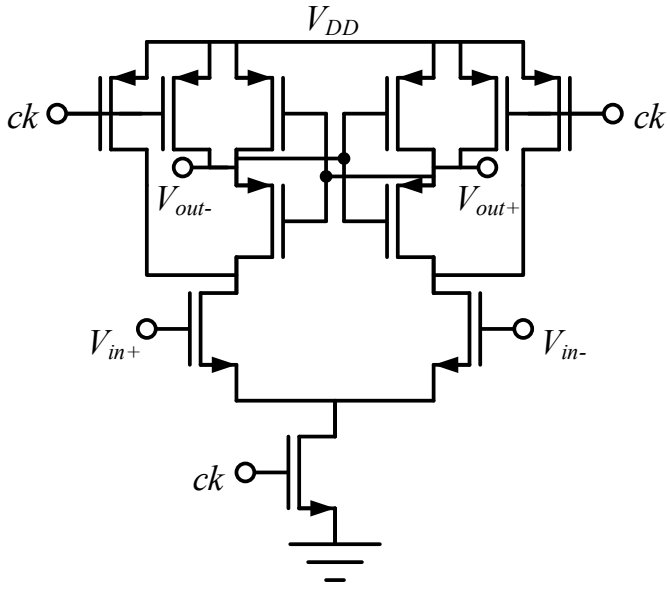


Figure 7.21 StrongARM comparator circuit. (Corresponding to Figure 6.5 and Figure 7.20)

H.2 RC Oscillator for control unit

Figure 7.22 illustrates the VCO for control unit implemented from a simple saw-tooth wave generator. The operating frequency is configurable by changing the reference current. As the system requires a very low operating frequency (typically at 100Hz), a divide by N is used to minimise the size of the capacitor used in this circuit.

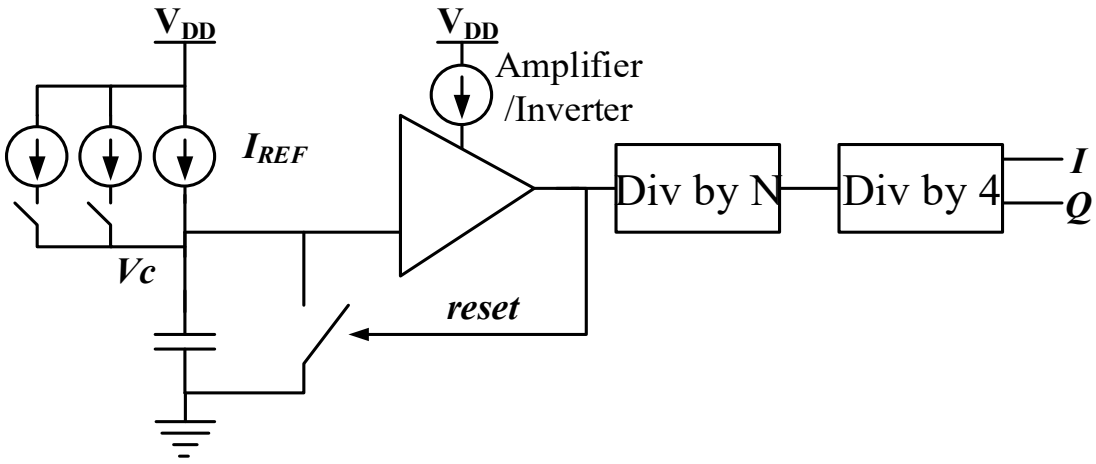


Figure 7.22 VCO for the control unit. (Corresponding to section 6.2 and 6.4)

H.3 Simulated Power Consumption of the Energy Harvesting and Data Demodulator Corresponding to Chapter 6

Figure 7.15 shows the simulated average power consumption of the circuit building blocks of the data demodulator powered by 600mV supply voltage in nominal condition when the incoming frequency is 1MHz. The estimated total power consumption of the data demodulator system is approximately 600nW.

Table 7.15 Power consumption of the circuit building blocks tested at nominal condition where the power supply is 600mV.

Circuit	Power consumption	Circuit	Power consumption
Amplifier	173nW	VCO	151nW
PFD	41nW	Charge pump	58nW
Hogge PD	73nW	Locked detection	50nW
Divide by four	44nW	Data detection	15nW

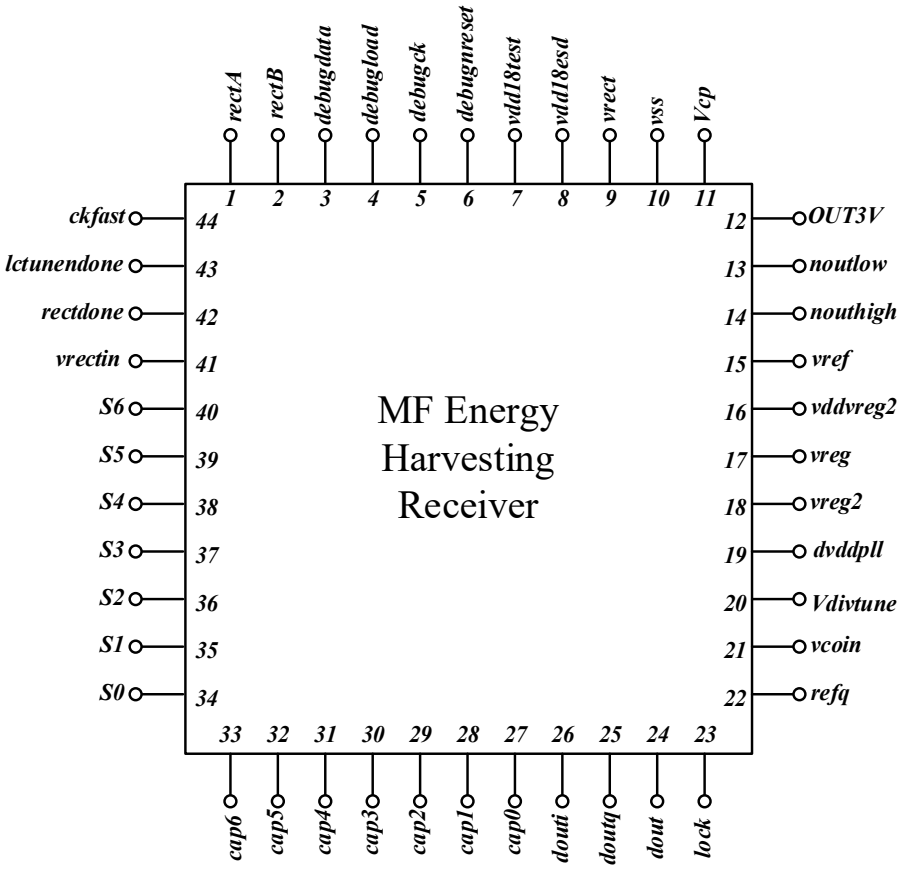
Figure 7.16 summarises the power consumption of the PMU circuit building blocks and the efficiency control unit tested at nominal condition where the power supply is 900mV for low voltage

circuit at 3V for the limiter for high voltage. The total power consumption of the blocks in PMU excluding the CP is 824nW when the supply voltage is 900mV.

Table 7.16 Power consumption of the circuit building blocks tested at nominal condition where the power supply (output from rectifier) is 900mV.

Circuit	Current	Power	Circuit	Current	Power
Low level detection	69nA	62nW	Efficiency control unit	167nA	150nW
3V level detection	11nA	10nW	CP	-	4µW
Voltage reference	141nA	127nW	Limiter	39nA	35nW
Voltage regulator	311nA	280nW	Limiter for high voltage (Tested at V_{DD} = 3V)	34nA	102nW

H.4 IC Floor Plan of the Energy Harvesting and Data Demodulator Corresponding to Chapter 6



(IC pin diagram from Figure 6.22)

Table 7.17 Pin list of the IC.

Pin name	Type	Description	Pin name	Type	Description
vdd18test	Power	1V supply for digital testing buffers	dvddpll	Power	Supply for data demodulator
vdd18esd	Power	Supply for ESD protection blocks	Vdivtune	Input	Demodulator N_{SS} configuration input
vrect	Output	Rectifier output	vcoin	Output	VCO input control voltage
vss	Power	Global ground	refq	Output	Demodulator reference clock
Vcp	Output	DC-DC CP output	lock	Output	Lock detection output
OUT3V	Output	Output from 3V level detection	dout	Output	Demodulator output data
noutlow	Output	Output from low voltage level detection	doutq	Output	
nouthigh	Output		douti	Output	
vref	Output	Reference voltage	lctunedone	Output	LC-tune enable signal
vddreg2	Power	Supply for secondary regulator	rectdone	Output	Rectifier configuration signal
vreg	Output	Regulator output	rectA	Output	
vreg2	Output	Regulator output	rectB	Output	
debugdata	Input	Debug pins for digital control unit configuration	vrectin	Input	RF input signal from the antenna
debugload	Input		ckfast	Output	Efficiency tracker clock
debugck	Input		S0-S6	I/O	LC-tune control signals
debugnreset	Input		cap0-cap6	I/O	Capacitors for LC-tuning

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