UNIVERSITY OF SOUTHAMPTON
FACULTY OF PHYSICAL SCIENCES AND ENGINEERING
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Iterative Initial Synchronization in Wireless Communications

by

Abbas Ahmed
B.E.E, M.Sc

A doctoral thesis submitted in partial fulfillment of the
requirements for the award of Doctor of Philosophy
at the University of Southampton

March 2019

SUPERVISORS:
Prof. Lajos Hanzo
FREng, FIEEE, FIEE, DSc, RS Wolfson Fellow
Chair of Southampton Wireless Group
and
Prof. Lie-Liang Yang
BEng, MEng, PhD, FIET, FIEEE
Professor
and
Dr. SeungHwan Won
BSc, MSc, PhD
Associate Professor
School of Electronics and Computer Science
University of Southampton
Southampton SO17 1BJ
United Kingdom

Dedicated to my parents, my loving wife, my adorable son, my charming daughter and my all family members, and to all of those less fortunate people of my homeland for the betterment of whom I am expected to work after I complete my education in this university.

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

Iterative Initial Synchronization in Wireless Communications

by Abbas Ahmed

The family of m-sequences has been widely used for the initial synchronization of generations of wireless systems. We exploit the fact that R chips uniquely and unambiguously determine the entire $(2^R - 1)$ chips of a sequence by designing a Soft-In-Soft-Out (SISO) Recursive Soft Sequence Estimation (RSSE) scheme, relying on similar iterative processing techniques to those of turbo decoders. To elaborate a little further, once R chips have been received, the RSSE scheme augments the soft *intrinsic* information gleaned from the channel with the aid of the extrinsic information constituted by the previous received chips. Hence, these turbo iterations substantially improve the initial synchronization performance attained.

The scheme advocated is then used for investigating the performance of a large variety of m-sequences as well as of the family of concatenated sequences, which can be generated with the aid of a pair of m-sequences. These concatenated sequences have substantial benefits over the m-sequences. We continued our investigations by tabulating the most attractive m-sequences and concatenated sequences having a large variety of different lengths. The convergence properties of our RSSE schemes were investigated with the aid of *EXtrinsic Information Transfer* (EXIT) charts. Finally, as a further refinement we introduced an Automatic Gain Control (AGC) scheme into our RSSE arrangements, which substantially improved its performance.

Declaration of Authorship

I, **Abbas Ahmed**, declare that the thesis entitled **Iterative Initial Synchronization in Wireless Communications** and the work presented in it are my own and has been generated by me as the result of my own original research. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University;
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- Where I have consulted the published work of others, this is always clearly attributed;
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- Parts of this work have been published as: [1, 2].

Signed: ..... Date: .....

Acknowledgements

Praising and Thanking are due to His Almighty Allah, who, in his infinite mercy, helped me to finish my work. He blessed me with unlimited bounties. One of these bounties, in the period I spent in preparing this work, is to honor me to work under the supervision of Professor Lajos Hanzo who provided me with the real atmosphere a student needs to pursue a successful research. His ideas, style of supervision, invaluable advice, encouraging and caring attitude played a substantial role in completing the work. I also take this opportunity to thank my second supervisor Professor Lie-Liang Yang for his scientific and moral support throughout the period I spent in the department and am also grateful to Dr. SeungHwan Won, my third supervisor for his countless suggestions and inexhaustible enthusiasm towards this work. The dedication of these supervisors in facilitating me most of the time during the *learning curve* to become a good researcher, with all technical help that I needed is highly acknowledged. Their determination and focus will always inspire me. I would not have been able to accomplish this formidable task without their guidance, patience, stimulation and assistance upon the work. Additionally, I am grateful to Professor Sheng Chen, Dr. Rob Maunder, Dr. Soon Xin Ng and Dr. Mohammed El-Hajjar for the useful discussions and suggestions throughout my research.

I also extend my gratitude to all my colleagues at Southampton for their continuous support and inspiration. I found an excellent environment for research, especially with Dr. Zunaira Babar, Dr. Panagiotis Botsinis, Dr. Ismiat Kadir, Dr. Shurti Gupta, Dr. Dimitrios Alanis, Dr. Rakshith Rajashekar and Mr. Daryus Chandra for many meaningful discussions that we had. Most of all, it has been a pleasure to be part of this research group and being here since 2015, I always regard Southampton as the place where I grew up.

My family has played an important role in ensuring that everything went smoothly with the help of Allah. I wish to express all my gratitude to my family members for their unconditional love and encouragement, as well as incredible non-technical support that they provided-there are no words that can describe their *behind-the-scene* effort in helping me-in many ways. I am deeply grateful for their understanding and patience in my quest to seek knowledge. To my dearest parents, I thank you for the hard work in raising me during the early years of my life, together with the guidance and wisdom to be what I am today. I am also very grateful to them for their financial support which they did during my life. A very special thanks to my

beloved wife, for sharing this wonderful life with me *through thick and thin*. I also appreciate my son and daughter for being a constant source of joy and bearing me through out this time. I would thank my brother, sister and my in-laws which are always there when I needed them.

Finally, I wish to thank every single one who has taught and guide me in my life to become what I am today. I hope after completing my studies I can help to rebuild my nation.

List of Publications

1. **A. Ahmed**, P. Botsinis, S.Won, L. L. Yang and L. Hanzo, "EXIT Chart aided convergence analysis of recursive soft m-sequence estimation in Nakagami-m fading channel," *IEEE Transactions on Vehicular Technology*, vol. 67, pp. 4655–4660, Jan. 2018. DOI:10.1109/TVT.2018.2789912.

2. **A. Ahmed**, P. Botsinis, S.Won, L. L. Yang and L. Hanzo, "Primitive Polynomials for Iterative Recursive Soft Sequential Acquistion of Concatenated Sequences," *IEEE Access*, vol. 3, pp. 1704–1728, 2018. DOI: 10.1109/ACCESS.2015.2478793.

3. **A. Ahmed**, I. Kadir, S.Won, L. L. Yang and L. Hanzo, "Iterative Soft Sequential Acquisition for Primitive Polynomials utilizing Automatic Gain Controller (AGC) ," *to be submitted in IEEE Access*

4. **A. Ahmed**, I. Kadir, S.Won, L. L. Yang and L. Hanzo, "Fast Frequency Hopping system in mm-Wave using Hybrid technology," *in preparation*

Contents

List of Symbols

'b'	bit stream
bps	bits per symbol
c_i	Corresponding chips of the first m-sequence generator
d_i	Corresponding chips of other m-sequence generator
DL	Downlink
e_i	output of concatenated sequence
I_A	*apriori* Information
I_E	*Extrinsic* Information
dB	Decibel
E_c	The transmitted chip energy
$f(t)$	the original input signal
$f(t-\tau)$	the delay of the original input signal
$g(X)$	primitive polynomial
GP	Generated Polynomial
N_0	Noise Spectral Density
$N_{\tau D}$	Mean Acquisition Time
P_e	Erroneous Loading Probability
PP	Primitive Polynomial
R	R Consecutive chips

R_{max}	the ratio between the peak magnitude of the cross correlation function
R_0	the peak value of the autocorrelation function
S	S consecutive chips
SNR	Signal to Noise Ratio
η	Nano seconds
T	Time Period
τ_D	Dwell time
τ	Lags
UL	UpLink
y_i	Received Signal
z_i	Output signal from SISO decoder
α	fading channel
β	Gain of Amplifier
$\in$	belongs to
L_a	LLR-value obeying Gaussian distribution
L_e	the extrinsic values of LLR
$P_A(\chi\|X)$	is the conditional PDF
X_i	transmitted signal
$P(X_i)$	probability of X_i
KHz	Kilo Hertz
MHz	MegaHertz
μ	micro

List of Acronyms

1G	The First Generation
2G	The Second Generation
3G	The Third Generation
4G	The Forth Generation
5G	5^{th} Generation
3GPP	3^{rd} Generation Partnership Project
ACF	Auto-Correlation Function
AGC	Automatic Gain Controller
AMPS	Advanced Mobile Phone Systems
AMI	Average Mutual Information
AT	Acquisition Time
AWGN	Additive White Gaussian Noise
BCH	Bose Chaudhuri Hocquengem
BER	Bit Error Ratio
BPSK	Binary Phase Shift Keying
BPF	Band Pass Filter
BS	Base Station
CCF	Cross Correlation Function
CDMA	Code Division Multiple Access
CDMA-2000	Code Division Multiple Access-2000

DL	Downlink
DS	Direct Sequence
DwPTS	Downlink Pilot Time Slot
DRSSE	Differential Recursive Soft Sequential Estimation
DS-CDMA	Direct Sequence Code Division Multiple Access
DS-UWB	Direct Sequence Ultra Wide Band
EDGE	Enhanced Data for Global System for Mobile Communication Evolution
eMBB	Enhanced Mobile BroadBand
ETSI	European Telecommunication Standards Institutes
EXIT	EXtrinsic Information Transfer
FDD	Frequency-Division Duplex
FDMA	Frequency Division Multiple Access
FH	Frequency Hopping
FM	Frequency Modulation
F-SYNC	Forward Synchronization Channel
F-PICH	Forward Common Pilot channel
GMSK	Gaussian Minimum-Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HSPA	High Speed Packet Access
IS	Interim Standard
ISDN	Integrated Services for Digital Network
ISI	Inter-Symbol-Interference
ITU	International Telecommunication Union
LFSR	Linear Feedback Shift Registers
LPF	Low Pass Filter

LLRs	Log-Likelihood Ratios
LO	Local Oscillator
LTE	Long Term Evolution
MAI	Multi Access Interference
MC-CDMA	Multi Carrier Code Division Multiple Access
MF	Match Filtering
MI	Mutual Information
MIMO	Multi Input Multi Output
MLD	Majority Logic Decoder
mm-Wave	Milli-Meter-Wave
MMTC	Massive Machine Type Communications
MS	Mobile Station
NOMA	Non-Orthogonal Multiple Access
NR	New Radio
OFDM	Orthogonal Frequency Division Modulation
OFDMA	Orthogonal Frequency Division Multiple Access
OVSF	Orthogonal Variable Spreading Factor
PA	Power Amplifier
PAPR	Peak to Average Power Ratio
PC	Pilot Channel
PDAs	Personal Digital Assistants
PN	Pseudo-Noise
PPs	Primitive Polynomials
PTL	Phase-Tracking Loop
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RASE	Rapid Acquisition Sequential Estimation
RF	Radio Frequency

RRC	Radio Resource Control
RSSE	Recursive Soft Sequential Estimation
SC-FDMA	Single Carrier Frequency Division Multiple Access
SCR	Soft-Chip Register
SCDUs	Soft-Chip-Delay-Units
SF	Spreading Factor
SISO	Soft-In-Soft-Out
SS	Spread-Spectrum
Sync	Synchronization channel
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division Synchronous Code Division Multiple Access
TIA	Telecommunication Industry Associations
TL	Tracking Loop
UE	User Equipment
UTC	Universal Time Coordinated
UL	UpLink
UWB	Ultra Wide Band
WCDMA	Wideband Code Division Multiplexing Access
WiFi	Wireless Network
WiMAX	World wide Interoperability for Microwave Access
XOR	Exclusive OR gate

Chapter 1

Introduction

1.1 Introduction

Wireless mobile communications have evolved from the first generation voice-only-systems to the second, third, fourth and fifth generation of cellular communication networks. Wireless mobile communication have seen an exponential growth in the last two decades and proven to be an unprecedented success story. No other technology has managed to support Billions of users, but hence the radio spectrum is becoming saturated [3, 4, 5, 6, 7]. This revolution has witnessed the introduction of digital modulations schemes, cellular reuse of frequency[1], and of physical layer technologies such as Code Division Multiple Access (CDMA), Wideband Code Division Multiplexing Access (WCDMA) Multi Input Multi output (MIMO) schemes, Orthogonal Frequency Division Multiple Access (OFDMA) etc. which have significantly contributed towards increasing the capacity of the networks [8,9,10,11]. *Initial synchronization* is a process, which is required whenever the Mobile Station (MS) is *turned on* [6, 12]. This chapter provides a rudimentary introduction of the wireless generations spanning from 1G to 5G.

1.2 History of the Wireless Generations

Each generation's technology evolved by invoking new innovations, as illustrated in Fig. 1.1.

1.2.1 First Generation (1G)

The concept of *frequency reuse* and *cell planning* was first exploited by the First Generation (1G) systems, such as the British Advanced Mobile Phone System (AMP) [13,

[1] frequency reuse

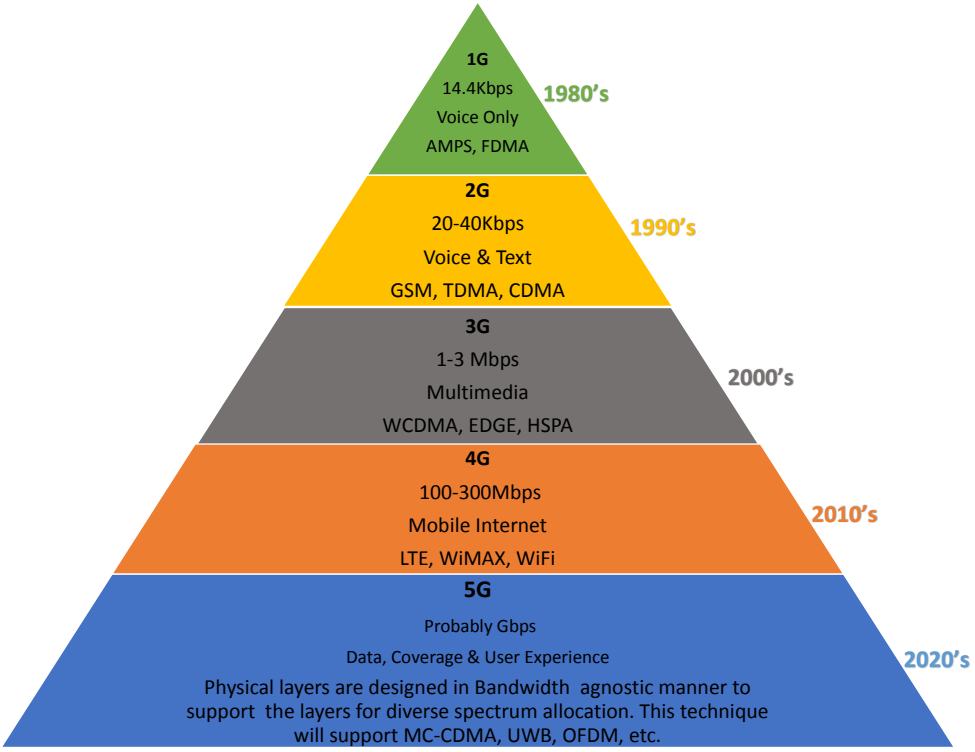


Figure 1.1: Evolution of cellular communication systems.

14]. This technology relied on Frequency Division Multiple Access (FDMA), Frequency-Division Duplex (FDD), Frequency modulation (FM) and supported cellular traffic in slots of 15 KHz per link [15, 16, 17]. *Carrier phase synchronization* was essential for this technology having a *spectrum efficiency* of 0.33 bits per symbol (bps) [15, 18, 19, 20].

1.2.2 Second Generation (2G)

This cellular generation was dominated by the Global System of Mobile Communication (GSM), which was one of the *first digital mobile systems* that relied on the concept of *pure circuit switched technology* known as Integrated Services for Digital Network (ISDN) [21, 22, 23]. The GSM model used the Time Division Multiple Access (TDMA), Frequency Division Duplex (FDD) and Gaussian Minimum-Shift Keying (GMSK) to support a better *voice communication* [12, 18, 19]. This scheme utilized oversampling for acquiring the timing synchronization [4, 16, 24, 25]. Furthermore in this era *error correction codes*, symbol *timing synchronization* and *adaptive equalization* techniques were adopted for mitigating the hostile fading and dispersion effects [24, 26].

1.2.3 Third Generation (3G)

The *first* commercial CDMA system was the Pan-American Interim Standard (IS)-95 system, which relied on 64-chip *orthogonal Walsh-Hadamard spreading sequences* [22, 27, 28, 29, 30]. In this era rapid advances were made in *adaptive modulation* and *coding*, which were combined with the compelling benefits of the *CDMA principles* demonstrated by the IS-95 system, which then exploited in the conception of the 3G system [10, 31, 32, 33]. This system is the *first one* utilizing the Orthogonal Variable Spreading Factor (OVSF) codes, where the Spreading Factor (SF) was adjusted according to the User's *bit rate requirement* and the channel quality [34, 35, 36]. For example, in Wideband Code Division Multiple Access (WCDMA) the OVSF code have *spreading factors* spanning from 4 to 512 [37, 38, 39] whereas in Time Division Synchronous Code Division Multiple Access (TD-SCDMA) the OVSF code are used in lies from 1 to 16 [37, 38, 39].

1.2.4 Fourth Generation (4G)

This technology was *designed* and *developed* by 3^{rd} Generation Partnership Project (3GPP) as the *air interface* for 4^{th} generation cellular mobile communication systems [40, 41]. Long Term Evolution (LTE) employs a channel bandwidth of upto 20 MHz to have a *maximum subcarriers* of 2048, OFDMA on the Downlink (DL) and Single Carrier FDMA (SC-FDMA) on the UpLink (UL) transmission.

1.2.5 Fifth Generation (5G)

Given the success of the 4G Multi-Carrier (MC) OFDMA solution, all the 5G proposals were *centered* on *MC principles*. A new feature is the introduction of the Non-Orthogonal Multiple Access (NOMA) principle in the interest of improving the attainable *throughput* at the cost of using *increased-complexity* receivers for eliminating the *extra interference* imposed [8, 42, 43]. This is in start contrast to the previous four generations, where the orthogonal FDMA, TDMA, CDMA and OFDMA principles where used. As the services to be supported became more sophisticated, *three* main operational modes were designed, namely the Enhanced Mobile Broad-Band (eMBB), ultra-reliable low latency communications and Massive Machine Type Communications (MMTC) [44, 45].

1.3 Motivation

The standard bodies of telecommunication industries such as International Telecommunication Union (ITU), European Telecommunication Standards Institutes (ETSI) and Telecommunication Industry Associations (TIA) set the principles for synchro-

nization which have been adopted since the emerge of 1G till now [46, 47, 48, 49]. For the sake of illustration the MS receiver must be capable of coarsely synchronously aligning a locally generated Pseudo-Noise (PN) code with the received composite multi-user signal containing the desired user PN sequence before transmitting the desired signal [26, 28, 50, 51]. This methodology is known as '*Initial Acquisition*', which is been followed by *optimum post-initial acquisition*[2] [16, 25, 40, 42, 52]. To achieve correct code initial synchronization, we need to adopt *two* consecutive steps, namely the *coarse alignment* for the code which is done *initially* and other is to acquire the *fine alignment* of the *phase code* which is done by the phase tracking system as illustrated in [13,16,53,54]. We focus our attention on initial code acquisition in this thesis. In wireless communication, initial acquisition is needed for both the *coarse timing* as well as for the *code phase alignment*, thus creating the challenging problems for the researcher due to their *short signalling chip-duration* [55,56,57,58]. This leads to a huge code-phase and timing- search space size, which is represented as the product of the number of *legitimate code phases* in the uncertainty region of the PN code and the number of legitimate signalling pulse positions [53, 59, 58]. For the sake of significantly reducing the *search space size*, we will investigate the *recursive soft sequential estimation* algorithm designed for the m- and the Concatenated-sequences assisted by the EXtrinsic Information Transfer (EXIT) scenario, which constitutes the main objective of this thesis.

Once synchronization has been established, the data can be demodulated [53,59]. The m-sequences are normally used for spreading information, but in the context of initial synchronization they are not used for spreading information bits, but rather for aiding the initial synchronization between the BS and a User Equipment (UE) [60,61, 62]. They are adopted because of their cyclic nature [16, 62, 63, 64]. Furthermore, it can be explain in more depth as in IS-95 and CDMA 2000, the code acquisition in the downlink is achieved by sending an *unmodulated pilot signal* over the *pilot channel*. The pilot channel is intended to provide a *reference signal* for all the MS within a cell and is always transmitted by the BS on each *active* Forward CDMA Channel [4, 65]. It is about 4-6 dB stronger than all other channels [4, 63, 64, 65]. The pilot channel is used for locking onto all the other logical channels [4, 24, 26, 28, 50, 65, 66]. The pilot channel uses the all *zero* Walsh code and contains *no information* except the RF carrier in IS-95. Therefore, the pilot signal is an *unmodulated spread spectrum* signal (as it is multiplied by an all zero Walsh code) which is then spread according to the *chip rate* of the sequence [4, 24, 29, 51, 66] as shown in Fig. 1.2. No data modulation is performed on this part of the transmission, as mentioned in [16, 30, 67].

In IS-95 [4, 26, 29, 50, 51, 66], the forward channel consists of *four types* of logical channels, i.e Pilot channel (PC), synchronization channel, paging channel and traffic channel as shown in Fig. 1.3. Each carrier contains a pilot channel, a synchronization

[2] to identifying the timing instants of the affordable-complexity-dependent number of delayed received signal paths, which are combined by the receiver

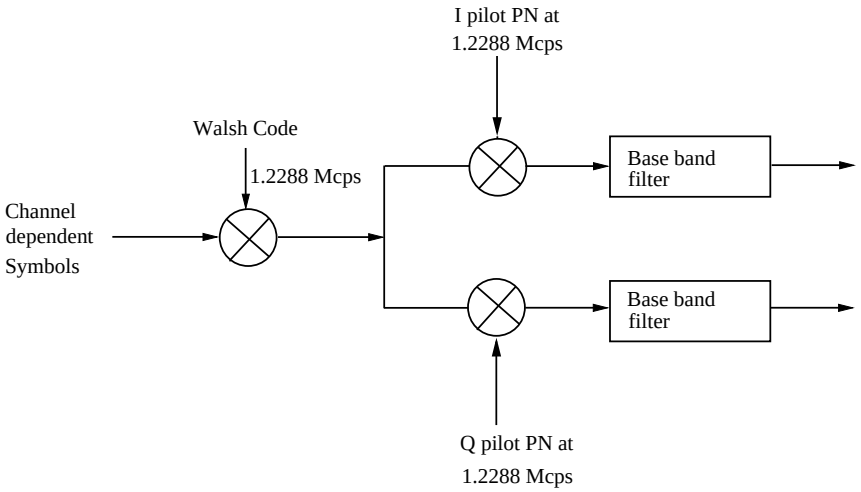


Figure 1.2: Pilot Channel in IS-95 [24, 50, 66].

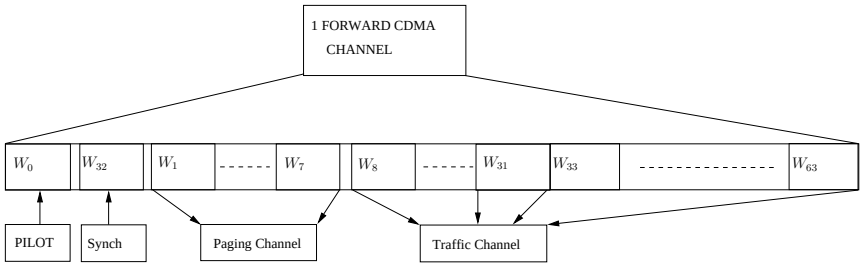


Figure 1.3: Forward Channel in IS-95, Forward Channel in IS-95, where the Walsh channels W_1 to W_7 are used for paging channels. W_{32} is the synchronization channel, while the traffic channels are W_8 to W_{31} and W_{33} to W_{63} [50, 65, 66].

channel, upto *seven* paging channels and traffic channels [16, 25, 40]. These channels are separated from one another using *different spreading codes* [4, 68, 69]. The information contained in the form of symbols are modulated by Walsh code [24, 26, 51]. Each Walsh code identifies one of the 64 forward channels. After the forward symbols are spread using orthogonal codes, they are further scrambled in the in-phase and quadrature-phase by the short PN-codes [24, 26, 28, 29] as shown in Fig. 1.3. These PN codes are formed by Linear Feedback Shift Registers (LFSR) having length 15 with a period of 32768 chips [24, 26, 28, 29].

The Walsh codes are used for *isolating* the transmissions between *different channels* within a cell [4, 68, 69]. The PN spreading codes are used for *separating the transmissions* between different cells [26, 28, 29]. The synchronization PN sequences are used for *differentiating* between several BSs in the areas that are all employing the same frequency [4, 68, 69]. The BSs have to be synchronized on the downlink by using the Global Positioning Systems (GPS) [4, 24, 26, 28, 50, 65, 66]. The downlink of IS-95 consists of *two categories* of channels, the common control channel and the traffic channel [24, 26, 28, 29, 50, 51, 65]. The common control channel consists of

three parts namely, the PC, the paging channel and the Synchronization (Sync) channel [24, 28, 50, 65]. The reverse traffic channel sends information to the BS related to the signal strength of the pilot signal and the frame error rate statistics [50, 65]. An MS uses the PC for coherent demodulation, acquisition, time delay tracking, power control measurements and as an aid for the handover [55, 56, 57]. In order to obtain a reliable phase reference for coherent demodulation, the PC is transmitted with higher power than the traffic channel [24, 26, 51]. After obtaining phase and code synchronization, the MS acquires the synchronization information from the synchronization channel [16, 24, 25, 40, 57]. Since the synchronization *frame* has the same length as the *pilot sequence*, the acquisition of the synchronization channel is possible [70, 71, 72]. The synchronization channel runs at a fixed rate of 1.2 $Kbps$. In the downlink *three types* of spreading codes are used [53, 59]. More specifically Walsh codes of length 64 at a fixed chip rate of $1.2288 Mcps$ separate the physical channels. A pair of long m-sequences of length $2^{15} - 1 = 32767$ chips is used for quadrature spreading [24, 29, 50]. Since the PC Walsh function is *all zeros*, this pair of m-sequences also forms the *pilot code* [16, 25, 28, 50, 65]. Different cells and sectors are distinguished with different phase offsets of this code [55, 56, 57]. A long PN sequence with a period of $2^{42} - 1$ is used for the base band data scrambling. It is decimated from a 1.2288 $Mcps$ rate down to $19.2 Kbps$ [4, 24, 29, 50]. The long PN sequence is used in the uplink for user *separation* and is generated by a modulo-2 inner product of a 42-bit state vector of the sequence generator [37, 38, 39, 60].

In CDMA-2000 [31, 73], the acquisition occurs as follows. When the mobile phone is turned on, the IS-2000 compatible terminal directly looks for a PC or Forward Common Pilot channel (F-PICH) [31, 74, 75]. The PC is a channel continuously transmitted by all CDMA-2000 compliant BS, consisting of a constant value of one [31, 73], scrambled by the *short complex* PN sequence. The PC is used for acquisition, for various tracking loops and as a reference for coherently demodulating the other forward channels [31, 74, 75]. Each BS transmitter scrambles all the forward link channels with a different offset relative to the Universal Time Coordinated (UTC) [76, 77, 78, 79]. This offset is refereed to as the *PN offset* and represents the *BS identity* amongst the neighbor BS. The number of *different PN offsets* in the system is limited to 512, therefore PN offsets are reused within a communication network [80, 81]. Once at least *one pilot signal* has been successfully acquired, the terminal locks to the strongest available PC [6, 80, 81, 82, 83]. At the time, it does not have a *time reference*, and since the PC signal is always the same, it does not know the *system parameters*, nor does it know whether it is allowed to operate with the *associated network* [84, 85, 86, 87, 88, 89]. In order to acquire all the information the terminal attempts to decode the Forward Synchronization Channel (F-SYNC) [28, 31, 75]. The F-SYNC channel rolls over every 2^{15} chips or 26.67 msec and is synchronized with the PC. In CDMA-2000 the signal transmitted by the terminal on the *reverse link* always includes a reference signal by Reverse Pilot Channel (RPC) [31, 73, 74]. The PC consists of a *continuous DC signal* (before scrambling) which is used as the *refer-*

ence signal for searching, tracking, measurement and coherent demodulation at the BS [26, 28, 50, 65].

However, in the case of the specific code acquisition problem related to the m- and concatenated- sequences, the state of a register stage is transmitted, instead of the bit of a conventional m-and concatenated-sequences [1, 2, 50, 90, 91, 92]. This is done so that the receiver may lock on to the correct states of each register stage after a minimum of R transmissions, where R is the number of registers stages, instead of 2^R transmissions, which would have been required if an m-sequence was transmitted [1, 2, 50, 90, 91, 92]. Therefore, in our design the transmitted bits are the states of the first register stage of the m-sequence and they do not spread information bits. Based on the proposed approach, we are able to acquire the current state of the m-sequence generator at the transmitter and load the phase tracking loop from that point onwards. Therefore, transmitting the feedback chip sequence is sufficient. This way, the iterative decoding process may be faster than waiting till $(2^R - 1)$ chips have been received completed. In the context of sequential estimation-based acquisition used for short m-sequences, the generator's state can be principally estimated using iterative decoding techniques, since each m-sequence produced by an 'R'-stage generator has a period of $(2^R - 1)$ chips, and can be considered to be a cyclic Bose Chaudhuri Hocquengem (BCH) codeword of length $(2^R - 1)$, having minimum distance of $(2^R - 1)$ [93, 94].

In our case the m-sequence generator, the feedback elements are duo-binary values, and the product of these feedback elements is used for generating a binary feedback quantity. In the context of the sequential estimation-based acquisition used for short m-sequences, the generator's state can be principally estimated using iterative decoding techniques, since each m-sequence produced by an 'R'-stage generator has a period of $(2^R - 1)$ chips, and can be considered to be a cyclic BCH codeword of length $(2^R - 1)$, having minimum distance of $(2^R - 1)$ [93,94]. Note that both the m-sequence generator and the soft-chip register use the same feedback branches [1, 2, 50]. Hence, in the m-sequence generator, the feedback elements are duo-binary values, and the product of these feedback elements is used for generating a binary feedback quantity. After the receiver obtained two sets of $2 \times (2^R - 1)$ number of consecutive samples of the transmitted m-sequence, the m-sequence generator's initial state of R chips is estimated by iteratively decoding the received m-sequence with the aid of its number of samples. By contrast, the feedback elements from the soft-chip register to the SISO decoder consist of the LLR values, and the specific operations must be employed in the soft-value domain to provide extrinsic information for the SISO decoding [1, 2, 50, 95, 96]. In both the Code Division Multiple Access-2000 (CDMA-2000) and IS-95 standards different number of m-sequences have been used [14,53,65]. Based on this accumulated experience, m-sequences have also found their way into the 5^{th} Generation (5G) standards for initial synchronization [97, 98, 99, 100, 101].

1.4 Novel Contributions

The novel contributions of this thesis are summarized below:

(a) We have conceived the *Recursive Soft Sequential Estimation scheme* (RSSE), which operates on the principle of *Soft In Soft Out* (SISO) iterations, for improving the reliabilities associated with the decision criteria of R consecutive chips. The recursive SISO decoder receives soft information from the channel's *current* output, thus soft extrinsic information from the soft channel output associated with the *previous chips*, provided by the recursive SISO decoder. An important feature of the proposed RSSE acquisition scheme is that it exploits the real-time knowledge of the reliabilities associated with the consecutive chips, whereas previous synchronization schemes [93, 102] used hard decision. Furthermore, we find the best possible primitive polynomials for RSSE schemes using the iterative SISO m-sequence acquisition principle which is analyzed in terms of its Erroneous Loading Probability (P_e) versus Signal to Noise Ratio (SNR) per chip in dB.

(b) In order to visualize the convergence of the RSSE-scheme we developed the *EXtrinsic Information Transfer* (EXIT) chart operating without using interleavers. This is a challenge, because the original EXIT charts rely on the employment of long, high-delay interleavers for ensuring that the mutual information processed by them becomes uncorrelated, obeying a Gaussian distribution. By contrast, the correlation of m-sequences is beneficially exploited during each iteration. We demonstrate that the m-sequences generated by lower-order polynomials maximize the mutual information more promptly with the aid of our RSSE scheme than those, which rely on a higher-order polynomial.

(c) We then proceed to the investigation of the so called concatenated sequence, which are generated by a pair of m-sequences, and conceived their SISO detection to improve their acquisition performance. This RSSE technique has a linearly increasing complexity with the number of chips in the concatenated sequence. Receiving as few as R consecutive chips of a (2^R-1)-chip sequence is sufficient for the local concatenated-sequence generator of the receiver to synchronize. Hence, this initial synchronization technique is eminently suitable for long m- and concatenated sequences. Another key result is the comparison of m- and concatenated sequences in terms of their Acquisition Time (AT). It is also observed that low-order Primitive Polynomials (PPs) achieve better performances than higher-order polynomials for both the m- and for the concatenated sequences. When considering PPs having a higher number of taps, concatenated sequences are capable of achieving in excess of 3 dB Signal to Noise Ratio (SNR) gains over m-sequences.

1.5 Thesis Structure

The rest of this thesis is structured as follows:

(a) In **Chapter 2** we provide a rudimentary introduction to sequences, comparing their basic characteristics such as their cross-correlation, auto correlation and Peak to Average Power Ratio (PAPR) values.

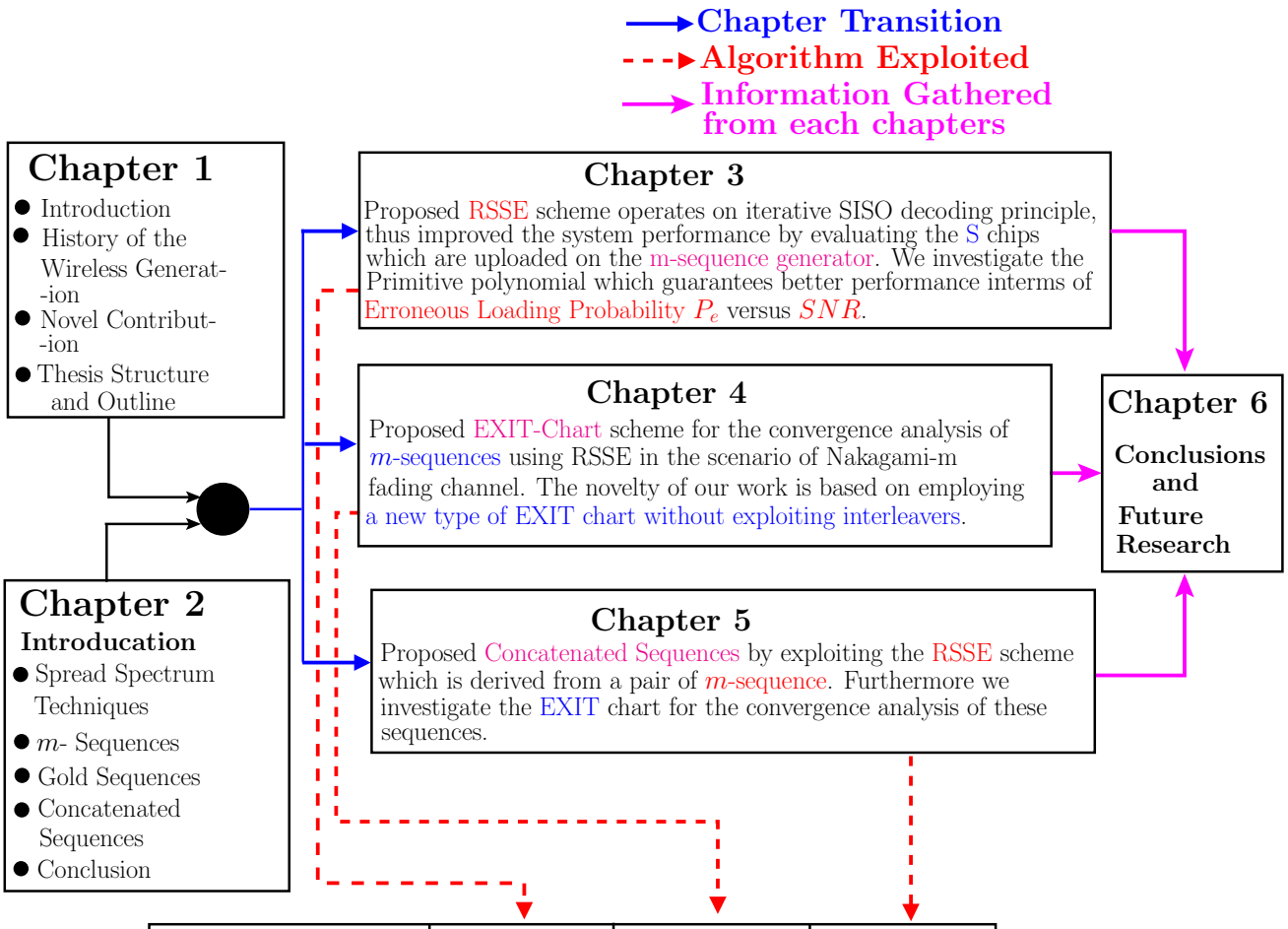
(b) In **Chapter 3** the performance of m-sequences exploiting the concept of Recursive Soft Sequential Estimation (RSSE) is discussed. The performance of RSSE scheme is evaluated by comparing the Erroneous Loading Probability P_e versus Signal to Noise Ratio (SNR). We will show that the performance of polynomials depends upon three factors, namely on the polynomial order, on the number of connecting taps and on the specific indices of the connecting taps.

(c) In **Chapter 4**, we present the so-called *EXtrinsic Information Transfer (EXIT)* Chart aided convergence analysis of recursive soft m-sequence estimation in Nakagami-m fading channels [1]. The novelty of this work is based on employing a new type of EXIT chart operating without using interleavers.

(d) In **Chapter 5** we proposed a novel design [2] for the acquisition of so-called concatenated sequences derived from a pair of m-sequences, which also relies on Soft-In-Soft-Out (SISO) detection for improving the acquisition performance.

(e) Finally, in **Chapter 6** our conclusions and future research will be presented.

Finally, the structure of this report is portrayed in Fig. 1.4.



Characteristics	Chapter 3	Chapter 4	Chapter 5
Primitive Polynomial	✓	✓	✓
RSSE Scheme	✓	✓	✓
Acquisition Time	✗	✓	✓
EXIT Chart	✗	✓	✓
Automatic Gain Controller (AGC)	✗	✓	✗

Figure 1.4: The structure of this report.

Chapter 2

Characteristics of Different Sequences in Mobile Communication

In this chapter we will lay the foundations, based on the sequences used for synchronization algorithms in mobile communication systems. Furthermore, we will elaborate on the sequences used in synchronization by comparing their basic characteristics such as *cross-correlation*, *auto-correlation* and *Peak to Average Power Ratio* (PAPR) values. The sequences exploited in this chapter are m-, concatenated-, and Gold- sequences respectively. In Section 2.1 m-sequences are presented, Section 2.2 deals with the Gold sequences while in Section 2.3 behavior of concatenated sequence is presented while in Section 2.4 PAPR is calculated and finally Section 2.5 deals with the conclusion.

2.1 m-Sequence

The m-sequences are generated by maximum-length linear feedback shift registers [4, 13, 103]. A general shift register structure constructing maximum-length sequences is depicted in Fig. 2.1. If there are m register stages, the maximum length of an output sequence is $(2^m - 1)$. These sequences are derived by a *generator polynomial* of degree m formulated as:

$$g(X) = g_m x^m + g_{m-1} x^{m-1} + g_{m-2} x^{m-2} + \ldots + g_1 x + g_0, \tag{2.1}$$

where $g_m \in \{0, 1\}$ and $i = 0, 1, \ldots, m$ and $g(X)$ has to be a primitive polynomial [104, 105], which is defined as a polynomial that cannot be *factorized*.

We can appropriately modify Fig. 2.1 to obtain the LFSRs model for any m-

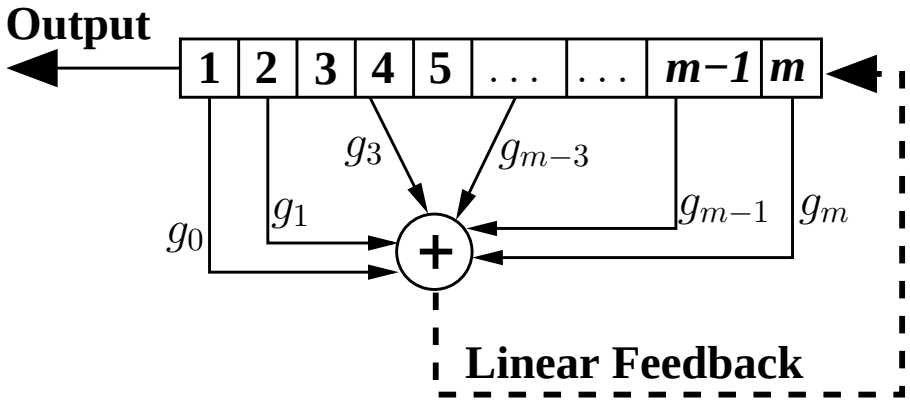


Figure 2.1: Linear Feedback Shift Register

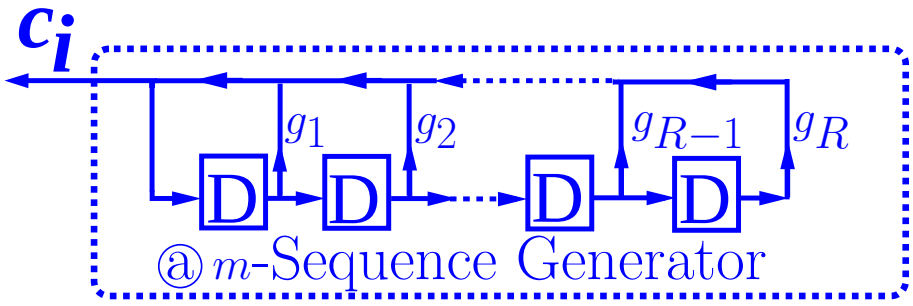


Figure 2.2: m-sequences generator that outputs the binary sequence g_1, g_2, ..., g_R represents the polynomial connections of the shift register.

sequence generator. In Fig. 2.2 'D' represents a unity time delay, while $g_1, g_2, \ldots, g_R$ represents the connections. Specifically, $g_i = 1$ represents the presence and $g_i = 0$ the absence of a connection. Furthermore, without loss of generality we assume that $\{r_1, r_2, \ldots, r_{M=R}\}$, where r_i is an integer in the range $[1, R]$, representing an index set corresponding to the set of feedback taps, implying that in Fig. 2.2, we have $g_{r_1} = g_{r_2} = \ldots = g_{r_M=R} = 1$, while the remaining coefficients are zero. The above configuration corresponds to a *generator polynomial* of degree m formulated as:

$$g(D) = 1 + D^{r_1} + D^{r_2} + \ldots D^{r_M=R}, \tag{2.2}$$

where R represents its highest-order term and $g(D)$ must be primitive polynomial that is a polynomial that cannot be factorized [104, 105]. Thus, in the wireless communication systems we use binary spreading sequences having values of $\{+1, -1\}$, where $+1$ represents '0' and '-1' represents 1 [4, 13, 16, 103, 104].

All possible PPs which generate maximum length sequences are illustrated in Fig. 2.3 for $m = 5$ that were found by a *full search* through all possible connection polynomials. Explicitly, it can be observed that *six* PPs have resulted in a maximum length of 31 chips. In order to generate a $(2^m - 1)$-length m-sequence, m register stages are required. Therefore, excluding $0, 0, 0, \ldots 0$, there are $(2^m - 1)$ *initial register*

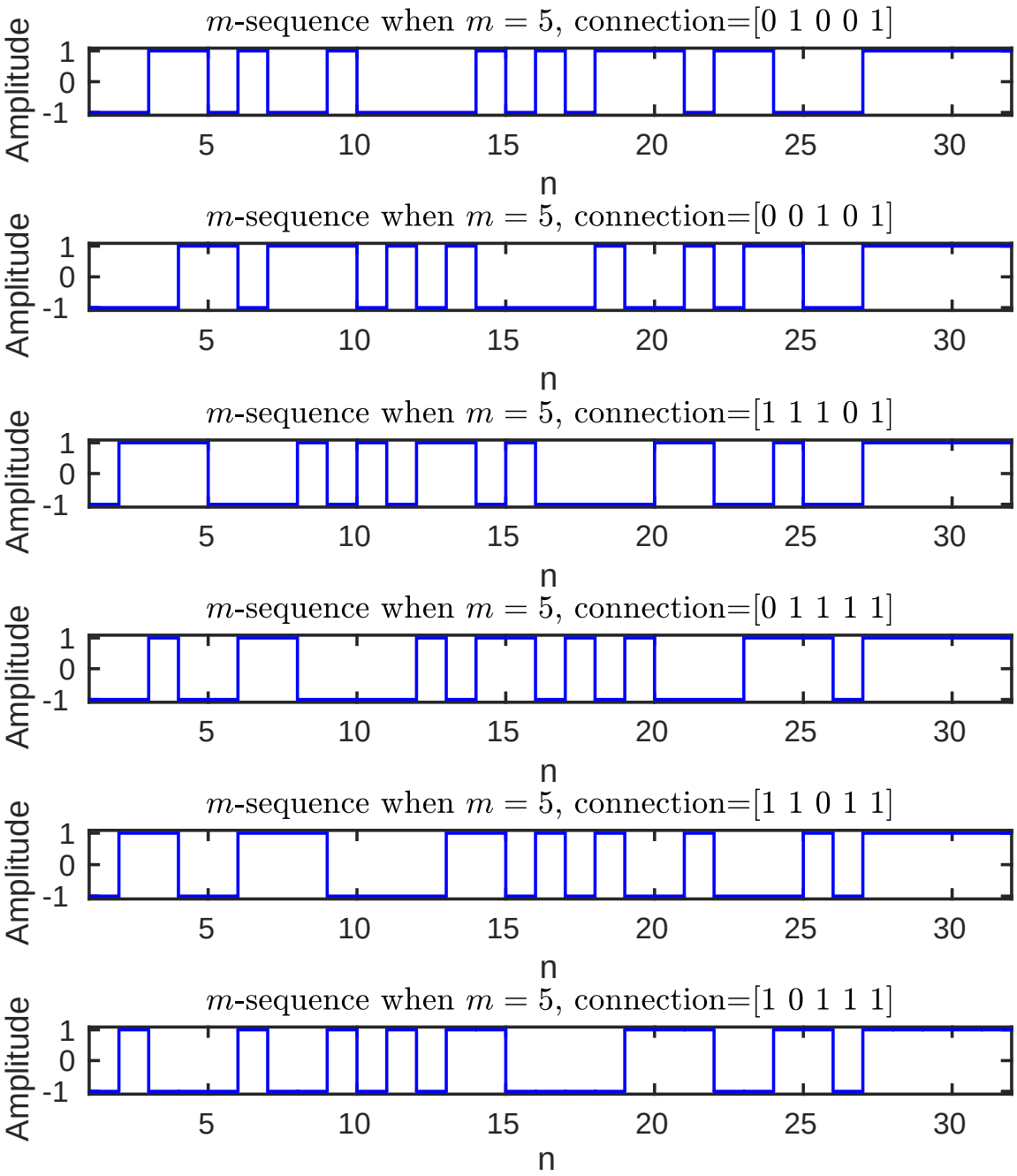


Figure 2.3: Six m-sequences for m=5.

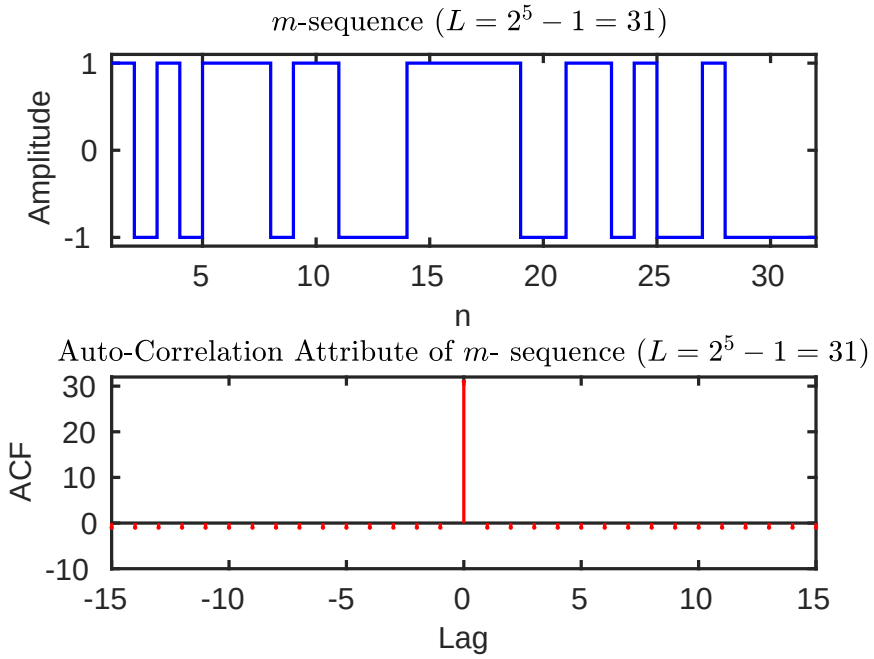


Figure 2.4: Auto-Correlation Function (ACF) of an m Sequence, where $m = 5$.

states. Fig. 2.3 depicts the m-sequence ($m = 5$) at the output of the generator for different PPs. When designing initial acquisition schemes, we have to ensure that the code sequence is periodic [1] and distinct from the *time-shifted versions* of other code sequences. These properties may be characterized by the *cross correlation* and *auto-correlation* functions. The Auto-Correlation Function (ACF) is defined as

$$\varphi_a = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} f(t) f(t-\tau) dt = \begin{cases} 0, & \tau \neq 0 \\ k, & \tau = 0. \end{cases} \tag{2.3}$$

In Eq. (2.3) the parameters are as follows:

- T represents the time period,
- $f(t)$ represents the original input signal,
- $f(t-\tau)$ is the delayed version of the original input signal.

As an example, the ACF of a 31-chip m-sequence is shown in Fig. 2.4.

[1] These are those polynomials which obey maximum length sequence. Thus the *position* of the *connection taps* helps to generate the desire m-sequence which obeys the maximum length duration that is $(2^m - 1)$ where m is the polynomial order [17, 22, 104, 106]. As a result of obeying the *maximum length sequences* these polynomials are used for *fast* synchronization.

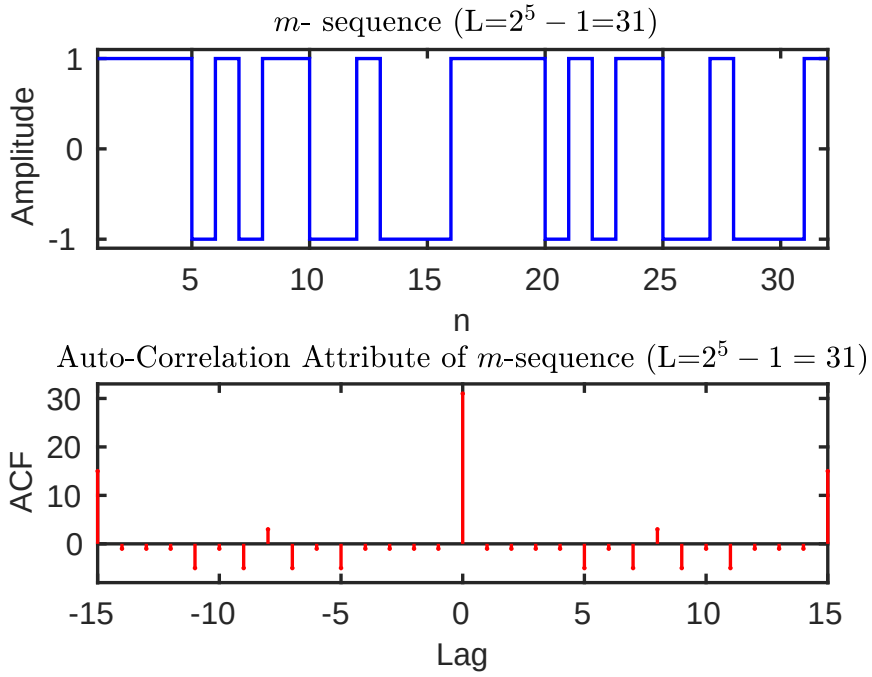


Figure 2.5: Auto-Correlation Function (ACF) of an arbitrary sequence of order 5.

2.1.1 Auto-Correlation Characteristics

First of all, m-sequences should have similar ACFs to that of *random sequences*. Fig. 2.4, plots the ACFs of m-sequence when $m = 5$, from which we can see that the non-normalized auto-correlation value is equal to the length of the sequence; $(2^m - 1)$ when the lag τ is zero, otherwise the auto-correlation value is -1. This observation can be expressed as:

$$R(\tau) = \begin{cases} L & \tau = 0 \\ -1 & 1 \leq \tau \leq L-1. \end{cases} \tag{2.4}$$

When comparing the maximum length sequence of Fig. 2.4 with an *arbitrary sequence* of order 5 in Fig. 2.5, the ACFs are seen to be *quite different*. Explicitly, observe in Fig. 2.5, that the latter has relatively high side lobes[2] and hence it is not suitable for synchronization purposes [16, 22, 28].

2.1.2 Cross-Correlation Characteristics

The cross correlation is defined as a *dot product* of two signals or the correlation between *two different signals*, thus more non-zero values are obtained because of the

[2] As a result the values obtained are non-zero even when τ is not equal to zero and thus, an arbitrary sequence of order 5 have larger values of ACF than those of the m-sequences. Thus, they are not used for synchronization [16, 76, 22, 28].

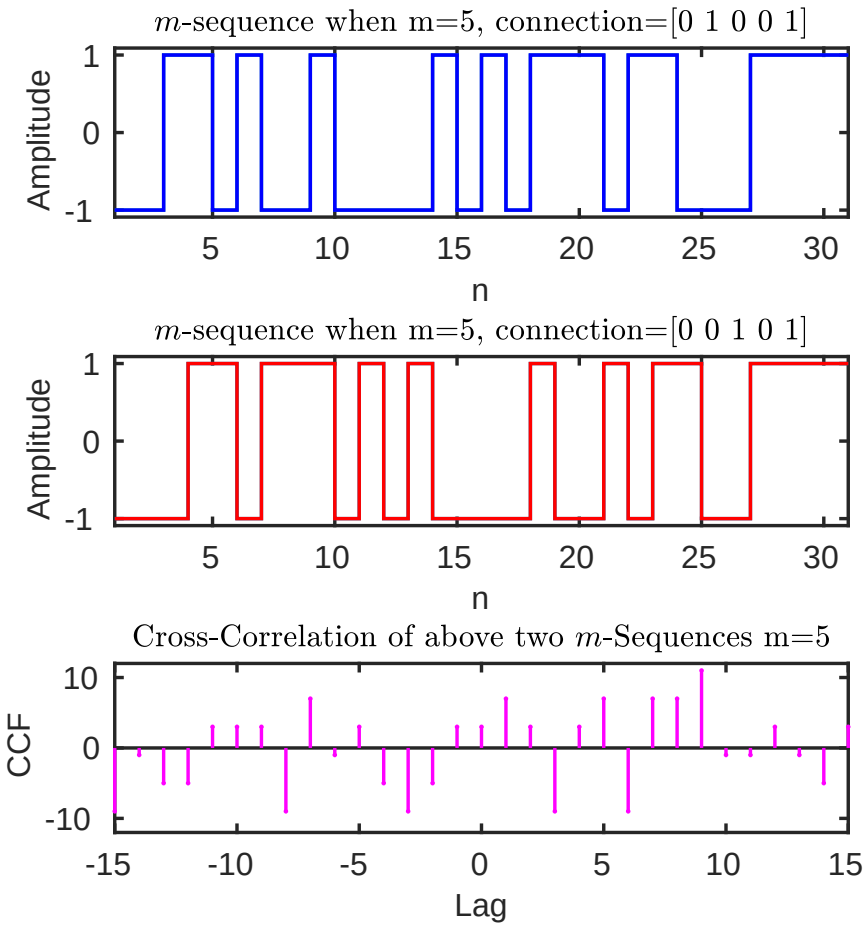


Figure 2.6: Cross correlation between two m-sequences having length L =31 when m =5.

dot product/multiplication of these signals having different tap connections:

$$f.g(\tau) = \int_{\infty}^{\infty} f(t)g(t+\tau)dt. \tag{2.5}$$

Fig.2.6 shows the Cross Correlation Function (CCF) of *two* m-sequences. It can be observed from Fig. 2.6 that *three different values* are obtained.

2.2 Generation of Gold Sequences

Although m-sequences have *substantial merits*, the number of available m-sequences is insufficient for supporting the needs of *commercial cellular systems* [13, 104, 106]. Another PN sequence called Gold sequence is generated by the model depicted in Fig. 2.7. They are generated by a *pair* of m-sequences, where the two m-sequence generators are represented by the dotted boxes and their feedback generated by the *linear feedback shift registers* as shown in Fig. 2.7. Explicitly, we add a pair of preferred m-sequences by performing their XOR operation to generate the Gold sequence. This idea was proposed by R. Gold in 1967 [107]. The resultant Gold

sequence has a length of $L = 2^m-1+2 = 2^m+1$. Gold sequences have ACFs and CCFs exhibiting *three possible values* as explained in [6, 16, 17]. This sequence is utilized

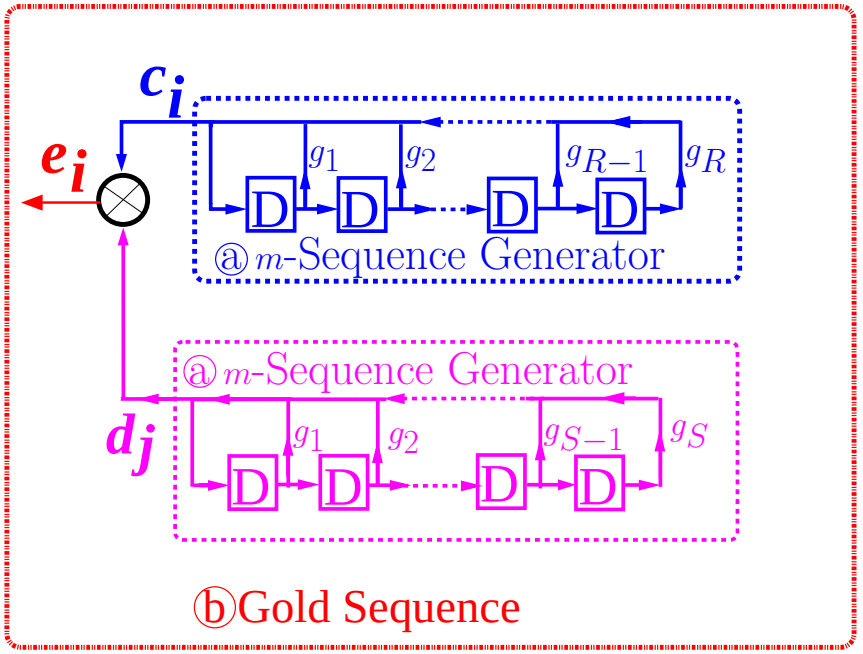


Figure 2.7: Gold Sequence Generator Model.

in the Third Generation (3G) communication systems for *supporting asynchronous* Wideband Code Multiple Access (WCDMA). In this section the main properties of Gold-sequences are discussed.

2.2.1 Auto-Correlation Characteristics

A Gold sequence is generated by two preferred m-sequences which are *periodic*, hence the Gold sequences are also *periodic* [108]. The ACFs of several Gold sequences associated with the length of 31 are plotted in Fig. 2.8, where the *peak* is equal to the *sequence length*, just like for m-sequences. Observe from Fig. 2.8, it can be concluded that there are three different values $(-1, -9, 7)$ for the *out-of-phase* Auto Correlation Lags (ACLs) of Gold sequences. This leads to another property of Gold sequences, namely that the Out-Of-Phase ACLs have only *three possible values*, which are given by:

$$R_{xx}(l) = \begin{cases} L & l = 0 \\ -1, -t(m), t(m) = 2 & l \neq 0 \end{cases} \tag{2.6}$$

$$t(m) = \begin{cases} 2^{\frac{m+1}{2}} + 1, m \text{ is odd} \\ 2^{\frac{m+2}{2}} + 1, m \text{ is even.} \end{cases} \tag{2.7}$$

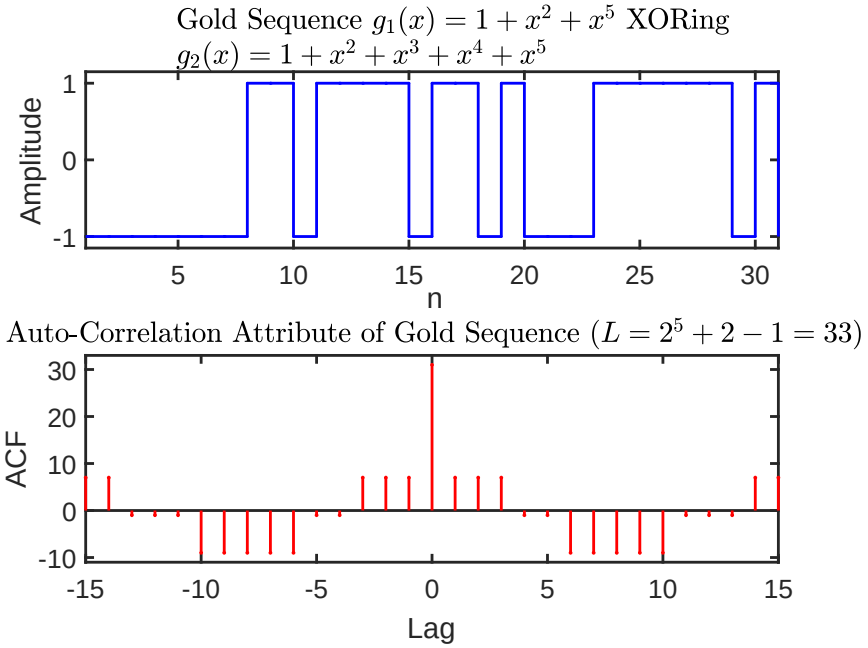


Figure 2.8: Auto-Correlation of a Gold Sequence ($L = 33$).

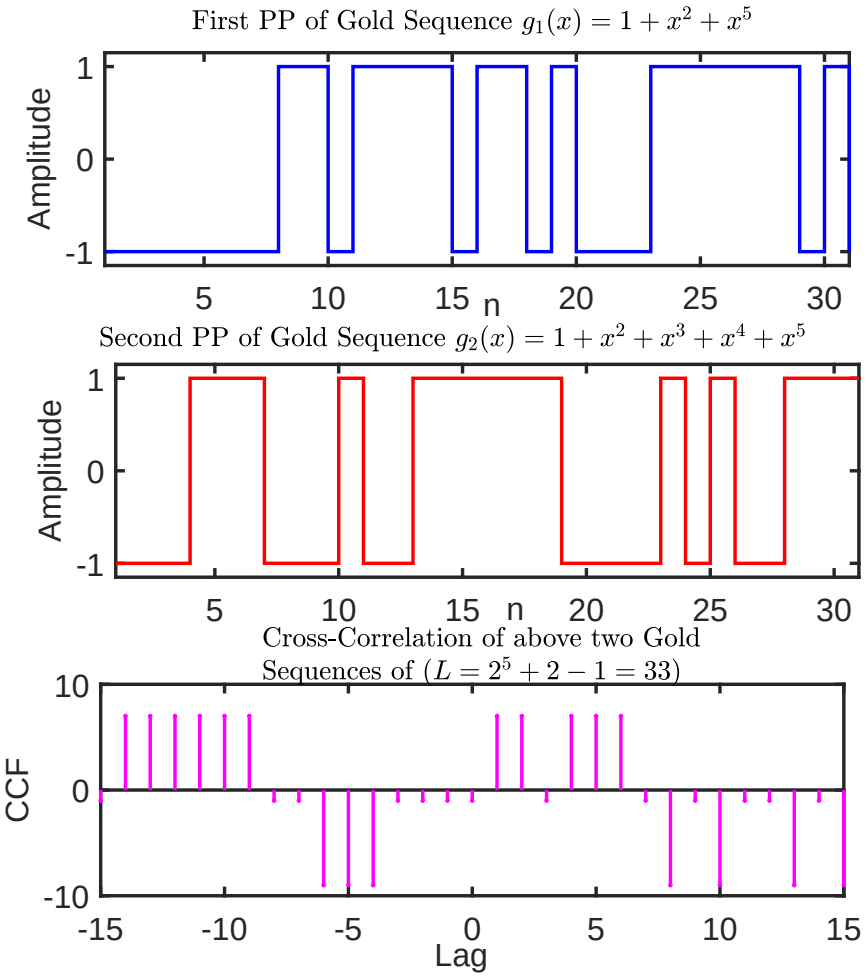


Figure 2.9: Cross-Correlation of a Gold Sequence (L=33).

m	$L = 2^m - 1$	$N = 2^m - 1 + 2$	$\mathbf{R}_{max}$	**Welch Bound**	**Sidelnikov bound**
3	7	9	5	2.51	3.46
4	15	17	9	3.76	5.29
5	31	33	9	5.49	7.75
6	63	65	17	7.88	11.14
7	127	129	17	11.23	15.87
8	255	257	33	15.94	22.54
9	511	513	33	22.58	31.94
10	1023	1025	65	31.97	45.21
11	2047	2049	65	45.23	63.97
12	4095	4097	129	63.98	90.48

Table 2.1: The Welch and Sidelnikov bounds for Gold sequences having different periods [16,22,28].

2.2.2 Cross-Correlation Characteristics

A similar property prevails for the CCF of Gold sequences, which is given below

$$R_{xy}(l) = -1, -t(m), t(m) - 2 \qquad \text{for all l and } x \neq \ y. \tag{2.8}$$

Fig. 2.9, depicts the CCF of 5^{th}-order Gold sequences. It can be observed that the Gold sequence generated for this order has three possible cross correlation values at different lags. From these basic results, it is difficult to determine, which sequences perform better, hence we have to further investigate the properties of m- and Gold-sequences.

The family of a Gold sequences has a period of $L = 2^R - 1$ or $L = 2^S - 1$, where R and S belongs to same polynomial order having different taps connection and so there are $N{=}L + 2 = 2^R + 2 - 1 = 2^R + 1$ family members. Table. 2.1 shows the Welch and Sidelnikov [16, 22, 28] bounds for Gold sequences having different values of m. It may be observed that the period L is odd and N is also odd.

2.2.3 m-Sequences versus Gold Sequences

Again, a pair of m-sequences having an identical length of $L = 2^R - 1$ or $L = 2^S - 1$ is used for constructing Gold sequences [16, 19, 22, 103, 104], where R and S belongs to same polynomial order having different taps connection. Hence Gold sequences inherit the main properties of these m-sequences [107]. Gold codes take advantage of the fact that if two distinct m-sequences with time shifts τ_{t1} and τ_{t2} are added together by modulo-2 or XOR operation, then the resultant sequence becomes unique for every unique value of τ_{t1} and τ_{t2} [16, 22, 28, 109]. Table 2.2 shows the total

m	$L = 2^m - 1$	m-sequences			Gold-sequences	
		total number of m-sequence	R_{max}	$R_{max}/R_{(0)}$	R_{max}	$R_{max}/R_{(0)}$
3	7	2	5	0.71	5	0.71
4	15	2	9	0.60	9	0.60
5	31	6	11	0.35	9	0.29
6	63	6	23	0.36	17	0.27
7	127	18	41	0.32	17	0.13
8	255	16	95	0.37	33	0.13
9	511	48	113	0.22	33	0.06
10	1023	60	383	0.37	65	0.06
11	2047	176	287	0.14	65	0.03
12	4095	144	1407	0.34	129	0.03

Table 2.2: Peak cross correlation of m- and Gold sequences [16, 22, 28]

number of m- and Gold-sequences along with the associated chip-synchronous peak cross-correlation value and the ratio between the peak magnitude R_{max} of the cross correlation function and the peak value of the autocorrelation function R_0 for PP orders of $3, 4, 5, 6, 7, 8, 9, 10, 11$ and 12 [22,28,109,110]. The peak cross correlation has to be significantly lower than the corresponding codes' autocorrelation peak, where the latter depends on the length of the sequence [16, 19, 22, 103, 104], as depicted in Table 2.2. In general, the cross-correlations of m-sequences is much higher than those of Gold sequences [3, 22, 110, 111].

Observe from Table 2.2 that when increasing m, the peak cross correlation value R_{max} which is related to the maximum number of identical chips present in a pair of different spreading codes [22, 28] substantially decreases for the Gold sequence, while it is near-constant or gracefully decaying for the m sequence. For the sake of a bold, explicit comparison, the peak of the cross-correlation function of both the m- and Gold sequences normalized by the in-phase auto-correlation having lengths of $m= 3, \ldots, 12$ are shown in Fig. 2.10. The blue bars represent the normalized cross correlation peak values of m-sequences for $m= 3, \ldots, 12$, which are seen to be higher than those of the identical-length Gold sequences for $m > 4$. Suffice to say that it would be desirable to use sequences, which exhibit a Dirac-delta-like auto correlation function and all-zero cross correlation function.

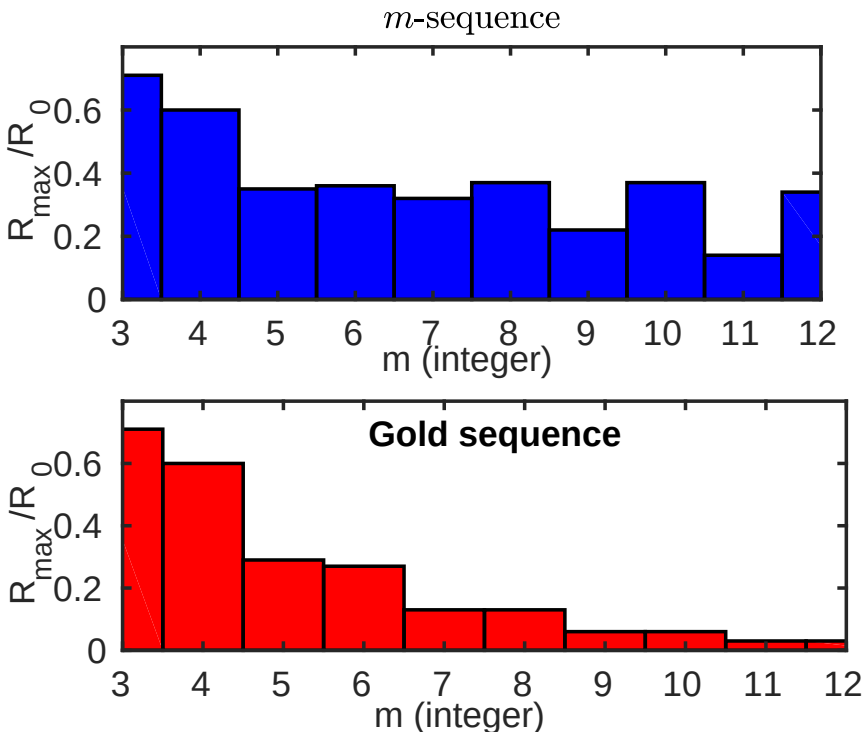


Figure 2.10: Peak cross-correlation values comparison between m- and Gold Sequences.

2.3 Concatenated-Sequences

The concatenated sequences are developed from two m-sequences having identical lengths using a pair of m-sequence generators. These sequences are *widely* used in communication [112, 113, 114, 115]. They have similar properties to the m- and Gold sequences [109,115,116]. The structure of concatenated sequences is specifically constructed for *minimizing the receiver complexity*. The concatenation of sequences is utilized for constructing long sequences from short sequences [116,117]. Furthermore, they are capable of reducing the sidelobes of the aperiodic ACF of the PN sequences. Fig. 2.11 illustrates a linear combination of a pair of m-sequences, where both m-sequences have different taps but the same length of $(L = 2^m - 1)$ [115, 116, 117]. The notation of c_i and d_i in Fig. 2.11 represents the output values of the two m-sequence generators constructing the concatenated sequence. Then by performing the modulo-2 addition we generate a concatenated sequence, as shown in Fig. 2.11. The basic properties of these sequences are discussed briefly in the next two sections.

2.3.1 Auto-Correlation Characteristics

The ACF of a concatenated sequence having a length of 31 is plotted in Fig. 2.12. Observe that $R(0)$ of this non-normalized ACF is equal to the *sequence length*, similarly to the m- and Gold-sequences. Hence, they behave *similarly* to the m- and Gold-sequences.

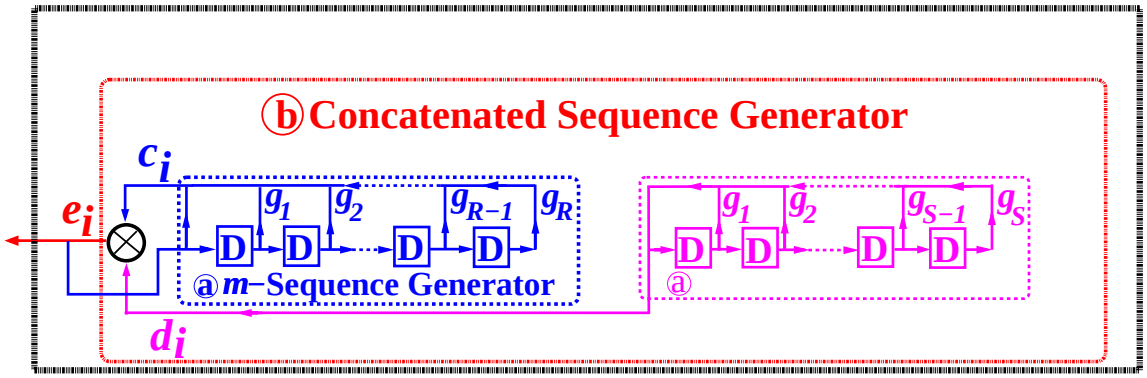


Figure 2.11: Generation of Concatenated Sequence.

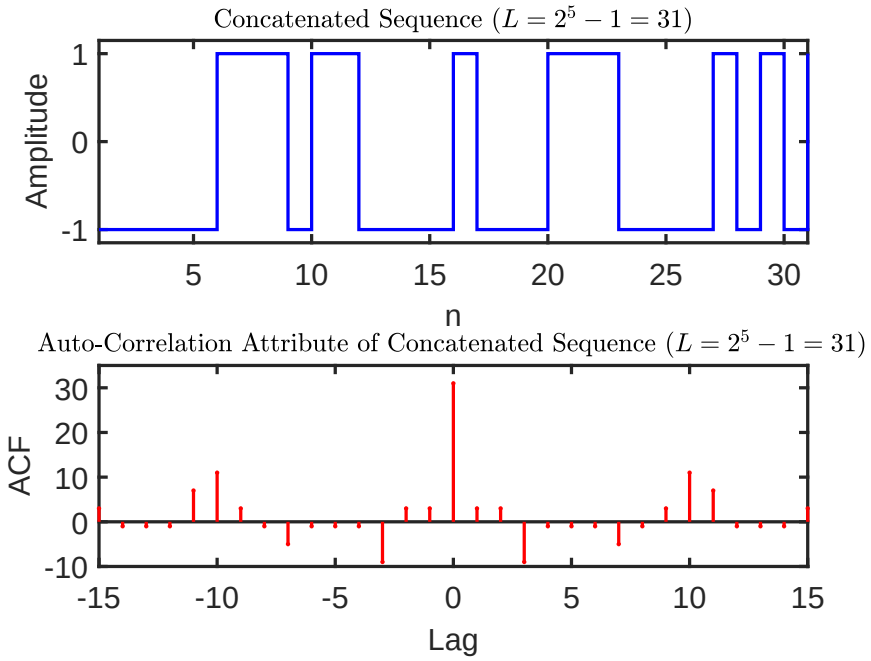


Figure 2.12: Auto-Correlation of Concatenated Sequence of (L=31).

2.3.2 Cross-Correlation Characteristics

Eq.2.5 is utilized to obtain the CCF of concatenated sequences. Fig. 2.13 depicts the CCF of 5^{th} order concatenated sequences. It can be observed that the concatenated sequence has four cross correlation values, which are lower than those of the Gold- and m-sequences.

2.4 Peak to Average Power Ratio

The Peak to Average Power Ratio (PAPR) is defined as the ratio of the maximum signal peak value to the total average values obtained in the given time slots of the

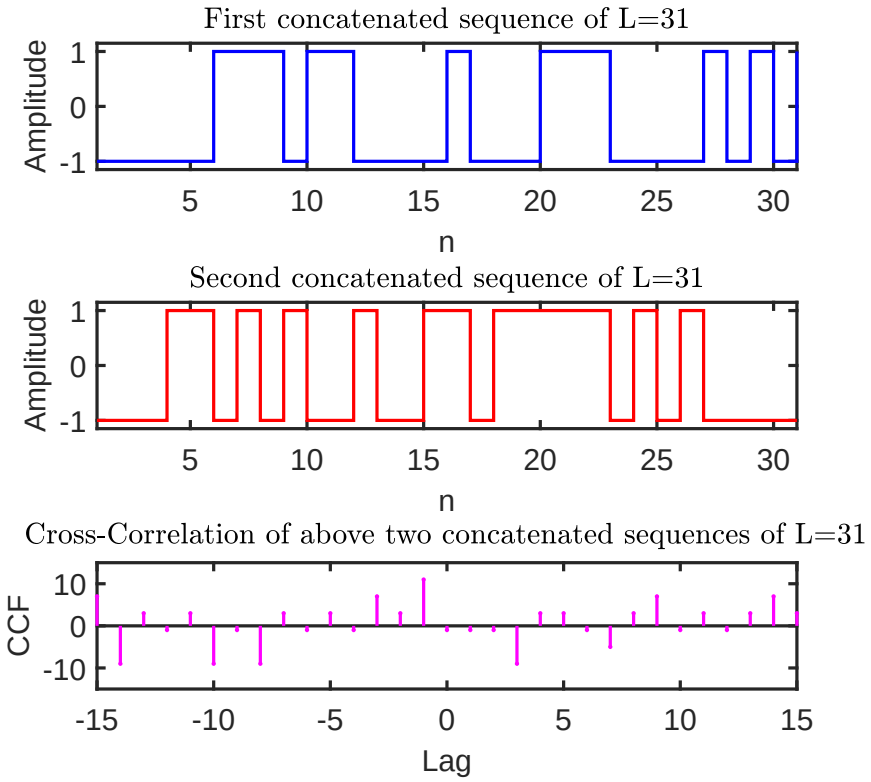


Figure 2.13: Cross-Correlation of Concatenated Sequence (L=31).

signal, which is calculated as:

$$PAPR = 10 \log \left[\frac{maximum\ [f(x)]}{Average\ [f(x)]} \right]. \tag{2.9}$$

Accordingly the PAPR should be as close to unity as possible, because the reduction of the PAPR reduces the receiver amplifier's linearity requirement. The PAPR values of the Concatenated-, Gold- and m are shown in Table. 2.3.

Sequence Utilized	**Length of Sequence**	**Peak to Average Power Ratio (PAPR)**
m− Sequence	**31**	**34.34 *dB***
Concatenated Sequence	**31**	**2.89 *dB***
Gold Sequence	**33**	**5.39 *dB***

Table 2.3: Comparison between different sequence regarding PAPR values.

2.5 Conclusion

In this chapter we have briefly investigated the basic features of the sequences utilized for the initial synchronization of cellular communication system. We commenced by discussing each sequence and their characteristics. It was observed that Gold and concatenated sequences have better cross correlation properties than the m-sequences, but by contrast, m-sequences have the better auto correlation properties therefore they have been used in almost every generation of cellular systems for synchronization.

Chapter 3

Performance of Iterative Acquisition

Accurate and fast synchronization plays a pivotal role in the efficient use of any wireless communication system [6, 18, 37]. Typically, the *initial step* in the process of synchronization between the Pseudo-Noise (PN) sequence and the locally generated despread sequence is termed as *code acquisition* [2, 92], or *initial synchronization*. Furthermore, initial synchronization is composed by a procedure of consecutive decisions, wherein the main goal is to bring *two sequences/codes* into coarse time alignments, mainly within a single sequence/code-chip interval. Once initial code acquisition is established by utilizing a *code tracking loop* [6, 66, 92], *fine alignment* of the *two* sequences completes the process of synchronization.

In this chapter a sequential estimation scheme is proposed for the *initial synchronization* of Pseudo-Noise (PN) sequences derived from m-sequences. The sequential estimation operates on the principle of iterative *Soft In Soft Out* (SISO) decoding. The *Recursive Soft Sequential Estimation* (RSSE) acquisition model exhibits a complexity identical to that of a traditional m-sequence generator, which increases linearly with the number of stages involved in generating the m-sequence. The appealing feature of RSSE is that the acquisition device is *capable of determining* the reliabilities linked with the *decision concerning of a set* of say R successive chips. These R number of correctly detected successive chips uniquely and unambiguously determine the m-sequence having $(2^R - 1)$ chips. Hence R chips are sufficient for the local m-sequence generator to generate a locally synchronized despreading m-sequence. Given these beneficial characteristics, the proposed RSSE acquisition model is deemed to be *more attractive* than the traditional serial search based model in terms of its *mean-acquisition time*, when the number of chips increases.

The original idea of sequential estimation based on acquisition was proposed by Ward in 1965 [102]. This method deals with m-sequences having any length of $L = (2^R - 1)$, which are correctly received by the acquisition device and are loaded

into the local m-sequence generator [102,118]. Ward's model is suitable for moderate Signal to Noise Ratio (SNR) per chip values, since it *imposes a lower acquisition time* than the *conventional sliding correlator* based scheme, as demonstrated in [119]. The basic principle of the sequence generator relies on generating chips that exactly match the forthcoming chips of the transmitted m-sequence received in the presence of noise [102]. More explicitly, when one or more of the R consecutive received chips are in error, the scheme loads erroneous values into the m-sequence generator [53,92, 120,121,122]. Therefore the authors of [93] investigated an Majority Logic Decoder (MLD) based model for synchronization. By contrast, the authors of [123] proposed a recursive sequential estimation aided acquisition technique. It was observed that the above schemes were capable of accurate sequence acquisition, despite using a simple hard decision approach. In fact, before the conception of SISO techniques [92, 124] all the previous schemes utilized hard decision techniques. However, as a benefit of the SISO concept [124,125] the system's performance can be substantially improved. We have evolved the summary of the field in Fig. 3.1, prior to the contributions of this chapter.

Against this background, the novel contributions of this chapter are as follows:

- An explicit technique of finding the best possible primitive polynomial for RSSE schemes using the iterative soft input and soft output m-sequence acquisition principle is analyzed in terms of its Erroneous Loading Probability (P_e) versus SNR in dB. We identify the polynomials having the best performance.
- We show that low-order Generated Polynomials (GPs) have a lower P_e at a given SNR than their high-order counterparts.
- When comparing GPs of the same order having non-consecutive feedback taps, the GPs associated with higher-index taps perform best. Furthermore, among GPs of the same order, those having non-consecutive feedback taps outperform those having consecutive feedback taps.

In a nutshell, this chapter deals with *the performance analysis of m-sequences* exploiting the concept of RSSE in the face of Additive White Gaussian Noise (AWGN). Section 3.1 introduces our *RSSE* model. Section 3.2 characterizes the *performance* of our RSSE scheme under AWGN, while Section 3.3 characterizes *the polynomials processed* by our RSSE scheme. Finally, Section 3.4 concludes the chapter.

3.1 Recursive Soft Sequential Estimation Acquisition

The detailed schematic diagram of the proposed RSSE acquisition scheme is depicted in Fig. 3.2, which consists of four fundamental building blocks:

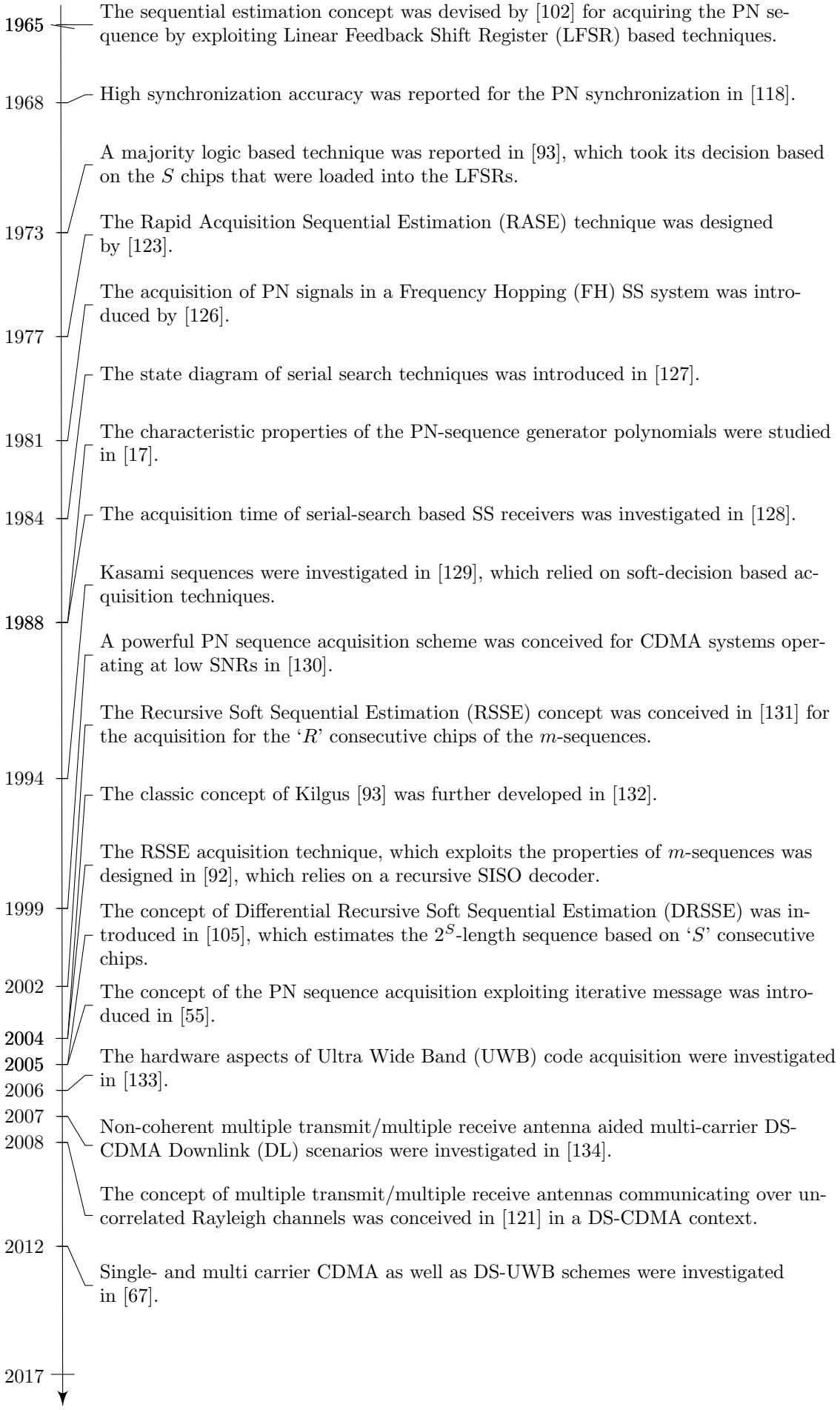


Figure 3.1: Timeline of Initial Acquisition Research.

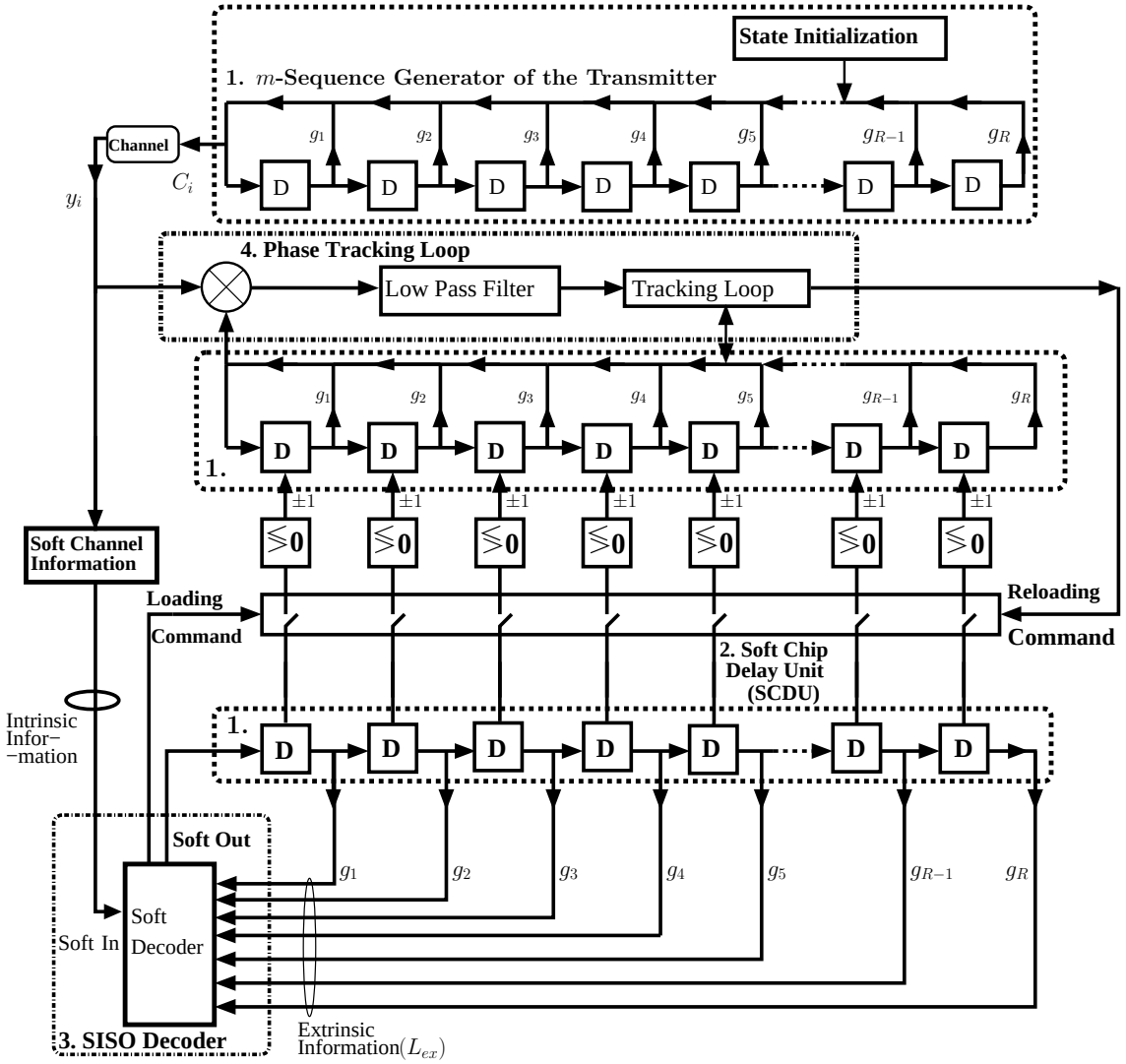


Figure 3.2: RSSE iterative acquisition scheme.

1 m-sequence generator;

2 Soft chip register;

3 SISO decoder;

4 Phase tracking loop;

For convenience, the top-level architecture is also shown in Fig. 3.3 for aiding the physical interpretation of Fig. 3.2. These blocks are explained in detail in the relevant sub-sections followed by the RSSE acquisition scheme. Before proceeding to the blocks concerned, we summarize our main points related to the RSSE scheme of Fig. 3.2 and of Fig. 3.3 where the soft chip register has the same number of delay elements as that of the m-sequence generator of Fig. 3.2. These delay units are referred to as soft-chip delay units and they store the instantaneous values of consecutive chips in the form of their Log-Likelihood Ratio (LLR). After obtaining the LLR values, they are loaded into the delay units of the m-sequence generator. The

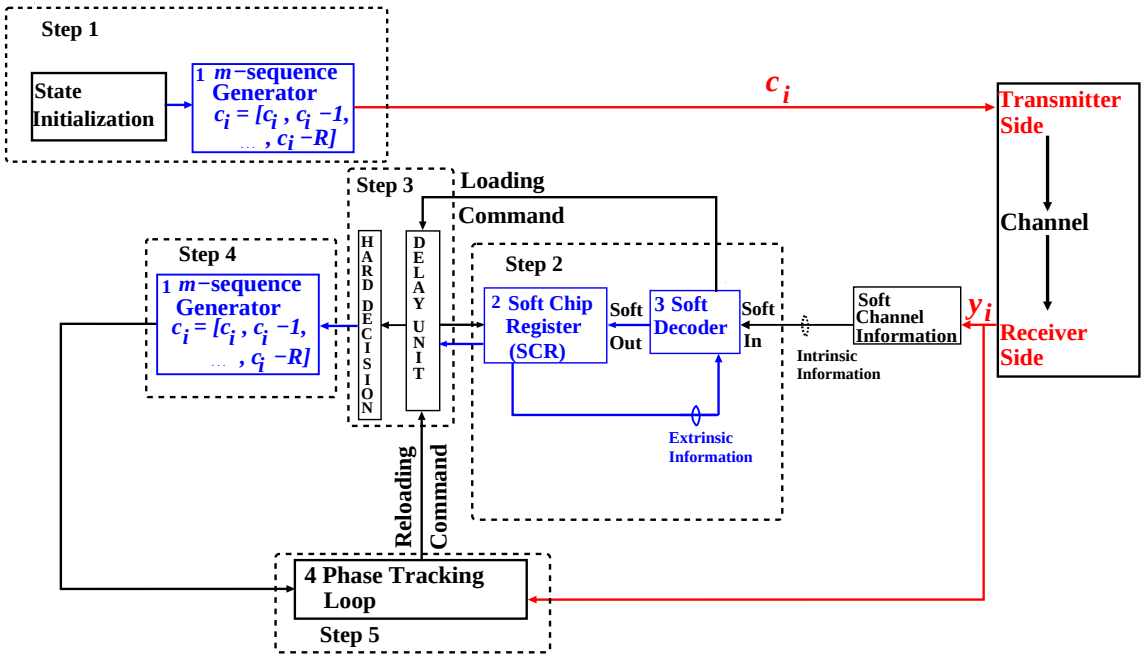


Figure 3.3: A schematic diagram of our purposed RSSE aided iterative acquisition scheme.

SISO decoder estimates the corresponding value of the soft LLR output after receiving a soft channel output associated with a given chip of the m-sequence. The SISO decoder processes both the intrinsic information received from the channel plus the extrinsic information related to the same chip based on the previously decoded LLR values stored in the soft-chip delay units. The output of the SISO decoder is then shifted to the left-most position of the soft-chip delay units in the soft-chip register of Figs. 3.2 and 3.3, while the soft value in the right-most soft-chip delay unit is discarded. The appealing feature of the RSSE is that it is capable of observing the reliabilities of all the consecutive chips by observing the amplitudes of the LLR values stored in the soft-chip delay units. The basic steps of the RSSE are illustrated as follows:

Step 1 At the transmitter side of Fig. 3.3, the m-sequence generator is initialized and the transmitter sends the phase-coded carrier signal without any data modulation[1]. Both the transmitter and the receiver know the GPs and the chip values. If the receiver has exactly the same feedback for the m-sequence generators as those of the transmitter side, then the corresponding chip values will be loaded

[1]In the context of initial synchronization, the m-sequences are utilized for aiding synchronization between the Mobile Station (MS) and the Base Station (BS). They have been specifically selected as a benefit of their cyclic nature. Explicitly, during code acquisition, the receiver becomes capable of locking on to the correct stage of each shift register after as few as R chip transmissions, despite transmitting m-sequences of length $(2^R - 1)$. Our DownLink (DL) transmission is initiated by transmitting an unmodulated pilot signal over the Pilot Channel (PC). The PC provides a reference signal for all the MSs within a cell, which is always transmitted by the BS [16, 65, 66]. Typically it is about 4-6 dB stronger than the power of all other channels. The PC uses the all-zero Walsh code and contains no information except for the Radio Frequency (RF) carrier in the IS-95. Therefore, the pilot signal is an unmodulated Spread Spectrum (SS) signal because it is multiplied by an all-zero Walsh code, which is then spread according to the chip rate of the sequence [51, 66]. No data modulation is performed during this part of the transmission, as mentioned in [92, 121].

into the register of the m-sequence generator.

Step 2 The SISO detector/decoder receives a channel output sample y_i associated with the chip c_i, and then it evaluates the LLR of c_i based on y_i as well as it determines the extrinsic information. The data are then fed to the SCRs of Fig. 3.3, where the SCRs have the same number of taps as well as connections as that of the m-sequence generator at the transmitter. The most recent R chip values are stored in the SCR of the SISO decoder, which are associated with R successive chips of the transmitted m-sequence, respectively. When the magnitudes of the most recent R soft outputs of the SISO detector become sufficiently high for ensuring a low P_e, a "Loading command" is issued by the scheme of Fig. 3.3.

Step 3 After that, R successive chips are calculated by using hard decisions, which is based on comparing the most recent R chips stored in the SCR at that instant of time to a threshold resulting in the binary value of either $+1$ or -1. After obtaining the hard decision result, the values are loaded into the corresponding delay units of the m-sequence generator of Fig. 3.3.

Step 4 As soon as the initial binary values are determined by the m-sequence generator, the received signal is despread, provided that the initial chip values of the m-sequence generator are correctly loaded.

Step 5 The despread signal is transferred to the Phase Tracking Loop (PTL) of Fig. 3.3 to acquire the phase. When the phase is acquired correctly, the updated chips of R will be loaded into the delay units of Fig. 3.3. By contrast, if the phase is not acquired correctly, then the PTL will be triggered to activate the "Reloading command". This procedure will be repeated until the correct code is found by the PTL. In other words, the task of PTL is to retrieve a signal received over the noisy channel and to produce a secure output so that the received and transmitted signals are perfectly aligned.

3.1.1 m-Sequence Generator

The m-sequences employed are referred to as maximum-length sequences [16, 104], which are generated by the feedback shift register of the transmitter seen in Fig. 3.2, where 'D' represents the unit time delay and the coefficients $g_1, g_2, \cdots, g_R$ represent the presence or absence of the feedback connections. The above configuration leads to the following GP:

$$g(D) = 1 + D^{r_1} + D^{r_2} + \ldots + D^R, \tag{3.1}$$

where R is the highest order GP coefficient and $g(D)$ has to be a primitive polynomial [104, 105]. According to Fig. 3.2, the binary output sequence c_i, for $i = 0, 1, \ldots,$

can be generated by the recursion of

$$c_i \quad = \quad c_{i-r_1} c_{i-r_2} \ldots c_{i-(R)} = \prod_{j=1}^{N} c_{i-r_j} \quad i = 0, 1, \ldots \tag{3.2}$$

Please note in the m-sequence generator of Fig. 3.2 that the feedback chip is transmitted to the receiver, instead of the output of the last shift register stage. The latter would have resulted in the generation of an m-sequence. However, in this specific code acquisition problem, the state of a register stage is transmitted, instead of the bit of a conventional m-sequence. This is done so that the receiver may lock on to the correct states of each register stage after a minimum of R transmissions, where R is the number of registers stages, instead of 2^R transmissions, which would have been required if an m-sequence was transmitted. Therefore, in our problem the transmitted bits are the states of the first register stage of the m-sequence and they do not spread information bits. Based on the proposed approach, we are able to acquire the current state of the m-sequence generator at the transmitter and load the phase tracking loop from that point onwards. Therefore, transmitting the feedback chip sequence is sufficient. This way, the iterative decoding process may be faster than waiting till $(2^R - 1)$ chips have been received completed. In the context of sequential estimation-based acquisition used for short m-sequences, the generator's state can be principally estimated using iterative decoding techniques, since each m-sequence produced by an 'R'-stage generator has a period of $(2^R - 1)$ chips, and can be considered to be a cyclic Bose Chaudhuri Hocquengem (BCH) codeword of length $(2^R - 1)$, having minimum distance of $\left\{2^R - 1\right\}$ [93].

Note that both the m-sequence generator and the soft-chip register use the same feedback branches. Hence, in the m-sequence generator, the feedback elements are duo-binary values, and the product of these feedback elements is used for generating a binary feedback quantity. After the receiver obtained two sets of $2 \times \left\{2^R - 1\right\}$ number of consecutive samples of the transmitted m-sequence, the m-sequence generator's initial state of R chips is estimated by iteratively decoding the received m-sequence with the aid of its number of samples. By contrast, the feedback elements from the soft-chip register to the SISO decoder consist of the LLR values, and the specific operations must be employed in the soft-value domain to provide extrinsic information for the SISO decoding.

3.1.2 Soft Chip Register and SISO Detector

The soft-chip-register at the receiver of Fig. 3.2 consists of R number of Soft-Chip-Delay-Units (SCDUs). It may be observed from Fig. 3.2 that the number of delay units in the SCDU is the same as that in the m-sequence generator. Furthermore, both the m-sequence generator and the SCDU use the same feedback connections

as the m-sequence generator of the transmitter, since both the transmitter and the receiver know the GP. The task of the SCDU is to store and shift the instantaneous LLR values of R consecutive chips. Since in the beginning the probability of having transmitted either chip value is the same, the LLRs are initialized to zero. These R LLR values will determine the hard values of the consecutive chips that will be loaded into the m-sequence generator after making a hard decision, as shown in Fig. 3.2. The SISO detector exploits the previously computed LLR values stored in the SCDU as the *a priori* information [92,105]. The intrinsic information processed by the SISO detector is received from the channel. The soft output of the SISO detector is then shifted to the left-most position of the SCDU registers, while the right-most SCDU's value is discarded [92, 105].

3.1.3 Soft Channel Outputs

The received signal corresponding to chip c_i can be expressed as $y_i = \alpha_i c_i + n_i$, $i = 0, 1, \ldots$. When communicating over a fading channel, α_i denotes the fading amplitude, where $\alpha_i = 1$ which means no fading is considered. Furthermore, n_i represents the Additive White Gaussian Noise (AWGN) having a zero mean and noise spectral density of N_0. Given y_i, the LLR of c_i is expressed as

$$\begin{aligned} L_{ex}(c_i) = L(c_i|y_i) &= \log\left[\frac{P(c_i = +1|y_i)}{P(c_i = -1|y_i)}\right], \\ &= L_{ch,\,i} \cdot y_i + L_{apr}(c_i), \quad i = 0, 1, \cdots \end{aligned} \tag{3.3}$$

where $L_{ch,\,i} = 4\alpha_i \frac{E_c}{N_0}$ represents the reliability value of the channel output and $L_{apr}(c_i)$ is the *a priori* LLR of the ith chip, E_c represents the transmitted chip energy and $\frac{E_c}{N_0}$ represents *Signal to Noise Ratio (SNR)*. It can be observed from Fig. 3.2 that the system behaves recursively, where the previous soft outputs of the SISO detector obtained at the time indices of $(i-1), (i-2), \ldots, (i-R)$ are fed back to the SISO detector. Therefore, the extrinsic information provided by them can be readily exploited for enhancing the correct decoding probability of the chip c_i. Let the previous R number of soft outputs of the SISO detector be $L_{ex}(c_{i-1}), L_{ex}(c_{i-2}), \cdots, L_{ex}(c_{i-R})$.

$$\begin{aligned} L_{apr}(c_i) \approx \left[\prod_{r=1}^{R} \mathrm{sign}(L_{ex}(c_{i-r}))\right] \times \\ \min\left\{|L(c_i - 1)|, |L(c_i - 2)|, \cdots, |L(c_i - R)|\right\}. \end{aligned} \tag{3.4}$$

The soft output of the SISO detector $L_{ex}(c_i)$ may be found by combining Eq.(3.3) and Eq.(3.4). where we assume that $L_e(c_{-\infty}) = \cdots = L_e(c_{1-r}) = L_e(c_{-2}) = L_e(c_{-1}) = 0$. Finally, the channel output information $L(c_i|z_i)$ in Eq.(3.3) and the extrinsic information $L_e(c_i)$ in Eq.(3.4) jointly yield the soft output of the SISO

decoder associated with chip c_i as

$$\begin{aligned} L(z_i) &= L(c_i|y_i) + L_e(c_i) \\ &= L_c y_i + L(c_i) + \left[\prod_{r=1}^{R} \text{sign}(L(z_{i-r_n}))\right] \\ &\cdot \quad \min\left\{|L(z_{i-r_1})|\right\}, \left\{|L(z_{i-r_2})|\right\}, \cdots, \\ &\cdots \quad \left\{|L(z_{i-(r_N=R)})|\right\}, \quad i = 0, 1, \cdots . \end{aligned} \tag{3.5}$$

If the channel's output SNR is sufficiently high, the LLR values of the last R consecutive chips will increase upon increasing the number of iterations in the receiver. The reliabilities associated with the R consecutive chips improve, while the erroneous loading probability of the generator - which is defined as the probability of the event that the m-sequence generator of Fig. 3.2 is loaded with at least one erroneous chip - decreases upon increasing the number of iterations. If the amplitudes of the LLR values in the SCDUs become sufficiently high after a number of iterations, then the SISO detector can carry out hard-decisions to obtain the binary $+1$ or -1 chip values, which are then loaded into the delay units of the receiver's m-sequence generator of Fig. 3.2. During the lth iteration, with $l = 1, \ldots, L$, R number of extrinsic LLR have to be calculated, so that the estimated value of each shift register is updated at the receiver. This requires the transmission of R chips during each iteration. Therefore, after L iterations a total of $R \times L$ received chips have been transmitted.

3.1.4 Phase Tracking Loop

Prior to despreading, the SNR is usually insufficiently high for reliable carrier phase tracking. The despread signal is passed to a low-pass filter and then to the tracking loop of Fig. 3.2. If the tracking loop is capable of obtaining the correct phase, the code acquisition process is successfully completed. By contrast, if the tracking loop is incapable of tracking the phase, the Reloading command of Fig. 3.2 will be activated and this time the m-sequence will have different values in the delay units of the local m-sequence generator. This process will continue until successful code acquisition is achieved. The main task of the PTL in Fig. 3.2 is to reliably detect the transmitted signal and to generate a stable output so that the transmitter and the receiver are perfectly synchronized, thus improving the SNR. The Local Oscillator (LO) in the PTL maintains phase-matching and if there is any phase drift, the LO adjusts its frequency to compensate for it.

3.2 Performance of the RSSE Scheme in AWGN Channel

The AWGN channel model imposes white noise with a constant power spectral density and a Gaussian distributed amplitude [15, 22, 106]. This model is often used in

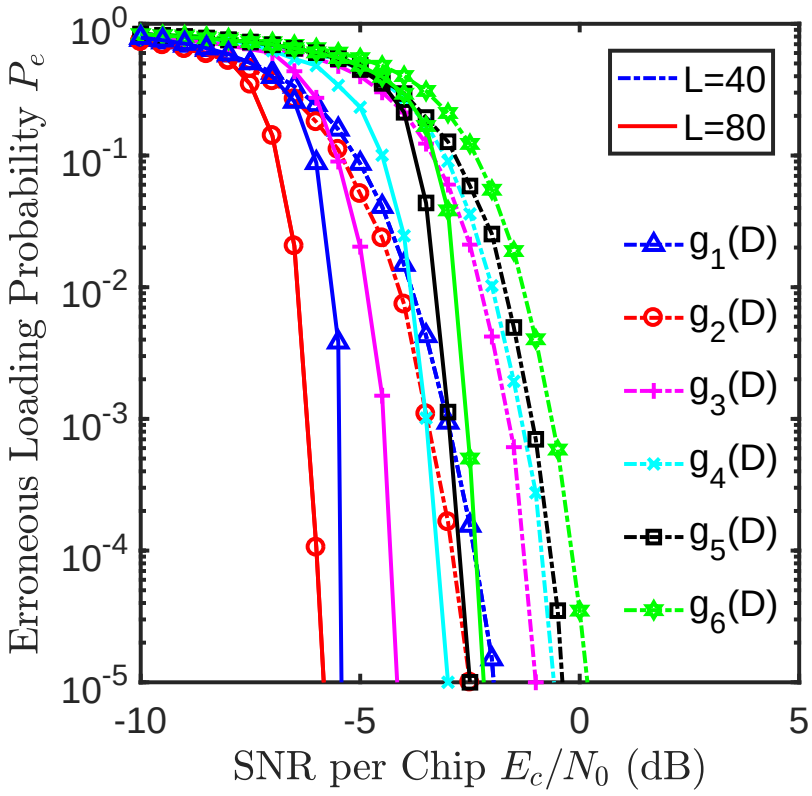


Figure 3.4: Six polynomials of $m = 5$ are characterized for transmission over an AWGN channel, when $L = 40$ and $L = 80$.

order to gain insight into the underlying behavior of various communications systems before other propagation phenomena, such as fading are considered [16, 104]. This model is also important, since it provides an upper bound on the communication system performance [15, 22, 135].

In this section we characterize the behavior of the RSSE scheme under AWGN channels. We will investigate the Erroneous Loading Probability P_e versus the SNR per chip (E_c/N_0), expressed in dB. In this section we have investigated various polynomials to characterize the effect of noise. The polynomials evaluated in this chapter are shown in Table 3.1. These polynomials are widely used in the field of cellular communication [16, 22, 136, 137, 138].

3.2.1 Performance of Polynomials in the $m = 5$ Group

In this subsection we evaluated the performance of the GP described in Table 3.1. As seen in Table 3.1, there are six 5^{th} order GPs. We have characterized their Erroneous loading Probability (P_e) versus the SNR in Fig. 3.4. In Fig. 3.4 we have used $L = 40$ and $L = 80$ iterations, which means that a total of received chips $R \times L = 40 \times 5 = 200$ and $80 \times 5 = 400$ are processed by the SISO decoder, respectively. If we compare the performance of polynomial $g_2(D)$ for $L = 40$ and $L = 80$ iterations, we observe in Fig. 3.4 that a gain of more than 3 dB is achieved at $P_e = 10^{-5}$. Upon doubling

Polyno--mial order	**No. of Poly--nomials Generated**	**Generator Polynomials**
5	6	$g_1(D) = 1 + D^2 + D^5$, $g_2(D) = 1 + D^3 + D^5$, $g_3(D) = 1 + D^2$ $+D^3 + D^4 + D^5$, $g_4(D) = 1 + D + D^3 + D^4 + D^5$, $g_5(D) = 1+$ $D + D^2 + D^4 + D^5$, $g_6(D) = 1 + D + D^2 + D^3 + D^5$
6	6	$g_1(D) = 1 + D + D^6$, $g_2(D) = 1 + D^5 + D^6$, $g_3(D) = 1 + D$ $+D^4D^5 + D^6$, $g_4(D) = 1 + D^2 + D^3 + D^5 + D^6$, $g_5(D) = 1 + D+$ $D^2 + D^5 + D^6$, $g_6(D) = 1 + D + D^3 + D^4 + D^6$
13	7	$g_1(D) = 1 + D + D^3 + D^4 + D^{13}$, $g_2(D) = 1 + D^5 + D^6 + D^7$ $D^8 + D^{12} + D^{13}$, $g_3(D) = 1 + D + D^4 + D^7 + D^8 + D^{11} + D^{13}$, $g_4(D) = 1 + D^4 + D^5 + D^7 + D^9 + D^{10} + D^{13}$, $g_5(D) = 1 + D^1 + D^2 + D^3 + D^6 + D^8 + D^9 + D^{10} + D^{13}$, $g_6(D) = 1 + D + D^2 + D^3 + D^4 + D^5 + D^6 + D^8 + D^{10} + D^{12}$ $+D^{13}$,$g_7(D) = 1 + D^2 + D^3 + D^5 + D^6 + D^7 + D^8 + D^9 + D^{10}$ $+D^{11} + D^{13}$
15	7	$g_1(D) = 1 + D + D^{15}$, $g_2(D) = 1 + D^4 + D^{15}$, $g_3(D) = 1 + D^4$ $+D^7 + D^{15}$, $g_4(D) = 1 + D + D^5 + D^{10} + D^{15}$, $g_5(D) = 1+$ $D^3 + D^5 + D^8 + D^9 + D^{10} + D^{15}$, $g_6(D) = 1 + D + D^2$ $+D^4 + D^5 + D^{10} + D^{15}$, $g_7(D) = 1 + D^2 + D^3 + D^4 + D^5 + D^6$ $+D^7 + D^8 + D^9 + D^{10} + D^{11} + D^{12} + D^{13} + D^{14} + D^{15}$
23	7	$g_1(D) = 1 + D^5 + D^{23}$, $g_2(D) = 1 + D^5 + D^{11}+$ $+D + D^{17} + D^{23}$, $g_3(D) = 1 + D^4 + D^5 + D^{12} + D^{23}$, $g_4(D) = 1 + D^4 + D^5 + D^{23}$, $g_5(D) = 1 + D^5 + D^7 + D^{21} + D^{22}$ $+D^{23}$, $g_6(D) = 1 + D^3 + D^5 + D^6 + D^{13} + D^{16} + D^{23}$, $g_7(D) = 1 + D^3 + D^4 + D^5 + D^7 + D^9 + D^{10} + D^{15} + D^{23}$
29	2	$g_1(D) = 1 + D^2 + D^{29}$, $g_2(D) = 1 + D^{27} + D^{29}$
31	2	$g_1(D) = 1 + D^3 + D^{31}$, $g_2(D) = 1 + D^{28} + D^{31}$

Table 3.1: The list of polynomials often used in communication systems.

the number of processed chips from $R \times L = 200$ to 400. It can be concluded from Fig. 3.4 that $g_1(D)$ and $g_2(D)$ perform better, than the rest of them because they have *less connections*, hence they impose *less grave error propagation*. Furthermore, the GP $g_2(D)$ performs better than $g_1(D)$, since its *second tap* is connected to *a higher index*, which is 3 as compared to $g_1(D)$, which is connected to chip-index 2. It also *mitigates the noise-propagation effects*. Hence, this significant gain of 3 dB is because of the increased number of $L = 80$ iterations. It can be inferred that allowing more decoding iterations to occur in the SISO decoder helps to achieve an infinitesimally low P_e at low SNRs. Furthermore, when comparing the other 5^{th} order polynomials having more than three taps, it can be observed that $g_3(D)$ performs better than the rest, because it only has *one consecutive tap*, whereas the others have two consecutive taps. Thus the performance of $g_3(D)$ is better than $g_4(D)$, $g_5(D)$ and $g_6(D)$. Now the question arises, why $g_4(D)$ performs better than $g_5(D)$ or $g_6(D)$. The reason is simple because the third tap of $g_4(D)$ is connected to a higher index of 3, while that of $g_5(D)$ is connected to a lower index of 2, hence $g_4(D)$ imposes less grave noise propagation. Finally, it can be concluded from Fig. 3.4 that the performance of the polynomials depends upon three factors:

- Number of connecting taps;
- Number of consecutive taps;
- Location of the highest connected tap.

When comparing polynomials of the same order, less connecting taps give better performance. When the total number of connecting taps is the same, the polynomials with less consecutive taps perform better. If both the number of connecting and number of consecutive taps are the same, then the location of the second connecting tap plays an important role. Generally, taps with higher second index perform better than the lower second-index taps. Table 3.2 summaries our comparisons for the polynomial order of $m = 5$.

3.2.2 Performance of Polynomials in the $m = 6$ Group

For the analysis of the set of GP associated with $m = 6$ we have generated all the six existing polynomials, which are used in our RSSE model to produce the P_e versus SNR results. The configuration of these polynomials is listed in Table 3.1. To understand the behavior of these polynomials Fig. 3.5 shows the P_e versus SNR performance in dB, where the total number of received chips processed are $L \times R = 40 \times 6 = 240$ and $80 \times 6 = 480$. Similar trends were observed in Fig. 3.5 to those of Fig. 3.4. It can be inferred that the influence of noise is more grave in case of having a higher number of taps. Now if we compare the polynomials in this group, we observe that all these polynomials have at least two consecutive taps, but the

Poly-no-mial	Total Taps	Consec-utive Taps	Second tap location in the GP	Third tap location in the GP	Fourth tap location in the GP	E_c/N_0 $[dB]$ at $P_e = 10^{-5}$ when $L = 80$ iterations
g_1	3	0	at Tap 2	-	-	-5.5
g_2	3	0	at Tap 3	-	-	-5.9
g_3	5	1	at Tap 4	at Tap 3	at Tap 2	-3.0
g_4	5	2	at Tap 4	at Tap 3	at Tap 1	-4.2
g_5	5	2	at Tap 4	at Tap 2	at Tap 1	-2.5
g_6	5	2	at Tap 3	at Tap 2	at Tap 1	-2.2

Table 3.2: The polynomial performance for $m = 5$ depends upon the number of consecutive taps as well as on the index of the second connecting tap present in the feedback.

performance of $g_3(D)$ is better than that of $g_4(D)$, $g_5(D)$ and $g_6(D)$, because the position of the second connecting tap in $g_3(D)$ is located at a higher index than that of the other GPs of this group having four taps. Hence, it can be concluded that the performance depends both upon the number of consecutive taps and on the location of the second tap present in the generator polynomial.

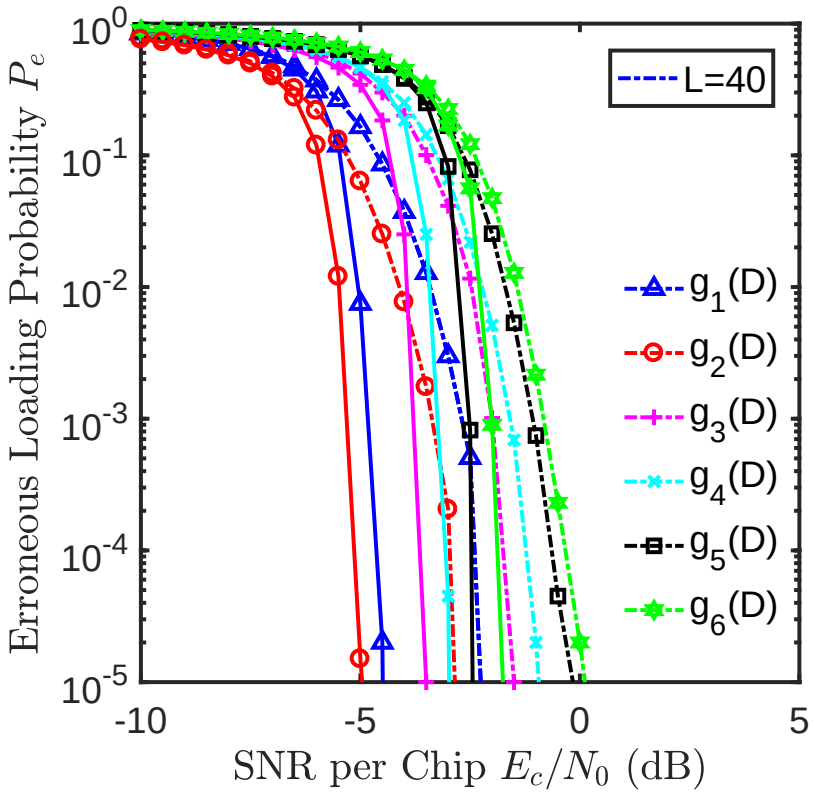


Figure 3.5: Six polynomials of $m = 6$ are characterized for transmission over an AWGN channel, when $L = 40$ and $L = 80$.

Poly--no--mial	**Total Taps**	**Consecut--ive Taps**	**Second tap location in GP**	**Third tap location in GP**	E_c/N_0 $[dB]$ **at** $P_e = 10^{-5}$ **when** $L = 80$ **iterations**
g_1	3	1	at Tap 1	-	-4.7
g_2	3	1	at Tap 5	-	-5.2
g_3	4	2	at Tap 5	at Tap 4	-3.5
g_4	4	2	at Tap 5	at Tap 3	-3.0
g_5	4	2	at Tap 5	at Tap 2	-2.5
g_6	4	2	at Tap 4	at Tap 3	-1.9

Table 3.3: The polynomial performance for $m = 6$ depends upon the number of consecutive taps as well as on the index of the second and third connecting tap present in the feedback.

In Table 3.3 we conclude that the performance of the RSSE scheme depends upon two factors, namely on the number of connecting taps and on the location of the second tap present in the polynomial order.

3.2.3 Performance of Polynomials in the $m = 13$ Group

In this section our simulations are carried for transmission over an AWGN channel for polynomial orders of $m = 13$. In this group we have seven polynomials, which are compared to each other in terms of their P_e versus SNR performance in dB. We have generated Figs. 3.6 and 3.7, where again, seven 13^{th} order polynomial are utilized.

In Fig. 3.6 we have plotted P_e of the seven polynomials at $L = 40$ to quantify their performance. Observe in Table 3.1 that all the polynomials in this group have at least one consecutive tap, thus the performance of these GPs is similar to each other. Having said that, $g_1(D)$ outperforms the rest of the GPs, because it has five connecting taps, whereas the rest of the group has more than five connecting taps. It can be observed that as the number of connection taps increases, the P_e performance degrades. The performance of $g_6(D)$ and $g_7(D)$ is the worst, since both have eleven taps, but $g_6(D)$ has a slightly better performance, because its second tap is connected to a higher index than that of $g_7(D)$. From the simulation result of Fig. 3.6 we can deduce that GPs having less taps perform better, because they impose less grave error propagation. In a nutshell, it can be concluded that GPs having *more taps are more gravely influenced* by the noise and thus they *benefit less* from an iterative scheme.

Similar trends were observed in Fig. 3.5, which indicates that $g_1(D)$ outperforms all the GPs present in this group because of having the least connecting taps. It can be observed that the influence of noise is directly linked to *the number of connection*

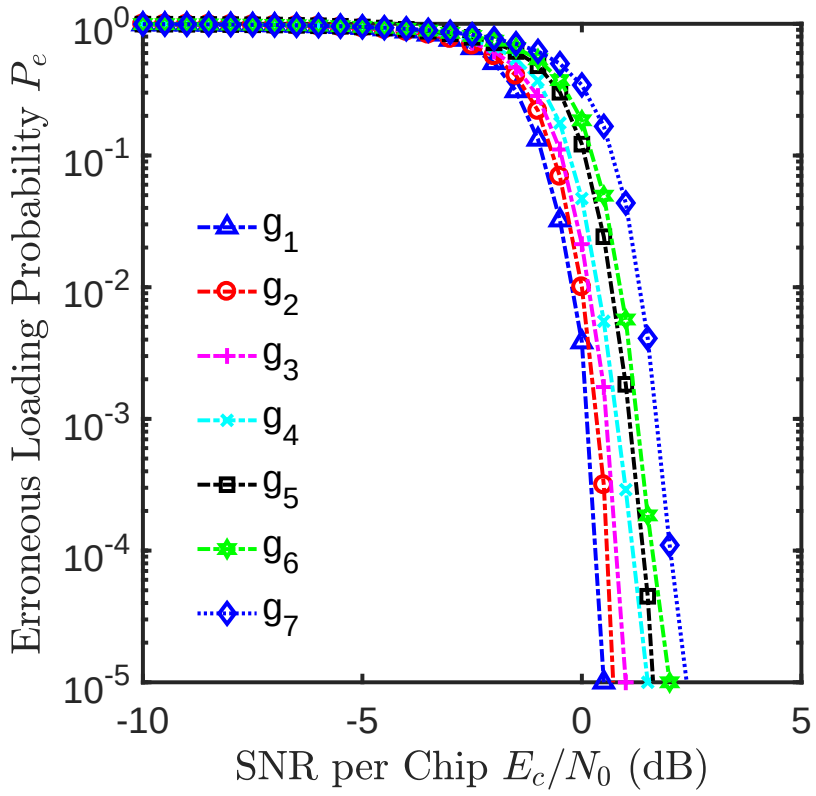


Figure 3.6: Seven polynomials of $m = 13$ are characterized for transmission over an AWGN channel, when $L = 40$.

taps as well as *the index of consecutive taps*. The performance of all the GPs is summarized in Table 3.4.

3.2.4 Performance of Polynomials in the $m = 15$ Group

In this section seven 15^{th} order GPs are evaluated in terms of their P_e versus SNR performance, which are listed in Table 3.1. According to Fig. 3.8, the total number of received chips is $L \times R = 40 \times 15 = 600$ and $80 \times 15 = 1200$, which are processed by the SISO decoder. It is observed that $g_1(D)$ and $g_2(D)$ perform better than the rest of the GPs in this group, because both have three taps. Furthermore, $g_2(D)$ performs better than $g_1(D)$ because $g_2(D)$ has no consecutive taps, whereas $g_1(D)$ has one pair of consecutive taps, since the performance is directly linked to the number of consecutive taps, as discussed in Figs. 3.4 and 3.5. Comparing the other GPs available in this group, $g_3(D)$ performs better because it has four taps, whereas the rest of the GPs have more than four taps. Thus, it can be concluded that the performance depends both on the total number of taps and on the number of consecutive taps, as discussed earlier in Figs. 3.4 and 3.5 as well as in Table 3.2. These GPs are characterized in Table 3.5, where it can be seen that GPs having *less taps* have a higher *likelihood of accurate extrinsic information* for the SISO acquisition model. Consequently, GPs having fewer taps may be preferred, since the malevolent

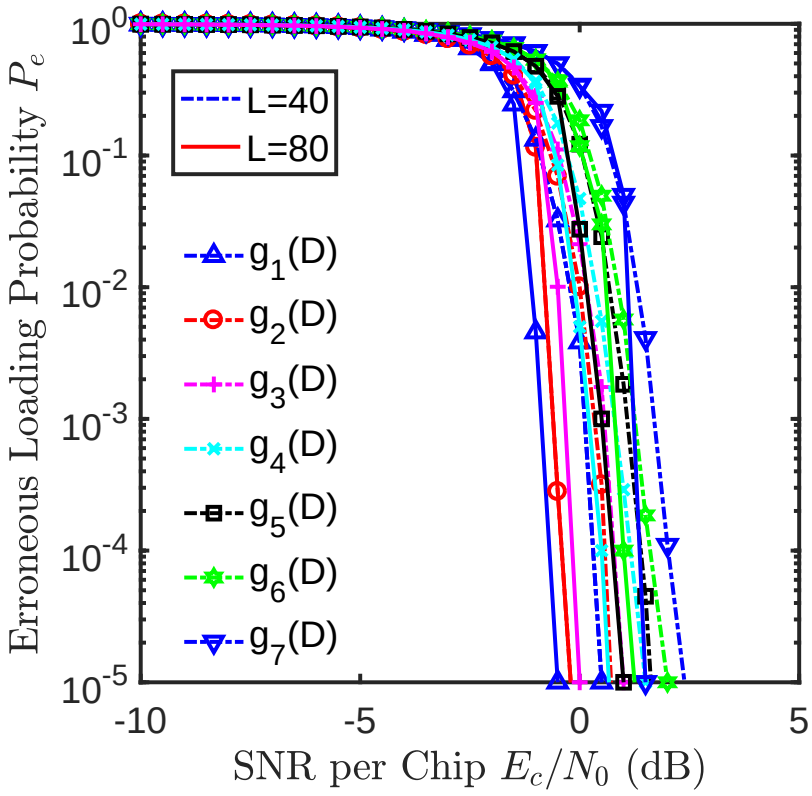


Figure 3.7: Seven polynomials of $m = 13$ are characterized for transmission over an AWGN channel, when $L = 40$ and 80.

effects of noise contaminates their chips less gravely, than those having more taps, as discussed in the section concering both $m = 5$ and $m = 6$.

3.2.5 Performance of Polynomials in the $m = 23$ Group

The family of seven 23^{rd} order GPs is investigated in this section for transmission over an AWGN channels, which are listed in Table 3.1. Figs. 3.9 and 3.10 show their performance in terms of P_e versus SNR expressed in dB. In Fig. 3.9 the number of iterations is $L = 40$, where $g_1(D)$ performs better than the rest of the GPs, because it has less connecting taps than the other GPs, which have more than three taps. Furthermore $g_2(D)$, $g_3(D)$ and $g_4(D)$ have five connecting taps, but $g_2(D)$ has no consecutive taps, thus its performance is better than those of $g_3(D)$ and $g_4(D)$. Moreover when comparing $g_3(D)$ with $g_4(D)$, $g_3(D)$ has one pair of consecutive tap while $g_4(D)$, where $g_4(D)$ has two pairs of consecutive taps. Therefore, $g_4(D)$ needs more iterations to achieve the desired performance. Hence, this result reflects again that more taps have inferior performance than their counterparts having less taps.

Similar trends were also observed in Fig. 3.10. The summary of these results can be tabulated in Table 3.6.

Poly-no-mial	**Total Taps**	**Consecut-ive Taps**	**Second tap location in GP**	E_c/N_0 $[dB]$ $P_e = 10^{-5}$ **for** $L = 80$ **iterations**
g_1	5	2	at Tap 4	-0.8
g_2	7	2	at Tap 12	-0.2
g_3	7	2	at Tap 11	0.0
g_4	7	2	at Tap 10	0.5
g_5	9	2	at Tap 10	1.0
g_6	12	2	at Tap 12	1.2
g_7	12	2	at Tap 11	1.6

Table 3.4: The polynomial performance for $m = 13^{th}$ depends upon the number of consecutive taps as well as on the index of the second connecting tap present in the feedback

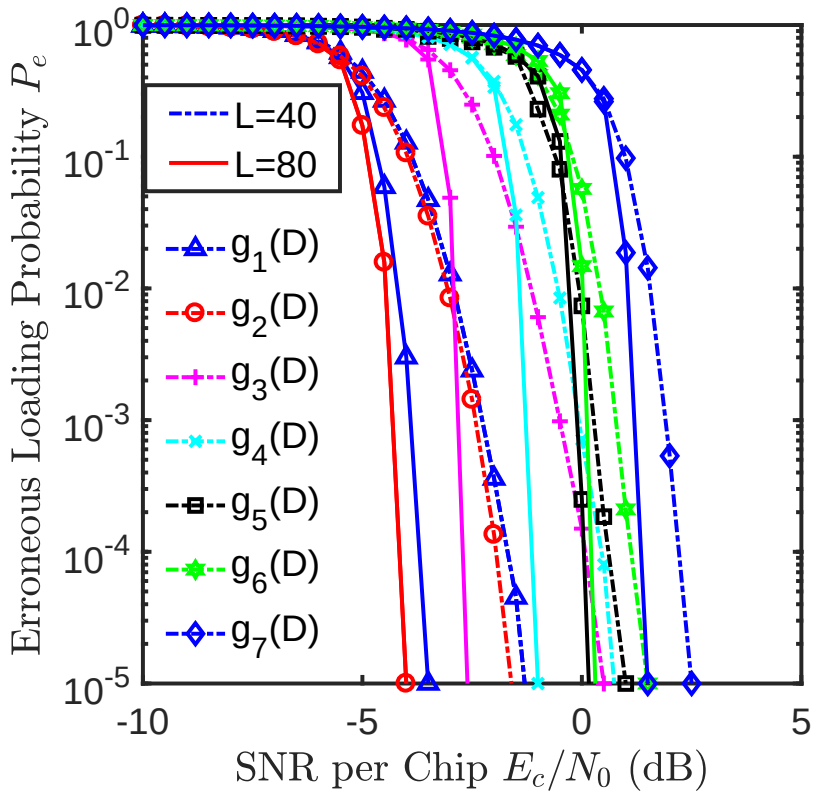


Figure 3.8: Seven polynomials of $m = 15$ are characterized for transmission over an AWGN channel, when $L = 40$ and $L = 80$.

3.2.6 Performance of Polynomials in the $m = 29$ Group

The pair of legitimate 29^{th} order GPs are compared in Fig. 3.11. It can be observed that the total number of received chips is $L \times R = 40 \times 29 = 1160$ and $80 \times 29 = 2320$, which are processed by the SISO decoder. It can be deduced that $g_2(D)$ performs

Poly-no-mial	**Total Taps**	**Consecu-tive Taps**	**Second tap location in the GP**	E_c/N_0 $[dB]$ $P_e = 10^{-5}$ **for** $L = 80$ **iterations**
g_1	3	1	at Tap 1	-4.5
g_2	3	-	at Tap 4	-4.0
g_3	4	-	at Tap 7	-2.5
g_4	5	1	at Tap 10	-1.0
g_5	7	1	at Tap 10	0.6
g_6	7	2	at Tap 12	1.0
g_7	15	1	at Tap 11	2.0

Table 3.5: The polynomial performance for $m = 15^{th}$ depends upon the number of consecutive taps as well as on the index of the second connecting tap present in the feedback. $g_7(D)$ polynomial have consecutive taps from tap location 15 to 2.

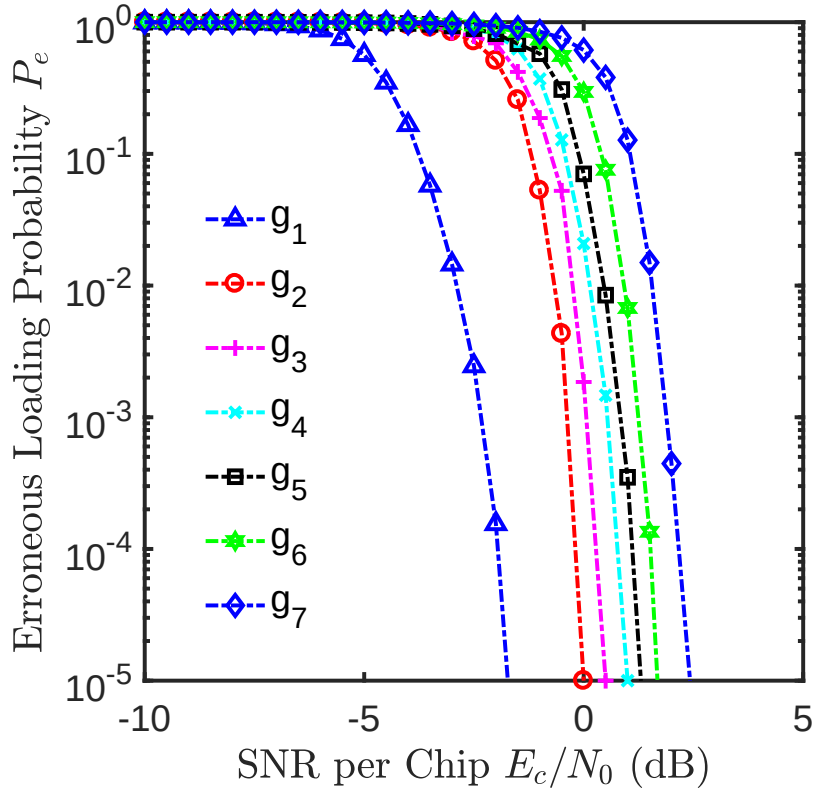


Figure 3.9: Seven polynomials of $m = 23$ are characterized for transmission over an AWGN channel, when $L = 40$.

better than $g_1(D)$, because its second tap is connected to a higher index, namely to index 27, whereas for $g_1(D)$ the second tap location is index 2. This trend is similar to that discussed earlier in Figs. 3.4 and 3.5 and Table 3.2. Furthermore, as expected, the performance improves, when the number of iterations is increased from $L = 40$ to

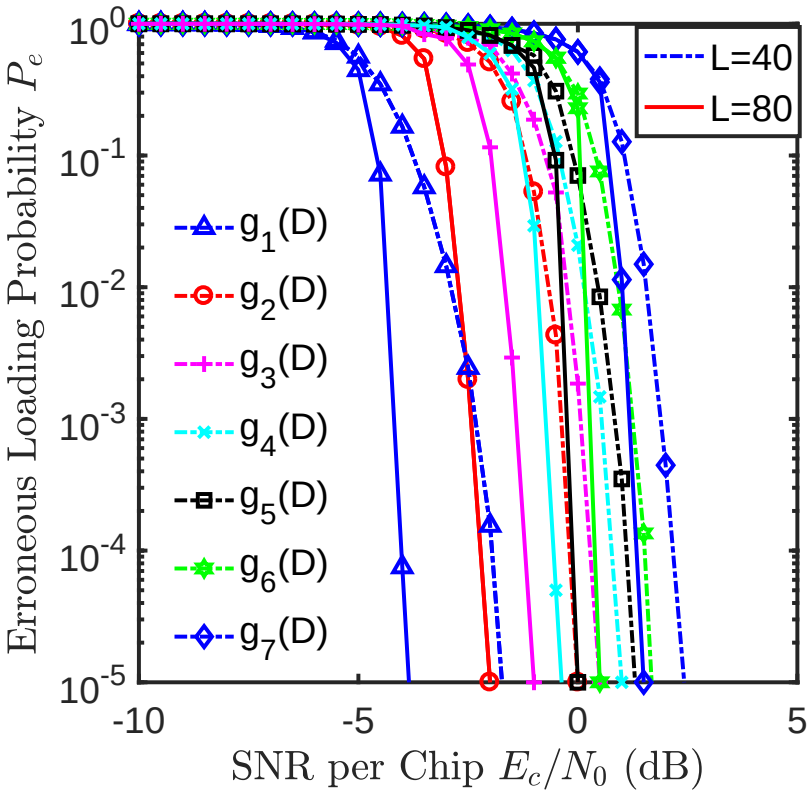


Figure 3.10: Seven polynomials of $m = 23$ are characterized for transmission over an AWGN channel, when $L = 40$ and $L = 80$.

$L = 80$. Since, more chips are processed by the SISO decoder, this increases the gain of the RSSE acquisition scheme. The summary of these polynomials can be observed in Table 3.7, where it can be seen that $g_2(D)$ requires lower SNR value than $g_1(D)$, as discussed earlier in the simulation analysis of GPs belonging to $m = 5$, $m = 6$, $m = 15$ having three taps.

3.2.7 Performance of Polynomials in the $m = 31$ Group

In this section the pair of legitimate 31^{st} order GPs are characterized in terms of their P_e versus SNR performance in Fig. 3.12, where the total number of received chips processed by the SISO decoder is $L \times R = 40 \times 31 = 1240$ and $80 \times 31 = 2480$. It can be inferred that $g_2(D)$ perform better than $g_1(D)$, because its second tap is connected to the higher index of 28, whereas for $g_1(D)$ the second tap is located at index 3. The summary of these GPs can be seen in Table 3.8, where it is observed that the performance depends on the location of the second feedback tap connection, which plays a vital role in achieving a better performance, as discussed earlier when comparing GPs of $m = 5$, $m = 6$ and $m = 15$ having three taps.

Poly--no--mial	**Total Taps**	**Consecut--ive Taps**	**Second tap location in the GP**	E_c/N_0 $[dB]$ $P_e = 10^{-5}$ **for** $L = 80$ **iterations**
g_1	3	-	at Tap 5	-4
g_2	5	-	at Tap 17	-2
g_3	5	2	at Tap 12	-1
g_4	5	2	at Tap 5	-0.5
g_5	6	1	at Tap 22	0
g_6	7	1	at Tap 16	0.5
g_7	9	2	at Tap 15	1.8

Table 3.6: The polynomial performance for $m = 23^{rd}$ depends upon the number of consecutive taps as well as on the index of the second connecting tap present in the feedback.

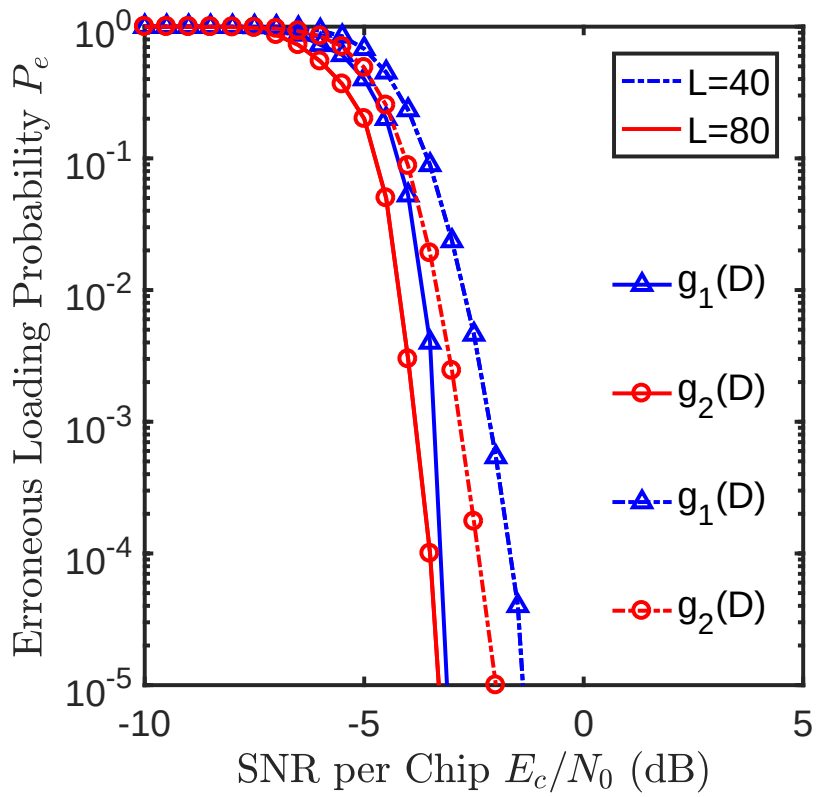


Figure 3.11: Two polynomials of $m = 29$ are characterized for transmission over an AWGN channel, when $L = 40$ and $L = 80$.

3.3 Summary

In this chapter we have evaluated many different GPs associated with $m = 5, 6, 13, 15, 23, 29$ and 31 in terms of their P_e versus the SNR performance expressed in dB. Comparing all GPs leads to difficulty in understanding the overall trends. Therefore

Poly-no-mial	Total Taps	Consecut-ive Taps	Second tap location in the GP	E_c/N_0 $[dB]$ at $P_e = 10^{-5}$ for $L = 80$ iterations
g_1	3	-	at Tap 2	-3.0
g_2	3	-	at Tap 27	-3.3

Table 3.7: The polynomial performance for $m = 29^{th}$ depends upon the number of consecutive taps as well as on the index of the second connecting tap present in the feedback.

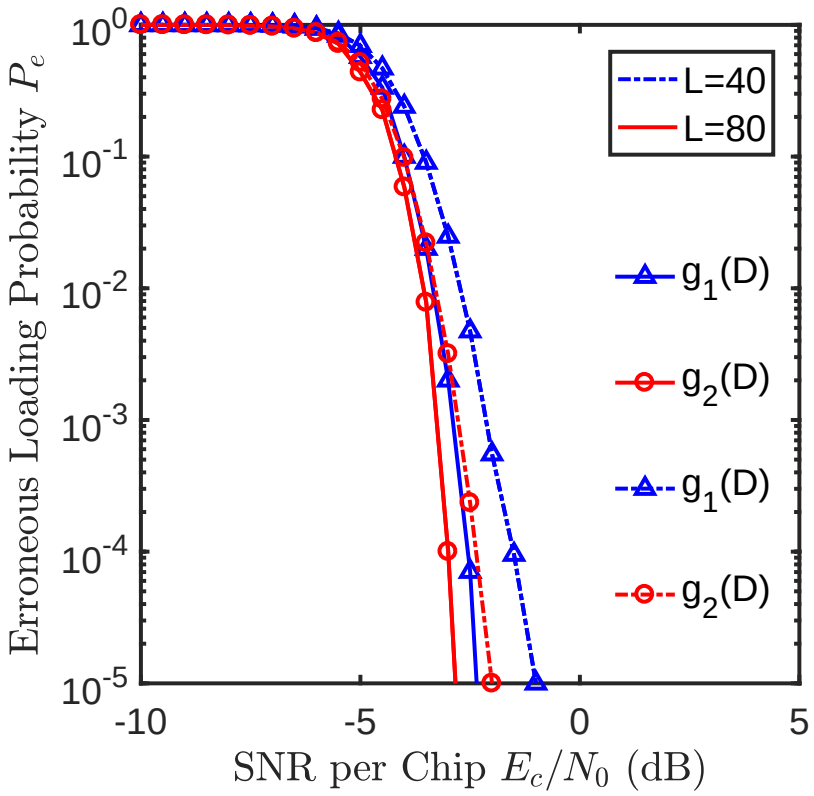


Figure 3.12: Seven polynomials of $m = 31$ are characterized for transmission over an AWGN channel, when $L = 40$ and $L = 80$.

we have taken the best two or worst two GPs of each group and compared them to the other groups to deduce our findings. Invoking the powerful iterative SISO decoding principle rather than hard decisions is capable of further improving the performance [16, 92, 121]. Among these GPs having similar orders, we chose the best two or three GPs based upon their P_e versus SNR performance characterized by our simulation results using the RSSE acquisition scheme. The RSSE scheme is constituted of four blocks, which are detailed in Section 3.1. The appealing feature of the RSSE is that it is capable of observing the reliabilities of all the consecutive chips by observing the amplitudes of the LLR values stored in the soft-chip delay units.

The maximum affordable number of iterations is $L = 80$, thus the total number of received chips processed by the SISO decoder is $L \times R$, where R denotes the GP's

Poly--no--mial	**Total Taps**	**Consecut--ive Taps**	**Second connecting location in the GP**	E_c/N_0 $[dB]$ **at** $P_e = 10^{-5}$ **for** $L = 80$ **iterations**
g_1	3	-	at Tap 3	-2.4
g_2	3	-	at Tap 28	-2.8

Table 3.8: The GP performance for $m = 31^{st}$ depends upon the number of consecutive taps as well as on the index of the second connecting tap present in the feedback.

Groups	**Polynomials**	**Representation of polynomials**
A	$g_1(D)$, $g_2(D)$	$(2, 5)$, $(3, 5)$
	$g_3(D)$, $g_4(D)$	$(1, 6)$, $(5, 6)$
B	$g_6(D)$, $g_7(D)$	$(1, 15)$, $(4, 15)$
	$g_8(D)$,	$(5, 23)$,
	$g_{10}(D)$, $g_{11}(D)$,	$(2, 29)$, $(27, 29)$
	$g_{12}(D)$, $g_{13}(D)$	$(3, 31)$, $(28, 31)$
C	$g_5(D)$, $g_9(D)$	$(1, 3, 4, 13)$, $(5, 11, 17, 23)$
D	$g_{14}(D)$	$(2, 3, 5, 6, 7, 8, 9, 10, 11, 13)$
	$g_{15}(D)$	$(1, 2, 3, 4, 5, 6, 8, 10, 12, 13)$
	$g_{16}(D)$	$(2, 3, \ldots, 15)$

Table 3.9: GPs invoked for our RSSE scheme, where g_{16} has consecutive feedback taps ranged from 2 to 15 and 0 in all polynomials was removed for simplicity.

order. Please note that the curves are plotted as P_e versus E_c/N_0 expressed in dB. Our comparisons in terms of P_e versus SNR are recorded for various GPs, as shown in Fig. 3.13, where the Groups A and B are created by grouping the curves and GPs of similar shape together. Here, the GPs in each group have three feedback taps. For clarity, the GPs are grouped together on the basis of their performance.

In Group A, we have four GPs, namely $[g_1(D), g_2(D)]$ and $[g_3(D), g_4(D)]$ having orders 5 and 6, respectively. The GP $g_2(D)$ has a better performance than $g_1(D)$, since its second feedback tap is connected to the third position of the entire feedback tap arrangement (tap3), whereas in g_1 the second feedback tap is linked to the second position (tap2), as described in Table 3.9. It is observed that the GPs $g_3(D)$ and $g_4(D)$ have consecutive taps, where $g_3(D)$ performs worse because its consecutive taps are at lower connection indices of 0 and 1 (taps 0 and 1), whereas the consecutive taps of $g_4(D)$ are located at higher connection indices of 5 and 6 (taps 5 and 6). Explicitly, $g_2(D)$ has a better performance than the rest, because it belongs to a

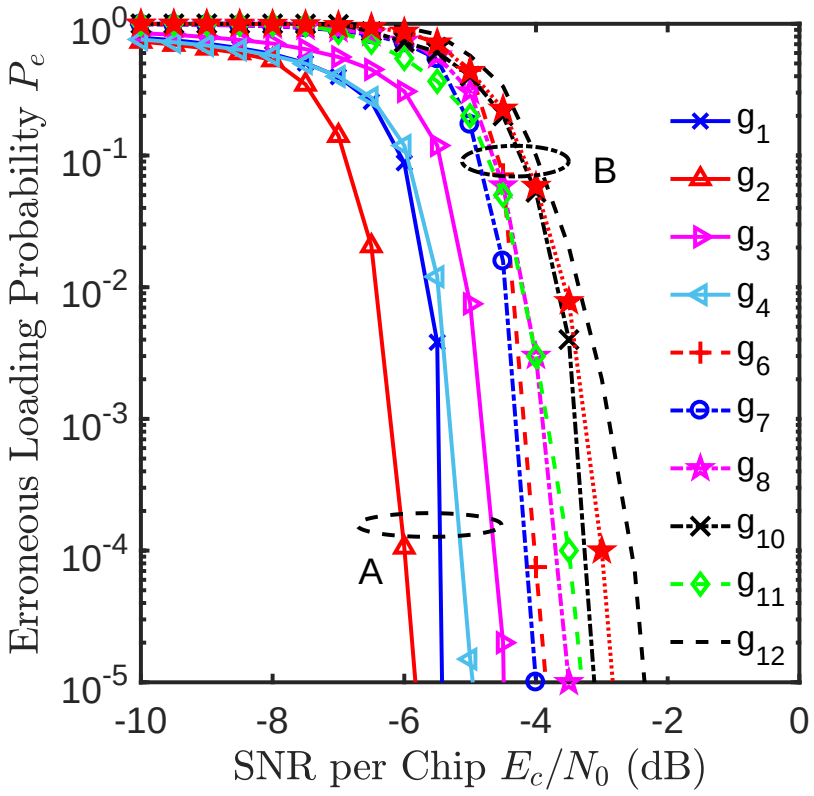


Figure 3.13: Performance comparison between GPs having three feedback taps, where A and B represent groups of primitive polynomials showing similar performance.

lower-order GP and its second feedback tap is connected to a higher index than the second tap of $g_1(D)$.

In Group B of Fig. 3.13, we have seven GPs, namely $g_6(D)$, $g_7(D)$, $g_8(D)$, $g_{10}(D)$, $g_{11}(D)$, $g_{12}(D)$, and $g_{13}(D)$ as portrayed in Table 3.9, where $g_6(D)$ and $g_7(D)$ have the order of 15. Here, $g_7(D)$ performs better than $g_6(D)$, since the former does not contain any consecutive feedback taps. Namely, in $g_6(D)$ the consecutive feedback taps are present at indices 0 and 1 (taps 0 and 1). Furthermore, $g_8(D)$, $[g_{10}(D), g_{11}(D)]$, and $[g_{12}(D), g_{13}(D)]$ have orders of 23, 29, and 31, respectively, as shown in Table 3.9. Observe in Fig. 3.13 that the performances of $g_{13}(D)$, $g_{11}(D)$, $g_{10}(D)$, and $g_8(D)$ are slightly better than that of $g_{12}(D)$. It also transpires from Fig. 3.13 that if the taps are non-consecutive and the GP's order is lower, then the SNR required for achieving a given P_e will be lower, especially for lower-order GPs. In contrast to Fig. 3.13 focusing on GPs having three feedback tap, let us now vary the number of feedback taps. The corresponding P_e versus SNR performance is recorded for the GPs in Fig. 3.14.

Observe in Fig. 3.14 that the groups A, C, and D are formed, where the corresponding GPs are again grouped together according to their performance trend. In group A, $g_2(D)$ is chosen owing to its better P_e versus SNR performance. Group C has $[g_5(D), g_9(D)]$, whereas $g_{14}(D)$, $g_{15}(D)$, and $g_{16}(D)$ belong to Group D of

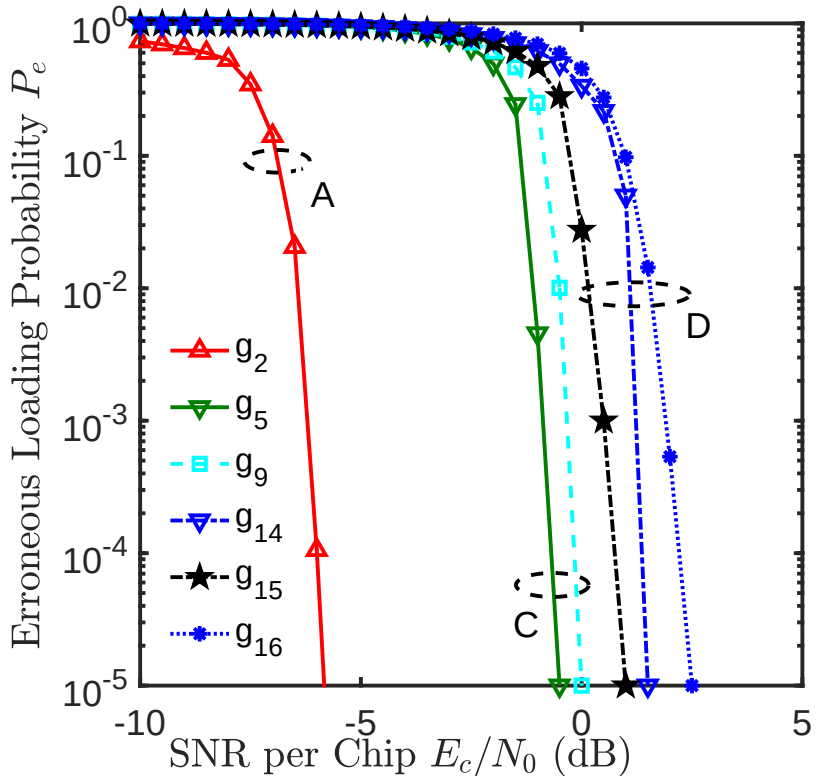


Figure 3.14: Performance comparison between primitive polynomials having a different number of feedback taps, where A, C, and D represent the groups of GPs having similar behavior.

Number of consecutive tap-groups	**Representation of primitive polynomials**
0	$g_1(D)$, $g_2(D)$, $g_7(D)$, $g_8(D)$, $g_9(D)$, $g_{10}(D)$, $g_{11}(D)$, $g_{12}(D)$, $g_{13}(D)$
1	$g_3(D)$, $g_4(D)$, $g_6(D)$
2	$g_5(D)$
8	$g_{15}(D)$, $g_{14}(D)$
13	$g_{16}(D)$

Table 3.10: Primitive polynomials according to the number of consecutive feedback taps.

Table 3.9. As visualized in Fig. 3.14, the SNR performance of the GPs deteriorates as the number of consecutive feedback taps increases. More explicitly, $g_{16}(D)$ has more consecutive feedback taps than the rest of the group, namely 2 to 15 taps, where each feedback-sample is noise contaminated, hence degrading the achievable performance. Upon comparing the performances of GPs having an order of 13, i.e. $g_{14}(D)$ and $g_{15}(D)$ generated using 10 taps, respectively it is found that both GPs

have two consecutive feedback taps. The GP g_{15} leads to better performance, because the connected feedback indices 7, 9, and 11 are absent, whereas in $g_{14}(D)$ we have no feedback tap connections at indices 1, 4, and 12. Therefore, more vacant positions exist at higher-order feedback indices in $g_{15}(D)$ as compared to $g_{14}(D)$, therefore $g_{15}(D)$ performs better. Hence, we infer that the detection capability of the receiver is reduced by the presence of the consecutive feedback taps. The receiver has a better chance of detecting the chips in the presence of noise in case of $g_{15}(D)$ as opposed to that of $g_{14}(D)$, since the detection capability of the receiver is degraded proportionally to the number of consecutive feedback taps.

Group C has $g_5(D)$ and $g_9(D)$, where $g_5(D)$ performs better than $g_9(D)$, because it belongs to lower order polynomial. From our simulation results obtained in Figs. 3.13 and 3.14, we conclude that the low-order GPs outperform the higher-order GPs, because the detrimental influence of noise imposed on the chips of lower-order GPs results in less grave error propagation than for their higher-order counterparts. It is also evident that GPs having different orders exhibit a performance, which depends on the specific number of consecutive feedback taps.

According to our findings in Figs. 3.13 and 3.14 the performance of the GPs depends upon two factors, namely on the number of consecutive taps and on the specific position of connecting taps. Observe in Table. 3.10 that GPs $g_1(D)$, $g_2(D)$, $g_7(D)$, $g_8(D)$, $g_9(D)$, $g_{10}(D)$, $g_{11}(D)$, $g_{12}(D)$, and $g_{13}(D)$ have non-consecutive taps. As seen in Figs. 3.13 and 3.14, the performance of $g_9(D)$ is the worst because it has four connecting taps, whereas the remaining GPs have only two connecting taps. Therefore, the low-order GPs having less connecting taps outperformed their higher-order counterparts, which precipitated the noise-effects by more feedback taps.

After arranging the GPs according to the number of consecutive feedback taps, the desired GPs having a single pair of consecutive feedback taps are $g_3(D)$, $g_4(D)$, and $g_6(D)$. The performance of $g_4(D)$ is better than $g_3(D)$, and $g_6(D)$ because it belongs to the low-order GP and its consecutive feedback tap are arranged at higher indices of 5 and 6 as compared to $g_3(D)$, where the consecutive feedback taps are at indices 0 and 1. Furthermore, when comparing the GPs based upon two or more consecutive taps i.e. $g_5(D)$, $g_{14}(D)$, $g_{15}(D)$, and $g_{16}(D)$ GPs having less consecutive feedback taps results in better performance than those having more consecutive feedback taps.

Finally, let us consider GPs having a similar number of consecutive feedback taps, such as $g_{14}(D)$ and $g_{15}(D)$. Observe in Fig. 3.14 that $g_{15}(D)$ performs better than $g_{14}(D)$, where taps 7, 9, and 11 are absent in g_{15}, while in $g_{14}(D)$ taps 1, 4, and 12 are absent. Therefore, we may infer that the SNR required depends on the specific positions of vacant indices, when comparing GPs having an identical order. Table 3.11 further corroborates our findings by using SNR values obtained in a Rayleigh fading channel. Similarly, $g_2(D)$ has the best SNR value of -4.6 dB at $P_e = 10^{-3}$, whereas g_{16}, g_{14}, and g_{15} are undesirable owing to the presence of more

$g_x(D)$	g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8
E_c/N_0 $[dB]$	-4.4	-4.6	-3.9	-4.2	-0.4	-2	-2.2	-1.2
$g_x(D)$	g_9	g_{10}	g_{11}	g_{12}	g_{13}	g_{14}	g_{15}	g_{16}
E_c/N_0 $[dB]$	-0.2	-1.4	-1.3	-1.5	-1.6	1.4	1.0	1.7

Table 3.11: Performance analysis of GPs under Rayleigh fading channel for different SNR values at P_e=10^{-3}.

consecutive taps.

3.4 Conclusions

In this chapter, the acquisition of m-sequences using the proposed RSSE scheme has been investigated. It has been observed that RSSE acquisition scheme has both an implementation complexity and an initial synchronization time, which are dependent on the number of stages in generating the m-sequence. We conclude that the performance of RSSE scheme depends upon three factors, namely on the order of the polynomial, on the number of connecting taps and on the specific indices of the connecting taps. When comparing GPs of identical order, GPs with less connecting taps will outperform those having a higher number of connecting taps, since the latter precipitated the noise-effects by having more feedback taps. Furthermore, if the connecting taps are same, then GPs with the second highest indices perform better. Therefore, the required SNR depends partially on the specific positions of vacant indices, when comparing GPs having identical orders. Finally, when comparing GPs of different order, the low-order GPs avoids the avalanche-like error-propagation of higher-order GPs, since the noise imposed on the chips of lower-order GPs results in fewer inaccuracy transmission than of higher-order GPs. We infer that the detection capability of the receiver is reduced by the presence of consecutive feedback taps. Thus the receiver having *less connecting taps*, has *a better chance of detecting the chips* in the presence of noise as opposed to that having *more connecting taps*.

Chapter 4

Primitive polynomials for iterative estimation of m-sequences

In this chapter, an *EXtrinsic Information Transfer* (EXIT) Chart assisted approach is used for the convergence analysis of m-sequences using *Recursive Soft Sequence Estimation* (RSSE) in the context of *Nakagami-m fading channels*. As we know that a delay of less than one millisecond is required by low-latency $5G$ wireless communication systems for supporting the 'tactile' Internet. Hence, conventional initial synchronization cannot be readily employed because of its potentially excessive delay. Explicitly, the novelty of our work is based on employing *a new type* of EXIT Charts operating *without using interleavers*. This is a challenge, because the original EXIT charts rely on the employment of *long, high-delay interleavers* for ensuring that the Mutual Information (MI) processed by them becomes uncorrelated in Gaussian distribution. By contrast, the correlation of m-sequences is beneficially exploited during each iteration. The m-sequences are generated using a *self-concatenated* approach. We demonstrate that the m-sequences generated by the lower-order polynomials *maximize the MI* more promptly with the aid of *our RSSE scheme* than those, which belong to a higher-order polynomial. Additionally, when EXIT chart analysis is applied to the lower-order polynomials, they yield a *large area* under the EXIT curves of the inner detector, which results in a higher achievable rate for systems which use m-sequences for Direct Sequence Code Division Multiple Access (DS-CDMA). Furthermore, we show that the erroneous loading probability of low order polynomials is also lower than that of higher-order polynomials at a given signal to noise ratio. Moreover, the polynomials having the *same order but fewer* consecutive taps outperform the polynomials with a higher number of consecutive taps. This chapter deals with the *performance* of m-sequence using *iterative estimation* scheme and their behavior in *fading channels* of mobile communication. Section 4.1 deals with the introduction of m-sequence generated by *iterative estimation* using RSSE acquisition scheme. Section 4.2 covers the system model of RSSE scheme while Section 4.3

deals with the Performance of EXIT Chart and its application in RSSE scheme under Nakagami Fading Channel, Section 4.4 deals with the simulation results while Section 4.5 deals with the performance of Automatic Gain Controller (AGC) and Section 4.6 concludes with the polynomial performance in iterative RSSE scheme under Nakagami Fading Channel.

4.1 Introduction

Wireless Communication is the backbone of telecommunication industries which is progressing at a very rapid pace. To make communication more efficient, reliable and effect we need to improve its basic structure; so that we can reduce *latency*, *throughput* and *secure the correct information* under any noisy channel. We need to obtain *synchronization* more quickly so that all communication should be *protected* and guarded well with less error. In the current era of mobile communication android phones, tablets, notebooks and laptops are in great demand throughout the world, which has resulted in an exponential increase of data traffic [9,16,139,140]. Hence the information transmission over the channel should be as bandwidth-efficient as possible [23, 135, 141]. Fortunately, the *performance of wireless systems* can be enhanced using *iterative decoding*, where *extrinsic soft information* is exchanged between the constituent receiver components [141, 142]. The increased tele-traffic has led to the development of new enabling techniques operating at increased millimetre wave carrier frequencies where more bandwidth is available for small cells [135, 139, 140, 143]. These advances will improve the area spectral efficiency in tele-traffic hot spots, such as stadiums, shopping malls etc. However, the Global Positioning System (GPS) cannot be used for indoor environments as a centralized time reference due to its high building-penetration loss.

Pseudo Noise (PN) sequence acquisition was conceived for the initial synchronization of classic spread-spectrum communication systems [23]. As early as 1965, Ward proposed an m-sequence acquisition arrangement [102], which was later relied upon by the solutions conceived in [105, 92]. The basic principle relies on generating m-chips by a local m-sequence generator based on the most likely received m-sequence. Once a minimum of m-chips have been received, we can update the estimate of the received sequence upon receiving each new chip. Naturally, the received chip may be contaminated by the channel, which may hence lead to loading erroneous values into the local m-sequence generator of the receiver [16, 92]. By invoking the iterative Soft Input Soft Output (SISO) decoding principle we can improve the initial sequence acquisition performance [140, 141, 144].

In this chapter, a Recursive Soft Sequence Estimation (RSSE) scheme is conceived for m-sequences [16, 92, 122], which relies on *soft decision feedback* for improving the performance of the system as compared to the *hard decision approach*, which is

achieved at the cost of a *modest increase* in complexity [16,92]. We will demonstrate that the RSSE scheme advocated performs well in generalized Nakagami-m fading channels. Our novel contributions in this chapter are as follows:

- We conceive a new EXIT chart tool, where the correlation of chips inherent in the m-sequences is exploited.
- We demonstrate that the m-sequences relying on low-order generator polynomials achieve higher mutual information than high-order polynomials after undergoing the same number of RSSE iterations.
- We also show with the aid of EXIT charts that the convergence behavior of low-order polynomials is better than that of the high-order polynomials.
- Low-order polynomials result in lower Erroneous Loading Probability (P_e) at a given Signal to Noise Ratio (SNR) than their higher-order counterparts. Furthermore, having less feedback taps is more beneficial at a given generator polynomial order.
- The initial acquisition delay between the Base Station (BS) and the User Equipment (UE) is minimized, if the generator polynomial has a low number of feedback connections and when these taps are non-consecutive.

4.2 System Model

The RSSE acquisition scheme is illustrated in Fig. 3.2, which consists of four fundamental building blocks, namely 1) the m-sequence generators 2) the soft chip registers 3) the SISO detector and 4) the phase tracking loop. We have discussed all these blocks in detail in Chapter 3, before proceeding to our novel contributions of this chapter, we summarized main procedure of RSSE scheme. Thus according to Fig. 3.2 where the soft chip register has the same number of delay elements as that of the m-sequence generator of the transmitter. These delay units are referred to as soft-chip delay units and they store the instantaneous values of consecutive chips in the form of their Log-Likelihood Ratio (LLR). After obtaining the LLR values, they are loaded into the delay units of the m-sequence generator. The SISO decoder estimates the corresponding value of the soft LLR output after receiving a soft channel output associated with a given chip of the m-sequence. The SISO decoder processes both the *intrinsic information* received from the channel plus the *extrinsic information* related to the same chip based on the *previously decoded* LLR values stored in the soft-chip delay units. The output of the SISO decoder is then shifted to the left-most position of the soft-chip delay units in the soft-chip register,while the soft value in the right-most soft-chip delay unit is discarded. The appealing feature of the RSSE

is that it is capable of observing the reliabilities of all the consecutive chips by observing the *amplitudes of the LLR values stored in the soft-chip delay units*. For more details on the basic procedure of the RSSE scheme please refer to Section 3.1 and the explanation of Figs. 3.2 and 3.3.

Please note, in this chapter we are transmitting the m-sequences over a fading channel, where α_i denotes the fading amplitude, which is assumed to obey the Nakagami-m_l distribution. Furthermore, n_i represents the Additive White Gaussian Noise (AWGN) having a zero mean and noise spectral density of N_0. Now let us proceed to novel contributions on the EXIT chart analysis of our RSSE scheme.

4.3 EXIT Chart Analysis for m-sequence Design

The concept of EXIT charts was introduced by tenBrink [145, 146] as a *powerful tool* of analyzing the *convergence behavior* of iteratively decoded systems. Explicitly, the EXIT chart was originally conceived for predicting the *specific* SNR value, at which a *vanishingly low* Bit Error Ratio (BER) can be achieved. This became possible without performing time-consuming bit-by-bit decoding based Monte Carlo simulations. In this chapter we conceive a *new application* of EXIT charts for predicting the convergence behavior of the polynomials used for the sake of investigating the evolution of the input/output MI exchange between the receiver's SISO components in consecutive iterations. The EXIT chart analysis can be invoked for evaluating the convergence behavior of our iterative acquisition scheme in *off-line mode* in order to evaluate the performance of the different m-sequences based on the mutual information and iterative decoding behavior. In iterative receivers, where there is an exchange of soft-information between the component channel decoders, or between the channel decoder and the demodulator. Once the specific decoders and demodulator components have been decided based on their EXIT curves, the EXIT chart is no longer used. Similarly, in our system, once the best m-sequences have been selected based on their EXIT chart analysis, they are used in a "real-time" fashion, without any real-time employment of the EXIT charts. The number of iterations required for specific m-sequences, the complexity imposed and the SNR required may be predicted based on the EXIT chart. Once the system design is finalized in terms of the specific m-sequence and the number of decoding iterations, to be used only the iterative code-acquisition is performed in "real-time", without calculating the mutual information.

At the transmitter of Fig. 4.1, the m-sequence generator's state is initialized to a predetermined state, which is known at the receiver. In contrast to conventional m-sequence generators, the output of the m-sequence is the feedback chip, which is also transmitted over the channel. In other words, assuming that Binary Phase Shift Keying (BPSK) modulation is used, the value of the ith transmitted chip c_i also

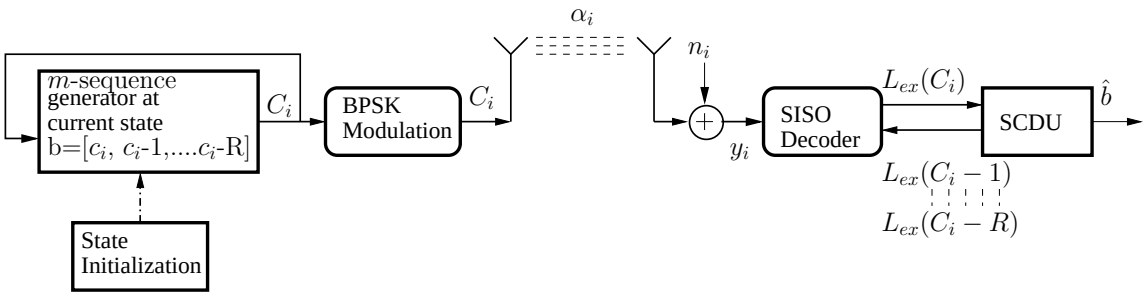


Figure 4.1: The system model used for the RSSE scheme of Fig. 3.2.

becomes the value of the first register stage in the transmitter's m-sequence generator. After it is transmitted over the noisy channel, the received signal is fed to the SISO decoder, along with the stored extrinsic LLR values $L_{ex}(c_{i-1}),\ldots,L_{ex}(c_{i-R})$ in the last R decoding iterations, which were calculated for the R previously transmitted chips. Based on these past extrinsic LLRs, the *a priori* LLR of c_i is computed from Eq. (3.4). Then, the extrinsic LLR of c_i is calculated based on Eq. (3.3), and the same procedure is followed for the next chip c_{i+1}. The SCDU of Fig. 4.1 stores the R most recently calculated extrinsic LLRs and shifts them accordingly. This procedure suggests that the receiver may be viewed as a self-concatenated system, reminiscent of the self-concatenated channel decoder of [147], since the SCDU does not alter the MI and it has a similar role to the interleavers in conventional EXIT charts. This requires a new EXIT chart generation technique for our RSSE scheme. After a predetermined number of decoding iterations, a hard decision is performed on the extrinsic LLR values stored in the SCDU and the current estimated state of the transmitter's m-sequence generator $\hat{\boldsymbol{b}}$ is obtained.

4.3.1 Self-Concatenated Approach

In the self-concatenated approach, there is only a single decoder, which is continuously used with different inputs, as depicted in Fig. 4.1. The first input of the SISO detector is the channel's output. In contrast to the conventional EXIT charts the channel's output is different during each decoding iteration. The second input of the SISO decoder is the output of the SCDU, which again, acts similarly to the interleaver of a conventional iterative receiver, since it essentially shifts the previously calculated extrinsic LLR values. The most likely (2^R-1) chip of the m-sequence has already been hypothesized by the transmitter and the receiver, therefore the SISO decoder is ready to calculate $L_{apr}(c_i)$ based on Eq.(3.4). Please note that the receiver exploits the knowledge of the specific m-sequence that has been selected only at the stage of calculating the *a priori* LLR values. The contents of these shift registers will keep on changing during each SISO iteration, therefore we have to store the most recently calculated R extrinsic LLR values at all times. Hence, we use iterations for the online exploitation of the inherent correlation of the (2^R-1) chips of the m-sequence, as imposed by the m-sequence generator.

4.3.2 Mutual Information

The main feature of using EXIT chart is to calculate the mutual information of the polynomials which can be used to obtain synchronization much quicker than the other polynomials. The concept of mutual information is based on Shannon's work. Suppose that an information source generating 'b' which is equally probable, then the probability of information will be $p_i = \frac{1}{b}$, where $i = 1, \ldots, b$. The information generated by any of d levels can be obtained as:

$$I = \log_2 \frac{1}{p_i} = \log_2(b) \tag{4.1}$$

The average information per symbol emitted by a transmitter is referred as entropy, which is expressed as:

$$H = \sum_{i=1}^{d} p_i I_i = \sum_{i=1}^{b} p_i \log_2 \frac{1}{p_i} = \sum_{i=1}^{b} p_i \log_2(b) \tag{4.2}$$

Whenever the data is transmitted over a non-ideal channel, alteration occurs and hence, the received signals varies. Let $P(X_i)$ is the probability that X_i is transmitted and $P(Y_i)$ is the probability that Y_i is received then $P(X_i/Y_i)$ denotes the conditional probability that X_i is transmitted such-that Y_i received. On the other hand, $P(Y_i/X_i)$ represents the conditional probability that Y_i is received given that X_i is transmitted [106, 144, 148]. The mutual information is expressed as [106, 144]:

$$\begin{aligned} I(X_i, Y_i) &= \log_2 \frac{P(X_i/Y_i)}{P(X_i)} \\ &= \log_2 \frac{P(Y_i/X_i)}{P(Y_i)} \; bits \end{aligned} \tag{4.3}$$

The average mutual information, which gives the average amount of source information collected per received signal, can be calculated as [106, 144]

$$\begin{aligned} I(X_i, Y_i) &= \sum_{x,y} P(X_i, Y_i) \cdot I(X_i, Y_i) \\ &= \sum_{x,y} P(X_i, Y_i) \cdot \log_2 \frac{P(X_i/Y_i)}{P(X_i)} \\ &\quad bits/symbols \end{aligned} \tag{4.4}$$

The encoder and the corresponding SISO decoder are shown in Fig.4.1. The encoder encodes the bit stream 'b' and outputs the bit stream 'b'. On the other hand, the decoder's input comprised of the value *a priori* LLRs denoted by $L_a = L_c \cdot y$ and display out the extrinsic values of LLR denoted by L_e. The mutual information between the information streams and the decoded *a priori* LLRs can be calculated

by I_A=$I(x;L_a)$,$0 \leq\ I_A \leq 1$. This can be used to calculate the *a priori* information of the bits [22, 135]

$$I(X,L_a) \quad = \quad I_A = \frac{1}{2} \cdot \sum_{x=-1,+1} \int_{-\infty}^{+\infty} P_A(\chi|X=x) \cdot \log_2 \frac{2.P_A(\chi|X=x)}{P_A(\chi|X=-1)+P_A(\chi|X=+1)} d\chi \tag{4.5}$$

where $P_A(\chi|X)$ is the conditional PDF linked with the prior LLR L_a and information bits b and both have equal probability $P(c_i=+1)=P(c_i=-1)=\frac{1}{2}$. In order to evaluate the mutual information of the LLR of the system L_a has to be known to the system. So, L_a as an independent zero-mean Gaussian random variable n_A having a variance of σ_A^2, the values of encoder will be $b_D \in \{0,1\}$ or $b_D \in \{1,-1\}$. The *a priori* input L_a is written as

$$L_a = L_c \cdot y + n_A \tag{4.6}$$

where L_c=$\sigma_A^2/2$, since L_a is an LLR-value obeying guassian distribution. Therefore, the conditional PDF of the *a priori* input L_a obeys:

$$p_A(\chi|X=x) = \frac{1}{\sqrt{2\pi}\sigma_A} exp\left(-\frac{(\chi-\frac{\sigma_A^2}{2}\cdot x)^2}{2\sigma_A^2}\right) \tag{4.7}$$

The bit sequence in this case consists of '−1' or '1' which are mapped to '1' or '0' respectively. As the mutual information values increase, the magnitude of the correct LLR also increases until all the values of LLR reach 1, which indicates that the mutual information reaches maximum point, that is 1.

4.4 Simulation Results

In this section, simulation results are presented for characterizing the performance of our RSSE in Rayeligh and Nakagami-m_l fading channels. We assume that the channel magnitude remains constant over a set of R consecutive chips. The *three* different GPs that we compare are $g_1(D)$=$1+D^2+D^5$, $g_2(D)$=$1+D+D^2+D^4+D^5$, and $g_3(D)$=$1+D+D^3+D^4+D^{13}$. The period of the first two GPs $g_1(D)$ and $g_2(D)$ is $2^5-1=31$, while that of the third GP is $2^{13}-1=8191$. The selection criteria of these GPs are based on the number of taps, as well as on their order. More specifically, both $g_1(D)$ and $g_2(D)$ have an order of 5, while $g_3(D)$ has an order of 13. At the same time, $g_1(D)$ has three non-consecutive taps, while $g_2(D)$ has five taps, two of which are consecutive. Finally, $g_3(D)$ also has five taps, two of which are consecutive. In our analysis $R \cdot L$ represents the total number of chips processed by the SISO detector, where R represents the polynomial's order and L represents

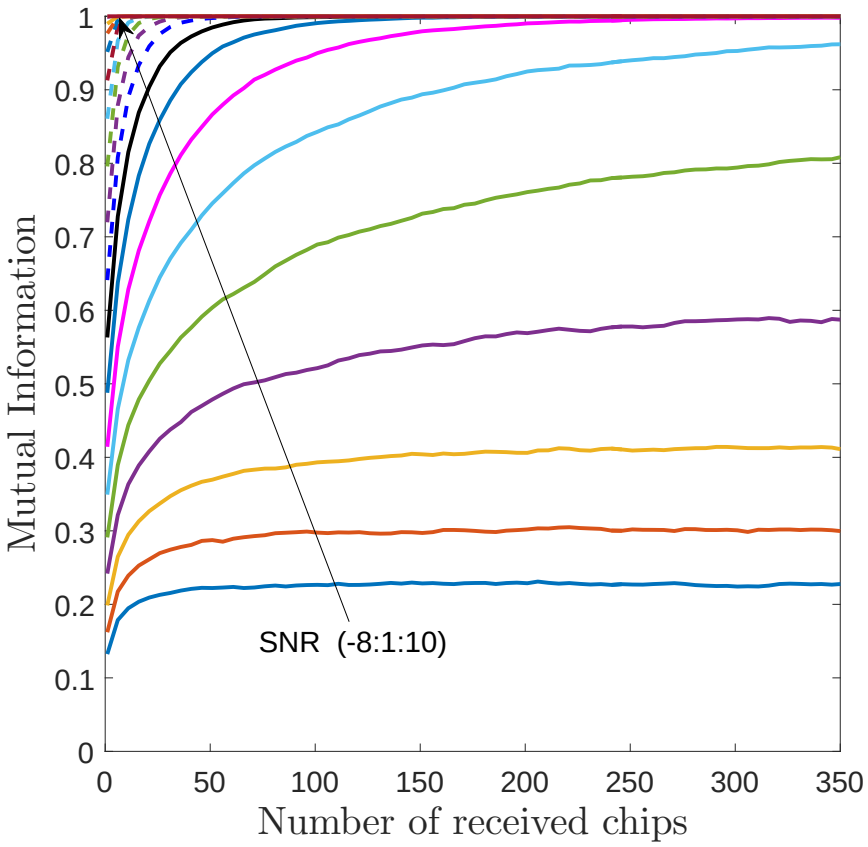


Figure 4.2: Mutual Information (MI) versus the number of received chips for the GP $g_1(D) = 1 + D^2 + D^5$, and for various SNR values.

number of iterations. Before evaluating the Erroneous Loading Probability P_e, we have investigated their performance based on the MI.

In Fig. 4.2, the relationship between the MI and the number of received chips is shown, when the polynomial $g_1(D)$ is employed. It can be observed from Fig. 4.2 that the MI of the polynomial $g_1(D)$ increased for a given number of received chips, when the SNR is increased. At the same time, fewer received chips are required in order to reach the unity MI target, when a higher SNR is encountered. Based on Fig. 4.2, we may conclude that for SNRs above -3 dB, the MI approaches unity after receiving fewer than 300 chips. The generator polynomial $g_1(D)$ evaluated has $R = 5$ register stages, therefore the maximum number of decoding iterations in the figure is $L = 350/R = 350/5 = 70$.

Fig. 4.3 depicts the MI versus the number of iterations at an SNR of 0 dB, when different GPs are employed. In our simulations, the Nakagami fading parameter is $m_l = 3.0$. It may be observed that the MI reaches its maximum value after less than 30 iterations, regardless of the GP employed. It may be noted from Fig. 4.3 the number of chips varies, depending on the generator polynomial used and the number of iterations employed. For example, if $g_1(D)$ is used, since it is associated with order $R = 5$, and it uses $L = 21$ iterations, the number of received chips

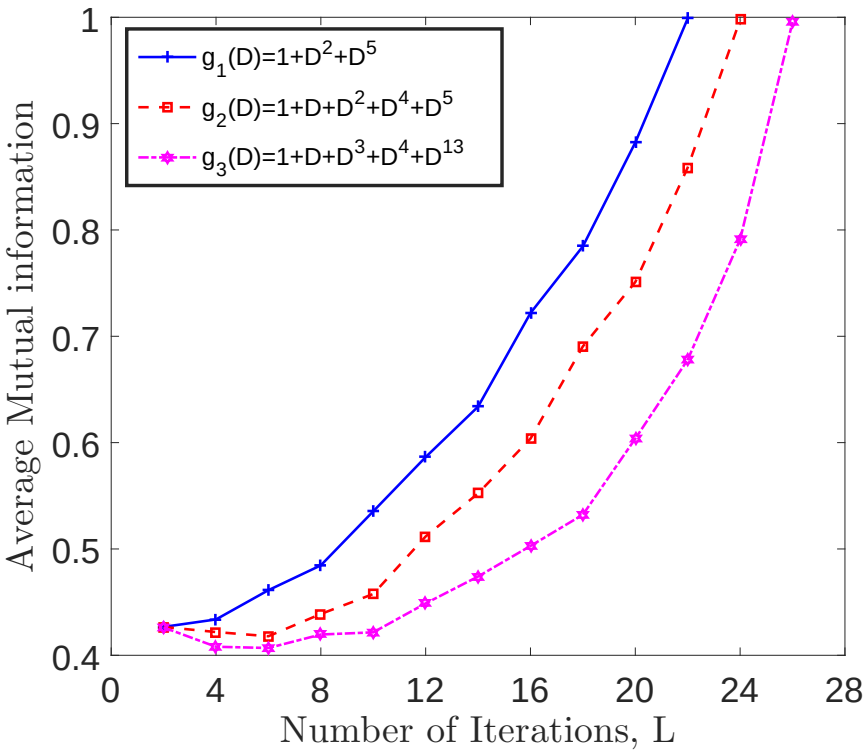


Figure 4.3: Mutual information (MI) versus the number of decoding iterations when SNR= 0 dB and the Nakagami Fading channel has $m_l = 3.0$.

will be $R \cdot L = 105$ which can be visualized in Fig. 4.2 for the particular value of $SNR = 0\ dB$. Since, $g_3(D)$ is used so it is linked with $R = 13$, and utilizes $L = 26$ iterations hence, the received chips will be $R \cdot L = 338$. Fig. 4.3 shows that the GPs $g_1(D)$ and $g_2(D)$ outperform $g_3(D)$ because of their lower order, while $g_1(D)$ achieves the best performance, due to its lower number of employed taps. As, the extrinsic information is dominated by the minimum of the LLR values of all the feedback branches. Therefore, the generator polynomial using a low number of feedback branches has a higher probability of providing the true extrinsic information for the SISO acquisition scheme, than that using a high number of feedback branches, because in the latter the average LLR might still be high, despite having a single low LLR like in the case of $g_1(D)$ with respect to $g_2(D)$. In a nutshell, GPs having a lower number of taps are preferred, because the detrimental influence of noise imposed on their chips results in less grave iteration-induced error propagation than for their counterparts with higher number of taps.

Fig. 4.4 shows an EXIT chart for our self-concatenated iterative RSSE scheme, at an $SNR = -3$ dB. The Nakagami fading value is $m_l = 3.0$. The inner and outer receiver component EXIT curves both represent the same decoder, therefore, they are symmetrical with respect to the diagonal $y = x$ line. The staircase-like curves correspond to the Monte-Carlo simulation-based decoding trajectories of the proposed system. In Fig. 4.4 it can be observed that the polynomials could not reach

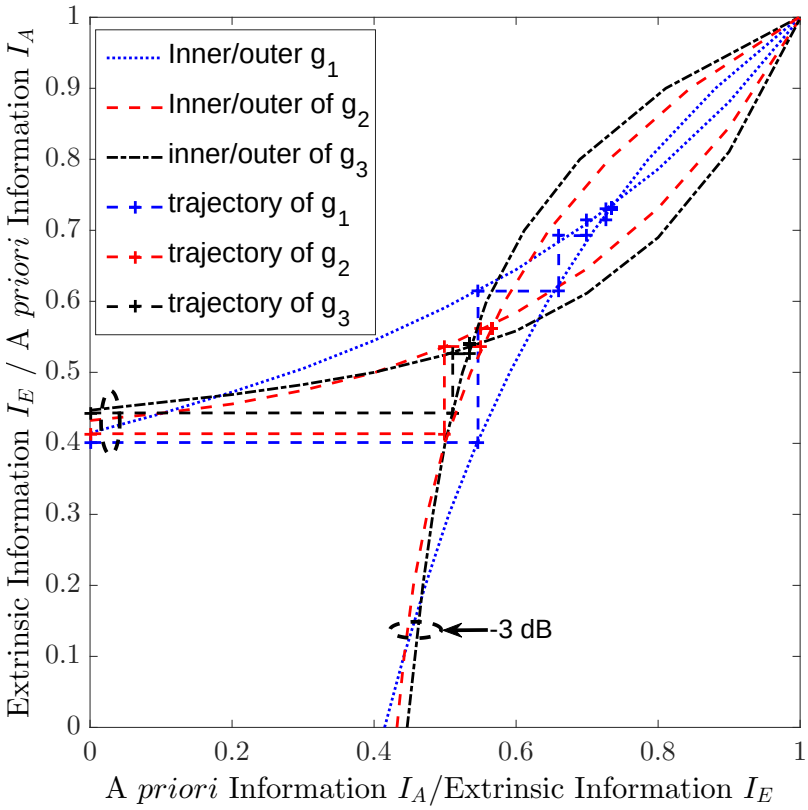


Figure 4.4: EXIT chart for the GPs of $g_1(D) = 1+D^2+D^5$ (blue), $g_2(D) = 1+D+D^2+D^4+D^5$ (red) and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ (black) over Nakagami channels, when $m_l = 3.0$ at SNR=-3 dB.

the maximum point and the top right corner at [1 1] as our inner and outer curves of EXIT charts intersect before this point and the trajectory stops. This indicates that we need to simulate above -3 dB SNR. The same information was obtained from Fig. 4.2 where the relationship between the MI and the number of received chips was plotted.

Indeed, Fig. 4.5 shows an EXIT chart for our self-concatenated iterative RSSE scheme, at an SNR value of -2 dB and 0 dB for the same Nakagami fading value of $m_l = 3.0$. All decoding trajectories approximately match their associated inner and outer component curves. According to the EXIT chart properties of iterative decoding, an infinitesimally low BER may only be achieved by an iterative receiver, if there is an open EXIT tunnel between the EXIT curves of the decoder. At a higher SNR, the open tunnel between the two EXIT curves is wider, hence the trajectory requires fewer iterations for higher SNR values. Furthermore, based on Fig. 4.5, we may conclude that a better match between the decoding trajectory as well as the inner and outer EXIT curves occurs at higher SNR values. In Fig. 4.5 it can be observed that the polynomial $g_1(D)$ requires the fewest decoding iterations to reach the top right corner at [1, 1] for both SNR values. Since $g_2(D)$ requires fewer decoding iterations to reach the [1, 1] corner, we may conclude that it outperforms $g_3(D)$. This

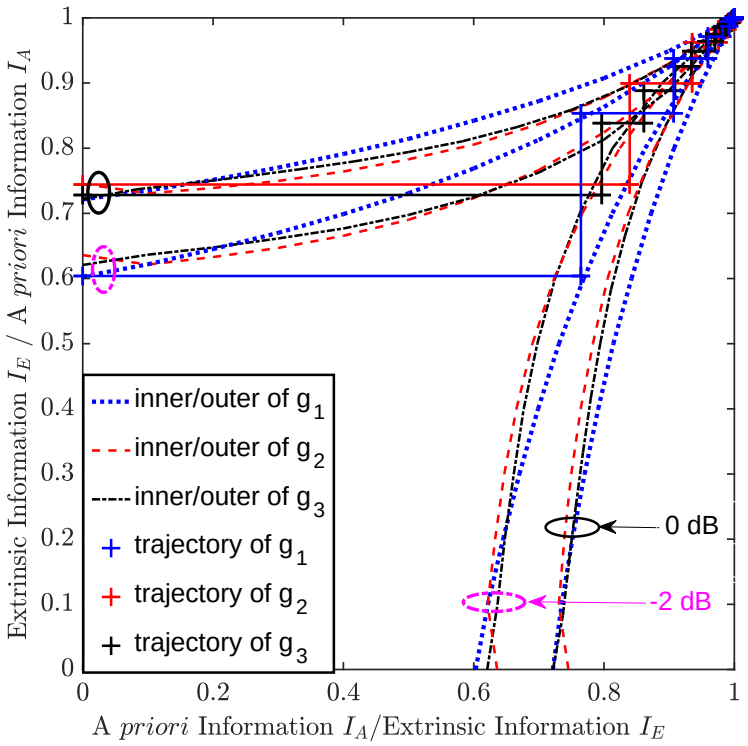


Figure 4.5: EXIT chart for the GPs of $g_1(D) = 1+D^2+D^5$ (blue), $g_2(D) = 1+D+D^2+D^4+D^5$ (red) and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ (black) over Nakagami channels, when $m_l = 3.0$ at SNR=-2 dB and SNR= 0 dB.

shows that the EXIT chart based performance prediction agrees with the MI-trends of Fig. 4.2, and that lower order polynomials have faster convergence capabilities. Therefore, when comparing GPs of different order, higher order GPs perform worse than lower order GPs as they require more data and have large memory component which exhibits excessive confidence in their own soft estimates and hence they do not benefit enough from an iterative scheme.

After investigating the results in EXIT charts, we verified our simulation results in terms of the erroneous loading probability, P_e versus SNR, which is measured in dB. The Nakagami fading value m_l is fixed to 3.0. It can be observed from Fig. 4.6 that the performance of the GPs for $L = 10$ iterations is inferior to that when $L = 100$, since by allowing a higher L more chips are transmitted and more decoding iterations are performed. Therefore, by allowing more decoding iterations L, the SISO decoder will eventually reach the (1,1) point of perfect convergence and P_e will become infinitesimally low. Fig. 4.6 thus demonstrates that as the value of L increases, the performance of all polynomials tends to improve. We may also observe that $g_1(D)$ outperforms the other two GPs, because it only has three taps and none of them are consecutive taps. On the other hand, even though both $g_2(D)$ and $g_3(D)$ have two consecutive taps, $g_2(D)$ performs better, because it has a lower GP order. Hence, it may be deduced that P_e depends both on the number of taps as well as on the GP order.

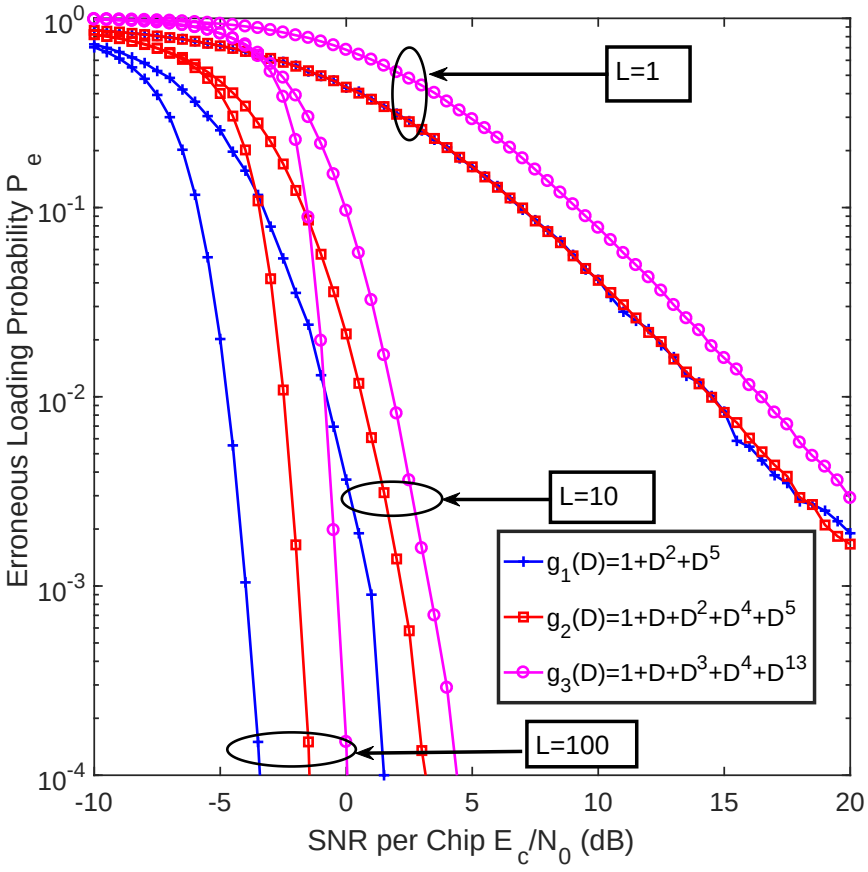


Figure 4.6: Erroneous loading probability P_e, versus the SNR, performance for various numbers of chips invoked into the proposed recursive SISO detector, when transmitting the said polynomials over Nakagami Fading channels when $m_l = 3.0$.

In Fig. 4.7, the erroneous loading probability P_e versus the SNR per chip performance for an m-sequence generated using the generator polynomial of $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ and transmitted over a Nakagami-m_l channel is shown. Note that in Fig. 4.7 the curve corresponding to the parameter $L = 1$ represents the erroneous loading probability of the RSSE acquisition scheme using no recursive SISO decoding. When more channel output chips are involved in the recursive SISO decoding process, a higher detection reliability is achieved resulting in lower erroneous loading probability. For the sake of illustration, let us assume that the transmitted m-sequence can be reliably acquired once the erroneous loading probability is lower than 10^{-3}. From the results of Fig. 4.7 for $m_l = 2.0$ we observe that the m-sequence can be reliably acquired at an SNR per-chip value of 1.5 dB by invoking about $L = 10$ which is equivalent to $10 \times 13 = 130$ chips into the recursive SISO decoding scheme. In contrast, without exploiting the power of recursive SISO decoding, the RSSE acquisition scheme has to operate at an SNR per-chip value of 18 dB, in order to achieve the same erroneous loading probability of 10^{-3}. Explicitly, at the erroneous loading probability of 10^{-3}, the SNR per chip gain is about 16.5 dB, when 130 chips are invoked by the recursive SISO decoding scheme. In general, it is expected that, when more chips can be used during the recursive SISO decoding

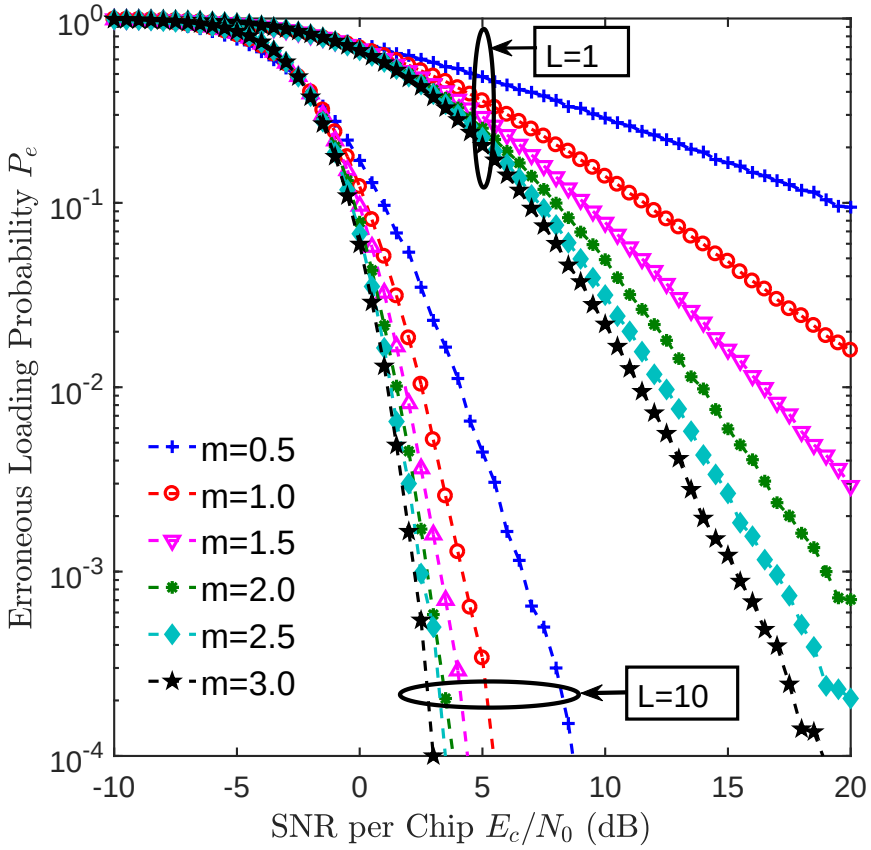


Figure 4.7: Erroneous loading probability P_e, versus the SNR performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g_3(D) = 1+D+D^3+D^4+D^{13}$ over Nakagami Fading channels.

process, increase in gain can be achieved by the proposed RSSE acquisition scheme. Finally, in Fig. 4.7 the performance of the RSSE acquisition system improves with the increase in m_l. The reason for this improvement is that the channel quality improves as the m_l value increases. For $m_l = 1.0$ the channel is Rayleigh faded while for $m_l = 2.0$ it corresponds to the Rician fading with Rician factor $K = 3$.

Fig. 4.8 illustrates the erroneous loading probability P_e versus the SNR per-chip performance for an m-sequence generated using the generator polynomial of $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ and transmitted over Nakagami-m_l channel with fading parameter $m_l = 2.0$. It is observed from the Fig. 4.8 that as the collected number of paths increase the performance of RSSE system improves. This gain in performance is because of the higher diversity order. In 5G networks especially when employing millimeter wave system due to higher bandwidth, there will be more number of paths to be resolved at the receiver side. These multipaths are expected to improve the system performance.

In Fig. 4.9, comparisons in terms of the delay is carried out. It can be seen that polynomial delay depends upon three factors. Firstly, the number of taps present in the polynomial influence delay. Secondly, the number of registers present in gener-

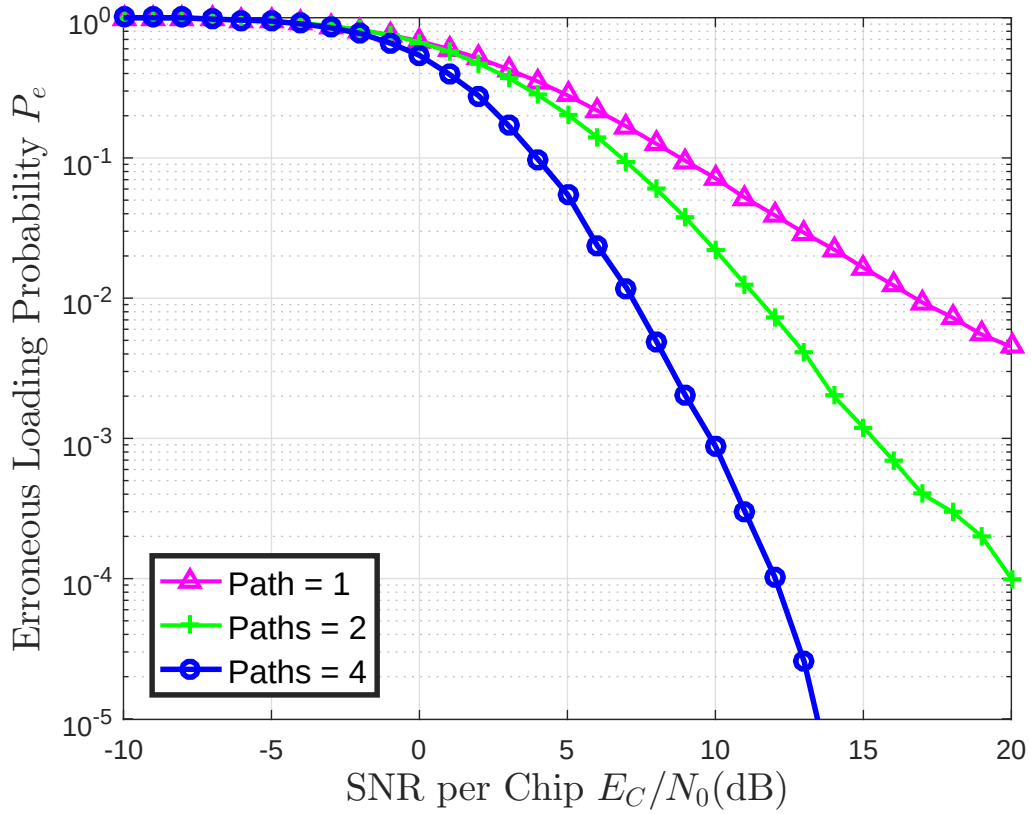


Figure 4.8: Erroneous loading probability P_e, versus the SNR performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g_3(D) = 1+D+D^3+D^4+D^{13}$ over Nakagami Fading channels when $m = 2.0$.

ating the polynomial. Thirdly, it is the number of non-consecutive taps versus the number of consecutive taps present in the polynomial. The delay is obtained by calculating the transfer function of the polynomials. Observing Fig. 4.9 polynomial $g_1(D)$ outperformed $g_2(D)$, and $g_3(D)$ as this polynomial has less number of taps, fewer number of feedback connection, less number of shift registers and no consecutive taps. So, this polynomial will require less time to reach the base station as compared to the other two polynomials. It reduces the latency requirement of the system and makes it suitable for synchronization. Hence, based on the simulation result generated in this Fig. 4.9, it is concluded that low order polynomials have better response time than the higher order polynomials. From this simulation, it becomes obvious that the synchronization of the system depends on the polynomials order and the number of taps presented. As the number of taps increases the delay of the system becomes more because more computational steps are required to achieve an accurate solution. Therefore, to achieve better synchronization less feedback connection polynomial is preferred.

Fig. 4.10 shows the acquisition performance of an m-sequence having a period of $N = 8191$ chips, generated by a 13-th order polynomial. Based on Fig. 4.10, the

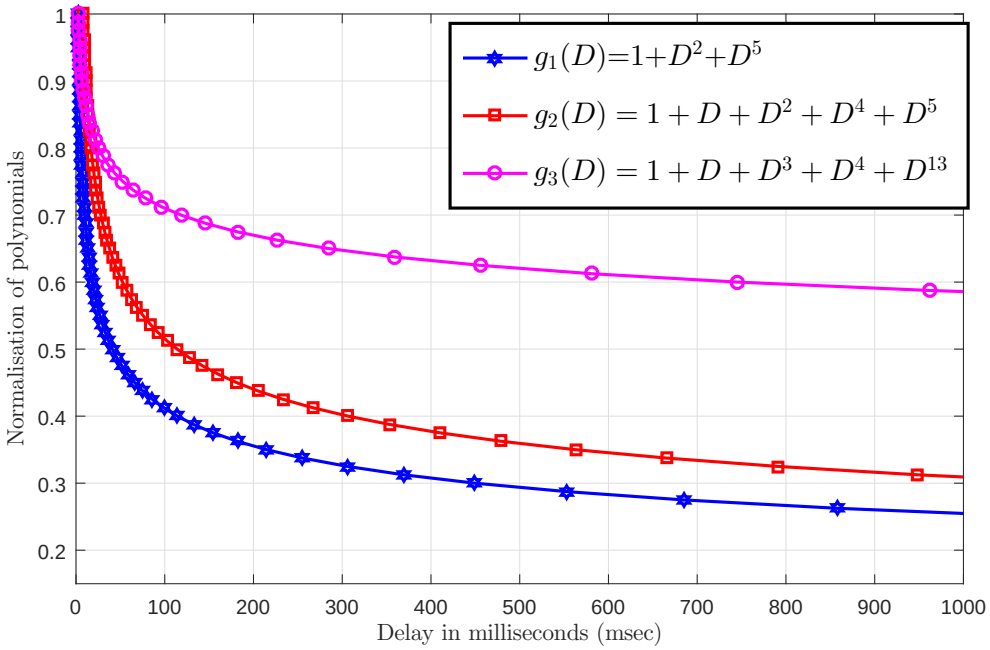


Figure 4.9: Delay is carried out where $g_1(D) = 1 + D^2 + D^5$ (blue), $g_2(D) = 1 + D + D^2 + D^5$ (red) and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ (magenta) over Nakagami channels when $m = 1.5$. The performance of g_1 outperform rest of the polynomials, as few connected connections performs better as the have sharp decline effect than others.

m-sequence can be reliably acquired at an SNR value of -0.5 dB by entering about $40 \times 13 = 520$ chips into the recursive SISO decoder, when transmitted over an AWGN channel. By contrast, when using a correlator, the PN code acquisition scheme has to operate at the SNR value of 9.8 dB in order to achieve the same erroneous loading probability of 10^{-4}. Hence, there is an SNR gain of approximately 10 dB, when the RSSE acquisition scheme is used instead of the correlator at an erroneous loading probability of 10^{-4}. Let τ_D represent the integration dwell time in the context of a conventional serial search-based acquisition scheme [119], which typically assumes values from tens to hundreds of chip intervals. In [119], it has been shown that the mean acquisition time of a conventional serial search-based acquisition scheme cannot be lower than $N_{\tau_D}/2 = 4095\tau_D >> 520$ chips for a sequence length of 8191, chips even if the SNR value is sufficiently high, namely, when the corresponding detection probability approaches one. Hence, the proposed RSSE acquisition scheme significantly outperforms the conventional serial search-based acquisition scheme in terms of its achievable acquisition time. Still referring to Fig. 4.10, we also investigated the acquisition performance of the RSSE acquisition scheme for transmission over different communication channels. We may observe that at a given SNR value, the erroneous loading probability decreases upon increasing the number of received chips entered into the recursive SISO decoder. Furthermore, Fig. 4.10 illustrates that for a given number of received chips entered into the recursive SISO decoder,

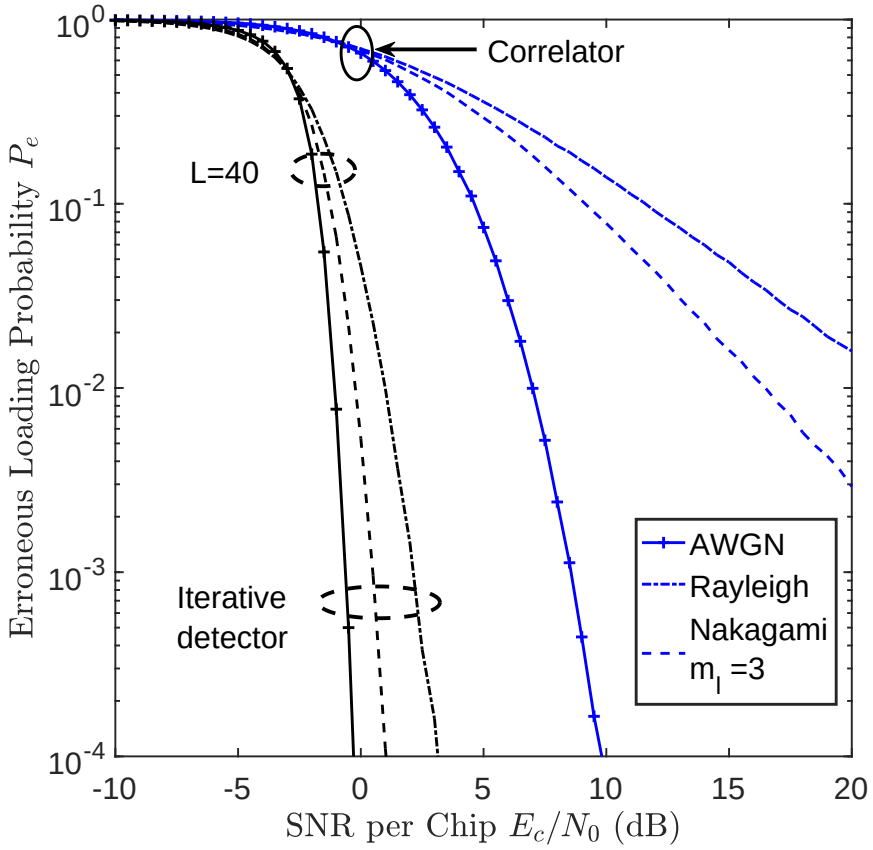


Figure 4.10: Performance comparisons between different communication channels

the SNR gain achieved in Rayleigh fading channels is significantly higher than those in Nakagami channel having $m_l = 3$ as well as in AWGN channels, when using the proposed RSSE acquisition scheme instead of the correlator. However, both for a given number of received chips used by the recursive SISO decoder and for a given SNR, the acquisition scheme communicating over AWGN channels achieves a lower erroneous loading probability than those of the fading channels.

In Fig. 4.11 we have compared the acquisition performances of the RSSE scheme to those of the correlator for m-sequences of various lengths, when transmitting over AWGN channels. More specifically, in Fig. 4.11 we have chosen three polynomials $g_1(D)$, $g_2(D)$ and $g_3(D)$, where $g_1(D)$ and $g_2(D)$ have a polynomial order of 5 and a length of $N = 31$ chips, while $g_3(D)$ has the polynomial order of 13 and a period of $N = 8191$ chips. Fig. 4.11 shows that the m-sequence can reliably be acquired at an SNR value of -3, -2 and -0.5 dB by invoking as few as 40 iterations. By contrast, when a correlator is used, the PN code acquisition scheme has to operate at an SNR value of 10 dB in order to achieve the Erroneous Loading Probability P_e of 10^{-4}. Hence, the attainable SNR gain of using the proposed RSSE acquisition scheme at an P_e of 10^{-4} is about 7, 8 and 9.5 dB, when $g_1(D)$, $g_2(D)$ and $g_3(D)$ are considered, respectively.

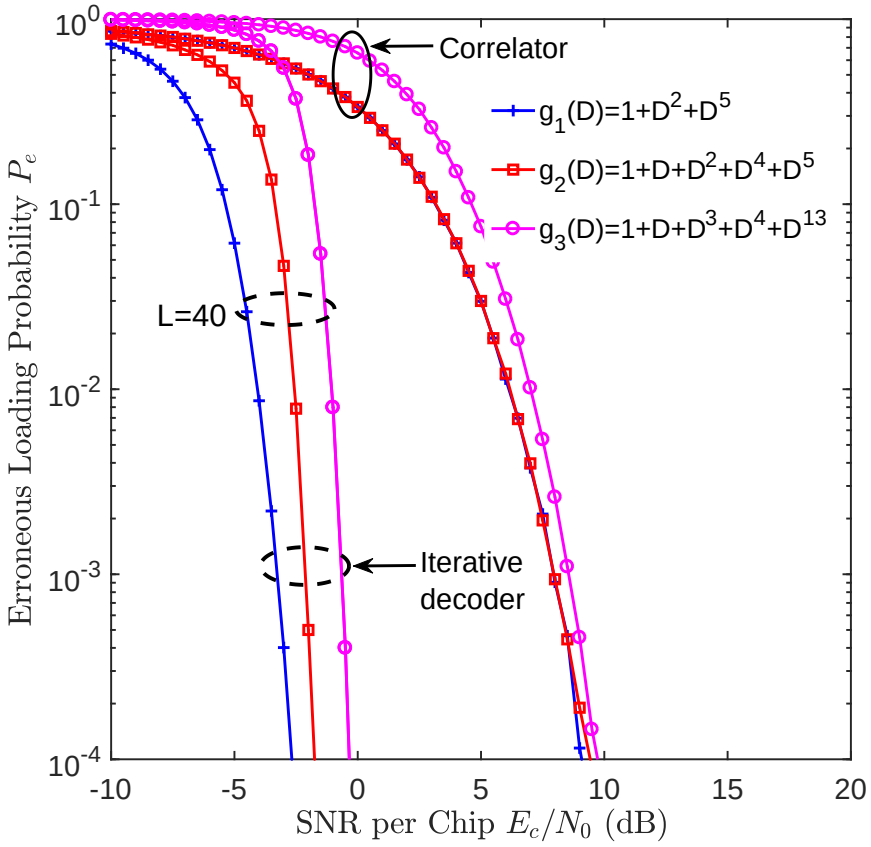


Figure 4.11: Erroneous loading probability P_e versus the SNR performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the generator polynomials of $g_1(D) = 1 + D^2 + D^5$, $g_2(D) = 1 + D + D^2 + D^4 + D^5$ and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ over AWGN channel

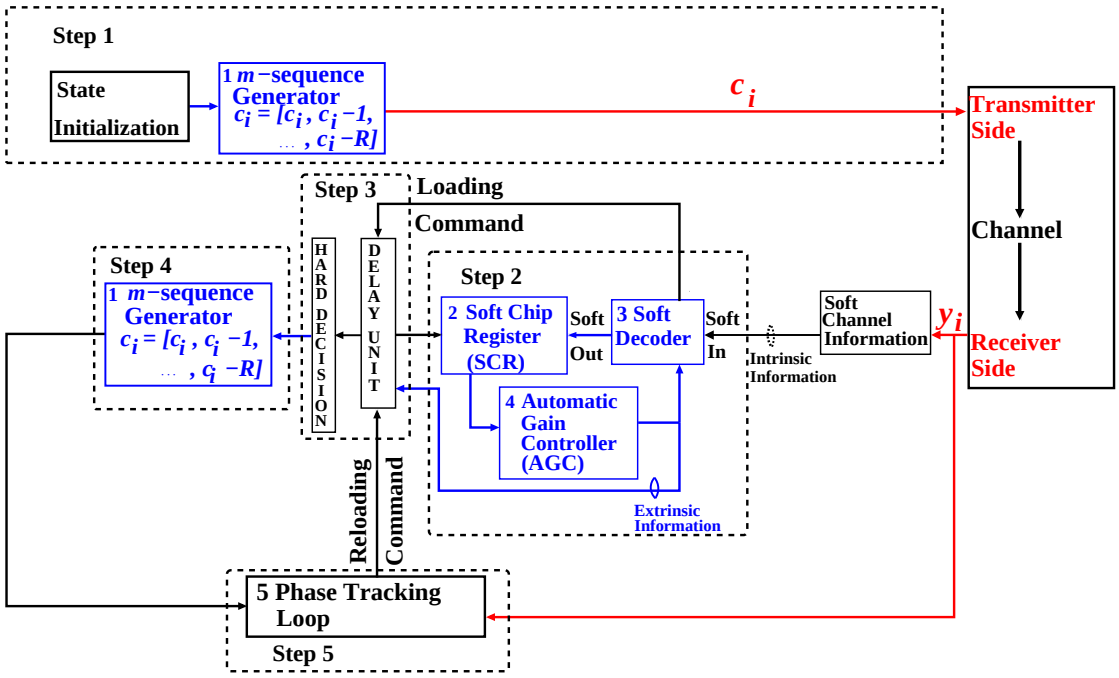


Figure 4.12: A schematic diagram of our proposed ISSE aided iterative acquisition scheme, where Step 1 to 5 shows the procedure involved in RSSE model.

4.5 Simulation Results For AGC

Fig. 4.12 depicts the proposed Automatic Gain Controller (AGC)-aided RSSE acquisition scheme, which is similar to our RSSE acquisition scheme shown in Fig. 3.3 except for the additional AGC block 4. The objective of the AGC is to amplify its input and feed its output back to the SISO decoder and then to store the value in the Delay unit, as portrayed in Fig. 4.12, where the values are linearly amplified, thus helping the SISO decoder to activate the loading command[1].The Delay unit of Fig. 4.12 stores the successive soft-chips values in form of the LLRs, which are computed by the AGC through the SCR of Fig. 4.12, where AGC is operating in its linear region throughout the process. The SISO decoder processes both the extrinsic information provided by the AGC and by the intrinsic information gathered from the channel. The Soft decoder's output is then transferred to the SCRs. Again the SCR forwards the current chip value to the AGC which amplifies the soft values by its gain. The basic steps involved in the RSSE model are explained as follows:

Step 1 The m-sequence generator is initialized and the chips generated are transmitted in the form of the phase-coded carrier signal without data modulation, as shown in Fig. 4.12. The GP and the chip values of the connecting taps of the LFSR are known both to the transmitter and receiver. At the receiver side, the receiver has the same number of identical taps, which were used while generating the GP at the transmitter side.

Step 2 The SISO detector/decoder collects a sample y_i from the channel which is associated with the transmitted chip c_i, and evaluates the LLR of the chips c_i based on y_i. The SCRs of Fig. 4.12, are set to zero prior to reception.The SCR has the same number of taps as that of the m-sequence generator. The soft output $L(c_i)$ of the SISO decoder then forward to the SCRs of Fig. 4.12. The R consecutive chips are now input to the AGC[2], where the values are linearly amplified thus helping the SISO decoder to activate[3] the "loading command" as illustrated in Fig. 4.12.

Step 3 Now R consecutive chips are estimated by applying hard decision to the most

[1]the loading command is activated when the output values of AGC become adequately high to ensure the low P_e.

[2]the purpose of AGC is to amplify the signal and transfer back to the SISO decoder and store the value in the Delay unit

[3]the Loading command is activated when the output values of AGC become adequately high to ensure the low P_e. From Eq.(3.4), the extrinsic information gleaned for improving the detection likelihood c_i maybe represent as $[1, 53, 92, 121]$

$$L_{apr}(c_i) = L_e(C_i) = L_{apr}c_i \approx \beta \prod_{n=1}^{N} \text{sign}(L_{ex}(c_{i\_R_n})) \times \big[\min\{|L(c_{i-R_1})|\}, \Big\{|L(c_{i_{-R_2}})|\Big\}, \ldots, \Big\{|L(c_{i_{-R_N}})|\Big\}\big] i \ = 0, 1, \ldots, \tag{4.8}$$

where we assume that $L_e(\beta c_{-\infty}) = \ldots = L_e(\beta c_{1-R}) = L_e(\beta c_{-2}) = L_e(\beta c_{-1}) = 0$ and the corresponding variables were defined in Chapter 3. Finally, the channel's output information $L(c_i|y_i)$ in Eq.(3.4) and the

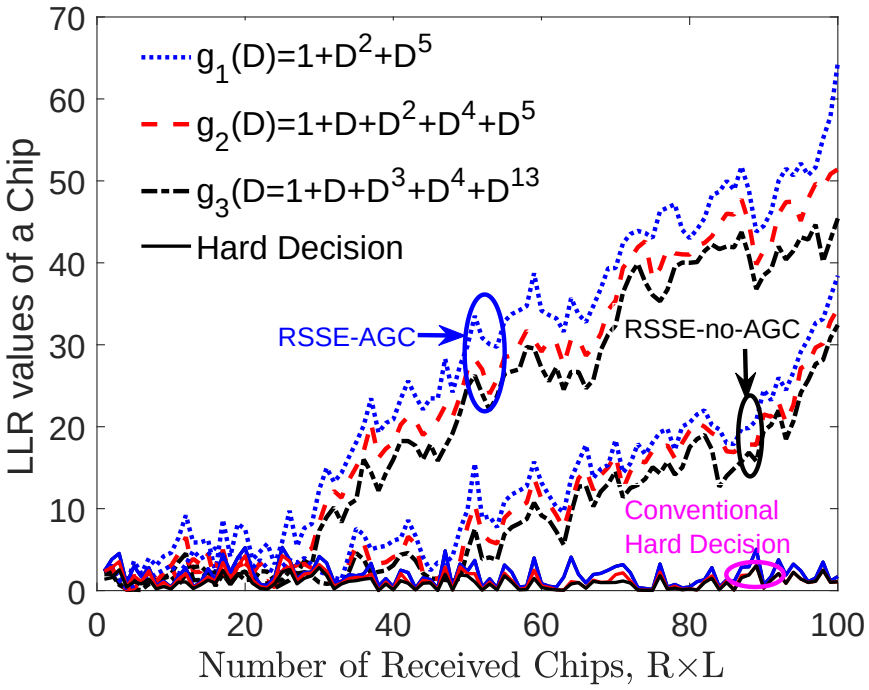


Figure 4.13: The number of received chips versus the decision reliability attained by ISSE SISO decoding, when communicating having a Nakagami Fading channel $m_l = 3.0$ and SNR= 0 dB

recent values stored in the Delay Unit.

Step 4 Then the resultant values obtained by the above-mentioned hard decision are loaded into the m-sequence generator of Fig. 4.12, but only if the generator received the correct chips.

Step 5 The despread signal is sent to the Phase Tracking Loop (PTL) of Fig. 4.12, where the phase is adjusted by the PTL. If phase has not been acquired correctly the PTL will trigger the "Reloading Command", because it is incapable of tracking the phase correctly [149, 150]. Thus, a new set of 'R' chips are loaded into the Delay units of the m-sequence generators of Fig. 4.12. This process will continue until the correct code phase is acquired by the PTL.

Fig. 4.13 demonstrates how the reliability of the chips of an m-sequence is improved upon processing more chips for transmission over over Nakagami fading channels. The decision reliability of SISO detection is computed from Eq.(4.9) which is derived from Eq(3.3), after each chip of a sequence has been received. The solid line

extrinsic information $L_e(c_i)$ in Eq.(3.5) yields the SISO decoder's expressed as:

$$L(z_i) = L(c_i|y_i) + L_e(c_i) = L_c y_i + L(c_i) + \beta \left[\prod_{n=1}^{N} \text{sign}(L(z_{i-r_n})) \right] \times \left[\min \{|L(z_{i-r_1})|\}, \{|L(z_{i-r_2})|\}, \ldots, \{|L(z_{i-r_N})|\} \right] \; i = 0, 1, \ldots. \tag{4.9}$$

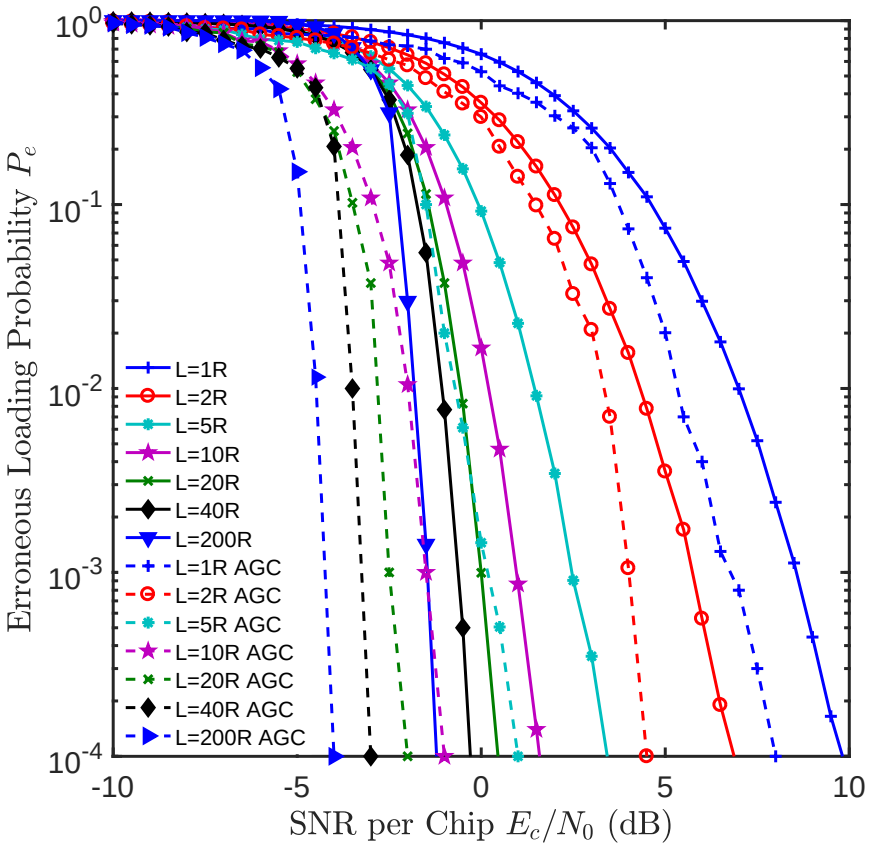


Figure 4.14: Erroneous loading probability P_e versus SNR parametrized by the number of chips entered into the recursive SISO decoder, when transmitting the m-sequence generated using the PP of $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ over an AWGN channel, where the dashed lines represent the AGC aided approach and solid lines represents the approach operating without an AGC in the RSSE model.

in Fig. 4.13 is related to the conventional hard decision based acquisition, which is defined as the absolute value of the channel output associated with the chips transmitted. Observe from Fig. 4.13 that the traditional hard decision based model has a decision reliability associated with the LLR values spanning from $0 - 10$, almost regardless of the number of chips processed, because the polarity of each chip is decided separately. By contrast, in the proposed RSSE acquisition model, the LLRs are increased as more chips are processed by the SISO detector. Hence the RSSE acquisition scheme outperforms the traditional hard decision sequential evaluation method of [102], since the latter operates without evaluating the *a priori* information given by the previously received chips. The acquisition schemes of [1, 92] are also outperformed by our AGC aided scheme. Our forthcoming simulation results will also supports this argument.

In Fig. 4.14 we evaluate the acquisition performance for a total sequence length of $N = 2^{13} - 1 = 8191$ chips,using the GP expressed as $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ having a total of five total taps out of which two are consecutive taps. Fig. 4.14 shows that $P_e = 10^{-5}$ is attained at an SNR value $= 1.7\ dB$ by processing $L \times R = 40 \times 13 = 520$ chips in the iterative SISO decoder without adopting the AGC approach, which

is represented by the solid lines. This PP is acquired at $P_e = 10^{-5}$ and an SNR value of about 1 dB by entering $L \times R = 200 \times 13 = 2600$ chips into the iterative SISO decoder, as visualized by the solid line seen in Fig. 4.14. By contrast the same GP is acquired by adopting the AGC approach and processing $40 \times 13 = 520$ chips in the iterative SISO decoder at -3 dB. This performance is further improved to -4 dB by processing 2600 chips.

The results portrayed in Fig. 4.15 were recorded for the transmission over Nakagami channel having a fading parameter of $m_l = 3.0$, where we examined the P_e versus SNR performance of an m-sequence using three different GPs. Note that when $L = 1$, we actually employ the hard decision approach using RSSE SISO decoding. Again, Fig. 4.15 demonstrates that the performance of all the polynomials tends to improve as the value of L increases at the cost of a higher computational complexity. We observe that $g_1(D)$ outperforms the other two GPs since it has three taps, which are non-consecutive, despite the fact that $g_2(D)$ and $g_3(D)$ have five taps instead of three, where two taps are consecutive. Furthermore $g_3(D)$ is inferior to $g_2(D)$, since a 13^{th} order polynomial is indeed expected to be outperformed by a 5^{th} order PP. Thus, similarly to the system using AGC, it can be inferred that the P_e performance depends both on the polynomial order as well as on the number of taps. From these results, we can deduce that by entering more chips into the iterative SISO sequence-detector, an improved correct detection probability is attained. Furthermore, upon employing an AGC we attain an improved SNR at a particular P_e. It is revealed that when an AGC is adopted, we achieved an increased gain by utilizing SISO detection, since in every iteration the gain of the amplifier multiplies the chips involved in generating the local m-sequence. For example, when performing $L = 100$ iterations instead of $L = 10$, the RSSE SISO decoder attains 3 dB SNR gain, upon processing a total of $100 \times 5 = 500$ chips of the PP $g_1(D)$. Similarly, for both $g_2(D)$ and $g_3(D)$ we attain almost 3 dB gain, which confirms again that utilizing the AGC technique substantially enhances the system performance. In line with Fig. 4.13, Fig. 4.15 shows that the GPs $g_1(D)$ and $g_2(D)$ outperform $g_3(D)$, since both of them are 5^{th} order polynomials. Furthermore, $g_1(D)$ outperforms the other two polynomials, because it relies on non-consecutive taps. Moreover, in line with our other scenarios, the GPs utilizing a low number of connections have a higher performance, than the GPs having more taps.

In Fig. 4.16 we compare our scheme operating with/without AGC, in terms of their P_e versus SNR performance recorded for three generator polynomials. Again, the Nakagami fading parameter was $m_l = 3.0$. Fig. 4.16 demonstrates that the AGC-aided concept attains a better gain in all respect. As expected, using $L = 1$ is inferior to $L = 100$, since by entering more chips when more decoding iterations are performed remarkably enhances the system performance. For example, when using the RSSE scheme without AGC, the GPs $g_1(D)$, $g_2(D)$ and $g_3(D)$ required unrealistic SNR values, which are as high as 32 dB, 33 dB and 35 dB at $P_e = 10^{-4}$

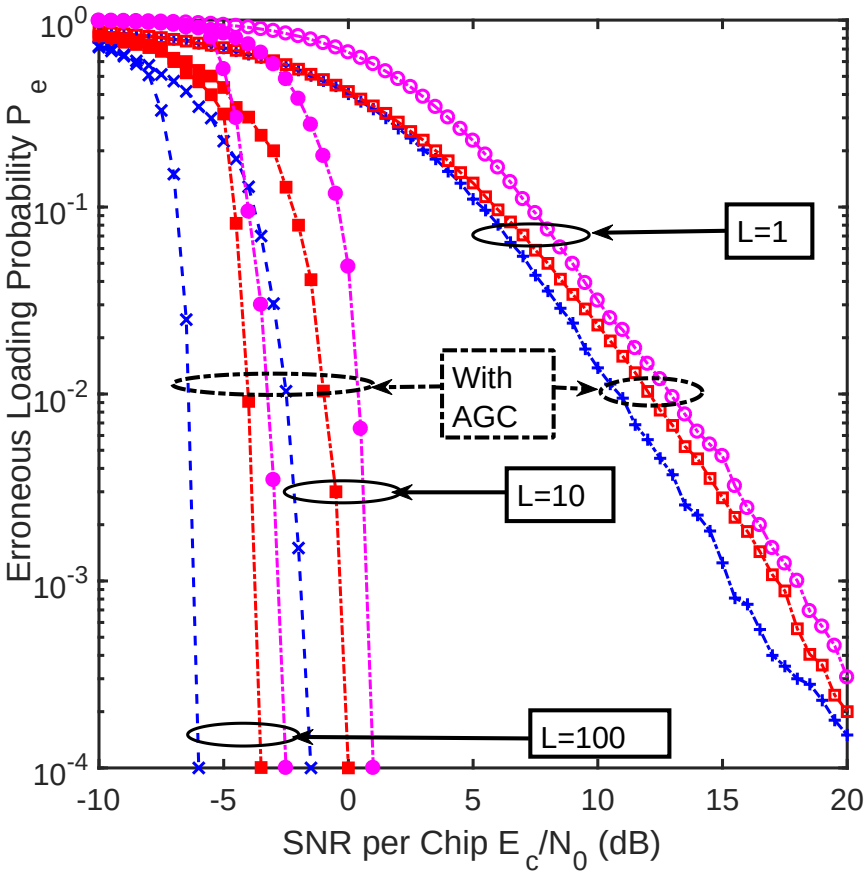


Figure 4.15: Erroneous loading probability P_e, versus the SNR for various numbers of iterations invoked by the proposed recursive SISO detector, when transmitting the m-sequence generated by the $g_1(D)$, $g_2(D)$ and $g_3(D)$ polynomials over Nakagami Fading channels when $m_l = 3.0$.

for $L = 1$. By contrast, upon using the AGC the same GPs $g_1(D)$, $g_2(D)$ and $g_3(D)$ required SNR values 21 dB, 22 dB and 24 dB at $P_e = 10^{-4}$ when $L = 1$, while for $L = 100$ we required SNRs of -6 dB for $g_1(D)$, -3.0 dB for $g_2(D)$ and -2.5 dB for $g_3(D)$, which illustrate that as expected that adopting an AGC improves the system performance.Furthermore, we observe in Fig. 4.16 that increasing L quite significantly, improves the performance of all GPs.

In Fig. 4.17 we compare the performance of the RSSE to that of the correlator-based acquisition of m-sequences having varying lengths, when communicating over AWGN channels both with and without AGC. Fig. 4.17 demonstrates that the resultant m-sequences can be acquired at P_e of 10^{-4} SNRs of -3, -2 and -0.5 dB by using $L = 40$ iterations without an AGC. By contrast, upon adopting the AGC the m-sequences are acquired at P_e of 10^{-4} at SNRs of -5, -4 and -2.5 dB by using $L = 40$ iterations. When using a correlator, the m-sequence acquisition scheme requires SNRs of 5, 6 and 7 dB in order to achieve a P_e of 10^{-4}, whereas without using an AGC the m-sequences acquisition scheme requires an SNR of about 10 dB in order to achieve a P_e of 10^{-4} for all three GPs. Therefore, the achievable SNR gain of the RSSE acquisition model at P_e of 10^{-4} is about 5, 6 and 7 dB, when exploiting

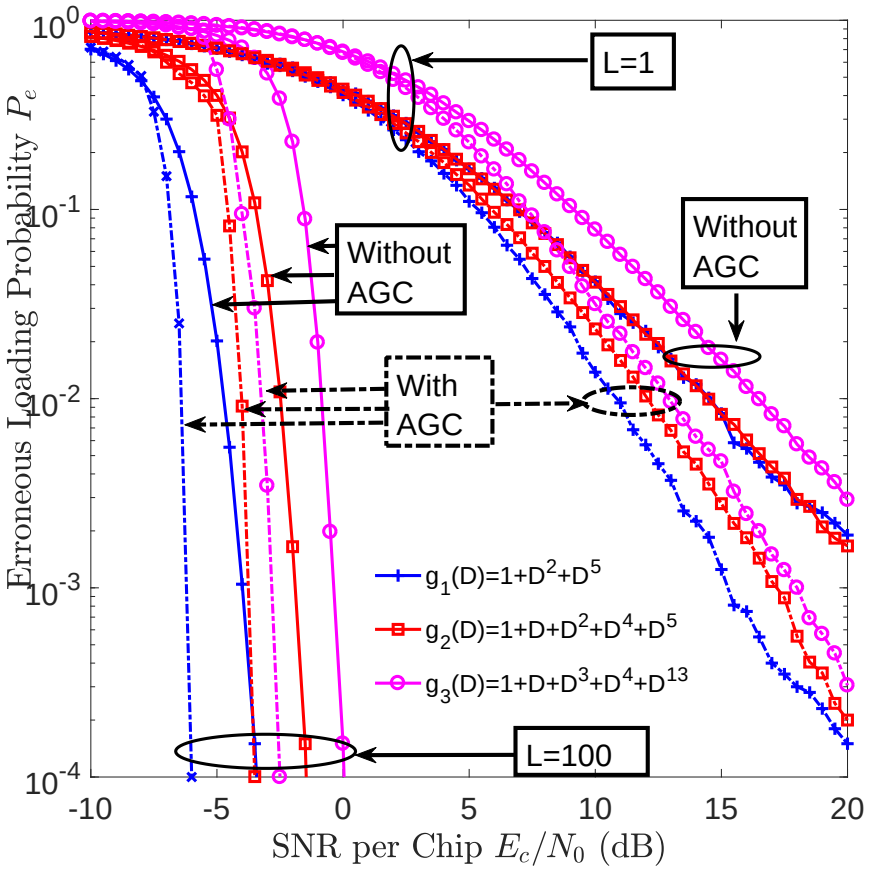


Figure 4.16: Erroneous loading probability P_e, versus the SNR, performance for various numbers of chips invoked into the proposed recursive SISO detector, when transmitting the m-sequence generated by the $g_1(D)$, $g_2(D)$ and $g_3(D)$ polynomials over Nakagami Fading channels when $m_l = 3.0$.

the AGC for $g_1(D)$, $g_2(D)$ and $g_3(D)$, respectively.

Fig. 4.18 illustrates the Average Mutual Information (AMI) versus the number of iterations at the same SNR value of 0 dB upon utilizing an AGC, when different GPs are employed. It is observed that $g_1(D)$ requires a maximum of $L = 10$ iterations to approach unity, whereas $g_2(D)$ requires $L = 12$ iterations and $g_3(D)$ necessitates $L = 15$ iterations to achieve the same goal. Hence our previous conclusions are confirmed again.

In Fig. 4.19 our EXIT chart analysis is carried out both with and without AGC, at an SNR value of 0 dB, where the Nakagami fading parameter was $m_l = 3.0$. All the inner and outer component EXIT curves match their Monte-Carlo simulation based decoding trajectories. Furthermore, there is an open tunnel between the inner and outer component curves, all the way to the [1,1] point. Hence an infinitesimally low P_e is attained by our iterative receiver. Furthermore, it can be observed that using a higher SNR value, the trajectories requires less iterations to reach the point [1, 1] of perfect convergence at the top right corner of Fig. 4.19. Moreover, it can be seen that by adopting the AGC-based approach we can obtain a wider tunnel between

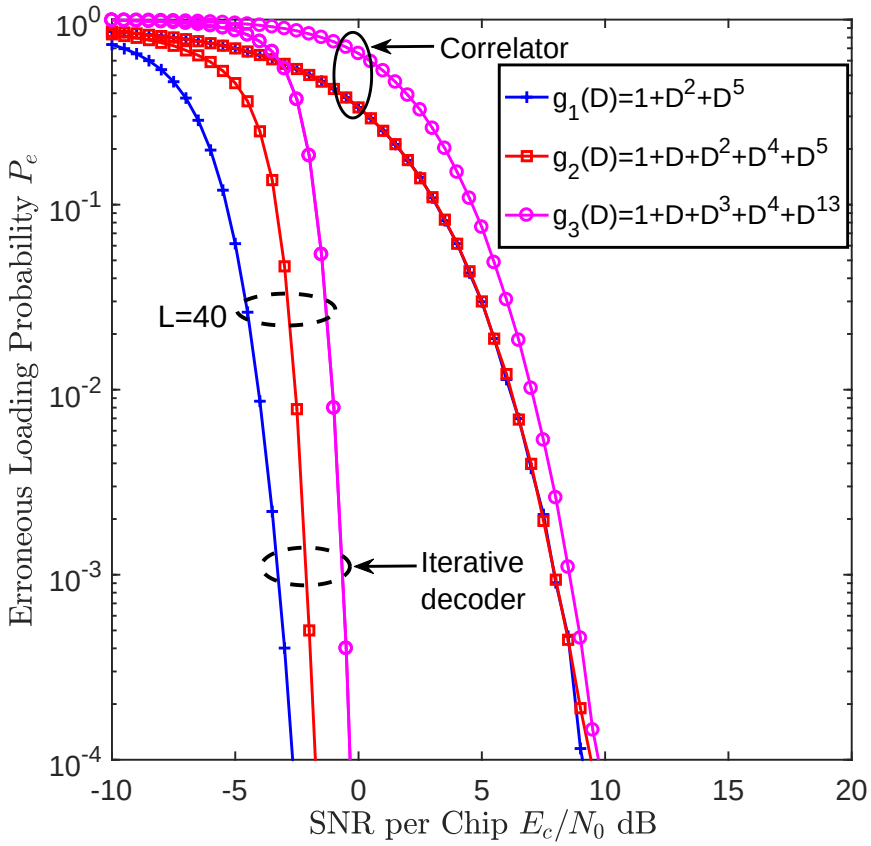


Figure 4.17: Erroneous loading probability P_e, versus the SNR, performance for various numbers of chips invoked into the proposed recursive SISO detector, when transmitting the said polynomials over Nakagami Fading channels when $m_l = 3.0$.

our inner and outer component curves of the EXIT chart and that our decoding trajectory matches to these curves. It is observed in Fig. 4.19 that the GP $g_1(D)$ needs less decoding iterations to reach the [1, 1] point for a given SNR value. On the other hand $g_2(D)$ needs more decoding iterations to reach the [1, 1] point but the performance of both $g_1(D)$ and $g_2(D)$ is better than that of $g_3(D)$, because both of them belongs are 5^{th} order GPs whereas $g_3(D)$ is a 13^{th} orde GP. This indicates that the higher-order polynomials have slower convergence than lower order polynomials. Thus, lower-order polynomials have lower number of connecting taps therefore they are preferred over higher order polynomials because of having lower complexity and require less computation to achieve better results.

In Table 4.1, it can be observed by our simulation results that AGC scheme outperform our previous purposed scheme because of its linear gain. The system achieve better performance in less time. Moreover it is observed that when AGC is employed the GPs performances better in RSSE scheme, $g_1(D)$ requires a maximum of 10 iterations to achieve unity, where as $g_2(D)$ requires 12 iterations and $g_3(D)$ necessitates 15 iterations. By contrast, when AGC was not employed in RSSE the $g_1(D)$ requires a maximum of 21 iterations to approach unity, where as $g_2(D)$ requires 22 iterations and $g_3(D)$ requires 26 iterations as listed in Table. 4.1.

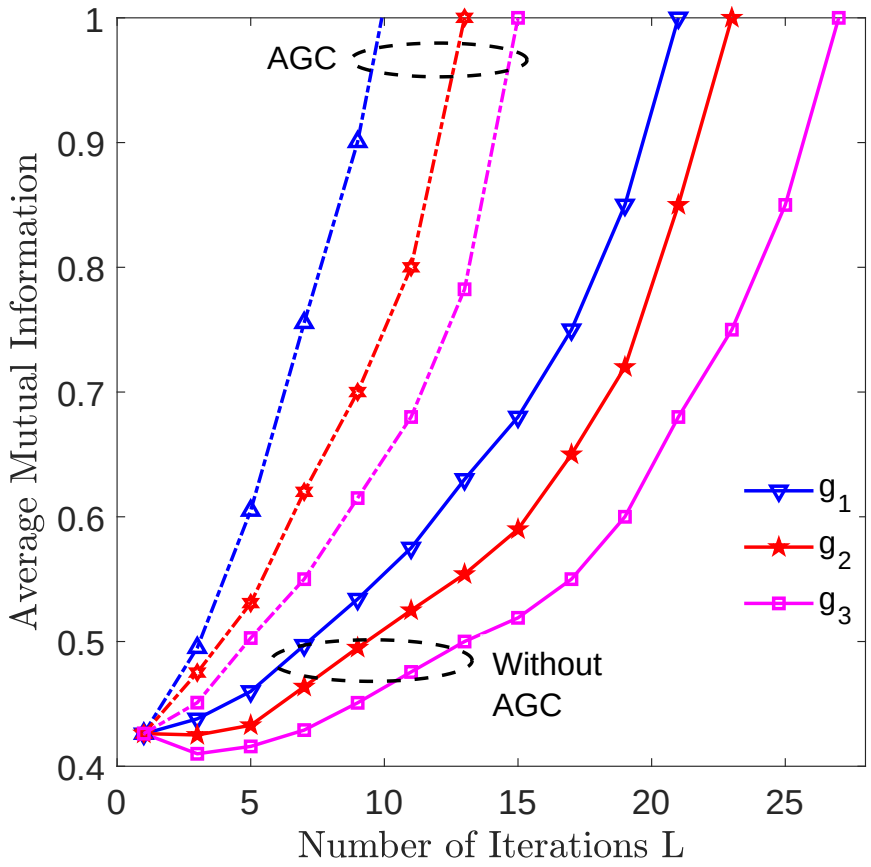


Figure 4.18: Average Mutual information (AMI) versus the number of decoding iterations where $g_1(D) = 1 + D^2 + D^5$ (blue), $g_2(D) = 1 + D + D^2 + D^4 + D^5$ (red) and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ (magenta) over Nakagami channels when $m_l = 3.0$.

Poly−−nomial Order	***Generated Polynomial***	***Total Number of Taps***	***Erroneous Loading Probability*** (P_e)	***SNR per Chip*** E_c/N_0 ***dB***		***Number of Iterations***	
				without AGC	***with AGC***	***without AGC***	***with AGC***
5^{th}	$g_1(D) = 1 + D^2 + D^5$	**3**	10^{-4}	**-3.5**	**-5.5**	**21**	**10**
5^{th}	$g_2(D) = 1 + D + D^2 + D^4 + D^5$	**5**		**0.0**	**-4.0**	**22**	**12**
13^{th}	$g_3(D) = 1 + D + D^3 + D^4 + D^{13}$	**5**		**0.5**	**-3.8**	**26**	**15**

Table 4.1: Comparisons of P_e versus SNR values in dB as well as the number of iteration involved to achieve desire goals.

4.6 Conclusions

It has been observed that for GPs of similar order, those having fewer taps outperform GPs with higher number of connected taps both with and without an AGC.

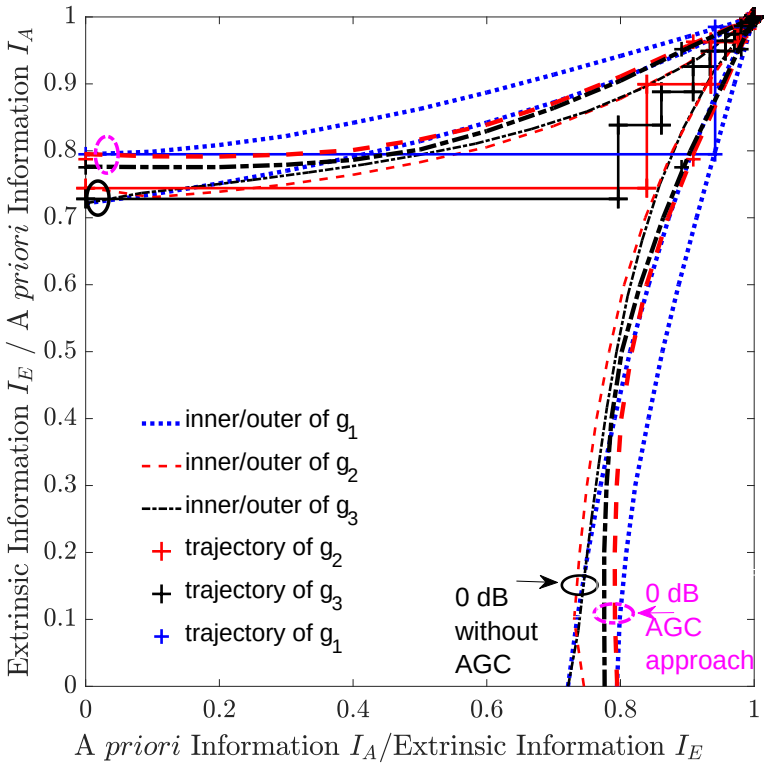


Figure 4.19: EXIT chart for the GPs of $g_1(D) = 1+D^2+D^5$ (blue), $g_2(D) = 1+D+D^2+D^4+D^5$ (red) and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ (black) over Nakagami channels, when $m_l = 3.0$ at SNR= 0 dB with/without AGC approach.

Explicitly, the attainable performance depends both on the number of taps and on the polynomial order. The low-order GPs having less taps are superior to those having more taps, because GPs having less connecting taps result in less grave error propagation than their counterparts having more taps. Accordingly, the GPs having less taps yield a wider EXIT chart opening, which in turn results into more prompt sequence acquisition at lower SNR values. The P_e versus SNR simulations and the EXIT chart results confirm each other. It is revealed that RSSE acquisition technique relying on an AGC scheme consistently outperforms its counterpart operating without an AGC arrangement.

Chapter 5

Primitive Polynomials for Iterative Recursive Soft Sequential Acquisition of Concatenated Sequences

5.1 Introduction

In this chapter we conduct an iterative initial sequence acquisition technique, which is proposed for the Pseudo-Noise (PN) signal derived from a pair of m-sequences used for generating the concatenated sequence, which relies on Soft-In-Soft-Out (SISO) detection to improve the acquisition performance. This Recursive Soft Sequential Estimation (RSSE) technique has a linearly *increasing complexity* with the number of chips in the concatenated sequence. Receiving as few as R consecutive chips of a $(2^R - 1)$-chip sequence is sufficient for the local concatenated-sequence generator of the receiver to synchronize. Hence, this initial synchronization technique is eminently suitable for long m- and concatenated sequences. Another key result is the comparison of m- and concatenated sequences regarding the Acquisition Time (AT). It is also observed that low-order Primitive Polynomials (PPs) achieve better performances than higher-order polynomials for both the m- and concatenated sequences. When considering PPs having higher number of taps, the exploitation of concatenated sequences is capable of achieving in excess of 3 dB Signal to Noise Ratio (SNR) gains over m-sequences. The popularity of notepads, laptops, smart phones, gaming consoles, smart televisions and Personal Digital Assistants (PDAs) has dramatically increased the tele-traffic [8, 9]. Efficient use of the transmit bandwidth plays a pivotal role in multi-media-centric environments [9, 6, 151]. PN sequence acquisition is the initial synchronization procedure of Spread-Spectrum (SS) commu-

nication systems [16, 53, 143, 152]. Once initial synchronization has been established, symbol- synchronization may take place and the data can be demodulated [53, 59] either using coherent or non-coherent detection. Numerous different m-sequences have been used in both the Interim Standard (IS)-95 [14, 53] and in the Code Division Multiple Access-2000 (CDMA-2000) standards [14, 65]. The 3^{rd} Generation Partnership Project (3GPP) also opted for using m-sequences for initial acquisition in the 5^{th} Generation (5G) standards [97, 98, 99, 100, 101].

In the context of m-sequence acquisition, Ward [102] proposed a sequential estimation acquisition arrangement, where the correctly received m-sequence output by the acquisition mechanism was then loaded into the receiver's m-sequence generator [92, 121]. Explicitly, provided that the received SNR is sufficiently high, the acquisition of an m-sequence having a period of $(2^S - 1)$ may be *successfully* concluded, once as few as S successive chips are perfectly recovered by the sequence acquisition device. These are then loaded into the m-sequence generator of the receiver. The sequence generator will produce chips that are identical to those generated by the transmitter [1, 92]. Naturally, some of the received chips might be corrupted by noise and interference, hence resulting in faulty loading of the m-sequence generator of the receiver with an Erroneous Loading Probability (P_e) [1, 92]. Ward [102] has demonstrated that for reasonable SNR values this technique leads to a shorter average initial Acquisition Time (AT) than the conventional sliding correlator-based initial acquisition technique [119]. However the received signal energy is typically distributed across hundreds or thousands of chips, hence the SNR per chip is extremely low. Moreover, hard decisions are typically unreliable for the estimation of R consecutive chips using a chip-by-chip-based approach [1, 53, 92, 152]. Hence, Kilgus devised a majority logic aided decoder for m-sequence acquisition [93]. As a further evolution of this kind of technique, Ward and Yiu [123] proposed the concept of recursive sequential estimation assisted acquisition. The basic principle of these two schemes was to adopt the hard decision approach relying on coherent detection. However, adopting any hard decision based coherent approach becomes unrealistic, since the SNR is usually very low prior to despreading [16, 59]. For this reason, we advocate the recursive Soft Input Soft Output (SISO) detection principle, which has its roots in the classic turbo channel decoding philosophy [1, 92, 141, 54]. Before delving into the new contributions of this chapter we have summarized the evolution of the field in Fig. 5.1.

Against this background, our novel contributions are as follows:

- We introduce a new concatenated sequence acquisition concept.
- We propose the application of EXIT charts for visualizing the convergence behaviour of the concatenated sequence aided synchronization. We demonstrate that the concatenated sequences produced by the low-order Primitive Polynomial (PP) relying on a low number of taps achieve higher MI than other PPs

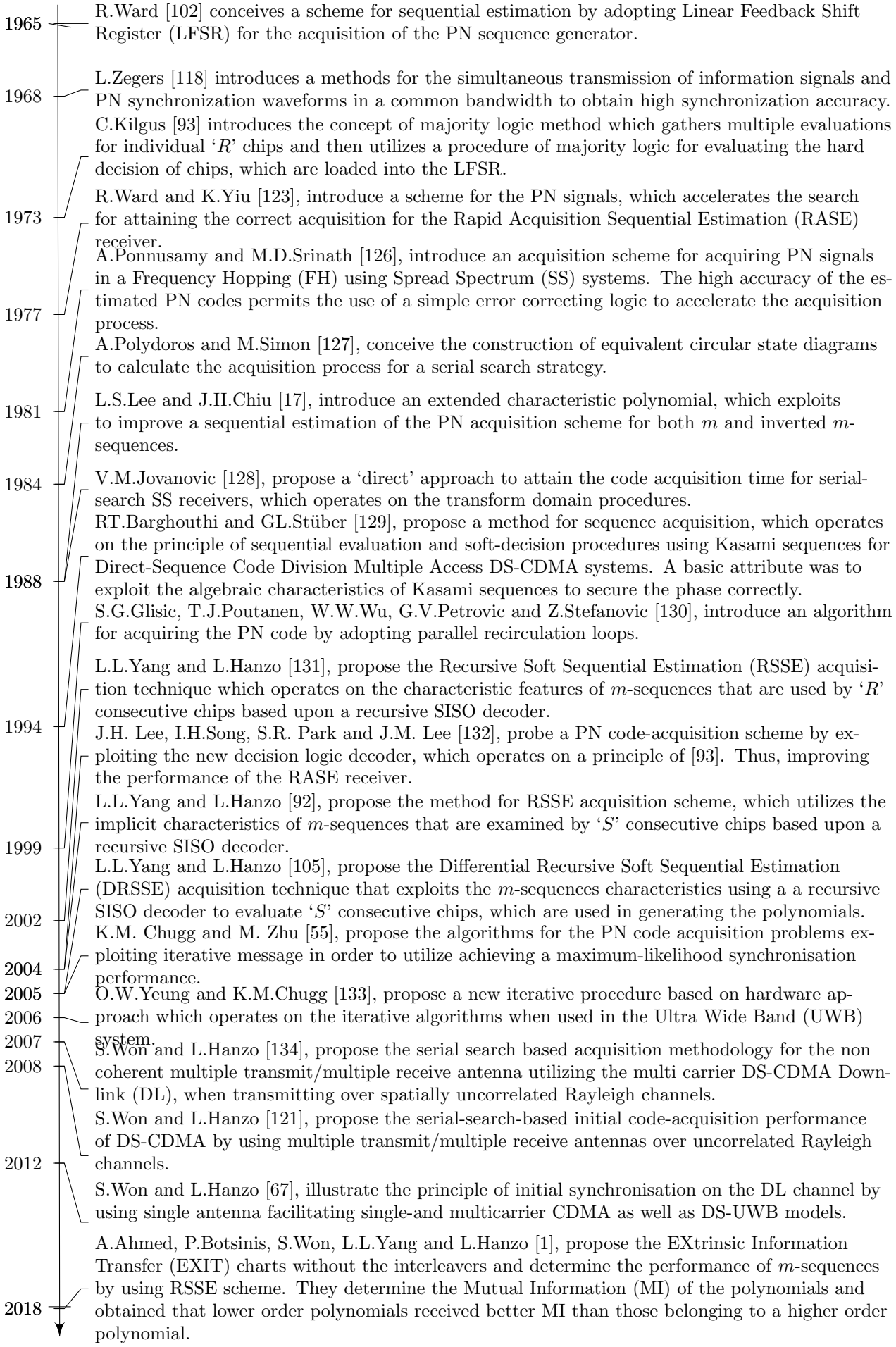


Figure 5.1: Timeline of initial acquisition for PN code sequence generator.

having more taps at a similar number of iterations. Our investigations verify that the convergence of our iterative acquisition scheme using high-order PPs is worse than that of low-order PPs.

- We demonstrate that low-order PPs have a lower P_e than their high-order counterparts. Among PPs of the same order having same number of feedback taps, PPs with higher-index taps perform best. Furthermore, PPs of the same order having non-consecutive feedback taps outperform those having consecutive feedback taps.
- We show that concatenated sequences attain a beneficial gain over m-sequences.
- We also demonstrate that concatenated sequences achieve a lower AT than m-sequences.

The outline of this chapter is as follows: Section 5.2 illustrates the RSSE acquisition design. Section 5.3 illustrates the employment of EXIT charts. We provide our simulation results in Section 5.4, prior to our conclusions in Section 5.5.

5.2 Proposed System Model

Fig. 5.2 portrays our acquisition scheme, constituted by five major components namely: a) m-sequence generators, b) Concatenated sequence generator, c) SISO detector/decoder, d) Soft-Chip Register (SCR) and e) Phase-Tracking Loop (PTL). Prior to our discussion of these components, we investigate the RSSE acquisition technique. The two SCRs have the same structured *delay units* as those of the m-sequence generators of the transmitter. Their task is to store the instantaneous values of the consecutive chips in the form of their LLRs. The SISO detector/decoder calculates the related values of the soft LLRs after receiving each soft channel output. The SISO detector/decoder processes both the *intrinsic information* received from the channel plus the *extrinsic information* related to the same chip, depending mainly upon the previously processed LLR values gathered in the SCRs. An appealing feature of the RSSE is that it takes into account the reliabilities of all the successive chips by monitoring their LLRs. The basic steps of the RSSE are illustrated as follows:

1 At the transmitter side of Fig. 5.2, the pair of m-sequence generators are initialized and the transmitter sends the phase-coded carrier signal without any data modulation[1]. Both the transmitter and the receiver know the PPs and the chip

[1]In the context of initial synchronization, the m-sequences are utilized for aiding synchronization between the Mobile Station (MS) and the Base Station (BS). They have been specifically selected as a benefit of their cyclic nature. Explicitly, during code acquisition, the receiver becomes capable of locking on to the correct stage of each shift register after as few as R or S chip transmissions, despite transmitting m-sequences of length $(2^R - 1)$ or $(2^S - 1)$. Our DownLink (DL) transmission is initiated by transmitting an unmodulated pilot signal over the pilot channel. The pilot channel provides a reference signal for all the MSs within a cell, which is always transmitted by the BS [16, 65, 66]. Typically it is about 4-6 dB

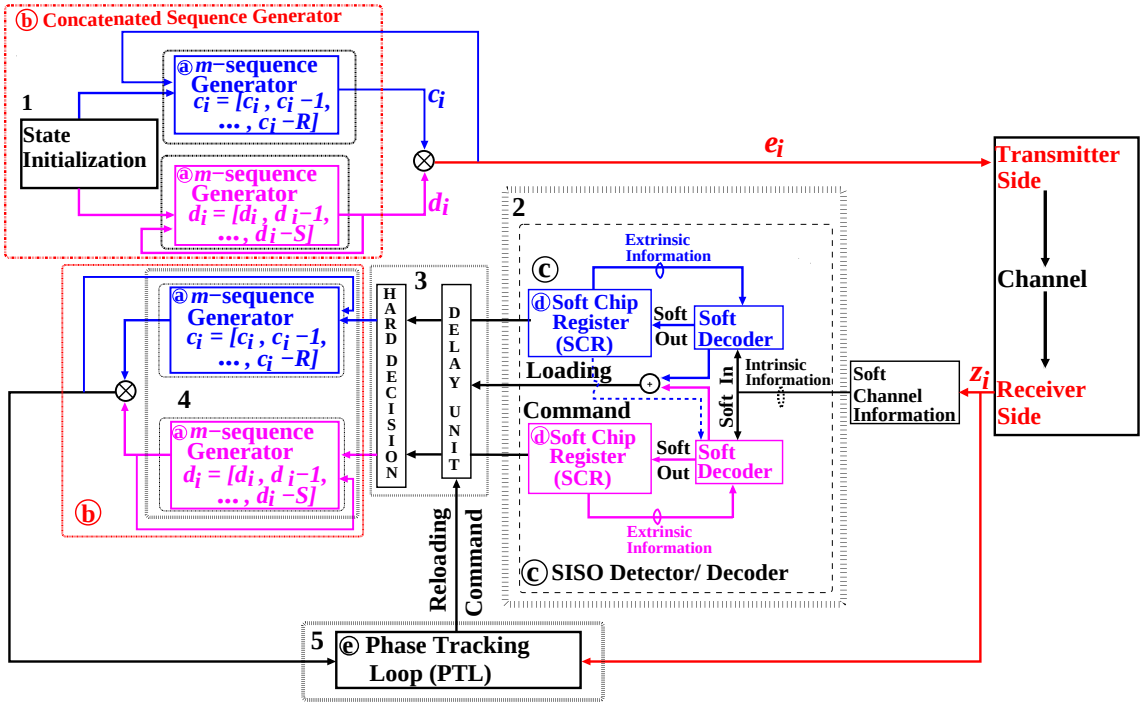


Figure 5.2: A schematic diagram of our proposed RSSE aided iterative acquisition scheme, where blue dotted line shows the information gathered from first SISO decoder to obtain the information for the second decoder, where the blue line represents the information about the SCR of c_i, which is used for calculating the soft information conveying d_i and in other words the values of one SCR at the receiver are utilized to calculate the *a priori* of the other shift register which is shown by blue dotted line.

values. If the receiver has exactly the same feedback for the two m-sequence generators as those of the transmitter side, then the corresponding chip values will be loaded into the appropriate registers of the two m-sequence generators.

2 The SISO detector/decoder receives a channel output sample z_i associated with the chip e_i, and then it evaluates the LLR of e_i based on z_i as well as it determines the extrinsic information. The data are then fed to the SCRs of Fig. 5.2, where the SCRs have the same number of taps as well as the connections as those of the two m-sequence generators at the transmitter. The most recent S and R chip values are stored in the SCRs of the SISO decoder, which are associated with S and R successive chips of the transmitted m-sequences, respectively. When the magnitudes of the most recent S and R soft outputs of the SISO detector become sufficiently high for ensuring a low P_e, a "Loading Command" is issued by the scheme of Fig. 5.2.

3 After that, S and R successive chips are calculated by using hard decisions, which is based on comparing the most recent S and R chips stored in the SCR at that instant of time to a threshold resulting in the binary value of either +1

stronger than the power of all other channels. The pilot channel uses the all-zero Walsh code and contains no information except for the RF carrier in the IS-95. Therefore, the pilot signal is an unmodulated SS signal because it is multiplied by an all-zero Walsh code, which is then spread according to the chip rate of the sequence [66, 51]. No data modulation is performed during this part of the transmission, as mentioned in [1, 92, 121].

or -1. After obtaining the hard decision result, the values are loaded into the corresponding delay units of the two m-sequence generators of Fig. 5.2.

4 As soon as the initial binary values are determined by a pair of m-sequence generators, the received signal is despread, provided that the initial chip values of the two m-sequence generators are correctly loaded.

5 The despread signal is transferred to the Phase Tracking Loop (PTL) of Fig. 5.2 to acquire the phase. When the phase is acquired correctly, the updated chips of S and R will be loaded into the delay units of Fig. 5.2. By contrast, if the phase is not acquired correctly, then the PTL will be triggered to activate the "Reloading Command". This procedure will be repeated until the correct code is found by the PTL. In other words, the task of PTL is to retrieve a signal received over the noisy channel and to produce a secure output so that the received and transmitted signals are perfectly aligned.

Let us now discuss all the blocks of the proposed RSSE technique in detail by relying on Fig. 5.3.

5.2.1 m-sequence Generator

Let us commence by discussing this processing block marked as ⓐ in Figs. 5.2 and 5.3. These m-sequences belong to the family of maximum length sequences [16, 143, 52], produced by LFSR. The LFSR connection polynomial uniquely describes the sequence generator [16, 120]. In Fig. 5.3, the unit time delay is represented by 'D' and g_1, g_2, ..., g_R denotes the absence or presence of the connections. Explicitly, a connection being present is represented by 1, while the connection being absent is represented by 0. The generator polynomial is expressed as:

$$g(D) = 1 + D^{r_1} + D^{r_2} + \ldots + D^{r_M=R}, \tag{5.1}$$

where $g(D)$ is a PP, therefore it cannot be factorized [16, 92, 104] and the r_1, r_2 ... are the index set corresponding to the feedback tap connections of the concerned PP used in generating the concerned m-sequences. According to Fig. 5.3, the m-sequence can be generated by the following recursion

$$c_i = c_{i-r_1} c_{i-r_2} \ldots \; c_{i-(r_M=R)} = \prod_{m=1}^{M} c_{i-r_m}, \quad \text{for } i = 0, 1, \ldots, I. \tag{5.2}$$

where c_i denotes the chip-values of the m-sequence having output values of $\{+1, -1\}$ respectively, since SS communication systems usually employ binary spreading sequences having chip values of $\{+1, -1\}$. In this contribution we assume that the

m-sequence generator outputs duo-binary $\{+1, -1\}$ symbols [2], representing a logical zero by $+1$, while the product operation is denoted by $\prod(\cdot)$. In the scenario of our iterative calculation-based acquisition method of Fig. 5.3 utilized for m-sequences, the generator's state can be calculated by iterative detection schemes, where each m-sequence generated by an 'R'-stage shift register having a length of $(2^R - 1)$ chips is represented by a cyclic Bose Chaudhuri Hocquengem (BCH) code of length $(2^R - 1)$, having a displacement of $(2^R - 1)$ [93]. Consequently, after the receiver has obtained $[2\times(2^R-1)]$ successive patterns of the m-sequence generated, the first stage of R chips is calculated for the m-sequence generator by iteratively detecting the m-sequence obtained with the help of its tap connections. Note that a pair of m-sequence generators and the SCRs of Fig. 5.3 have the same feedback elements. Moreover, the feedback branches are duo-binary in the m-sequence generator and the results obtained from these branches are utilized for producing a binary feedback flag.

5.2.2 Concatenated Sequences

Let us now turn our attention to processing the block marked as ⓑ in Figs. 5.2 and 5.3. Concatenated sequences are widely used in wireless communication as these sequences are derived from two PPs, having similar cross correlation and auto-correlations properties of the Gold codes and long PN-sequences [112, 113, 114, 153, 154]. A pair of m-sequence generators are used for generating the concatenated sequence by XOR-ing or performing modulo-2 addition of the appropriately shifted versions of the two m-sequences created by two different PPs having the length of $2^R - 1$ and $2^S - 1$ respectively, as shown in Fig. 5.3. In this paper we assume R=S, so that the generated concatenated sequences has the properties as the Gold sequence. These PPs cannot be factorized and they obey:

$$\begin{aligned} c_i &= c_{i-r_1} c_{i-r_2} \ldots c_{i-(r_M=R)} \\ &= \prod_{m=1}^{M} c_{i-r_m} \quad \text{for } m = 0, 1, \ldots, M, \\ &\qquad\qquad i = 0, 1, \ldots, I, \end{aligned} \tag{5.3}$$

$$\begin{aligned} d_i &= d_{i-s_1} d_{i-s_2} \ldots d_{i-(s_N=S)} \\ &= \prod_{n=1}^{N} d_{i-s_n} \text{ for } n = 0, 1, \ldots, N, \\ &\qquad\qquad i = 0, 1, \ldots, I, \end{aligned} \tag{5.4}$$

[2] Please note that c_i over here will be feed to the channel when exploit the RSSE scheme of [1, 92] to obtain synchronization for m-sequence.

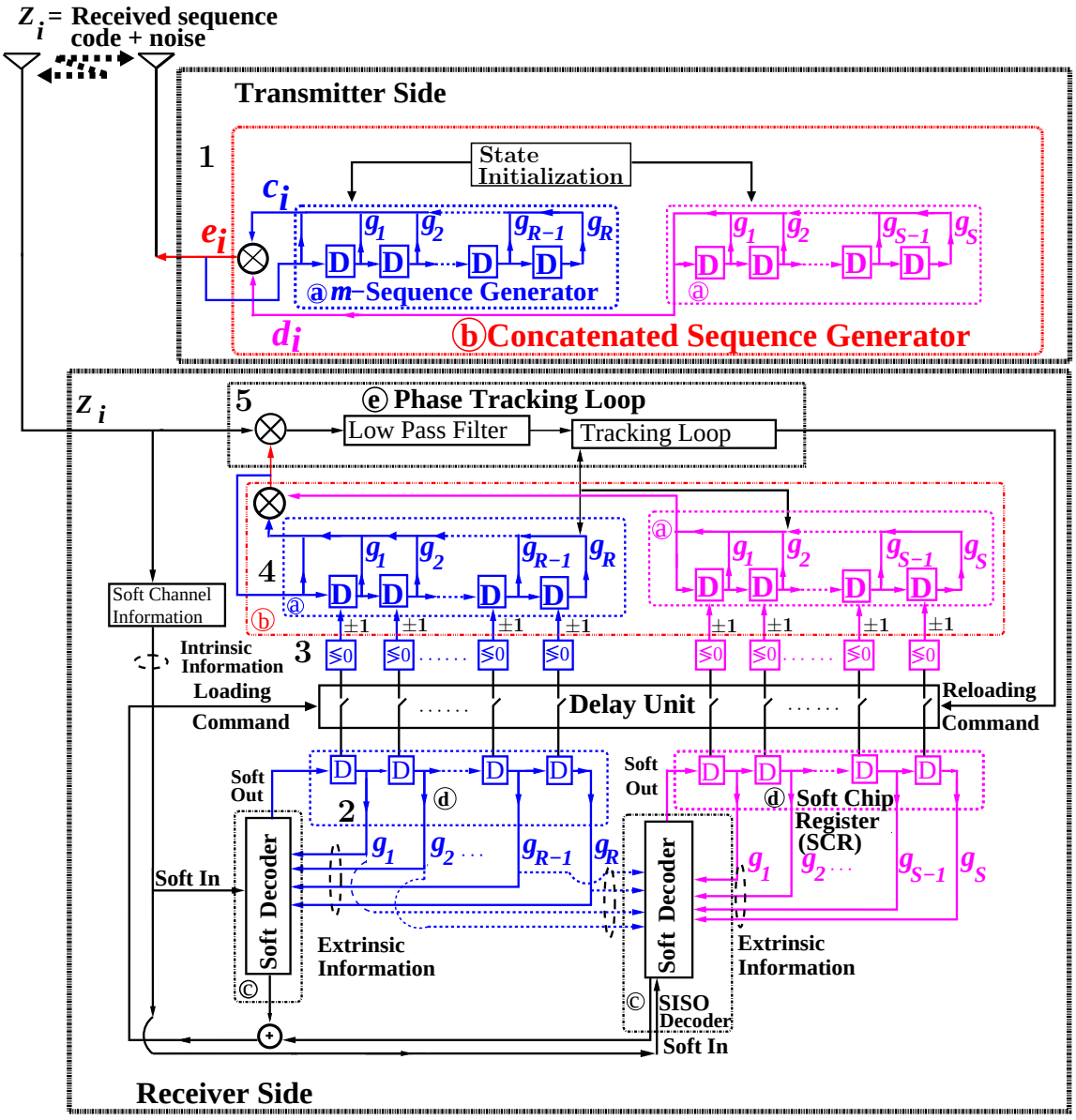


Figure 5.3: RSSE aided iterative acquisition model, where R and S have the same polynomial order, whilst c_i and d_i are the chips concerned, where the blue dotted line represents the information about the SCR of c_i, which is used for calculating the soft information conveying d_i.

where c_i and d_i of Fig. 5.3 represent the chip values of the two m-sequences used for generating the concatenated sequence, respectively[3]. Eqs. (5.3) and (5.4) can be combined as follows:

$$\begin{aligned} e_i &= c_i \cdot d_i \\ &= \prod_{m=1}^{M} c_{i-r_m} \cdot \prod_{n=1}^{N} d_{i-s_n} \text{ for } i = 0, 1, \ldots, I, \end{aligned} \tag{5.5}$$

where e_i is the resultant output of two m-sequence generators, i.e, the chip values of the concatenated sequence.

5.2.3 Soft Chip Register and SISO Decoder

We now continue our discourse by discussing the processing block marked as © in Figs. 5.2 and 5.3. In Fig. 5.3 the SCRs have R and S number of delay-units. The number of SCRs is identical to that of the delay units in a pair of m-sequence generators. Furthermore, the two SCRs rely on the same feedback connections as those of the transmitter side, because the PPs are known to both the receiver and to the transmitter. The chip-LLR values of the R and S successive chips are stored and shifted by the SCR. Again, at the first iteration the likelihood of having a '1' or '0' chip is identical, hence the LLRs are set to zero [1, 92]. As portrayed in Fig. 5.3, the LLRs of these R and S chips will be used to obtain the hard decisions of the successive chips that are then loaded into the pair of m-sequence generators. The SISO decoder utilizes the previous LLRs computed by the SCR as the *a priori* information [1, 92]. The information gleaned at the output of the channel for a specific chip is referred to as intrinsic information, which is calculated by the SISO decoder. The soft output of the SISO decoder of Fig. 5.3 is then entered at the left-most location of the SCR, while the right-most SCR's value is removed [1, 92]. At the last iteration we observe the maximum values of our two SISO decoders as seen in Fig. 5.3, and then a "loading command" is triggered[4], provided that the soft outputs of the SISO decoders become sufficiently high for ensuring a low P_e. The corresponding chips are evaluated by

[3]The chip-values of the two m-sequence have output values of $\{-1, +1\}$ respectively. The information about the chip d_i can be obtained by taking the information about e_i plus the information obtained by the corresponding chip c_i of the first SISO decoder because both sequences are used for producing the concatenated sequence. Therefore by performing the modulo-2 addition or XORing we generate a concatenated sequence, as shown in Figs. 5.2 and 5.3. Hence for calculating the soft information d_i we have to obtain the information from the e_i and also from the chips of the other m-sequence's decoder. This is because the values of the one of the m-sequences SCR at the receiver are utilized to calculate the *a priori* of the other shift register.

[4]When the magnitudes of the LLR values in the SCR become sufficiently high after a set of iterations, then the SISO detector carries out hard decisions to generate the binary values -1 or $+1$ of the chip, which are loaded into the two m-sequence generators at the receiver. Let us assume that we carry out the i^{th} iteration, with $i = 1, \ldots, I$ and the number of extrinsic LLRs to be evaluated is S and R, thus the values calculated in the LFSR are updated at the receiver. During each iteration S and R chips have to be transmitted. Thus after I iterations the total number of received chips will be $I \cdot R$ or $I \cdot S$, where R and S have the same polynomial order.

applying hard decisions to the most recent values of the LLR, which are stored in the SCR. Finally, after the hard-decisions the resultant binary chips are entered into the related shift registers of the two m-sequence generators of the receiver of Fig. 5.3.

5.2.4 Soft Channel Outputs

Focusing our attention on the block marked as ⓓ in Figs. 5.2 and 5.3, the chip e_i is related to the received signal as

$$z_i = \alpha_i e_i + n_i, \qquad i = 0, 1, \ldots, \tag{5.6}$$

where n_i is the Additive White Gaussian Noise (AWGN) having a zero mean, N_0 is the noise power spectral density and α_i is the channel state. Given z_i, the LLR of e_i is expressed as

$$\begin{aligned} L_{ex}(e_i) = L(e_i|z_i) &= \log\left[\frac{P(e_i = +1|z_i)}{P(e_i = -1|z_i)}\right] \\ &= L_e z_i + L(e_i),\ i = 0, 1, \ldots, \end{aligned} \tag{5.7}$$

where $L_e = 4\alpha_i \frac{E_c}{N_0}$, the energy per chip is E_c and $L_e(e_i) = 0$, since we assume that the chip's value e_i is binary and equiprobable. Observe from Eq.(5.6) and Fig. 5.3 that the soft outputs of the SISO decoder are calculated at the time instants of $(i-r_1), (i-r_2), (i-r_3), \cdots, (i-r_M)$, as well as $(i-s_1), (i-s_2), (i-s_3), \cdots, (i-s_N)$ and then fed into the SISO decoder. These outputs constitute the *a priori* inputs of $(c_{i-r_1}), (c_{i-r_2}), (c_{i-r_3}), \cdots, (c_{i-r_M})$, and $(d_{i-s_1}), (d_{i-s_2}), (d_{i-s_3}), \cdots, (d_{i-s_N})$. Then, the extrinsic information calculated at its output is used for correctly detecting the chip e_i with a high probability. Assuming that the previous R and S number of soft outputs of the SISO decoder are denoted by $L_{ex}(e_{i,-1}), L_{ex}(e_{i,-2}), \ldots, L_{ex}(e_{i,-R})$ and $L_{ex}(e_{i,-S})$. As opposed to the *a priori* LLRs of traditional EXIT charts [145,155,116], in our model the magnitude of the *a priori* LLR of the i^{th} chip is equal to the least confident LLR value of the previous chip that was utilized for generating a concatenated sequence. Hence, the procedure of evaluating the *a priori* LLR of the i^{th} chip $L_{apr}(e_i)$ is represented as [1, 53, 92, 116, 121].

$$\begin{aligned} L_e(e_i) = L_{apr}(e_i) \approx \Bigg[\prod_{m=1}^{M} \operatorname{sign}(L_{ex}(e_i - r_m)) \cdot \\ \prod_{n=1}^{N} \operatorname{sign}(L_{ex}(e_i - s_n))\Bigg] \times [\min\{|L(e_{i-r_1})|\}, \\ \{|L(e_{i-r_2})|\}, \ldots, \{|L(e_{i-r_M})|\} \\ \{|L(e_{i-s_1})|\}, \{|L(e_{i-s_2})|\}, \ldots, \\ \{|L(e_{i-s_N})|\}]\ \ \mathrm{i} = 0, 1, \ldots, I, \end{aligned} \tag{5.8}$$

where we assume that $L_{apr}(e_{-\infty}) = \ldots = L_{apr}(e_{1-r}) = L_{apr}(e_{-2}) = L_{apr}(e_{-1}) = 0$ and $L_{apr}(e_{-\infty}) = \ldots = L_{apr}(e_{1-s}) = L_{apr}(e_{-2}) = L_{apr}(e_{-1}) = 0$. Finally, the channel's output information $L(e_i|z_i)$ in Eq.(5.7) and the *a priori* information $L_{apr}(e_i)$ in Eq.(5.8) will yield the soft output of the SISO decoder related to the chip e_{out} as

$$\begin{aligned} L(e_{out}) &= L_{ex}(e_i) = L(e_i|z_i) + L_e(e_i) \\ &= L_e z_i + L(e_i) + \left[\prod_{m=1}^{M} \text{sign}(L_{ex}(e_i - r_m)\right. \\ &\left.\prod_{n=1}^{N} \text{sign}(L_{ex}(e_i - s_n)\right] \times [\min\{|L(e_{i-r_1})|\}, \\ &\{|L(e_{i-r_2})|\}, \ldots, \{|L(e_{i-r_M})|\} \\ &\{|L(e_{i-s_1})|\}, \{|L(e_{i-s_2})|\}, \ldots, \\ &\{|L(e_{i-s_N})|\}] \quad \text{i} = 0, 1, \ldots, I. \end{aligned} \tag{5.9}$$

Note that Eq.(5.9) represents the recursive relationship used for evaluating the consecutive chips required by a pair of m-sequence generators in order to produce the concatenated sequence. Thus, the acquisition device becomes more confident in correctly deciding the R and S consecutive chips from the magnitudes of the LLR in the SCRs of Fig. 5.3. When the SISO detector attains a channel output sample z_i linked to the chip e_i, it calculates the LLR utilizing Eqs.(5.8) and (5.9) for estimating the intrinsic information.

5.2.4.1 Algorithm used for Acquiring the Synchronization of the Concatenated Sequence

The followings are the basic steps involved in acquiring the concatenated sequence as shown in Fig 5.4.

- Step 1: Generate two m-sequences having the same length of $2^R - 1$ and $2^S - 1$, where R and S are the same polynomial order $[112, 113, 115, 154, 156]$. These two m-sequences have $+1$ and -1 values. As an example generated PPs are $g_{c_i}(D) = 1 + D^2 + D^5$ and $g_{d_i}(D) = 1 + D^3 + D^5$. We will use this example for further clarification throughout this algorithm.

- Step 2: As shown in Figs. 5.2, 5.3 and 5.4, we XOR c_i and d_i to obtain e_i, where e_i is mapped to $+1$ or -1, respectively as shown in Eq.5.5.

- Step 3: After transmitting e_i over AWGN channel, we obtain z_i as shown in Eq. (5.6).

- Step 4: z_i is fed to both soft decoders of Figs. 5.2 and 5.3, where SCR values are initialized to zero as the probability of zeros and ones will be the same.

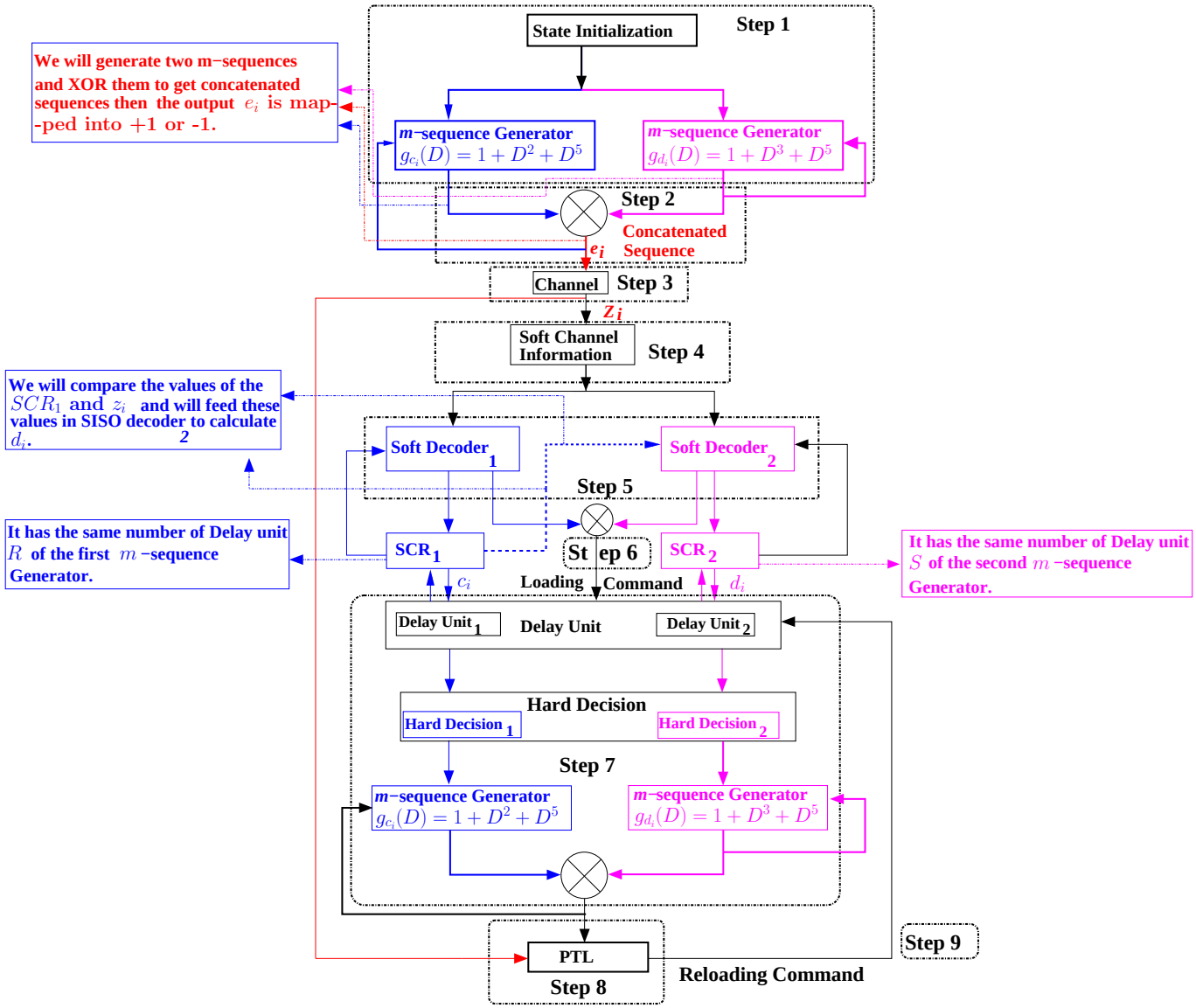


Figure 5.4: Flow chart of our proposed algorithm for obtaining the concatenated sequence.

- Step 5: After some iteration between the soft decoders and the SCRs of Figs. 5.2 and 5.3, we obtain the LLRs values by calculating Eq. 5.8. The $D(0), D(2), C(0)$ and $C(3)$ are the concerned taps involved in generating the PPs of two m-sequence to obtain concatenated sequence as shown in our proposed algorithm in Fig. 5.4. Fig. 5.4 manifests that for evaluating the soft information about d_i which is the other SISO decoder, we need to exploit the concerned taps of the first m-sequence generator, i.e. c_i. These tap values are $C(0)$ and $C(3)$ for the c_i value given above. As a result, the values of the first m-sequence SCR are utilized to calculate the *a priori* of the other shift register to decode the transmitted value of d_i at the receiver.

- Step 6: After obtaining the desired values, the loading command is activated by the SISO decoders, which helps to retrieve the data from the delay unit to perform hard decision as shown in Fig. 5.4.

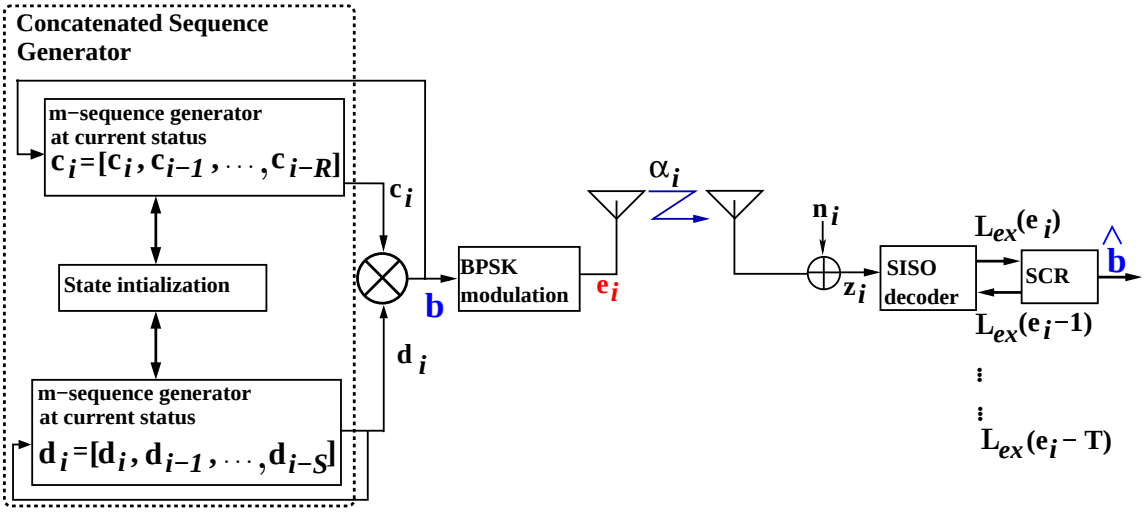


Figure 5.5: The system model used for the RSSE scheme of Fig. 5.3.

- Step 7: After gaining the information from the hard decision, the values 1 or 0 are processed to the LFSRs of the two m-sequence generator of Figs. 5.2 and 5.3. The output of these m-sequences are again XORed together.

- Step 8: The value calculated in Step 7 is compared with the value of z_i by the PTL, if these values match, then the synchronization is achieved by our purposed system.

- Step 9: If there is decoding error, then PTL will restart the command "Reloading command", which means we need to go back to Step 5, where the two m-sequences will have distinguished values in the delay units of the two m-sequence generators and the process will repeated again until the correct code is achieved.

5.2.5 Phase Tracking Loop

Finally, we discussed block marked as ⓔ in Figs. 5.2 and 5.3. Prior to despreading, the chip-SNR is typically too low for attaining accurate carrier phase tracking [149, 150]. The despread signal is then entered into the low-pass filter of Fig. 5.3. Following this, the information is forwarded to the Tracking Loop (TL) of Fig. 5.3. If the initial phase is determined accurately by the TL, then payload data reception may commence[5]. This procedure is repeated until correct code acquisition is accomplished.

[5]If not, the TL will activate the reloading command, where the two m-sequences will have distinguished values in the delay units of the two m-sequence generators.

5.3 EXIT Chart Analysis for Concatenated Sequence Design

Ten Brink introduced the principles of EXIT charts [145, 155] as an accurate mechanism of predicting the convergence characteristics of iteratively decoded techniques. They are capable of estimating the specific SNR value at which an infinitesimally low Bit Error Ratio (BER) can be achieved instead of conducting time-consuming bit-by-bit detection based Monte-Carlo simulations. To elaborate a little further, accurate EXIT chart techniques rely on the condition that the inputs of two SISO components of an iterative receiver have a Gaussian distribution, which can only be approached using a sufficiently long interleaver. Since this is not the case for our initial acquisition scheme, a bespoke EXIT-chart has to be conceived. Hence we introduce a novel EXIT chart design for predicting the convergence characteristics of our RSSE scheme utilized for investigating the evolution of the input/output Mutual Information (MI) transfer among the receiver's SISO components in successive iterations. In a traditional EXIT chart there are three components, namely the inner detector's MI-curve, the outer detector's MI-curve and the stair-case-shaped iterative detector trajectories based on a specific instance of iterative detection. More explicitly, the stair-case-shaped detection trajectory visualizes how much extra MI improvement is achieved during each iteration. This can be readily arranged, provided that interleavers are used between the inner and outer components. However, in contrast to the conventional EXIT chart [155], the same detector is operated repeatedly in our 'self-concatenated' approach, where the output of the acquisition scheme is used as its inputs in the next iteration, as portrayed in Fig. 5.5. More explicitly, Fig. 5.5 illustrates the two inputs of the SISO detector, namely the channel output and the SCR output of Fig. 5.3. Hence the inner and the outer decoders' EXIT curves are the same. However, they are mirrored with regard to the diagonal x=y of the EXIT curves, as shown in Fig. 5.6, where the Extrinsic Information (I_E) / *a priori* Information (I_A) is plotted against the intrinsic or *a priori* Information (I_A) / the Extrinsic Information (I_E), when the SNR is fixed to -2 dB. Fig. 5.6 also reveals that the polynomial $g_2(D) = 1 + D^3 + D^5$ requires 5 to 6 decoding iterations to reach the [1,1] point. Furthermore, the trajectory of $g_2(D)$ approximately matches the inner and outer curves represented by red solid lines. Again, the inner and outer curves are the same and have a mirror image with regard to the diagonal line x=y of the EXIT curves.

Below we examine the theoretical resemblance between the self-concatenated detection design of [147] and our existing initial acquisition problem. However, there is also a significant dissimilarity between them, since in [147] an interleaver was adopted for changing the detector's output before passing it back to its input. As opposed to this, we introduce the new concept of using EXIT charts without any interleavers. We arrange this by the online exploitation of the inherent correlation between the chips in the two m-sequence generators, as enforced by the LFSRs of Fig. 5.5 instead

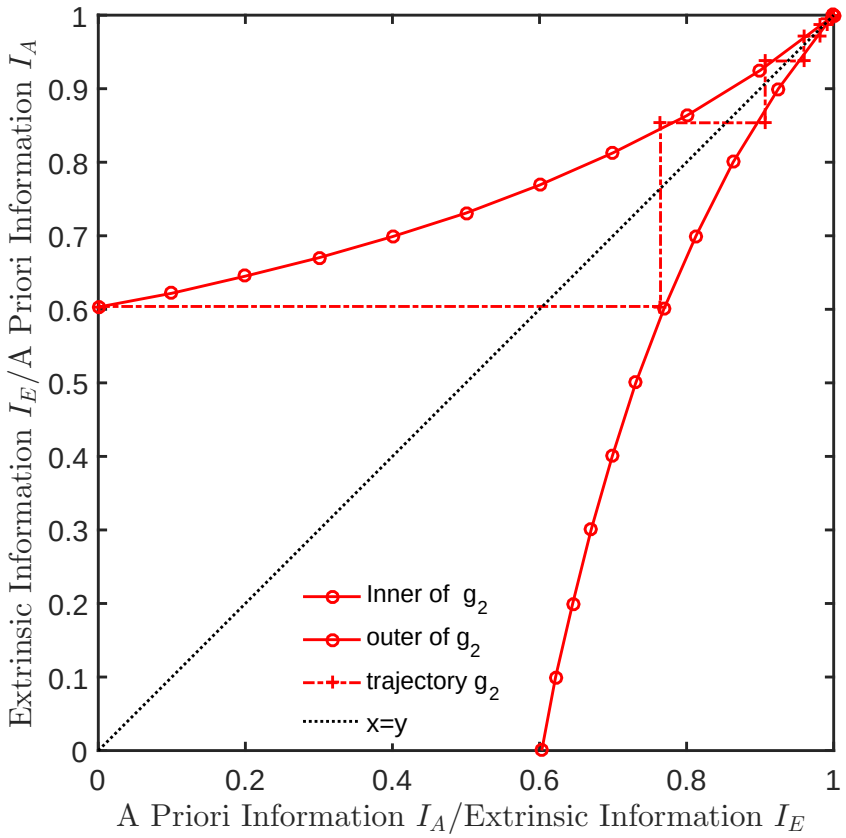


Figure 5.6: EXIT chart of $g_2(D) = 1 + D^3 + D^5$ over AWGN channels at SNR $= -2dB$.

of invoking any iterations for decoding similar bit sequences. This is the main aspect which differentiate it from the traditional EXIT chart.

The SISO decoder's output will be modified according to the *a priori* LLR values L_{ex}, which in turn, contains the extrinsic LLR values of the preceding iteration at the receiver of Fig. 5.5. Binary Phase Shift Keying (BPSK) is employed, the value e_i of the i^{th} generated chip also becomes the value of the first LFSR stage in the two m-sequence generators. As illustrated in Fig. 5.5, during reception the signal obtained by the SCR is fed back to the SISO decoder in form of the extrinsic LLR values $L_{ex}(e_{i-1}), \ldots, L_{ex}(e_{i-(T=R=S)})$ that were gathered during the most recent I detection iterations, which were estimated for the T earlier generated chips. Based on these previous extrinsic LLRs, the *a priori* LLR of E_i is calculated from Eq. (5.8). Later, the extrinsic LLR of e_i is evaluated from Eq. (5.9) and the same method is also used for the subsequent chip e_{i+1}. Again, the task of the SCR in Fig. 5.5 is to store the most recent T extrinsic LLRs and to shift them by one position. Once a detection iteration[6] has been carried out, a hard decision is invoked and the most recent estimate of the generator's concatenated sequence $\hat{\boldsymbol{b}}$ becomes available.

[6]Each iteration refers to the exchange of information between the SISO decoder and the SCR of Fig. 5.5 where the iteration depends upon two factors, namely on the number of chip received and on the polynomial order.

5.3.1 Self-Concatenated Approach

In the self-concatenated approach of [145,147], the same detector/decoder component is used twice, namely once as the inner SISO component and once as the outer SISO component, as shown in Fig. 5.5. The SISO detector has two inputs, namely the output of the two m-sequence generators and the channel's output. The LLR $L_e(e_i)$ is determined by the SISO detector. Note that the receiver utilizes the information of the two m-sequence generators, related to the time instant of determining the *a priori* LLR values. Thus, the information in the LFSRs of the two m-sequence generators will be shuffled during each SISO iteration, therefore we have to store the previous values of $\hat{\boldsymbol{b}}$, which are constituted by the $(2^R - 1)$ and $(2^S - 1)$ values of the two m-sequence generators having the same length. Again, for the sake of avoiding any acquisition delay, we do not employ any interleaver in our self-concatenated system represented by Fig. 5.5. This is the specific feature that differentiates our approach from the traditional EXIT charts [155]. Therefore, we may observe a conceptual similarity with the self-concatenated decoding approach of [116, 145]. Again, our basic EXIT chart model relies on Fig. 5.5, where there is a single detector processing different inputs during its two operating phases. The channel's output is used as the initial input of the SISO decoder. The SCR's output in Fig. 5.5 is the second input of the SISO detector, which shifts the extrinsic LLR sequence, hence its action is reminiscent of the basic role of an interleaver in a traditional iterative receiver. Hence, the SISO detector computes $L_e(e_i)$ based on Eq. (5.8).

5.3.2 Mutual Information

In this scenario, we opted for time-averaging in order to determine the MI between the associated extrinsic LLRs and the chips generated [1, 145, 155].

5.4 Simulation Results

In this section the polynomial orders of 5, 6, 13, 15 and 23 are selected, because these sets are extensively used in wireless communication [1, 55, 92, 121, 157, 158]. Among the PPs having similar orders, we opt for the PPs having the best P_e versus SNR performance. This section is divided into the following five subsections. Section 5.4.1 deals with the performance of the m-sequence. Section 5.4.2 quantifies the performance of the Concatenated sequence, while in Section 5.4.3 our P_e versus SNR performance comparisons of the m- and Concatenated sequences are provided. Finally, in Section 5.4.4 the AT is evaluated, while Section 5.4.5 deals with the EXIT chart analysis of both the m- and concatenated sequences.

Fig. 5.7 depicts the performances of the PP $g_5(D) = 1+D+D^3+D^4+D^{13}$ having a period of $N = 2^{13} - 1 = 8191$ chips produced by a 13^{th}- order polynomial. The

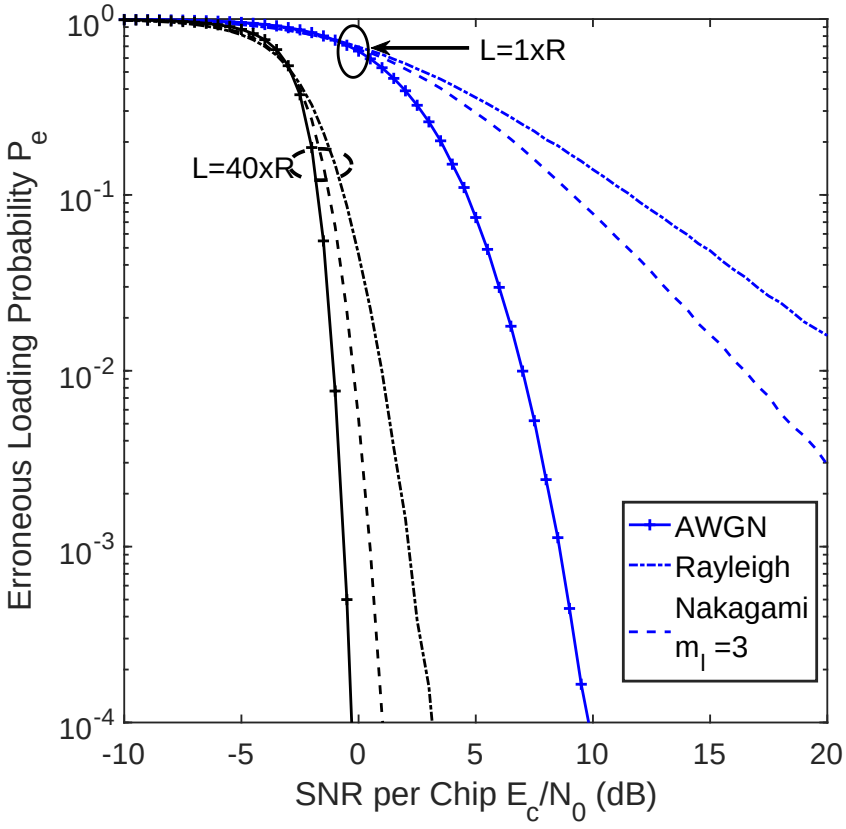


Figure 5.7: Performance comparisons between three different communication channels.

affordable number of iterations is $L = (40\times\ R)$, where L is the total number of chips that the SISO decoder processes and R denotes the number of chips corresponding to the PP's order. In Fig. 5.7, the acquisition performance of the RSSE technique is evaluated for transmission over three different communication channels. It can be concluded that reliable acquisition is achieved above an SNR value of $-0.5\ dB$ by entering $40 \times 13 = 520$ chips into the SISO detector, when transmitting through an AWGN channel. It is also inferred that for a given SNR value, P_e decreases upon increasing the number of received chips entered into the SISO detector. Fig. 5.7 illustrates that for a given number of received chips input into the SISO detector, the SNR gain attained for an AWGN channel is significantly lower than those under a Nakagami channel having $m_l = 3$ as well as under a Rayleigh channel. Naturally, our RSSE scheme attains a lower P_e for an AWGN than for fading channels. To limit the paper's length, only an AWGN channel is considered for our further simulations.

5.4.1 Performance Results for m-sequences

Table 5.1 describes the PPs used for constructing the m-sequences. The affordable number of iterations is $L = (200\ \times\ R)$, and the total length of the m-sequence is $(2^R - 1)$. Our P_e versus SNR comparisons are recorded for various PPs, as depicted

Groups	Polynomials	Representation of polynomials
A	$g_1(D)$, $g_2(D)$	$(0, 2, 5)$, $(0, 3, 5)$
	$g_3(D)$, $g_4(D)$	$(0, 1, 6)$, $(0, 5, 6)$
B	$g_6(D)$, $g_7(D)$	$(0, 1, 15)$, $(0, 4, 15)$
	$g_8(D)$,	$(0, 5, 23)$,
C	$g_5(D)$, $g_9(D)$	$(0, 1, 3, 4, 13)$, $(0, 5, 11, 17, 23)$
D	$g_{10}(D)$	$(0, 2, 3, 5, 6, 7, 8, 9, 10, 11, 13)$
	$g_{11}(D)$	$(0, 1, 2, 3, 4, 5, 6, 8, 10, 12, 13)$
	$g_{12}(D)$	$(0, 2, 3, \ldots, 15)$

Table 5.1: Primitive Polynomials (PPs) invoked for our RSSE scheme, where g_{12} has consecutive feedback taps ranging from 2 to 15

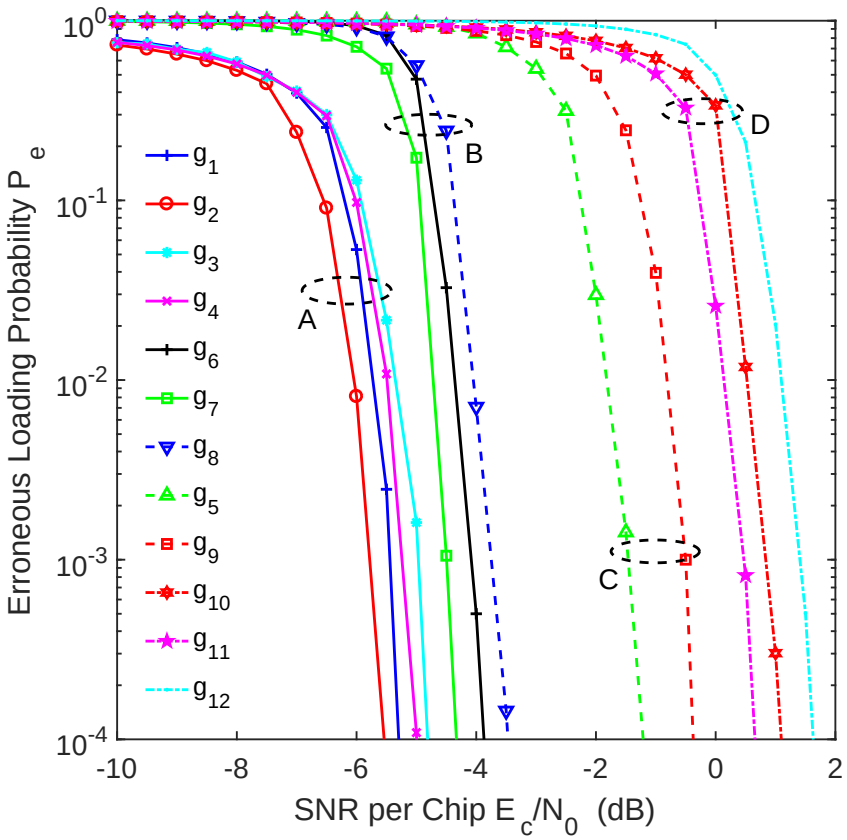


Figure 5.8: Performance comparisons between Primitive Polynomials (PPs) having three and more feedback taps, where A, B, C and D represent groups of PPs showing similar performance of m-sequences.

in Fig. 5.8, where the groups A, B, C and D are created by grouping the curves according to their P_e versus SNR performance. In group A, we have four PPs, namely (g_1, g_2) and (g_3, g_4) having orders of 5 and 6, respectively. The PP g_2 has a better performance than g_1, since its second feedback tap is connected to the third position of the entire feedback tap arrangement (tap 3), whereas in g_1 the second feedback tap is linked to the second position (tap 2), as described in Table 5.1. It is observed that PPs g_3 and g_4 have consecutive taps, where g_3 performs worse, because its consecutive taps are at lower connection indices of 0 and 1 (taps 0 and 1), whereas the consecutive taps of g_4 are located at higher connection indices of 5 and 6 (taps 5 and 6). More explicitly, g_2 has the best performance because it belongs to a lower-order PP and its second feedback tap is connected to a higher index than the second tap of g_1. The minimum of the LLR values of all the tap connections are used to generate the extrinsic information. For this reason, the transmitted PP using a low number of tap connections associated with the higher indices has a higher likelihood of giving the exact extrinsic information for the SISO acquisition design, than that of utilizing a high number of tap connections. In group B, we have three PPs, namely g_6, g_7 and g_8 as portrayed in Table 5.1, where g_6 and g_7 have the order of 15. Here, g_7 performs better than g_6, since the former does not contain any consecutive feedback taps. In g_6 consecutive feedback taps are present at indices 0 and 1 (taps 0 and 1). Since these consecutive taps act as a switch and during normal operation they may become contaminated by the noise, the performance of g_6 is worse than that of g_7.

Furthermore, g_8 has a PP order of 23, as depicted in Table 5.1, hence it has a worse performance as compared to g_6 and g_7. When comparing the PPs of different order, PPs having higher order exhibit a longer memory requirement and they exhibit excessive confidence in their own soft approximations. Therefore, they do not benefit sufficiently from the extrinsic information provided by the iterative scheme. It also transpires from Fig. 5.8 that if the taps are non-consecutive and the PP's order is lower, the SNR required for achieving a given P_e will be lower, especially for lower-order PPs, since less taps become less contaminated by noise than those having a higher number of taps.

In Table 5.1, group C has (g_5, g_9), whereas g_{10}, g_{11}, and g_{12} belong to group D, since they all contain more than three taps. As visualized in Fig. 5.8, the SNR performance is degraded, as the number of consecutive feedback taps is increased. In group C we have g_5 and g_9, where g_5 performs better than g_9, because it has a 13 order PP, while g_9 has a 23 order PP. More explicitly, in group D g_{12} has more consecutive feedback taps than the rest of the group, namely as many as 2 to 15 taps, where each feedback-sample is noise-contaminated, hence degrading the achievable performance. Upon comparing the performances of PPs having an order of 13, i.e. g_{10} and g_{11} generated using 10 taps each, it is found that both PPs have two consecutive feedback taps. The PP g_{11} leads to an improved performance, because second higher feedback tap is connected to index 12 while in g_{10}, the second most index is connected

Groups	Representation of Polynomials	Polynomials Achieved by Concerned PPs	Polynomial Order
E	$gg_1(D)$	$g_1(D) \oplus g_2(D)$	5
F	$gg_2(D)$	$g_3(D) \oplus g_4(D)$	6
G	$gg_3(D)$	$g_6(D) \oplus g_7(D)$	15
H	$gg_4(D)$	$g_8(D) \oplus g_9(D)$	23
I	$gg_5(D)$	$g_5(D) \oplus g_{11}(D)$	13
J	$gg_6(D)$	$g_5(D) \oplus g_{10}(D)$	13
K	$gg_7(D)$	$g_7(D) \oplus g_{12}(D)$	15
L	$gg_8(D)$	$g_6(D) \oplus g_{12}(D)$	15

Table 5.2: Generation of concatenated sequence from Primitive polynomials invoked for our RSSE scheme

to index 11.

We infer that the detection capability of the receiver is reduced by the presence of consecutive feedback taps. The receiver exploiting g_{11} has a better chance of detecting the chips in the presence of noise as opposed to that employing g_{10}, since the detection capability of the receiver is degraded proportionally to the connecting indices of the feedback taps.

Based on our simulation results seen in Fig. 5.8, we conclude that the performance of the PPs predominantly depends upon three factors, namely on the order of the PP, on the number of connecting taps and on the specific indices of the connecting taps. When comparing PPs of similar order, PPs with less connecting taps will outperform those having a higher number of connecting taps, since the latter precipitated the noise-effects by having more feedback taps. Furthermore, if the connecting taps are same, then PPs with the second highest indices perform better. Therefore, the required SNR depends partially on the specific positions of vacant indices, when comparing PPs having similar orders. Finally, when comparing PPs of different order, the low-order PPs avoids the avalanche-like error-propagation of higher-order PPs, since the noise imposed on the chips of lower-order PPs results in fewer inaccuracy transmission than of higher-order PPs.

5.4.2 Performance of the Concatenated Sequences

We proceed by generating results for the concatenated sequences by utilizing the affordable number of iterations given by L = ($200 \times R$ or S), where R and S represent the two PPs of the same order. A total of eight concatenated sequences are generated

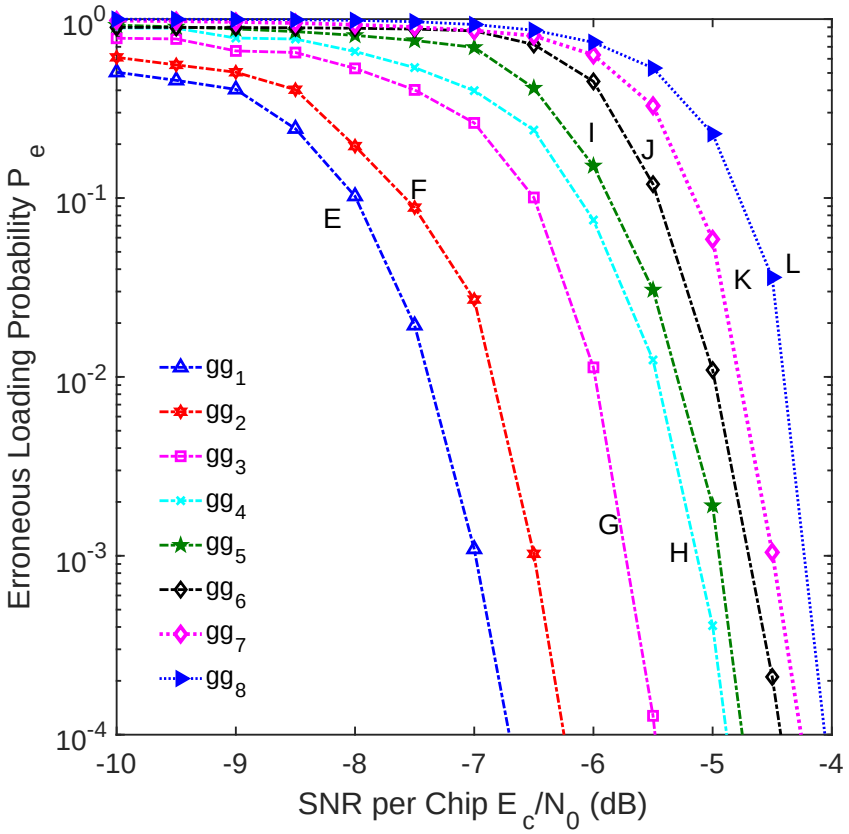


Figure 5.9: Performance comparisons between the different concatenated sequences, where E, F, G, H, I, J, K and L represent the concatenated sequences generated by two different PPs of the same length, as illustrated in Table 5.2 and gg denotes concatenated sequences.

as shown in Fig. 5.9 by utilizing the information given in Table 5.2, where E to L represent the concatenated sequences denoted as gg. The P_e versus SNR performance of the concatenated sequences demonstrates that the low-order PPs perform better than the high-order PPs, if they have fewer taps. The performance of gg_1 is superior to the rest, because it has a lower polynomial order of 5 as evidenced by Fig. 5.9. The performance of gg_3[7] is better than gg_7[8] and gg_8[9], despite having the same polynomial order of 15.

Therefore, similarly to the m-sequence's case, it can be inferred that PPs having less taps provide a higher likelihood of accurate extrinsic information for the SISO acquisition model. Consequently, PPs having fewer taps are adopted, as the malevolent effects of noise contaminates their chips less gravely, than for their higher-order counterparts. Furthermore, gg_1 performs better than the rest of the PPs, since it relies on a shorter memory. However, gg_1 has less confidence in its own soft values and thus it benefits more substantially from the use of an iterative scheme.

[7] gg_3 is obtained by two different PPs of order 15, namely g_6 and g_7 having three taps.
[8] gg_7 is obtained by two different PPs of the order 15, namely g_7 and g_{12} having three and fourteen taps respectively.
[9] gg_8 is obtained by two different PPs of the order 15, namely g_6 and g_{12} having three and fourteen taps respectively.

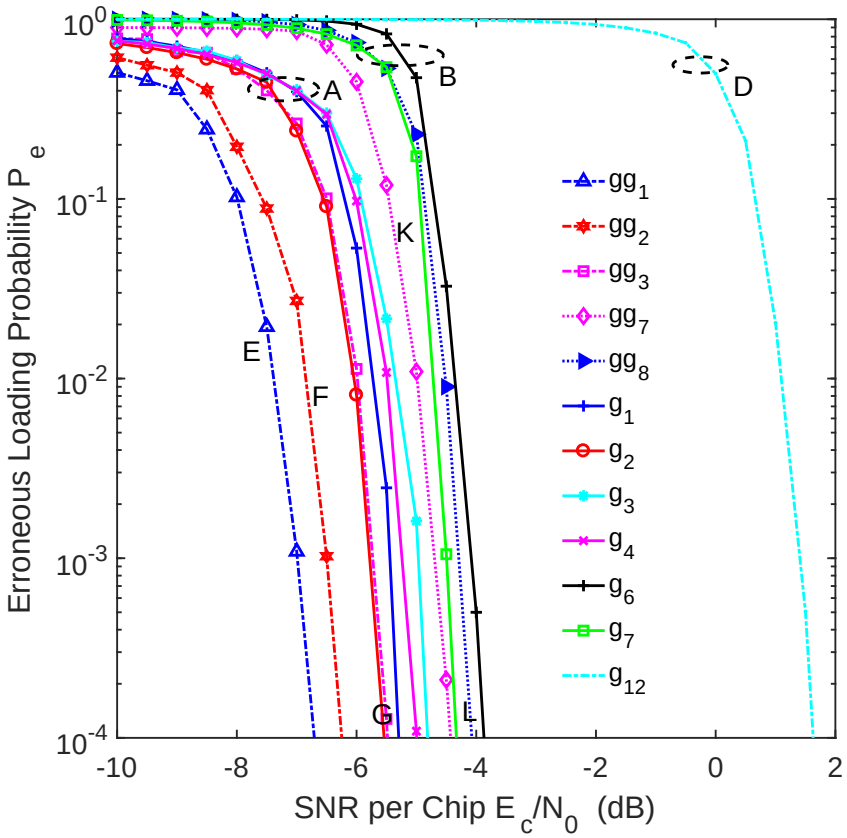


Figure 5.10: Comparisons between concatenated sequences and m-sequences are provided for polynomial orders of 5, 6 and 15. The dotted lines show the performances of concatenated sequences.

5.4.3 Comparison between the m- and the Concatenated-Sequences

Let us now embark on comparing two types of PN sequences. A variety of simulation results are obtained for distinguishing the performances of the RSSE in an AWGN channel. In Figs. 5.10 and 5.11, P_e versus the SNR comparisons are recorded for the polynomial orders of 5, 6, 13, 15 and 23 for both m- and concatenated sequences. It may readily be inferred that the performances of concatenated sequences are better than those of m-sequences, which are represented by the dotted lines and are labelled as E, F, G, K and L in Figs. 5.10 and 5.11. We achieve a 1.85 dB gain for the best case upon comparing gg_1 to g_1 and also attain 1.5 dB gain compared to g_2, as observed in Fig. 5.10 for group E. This conclusion is confirmed by comparing the blue dotted line of gg_1 to the red solid line of g_2 and the blue solid line of g_1 to the blue dotted line of gg_1, which represents the PP order of 5 having three taps. When we compare PPs gg_2 to g_3 and g_4 of order 6 having three taps, we acquire a 1.85 dB gain in the best-case upon comparing gg_2 to g_3 and 1.5 dB gain, when compared to g_4. This result indicates that by using a low-order PP we can achieve a better performance for concatenated sequences. In Fig. 5.10, gg_3 performs better than gg_7 and gg_8. Upon comparing gg_3 to the chosen m-sequences, it is observed that in the best-case P_e

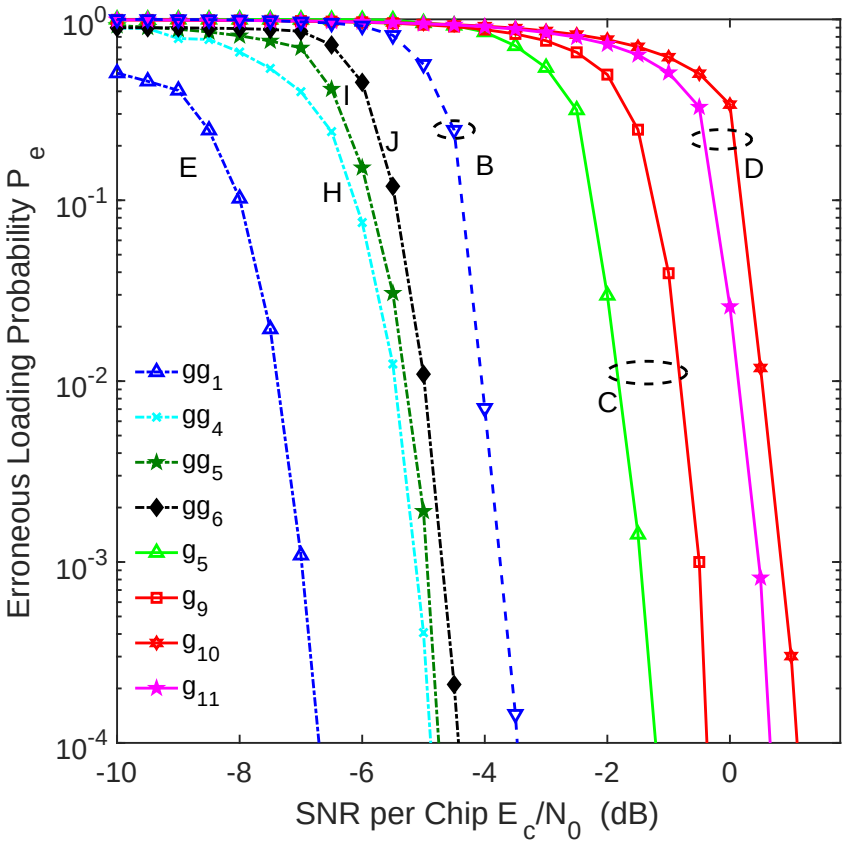


Figure 5.11: Comparisons between concatenated and m-sequences are carried out for PPs of 5, 13 and 23 order. The dashed lines show the performances of concatenated sequences.

versus SNR performance scenario of g_6 we obtain 1.85 dB gain by gg_3 over g_6 and 1.5 dB gain when compared to g_7, since it has the order 15 having three taps. When considering gg_7, we achieve 0.75 dB gain compared to g_7, while upon comparing g_6 to gg_8 denoted by L in Fig. 5.10 we obtain 0.75 dB gain. For the polynomial order of 15, we obtain 7.5 dB gain in the best-case upon comparing gg_3 to g_{12} as g_{12} contains all consecutive taps located at the positions 2 and 15 (taps 2 and 15). For the worst case, we obtained at most 5.8 dB gain, if we compare gg_8 to g_{12}, as depicted in Fig. 5.10.

In Fig. 5.11 we have compared m- and concatenated sequences of the polynomial orders of 5, 13 and 23. It is evident that the concatenated sequences perform better than m-sequences. For the polynomial order of 5, the performance gain of concatenated sequences is 1.5 dB for the worse-case scenario when comparing the SNR at a P_e values of 10^{-4}, as discussed earlier in the context of Fig. 5.10. For a polynomial order of 13, gg_5 achieves a 5.5 dB gain for the best-case scenario over g_{11} and even in the worst-case we achieve a 3.0 dB gain over g_5.

This is because the concatenated sequence gg_5 is composed of the PPs g_5 and g_{11} having an order of 13. The PP g_5 has two consecutive taps, namely one located at the positions of 0 and 1 (taps 0 and 1) and the other located at the positions

3 and 4 (taps 3 and 4), similarly, PP g_{11} also has two consecutive taps, namely one located at the positions of 0 and 6 (taps 0 and 6) and the other located at the positions 12 to 13 (taps 12 to 13). This indicates that the presence of consecutive taps dominates the performance of the PPs. More clearly, these consecutive taps gravely boost the deteriorated effect of noise. Hence the performances of gg_5 and gg_6 are better than those of g_5, g_{10} and g_{11}. On the other hand, for the worst-case, we obtain at most 5.5 dB gain if we compare gg_6 to g_{10}, as depicted in Fig. 5.11. Furthermore, for gg_4 the gain attained is 1.35 dB compared to g_8 of a polynomial order of 23, where this concatenated sequence is composed of g_8 and g_9, as depicted in Tables 5.1 and 5.2, respectively. Upon considering the polynomial order of 23 and comparing gg_4 to g_9, we attain a gain of 3.8 dB. In summary, PPs having more taps are substantially influenced by the noise imposed on them, therefore they cannot provide better LLR values than their counterparts having less taps, which can be visualized upon comparing gg_3 to both gg_7 and to gg_8.

5.4.4 Comparison between the Acquisition Time of m- and Concatenated-Sequences

Our iterative detection aided RSSE acquisition technique proficiently exploits the reliabilities of the latest successive chips during examining the magnitudes of the related soft outputs stored in the SCRs of Fig. 5.5. When P_e is as low as 10^{-4}, successful m-sequence acquisition can typically be declared with a sufficiently high likelihood after the initial loading of the chips. Resultantly, the total AT of the RSSE acquisition technique may be approximated by the time interval required by the RSSE for carrying out SISO detection, at a sufficiently low P_e. According to the iterative decoding principle [124, 144], the time required by the RSSE scheme for operating at a sufficiently low SNR value[10] and for generating a recursive SISO detection output depends both upon the number of stages, as well as on S and R in the associated m-sequence generators. Based on our design proposed in Fig. 5.5 the performance of the RSSE acquisition technique is determined by the SCR having the periods of S and R for the two m-sequence generators.

Fig. 5.12 characterizes the acquisition performance of the 13^{th} order polynomial g_5 having a length of $N = 2^{13} - 1 = 8191$ chips. Observe in Fig. 5.12 that $P_e = 10^{-4}$ is achieved at an SNR value of 9.5 dB by entering $L = 1 \times R = 1 \times 13 = 13$ chips into the iterative SISO detector of Fig. 5.5. In this case our system does not have any *a priori* information, hence it acts as the traditional acquisition technique of [102]. However, we can achieve a better performance by entering more chips into the proposed iterative acquisition technique scheme. As seen in Fig. 5.12, by entering $L = 40 \times R = 40 \times 13 = 520$ chips into the iterative SISO detector of Fig. 5.5 we achieved $P_e = 10^{-4}$ at an SNR value of -0.8 dB. Furthermore, we attained a better

[10]The value indicates that P_e is in the range of between 10^{-3} to 10^{-4}.

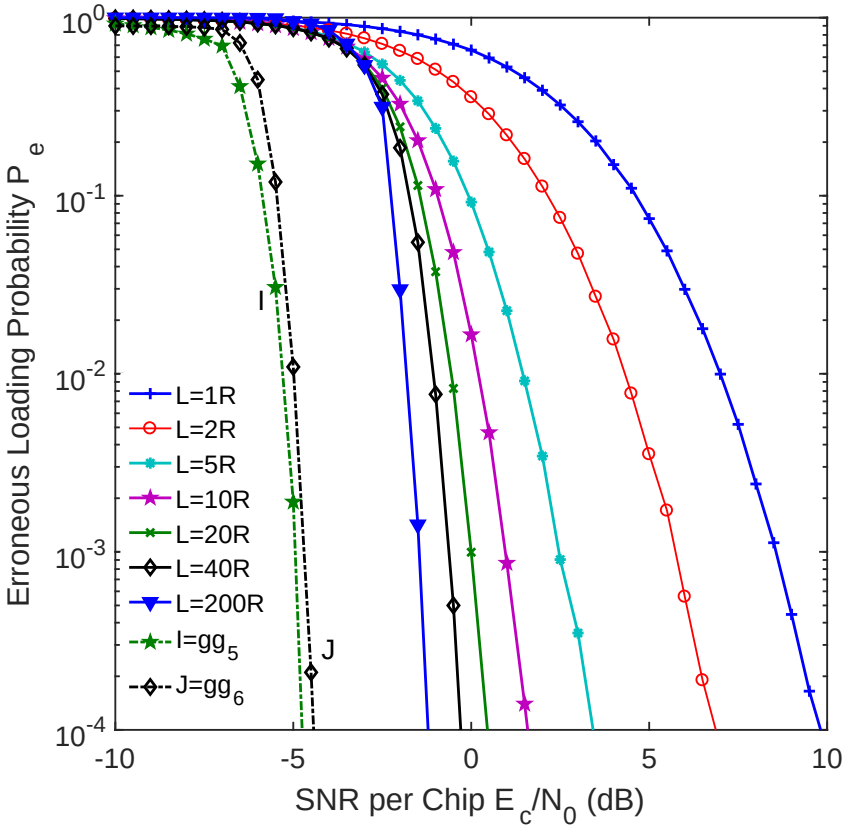


Figure 5.12: Erroneous loading probability P_e versus SNR parametrized by the number of chips entered into the recursive SISO decoder, when transmitting the m-sequence generated using the PP of $g_5(D) = 1 + D + D^3 + D^4 + D^{13}$ over an AWGN channel, where $gg_5(D)$ and $gg_6(D)$ are the concatenated sequences.

SNR value of $-1.8\ dB$ at a $P_e = 10^{-4}$ upon entering $L = 200 \times R = 200 \times 13 = 2600$ chips into the SISO detector. Therefore, the SNR gains at a P_e of 10^{-4} are about 10.3 to 11.3 dB compared to the traditional acquisition technique of [102], when the total number of received chips are 520 and 2600, respectively. Even though a total of 2600 chips have been received by the SISO scheme for attaining $P_e = 10^{-4}$ at the SNR per chip of $-1.8\ dB$, the AT still remains significantly inferior to that of any traditional serial search technique [119, 159]. This observation indicates that the AT is directly proportional to the length of the sequences measured, which is 8191 chips in this case. As compared to the concatenated sequences of similar orders, such as gg_5 and gg_6, the required SNRs are -4.9 and $-4.6\ dB$, respectively when entering 2600 chips into the iterative SISO detector for attaining reliable acquisition. It has been stated in [119] that the AT τ_D of a conventional technique has to obey $N_{\tau_D/2}$[11] $= 4095 \cdot \tau_D >>$ 2600 chips, even if the SNR value is sufficiently high. Therefore, the proposed RSSE acquisition technique becomes the best, substantially outperforming the best known benchmarkers of [7, 92, 119, 123, 160].

[11] $N_{\tau_D/2}$ represents the mean acquisition time of a sequence having a particular chip length, i.e. 8191. and τ_D corresponds to the dwell time which normally spans from hundreds to thousands of chip periods [119]

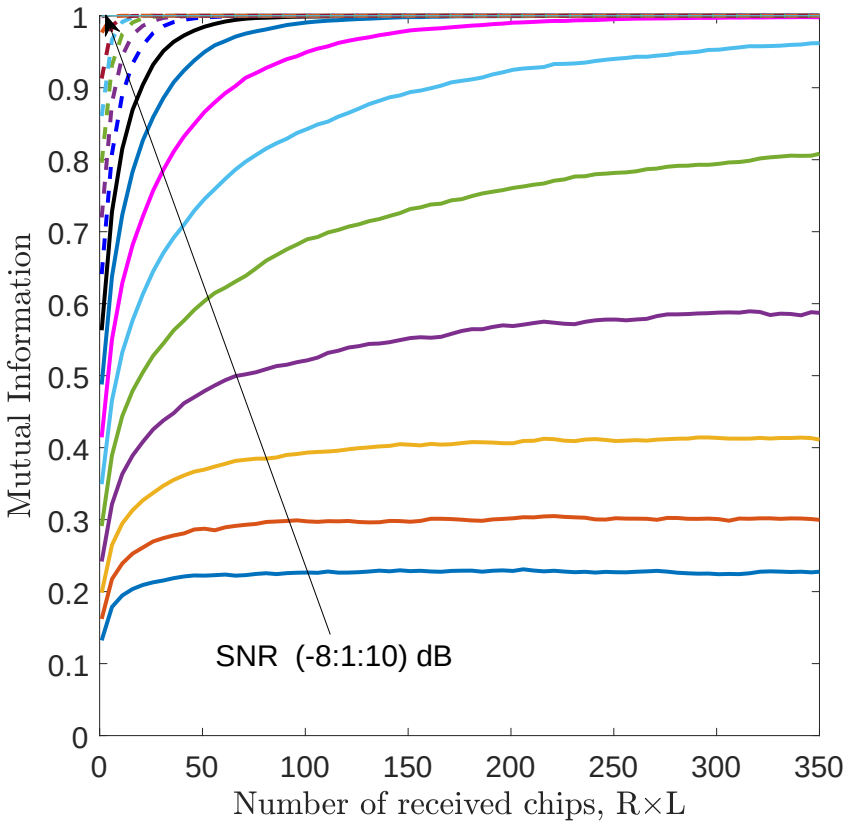


Figure 5.13: Mutual information versus the number of received chips for the m-sequence of PP $g_1(D) = 1 + D^2 + D^5$ having a polynomial order of 5 parametrized by various SNR values ranging from -8 to 10 dB having a maximum of $L = 70$ decoding iterations to reach MI= 1

5.4.5 EXIT Chart Analysis of Concatenated Sequences

The relationship between the MI and the number of received chips is revealed by Fig. 5.13, when the PP g_1 of Table. 5.1 is used. As expected, the MI of the PP g_1 increases upon increasing the number of received chips, provided that the SNR is increased. We may infer from Fig. 5.13 that we need fewer received chips to approach $MI = 1$ upon increasing the SNR. The results of Fig. 5.13 also reveal that for SNR values higher than -3 dB, the MI reaches unity after receiving at most 300 chips. The PP g_1 has $R = 5$ register stages, hence the highest number of detection iterations is given by the ratio of the number of received chips to the polynomial order. Hence we have L= 350/5 = 70.

Fig. 5.14 shows the MI versus the number of received chips for the PP gg_1 of Table 5.2. We observe that a lower number of received chips is required to approach MI=1 at a higher value of SNR. Furthermore, we infer that the MI approaches unity after receiving less than 100 chips for SNRs higher than -4 dB. Upon comparing Fig. 5.13 to Fig. 5.14, we observe that the concatenated sequences need fewer iterations to achieve MI=1 than the m-sequences. Hence, the performance of the concatenated sequence is better than that of the m-sequence.

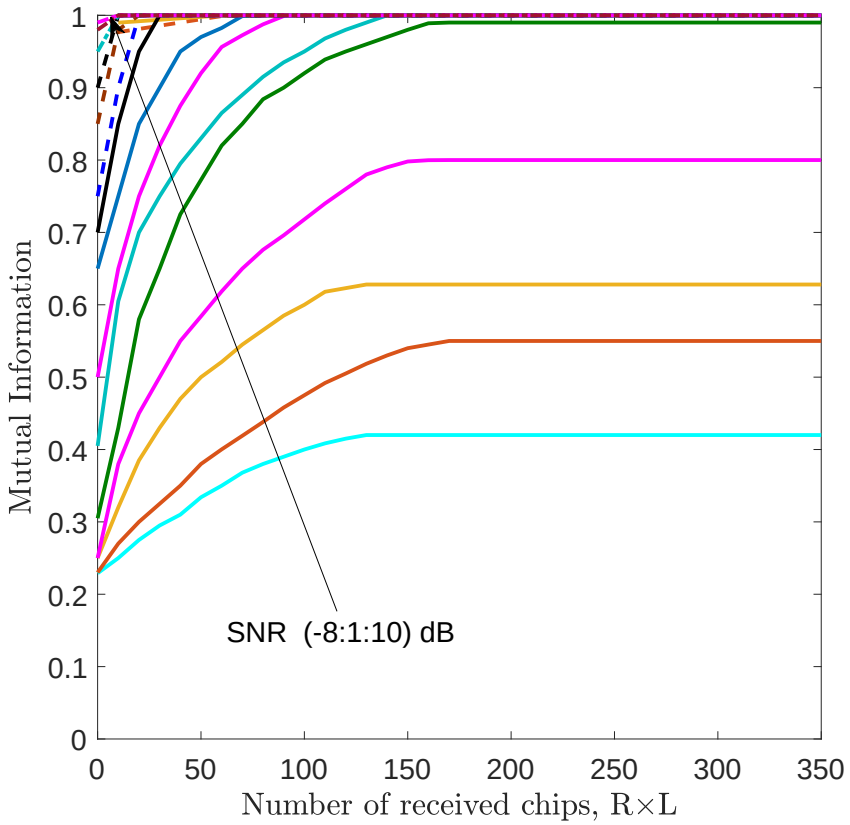


Figure 5.14: Mutual information versus the number of received chips for the concatenated sequence of PP $gg_1(D) = g_1(D) \otimes g_2(D)$ having the polynomial order of 5 parametrized by various SNR values ranging from -8 to 10 dB having a maximum of $L = 70$ decoding iterations to reach MI= 1

Fig. 5.15 depicts the Average Mutual Information (AMI) versus the number of iterations at an SNR of 0 dB, when PPs of different orders are utilized for generating m-sequences. It is predicted that the AMI becomes unity for a maximum of 25 iterations. Fig. 5.15 also shows that PPs associated with a lower polynomial order perform better, which is a benefit of their lower number of taps. Moreover, when comparing PPs, which have the same order and a similar number of taps, the ones having their second tap at a higher index result in a higher AMI after a specific number of iterations. The AMI analysis also corroborates that PPs having less taps guaranteed better performance than those having more taps, because the adverse effects of noise imposed on their chips resulted in lower distortion than for their counterparts having more taps, as exemplified by comparing g_5 to both g_{14} and to g_{15}, respectively.

Fig. 5.16 characterizes the AMI versus the number of iterations at an SNR of 0 dB, when PPs of the same order are used for producing concatenated sequences. It is anticipated that for any PPs employed for generating the concatenated sequence we need fewer than 18 iterations to approach the maximum MI of one. Fig. 5.16 also reflects the same fact that the PPs of lower order perform better due to having

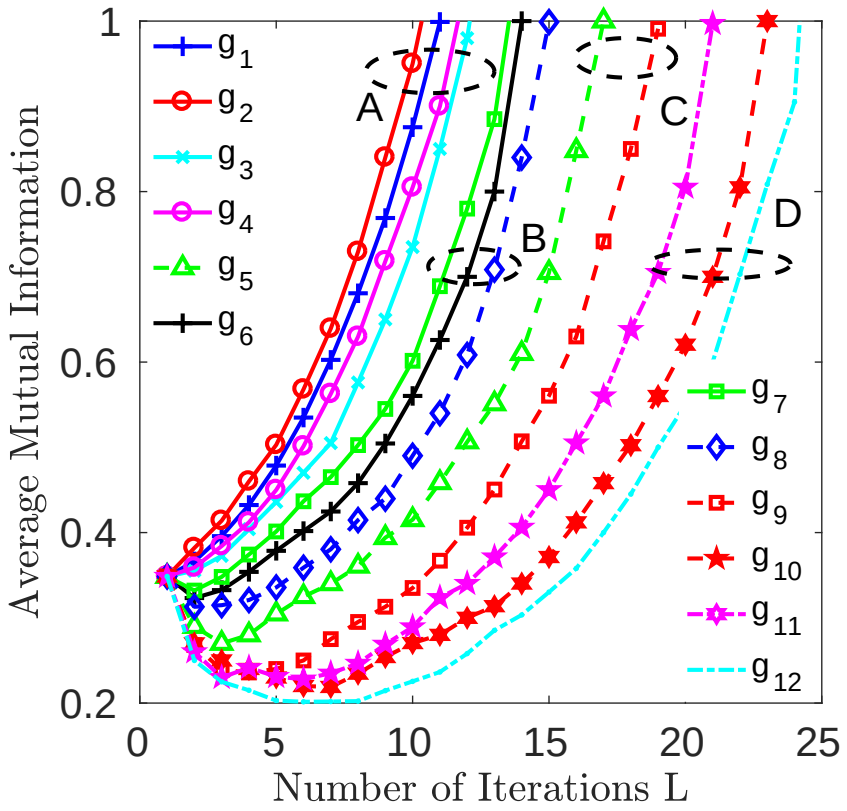


Figure 5.15: Average mutual information versus the number of decoding iteration when SNR = 0 dB for m-sequences.

less taps, as discussed earlier in Figs. 5.11 and 5.15. Similarly, Fig. 5.17 shows our comparison between the performances of m- and concatenated sequences by plotting the AMI against the number of iterations. The results also confirm the same trend as those found in Figs. 5.15 and 5.16.

Table 5.3 compares three major factors in the focus of this analysis, namely the P_e versus SNR, the location of the second tap present in the PP as well as the number of iterations. Our findings of Figs. 5.9 to 5.17 as well as Table 5.3 corroborate that the concatenated sequences have superior performance in terms of P_e versus SNR when different orders of PPs are compared. It can also be concluded that any pair of concatenated sequences require less iterations to achieve AMI=1 and attain a better iteration gain compared to m-sequences. Fig. 5.18 illustrates the EXIT chart of the self-concatenated method used for characterizing the RSSE technique at an SNR value of 0 dB. We have selected PPs according to their P_e versus SNR performances and AMI versus iteration index. The PPs having orders of 5, 13 and 23 are used for generating the EXIT-trajectories. It is observed that all detection trajectories match their related outer and inner decoder curves. Based on the open EXIT tunnel we expect a low BER for an RSSE receiver, namely when an open EXIT tunnel is guaranteed between the inner/outer decoder's EXIT curves. When the open tunnel becomes wider, less iterations are required.

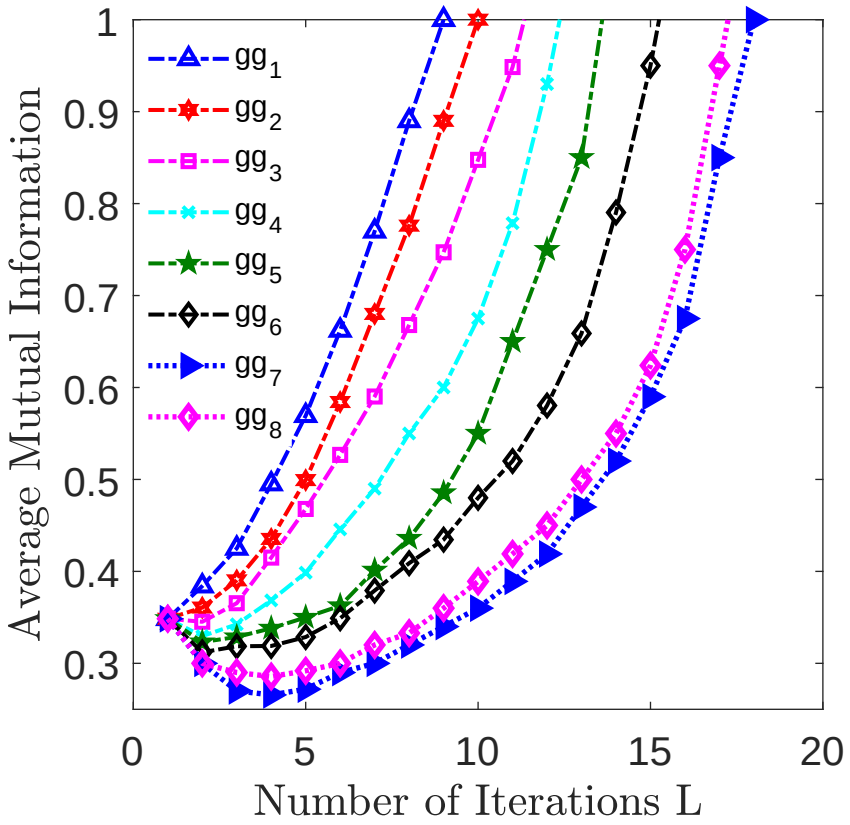


Figure 5.16: Average mutual information versus the number of decoding iterations at SNR = 0 dB for concatenated sequences.

Additionally, it can be observed that the PP g_{11} of order 13 failed to reach the [1,1] position at the top right end, since the outer and inner curves intersect prior to reaching the [1,1] point. Hence, the decoding trajectory exhibits no MI improvements beyond the crossover point. As expected, a lower number of taps widens the gap between the inner and outer EXIT curves. Furthermore, the associated decoding trajectory perfectly matches the inner and outer EXIT curves. We also deduce that the m-sequences having more taps tend to require larger memory and therefore a reduced iteration gain is attained. Both g_5 and g_{11}, perform worse than the other PPs, because they have more feedback taps, as discussed in Section 5.4.2. Accordingly, we conclude that the use of a lower number of taps provides wider opening between their inner and outer decoder curves and have better match between their stair-case-shaped decoding trajectory and the EXIT-curves of the inner and outer decoders.

Fig. 5.19 demonstrates that the polynomial gg_1 of Table 5.3 approaches the [1,1] point at SNR = 0 dB. An improved resemblance amongst the detection trajectories as well as the outer and inner EXIT curvatures arises at higher SNR values. This illustrates that the EXIT chart trends confirm the AMI-trends of Figs. 5.15 and 5.16. Explicitly, the lower-order PPs have a superior convergence, since they benefit more substantially from the iterative procedure. Accordingly, PPs having more taps are

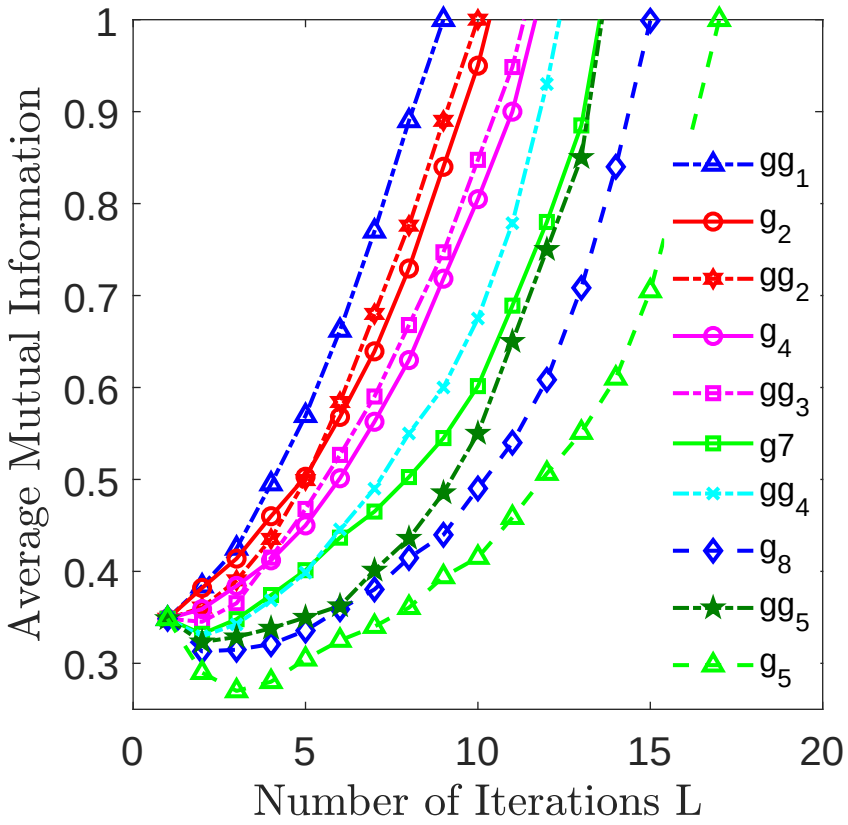


Figure 5.17: Comparison between m- and concatenated sequences w.r.t. the number of decoding iterations versus average mutual information when plotted at SNR = 0 dB.

directly influenced by the noise and need more iterations to attain error-free decoding. We further benchmark the performance of our system by investigating PPs of the order 13 in Fig. 5.20. The PP gg_5 of Table 5.3 requires the least detecting iterations to approach the [1,1] point at SNR = 2 dB. Moreover, by invoking more decoding iterations, the SISO detector approaches the [1,1] point of perfect convergence to a vanishingly low P_e. Therefore, we conclude that the lower-order polynomials having less taps perform better, despite requiring less computations.

5.5 Conclusions

We conclude that the performance of concatenated sequences is superior to that of m-sequences, when comparing their P_e versus SNR performance. When considering PPs having the same order but different number of taps, the PPs having less taps outperform the PPs having more taps. This is due to the noise affecting the chips of PPs having more taps more gravely, than their counterpart having less taps. In other words, the PPs relying on a low number of tap connections have a higher probability of reaching MI = 1 for the SISO acquisition technique than those utilizing a higher number of tap connections. It is revealed that the PPs having taps located

Poly--nomial order	**Represent--ation of Polynomials**	**SNR (dB) at P_e 10^{-3}**	**Location of the second highest tap present in PP**	**Number of Iterat--ion**
5	$g_1(D)$	-5.6	2	11
5	$g_2(D)$	-5.8	3	10
5	$gg_1(D)$	-7.0	3	8
13	$g_5(D)$	-1.0	4	17
13	$g_{10}(D)$	0.6	11	23
13	$g_{11}(D)$	0.5	12	21
13	$gg_5(D)$	-5.0	12	14
13	$gg_6(D)$	-4.5	11	15
23	$g_8(D)$	-3.8	5	15
23	$g_9(D)$	-0.5	17	19
23	$gg_4(D)$	-5.5	17	12

Table 5.3: Comparisons of SNR values in dB versus the location of the second highest tap present in PP as well as the number of iteration, where PPs of the orders 5, 13 and 23 are evolved in producing m- and concatenated sequences

at higher indices yield a wider EXIT tunnel, indicating more rapid convergence for concatenated sequence acquisition. The simulation results of Figs. 5.8 to 5.11 and Table 5.3 also confirm the validity of the EXIT chart model proposed. Owing to these appealing attributes, our iterative RSSE acquisition scheme is capable of performing efficient initial synchronization of both long m- and concatenated sequences with a low AT. Furthermore, the proposed scheme performs better than the family of conventional serial and parallel search-based acquisition techniques. Accordingly, its exploitation may shed light on more efficient receiver design for PN sequence detection in 5G.

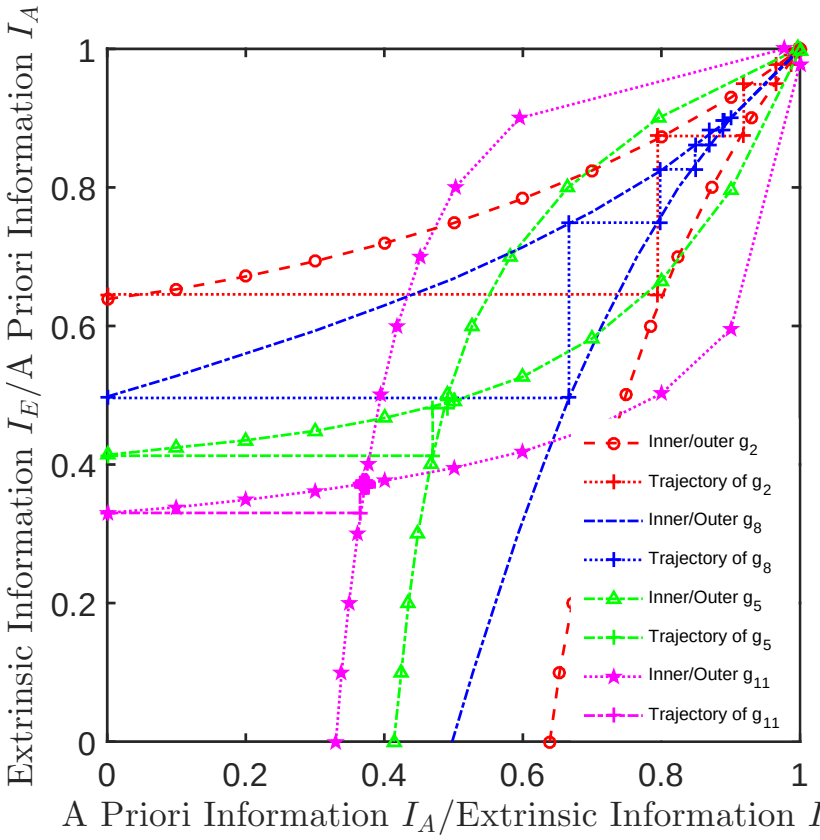


Figure 5.18: EXIT chart for PPs of different orders for transmission over an AWGN channel, at SNR = 0 dB.

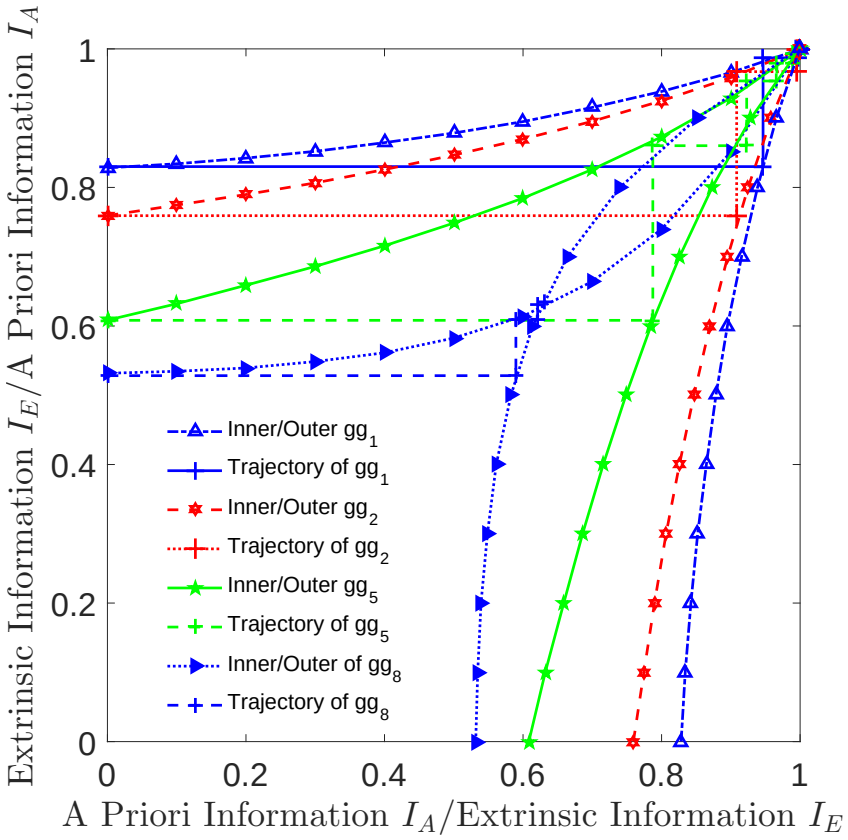


Figure 5.19: EXIT chart for the PPs of gg_1, gg_2, gg_5 and gg_8 for transmission over an AWGN channel at SNR $= 0$ dB.

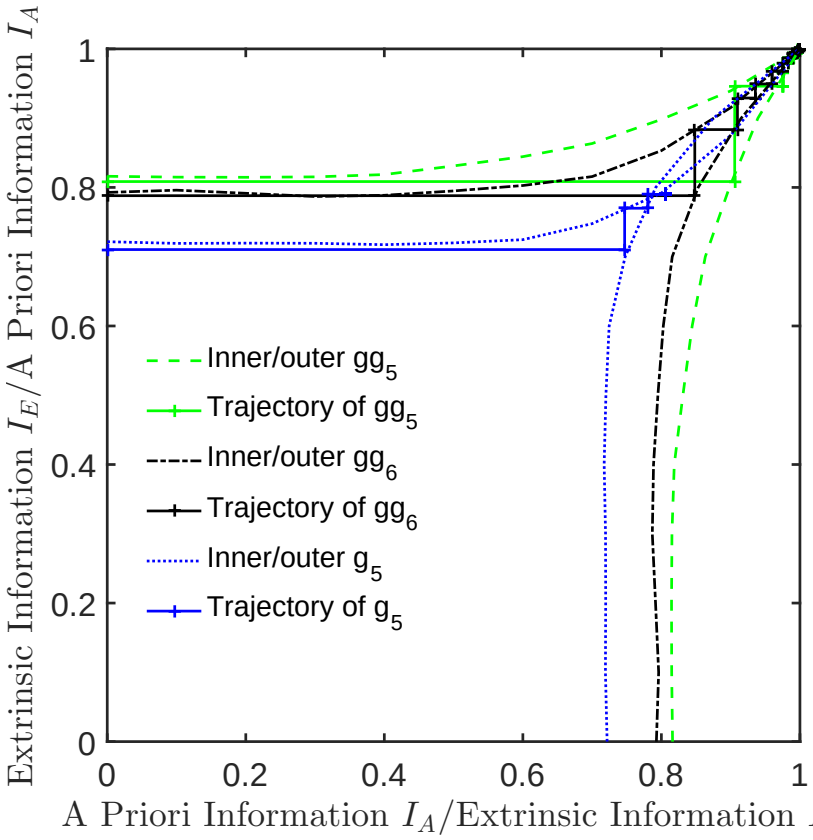


Figure 5.20: EXIT chart for the PPs of order 13 for transmission over an AWGN channel at SNR = 2 dB.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis we have developed *Recursive Soft Sequential Estimation* (RSSE) utilizing a Soft In Soft Out algorithms for both m-sequence acquisition [1] and for *concatenated sequence* acquisition [2]. We have introduced the new concept of EXIT charts in the context of synchronization, which operates without interleavers. Then the best primitive polynomials were found for iterative soft input and soft output m-sequence acquisition based on their Erroneous Loading Probability (P_e) versus Signal to Noise Ratio (SNR) in dB. We have shown that low-order PPs have a lower P_e at a given SNR than their high-order counterparts and we have exploited the EXIT charts for the convergence analysis of m-sequences used for synchronization. Adapting the EXIT charts for operation without using interleavers was a challenge, because the original EXIT charts rely on the employment of long, high-delay interleavers for ensuring that the *extrinsic* information processed by them becomes uncorrelated and obeys the Gaussian distribution. We demonstrate that the m-sequences generated by the lower-order polynomials maximize the mutual information more promptly by processing less received chips with the aid of our RSSE scheme than those, which belong to a higher-order polynomial.

We also designed an iterative initial sequence acquisition technique, for concatenated sequences. This RSSE technique has a linearly increasing complexity with the number of chips in the concatenated sequence. Receiving as few as R consecutive chips of a (2^R-1)-chip sequence is sufficient for the local concatenated-sequence generator of the receiver to synchronize. Hence, this initial synchronization technique is eminently suitable for both long m-sequences and for concatenated sequences. Another key result is the comparison of m- and concatenated sequences regarding their *Acquisition Time* (AT). Again we have shown that low-order PPs achieve better performances than higher-order polynomials for both the m-sequences and the concatenated sequences. When considering PPs having higher number of taps, the

Sequence Utilized	Length of Sequence	Peak to Average Power Ratio (PAPR)
m− Sequence	31	34.34 *dB*
Concatenated Sequence	31	2.89 *dB*
Gold Sequence	33	5.39 *dB*

Table 6.1: Comparison between different sequence regarding PAPR values.

concatenated sequences is capable of achieving in excess of 3 dB SNR gains over m-sequences.

In Chapter 2 we investigated the basic features of the sequences utilized in the synchronization in cellular communication system. We commenced by discussing each sequence and their characteristics. It was observed that Gold and concatenated sequences have better cross correlation properties than the m-sequences, but by contrast, m-sequences have the better auto correlation properties therefore they have been used in almost every generation of cellular systems for synchronization. Table 6.1 illustrates the PAPR of each of the sequences considered. Explicitly high signal peaks would drive the Power Amplifier (PA) into saturation, hence degrading the BER due to the non-linear behavior of the PA.

Chapter 3 deals with the performance analysis of m-sequences in AWGN channels. The best possible PPs were selected by exploiting the iterative SISO process, based on their P_e versus SNR performance. In Table 6.2 the polynomials are grouped together according to their behavior in terms of P_e versus the SNR expressed in dB. Group A contains four polynomials namely $[g_1(D), g_2(D)]$ and $[g_3(D), g_4(D)]$ having orders 5 and 6, respectively. Group B has seven polynomials namely $[g_6(D), g_7(D)]$, $[g_8(D)]$, $[g_{10}(D), g_{11}(D)]$ and $[g_{12}(D), g_{13}(D)]$ having PP orders of 15,23, 29 and 31, respectively. Similarly, in group C we have two polynomials $[g_5(D)]$ and $[g_9(D)]$ belonging to order 13 and 23, respectively. In group D we have three polynomials $[g_{14}(D), g_{15}(D)]$ having the polynomial order 13, whereas $[g_{16}(D)]$ has a polynomial order of 15. Two sets of simulation results are plotted in Figs. 6.1 and 6.2 to quantify the performance of polynomials present in Table 6.2.

Observe from the simulation results of Fig. 6.1, that the PP $g_2(D)$ has a better performance than $g_1(D)$, since its second feedback tap is connected to the third position of the entire feedback tap arrangement (tap3), whereas in $g_1(D)$ the second feedback tap is linked to the second position (tap2), thus the PP generated using a low number of tap connections associated with a higher index has a higher likelihood of providing the higher *extrinsic* information for the SISO acquisition scheme, than that of utilizing a *high number of tap connections*. Similar trends can also be observed

Groups	Polynomials	Representation of polynomials
A	$g_1(D)$, $g_2(D)$	$(2,5)$, $(3,5)$
	$g_3(D)$, $g_4(D)$	$(1,6)$, $(5,6)$
B	$g_6(D)$, $g_7(D)$	$(1,15)$, $(4,15)$
	$g_8(D)$,	$(5,23)$,
	$g_{10}(D)$, $g_{11}(D)$,	$(2,29)$, $(27,29)$
	$g_{12}(D)$, $g_{13}(D)$	$(3,31)$, $(28,31)$
C	$g_5(D)$, $g_9(D)$	$(1,3,4,13)$, $(5,11,17,23)$
D	$g_{14}(D)$	$(2,3,5,6,7,8,9,10,11,13)$
	$g_{15}(D)$	$(1,2,3,4,5,6,8,10,12,13)$
	$g_{16}(D)$	$(2,3,\cdots,15)$

Table 6.2: Primitive polynomials invoked for our RSSE scheme, where g_{16} has consecutive feedback taps ranging from 2 to 15 and the 0 taps of all polynomials were removed for simplicity.

for $g_4(D)$, $g_3(D)$, $g_7(D)$, $g_6(D)$, $g_{11}(D)$, $g_{10}(D)$ and $[g_{13}(D), g_{12}(D)]$, where $g_4(D)$, $g_7(D)$ and $g_{11}(D)$ are all polynomials that have their second tap associated with a higher index compared to their counterparts having the same polynomial order.

Observe in Fig. 6.2, that the SNR performance of the PPs degrades as the number of consecutive feedback taps increases. Group C has $g_5(D)$ and $g_9(D)$, where $g_5(D)$ performs better than $g_9(D)$, because it is a lower-order polynomial. More explicitly, $g_{16}(D)$ has more consecutive feedback taps than the rest of the group, namely 2 to 15 taps, where each feedback-sample is noise contaminated, hence degrading the achievable performance. Upon comparing the performances of PPs having an order of 13, i.e. of $g_{14}(D)$ and $g_{15}(D)$ generated using 10 taps, respectively, it is found that both PPs have two consecutive feedback taps. Hence, more vacant positions exist at higher order feedback indices in $g_{15}(D)$ than in $g_{14}(D)$, therefore $g_{15}(D)$ performs better. Hence, we infer that the detection capability of the receiver is reduced by the presence of the consecutive feedback taps. The receiver has a better chance of detecting the chips in the presence of noise in case of $g_{15}(D)$ as opposed to that of $g_{14}(D)$, since the detection capability of the receiver is degraded proportionally to the number of consecutive feedback taps. We conclude from our simulation results obtained in Figs. 6.1 and 6.2, that the low-order PPs outperform the higher-order PPs, because the detrimental influence of noise imposed on the chips of lower-order PPs ultimately results in less grave error propagation than for their higher-order counterparts.

In Chapter 4 we conceived *a new* EXIT chart tool, where the *correlation of chips inherent in the m-sequences* is exploited. We confirm again that the m-sequences

Groups	***Polynomial Order***	***Erroneous Loading Probability*** P_e	***SNR per Chip*** E_C/N_0 ***dB***
A	5^{th}	10^{-4}	
	$g_1(D)$		*-5.5*
	$g_2(D)$		*-6.0*
	6^{th}		
	$g_3(D)$		*-4.8*
	$g_4(D)$		*-5.2*
B	15^{th}	10^{-4}	
	$g_6(D)$		*-3.8*
	$g_7(D)$		*-4.2*
	23^{rd}		
	$g_8(D)$		*-3.6*
	29^{th}		
	$g_{10}(D)$		*-3.0*
	$g_{11}(D)$		*-3.3*
	31^{st}		
	$g_{12}(D)$		*-2.4*
	$g_{13}(D)$		*-2.8*
C	13^{th}	10^{-4}	
	$g_5(D)$		*0.0*
	23^{rd}		
	$g_9(D)$		*1.0*
D	13^{th}	10^{-4}	
	$g_{14}(D)$		*1.8*
	$g_{15}(D)$		*1.2*
	15^{th}		
	$g_{16}(D)$		*2.0*

Table 6.3: Performance evaluated in terms of Erroneous Loading Probability P_e versus SNR expressed in dB.

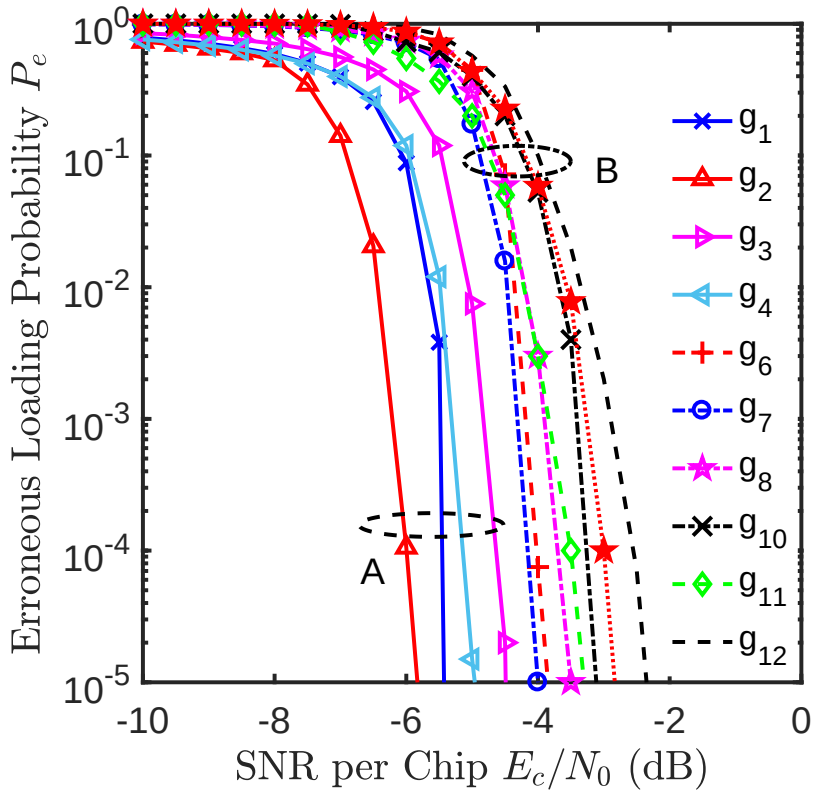


Figure 6.1: Performance comparison between primitive polynomials having three feedback taps, where A and B represent groups of primitive polynomials showing similar performance.

Poly−nomial Order	*Generated Polynomial*	*Total Number of Taps*	*Erroneous Loading Probability* (P_e)	*SNR per Chip* E_c/N_0 *dB*		*Number of Iterations*	
				without AGC	*with AGC*	*without AGC*	*with AGC*
5^{th}	$g_1(D) = 1+ D^2 + D^5$	**3**	10^{-4}	**-3.5**	**-5.5**	**21**	**10**
5^{th}	$g_2(D) = 1+ D + D^2+ D^4 + D^5$	**5**		**0.0**	**-4.0**	**22**	**12**
13^{th}	$g_3(D) = 1+ D + D^3+ D^4 + D^{13}$	**5**		**0.5**	**-3.8**	**26**	**15**

Table 6.4: Comparisons of P_e versus SNR values in dB as well as the number of iteration involved to achieve desire goals.

relying on low-order generator polynomials achieve higher mutual information than high-order polynomials using the same number of RSSE iterations. In Table. 6.4 we compare the polynomials based on their P_e versus SNR and the number of iteration required for the convergence. We observe from our simulation results presented in Fig. 6.3 that the convergence behavior of low-order polynomials is better than that of the high-order polynomials. When comparing PPs of different order, the PPs utilizing a high number of tap connections have a lower likelihood of giving inaccurate extrinsic information for the SISO acquisition technique, than those having less tap

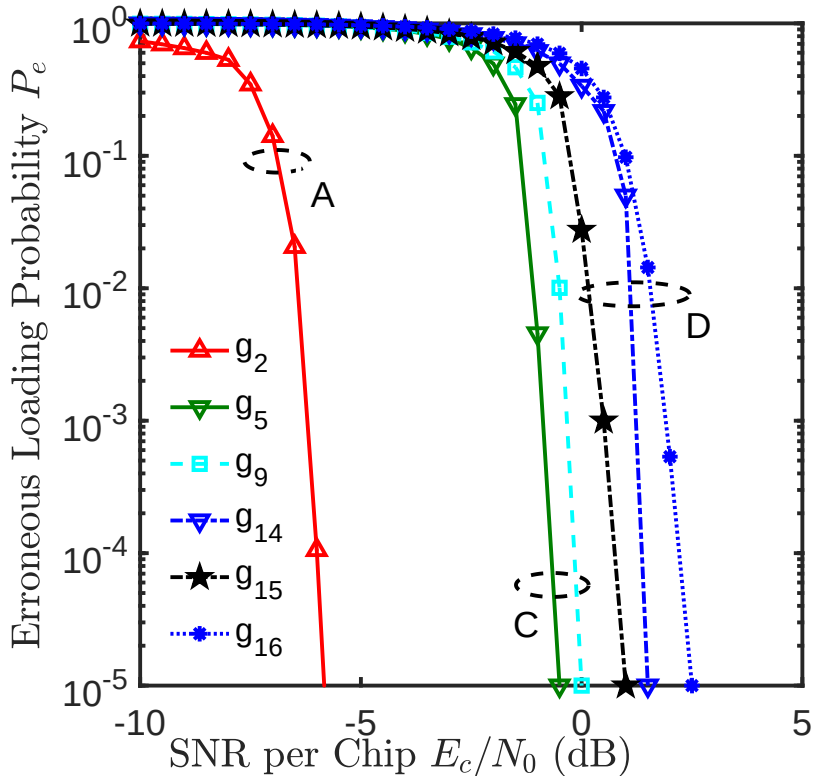


Figure 6.2: Performance comparison between primitive polynomials having a different number of feedback taps, where A, C, and D represent the groups of primitive polynomials having similar behavior.

connections, since at the last stage the average LLR still remains low, in spite of having one or two high LLRs. Since, the extrinsic information is dominated by the minimum of the LLR values of all the feedback branches, the generator polynomial using a low number of feedback branches has a higher probability of providing the higher extrinsic information for the SISO acquisition scheme, than that using a high number of feedback branches. In a nutshell, PPs having a lower number of taps are preferred, because the detrimental influence of noise imposed on their chips results in less grave iteration-induced error propagation than for their counterparts with higher number of taps.

Moreover, Fig. 6.4 demonstrates the *reliability of the chips* of an m-sequence, for transmission over *Nakagami fading channels*. The decision reliability of SISO detection is computed after each chip of a sequence has been received. The solid line in Fig. 6.4 is related to the hard decision based acquisition, which is defined as the absolute value of the channel output associated with the chips transmitted. Observe from Fig. 6.4 the traditional hard decision based model, has a decision reliability spanning from $0-10$, which remains between $0-10$ even if more chips are processed, thus indicates that the polarity of each chip is decided separately. By contrast, in the proposed RSSE acquisition model, the decision reliability increases as more chips are processed by the SISO detector. Hence the RSSE acquisition scheme outperforms the

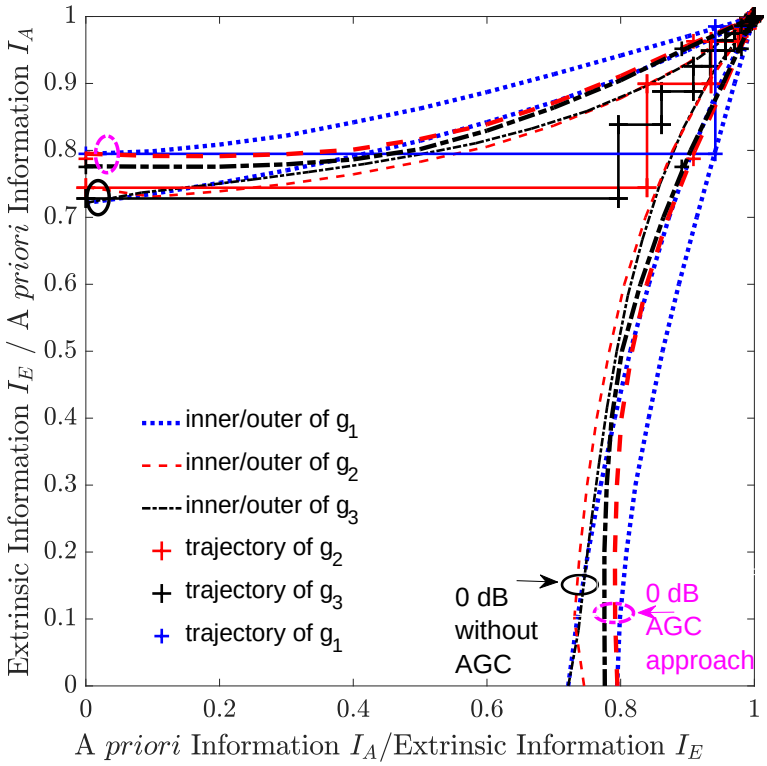


Figure 6.3: EXIT chart for the GPs of $g_1(D) = 1+D^2+D^5$ (blue), $g_2(D) = 1+D+D^2+D^4+D^5$ (red) and $g_3(D) = 1+D+D^3+D^4+D^{13}$ (black) over Nakagami channels, when $m_l = 3.0$ at SNR= 0 dB with/without AGC approach.

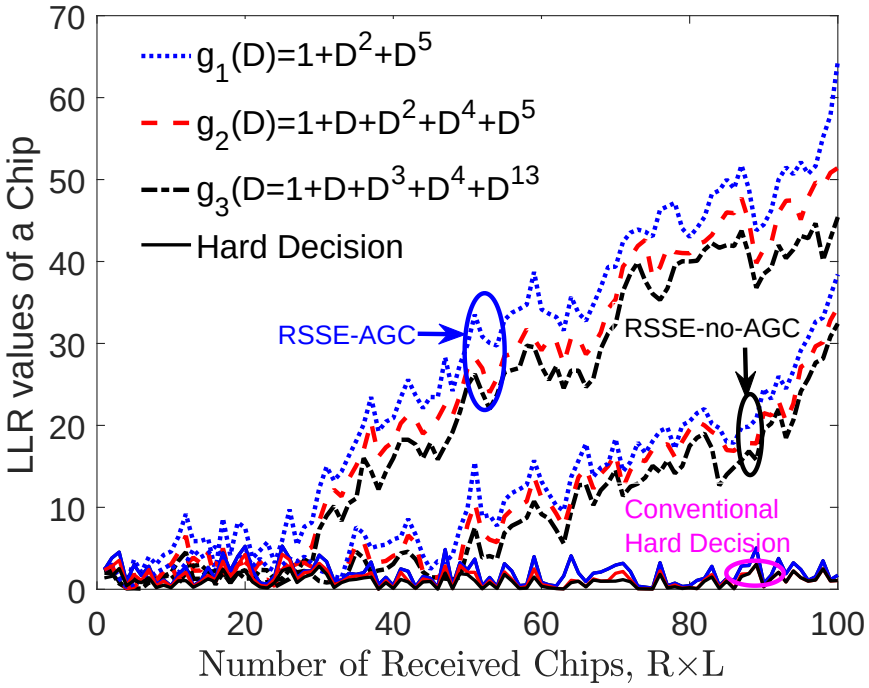


Figure 6.4: The number of received chips versus the decision reliability attained by RSSE SISO decoding, when communicating having a Nakagami Fading channel $m_l = 3.0$ and SNR= 0 dB

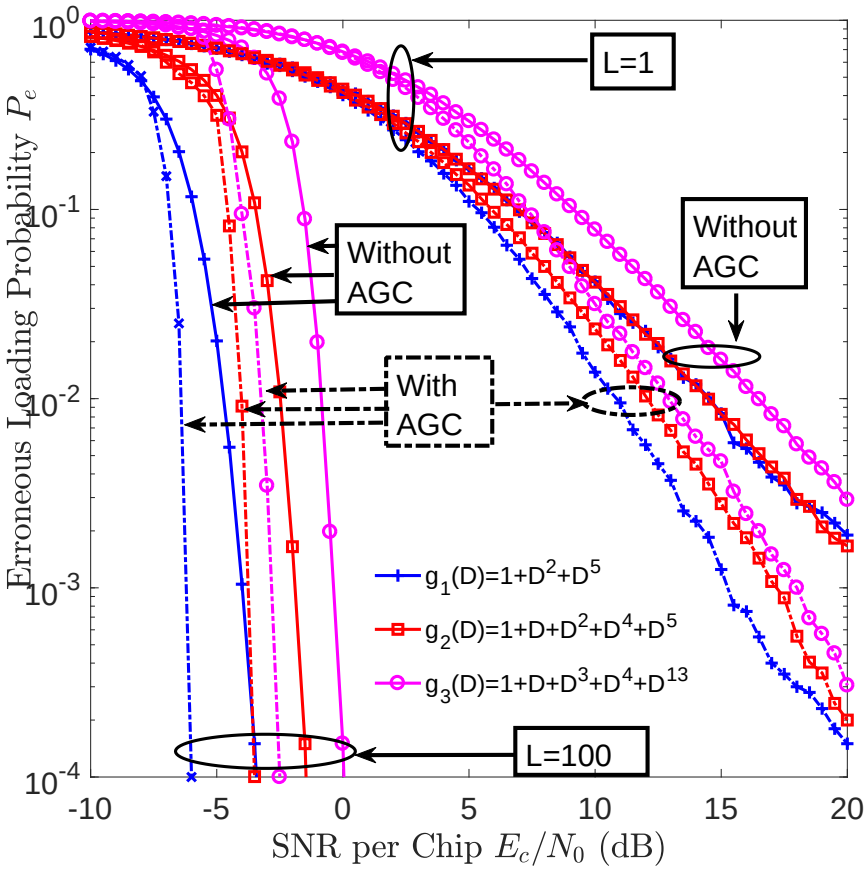


Figure 6.5: Erroneous loading probability P_e, versus the SNR, performance for various numbers of chips invoked into the proposed recursive SISO detector, when transmitting the m-sequence generated by the $g_1(D)$, $g_2(D)$ and $g_3(D)$ polynomials over Nakagami Fading channels when $m_l = 3.0$.

traditional sequential estimation method of [102], since the latter operates without evaluating the *a priori* information given by the previously received chips.

Furthermore, based on in Fig. 6.5 we conclude that invoking an AGC improves the attainable performance as a benefit of its linear gain. Explicitly, the system achieves better performance in less time. To elaborate a little further, the performance depends on the number of taps, on the polynomial order as well as on the linear gain obtained by an AGC. Hence, low order GPs having less taps are superior to those having more taps. In Table 6.5, we compare all the schemes used in Chapter 4. It is observed that when an AGC is utilized, $g_1(D)$ requires a maximum of $L = 10$ iterations to approach unity, whereas $g_2(D)$ requires $L = 12$ iterations and $g_3(D)$ necessitates $L = 15$ iterations. Bycontrast, if no AGC is employed, then $g_1(D)$ requires a maximum of $L = 21$ iterations to approach unity, where as $g_2(D)$ requires $L = 22$ iterations and $g_3(D)$ requires 26 iterations as tabulated in Table. 6.5.

In Chapter 5 the family of *concatenated sequences* was proposed, which were derived from a pair of m-sequences. Again, we employed SISO detection to improve the acquisition performance. We observed that the performance of concatenated

Polynomial Order	*Generated Polynomial*	*Number of Taps*	*Erroneous Loading Probability* (P_e)	*Signal to Noise (SNR)*	*Number of Iteration*
5^{th}	$g_1(D)$	3	10^{-3}	-5.6	11
	$g_2(D)$	3		-5.8	10
	$gg_1(D) = g_1(D) \oplus g_2(D)$	3		-7.0	8
13^{th}	$g_5(D)$	5		-1.0	17
	$g_{10}(D)$	11		0.6	23
	$g_{11}(D)$	11		0.5	21
	$gg_5(D) = g_5(D) \oplus g_{11}(D)$	11		-5.0	14
	$gg_6(D) = g_5(D) \oplus g_{10}(D)$	11		-4.5	15
23^{rd}	$g_8(D)$	3		-3.8	15
	$g_9(D)$	5		-0.5	19
	$gg_4(D) = g_8(D) \oplus g_9(D)$	5		-5.5	12

Table 6.5: Comparisons of SNR values in dB versus the Erroneous Loading Probability P_e as well as the number of iteration.

sequences is *superior* to that of m-sequences, when comparing their P_e versus SNR performance, regardless of the specfic number of iterations as indicated in Table 6.5. We observed that the PPs relying on a low number of tap connections have *a higher probability* of reaching MI = 1 for the SISO acquisition technique, than those utilizing a higher number of tap connections. It is revealed in Table 6.5 and by the simulation results presented in the Chapter 5 that the PPs of the same order containing similar number of taps, a wider open EXIT tunnel and better but having higher tap-indices exhibit.

6.2 Future Work

Apart from the aforementioned RSSE algorithms, which we designed in the context of the acquisition of m- and concatenated sequences, similar arrangements could be designed also for *Gold* and *Golay* sequences. However, the received signal energy is typically distributed across hundreds or thousands of chips, hence the SNR per chip is extremely low. Moreover, hard decisions are typically unreliable for the estimation of R consecutive chips using a chip-by-chip-based approach [53, 92, 152]. Hence, Kilgus devised a majority logic aided decoder for m-sequence acquisition [93]. As a further evolution of this kind of technique, Ward and Yiu [123] proposed the concept

of recursive sequential estimation assisted acquisition. The basic principle of these two schemes was to adopt the hard decision approach relying on coherent detection. However, adopting any hard decision based coherent approach becomes unrealistic, since the SNR is usually very low prior to despreading [16, 59]. For this reason, we advocate the recursive Soft Input Soft Output (SISO) detection principle, which has its roots in the classic turbo channel decoding philosophy [54, 92, 141]. Therefore, we have in our possession a variety of algorithms for code acquisition. Our future work will be focused on the following issues:

(a) Design further improved iterative sequential estimation aided receivers. This design method will target Gold, Golay and Zadoff Chu sequence detection for transmission over AWGN/ Rayleigh/ Nakagami-m fading channels. The particular emphasis will be on Rayleigh and Ricean channels, which can also be matched by the Nakagami channel model. Our aim is to conceive a receiver exhibiting a good performance in diverse communication channels. Furthermore, differential coherent schemes may also be designed for Gold, Golay and Zadoff Chu sequences transmitted over Nakagami-m fading channels.

(b) Investigate the detection performance improvements for transmission over dispersive multipath channels, in the context of both diversity-aided receivers, and of the classic majority voting method, as well as of maximum ratio combining, equal-gain and selection combining.

(c) We can employ Machine learning to improve the predication of LLRs which are computed by the SCDUs. Thus, will enhance the system performance.

(d) Finally we will conceive initial acquisition schemes for millimeter-Wave (mm-Wave) systems relying on Multi In Multi Out (MIMO)-aided multicarrier transceivers. mm-Wave does not propagate over long distance because of high path loss we need to do beam forming aided directional transmission, which plays a significant role in mm-Wave. This leads to investigate initial synchronization and conduct performance comparison between stand-a-lone and microwave overlaid millimetre communication in-terms of mean synchronization time.

(e) We will focus on implementing new iterative sequential estimation receiver, targeting m-sequence and Gold-sequence detection over mm-Wave channel having high Signal to Interference Noise Ratio (SINR).

(f) We aim to implement Match Filtering (MF) schemes which have effective SINR. By employing MF aided approach, we need to consider correct detection/ missed detection and false detection probability for optimal synchronization. Based on it, we will also investigate mean frame detection time analysis and its features in more detail. Our further objective will be to derive formulas for these probabilities and mean frame detection time.

Bibliography

[1] A. Ahmed, P. Botsinis, S. Won, L. L. Yang, and L. Hanzo, "EXIT chart aided convergence analysis of recursive soft m-sequence estimation in Nakagami-m fading channels," *IEEE Transactions on Vehicular Technology*, vol. 67, no. 5, pp. 4655–4660, January 2018.

[2] A. Ahmed, P. Botsinis, S. Won, L. Yang, and L. Hanzo, "Primitive polynomials for iterative recursive soft sequential acquisition of concatenated sequences," *IEEE Access*, vol. 7, pp. 13 882–13 900, 2019.

[3] A. Carlson, P. B.Crilly, and J. C. Rutledge, "Communication systems an introduction to signals and noise in electrical communication," *McGraw Hill*, 2002.

[4] M. Schwartz, "Mobile wireless communications," *Cambridge University Press*, 2005.

[5] C. Östberg, H. Stattin, and B. Lindoff, "Mobile terminals and methods for performing fast initial frequency scans and cell searches," *US Patent 7,013,140*, march 2006.

[6] J.-C. Lin, "Synchronization requirements for 5G: An overview of standards and specifications for cellular networks," *IEEE Vehicular Technology Magazine*, vol. 13, no. 3, pp. 91–99, 2018.

[7] K. K. Chawla and D. V. Sarwate, "Parallel acquisition of PN sequences in DS/SS systems," *IEEE Transactions on Communications*, vol. 42, no. 5, pp. 2155–2164, May 1994.

[8] H. Li, L. Han, R. Duan, and G. M. Garner, "Analysis of the synchronization requirements of 5G and corresponding solutions," *IEEE Communications Standards Magazine*, vol. 1, no. 1, pp. 52–58, March 2017.

[9] L. Hanzo, H. Haas, S. Imre, D. O'Brien, M. Rupp, and L. Gyongyosi, "Wireless myths, realities, and futures: from 3G / 4G to optical and quantum wireless,"

Proceedings of the IEEE, vol. 100, no. Special Centennial Issue, pp. 1853–1888, April 2012.

[10] E. Bastug, M. Bennis, and M. Debbah, "Living on the edge: The role of proactive caching in 5G wireless networks," *IEEE Communications Magazine*, vol. 52, no. 8, pp. 82–89, Aug 2014.

[11] S. Parkvall, E. Englund, M. Lundevall, and J. Torsner, "Evolving 3G mobile systems: broadband and broadcast services in WCDMA," *IEEE Communications Magazine*, vol. 44, no. 2, pp. 30–36, Feb 2006.

[12] G. Wunder, P. Jung, M. Kasparick, T. Wild, F. Schaich, Y. Chen, S. Ten Brink, I. Gaspar, N. Michailow, A. Festag *et al.*, "5GNOW: non-orthogonal, asynchronous waveforms for future mobile applications." *IEEE Communications Magazine*, vol. 52, no. 2, pp. 97–105, 2014.

[13] A.Viterbi, "CDMA: Principles of spread spectrum communication," *Addison Wesley*, 1995.

[14] A. Bensky, "Wireless positioning technologies and applications," *Artech House*, 2016.

[15] R. Steele and L. Hanzo, "Mobile radio communications: Second and third generation cellular and WATM systems: 2nd," *IEEE Press-John Wiley*, 1999.

[16] L. Hanzo, L. L. Yang, E. Kuan, and K. Yen, "Single-and multi-carrier DS-CDMA: multi-user detection, space-time spreading, synchronisation, standards and networking," *John Wiley & Sons.*, 2003.

[17] L. Lee and J. Chiu, "An improved sequential estimation scheme for PN acquisition," *IEEE Transactions on Communications*, vol. 36, no. 10, pp. 1182–1184, Oct 1988.

[18] C. E. Wheatley III and E. G. Tiedemann Jr, "Mobile station assisted timing synchronization in CDMA communication system," *US Patent 6,307,840*, Oct 2001.

[19] J. G. Proakis, M. Salehi, N. Zhou, and X. Li, "Communication systems engineering," *Prentice-hall Englewood Cliffs*, vol. 1, 1994.

[20] S. Hara and R. Prasad, "Multicarrier techniques for 4G mobile communications," *Artech House*, 2003.

[21] B. P. Lathi, "Modern digital and analog communication systems 3e osece," *Oxford university press*, 1998.

[22] J. G. Proakis, "Digital communication," *McGraw Hill*, vol. 4^{th} Edition, 2001.

[23] G. Stuber, "Principle of mobile communication," *Kluwer Boston MA*, 2001.

[24] R. Prasad, "CDMA for wireless personal communications," *Artech Hall*, 1996.

[25] M. Peng and W. Wang, "Technologies and standards for TD-SCDMA evolutions to IMT-advanced," *IEEE Communications Magazine*, vol. 47, no. 12, pp. 50–58, Dec 2009.

[26] L. Harte, "CDMA IS-95 for cellular and PCs:technology, applications and resource guide," *McGraw Hill*, 1999.

[27] Y. Tsai, G. Zhang, D. Grieco, and F. Ozluturk, "Cell search in 3GPP long term evolution systems," *IEEE Vehicular Technology Magazine*, vol. 2, no. 2, pp. 23–29, June 2007.

[28] J. S. Blogh and L. L. Hanzo, "Third-generation systems and intelligent wireless networking: smart antennas and adaptive modulation," *John Wiley & Sons*, 2002.

[29] J. Liberti and T. Rappaport, "Smart antennas for wireless communications: IS-95 and third generation CDMA applications," *Prentice Hall*, 1999.

[30] U. Madhow and M. B. Pursley, "Acquisition in direct-sequence spread-spectrum communication networks: An asymptotic analysis," *IEEE Transactions on Information Theory*, vol. 39, no. 3, 1993.

[31] S.Willenegeger, "CDMA 2000 physical layer: An overview," *Journal of Communications and Networks*, vol. 2, no. 1, 2000.

[32] M. Weiss, "Telecom requirements for time and frequency synchronization," *National Institute of Standards and Technology (NIST), USA,[Online]: www. gps. gov/cgsic/meetings/2012/weiss1. pdf*, 2012.

[33] "TS 25.213 v(12.0.0): Spreading and modulation (FDD)," *3GPP*, pp. 1–50, 2014.

[34] G. C.S0010-B, "Recommended minimum performance standards for CDMA-2000 spread spectrum systems," *3GPP2 C.S0010-B*, 2004.

[35] M. K. Simon and M.-S. Alouini, "Digital communication over fading channels," *John Wiley & Sons*, vol. 95, 2005.

[36] G. C.S0002-C, "Physical layer standards for CDMA-2000 spread spectrum systems," *3GPP2 C.S0002-C*, 2004.

[37] N. H. Kim and Y. B. Park, "Apparatus for performing initial synchronization and frame synchronization in mobile communications system and method thereof," *US Patent 7,894,554*, Feb 2011.

[38] G. Giunta, A. Neri, and L. Vandendorpe, "Initial code synchronization of W-CDMA mobile systems exploiting local phase coherence and pisarenko estimation," *IEEE Transactions on Communications*, vol. 53, no. 1, pp. 48–52, 2005.

[39] E. Dahlman, P. Beming, J. Knutsson, F. Ovesjo, M. Persson, and C. Roobol, "WCDMA-the radio interface for future mobile multimedia communications," *IEEE Transactions on Vehicular Technology*, vol. 47, no. 4, pp. 1105–1118, 1998.

[40] D. Xenakis, N. Passas, L. Merakos, and C. Verikoukis, "Mobility management for femtocells in LTE-Advanced: Key aspects and survey of handover decision algorithms," *IEEE Communications Surveys Tutorials*, vol. 16, no. 1, pp. 64–91, First 2014.

[41] K. Gomez, L. Goratti, T. Rasheed, and L. Reynaud, "Enabling disaster-resilient 4G mobile communication networks," *IEEE Communications Magazine*, vol. 52, no. 12, pp. 66–73, December 2014.

[42] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. Soong, and J. C. Zhang, "What will 5G be?" *IEEE Journal on selected areas in communications*, vol. 32, no. 6, pp. 1065–1082, 2014.

[43] C.-X. Wang, F. Haider, X. Gao, X.-H. You, Y. Yang, D. Yuan, H. M. Aggoune, H. Haas, S. Fletcher, and E. Hepsaydir, "Cellular architecture and key technologies for 5G wireless communication networks," *IEEE communications magazine*, vol. 52, no. 2, pp. 122–130, 2014.

[44] A. Osseiran, F. Boccardi, V. Braun, K. Kusume, P. Marsch, M. Maternia, O. Queseth, M. Schellmann, H. Schotten, H. Taoka *et al.*, "Scenarios for 5G mobile and wireless communications: the vision of the metis project," *IEEE communications magazine*, vol. 52, no. 5, pp. 26–35, 2014.

[45] N. Bhushan, J. Li, D. Malladi, R. Gilmore, D. Brenner, A. Damnjanovic, R. T. Sukhavasi, C. Patel, and S. Geirhofer, "Network densification: the dominant theme for wireless evolution into 5G," *IEEE Communications Magazine*, vol. 52, no. 2, pp. 82–89, 2014.

[46] A. F. Myles, D. S. Goodall, and A. C. Lam, "Method and apparatus for clock synchronization in a wireless network," *US Patent 7,151,945*, Dec. 19 2006.

[47] Y. F. Chang, C. Chen, and H. Zhou, "Smart phone for mobile commerce," *Computer Standards & Interfaces*, vol. 31, no. 4, pp. 740–747, 2009.

[48] A. Sinitsyn, "A synchronization framework for personal mobile servers," *IEEE Proceedings of the Second Annual Conference on Pervasive Computing and Communications Workshops, 2004.*, pp. 208–212, 2004.

[49] S. Mumtaz, K. M. S. Huq, and J. Rodriguez, "Direct mobile-to-mobile communication: Paradigm for 5G," *IEEE Wireless Communications*, vol. 21, no. 5, pp. 14–23, 2014.

[50] V. K. Gary, "IS 95 CDMA and CDMA 2000 cellular/ PCS systems implementation," *Prentice Hall*, 1999.

[51] L. Korowajczuk, B. Xavier, and de Souza Abreu, "Designing CDMA 2000 systems," *John Willey & Sons*, 2005.

[52] L. L. Yang and L. Hanzo, "Serial acquisition of DS-CDMA signals in multipath fading mobile channels," *IEEE Transactions on Vehicular Technology*, vol. 50, no. 2, pp. 617–628, March 2001.

[53] S. Won and L. Hanzo, "Synchronization of noncoherent MIMO systems: Synchronization issues," *IEEE Vehicular Technology Magazine*, vol. 7, no. 4, pp. 95–103, December 2012.

[54] X. Shen, Y. Liao, X. Dai, M. Zhao, K. Liu, and D. Wang, "Joint channel estimation and decoding design for 5G-enabled V2V channel," *China Communications*, vol. 15, no. 7, pp. 39–46, July 2018.

[55] K. M. Chugg and M. Zhu, "A new approach to rapid PN code acquisition using iterative message passing techniques," *IEEE Journal on Selected Areas in Communications*, vol. 23, no. 5, pp. 884–897, May 2005.

[56] G. E. Corazza, C. Caini, A. Vanelli-Coralli, and A. Polydoros, "DS-CDMA code acquisition in the presence of correlated fading-Part I: Theoretical aspects," *IEEE Transactions on Communications*, vol. 52, no. 7, pp. 1160–1168, 2004.

[57] C. Caini, G. E. Corazza, and A. Vanelli-Coralli, "DS-CDMA code acquisition in the presence of correlated fading-part II: application to cellular networks," *IEEE Transactions on Communications*, vol. 52, no. 8, pp. 1397–1407, 2004.

[58] L. Hanzo, M. Münster, B. Choi, and T. Keller, "OFDM and MC-CDMA for broadband multi-user communications, WLANs and broadcasting," 2005.

[59] K.-B. Song and C. Pandana, "Low complexity sequence estimator for general packet radio service GPRS system," *US Patent App. 10/050,813*, vol. 14, August 2018.

[60] H. Meyr, M. Moeneclaey, and S. Fechtel, *Digital communication receivers: synchronization, channel estimation, and signal processing.* John Wiley & Sons, Inc., 1997.

[61] A. Zatsman, "Synchronization signal detection and phase estimation apparatus and method," Nov. 7 2000.

[62] N. Suehiro, "A signal design without co-channel interference for approximately synchronized cdma systems," *IEEE Journal on selected areas in communications*, vol. 12, no. 5, pp. 837–841, 1994.

[63] R. C. Dixon, "Spread spectrum systems: with commercial applications," *Wiley New York*, vol. 994, 1994.

[64] D. J. Goodman *et al.*, "Trends in cellular and cordless communications," *IEEE Communications Magazine*, vol. 29, no. 6, pp. 31–40, 1991.

[65] F. Ling, "Synchronization in digital communication systems," *Cambridge University Press*, 2017.

[66] S. C. Guido De Angelis, Giuseppe Baruffa, "Parallel PN code acquisition for wireless positioning in CDMA handsets," *IEEE Advanced Satellite Multimedia Systems and the Signal Processing for Space Communication Conference*, 2010.

[67] S.Won and L. Hanzo, "Analysis of serial-search-based code acquisition in the multiple-transmit/multiple-receive-antenna-aided DS-CDMA downlink," *IEEE Transactions on Vehicular Technology*, vol. 57, no. 2, pp. 1032–1039, March 2008.

[68] C. Grell, J. Guralnick, I. J. Rothmuller, C. Bennett, and M. Theiss-Aird, "Method and apparatus for determining location of a subscriber device in a wireless cellular communications system," *US Patent 5,815,538*, Sep 1998.

[69] K. S. Gilhousen, I. M. Jacobs, R. Padovani, L. A. Weaver Jr, C. E. Wheatley III, and A. J. Viterbi, "System and method for generating signal waveforms in a CDMA cellular telephone system," April 1992.

[70] J. H. Iinatti, "On the threshold setting principles in code acquisition of DS-SS signals," *IEEE Journal on selected Areas in Communications*, vol. 18, no. 1, pp. 62–72, 2000.

[71] M. Vayrynen, "Mobile station using synchronization word order information for improved channel acquisition," *US Patent 6,256,304*, Jul. 3 2001.

[72] S. Hosur, S. Sriram, T. M. Schmidl, and A. G. Dabak, "Acquisition of an unevenly spaced synchronization channel in a wireless communication system," *US Patent 6,834,046*, Dec. 21 2004.

[73] T. Ojanpera and R. Prasad, "WCDMA: Towards IP mobility and mobile internet," *Artech House*, March 2001.

[74] E. A. Yavuz, "WCDMAand CDMA 2000: The radio interfaces for future mobile multimedia communication-Part II," 2001.

[75] J. Schiller, "Mobile communication," *Pearson Education*, vol. 2, 2009.

[76] P. J. A. Nyström, K. Jamal, R. Esmailzadeh, and Y.-P. E. Wang, "Cell searching in a CDMA communications system," *US Patent 6,185,244*, Feb 2001.

[77] K.-M. Ok, J.-K. Kim, C.-M. Lim, S.-H. Hur, and D.-R. Ryu, "Cell search apparatus and method in a mobile communication system," *US Patent 7,532,590*, May 12 2009.

[78] U. Schmid, "Synchronized universal time coordinated for distributed real-time systems," *Control Engineering Practice*, vol. 3, no. 6, pp. 877–884, 1995.

[79] K. Schossmaier, U. Schmid, M. Horauer, and D. Loy, "Specification and implementation of the universal time coordinated synchronization unit (UTCSU)," *Real-Time Systems*, vol. 12, no. 3, pp. 295–327, 1997.

[80] P.-h. Wee, "Pilot PN offset assigning method for digital mobile telecommunications system," *US Patent 6,272,122*, Aug 2001.

[81] X. D. Lin and K. H. Chang, "Optimal PN sequence design for quasisynchronous CDMA communication systems," *IEEE Transactions on Communications*, vol. 45, no. 2, pp. 221–226, 1997.

[82] C. D. Near and M. U. Uyar, "Method for synchronizing interconnected digital equipment," *US Patent 5,068,877*, Nov. 26 1991.

[83] D. Bharadia and S. Katti, "Full duplex MIMO radios," 11^{th} *USENIX Symposium on Networked Systems Design and Implementation NSDI 14*, pp. 359–372, 2014.

[84] D. Tse and P. Viswanath, *Fundamentals of wireless communication*. Cambridge university press, 2005.

[85] K. Sohrabi, J. Gao, V. Ailawadhi, and G. J. Pottie, "Protocols for self-organization of a wireless sensor network," *IEEE personal communications*, vol. 7, no. 5, pp. 16–27, 2000.

[86] R. Etkin, A. Parekh, and D. Tse, "Spectrum sharing for unlicensed bands," *IEEE Journal on selected areas in communications*, vol. 25, no. 3, pp. 517–528, 2007.

[87] I. F. Akyildiz, W.-Y. Lee, M. C. Vuran, and S. Mohanty, "Next generation/dynamic spectrum access/cognitive radio wireless networks: A survey," *Computer networks*, vol. 50, no. 13, pp. 2127–2159, 2006.

[88] Q. Zhao and B. M. Sadler, "A survey of dynamic spectrum access," *IEEE signal processing magazine*, vol. 24, no. 3, pp. 79–89, 2007.

[89] T. Yucek and H. Arslan, "A survey of spectrum sensing algorithms for cognitive radio applications," *IEEE communications surveys & tutorials*, vol. 11, no. 1, pp. 116–130, 2009.

[90] S. Chen, S. Sun, Y. Wang, G. Xiao, and R. Tamrakar, "A comprehensive survey of TDD-based mobile communication systems from TD-SCDMA 3G to TD-LTE(A) 4G and 5G directions," *China Communications*, vol. 12, no. 2, pp. 40–60, Feb 2015.

[91] K. S. Kim, S. W. Kim, Y. S. Cho, and J. Y. Ahn, "Synchronization and cell-search technique using preamble for OFDM cellular systems," *IEEE Transactions on Vehicular Technology*, vol. 56, no. 6, pp. 3469–3485, Nov 2007.

[92] L. L. Yang and L. Hanzo, "Acquisition of m-sequences using recursive soft sequential estimation," *IEEE Transactions on Communications*, vol. 52, no. 2, pp. 199–204, February 2004.

[93] C. Kilgus, "Pseudonoise code acquisition using majority logic decoding," *IEEE Transactions on Communications*, vol. 21, no. 6, pp. 772–774, June 1973.

[94] M. D. Pollman and T. O. Grosch, "Providing global positioning system (GPS) timing signals to remote cellular base stations," *US Patent 7,558,356*, Jul. 7 2009.

[95] L. C. Yun, C. H. Barratt, and C. Uhlik, "Adaptive method for channel assignment in a cellular communication system," *US Patent 6,047,189*, Apr. 4 2000.

[96] B. G. Lee and B. H. Kim, "High-speed cell searching apparatus and method for communication system," *US Patent 6,822,999*, Nov. 23 2004.

[97] Intel Corporation, "R1-1710501 NR PSS and SSS design," *P.R China Inter Corporation Qingdao*, pp. 1–6, June 2017.

[98] Intel Corporation, "R1-162386: Numerology for new radio interface," *Intel Corporation*, pp. 1–6, April 2016.

[99] 3GPP, "TR 38.802 v(2.0.0): study on new radio NR access technology; physical layer aspects," *3GPP*, pp. 1–134, September 2017.

[100] 3GPP, "TS 38.211 v(15.0.0): NR; physical channels and modulation," *3GPP*, pp. 1–73, April 2017.

[101] 3GPP, "TS 38.213 v(15.0.0): NR; physical layer procedures for control," *3GPP*, pp. 1–56, April 2018.

[102] R. Ward, "Acquisition of pseudonoise signals by sequential estimation," *IEEE Transactions on Communication Technology*, vol. 13, no. 4, pp. 475–483, December 1965.

[103] D. Sarwate and M. Pursley, "Crosscorrelation properties of pseudorandom and related sequences," *Proceedings of IEEE*, 1980.

[104] R. E. Ziemer and R. L. Peterson, "Digital communication and spread spectrum systems," "New York Macmillan, 1985.

[105] L. L.Yang and L. Hanzo, "Differential acquisition of m-sequences using recursive soft sequential estimation," *IEEE Transactions on Wireless Communications*, vol. 4, no. 1, pp. 128–136, Jan 2005.

[106] B. Sklar, "Digital communications: Fundamentals and applications," *Prentice-hall Englewood Cliffs*, 1988.

[107] R. Gold, "Optimal binary sequences for spread spectrum multiplexing," *IEEE Transactions on Information Theory*, vol. 13, no. 4, pp. 619–621, October 1967.

[108] S. M. Killough, M. M. Olama, and T. Kuruganti, "Gold code-phase-shift keying: A power and bandwidth efficient communication scheme for smart buildings," *IEEE International Workshop Technical Committee on Communications Quality and Reliability (CQR)*, pp. 1–6, August 2018.

[109] B. M. Popvic', "Spreading sequences for multi-carrier CDMA systems," *IET*, 1997.

[110] R. Krüger and H. Mellein, "Introduction and measurement," *ROHDE & SCHWARZ*, 2008.

[111] I. T. Stefania Sesia and M. Baker, "LTE the UMTS long term evolution from theory to practice," *John Willey & Sons*, 2009.

[112] S. Maskara and J. Das, "Concatenated sequences for spread spectrum systems," *IEEE Transactions on Aerospace and Electronic Systems*, no. 3, pp. 342–350, 1981.

[113] S. Spinsante and E. Gambi, "De Bruijn binary sequences and spread spectrum applications: A marriage possible?" *IEEE Aerospace and Electronic Systems Magazine*, vol. 28, no. 11, pp. 28–39, 2013.

[114] M.-H. Fong, V. K. Bhargava, and Q. Wang, "Concatenated orthogonal / PN spreading sequences and their application to cellular DS-CDMA systems with integrated traffic," *IEEE Journal on selected areas in communications*, vol. 14, no. 3, pp. 547–558, 1996.

[115] H. Elders-Boli, A. Busboom, and H. Schotten, "Fast acquisition in DS-CDMA using concatenated spreading sequences," *IEEE First Signal Processing Workshop on Signal Processing Advances in Wireless Communications*, pp. 373–376, 1997.

[116] Q. Zhang, A. Liu, Y. Zhang, and X. Liang, "Practical design and decoding of parallel concatenated structure for systematic polar codes." *IEEE Transactions on Communications*, vol. 64, no. 2, pp. 456–466, February 2016.

[117] B. Azimdoost, H. R. Sadjadpour, and J. J. Garcia-Luna-Aceves, "Capacity of Wireless Networks with Social Behavior," *IEEE Transactions on Wireless Communications*, vol. 12, no. 1, pp. 60–69, January 2013.

[118] L. Zegers, "Common bandwidth tranmission of information signals and pseudonoise synchronization waveforms," *IEEE Transactions on Communication Technology*, vol. 16, no. 6, pp. 796–807, 1968.

[119] J. K. Holmes and C. C. Chen, "Acquisition time performance of PN spread-spectrum systems," *IEEE Transactions on Communications Technology*, vol. Com-25, no. 4, pp. 778–784, August 1977.

[120] L. L. Yang, "Multicarrier communication," *John Wiley & Sons*, 2009.

[121] S. Won and L. Hanzo, "Initial synchronisation of wideband and UWB direct sequence systems: Single- and multiple-antenna aided solutions," *IEEE Communications Surveys Tutorials*, vol. 14, no. 1, pp. 87–108, November 2012.

[122] S. Won and L. Hanzo, "Synchronization issues in relay-aided cooperative MIMO networks," *IEEE Wireless Communications*, vol. 21, no. 5, pp. 41–51, October 2014.

[123] R. B. Ward and K. Yiu, "Acquisition of pseudonoise signals by recursion-aided sequential estimation," *IEEE Transactions on Communications*, vol. 25, no. 8, pp. 784–794, August 1977.

[124] C. Berrou and A. Glavieux, "Near optimum error correcting coding and decoding: Turbo-codes," *IEEE Transactions on communications*, vol. 44, no. 10, pp. 1261–1271, October 1996.

[125] J. Kliewer, S. X. Ng, and L. Hanzo, "Efficient computation of EXIT functions for nonbinary iterative decoding," *IEEE Transactions on Communications*, vol. 54, no. 12, pp. 2133–2136, 2006.

[126] J. Ponnusamy and M. Srinath, "Acquisition of pseudonoise codes in FH systems," *IEEE Transactions on Aerospace and Electronic Systems*, no. 3, pp. 335–341, 1981.

[127] A. Polydoros and M. Simon, "Genralized serial search code acquisition: The equivalent circular state diagram approach," *IEEE Transactions on Communications*, vol. 32, no. 12, pp. 1260–1268, December 1984.

[128] V. M. Jovanovic, "Analysis of strategies for serial-search spread-spectrum code acquisition-direct approach," *IEEE Transactions on Communications*, vol. 36, no. 11, pp. 1208–1220, Nov 1988.

[129] R. T. Barghouthi and G. L. Stüber, "Rapid sequence acquisition for DS/CDMA systems employing Kasami sequences," *IEEE Transactions on Communications*, vol. 42, no. 234, pp. 1957–1968, 1994.

[130] S. G. Glisic, T. J. Poutanen, W. W. Wu, G. V. Petrovic, and Z. Stefanovic, "New PN code acquisition scheme for CDMA networks with low signal-to-noise ratios," *IEEE Transactions on Communications*, vol. 47, no. 2, pp. 300–310, Feb 1999.

[131] L.-L. Yang and L. Hanzo, "Iterative soft sequential estimation assisted acquisition of m-sequences," *IEEE IET Electronics Letters*, vol. 38, no. 24, pp. 1550–1551, Nov 2002.

[132] J. H. Lee, I. Song, S. R. Park, and J. Lee, "Rapid acquisition of PN sequences with a new decision logic," *IEEE Transactions on Vehicular Technology*, vol. 53, no. 1, pp. 49–60, Jan 2004.

[133] O. W. Yeung and K. M. Chugg, "An iterative algorithm and low complexity hardware architecture for fast acquisition of long PN codes in UWB systems," *Journal of VLSI signal processing systems for signal, image and video technology*, vol. 43, no. 1, pp. 25–42, Apr 2006.

[134] S. Won and L. Hanzo, "Non-coherent code acquisition in the multiple transmit/multiple receive antenna aided single-and multi-carrier DS-CDMA downlink," *IEEE Transactions on Wireless Communications*, vol. 6, no. 11, pp. 3864–3869, 2007.

[135] A. Goldsmith, "Wireless communications," *Cambridge university press*, 2005.

[136] T. Keller and L. Hanzo, "Orthogonal frequency division multiplex synchronisation techniques for wireless local area networks," *Seventh IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, vol. 3, pp. 963–967 vol.3, Oct 1996.

[137] T. Schmidl and D. Cox, "Robust frequency and timing synchronization for OFDM," *IEEE Transactions on Communications*, vol. 45, no. 12, pp. 1613–1621, Dec 1997.

[138] J.-C. Guey, "The design and detection of signature sequences in time-frequency selective channel," *IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, pp. 1–5, Sept 2008.

[139] S. Rangan, T. Rappaport, and E. Erkip, "Millimeter-wave cellular wireless networks: Potentials and challenges," *Proceedings of the IEEE*, vol. 102, no. 3, pp. 366–385, March 2014.

[140] R. M.K Simon, J.M.Omura and B. Levitt, "Spread spectrum communication," *IEEE communication Magazine,vol 35,pp 102-109*, 1994.

[141] W. Zhao, Q. Guo, Y. Yu, J. Xi, and J. Tong, "Iterative nonlinearity mitigation and decoding for led communications," *IEEE Photonics Technology Letters*, pp. 1731–1734, August 2018.

[142] J. Hagenauer, "The EXIT chart - introduction to extrinsic information transfer in iterative processing," *IEEE European Signal Processing Conference*, pp. 1541–1548, 2004.

[143] E. A. Lee and D. G. Messerschmitt, "Digital communication," *Springer Science & Business Media*, 2012.

[144] J. Hagenauer, E. Offer, and L. Papke, "Iterative decoding of binary block and convolutional codes," *IEEE Transactions on Information Theory*, vol. 42, no. 2, pp. 429–445, March 1996.

[145] M. El-Hajjar and L. Hanzo, "EXIT charts for system design and analysis," *IEEE Communications Surveys Tutorials*, vol. 16, no. 1, pp. 127–153, May 2014.

[146] S. Ten Brink, "Designing iterative decoding schemes with the extrinsic information transfer chart," *AEU Int. J. Electron. Commun*, vol. 54, no. 6, pp. 389–398, 2000.

[147] M. F. U. Butt, S. X. Ng, and L. Hanzo, "Self-concatenated code design and its application in power-efficient cooperative communications," *IEEE Communications Surveys Tutorials*, vol. 14, no. 3, pp. 858–883, January 2012.

[148] A. Papoulis, "Random variables, and stochastic processes," *McGraw-Hill, New York*, 1990.

[149] J. Klapper, "Phase-locked and frequency feedback systems: Principle and techniques," *Elsevier*, 2012.

[150] T. E. Humphreys, M. L. Psiaki, and P. M. Kintner, "Modeling the effects of ionospheric scintillation on GPS carrier phase tracking," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 46, no. 4, pp. 1624–1637, December 2010.

[151] I. Filippini, V. Sciancalepore, F. Devoti, and A. Capone, "Fast cell discovery in mm-wave 5G networks with context information," *IEEE Transactions on Mobile Computing*, vol. 17, no. 7, pp. 1538–1552, November 2018.

[152] Z. Na, Z. Pan, M. Xiong, J. Xia, and W. Lu, "Soft decision control iterative channel estimation for the internet of things in 5G networks," *IEEE Internet of Things Journal*, Early Access 2018.

[153] Z. Chang, M. F. Ezerman, S. Ling, and H. Wang, "Construction of de Bruijn sequences from product of two irreducible polynomials," *Cryptography and Communications*, vol. 10, no. 2, pp. 251–275, 2018.

[154] C. C. Tseng and C. Liu, "Complementary sets of sequences," *IEEE Transactions on Information theory*, vol. 18, no. 5, pp. 644–652, 1972.

[155] S. Ten Brink, "Convergence behavior of iteratively decoded parallel concatenated codes," *IEEE Transactions on Communications*, vol. 49, no. 10, pp. 1727–1737, October 2001.

[156] X. D. Lin and K. H. Chang, "Optimal PN sequence design for quasisynchronous CDMA communication systems," *IEEE Transactions on Communications*, vol. 45, no. 2, pp. 221–226, Feb 1997.

[157] H. Li, X. Cui, M. Lu, and Z. Feng, "Dual-folding based rapid search method for long PN-code acquisition," *IEEE Transactions on Wireless Communications*, vol. 7, no. 12, pp. 5286–5296, December 2008.

[158] F. Benedetto, G. Giunta, and S. Bucci, "A unified approach for time-delay estimators in spread spectrum communications," *IEEE Transactions on Communications*, vol. 59, no. 12, pp. 3421–3429, December 2011.

[159] A. Polydoros and C. L. Weber, "A unified approach to serial search spread-spectrum code acquisition-Part I: General theory," *IEEE Transactions on Communications Technology*, vol. Com-32, no. 3, pp. 542–549, May 1984.

[160] W. Wang and Z. Wang, "FPGA implementation of rapid PN code acquisition using iterative message passing algorithms," *IEEE Aerospace and Electronic Systems Magazine*, vol. 29, no. 6, pp. 13–23, June 2014.

Subject Index

Author Index