UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES

Optoelectronics Research Centre

UV-written Waveguide Circuits for Integrated Quantum Optics

by

Paolo L. Mennea

Thesis for the degree of Doctor of Philosophy

March 2018

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES
Optoelectronics Research Centre

Doctor of Philosophy

UV-WRITTEN WAVEGUIDE CIRCUITS FOR INTEGRATED QUANTUM OPTICS

by Paolo L. Mennea

Direct UV-written silica-on-silicon provides an attractive platform for quantum optics, offering the key benefits of low propagation losses and excellent optical fibre compatibility. This work has aimed to develop the necessary techniques and components for completely integrated quantum optics experiments to be carried out using this platform, on a larger scale than previously possible. Arrays of matched on-chip photon sources based on birefringence-matched spontaneous four-wave mixing (FWM) are demonstrated, both at 800 nm and in the telecommunications C-band, along with progress towards further integration of these sources. Thermo-optic phase shifters, for use in room temperature quantum circuits, have been optimised via modelling, and a range of alternative modulator technologies have been explored. Further work has been concerned with the development of a modular system for quantum optics, comprising a set of duplicate reconfigurable modules and the necessary drive electronics and software, with the intent of simplifying the task of identifying and quantifying manufacturing imperfections in large integrated experiments. Efforts have also been made to improve the detection efficiency of on-chip transition edge sensor (TES) single photon detectors, including the use of longer absorbers and high reflectors for multiple absorption passes; this has resulted in the demonstration of a photon-number-resolving detector with a Bragg grating enhanced quantum efficiency of 87%. Approaches for further increasing the detection efficiency are considered and a device for on-chip Hong-Ou-Mandel and photon subtraction experiments using these detectors is reported.

Declaration of Authorship

I, Paolo L. Mennea , declare that the thesis entitled *UV-written Waveguide Circuits for Integrated Quantum Optics* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as: See appendix A

Signed:.....

Date:.....

Acknowledgements

Thanks go to my supervisors James and Peter, without whom this thesis wouldn't exist. My many collaborators; Sae Woo Nam's group at NIST for their work on the detectors, particularly Thomas Gerrits, Adriana Lita and Brice Calkins. Ian Walmsleys group at the University Oxford, especially Ben Metcalf and William Clements for their experiments with the modular chips, and Justin Spring, Thomas Hiemstra, and Adrian Manssen for testing the waveguide sources. Thanks also to my colleagues, Matthew Posner for continuing with the source development, and Rex Bannerman for producing an invaluable mode measuring system. The oft overlooked technical staff also deserve a mention here, for their efforts in keeping the cleanroom facilities running smoothly, most of the time.

To M.D.M

Contents

List of Figures

Acronyms

ADC	analogue-to-digital converter.
ADR	adiabatic demagnetization refrigerator.
AOM	acousto-optic modulator.
APD	avalanche photodiode.
ASE	amplified spontaneous emission.
BPM	beam propagation method.
CAR	coincidence to accidental ratio.
CNOT	controlled-NOT.
DAC	digital-to-analogue converter.
DGW	direct grating writing.
EDFA	erbium doped fibre amplifier.
EO	electro-optic.
EOM	electro-optic modulator.
FBG	fibre bragg grating.
FFC	flat flexible cable.
FFT	fast Fourier transform.
FHD	flame hydrolysis deposition.
FPGA	field-programmable gate array.
FWM	four-wave mixing.
HBT	Hanbury Brown and Twiss.
HOM	Hong-Ou-Mandel.
ITO	indium-tin oxide.
KLM	Knill-Laflamme-Milburn.
MMI	multi-mode interference.
MZI	Mach-Zehnder interferometer.
NIST	National Institute of Standards and Technology.
NQIT	Networked Quantum Information Technologies.
NV	nitrogen vacancy.
OBR	optical backscatter reflectometer.
ODC	oxygen deficiency centre.

OSA	optical spectrum analyser.
OVD	outside vapour deposition.
PCF	photonic crystal fibre.
PLC	planar lightwave circuit.
PM	polarisation maintaining.
PMT	photo-multiplier tube.
PNR	photon number resolution.
PSO	position synchronised output.
PWM	pulse-width modulation.
QIP	quantum information processing.
QKD	quantum key distribution.
RIE	reactive ion etching.
RTA	rapid thermal annealer.
SLED	superluminous light-emitting diode.
SNSPD	superconducting nanowire single photon detector.
SPDC	spontaneous parametric down conversion.
SSPD	superconducting single photon detector.
TE	transverse electric.
TES	transition edge sensor.
TM	transverse magnetic.

Chapter 1

Introduction

Since the discovery of the 'quantum strangeness' lying at the heart of fundamental interactions at the smallest scales, many a physicist has dreamed of harnessing such effects for useful purposes, both in furthering our understanding of the universe and in performing real work. Great lengths have been taken to make this a reality and significant progress has already been made; and though there is still much to be done, this dream is perhaps at last within our reach.

In selecting a particular entity with which to study this strangeness we have numerous options, from electron spins to whole atoms; here we are concerned solely with photons — their generation, manipulation and detection. If we wish to do this on a large scale (while retaining our sanity), we must look toward integration to simplify matters. In this work, elements of a planar integrated platform are developed for linear quantum optics experiments, with the aim of ultimately forming a complete platform, capable of scaling to support larger experiments than are currently practical.

1.1 Harnessing Quantum Phenomena

Quantum information processing (QIP) is a topic of particular current interest, having captured both the public eye and significant industrial interest of late. QIP may broadly be divided into two areas; the first of these, quantum computing, promises an exponential reduction in algorithmic complexity for a variety of problems, while quantum communication offers truly secure communications channels.

1.1.1 Quantum Cryptography

Quantum cryptography is concerned with the application of physical phenomena to the provision of absolute information security. The fundamental security of such methods

stems from the impossibility of duplicating the state of an arbitrary qubit without modifying it, as stated by the quantum no cloning theorem [1].

Typically this takes the form of a lower bandwidth quantum communication channel used in tandem with a traditional classical channel. This quantum channel need not provide a great deal of bandwidth, it may be used purely to distribute secure keys for use in classical encryption algorithms on conventional channels; this is known as quantum key distribution (QKD). A number of commercial implementations of QKD have already been developed, and point-to-point fibre links have been operated over distances in excess of 300 km [2]. The main downfalls of current systems are the incompatibility of these channels with existing optical fibre networks, and the lack of quantum repeaters limiting the achievable link lengths, or equivalently key rates, due to loss.

1.1.2 Quantum Computing

The immense parallelism of quantum state evolution leads to the exciting prospect of performing computation in a way entirely different to classical methods. A handful of such algorithms have thusfar been developed, most notably Shor's algorithm for factoring integers [3] and Grover's search algorithm [4]. Both of these algorithms provide an exponential speed-up over the best known classical counterparts given equivalent resources, making their implementation highly desirable. The search for further algorithms offering quantum supremacy is still an active research topic, and indeed the nonexistence of equally fast classical algorithms is as yet unproven.

1.2 Universal Quantum Computation

A range of schemes have been proposed as potential platforms for quantum computation, including trapped ions, flux states in superconductors, and photon path states. It is the latter of these which is of relevance in this work. The exceedingly weak coupling of photons to sources of decoherence provides a clear advantage for QIP implementations, while the difficulty of creating and manipulating entanglement between photons poses a significant challenge.

1.2.1 Scalability and Error Correction

In any physical implementation, errors will occur during the course of a computation. In an optical system these predominantly consist of photon losses, though this is exacerbated by the probabilistic nature of the linear optical approach discussed shortly. These errors are introduced to some degree by every component of the system, thus as the system scales and more complex operations are attempted the likelihood of an error

occurring somewhere throughout the course of the computation increases. In order for a computer to be of any practical use clearly it must successfully complete an operation at least some proportion of the time. Thus, either the error probability must be small enough to permit this or the machine must be capable of recovering should an error occur, such a machine is termed fault tolerant.

In a classical computer an operation could simply be repeated until successful, operating on copies of the input; unfortunately, however, the no-cloning theorem mentioned previously prevents us from proceeding in this manner. A solution to these difficulties was proposed by Shor in a scheme in which each logical qubit is encoded within a multiphoton state formed from a set of entangled physical qubits, which can be much more robust to photon loss; operations are carried out on this cluster state and the single qubit result extracted from it for measurement at the end. The additional circuitry to form and operate on this larger state does of course introduce its own source of potential errors.

More recently the use of cluster states for fault tolerant computation has shown great promise, and garnered much interest. In such a state the loss of one qubit, or its measurement as the result of a failed entangling operation, does not collapse the rest of the state; an invaluable property when constructing larger states.

1.2.2 Surface Code

If a 2D array of cluster states is constructed, each formed by entangling a physical qubit with its four nearest neighbours, the resulting structure encodes a set of logical qubits in a surface code. This has a number of beneficial properties for fault-tolerant computation; by monitoring the parity of rows and columns one may detect and locate single bit flip errors within the surface, which may then be corrected by a suitable single-qubit operation [5]. Moreover, a range of multi-qubit errors have no adverse impact on the action of the network provided they form a closed loop of sites, preserving parity.

In this architecture operations are carried out by performing single qubit operations and making measurements on specific logical qubits in a particular order, selectively collapsing the entanglement; this is termed measurement based quantum computing. Since single qubit operations cannot introduce new entanglement the initial surface of cluster states provides the entire entanglement resource for any universal operation.

1.3 Optical Quantum Computing

1.3.1 Encoding Approaches

A single photon has a number of degrees of freedom which may be exploited for encoding quantum information, with varying degrees of difficulty, these are polarisation, path, frequency, and time-bin.

Polarisation — The efficient manipulation of polarisation with free space waveplates and beamcubes makes this an ideal encoding scheme for free space experiments. Polarisation is much more difficult to manipulate in an integrated format, though active materials such as $LiNiO_3$ and InP have been used for this purpose.

Path — Path encoding is commonly implemented in a dual rail scheme in which one path represents 0 and another 1. Gates can then readily be formed from beamsplitters and interferometers, which readily supports an integrated format.

Time-bin/Frequency — Time-bin encoding lends itself well to an optical fibre implementation, where sufficiently long delays may be achieved with relatively little loss. Frequency encoding has seen little use to date due to the difficulty of switching between frequency bins.

1.3.2 KLM Scheme

The linear optical approach to quantum computing was first proposed by Knill et al. in 2001 [6]. Until this point it was believed that quantum computation required a sufficiently strong non-linearity for high efficiency interactions between single photons to occur, which has not yet been accomplished [7]. The approach makes use of path encoded qubits, and in the simplest case requires single photon sources, beam splitters, phase shifters and high efficiency single photon detectors. Its primary drawback is that it is non-deterministic, that is to say the correct result will only be produced in a proportion of executions [6]. The success of an execution can however be determined through the use of additional 'ancilla' inputs [8], and a success probability arbitrarily close to unity may be obtained through more advanced schemes using additional ancillary resources [8].

This work was closely followed by myriad implementations based on the scheme using bulk optics [9, 10, 11], however, the scaling of these circuits is limited by their physical size [12]. This problem may be solved through integration of the circuit elements, providing a practical option for photonic quantum computing [12]; the monolithic nature of such devices also permits far greater stability than in bulk experiments. In a fully

integrated solution, suitable devices must be found to fulfill each of the roles outlined above.

Fault tolerance may be incorporated into this design by distributing a state of interest amongst several photons; partial measurements on these photons may then be used to determine whether a fault has occurred and to correct it via feed-forward. This permits error free computation to be carried out despite imperfect components, but does however carry the penalty of requiring significant overhead.

The chief difficulty with KLM based computational schemes is their inherently low success probability; this, compounded with material losses leads to impracticable resource requirements for fault-tolerant universal quantum computation based on a surface code architecture, with current best approaches requiring in excess of 10^5 detectors per qubit [13]. High-fidelity quantum memories would drastically improve matters, however based on current progress these are not likely to be available for some time, especially not in a suitably compact format to be used in number.

Even in the eventuality that *universal* all-optical quantum computation does not become feasible in the near future, there still exist a number of more specialised computational tasks to be explored, of which the most notable is boson sampling.

1.3.3 Boson Sampling

Whilst a truly universal linear optical quantum computer capable of outperforming classical systems does not appear to be feasible in the short term, principally due to the presence of significant loss and lack of probabilistic nature of linear optical operations, there are areas for which relatively small optical systems can indeed exceed current capabilities; in particular the area of boson sampling.

It has been demonstrated that sampling from the outputs of a linear optical network is equivalent to the calculation of a quantity related to the permanent of the systems' transfer function, and furthermore that this quantity is #P-hard in the computational complexity sense [14]. This means that the problem falls into a class for which, it is believed, no polynomial-time algorithm exists. The consequence of this is that the demonstration of such a computation, that of operating such a network and measuring its outputs, would either invalidate the extended Church-Turing theses or collapse the complexity polynomial hierarchy, both of which are strongly regarded in their respective fields. The former of these states that any algorithm may be efficiently simulated on a non-deterministic Universal Turing machine.

Following this development came a number of small scale demonstrations of such an experiment in integrated networks [15, 16, 17, 18], with no more than three photons. More recently Wang *et al.* showed sampling with up to five bosons [19]. In order for

current classical computers to be outperformed it has been calculated that a network in the region of of 100 modes with 35 photons is required. While challenging, this is within the realms of current capabilities given that, via the scatter-shot approach, simultaneous counts of all input photons are not necessary [20].

1.3.4 A Hybrid approach

Arguably the most promising approach to fault-tolerant computation is a hybrid approach consisting of modules of qubits with high-fidelity state preparation, implemented with trapped ions for example, linked via a photonic interconnect permitting entanglement between modules; it is exactly this scheme that the Networked Quantum Information Technologies (NQIT) project is exploring.

1.4 An Engineering Challenge

1.4.1 Components of a Photonic Quantum Machine

With the set of one qubit operations and a single two-qubit operation, forming a universal set, it is possible to implement any quantum computational algorithm.

Photon Sources To begin with we must first have a source of photons, suitably pure and indistinguishable in order to permit high-quality quantum interference.

Single-photon Operations There are three single photon operations, corresponding to the Pauli rotations on the Bloch sphere.

Two-photon Gates A circuit performing a two-photon operation such as the controlled-NOT (CNOT) gate; any one type of two-photon gate is sufficient to produce arbitrary circuits. The unitary nature of quantum circuits requires that they have an equal number of inputs and outputs, two in this case.

Photon Detection The outputs of our quantum machine are extracted through detection of photons, of which there are a range of options depending on the encoding scheme. The 'click' type detectors include photo-multiplier tubes (PMTs), avalanche photodiodes (APDs) and superconducting nanowire single photon detectors (SNSPDs), while number-resolving detectors are implemented with transition edge sensors (TESs) or multiplexed click detectors. Detection is not solely a form of readout, in the KLM scheme measurement forms an integral part of the machine's operation.

1.4.2 Integrated Quantum Optics

A number of platforms are currently being explored for integrated optical QIP; these include silica-on-silicon, lithium niobate, GaAs and silicon [21]. To date, silica is perhaps the most developed of these for QIP applications, with much of the early experiments being done using this platform. Initial experiments began with the analysis of quantum and classical interference by Politi et al. [22], for which an etched silica-on-silicon directional coupler was used as an integrated equivalent of a beamsplitter. The first integrated, two-qubit path encoded quantum gate, a CNOT gate, was also demonstrated [22]; although full characterisation of this device was not possible at the time due to the additional circuitry required. A CNOT gate has also been produced for polarisation qubits [23].

In 2009, on-chip thermo-optic phase shifters were used in conjunction with Mach-Zehnder interferometers (MZIs) to provide a configurable quantum circuit element using this technology for the first time [24], operating at 800 nm. This was followed by the implementation of a somewhat contrived compiled version of Shor's algorithm, capable of factoring the input 15, and demonstrating entanglement of four photons [25]. In 2011, a fully configurable two qubit gate was produced by Shadbolt et al., this again utilised the combination of thermo-optic phase shifters and MZIs to form variable beam splitters [26]. More recently, this field has seen a great deal of interest, with experiments using up to five photons having been demonstrated.

Silica has also been used extensively in QKD experiments; for example, in 2004 it was utilised to provide the critical MZI component in a QKD system operating at 1550 nm [27]. The excellent fibre coupling possible with silica planar lightwave circuits (PLCs) along with their low waveguide loss of < 0.1 dB/cm makes silica an ideal choice for this type of application [28].

Recently, there has been significant progress in on-chip single photon detection, with two groups developing integrated SNSPDs on GaAs ridge waveguides [29, 30]. Compared with the integrated TES based detector [31], which forms the basis for part of this project, higher detection efficiencies have been reported for SNSPDs, although with significantly lower fibre coupling efficiencies. Additionally, these detectors are not number resolving and photon number resolution has not as yet clearly been demonstrated with superconducting nanowire detectors.

1.4.3 Material platforms

The various material platforms under investigation for QIP each have relative merits; the parameters of most interest being their material loss, achievable coupling loss, and device density. Silica offers the lowest material and fibre coupling losses, while the high-index materials offer improved device densities. Also of importance are the types of

active elements permitted by each material, III-V semiconductors allow for quantum-dot based single-photon sources, while lithium niobate and other electro-optic materials offer efficient on-chip modulators. Some important parameters for consideration are collected in table 1.1.

Femtosecond-written silica offers the freedom to define waveguide structures in three dimensions, this has been used to produce 2D-waveguide arrays for quantum-walk simulations. It is also possible to manipulate the waveguide cross section along its length both vertically and horizontally, which has been used to produce mode converters between source and circuit chips of different materials. Historically this fabrication technique suffered from high induced material losses and poor uniformity, however, this technology has improved greatly and is now comparable in device performance to other silica fabrication approaches.

Silicon photonics has seen a great deal of interest of late for quantum applications, principally due to the high device densities possible. The enormous research activity in silicon photonics for electronic device interconnects, among other applications, has led to drastic reductions in both the material and coupling losses of this platform and this trend is likely to continue for some time. Furthermore, commercial photonics foundries have made well-developed processes available to quantum optics researchers. Practical coupling efficiencies are still relatively high however, which has hindered quantum experiments with these devices. Ideally all elements of an experiment, from photon-sources to detectors, would be integrated on a single chip which would make coupling efficiency irrelevant; however, combining cryogenic photon detectors in particular with most modulator and source technologies will be very difficult to achieve due to the limited cooling power of refrigerators – this challenge is discussed in more detail in chapter 6.

Recently, there has been interest in heterogeneous integration [32], combining the advantages of different materials and techniques at the cost of additional fabrication complexity. III–V Quantum dot sources have been integrated with silicon nitride waveguides for example [33], and diamond nitrogen vacancy (NV) centres transferred to fibre tapers [34]. Detectors too have been integrated in this way, Najafi *et al.* having combined SNSPDs with silicon waveguides via a surprisingly high-yield transfer approach [35].

For each platform the inherent material losses place restrictions on the range of operating wavelengths, which have consequences for the other elements in the system, thereby limiting the types of sources and detectors that may be used and compatibility with memories. In the next section we shall discuss this issue of operating wavelengths specifically.

1.4.4 Operating wavelengths

The telecommunication C-band centered at 1550 nm offers a number of important advantages for photonic quantum circuits, principally this is the minimum loss window for silica, itself the lowest loss optical material available for the near infrared [36]. This wavelength also offers compatibility with existing telecommunications components. It is also informative to note that optical fibre is one of only two mediums, along with free space, for which quantum communication is currently believed to be practical [8]. Traditionally, the primary disadvantage of 1550 nm has been the absence of readily available high-efficiency single-photon detectors, as well as the lack of suitable atomic resonances within this band for the production of quantum memories. It is for this reason that the majority of integrated quantum circuits to-date have operated in the 800 nm region. As a result, while moving entirely to 1550 nm would be desirable within this project, work was conducted at both of these wavelengths with a gradual shift to the telecommunications band throughout its course.

Table 1.1: A comparison of common material platforms in use for integrated quantum optics experiments. Free space is included for reference.

Material	Operating wavelength[3]	n[1]	Propagation[2] loss (dB/cm)	Fibre coupling loss (dB)	Source schemes	Detectors	Entanglement record
Silica	800 nm	1.4	0.3	0.2	FWM	TES, SNSPD	4 [37]
Silica	1.5 µm	1.4	0.05	0.1	FWM	TES, SNSPD	2
Silicon	1.5 µm	3.5	2.0	5	FWM	SNSPD [35]	2 [35]
Si_3N_4 [4]	1.5 µm	2.0	< 0.2	1[5]	FWM [38]	SNSPD	2 [39]
$LiNiO_3$	1.5 µm	2.4				SNSPD [40]	2
Diamond	700 nm	2.4			Colour centres	SNSPD	
GaAs	920 nm	3.7	66 dB/cm		InGaAs QD [41]	SNSPD [41]	2 [42]
Free space	N/A	1	0	N/A	SPDC, PPLN	TES, SNSPD	8 [43]

[1] At operating wavelength. [2] Minimum reported for a waveguide in a quantum experiment. [3] Typical operating wavelengths for quantum optics experiments.
[4] TriPlex [5] With spot-size conversion [39]

1.5 Building Large Quantum States Project

It should be noted that the work detailed herein has a close relationship with the EPSRC funded programme grant, Building Large Quantum States out of light (BLoQS), led by the University of Oxford in collaboration with the University of Southampton and Imperial College London.

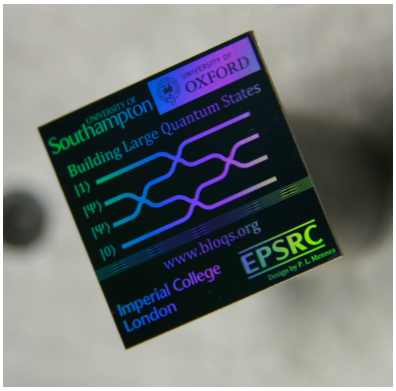


Figure 1.1: An outreach chip for the Building Large Quantum States out of light (BLoQS) project, designed and fabricated by the author.

1.6 Chapter Layout

The aim of this project is broadly that of further developing the silica-on-silicon platform for integrated quantum optics, including work on on-chip single photon sources, modulators and detectors. In much of this work the Direct UV Writing process is used to pattern waveguiding structures in a photosensitive silica-on-silicon planar structure. In the next chapter the fabrication of this substrate and the UV writing process are detailed, along with other fabrication techniques used throughout the work. Chapter 3 is concerned with work on on-chip single photon sources. Chapter 4 deals with modulators for quantum networks, which is followed by the development of a system of modular circuits in chapter 5. Chapter 6 covers integration of single photon detectors with waveguides. Finally, in Chapter 7 conclusions are drawn and areas for further development highlighted. All work detailed was carried out by the author, and where this is not the case it has been stated explicitly in the relevant section.

References

[1] B. W. Kok, Pieter; Lovett, *Introduction to Optical Quantum Information Processing.* New York: Cambridge University Press, 2010.

[2] B. Korzh, C. C. W. Lim, R. Houlmann, N. Gisin, M. J. Li, D. Nolan, B. Sanguinetti, R. Thew, and H. Zbinden, "Provably secure and practical quantum key distribution over 307 km of optical fibre," *Nature Photonics*, vol. 9, no. 3, pp. 163–168, Feb 2015.

[3] P. W. Shor, "Algorithms for quantum computation: discrete logarithms and factoring," in *Proceedings 35th Annual Symposium on Foundations of Computer Science*, Nov 1994, pp. 124–134.

[4] L. K. Grover, "A fast quantum mechanical algorithm for database search," in *Proceedings of the Twenty-eighth Annual ACM Symposium on Theory of Computing*, ser. STOC '96. New York, NY, USA: ACM, 1996, pp. 212–219.

[5] R. Raussendorf and J. Harrington, "Fault-tolerant quantum computation with high threshold in two dimensions," *Phys. Rev. Lett.*, vol. 98, p. 190504, May 2007.

[6] E. Knill, R. Laflamme, and G. J. Milburn, "A scheme for efficient quantum computation with linear optics." *Nature*, vol. 409, no. 6816, pp. 46–52, Jan 2001.

[7] S. Tanzilli, A. Martin, F. Kaiser, M. De Micheli, O. Alibart, and D. Ostrowsky, "On the genesis and evolution of Integrated Quantum Optics," *Laser & Photonics Reviews*, vol. 6, no. 1, pp. 115–143, Jan 2012.

[8] P. Kok, K. Nemoto, T. C. Ralph, J. P. Dowling, and G. J. Milburn, "Linear optical quantum computing with photonic qubits," *Reviews of Modern Physics*, vol. 79, no. 1, pp. 135–174, Jan 2007.

[9] J. L. O'Brien, G. J. Pryde, A. G. White, T. C. Ralph, and D. Branning, "Demonstration of an all-optical quantum controlled-NOT gate." *Nature*, vol. 426, no. 6964, pp. 264–7, Nov 2003.

[10] P. Kok, H. Lee, and J. Dowling, "Single-photon quantum-nondemolition detectors constructed with linear optics and projective measurements," *Physical Review A*, vol. 66, no. 6, pp. 1–9, Dec 2002.

[11] R. Okamoto, J. L. O'Brien, H. F. Hofmann, and S. Takeuchi, "Realization of a Knill-Laflamme-Milburn controlled-NOT photonic quantum circuit combining effective optical nonlinearities." *Proceedings of the National Academy of Sciences of the United States of America*, vol. 108, no. 25, pp. 10 067–71, jun 2011.

[12] A. Politi, J. Matthews, M. Thompson, and J. O'Brien, "Integrated Quantum Photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 15, no. 6, pp. 1673–1684, 2009.

[13] Y. Li, P. C. Humphreys, G. J. Mendoza, and S. C. Benjamin, "Resource costs for fault-tolerant linear optical quantum computing," *Physical Review X*, vol. 5, no. 4, pp. 1–15, 2015.

[14] S. Aaronson, "A linear-optical proof that the permanent is #p-hard," *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 467, no. 2136, pp. 3393–3405, Jul 2011.

[15] J. Spring, B. Metcalf, and P. Humphreys, "Boson sampling on a photonic chip," *Science*, vol. 050502, no. 2008, 2013.

[16] M. A. Broome, A. Fedrizzi, S. Rahimi-Keshari, J. Dove, S. Aaronson, T. C. Ralph, and A. G. White, "Photonic boson sampling in a tunable circuit," *Science*, vol. 339, no. 6121, pp. 794–798, Dec 2012.

[17] M. Tillmann, B. Dakić, R. Heilmann, S. Nolte, A. Szameit, and P. Walther, "Experimental boson sampling," *Nature Photonics*, vol. 7, no. 7, pp. 540–544, May 2013.

[18] A. Crespi, R. Osellame, R. Ramponi, D. J. Brod, E. F. Galvão, N. Spagnolo, C. Vitelli, E. Maiorino, P. Mataloni, and F. Sciarrino, "Integrated multimode interferometers with arbitrary designs for photonic boson sampling," *Nature Photonics*, vol. 7, no. 7, pp. 545–549, May 2013.

[19] H. Wang, Y. He, Y.-H. Li, Z.-E. Su, B. Li, H.-L. Huang, X. Ding, M.-C. Chen, C. Liu, J. Qin, J.-P. Li, Y.-M. He, C. Schneider, M. Kamp, C.-Z. Peng, S. Höfling, C.-Y. Lu, and J.-W. Pan, "High-efficiency multiphoton boson sampling," *Nature Photonics*, vol. 11, no. 6, pp. 361–365, May 2017.

[20] M. Bentivegna, N. Spagnolo, C. Vitelli, F. Flamini, N. Viggianiello, L. Latmiral, P. Mataloni, D. J. Brod, E. F. Galvao, A. Crespi, R. Ramponi, R. Osellame, and F. Sciarrino, "Experimental scattershot boson sampling," *Science Advances*, vol. 1, no. 3, Apr 2015.

[21] M. Thompson, A. Politi, J. Matthews, and J. O'Brien, "Integrated waveguide circuits for optical quantum computing," *IET Circuits, Devices & Systems*, vol. 5, no. 2, p. 94, 2011.

[22] A. Politi, M. J. Cryan, J. G. Rarity, S. Yu, and J. L. O'Brien, "Silica-on-silicon waveguide quantum circuits." *Science (New York, N.Y.)*, vol. 320, no. 5876, pp. 646–9, may 2008.

[23] A. Crespi, R. Ramponi, R. Osellame, L. Sansoni, I. Bongioanni, F. Sciarrino, G. Vallone, and P. Mataloni, "Integrated photonic quantum gates for polarization qubits," *Nature communications*, vol. 2, p. 566, Jan 2011.

[24] B. J. Smith, D. Kundys, N. Thomas-peter, and I. A. Walmsley, "Phase-controlled integrated photonic quantum circuits," *Optics Express*, vol. 17, no. 16, pp. 264–267, Jul 2009.

[25] A. Politi, J. C. F. Matthews, and J. L. O. Brien, "Shor's Quantum Factoring Algorithm on a Photonic Chip," *Quantum Information Processing*, vol. 325, no. 5945, p. 1221, Sep 2009.

[26] P. J. Shadbolt, M. R. Verde, A. Peruzzo, A. Politi, A. Laing, M. Lobino, J. C. F. Matthews, and J. L. O'Brien, "Generating, manipulating and measuring entanglement and mixture with a reconfigurable photonic circuit," *Nature Photonics*, vol. 6, no. 1, p. 6, Dec 2011.

[27] Y. Nambu, T. Hatanaka, and K. Nakamura, "BB84 Quantum Key Distribution System Based on Silica-Based Planar Lightwave Circuits," *Japanese Journal of Applied Physics*, vol. 43, no. No. 8B, pp. L1109–L1110, Jul 2004.

[28] G. P. Agrawal, *Lightwave Technology Components and Devices*, 2nd ed. Hoboken, New Jersey: John Wiley & Sons, 2004.

[29] J. P. Sprengers, A. Gaggero, D. Sahin, S. Jahanmirinejad, G. Frucci, F. Mattioli, R. Leoni, J. Beetz, M. Lermer, M. Kamp, S. Hofling, R. Sanjines, and A. Fiore, "Waveguide superconducting single-photon detectors for integrated quantum photonic circuits," *Applied Physics Letters*, vol. 99, no. 18, p. 181110, Nov 2011.

[30] W. Pernice, C. Schuck, O. Minaeva, M. Li, G. Goltsman, A. Sergienko, and H. Tang, "High-speed and high-efficiency travelling wave single-photon detectors embedded in nanophotonic circuits," *Nature Communications*, vol. 3, no. 1, Jan 2012.

[31] T. Gerrits, N. Thomas-Peter, J. Gates, A. Lita, B. Metcalf, B. Calkins, N. Tomlin, A. Fox, A. Linares, J. Spring, N. Langford, R. Mirin, P. G. Smith, I. Walmsley, and S. W. Nam, "On-chip, photon-number-resolving, telecommunication-band detectors for scalable photonic information processing," *Physical Review A*, vol. 84, no. 6, pp. 1–4, Dec 2011.

[32] S. Bogdanov, M. Y. Shalaginov, A. Boltasseva, and V. M. Shalaev, "Material platforms for integrated quantum photonics," *Optical Materials Express*, vol. 7, no. 1, pp. 111–132, Jan 2017.

[33] M. Davanco, J. Liu, L. Sapienza, C.-Z. Zhang, J. V. D. M. Cardoso, V. Verma, R. Mirin, S. W. Nam, L. Liu, and K. Srinivasan, "Heterogeneous integration for on-chip quantum photonic circuits with single quantum dot devices," *Nature Communications*, vol. 8, no. 1, Oct 2017.

[34] R. N. Patel, T. Schröder, N. Wan, L. Li, S. L. Mouradian, E. H. Chen, and D. R. Englund, "Efficient photon coupling from a diamond nitrogen vacancy center by integration with silica fiber," *Light: Science & Applications*, vol. 5, p. e16032, Feb 2016.

[35] F. Najafi, J. Mower, N. C. Harris, F. Bellei, A. Dane, C. Lee, X. Hu, P. Kharel, F. Marsili, S. Assefa, K. K. Berggren, and D. Englund, "On-chip detection of non-classical light by scalable integration of single-photon detectors," *Nature Communications*, vol. 6, no. 1, Jan 2015.

[36] A. Ghatak and K. Thyagarajan, *Introduction to Fiber Optics*. Cambridge University Press, 2000.

[37] J. Carolan, C. Harrold, C. Sparrow, E. Martin-Lopez, N. J. Russell, J. W. Silverstone, P. J. Shadbolt, N. Matsuda, M. Oguma, M. Itoh, G. D. Marshall, M. G. Thompson, J. C. F. Matthews, T. Hashimoto, J. L. O'Brien, and A. Laing, "Universal linear optics," *Science*, vol. 349, no. 6249, pp. 711–716, Aug 2015.

[38] X. Zhang, Y. Zhang, C. Xiong, and B. J. Eggleton, "Correlated photon pair generation in low-loss double-stripe silicon nitride waveguides," *Journal of Optics*, vol. 18, no. 7, p. 074016, Jun 2016.

[39] C. Xiong, X. Zhang, A. Mahendra, J. He, D.-Y. Choi, C. J. Chae, D. Marpaung, A. Leinse, R. G. Heideman, M. Hoekman, C. G. H. Roeloffzen, R. M. Oldenbeuving, P. W. L. van Dijk, C. Taddei, P. H. W. Leong, and B. J. Eggleton, "Compact and reconfigurable silicon nitride time-bin entanglement circuit," *Optica*, vol. 2, no. 8, pp. 724–727, Aug 2015.

[40] M. G. Tanner, L. S. E. Alvarez, W. Jiang, R. J. Warburton, Z. H. Barber, and R. H. Hadfield, "A superconducting nanowire single photon detector on lithium niobate," *Nanotechnology*, vol. 23, no. 50, p. 505201, Nov 2012.

[41] G. Reithmaier, M. Kaniber, F. Flassig, S. Lichtmannecker, K. Mller, A. Andrejew, J. Vukovi, R. Gross, and J. J. Finley, "On-chip generation, routing, and detection of resonance fluorescence," *Nano Letters*, vol. 15, no. 8, pp. 5208–5213, 2015.

[42] J. Wang, A. Santamato, P. Jiang, D. Bonneau, E. Engin, J. W. Silverstone, M. Lermer, J. Beetz, M. Kamp, S. Höfling, M. G. Tanner, C. M. Natarajan, R. H. Hadfield, S. N. Dorenbos, V. Zwiller, J. L. O'Brien, and M. G. Thompson, "Gallium arsenide (GaAs) quantum photonic waveguide circuits," *Optics Communications*, vol. 327, pp. 49–55, Sep 2014.

[43] X.-C. Yao, T.-X. Wang, P. Xu, H. Lu, G.-S. Pan, X.-H. Bao, C.-Z. Peng, C.-Y. Lu, Y.-A. Chen, and J.-W. Pan, "Observation of eight-photon entanglement," *Nature Photonics*, vol. 6, no. 4, pp. 225–228, Feb 2012.

Chapter 2

UV Writing and Integrated Planar Waveguides

2.1 Introduction

In this chapter we will begin with the fundamental concepts of planar waveguides, as well as the various fabrication techniques used throughout the following chapters in producing UV-written waveguides.

2.2 Planar Waveguides

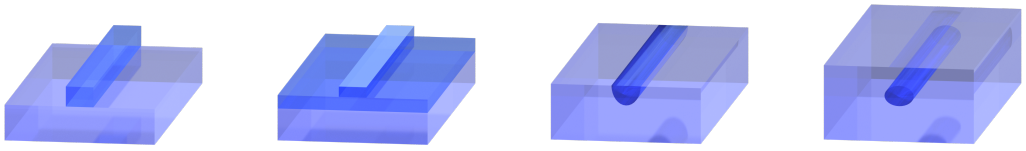
This work makes use of UV written waveguides composed of a fixed slab structure, defining the vertical extent of the waveguide, which is modified through an absorption induced refractive index increase to provide lateral confinement. Typically this structure is composed of undercladding, core, and overcladding layers, while in the integrated detector work of Chapter 6 it is necessary that waveguides without an overcladding are used.

Due to the limited space available a full review of the relevant planar waveguide theory is not possible here, the reader is instead directed to other sources [1, 2] for a more complete treatment.

2.2.1 Waveguide Geometries

There are several types of planar waveguide geometry, as illustrated in figure 2.1; the first of these is the ridge waveguide, in which the waveguide sits proud of the substrate, the most common form for semiconductor waveguides; this ridge may also only be partially

etched, resulting in a rib waveguide. Next we have the channel waveguide, where the core is in line with the surface of the structure, which is typical of devices formed by ion diffusion. Finally we have the buried channel waveguide in which the core is completely embedded in the cladding, which is typical of laser-written waveguides such as those of this work.



(a) (b) (c) (d)

Figure 2.1: An illustration of the types of planar waveguiding structures; (a) ridge, (b) rib, (c) channel and (d) buried channel.

2.3 Modelling of Planar Waveguides

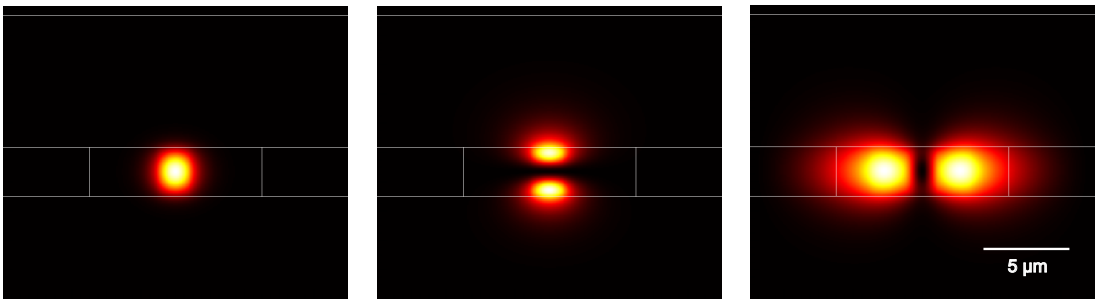
Several different techniques were adopted during this project for modelling the behaviour of planar waveguides; these are outlined in the following sections.

2.3.1 Mode Solving

A commercial 2D mode-solving package, FIMMWAVE, was used throughout this work to identify the supported modes in a given waveguide geometry. FIMMWAVE provides mode solvers for a variety of waveguide types; in particular, graded-index structures suitable for representing UV-written waveguides may be analysed with the use of its MWG interface and numerical solvers. Importantly, this software is capable of the complex-mode solving necessary for modelling devices with absorbing metal layers, such as the integrated single-photon detectors of Chapter 4.

Modelling of this type of waveguide is complicated somewhat compared with the step refractive index profiles of etched devices. The photosensitive inscription process results in a lateral profile following the intensity profile of the writing beam. In the vertical dimension the device is typically modelled with a step profile.

Figure 2.2 presents FIMMWAVE modelling of the typical UV-written waveguiding structure used throughout the following chapters, displayed are profiles of the fundamental mode and first two higher-order modes in the TM polarisation, based on a wafer designed for 780 nm operation (NB215). In the following section the UV-writing process used in fabricating these structures is discussed.



(a) (b) (c)

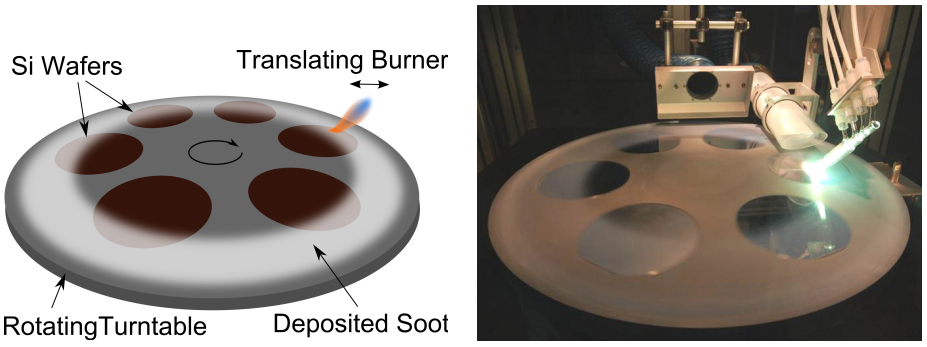
Figure 2.2: (a) TM_{00} fundamental guided mode and (b) TM_{01} (c) TM_{10} higher-order modes of a UV-written waveguide (operating at 780 nm) modelled in FIMMWAVE.

2.4 Silica-on-silicon

In this section the fabrication process for the silica-on-silicon waveguides used throughout this work is outlined. The waveguides themselves are either etched or, as is exclusively used here, UV written. UV writing is carried out on individual chips diced from a silicon wafer, on which is deposited a series of glass layers through flame hydrolysis deposition (FHD); it is with this process that we shall commence.

2.4.1 Flame Hydrolysis Deposition

The layered slab waveguide structure used in this work was fabricated via FHD, a process in which doped silica is deposited upon a substrate through hydrolysis and oxidisation of halide precursors in a similar fashion to outside vapour deposition (OVD), which is used to produce optical fibre preforms. A rotating turntable is utilised in combination with a translating torch to deposit a uniform soot layer over a wafer. This soot layer is then consolidated in a furnace at a temperature of $\sim 1200°C$ to form a glass.



(a) (b)

Figure 2.3: (a) Diagram and (b) image of the FHD system (Norberta) in use throughout this work.

2.4.1.1 Substrates for FHD

A silicon wafer is used as the substrate, with a thermally grown native oxide layer commonly forming the undercladding. Silicon provides a low-cost substrate option with the advantage of permitting growth of a thermal oxide. The key parameters restricting the type of substrate that may be used are the thermal expansion coefficient and any layer reactivity.

2.4.1.2 Deposition Process

Core and overcladding layers are then deposited via FHD with a consolidation step for each. Crucially, the precursor composition fed to the flame permits doping of the glass to affect its optical properties and consolidation temperature. Three different dopants are used, germanium, boron, and phosphorus; each having different effects on the properties of the resulting glass matrix. The addition of any of these dopants will tend to reduce the melting point of the glass; each layer should have a lower melting point than that preceding it to prevent re-melting of these layers during subsequent consolidation steps, thus the cladding must be more heavily doped than the core. Germanium doping increases the refractive index of the layer, while also providing the defects that lead to the photosensitivty utilised during UV writing as described in section 2.5.1; it is thus only present in the core layer. Boron reduces the refractive index and is used in combination with the germanium to provide the required index contrast in the core layer, as well as promoting photosensitivty. Phosphorus increases the refractive index without providing photosensitivity, it is used in combination with boron to reduce the melting point of cladding layers while maintaining a refractive index matched to thermal oxide.

The precursors used as the source for these dopants and the silica matrix are halides, $SiCl_4$, $GeCl_4$, PCl_3 and BCl_3. With the exception of BCl_3 these precursor gasses are provided via a nitrogen bubbler system; a heated oil bath houses liquid precursors, through which a flow of nitrogen is passed that draws with it a small quantity of the precursor in vapour form. The quantity of precursor is determined by the nitrogen flow rate, controlled via mass-flow controllers. This system has the advantage of purifying the precursors at point of use; in particular transition metal halides have a much lower vapour pressure than do the precursors of interest, thus the system minimises transition metal contamination of the resulting glass. This approach cannot be used for BCl_3 since it is not found in liquid form at atmospheric pressure, it is instead fed directly to the torch in gaseous form. The precursors are fed to a hydrogen oxygen flame with an argon sheath flow. The ratio of these torch gasses controls the shape and temperature of the flame, which in turn affects the properties of the deposited soot particles.

2.4.1.3 Layer Consolidation

Consolidation of the deposited soot to form a glass layer is carried out in a vertical tube furnace; the temperature is ramped from 500°C to the soak temperature of 1360°C for a core layer, 1260°C for a cladding, over a period of two hours. It is held at this temperature for 2-5 hours, during which the layer is above its glass-transition temperature, before a controlled ramp down to 600°C at 7°C $\cdot \text{min}^{-1}$; as the wafer cools it undergoes significant thermal contraction which places the core layer under compressive stress due to the differing expansion coefficients of the FHD layers and silicon substrate. The consolidation process can induce defects in the final glass matrix, typically caused by particulates from the furnace settling on the soot layer. Often, several defects will be induced per layer for a 6-inch wafer.

2.4.2 Layer Metrology

Typically a separate test wafer is included in each layer deposition run, from which the layer thickness and refractive index are determined via a prism coupling technique with knowledge of the substrate refractive index, using a Metricon prism-coupling system. The key parameters of an FHD layer are its thickness and index contrast with respect to the thermal oxide cladding (n = 1.4449 at 1550 nm). The overcladding is commonly index matched to the thermal oxide to make the waveguide symmetrical; the core is often also of small contrast (zero-delta) to improve matching with an optical fibre mode.

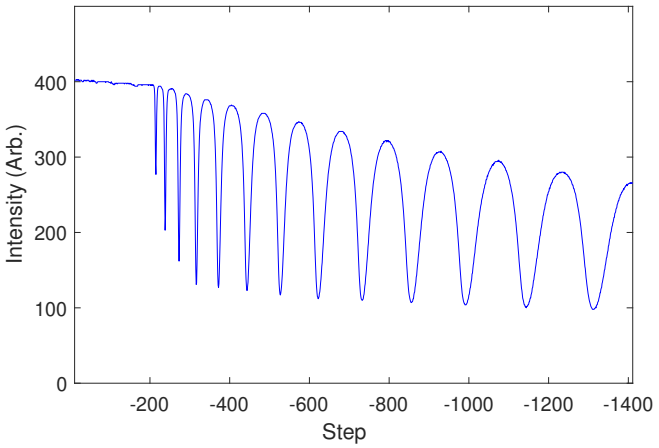


Figure 2.4: An example scan from the Metricon prism coupling system for thin film metrology, fitting to the dip positions yields layer refractive index and thickness.

In the prism coupling approach a laser is incident on the layer to be measured via a prism of calibrated refractive index which is held in contact. The reflected beam power

is monitored as the assembly is rotated, adjusting the incident angle; for some angles light is coupled into a guided planar mode of the layer and reflection is suppressed, leading to a plot like that of figure 2.4. The angles at which these couplings occur are related to the effective indices of the guided modes, from which the refractive index and thickness of the layer may be computed.

2.4.3 Sample Preparation

After fabrication, the wafer is diced into individual chips of the desired size, usually 10 mm wide and between 10 mm and 60 mm long depending on the application, with the use of a dicing saw. Careful choice of blades and suitable blade dressing procedures enables optical-quality facets to be produced through dicing alone [3]; in most cases however this is unnecessary since butt-coupling is used, making the effects of top-surface chipping and facet imperfections less significant. For the majority of wafer dicing in this work, 1200 grit diamond embedded resin blades were used at 20,000 rpm with a feed rate of 0.4 $\text{mm}\cdot\text{s}^{-1}$.

2.5 Direct UV Writing

Direct UV Writing is a technique to produce channel waveguides in photosensitive glass layers, commonly produced via FHD. It is a versatile technique capable of producing a range of waveguiding structures rapidly without the need for photolithographic processing or cleanroom conditions. A focussed 244 nm UV laser beam is translated over the surface using a 4-axis air-bearing stage system under software control. Absorption in exposed regions leads to a localised refractive index increase in the visible to near infrared via the Kramers-Kronig relationship, allowing wave-guiding structures to be produced. Refractive index contrasts of the order of 10^{-3} are typically achieved through this process; this makes it suitable for devices with mode sizes matched to that of optical fibre ($\approx$ 8 µm at 1550 nm), permitting high coupling efficiencies to be achieved between the two [4]. Waveguides have been produced using this technique with propagation losses as low as 0.05 dB/cm [5]; the relatively low index contrasts do, however, place restrictions on the achievable device dimensions, thus limiting the packing density in more complex devices.

2.5.1 Photosensitivity Mechanisms

Photosensitivity is induced in the core layer through the addition of germanium and boron in the glass matrix. This leads to the formation of a variety of lattice defects known as oxygen deficiency centres (ODCs), which absorb in the UV. It is believed that

the majority of the observed UV induced index change is due to the breaking of bonds associated with these defects [6], although thermal effects and densification likely also contribute to the change [7].

2.5.1.1 Hydrogen Loading

Hydrogenation of the samples, achieved by storing them in a high pressure hydrogen cell for ~ 1 week, is used to enhance the photosensitivity. This increase in photosensitivity is due both to the formation of OH groups, which leave additional ODCs, and its action as a photobleaching catalyst [6].

This hydrogen does out-diffuse over time at room temperature. After hydrogenation, the samples are thus stored in liquid nitrogen to greatly slow this process until UV writing is carried out.

2.5.2 Fluence

The magnitude of this index increase is dependent on the total exposure, or writing fluence, used. This relationship is approximately linear but saturates at higher fluence values. The writing fluence also affects the lateral dimension of the waveguide; although this is largely determined by the spot size, the Gaussian beam profile will be reflected in the induced index profile, hence the increasing peak index with fluence will also cause broadening of the waveguide.

2.6 Integrated Bragg Gratings

One particular advantage of the direct UV writing approach is that Bragg gratings may readily be incorporated within the defined waveguides. This is achieved through the use of a pair of overlapping beams, providing an interference pattern with a period defined by the wavelength and crossing angle of the beams.

The grating period is not limited to that of the interference pattern however. Selectively exposing areas as the spot is translated allows other periods to be built up; this may be accomplished by either amplitude modulating the beam, or by shifting the interference pattern via a phase shift. This will result in a reduced modulation depth for periods with increasing detuning from the interference pattern period, though this effect is small and periods corresponding to wavelengths between 1400 nm and 1700 nm are achievable in the current system due to the small number of fringes present within the spot size.

Bragg gratings have proven to be an invaluable tool, both out-of-band for characterisation of waveguide arrangements, and in-band, particularly in the work of section 6.4.3.

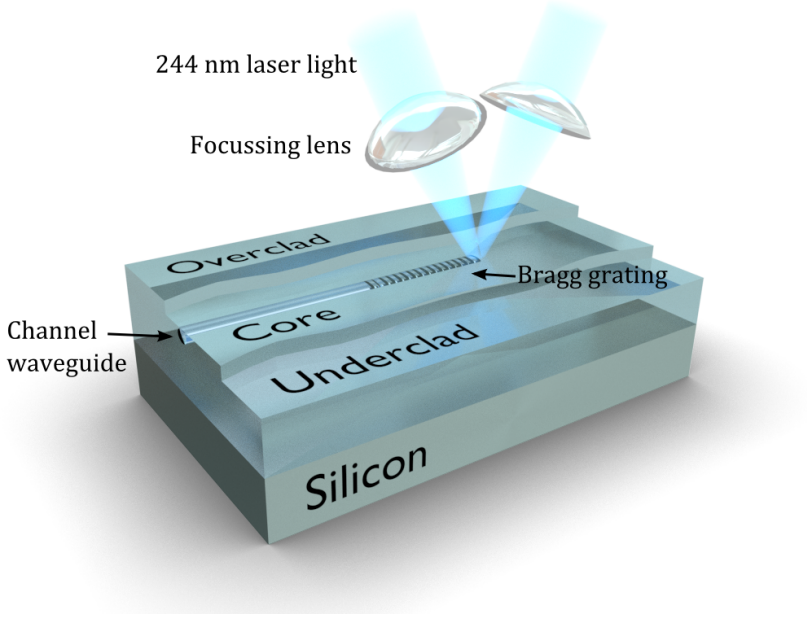


Figure 2.5: The two-beam UV writing arrangement – laser beams at 244 nm are focussed and overlapped in the core of a photosensitive sample, the resulting interference pattern is used to inscribe both waveguides and gratings as the sample is translated relative to the writing spot.

Gaussian apodised gratings are primarily used here since their suppressed sidebands permit closer spectral spacing of gratings without significant interference between adjacent peaks [8].

2.6.1 Planar Bragg Grating Theory

A Bragg grating is a periodic variation in refractive index that coherently scatters forward propagating light into a backwards propagating mode; this occurs for a range of wavelengths with centre, or Bragg wavelength λ_{B}, set by the period Λ of the grating via the Bragg equation (Eq.2.1), where n_{eff} is the effective index of the guided mode.

$$\Lambda = \frac{\lambda_{\mathrm{B}}}{2 \cdot n_{\mathrm{eff}}} \tag{2.1}$$

We may model such a refractive index variation in the form of equation 2.2, in which $n_{Waveguide}$ represents the guiding structure. In fibre Bragg gratings, in which the grating is superimposed on an existing waveguide, there is a net increase in the refractive index, modeled by the n_{DC} term – in the case of direct-UV writing used throughout this work $n_{DC} = 0$. The modulation amplitude of the grating structure, $n_{AC}(z)$, may vary with position along the waveguide.

$$n = n_{Waveguide} + n_{DC} + n_{AC}(z) \cdot \cos(2\pi\Lambda z + \phi(z)) \tag{2.2}$$

The spectral shape of the grating's response is given by the Fourier transform of its modulation amplitude; thus a typical uniform Bragg grating has a sinc^2 spectral intensity profile. By tailoring the modulation envelope of a grating we can achieve a range of spectral responses, this is termed *apodisation*. In this work a Gaussian apodisation profile is predominantly used due to its suppression of sidebands, allowing for more efficient use of available bandwidth.

A further possibility is the alteration of the modulation period along its length, which is know as *chirp*. This has the effect of broadening the grating at the cost of reflectivity in addition to introducing spectral dispersion.

2.6.2 Bragg Grating Inscription

The direct grating writing (DGW) system makes it possible to co-pattern waveguides with gratings having programmatically defined properties, without the need for separate phase masks as is traditionally required for fibre bragg grating (FBG) inscription. In the DGW approach, an interference pattern is formed at the focus of the writing spot by splitting and recombining the beam path as shown in figure 2.6. The period of this interference pattern is determined by the angle of the intersecting beams, however, by modulating the interference pattern as it is passed over the sample a range of Bragg grating periods may be built up. The centre of this detuning range is set by the period of the pattern, and therefore the crossing angle of the beams; the interferometer is thus mounted on an interchangeable board, several of which are used to cover different spectral regions of interest. The possible detuning range of the system is governed by the number of periods present in the writing spot; a spot the size of a single period would permit any grating wavelength to be written, while a spot the size of the final grating would only allow for one particular grating wavelength, that of the interference pattern. Here a ~ 5 µm spot is used, corresponding to about seven fringes and thus a detuning range of ~ 300 nm.

The same system can also pattern waveguides by simply neglecting to modulate the interference pattern, causing the modulation to wash out as the sample is translated. Apodisation of the grating may be accomplished by controlling the amount of 'washing out' that occurs as a function of position along the grating.

2.6.2.1 Amplitude-modulation Technique

Initial devices fabricated as part of this work were produced using an amplitude modulation technique with the use of an acousto-optic modulator placed in the beam path. The beam is diffracted out of the writing path in an on-off fashion as the sample is translated, such that the interference pattern is only imprinted when it is phase-aligned

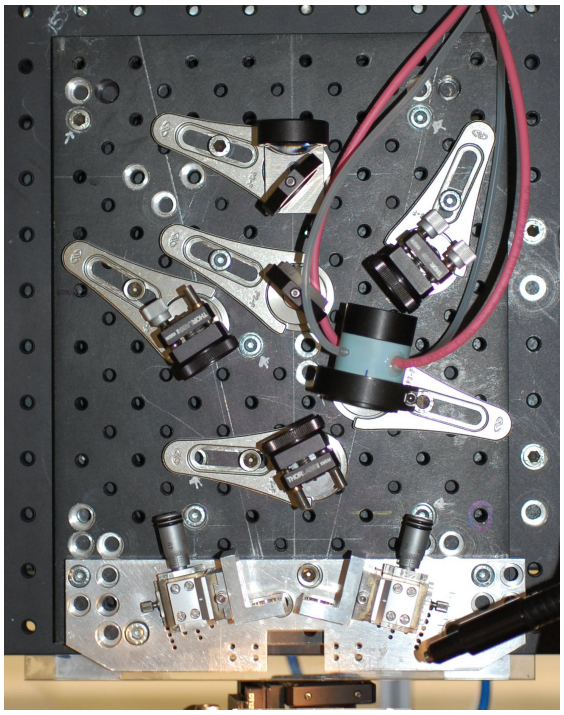


Figure 2.6: Image of the interferometer board of the UV-writing system, designed for 1550 nm operation. An electro-optic modulator (EOM) for phase modulation can be seen in the right-hand arm of the interferometer.

with the sections written previously. Since the sample is now exposed to the beam for a proportion of the time, translation must be slowed to maintain a constant fluence such that waveguide strength is not reduced in the grating region. The control signal for the acousto-optic modulator (AOM) is provided by the position synchronised output (PSO), an output that is hardware synchronised with the translation stage's motion; this helps to ensure phase stability of the inscribed pattern. For the majority of the work carried out, an alternative to this technique was adopted.

2.6.2.2 Phase-modulation Technique

In phase modulation grating writing the AOM is dispensed with and instead an EOM placed in one arm of the interferometer, with the aim of adjusting the phase shift between arms such that the interference pattern is translated between adjacent fringes before jumping back, thereby inscribing a continuous fringe pattern as the sample is translated. This is accomplished by driving the EOM with the output of an integrator, via a high voltage amplifier, reset by the PSO signal [9]. The primary advantage of this approach is that the considerable losses associated with the AOM are avoided, thus more power is available and writing times may be diminished; reduced translation speeds in the grating region are also no longer necessary.

2.7 Spectral Characterisation of Waveguides

Characterisation of fabricated samples under reflection is typically carried out using the experimental setup of figure 2.7. A broadband input spectrum is provided by a fibre-coupled erbium doped fibre amplifier (EDFA) based amplified spontaneous emission (ASE) or SLED source. The reflected spectrum is separated from the input using either a 3-dB coupler or circulator, the former offering a broader bandwidth, and is monitored with an optical spectrum analyser (OSA).

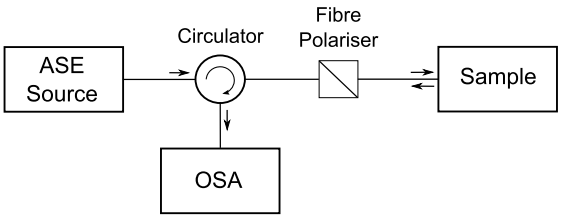


Figure 2.7: The characterisation setup used to measure the reflection spectrum of a sample, either a circulator or 3 db splitter may be used.

Fitting of any Bragg grating peaks in the reflection spectrum for a waveguide may then be used to determine the corresponding centre wavelengths and relative reflectivities. The spectrum is typically normalised to the Fresnel reflection from an unterminated input fibre, known to be 4%.

2.7.1 Loss Measurement

Integrated Bragg gratings also provide an elegant means of measuring the propagation losses of a planar waveguide, developed by Rogers *et al.* [10], without the need to resort to the traditional cut-back techniques common in other waveguide platforms. These cut-back methods involve measurement of the transmission through a set of waveguides of varying length, achieved by successively cutting and repolishing a sample, typically leading to large uncertainties associated with variation in the coupling efficiency.

Measurement of the reflection spectrum of a series of Bragg gratings in both the forward and reverse launch directions permits a ratio to be taken that eliminates the terms resulting from the grating reflectivities, source intensity, and coupling efficiency, to leave a measure of the relative power at each grating. These values represent the average power along the length of the grating and are associated with the midpoint of the grating. Plotting the position-power pairs for a series of gratings along a waveguide and the fitting of a straight line permits the gradient to be extracted, as shown in figure 2.8, representing the propagation loss. The quality of the fit also provides a convenient measure of the uncertainty of the measurement.

This technique is used commonly throughout this work, both in the measurement of propagation loss and in estimating point losses, as seen in chapter 6. Furthermore, a

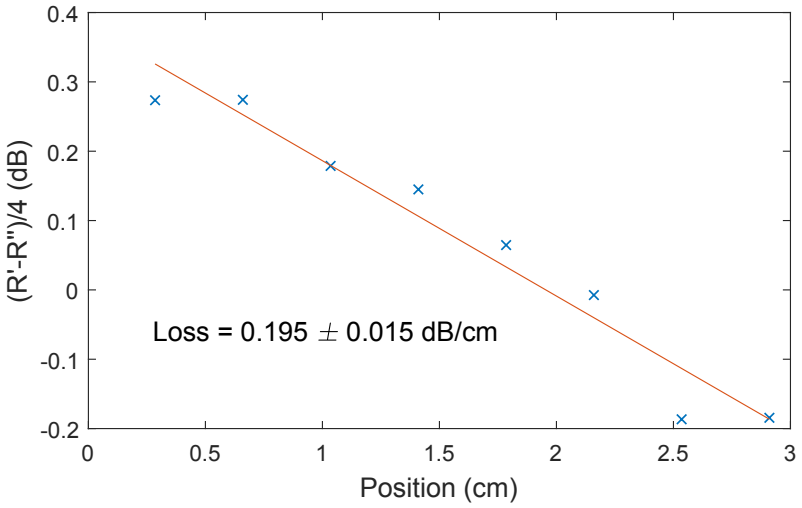


Figure 2.8: An example of the relative power profile obtained using the grating-based loss-measurement technique for a waveguide inscribed in wafer NB86 at a fluence of 14, interrogated under TM polarisation. R' and R" are the peak grating reflections obtained from each of the two launch directions, the gradient of the linear fit is a measure of the propagation loss.

similar approach was used to develop a means of characterising couplers with the use of Bragg gratings, a derivation of which can be found in appendix B.

2.7.2 Layer Birefringence

The stresses resulting from the consolidation process lead to significant layer birefringence, typically of the order of 2×10^{-4}, which plays a key role in the parametric photon sources developed in chapter 3. The magnitude of this birefringence may be measured readily with the use of Bragg gratings; the different effective indices of the TE and TM polarisations leads to Bragg gratings having different centre wavelengths for these two conditions. The reflection spectrum may thus be measured when launching light of each of these polarisations, and the grating centre wavelengths extracted via fitting and used to calculate the effective index values. Errors in this estimate are dominated by the quality of the fit; any misalignment of the input fibre axis or imperfect polarisation extinction will lead to a reflection at the wavelength corresponding to the other polarisation, which may bias this fit.

2.7.3 Dispersion Measurement

Dispersion too may be measured via a Bragg grating approach; gratings may be written for a range of wavelengths limited only by the detuning range of the UV writing system. The centre wavelengths may then be determined from the reflection spectrum and the effective index values for each wavelength computed.

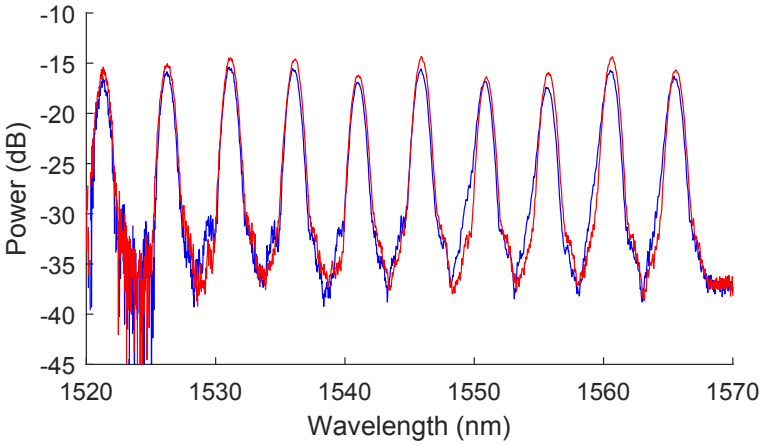


Figure 2.9: Example normalised reflection spectra from a waveguide of wafer NB86 with 10 first-order Bragg gratings, for TE (blue) and TM (red) launch polarisations. The shift in central wavelength of the Bragg peaks provides a measure of the birefringence.

2.8 Coupling and Pigtailing

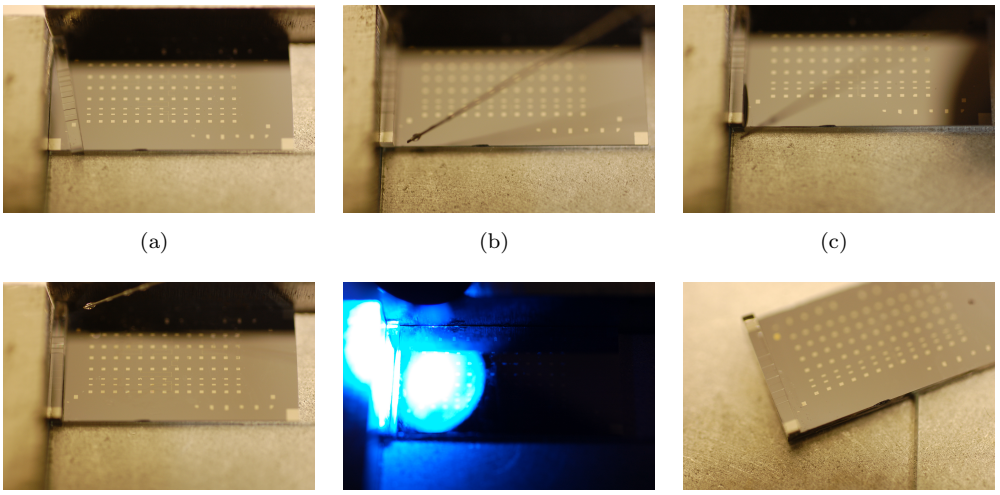
2.8.1 Butt coupling

In the majority of devices throughout this work waveguides were coupled to optical fibre pigtails via butt coupling. This entails the fibre and waveguide facets being placed in contact and aligned with an index matched medium filling any gaps, thereby preventing Fresnel reflections and minimising scattering at the interface. For temporary coupling index-matching oil is used, while for permanent pigtailing a UV-cured optical adhesive is utilised.

Improved pigtail strength and reduced alignment change during curing is achieved by gluing a glass bar to the topside of the facet prior to pigtailing; the process of attaching these strengthening bars is illustrated in figure 2.10. This both increases the gluing surface area and prevents tilting of the pigtail due to asymmetric glue shrinkage, which is particularly important for the chip-to-chip bonding described in chapter 5, as well as the low-temperature on-chip detector devices of chapter 6.

2.8.2 Facet Polishing

In the case of the four-wave mixing experiments of chapter 3, fibre coupling cannot easily be used for the ultrafast pump input since it would lead to both dispersion of the pump pulses and nonlinear generation in the fibre prior to the waveguide, introducing an additional noise source. The former of these could potentially be compensated for but the latter would contribute noise, reducing the source performance. Instead, free-space



(a) (b) (c)

(d) (e) (f)

Figure 2.10: Sequence of steps used to align and glue the strengthening bars above the chip end facets. The bar and chip are aligned to a pair of square plates (a), a bead of glue is then applied (b) and cured using a UV gun (e).

coupling is used, requiring angle polished facets to prevent back-reflections. Polished facets were also found to reduce coupling losses for the butt-coupled modular chips discussed in chapter 5, which were polished flat.

Polishing of silica-on-silicon samples is accomplished by first lapping the samples flat on a Logitech LP-50 using a succession of 6, 3 and 1 µm alumina slurries on cast-iron plates; the process proceeds quickly due to the softness of silicon, making up the majority of the layer. This is followed by a short 4-5 minute polish step with a silica polishing suspension; the length of this step is minimised since it preferentially removes material from the silica layers, leading to curvature on the end-face with excessive polishing.

Samples are mounted for polishing in a clamp mount as a stack with packing chips either side, since chipping tends to occur at the edges of the stack, and bonded with wax. Care was taken to ensure samples were supported on both sides and that the stack protruded from the mount as little as possible, since flexing of insufficiently supported samples can lead to rounding off of the edges during polishing, producing a curved facet that inhibits efficient coupling.

A more specialised polishing approach was developed for the modular work of chapter 5, making use of an Allied Technology Opti-Prep (figure 2.11) with disposable silicon carbide and alumina lapping films of various grits, the recipe is included in section D.4.

Figure 2.11: OptiPrep (Allied Technology) polishing system used for much of the polishing work.

2.9 Conclusion

In this chapter we have seen the range of fabrication techniques available to us in producing UV-written waveguide devices. Typically the procedure involves the production of a wafer via FHD that is then diced into chips, which are UV-written individually and finally polished if necessary. In the next chapter we discuss photon sources based on these waveguides, an invaluable component in integrated experiments, while the following chapters will detail the application of these techniques to the production of further components.

References

[1] J. Snyder, A .W. and Love, *Optical Waveguide Theory*, 1st ed. Springer, 1983.

[2] K. Okamoto, *Fundamentals of Optical Waveguides*, 2nd ed. London: Elsevier, 2006.

[3] L. G. Carpenter, H. L. Rogers, P. A. Cooper, C. Holmes, J. C. Gates, and P. G. R. Smith, "Low optical-loss facet preparation for silica-on-silicon photonics using the ductile dicing regime," *Journal of Physics D: Applied Physics*, vol. 46, no. 47, p. 475103, Oct 2013.

[4] D. Zauner, K. Kulstad, J. Rathje, and M. Svalgaard, "Directly uv-written silica-on-silicon planar waveguides with low insertion loss," *Electronics Letters*, vol. 34, no. 16, pp. 1582–1584, Aug 1998.

[5] M. Svalgaard and M. Kristensen, "Directly uv written silica-on-silicon planar waveguides with low loss," *Electronics Letters*, vol. 33, no. 10, pp. 861–863, May 1997.

[6] C. Holmes, "Direct UV Written Planar Devices for Sensing and Telecommunication Applications," Ph.D. dissertation, University of Southampton, 2009.

[7] M. Douay, W. Xie, T. Taunay, P. Bernage, P. Niay, P. Cordier, B. Poumellec, L. Dong, J. Bayon, H. Poignant, and E. Delevaque, "Densification involved in the UV-based photosensitivity of silica glasses and optical fibers," *Journal of Lightwave Technology*, vol. 15, no. 8, pp. 1329–1342, Aug 1997.

[8] R. Kashyap, *Fiber Bragg Gratings*, 1st ed. San Diego: Academic Press, 1999.

[9] C. Sima, J. C. Gates, H. L. Rogers, P. Mennea, C. Holmes, M. N. Zervas, and P. G. R. Smith, "Ultra-wide detuning planar bragg grating fabrication technique based on direct UV grating writing with electro-optic phase modulation," *Optics Express*, vol. 21, no. 13, pp. 15 747–15 754, Jul 2013.

[10] H. L. Rogers, S. Ambran, C. Holmes, P. G. R. Smith, and J. C. Gates, "In situ loss measurement of direct UV-written waveguides using integrated Bragg gratings," *Optics Letters*, vol. 35, no. 17, pp. 2849–2851, Sep 2010.

Chapter 3

Single Photon Sources

3.1 Introduction

Before any quantum experiments may be conducted it is first necessary to have a suitable source of single photons; this chapter concerns the development of parametric photon sources using UV-written waveguides.

Key features of photon sources for QIP applications include high purity — generation of a photon in a single mode that is not entangled with other elements of the system, and reproducibility — multiple sources must be capable of generating indistinguishable photons [1]. Ideally it is also desirable that such a source produce exactly one photon and that it do so on demand, this is difficult to achieve in practice however.

There are two classes of source currently in use; parametric sources based on spontaneous parametric down conversion (SPDC), FWM or other nonlinear processes, and single-photon emitters based on quantum dots, colour centres in diamond, and atom traps.

3.1.1 Single-photon Source Metrics

When comparing sources there are a number of parameters which are indicative of performance. The first of these, $g^{(2)}(0)$, is the second order coherence function, which provides a measure of the multiphoton emission probability. In the case of a perfect single-photon source we would find $g^{(2)}(0) = 0$, while a value below unity indicates non-classicality.

The true measure of the quality of emitted photons is given by interfering them and measuring the visibility of the resulting HOM quantum interference dip. When two photons are incident on a beamsplitter, with a single-photon detector at each output port, the resulting behavior is dependent on the indestinguishability of their various properties.

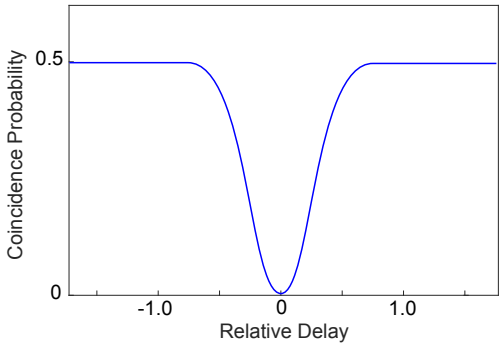


Figure 3.1: Hong-Ou-Mandel (HOM) interference dip resulting from bunching of identical photons at a beamsplitter, where here distinguishability is introduced via a relative delay. The visibility of this dip offers a measure of the quality of photons emitted from a single-photon source.

A means of distinguishing the two photons may be induced with the introduction of a time delay between them. Adjusting the time delay and plotting the detector coincidence count rate produces the characteristic dip of figure 3.1. For identical photons the coincidences will drop to zero due to photon bunching, while any deviation from this value indicates a level of distinguishability between the photons. As the relative time-shift increases they become completely distinguishable and the coincidence count raises to the entirely classical value of 0.5. We define the HOM visibility V as

$$\mathrm{V} = \frac{\mathrm{P_c}(\infty) - \mathrm{P_c}(0)}{\mathrm{P_c}(\infty)}, \tag{3.1}$$

where $\mathrm{P_c}(\tau)$ is the coincidence probability for a relative time delay τ. A further reduction in the visibility will be observed should the individual photons lack purity, that is, should they be described by a mixed state. Any tendency for a source to emit into more than one mode, for example, will yield photons in a mixed state.

A non-zero $\mathrm{g}^{(2)}(0)$ will also adversely affect the visibility, however this quantity may be measured independently via a Hanbury Brown and Twiss (HBT) experiment [2] and its contribution to the visibility accounted for.

Also of great importance is the brightness of the source, the rate of single-photon production. Often the purity and other parameters of a source may be improved at the cost of brightness, through filtering for example, though this increases the runtime of any given experiment.

3.1.2 Coherent light

The most readily available source of single photons is an attenuated coherent laser. The photon number distribution of such a source follows a Poisson distribution as described

by equation 3.2 [1],

$$p\left(n|\alpha\right) = \frac{\left|\alpha^{2n}\right| \exp\left(-\left|\alpha\right|^2\right)}{n!} \tag{3.2}$$

where n is the number of photons and $|\alpha|^2$ is the mean photon number; from which it can be seen that $p\left(2|\alpha\right) = \frac{1}{2}p\left(1|\alpha\right)^2$. The consequence of this is that with sufficient attenuation, $p\left(n > 1|\alpha\right)$ may be made arbitrarily small at the cost of a lower photon rate, allowing a true single-photon source to be approximated in certain situations.

3.1.3 Single-emitter Sources

Single photon-emitters are an attractive approach to photon generation, emitting on demand with high probability and ideally having an inherent zero multi-photon probability ($g^{(2)}(0)$). Perhaps the most well-developed single-emitter sources are quantum dots; these are sufficiently small regions of semiconductor that their band structure becomes discrete levels, between which radiative transitions may occur as in a single atom. Early sources of this type suffered from poor collection efficiency of generated photons; more recently, photonic structures such as cavities and micropillars have been employed to overcome this issue [3], allowing high-quality quantum-dot sources to be produced.

Two key challenges are still faced in the use of quantum-dot sources, the first of these is the difficulty of producing multiple identical sources; the emission wavelength of a quantum dot is set by its physical dimensions which vary significantly due to fabrication tolerances. This can be mitigated somewhat through tuning schemes such as that of Hoang *et al.* in which Stark shifting was used [4]. The second challenge is a consequence of the self-assembly process used in their fabrication, which gives no control over the final location of quantum dots. For this reason the majority of studies have used fluorecence measurements to locate the sites of emission and fabricate the rest of the device at these locations; while sophisticated devices have been constructed in this manner it is difficult to argue that this approach could be scaled to larger numbers of sources.

3.1.4 Parametric Photon Sources

A further commonly used source in QIP experiments makes use of the SPDC process, in which a photon propagating within a material with a χ^2 nonlinearity may be converted into a pair of photons with energies summing to that of the original photon, such that equation 3.3 is satisfied. Typically a nonlinear crystal such as KDP is used as the active medium. The wavelengths of the generated photons, termed signal and idler, are governed by the phase matching conditions; these are the wavelengths for which generation is constructive along the material, permitting a net output.

$$\frac{1}{\lambda_\mathrm{p}} = \frac{1}{\lambda_\mathrm{s}} + \frac{1}{\lambda_\mathrm{i}} \tag{3.3}$$

An important feature of this type of source is that it generates pairs of photons, permitting a heralding technique in which the two photons of each pair are made to take different paths, with one directed to a detector; a detection event in this path will herald the presence of a photon in the other path. The two photons must of course be separable and pure for this scheme to avoid heralding a mixed state. The heralding efficiency of a heralded source represents the probability that an output photon is available given that the herald was detected.

A key potential source of mixedness in the case of heralded parametric sources is spectral correlations between the signal and idler photons. The joint spectra of such a source is displayed in figure 3.2; of note is the circular shape of the central lobe, the widths in the two diagonal axis corresponding to the energy conservation and phase matching conditions, determined by the pump bandwidth and the chip length respectively; this circular profile allows photons to be heralded in a pure state. Also of note are the faint sidelobes in the phase matching axis, these are due to the abrupt termination of phase matching conditions at the ends of the finite-length chip, resulting in a sinc-like profile.

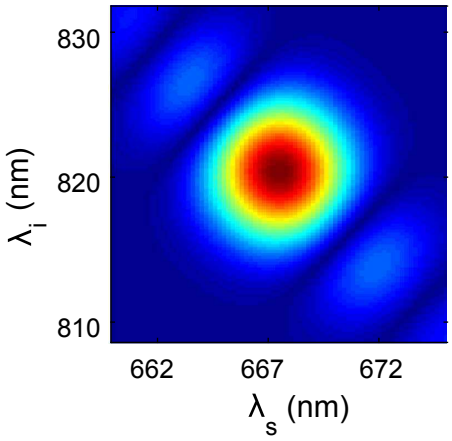


Figure 3.2: Example modelled joint-spectral density of a high-purity FWM waveguide source pumped at 731 nm with a 3 nm bandwidth, adapted from [5].

3.1.5 Source Scaling

A key challenge in scaling to larger experiments with parametric sources is a result of the low emission probability of each source, which must be kept low to avoid generation of multi-photon states. Table 3.1 illustrates the enormous impact this has on experimental runtimes as the number of photons required increases. This necessitates the synchronisation of multiple sources, either requiring a low-loss quantum memory, or a multiplexing scheme using a switchable delay line or similar. In such multiplexing schemes system losses, often dominated by the switching element, make significant count

improvements difficult to achieve in practice; nevertheless, such schemes have shown coincidence probability increases by up to a factor of 6 without additional noise, but with limited purity [6, 7]. Notably, Francis-Jones *et al.* showed all-fibre spatial multiplexing of two high-purity silica photonic crystal fibre (PCF) based FWM sources with a coincidence count improvement by a factor of 1.5 [8].

Table 3.1: Expected duration between multiphoton coincidence counts for a range of device insertion losses and numbers of heralded photons, given a heralding efficiency of 0.7, detector efficiency of 0.9, and repetition rate of 80 MHz.

Loss	3 Photons	4 Photons	5 Photons	6 Photons
0.1 dB	27 ms	3.5 s	7.4 min	16 min
1 dB	50 ms	7.9 s	20 min	55 h
5 dB	790 ms	5.3 min	36 h	560 d
10 dB	25 s	8.8 h	460 d	1600 a

3.1.6 Identical Sources

Relatively little work has yet been conducted by the research community in producing many well-matched sources, that is many sources emitting photons with spatial and spectral overlap sufficient to permit high quality quantum interference between them.

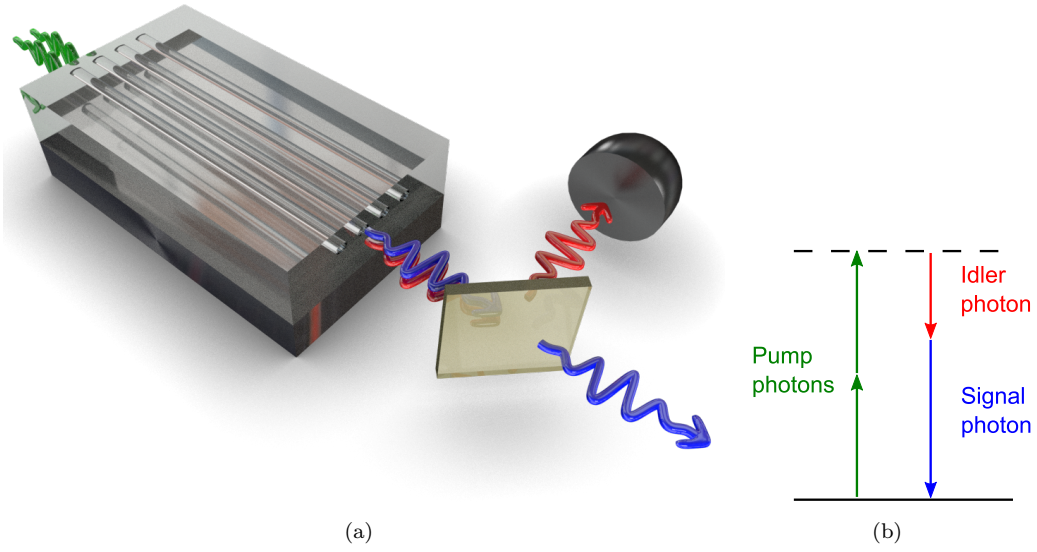
3.2 Birefringence Matched FWM Sources

Birefringence matched FWM in silica is an attractive approach to single-photon generation, due to the potential for excellent mode matching to optical fibre. Such a source has previously been demonstrated in PM fibre [9], where it was found to produce high-purity photons with minimal filtering. Spring *et al.* produced a similar source in an integrated format using a femtosecond written waveguide with a birefringence of 1×10^{-4}, achieving a $g^{(2)}(0)$ of 0.0092 and heralding efficiency of 40% (detector corrected to 80%) [10].

Our efforts here are concerned with producing several such high-quality photon sources, all producing indestinguishable photons. The key challenge here is ensuring each waveguide has the same birefringence. FHD appears to be an ideal material for this task, having an inherent layer birefringence of 2×10^{-4} due to stresses 'locked in' during consolidation, which should be highly uniform across a wafer.

3.2.1 Four-wave Mixing in Silica

Non-degenerate four-wave mixing is a process occurring in materials possessing a χ^3 nonlinearity in which a pair of pump photons are converted into a red-shifted signal photon and a blue-shifted idler photon, as illustrated in figure 3.3. This process must of course satisfy energy conservation, and the wavelengths for which this conversion takes place efficiently are defined by the phase-matching conditions in the material. A significant source of noise in silica FWM is the Raman noise generated either side of the pump, occupying a band of some tens of nanometres. The birefringence must thus be sufficiently high to place the phase-matched signal and idler wavelengths outside of this spectral region. This results in a minimum birefringence requirement of $\approx 2 \times 10^{-4}$, which is in the region of the typical birefringence observed in UV-written waveguides.



(a) (b)

Figure 3.3: Four-wave mixing in silica; two pump photons (green) produce a signal (red) and idler (blue) photon. In the heralding arrangement shown the signal photon is separated from the idler using a dichroic filter and directed to a detector.

3.2.1.1 UV-written Sources

The sources in this work were designed to operate at 780 nm, due to the availability of high-efficiency silicon APDs and a suitably intense pump. Silica has a particularly low χ^3 nonlinearity and as a result high pump intensities are required for significant generation to occur. This is acceptable, however, since the Ti-sapphire pump utilised is capable of supplying over 150 mW of average power; it is also offset by the high purity possible with these sources, allowing strong filtering to be avoided and thus producing a brighter source.

Initial UV-written waveguide sources were found to have an elliptical output mode, which limited fibre coupling efficiencies; this was remedied by a 20% reduction in the spot size of the UV writing system, and thus the lateral waveguide dimension, in turn allowing $> 80\%$ coupling to single-mode fibre to be reached.

Characterisation of these sources was carried out by collaborators at the University of Oxford. A heralded $g^{(2)}(0)$ of 0.03 ± 0.01 was measured at a pump power of 80 mW with 80 MHz rep-rate, for which heralded photons are produced at a rate of ~ 200 kHz. The $g^{(2)}(0)$ may of course be reduced further with weaker pumping, at the cost of a reduced production rate.

3.2.1.2 Fluorescence Features

An additional source of noise was encountered while operating these waveguides, having a broad spectrum and being relatively insensitive to the pump wavelength; these properties are indicative of a fluorescence process, and indeed, the non-bridging oxygen deficiency centre is a reported fluorescence feature in this band [11]. To mitigate the effect of this noise the photon counting electronics were modified to include time gating synchronised with the modelocked pump pulses, ignoring photons outside of a 0.8 ns window [5]. This greatly reduces the significance of the fluorescence photons in most experiments, though the detector is still triggered in this case and thus may pose a problem for detectors with a longer recovery time such as TESs.

3.2.1.3 Birefringence Drift

Upon pumping these sources for long periods of time at average pump powers in excess of 100 mW it was found that the signal-idler separation gradually decreases over time, as shown in figure 3.4. This is a small effect but would reduce the spectral matching between sources if they were pumped for different lengths of time, or if the input coupling varied for example. In locating the cause of this drift, a consideration of the pump wavelength (729 nm) is informative; we find that this wavelength is a multiple of 243 nm, the peak wavelength of the absorption feature targeted by the UV writing process. It is thus highly likely that the ultrafast pump is bleaching this absorption as a three-photon process, thereby changing the waveguide's effective index and birefringence slightly over time. A simple solution to this problem is to operate at a different pump wavelength such that its third harmonic is sufficiently detuned from the absorption. Interestingly, pumping in the complementary polarisation was found to have the opposite effect, although this was only observed in one waveguide and further testing would be necessary to identify the cause of this effect.

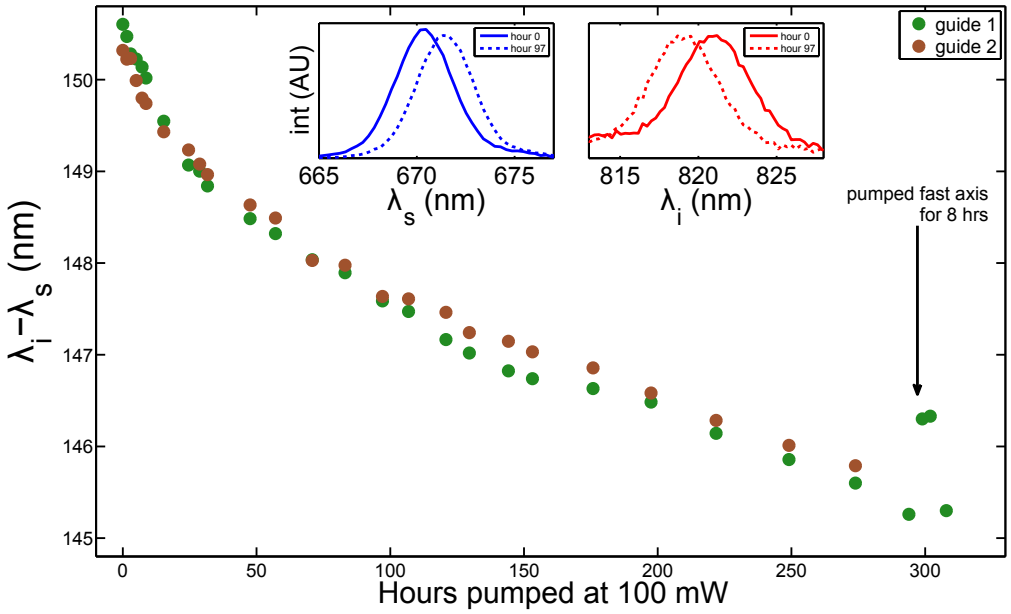


Figure 3.4: Observed drift in the signal-idler separation over time when pumped at 729 nm with 100 mW. Insets show the corresponding shift in signal (blue) and idler (red) spectra.

3.3 FWM Source Arrays

As explained in chapter 1, current quantum optics experiments require a number of well-matched photon sources. To date, few demonstrations of multiple matched sources have been achieved in an integrated format. The high birefringence uniformity of FHD glass makes this approach attractive from a source-matching perspective; efforts were thus made to demonstrate this capability.

In order to investigate the waveguide-to-waveguide uniformity, a device with sets of waveguides at a range of pitches 50–250 µm was produced and characterised. Waveguide groups showed similar variability in all cases, demonstrating similar layer uniformity over these scales. Nevertheless a 50 µm pitch was adopted for these entirely free-space coupled experiments since this enabled multiple adjacent guides to be coupled with a single aspheric objective using multiple beams. Both input and output facets were angle polished to 8° to prevent back reflections which would interfere with the mode-locking of the pump laser, since no isolator was used.

3.3.0.1 Source Uniformity

While the true test of source identicallity is a quantum interference experiment such as HOM, much can be gathered through an examination of the spectral characteristics of output photons. The signal and idler spectra from an on-chip array of 10 sources are shown in figure 3.5(a), from which it may be seen that the sources show excellent

overlap. Examination of the signal and idler separation when launching into each of these waveguides in turn gives us an indication of the birefringence uniformity across the device, any variation along each waveguide appears as broadening in the output spectra. The measured signal-idler separation for an array of 10 FWM sources is plotted in figure 3.5(b), these data corresponding to a calculated birefringence uniformity of 1.3×10^{-7} (standard error).

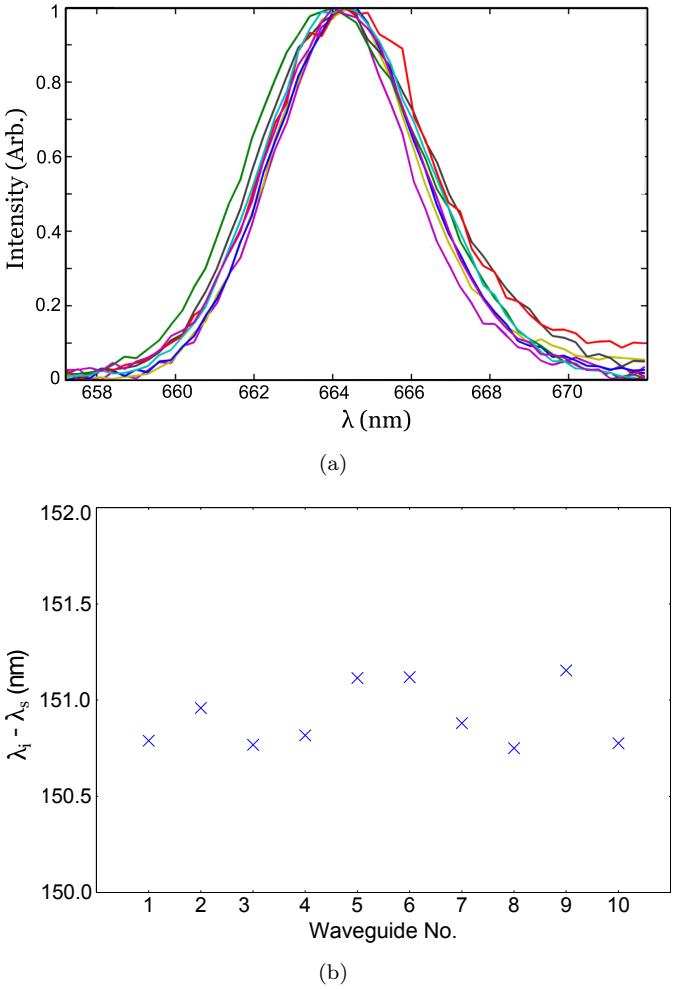


Figure 3.5: (a) Idler spectra and (b) signal-idler separation for an array of 10 FWM source waveguides with a 50 µm spacing.

3.3.1 Nonclassical Interference Measurements

While the spectral overlap of these sources is excellent, the true measure of their indestinguishability is given by interfering them and measuring the visibility of the resulting HOM dip. Pairs of sources were thus interfered using the setup shown in figure 3.6; femtosecond pulses are spectrally filtered using a grating and slit before being split and focussed into two waveguides using a single objective, with a delay line in one path. Output light is collected again with a single objective and the signal and idler separated

via a dichroic filter. The remaining pump light is suppressed using angle-tuned band-pass filters before each beam is coupled into a fibre and the idlers interfered at a 50-50 fibre coupler; detection is via a set of fibre-coupled silicon APDs.

Figure 3.7 presents the measured HOM visibilities for pairs of sources in a group of five, both raw and background subtracted. In each case two different filtering arrangements were tested, a loose filter giving a mean background subtracted visibility of 0.836 ± 0.019 (0.807 ± 0.018 raw) and a tighter filter selected to remove the sidebands, which raised the mean background subtracted visibility to 0.95 ± 0.024 (0.919 ± 0.023 raw). In each case these values are very close to the expected maximum, represented by a dotted line in figure 3.7, indicating that these sources are indeed well matched. This theoretical maximum is limited by the angular deviation of the beams since a single objective and filter are used for both.

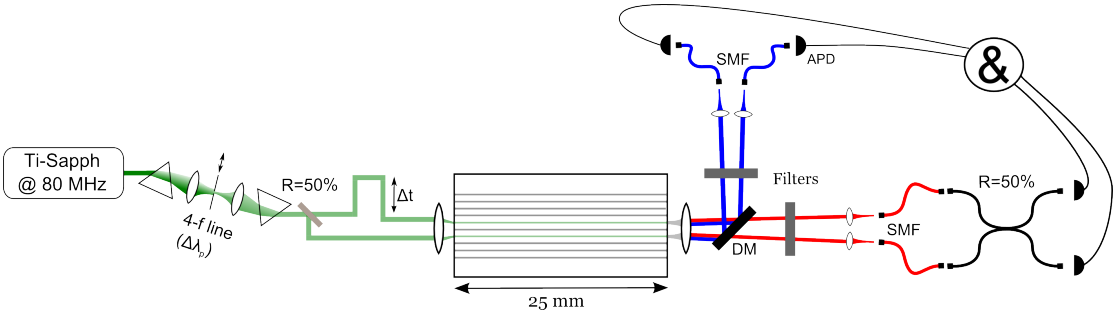


Figure 3.6: Experimental setup for nonclassical interference measurements with pairs of sources from an on-chip array fabricated by the author. A dichroic mirror is used to separate signal and idler beams, each of which is filtered to remove the pump. The filtered signal and idler beams from each source are then fibre-coupled, signal photons proceed to APDs for detection as heralds, while the two idlers are connected to a 3 dB coupler. Coincidences of the four detectors are counted as a function of the variable delay Δt. Reproduced from [12].

The excellent visibilities observed for these sources, coupled with their high brightness, enabled heralded three-photon interference experiments to be carried out using this array. This required six-fold coincidences, which were observed at a rate of 0.4 Hz [12].

3.3.2 Birefringence tuning

The birefringence of UV written waveguides is predominantly determined by the inherent layer stress present in the FHD wafer, resulting from the elevated consolidation temperature and subsequent cooling described in chapter 2. Since the consolidation temperature is controlled by the dopant concentration in the glass while the layer index is determined by the ratio of boron to germanium, these two parameters may be adjusted independently. Thus a higher consolidation temperature, higher stress, glass may be produced with the same layer index and modal properties by adjusting the FHD

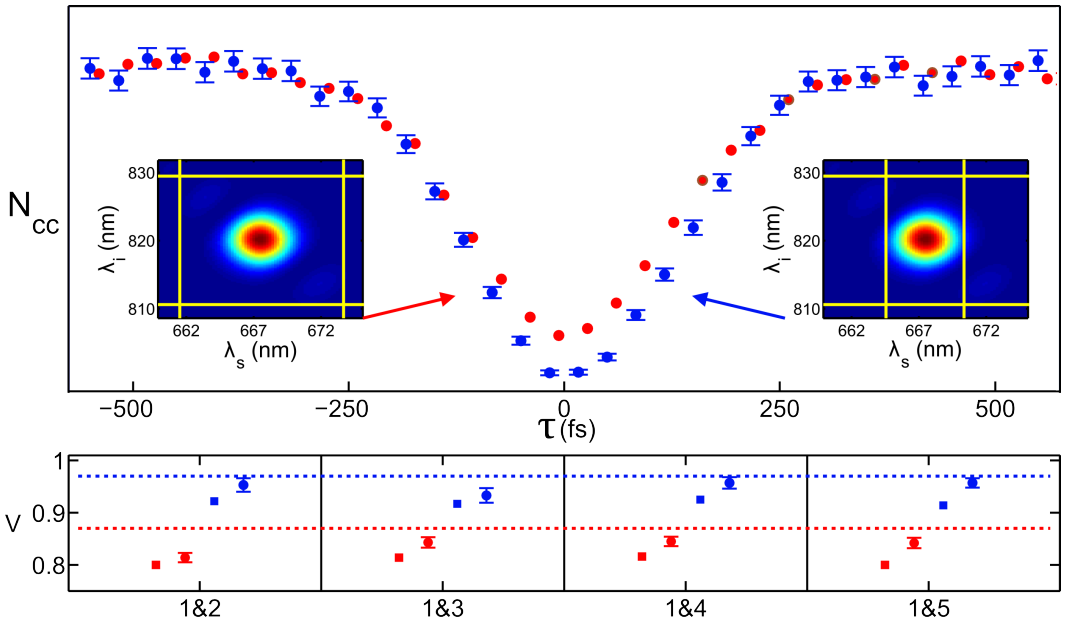


Figure 3.7: Nonclassical interference measurements conducted by Justin Spring at the University of Oxford with pairs of sources from an array fabricated by the author at Southampton, for cases of weak (red) and modest (blue) filtering. The lower plot presents the measured HOM interference visibilities for pairs of sources within a set of five, square points being the raw data while circles show the background subtracted values. The dashed lines represent the maximum expected visibilities for the experimental setup.

dopants. This offers the possibility of producing a wafer with much higher birefringence, of the order of 3.5×10^{-4}, capable of a very wide signal-idler separation and able to produce photons at telecommunications wavelengths.

3.3.3 Telecom-band FWM Source

With a sufficiently high layer birefringence it is possible to produce signal and idler photons at 780 nm and 1550 nm respectively, with a pump at $\sim$ 1060 nm. This arrangement is attractive since it permits the use of convenient and efficient Si APDs to herald photons in the low loss window for silica, where experiments would ideally take place. Figure 3.8 shows the idler spectrum for one such chip, pumped at 989 nm.

In the initial device of this type heralding efficiency was limited by the out-coupling efficiency of the idler. Here the three broadly spaced operating wavelengths dictate that a compromise must be made in the choice of waveguide dimensions; ideally the waveguide would be single mode at all wavelengths however this leads to an output mode for the idler that is poorly matched to the output fibre. Further efforts are required to determine the optimum waveguide parameters to improve this value. These higher birefringence chips also offer a means of mitigating the pump filtering requirements in a multi-chip integrated source, as we shall now see.

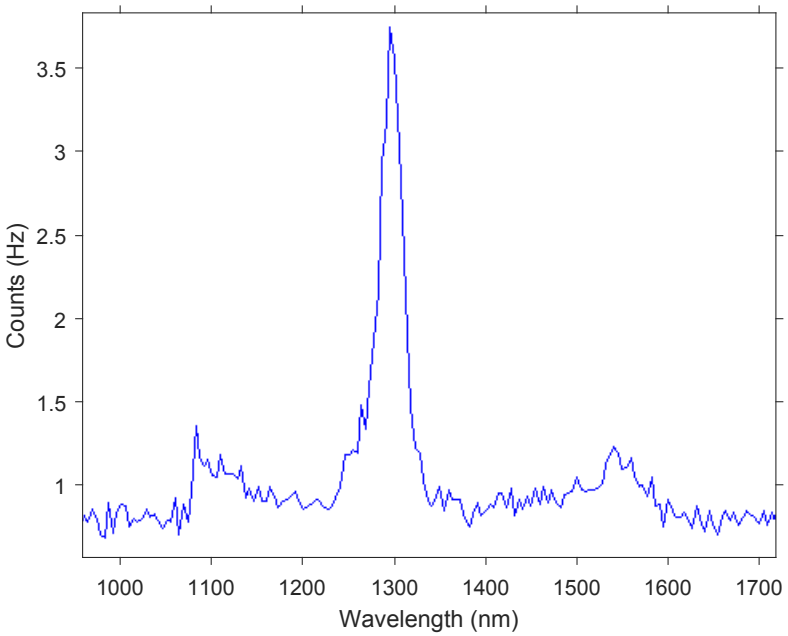


Figure 3.8: FWM idler spectrum from a high-birefringence chip pumped at 989 nm.

3.4 Multi-chip FWM sources

The ability to produce two wafers with significantly different birefringence values and yet similar mode profiles affords the possibility of providing simplified integration of FWM array sources with other components, without the need for > 100 dB level pump attenuation. Such a system may be composed of separate source and network chips; the former fabricated of a wafer with suitable birefringence to produce photons at the target wavelength, while the latter may be produced using a sufficiently different birefringence wafer for any generated photons to be out-of-band. While filtering would still need to occur prior to detection in this case, it could be carried out after the network at a stage where the outputs have been fibre-coupled for detection. This avoids the need for a free space optics stage between the sources and network. Furthermore, the multiple input launches may be replaced by a one-by-N splitter chip, again having a 'detuned' birefringence, further simplifying the free-space optics requirements. A schematic of such an arrangement is shown in figure 3.9.

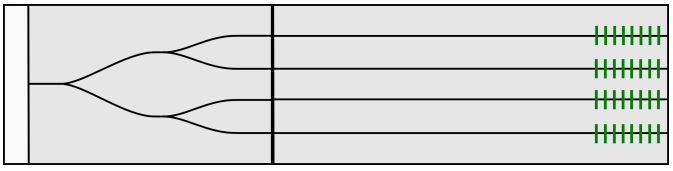
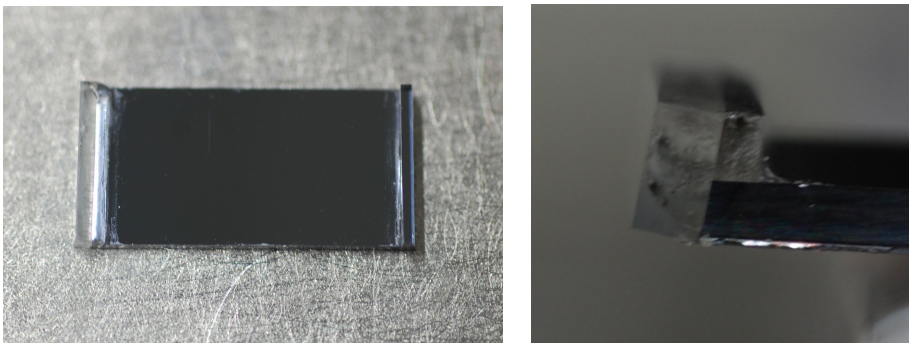


Figure 3.9: Schematic of a proposed multi-chip integrated source array, with a splitter chip of different birefringence for pump distribution, and an end cap for power management.

For this to be implemented it must be possible to bond the chips together in a means that will survive the $\sim$ 100 mW, 100 fs pump pulses expected. Ideally, a refractive-index-matched UV adhesive in the optical path would be used here, preventing Fresnel reflections at the facets, however, this is likely to be damaged by the pump pulses; alternatives include bonding the edges of the chips, requiring AR coatings on the facets, and possibly fusion splicing.



(a) (b)

Figure 3.10: Glue damage-threshold test chip, with an end cap glued onto one of the 8° angle polished facets.

In order to test the damage threshold of the UV glue used, a float-glass cap was glued onto an 8° polished input facet of a source chip, having an array of 16 waveguides at a spacing of 250 µm—this device is shown in figure 3.10. Pump light was coupled into the chip and the transmitted light collected and monitored at increasing pump powers in two different launch configurations, having the capped or uncapped side as input. In the capped input configuration, transmission was constant up to a power of 150 mW, at which point the transmission dropped off over a time period of several seconds, corresponding to charring of the glue layer. In the uncapped input case break-down occurred at a pump power of 220 mW, at which point the transmission broke down over a much longer timescale of minutes. This is believed to be associated with the damage threshold for the FHD facet, rather than the glue layer on the output side, since no charring of the glue layer was visible and attenuation of the pump would lead to an output power less than the 150 mW threshold established in the previous test.

This suggests that for the expected single waveguide pump powers of $\sim$ 100 mW the separate splitter chip could indeed be glued to the source chip, but the end-cap at the splitter input would need to be bonded by some other means such as fusing; further experiments are required to develop a suitable bonding scheme.

3.5 Quasi-Phase Matching

Quasi phase matching provides an alternative phase matching scheme to birefringence phase matching, permitting control over the signal and idler separation without the need to vary the layer birefringence. In this approach, periodic domains introduced in the material provide an additional k-vector, resulting in phase-matching of an otherwise inefficient process with the correct choice of poling period.

This approach could potentially allow for a more controllable and repeatable phase matching scheme, simplifying the creation of identical sources on the same device, or on different chips, when compared with the birefringence matched case.

3.6 Poling of Silica

Thermal poling is a well known technique capable of producing a χ^2 non-linearity in silica, largely due to charge separation[13]. A related technique, UV-assisted poling, has been shown to produce surprisingly high χ^2 coefficients in both germanosilicate fibre [14] and bulk glass [15]. Furthermore, electro-optic coefficients as high as 12.5 $\mathrm{pm \cdot V^{-1}}$ have been demonstrated [16] in sputtered germanosilicate films with an applied poling field of $\sim 1 \times 10^5$ V. In all cases the resulting nonlinearity is not stable however, and decays over a period of some tens to hundreds of days; although decay time-constants have been shown to increase to several years through hydrogen loading [16]. This suggests that a similar approach should be possible with a planar FHD substrate.

3.7 Poled UV Writing of Silica

It is known that the UV writing process produces significant local heating within the glass, thus with the application of an external field it may be possible to pole silica during the UV writing process. In this way periodic poling may be achieved with the use of only two electrodes, since the field may be applied to the entire device and its polarity reversed in synchronisation with the writing rate to achieve the desired poling period.

This scheme does require that the waveguide be written through the top contact, as illustrated in the schematic of figure 3.11, however this should be possible with a sufficiently thin film and the correct choice of material. Gold was selected for the top contact, since previous work by the group had suggested it to be partially transparent at 244 nm. When depositing this contact a border (> 1 mm) was masked off around the sample to ensure a breakdown voltage exceeding 3 kV. The silicon substrate is a suitable bottom contact in this case, a side connection to this was chosen to avoid removal of

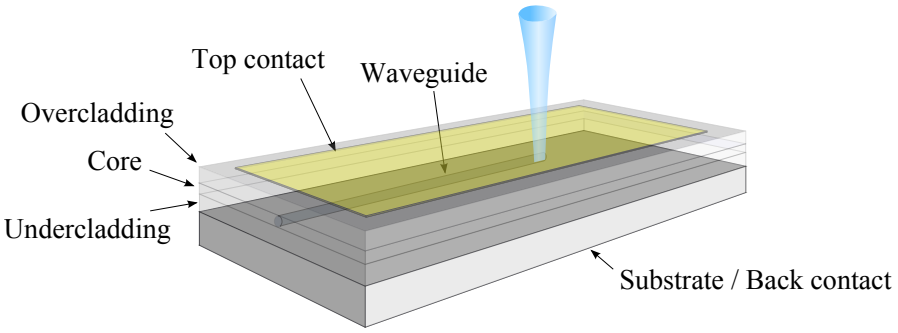


Figure 3.11: Diagram of the poled UV writing approach.

the thick thermal oxide; the surface was cleaned and a conductive silver paste applied to prevent oxidation. For this technique an insulating chuck was made to hold the sample by means of a vacuum during writing, having contacts at the top and side for connection to the sample.

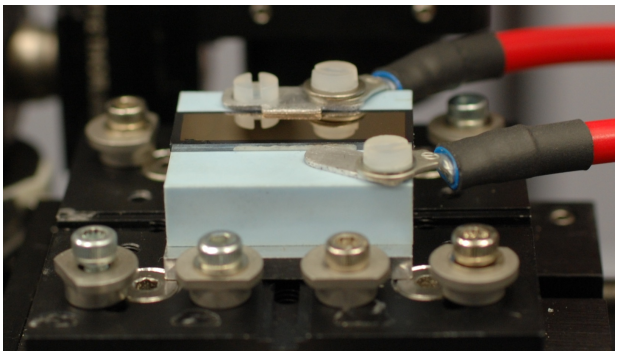


Figure 3.12: Image of the insulating chuck produced to hold the sample and provide the necessary connections during the UV-writing process.

3.8 Towards Quasi Phase Matched Sources

While this approach could ultimately be used for phase matching a range of nonlinear processes, in order to simplify initial testing phase matching of a SHG process at 1550 nm was chosen, since this may readily be tested for with the use of a germanium photodetector and 1550 nm femtosecond source which were available. The required poling period for phase matching may be calculated simply through consideration of the material refractive index at the signal and idler wavelengths, obtained via an appropriate Sellmeier equation. For initial testing, the Sellmeier coefficients extracted for a similar wafer composition were utilised [17], since these do not vary significantly for the types of composition used. The required period for this process was thus calculated to be 66.8 µm.

A 12 nm thick gold top electrode was deposited on a test chip, with a 2 nm chromium adhesion layer, which was then hydrogen loaded. Connections were made to a high

voltage amplifier, controlled via the analogue Position Synchronised Output (PSO) of the UV-writing system. A set of waveguides were inscribed, at fluences of between 12 and 100 $\mathrm{kJ \cdot cm^{-2}}$, with a position synchronised square wave of period 60 µm and peak voltage of between 500 V and 3 kV applied across the contacts, corresponding to a field of $1.25–7.5 \times 10^7\ \mathrm{V \cdot m^{-1}}$ across the ~ 40 µm of silica.

Characterisation of the device revealed a failure of guidance in the waveguides however. An explanation for this was found from measurements of a test gold film deposited on a silica slide at the same time as the top contact. The transmission through this film at 244 nm was measured to be only 18%, after accounting for the loss in the silica.

This issue may be solved with the use of an alternative top contact material with better transmissivity at 244 nm; indium-tin oxide (ITO) should provide adequate conductivity while increasing the transmission to an acceptable level. Alternatively, the edge of the contact region may be detected, through monitoring of the back-reflection, and the fluence increased to compensate for the measured transmission so as to produce a waveguide without a significant discontinuity.

3.9 Conclusion

Single-photon emitters can provide on demand photons in a compact format, however, significant fabrication challenges prevent the production of arrays of identical sources at present. While ultimately this approach may win-out for large systems, at present parametric sources provide a means to access new science at the few to tens of photons level. FWM sources in UV-written silica offer high purity and excellent mode matching to fibre, and crucially we have shown that an array of these sources may be fabricated to produce identical photons. Tuning of the FHD layer birefringence has enabled chip-based heralded sources at both 800 nm and 1500 nm to be produced; the former of these has been demonstrated to provide a low $g^{(2)}(0)$ and high-visibility quantum interference, while in the latter case the source has yet to be fully characterised. Initial work in further integrating these sources has been carried out, with the aim of distributing the pump on-chip to reduce the number of free space couplings, though this has not yet been accomplished.

Some progress has been made towards poled QPM silica photon sources via a combined UV writing and poling technique, though this system is as yet untested. In particular, it is not clear whether the resulting sources will be sufficiently reproducible, since unpredictability in the induced nonlinearity was found to be the primary difficulty in similar UV poling work in fibre; should this method be successful however, it would provide a means of including photon sources in the FHD platform with greater control.

References

[1] B. W. Kok, Pieter; Lovett, *Introduction to Optical Quantum Information Processing*. New York: Cambridge University Press, 2010.

[2] M. Fox, *Quantum Optics: An Introduction (Oxford Master Series in Physics)*. Oxford University Press, 2006.

[3] P. Senellart, G. Solomon, and A. White, "High-performance semiconductor quantum-dot single-photon sources," *Nature Nanotechnology*, vol. 12, no. 11, pp. 1026–1039, Nov 2017.

[4] T. B. Hoang, J. Beetz, M. Lermer, L. Midolo, M. Kamp, S. Höfling, and A. Fiore, "Widely tunable, efficient on-chip single photon sources at telecommunication wavelengths," *Optics Express*, vol. 20, no. 19, pp. 21 758–21 765, Sep 2012.

[5] J. B. Spring, "Single Photon Generation and Quantum Computing with Integrated Photonics," Ph.D. dissertation, University of Oxford, 2014.

[6] F. Kaneda, B. G. Christensen, J. J. Wong, H. S. Park, K. T. McCusker, and P. G. Kwiat, "Time-multiplexed heralded single-photon source," *Optica*, vol. 2, no. 12, pp. 1010–1013, Dec 2015.

[7] C. Xiong, X. Zhang, Z. Liu, M. J. Collins, A. Mahendra, L. G. Helt, M. J. Steel, D. Y. Choi, C. J. Chae, P. H. W. Leong, and B. J. Eggleton, "Active temporal multiplexing of indistinguishable heralded single photons," *Nature Communications*, vol. 7, p. 10853, Mar 2016.

[8] R. J. A. Francis-Jones, R. A. Hoggarth, and P. J. Mosley, "All-fiber multiplexed source of high-purity single photons," *Optica*, vol. 3, no. 11, pp. 1270–1273, Nov 2016.

[9] B. J. Smith, P. Mahou, O. Cohen, J. S. Lundeen, and I. A. Walmsley, "Photon pair generation in birefringent optical fibers," *Optics Express*, vol. 17, no. 26, pp. 23 589–23 602, Dec 2009.

[10] J. B. Spring, P. S. Salter, B. J. Metcalf, P. C. Humphreys, M. Moore, N. Thomas-Peter, M. Barbieri, X.-M. Jin, N. K. Langford, W. S. Kolthammer, M. J. Booth, and I. A. Walmsley, "On-chip low loss heralded source of pure single photons," *Optics Express*, vol. 21, no. 11, pp. 13 522–13 532, Jun 2013.

[11] L. Skuja, "Optically active oxygen-deficiency-related centers in amorphous silicon dioxide," *Journal of Non-Crystalline Solids*, vol. 239, no. 1, pp. 16 – 48, Oct 1998.

[12] J. B. Spring, P. L. Mennea, B. J. Metcalf, P. C. Humphreys, J. C. Gates, H. L. Rogers, C. Söller, B. J. Smith, W. S. Kolthammer, P. G. R. Smith, and I. A. Walmsley, "Chip-based array of near-identical, pure, heralded single-photon sources," *Optica*, vol. 4, no. 1, p. 90, Jan 2017.

[13] S. Fleming and H. An, "Poled glasses and poled fibre devices," *Journal of the Ceramic Society of Japan*, pp. 1007–1023, 2008.

[14] T. Fujiwara, D. Wong, Y. Zhao, S. Fleming, S. Poole, and M. Sceats, "Electro-optic modulation in germanosilicate fibre with UV-excited poling," *Electronics Letters*, vol. 31, no. 7, p. 573, Mar 1995.

[15] T. Fujiwara, M. Takahashi, and A. J. Ikushima, "Second-harmonic generation in germanosilicate glass poled with ArF laser irradiation," *Applied Physics Letters*, vol. 71, no. 8, pp. 1032–1034, 1997.

[16] J. Khaled, T. Fujiwara, and A. J. Ikushima, "Optimization of second-order nonlinearity in UV-poled silica glass," *Optical Materials*, vol. 17, pp. 275–278, Jun 2001.

[17] H. L. Rogers, C. Holmes, J. C. Gates, and P. G. R. Smith, "Analysis of Dispersion Characteristics of Planar Waveguides via Multi-Order Interrogation of Integrated Bragg Gratings," *IEEE Photonics Journal*, vol. 4, no. 2, pp. 310–316, Apr 2012.

Chapter 4

Phase shifters and Modulators

4.1 Introduction

A key component of integrated quantum circuits is the phase shifter, which permits configuration of the circuit through manipulation of both the phase and, in combination with a splitter, the intensity. Typically, phase shifters in silica make use of either the thermo-optic effect or the electro-optic Pockels effect [1], another possibility being the stress-optic effect. The most developed of these for the silica-on-silicon platform is the thermo-optic approach, which has been used previously by the group to produce the active elements of two and three photon quantum circuits [2, 3]. In this previous work it was found that the drive currents required by these devices, their failure rate, and their large physical size would be prohibitive in more complex circuits. This chapter details advances made to these components, as well as conceptual design work on alternative phase shifters for use at low temperature.

4.1.1 Regimes of operation

There are two distinct applications of phase-shifters in quantum optics experiments, distinguished primarily by the bandwidth of the modulator; these are circuit configuration and fast feed-forward. In the former of these modes, the modulator performs the reconfiguration necessary to both setup the input state and probe the output state. This configuration is then held for a period of time while sufficient detection events are collected; as a result the modulator need not be fast and a bandwidth of kilohertz is ample. In the latter mode of operation the aim is to detect photons from within a network and perform some alteration of the network forward of this point, requiring both high-speed detectors and high-bandwidth (GHz) modulators such that the time required to make the change is shorter than the flight time of the photons in the network; this is exceedingly difficult to accomplish. A further use of fast modulators is in frequency

shifting photons by applying a phase-ramp modulation, which could permit frequency encoding of qubits, but again, this would be very challenging in an integrated format at present. As a result, we restrict ourselves here to slow modulators for configurational purposes.

4.2 Amplitude Modulators

Amplitude modulators in planar circuits are typically implemented with a Mach-Zehnder interferometer [1], composed of two couplers, with a phase shifter on one arm as shown in figure 4.1. This design may be improved with the addition of a second phase-shifter in the other arm and operating both at their mid-point; for thermal devices this results in a constant power dissipation at all modulation points in the network independent of setting, helping to reduce crosstalk effects as we shall see in section 4.3.2.3. This also provides redundancy in the case of a manufacturing defect or failure of one of the elements. The use of push-pull elements is common in electo-optic modulators, but little evidence is found of this in thermo-optic devices; Chaboyer *et al.* place heaters on both arms of their MZIs but only drive them one at a time [4].

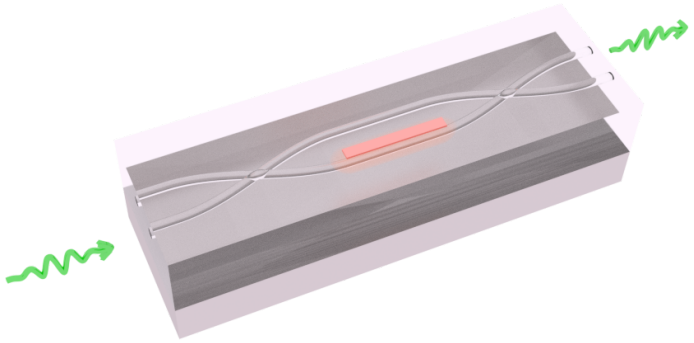


Figure 4.1: Diagram of a Mach-Zehnder amplitude modulator based on a thermal phase shifter in combination with a pair of 50:50 couplers.

The aim of this segment of work is ultimately the production of larger quantum circuits from identical configurable elements, in order to both simplify the fabrication process and permit a wider range of experiments to be carried out using the same device.

4.2.1 Cross couplers

Cross-couplers were selected over directional couplers here due to their larger bandwidth and simpler design [5]; in particular, a compact version of the cross-coupler [6] making use of a double s-bend was utilised. The coupling ratio of a coupler of this type is determined by two parameters, these are the angle of the crossing, and the effective index within this region. In previous UV-written devices of this type coupling ratios have been measured

by fibre-coupling the two output ports and measuring the transmitted power, which is subject to variation in the coupling efficiency at these ports. With the addition of gratings in all arms of a coupler it is possible to determine the coupling ratio and excess loss of a coupler independent of its facet losses. This is done by launching into each port in turn and recording a reflection spectrum, by ratioing the fitted peak heights from the different launches the required parameters may be extracted in a manner akin to the grating based loss measurement technique [7]. The complete approach is detailed in appendix B.

4.3 Thermo-optic Phase Shifters

Thermo-optic phase shifters exploit the variation in refractive index with temperature of the wave-guiding material, in this case silica. A heating element is placed in proximity with the waveguide, the resulting localised temperature increase alters the refractive index and thus the optical path length, producing a phase shift of the guided mode. Modulators of this sort were first used in a quantum optics context in 2009 [2] and have become standard in devices since then. Their ubiquity in this field is principally due to their minimal impact on device losses, as well as their simplicity and reliability.

While this type of phase shifter is well developed commercially [8], previous devices used by the quantum optics community have required significant input power during operation. For the purposes of producing more complex and highly configurable circuits, having many more phase shifters, it was desirable to improve the performance of these devices. To this end, numerical modelling of the devices was conducted to further optimise their design.

In this work we make use of nichrome (Ni80/Cr20) as the resistive material, for its resistivity permits convenient resistance values to be achieved with reasonable dimensions; it provides a low temperature coefficient of resistivity, has excellent oxidisation resistance, and can be deposited via evaporation.

4.3.1 Thermo-optic Effects in Silica

The thermo-optic effect in silica is comprised of two components, a temperature dependance of refractive index and thermal expansion of the medium. Since heating in this case is only local, expansion is constrained to the region immediately below the heater; this will also create a region of strain surrounding the heater.

4.3.2 Device Modelling

In an effort to optimise the device geometry a FEM model was constructed using COMSOL, allowing the temperature profile within the device to be computed in the presence of different heating conditions.

4.3.2.1 Model Parameters

A 2D heat transfer model was used initially to minimise processing time; this included a heating element with a specified heating power, the three silica layers, and the silicon substrate. The back face of of the silicon was held at a fixed temperature of 21°C, which may be accomplished in a real device by mounting it on a water cooled heat-sink or peltier. The surrounding air was modelled as a fluid with open boundaries under the effect of gravity, allowing convective cooling to be included.

4.3.2.2 Efficiency Improvement

The modelled temperature profile for the device designs used previously, a 50 µm heater with a thickness of $\sim$ 200 nm, with a heating power of 0.4 W and length 1 mm, is displayed in figure 4.2(a). It can be seen that the temperature profile extends to approximately 50 µm either side of the waveguide, placing a limit on the proximity of adjacent devices without excessive crosstalk. It was also found that a significant temperature gradient is produced across the core region, raising the question of whether the resulting strain profile gives rise to additional birefringence.

For the purposes of optimisation, the temperature within the core region is taken as an indication of the resulting phase shift, which should be a good approximation, although the strain optic component of the change will not necessarily be proportional to this value. Clearly this temperature may be increased for the same heating power by placing the heater closer to the core layer, i.e. reducing the over-cladding thickness. The computed average core temperature for a range of cladding thicknesses is displayed in figure 4.3; the minimum thickness was taken to be 7 µm since a cladding much thinner than this would produce a mode with power at the surface, which is undesirable. Reducing the overcladding thickness also increases the core temperature gradient, as would be expected, though not considerably. The temperature range varies from 37 K to 45 K as the cladding thickness is reduced from 17 µm to 7 µm.

With the hopes of further improving the device efficiency, a narrower 20 µm heater was tested; this was chosen as the minimum device width after consideration of the waveguide dimensions, in order to ensure that heating accross the waveguide is uniform. This concentrates the heating in a smaller region around the core, as shown in figure 4.2(b),

thus reducing the required alignment tolerance, though not to the degree that it becomes overly challenging. As can be seen, a higher core temperature may be reached in this way for the same input power, with a total improvement of 47% for a 7 µm overcladding layer.

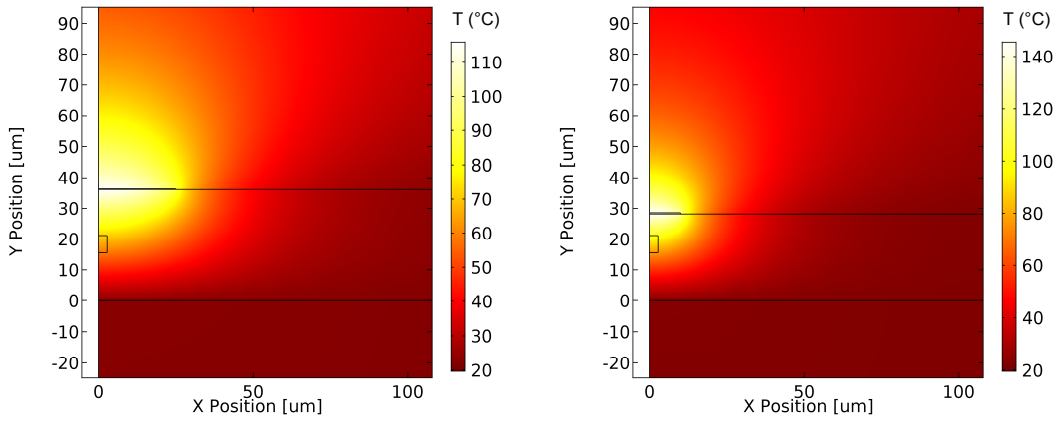


Figure 4.2: (a) Modelled temperature profile of a 0.4 W microheater of the initial design, 1.5 mm×50 µm with 15 µm overcladding thickness. (b) An optimised design, 1.5 mm×20 µm with 7 µm overcladding, under the same conditions.

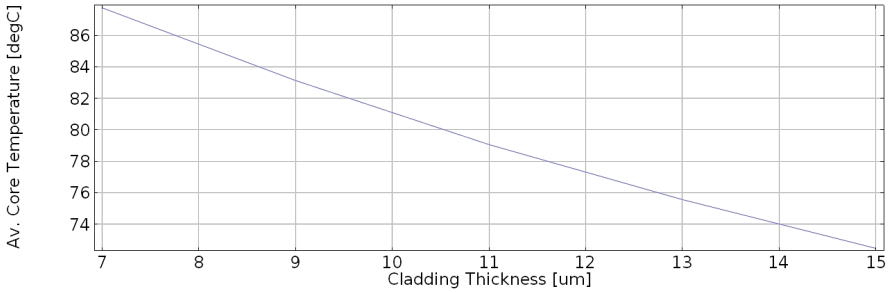


Figure 4.3: Average core temperature as a function of overcladding thickness for 50 µm heater.

It was also found that even with only a thin silica layer no appreciable temperature gradient is produced in the silicon, due to its high thermal conductivity. This suggests that by increasing the undercladding thickness, further improvements in the efficiency may be obtained; this comes at the cost of a slower temporal response, but for a circuit configuration application this is of little importance. The primary obstacle in this approach is the difficulty in further increasing the thickness of the thermal oxide layer, since the growth time of a 17 µm layer is already several weeks. Alternatively, an FHD undercladding may be added; this has been accomplished before, but does create the difficulty of adjusting the consolidation temperatures to avoid significant diffusion of dopants out of the core layer.

A further possibility is the complete removal of the silicon layer through machining or etching, which can greatly increase the core temperature and device efficiency as

demonstrated in [9]. Accomplishing this for multiple phase shifters, however, without also compromising the heat-sinking ability of the substrate, would be challenging.

An alternative approach to increasing the achieved tuning range for the same driving voltage is to place heaters in both arms of the MZI, operated in complement. As mentioned previously, this push-pull configuration has a number of benefits in terms of thermal crosstalk; this will be investigated in the next section.

4.3.2.3 Thermal Crosstalk

The dual heater configuration reduces crosstalk not only by way of its reduced operating voltage, but also because the total power delivered by the pair remains constant for all settings, which becomes more significant for couplings beyond nearest-neighbor. Modelling carried out of a set of five heaters spaced 127 µm apart in both single-heater and dual-heater modes illustrates the benefits of this approach. In this model the thermal sinking of the chip is significant; optimistic heatsinking parameters are used, corresponding to a large thermal mass coupled via a thin (100 µm) layer of high conductivity thermal paste (1.4 W/m/K). Results suggest a factor of 10 reduction in the temperature perturbation of the adjacent waveguide in the dual heater case, and thus a corresponding reduction in crosstalk.

4.3.3 Fabrication

In fabricating these devices a lift-off process was used, in which the substrate is spin coated with a positive resist which is patterned via photolithography, as shown in figure 4.4. After developing the resist, the nichrome layer is deposited through e-beam evaporation and the sample soaked in acetone to remove the resist, along with the excess metal [10].

During initial fabrication of these elements it was found that significant stress was present within the deposited nichrome layer, leading to poor adhesion to both the photo-resist and substrate. An attempt was made to reduce layer stress through a reduced deposition rate, as well as heating the substrate to avoid significant temperature change during deposition; though neither of these approaches had the desired effect. It was found that the addition of a ~ 5 nm chromium or titanium layer prior to the nichrome deposition acted as a stress relief layer and improved adhesion significantly.

In the case of the 20 µm elements, the additional thickness required to provide the same resistance as a similar 50 µm element did lead to difficulties during the lift-off process; deposition on the sidewalls of the resist prevented adequate access of the solvent to the unexposed resist, as well as creating rough edges in the areas in which the lift-off was

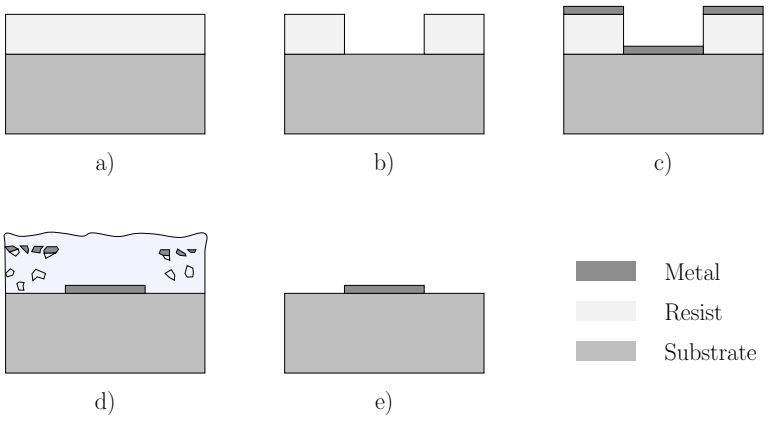


Figure 4.4: Diagram of the lift-off process stages, a) spin coating, b) patterning, c) deposition, and d) lift-off.

successful. To remedy this, a thicker ~ 2.0 µm resist recipe was used rather than the ~ 1.2 µm used previously, and a chlorobenzene soak was used prior to development; this causes the surface layer of the resist to swell, resulting in slower development at the top relative to the layer below. This has the effect of creating an overhang, which reduces deposition on the sidewalls and produces a cleaner lift-off.

A 250 nm silica layer was deposited over the nichrome, also via e-beam evaporation, in order to prevent oxidation of the element during operation which would lead to degradation over time; this is common practice in commercial microheaters [8].

4.3.4 Device Testing

Measurements of fabricated heaters show a resistance variability below 1% in all cases. Further details of device performance may be found in chapter 5, discussing modular circuits, where extensive use is made of these devices.

4.4 Low-Temperature Phase Shifters

Due to the cryogenic conditions required for operation of the integrated single photon detectors (further discussed in chapter 6), and the limited cooling power of the refrigerators in use ($\sim$100 µW), localised temperature variations of the scale required for thermo-optic phase shifters are impracticable. For this reason the non-thermal alternative methods must be considered. One potential solution is the use of piezoelectric stressor phase shifters; in section 4.6 we detail efforts aimed at improving the efficiency of these devices. A second alternative is the use of electro-optic (EO) materials, discussed in section 4.5. A third approach found in the literature is the use of electro-static

MEMS based devices [11], the low quiescent power dissipation of such devices makes them very promising for this application in compatible material platforms.

4.5 Electro-optic Phase Shifters

4.5.1 Device Geometries

A number of possible device structures exist for such a modulator; the silica waveguide itself may be utilised as the EO material through the use of poling, as was discussed in chapter 3 in the context of quasi phase matching. EO coefficients of up to 12.5 $\mathrm{pm \cdot V^{-1}}$ have been reported with UV-assisted poling [12], and Fujiwara *et al.* demonstrated a modulator using a UV-poled fibre, having an electro-optic coefficient of 5.8 $\mathrm{pm \cdot V^{-1}}$ [13]. In silica-on-silicon devices the silicon substrate may act as the bottom contact, while a top contact may be deposited upon a buffer layer over the required phase shifting region.

Alternatively, a channel may be formed across the waveguide and filled with an EO material such as an EO polymer; such polymers have been shown to exhibit a much greater EO coefficient than poled silica, allowing for reduced device lengths and operating voltages. The difficulty in this case lies with guiding the optical mode suitably in the channel region such that losses due to imperfect modal overlap with the main waveguide, as well as additional scattering, are minimised. The channel may be either machined or etched via RIE, and may be broad to allow for MMI based coupling with the exit waveguide, or narrow to match the single mode UV written waveguide as closely as possible.

A further possibility is an evanescently coupled EO layer placed above the waveguide, in much the same way as the detectors are in chapter 6. In this case a material with large EO coefficient may be used as in the channel filled case, however, the limited overlap with the mode, in the region of 5% based on FIMMWAVE modelling, necessitates a larger voltage for a given phase shift when compared with the previous approach. The use of an alternative contact arrangement whereby the bottom contact is placed immediately below the EO material would result in an approximately tenfold increase in field strength, and hence induced phase, allowing for similar operation to the previous approach. The advantage in this case lies in the potentially reduced losses due to modal mismatch and scatter; it does, however, require a contact to be placed in contact with the evanescent field, leading to appreciable absorption. The transparent conductor ITO, having a suitably low refractive index (1.6) to avoid significant perturbation of the mode with reasonable thicknesses, would produce unacceptable losses over a 500 µm length scale.

4.5.2 Choice of materials

A broad range of materials have been demonstrated with electro-optic coefficients, though the specifics of this application limit the available options. The chosen material is required to be deposited at low temperature, ideally at less than 120°C to remain compatible with on-chip TES detectors. For the material to also be used as an over-cladding for the entire chip its refractive index must be less than 1.40 at 1550 nm, since FIMMWAVE modelling suggests that a value above this allows higher order modes to exist below the TES regions, adversely affecting the detector performance. Additionally, the device must survive and operate at cryogenic temperatures; requiring a favourable combination of thermal expansion, strength, and layer adhesion to avoid damage.

4.6 Piezoelectric Phase Shifters

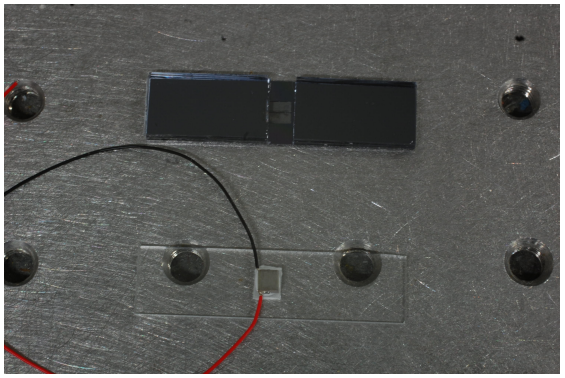
A more accessible route to producing phase-shifters capable of operating at low temperatures potentially lies with the strain-optic effect, since piezo actuators dissipate relatively little heat. Strain-optic modulators have previously been demonstrated in silicon nitride [14], though with a long active length of 10 mm due to the limited effective index change created by the shear arrangement used.

4.6.1 Ridge Strain-optic Enhancement

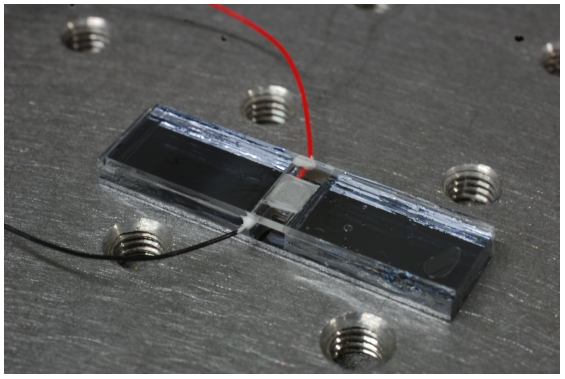
One may obtain an enhancement of the strain in such a device by reducing the contact area of the piezo to the region immediately surrounding the waveguide, achieved by machining a slot either side of the waveguide to leave a ridge, as proposed by Humphreys *et al.* [15]. A device was constructed to explore this approach in a MZI arrangement, in which a dicing saw was used to remove material with plunge cuts to produce a 5 mm long ridge in one arm of the interferometerer. The smallest piezo readily available was 3×3×2mm, requiring a minimum 1.5 mm spacing between the arms of the interferometer. The device was thus designed to accommodate this with 250 µm pitch input ports widening to 2 mm in the MZI and returning to 250 µm at the output; the resulting device is relatively large (40×10 mm) because of this. The waveguides were UV-written for operation at 780 nm.

A borosilicate capping piece was used to hold the piezo in place above the ridge, attached using a high Young's modulus optically clear glue (Dymax OP4-20632) and relying on the much larger glue surface area between the cap and chip than between the piezo and bridge to maximise the applied strain. The device required careful assembly to avoid wedge error in the piezo positioning that would lead to lateral forces on the bridge, as such the thicknesses of all pieces were measured and the top cap diced from a piece of

float glass selected to have the correct thickness; spacer beads were mixed into the glue to ensure that all adhesive layers had a consistent thickness of 17.5 µm. The final device is shown in figure 4.5.



(a)



(b)

Figure 4.5: An assembled piezoelectric stress based integrated MZI modulator, making use of a ridge structure for enhancement of the stress-optic effect.

While this device is a functional phase shifter at cryogenic temperatures it suffers a number problems, firstly its insertion loss is very high, predominantly due to relatively tight bends used to reach the 2 mm spacing required in the MZI region to accommodate the piezo, though this value is not inherent in the design and may be improved upon. The second and more significant issue is its large physical size; it is difficult to envision a device with more than a few of these modulators without significant miniaturisation of the piezo elements.

4.7 Conclusion

Here we have seen a number of design improvements to thermo-optic phase shifters for use with silica-on-silicon waveguides, as well as their use in amplitude modulators. COMSOL modeling has informed changes to both the heater geometry and FHD layer structure to provide a significant efficiency increase. These developments play a key role

in the reconfigurable circuits, developed in the next chapter. We have also seen initial work on alternative phase-shifter approaches more suitable for cryogenic operation, which are of importance for compatibility with the integrated single photon detectors discussed in chapter 6.

References

[1] G. P. Agrawal, *Lightwave Technology Components and Devices*, 2nd ed. Hoboken, New Jersey: John Wiley & Sons, 2004.

[2] B. J. Smith, D. Kundys, N. Thomas-peter, and I. A. Walmsley, "Phase-controlled integrated photonic quantum circuits," *Optics Express*, vol. 17, no. 16, pp. 264–267, Jul 2009.

[3] B. J. Metcalf, J. B. Spring, P. C. Humphreys, N. Thomas-Peter, M. Barbieri, W. S. Kolthammer, X.-M. Jin, N. K. Langford, D. Kundys, J. C. Gates, B. J. Smith, P. G. R. Smith, and I. A. Walmsley, "Quantum teleportation on a photonic chip," *Nature Photonics*, vol. 8, no. 10, pp. 770–774, Sep 2014.

[4] Z. Chaboyer, A. Stokes, J. Downes, M. J. Steel, and M. J. Withford, "Design and fabrication of reconfigurable laser-written waveguide circuits," *Optics Express*, vol. 25, no. 26, pp. 33 056–33 065, Dec 2017.

[5] F. R. M. Adikan, C. B. E. Gawith, P. G. R. Smith, I. J. G. Sparrow, G. D. Emmerson, C. Riziotis, and H. Ahmad, "Design and demonstration of direct UV-written small angle X couplers in silica-on-silicon for broadband operation." *Applied optics*, vol. 45, no. 24, pp. 6113–8, Aug 2006.

[6] D. Kundys, J. Gates, S. Dasgupta, C. Gawith, and P. Smith, "Use of Cross-Couplers to Decrease Size of UV Written Photonic Circuits," *IEEE Photonics Technology Letters*, vol. 21, no. 13, pp. 947–949, Jul 2009.

[7] H. L. Rogers, S. Ambran, C. Holmes, P. G. R. Smith, and J. C. Gates, "In situ loss measurement of direct UV-written waveguides using integrated Bragg gratings," *Optics Letters*, vol. 35, no. 17, pp. 2849–2851, Sep 2010.

[8] J. Rolke, "Nichrome Thin Film Technology and its Application," *Electrocomponent Science and Technology*, vol. 9, pp. 51–57, 1981.

[9] P. A. Cooper, L. G. Carpenter, C. Holmes, C. Sima, J. C. Gates, and P. G. R. Smith, "Power-efficiency enhanced thermally tunable bragg grating for silica-on-silicon photonics," *IEEE Photonics Journal*, vol. 7, no. 2, pp. 1–11, Apr 2015.

[10] S. Franssila, *Introduction to Microfabrication*. Chichester: John Wiley & Sons, Ltd., 2004.

[11] M. Poot and H. X. Tang, "Broadband nanoelectromechanical phase shifting of light on a chip," *Applied Physics Letters*, vol. 104, no. 6, p. 061101, Feb 2014.

[12] J. Khaled, T. Fujiwara, and A. J. Ikushima, "Optimization of second-order nonlinearity in UV-poled silica glass," *Optical Materials*, vol. 17, pp. 275–278, Jun 2001.

[13] T. Fujiwara, D. Wong, Y. Zhao, S. Fleming, S. Poole, and M. Sceats, "Electro-optic modulation in germanosilicate fibre with UV-excited poling," *Electronics Letters*, vol. 31, no. 7, p. 573, Mar 1995.

[14] N. Hosseini, R. Dekker, M. Hoekman, M. Dekkers, J. Bos, A. Leinse, and R. Heideman, "Stress-optic modulator in TriPleX platform using a piezoelectric lead zirconate titanate (PZT) thin film," *Optics Express*, vol. 23, no. 11, pp. 14 018–14 026, Jun 2015.

[15] P. C. Humphreys, B. J. Metcalf, J. B. Spring, M. Moore, P. S. Salter, M. J. Booth, W. S. Kolthammer, and I. A. Walmsley, "Strain-optic active control for quantum integrated photonics," *Optics Express*, vol. 22, no. 18, pp. 21 719–21 726, Sep 2014.

Chapter 5

Modular Quantum Circuits

5.1 Introduction

This chapter details the development of a modular reconfigurable system for implementing arbitrary linear quantum optics experiments on-chip. The use of universal linear networks for quantum optics has become increasingly common of late [1, 2], though to date these have all been monolithic devices. Here we design duplicate chips having an array of thermo-optically tuned MZIs, as well as the necessary control and interfacing hardware and software. All design and fabrication throughout this chapter was carried out by the author, while much testing was conducted by collaborators at Oxford.

5.1.1 Motivation

A number of major challenges were identified while producing and using larger optical circuits for specific quantum experiments, principally related to ensuring that the produced device meets its design. In order to determine whether such an experiment is indeed providing the expected non-classical results, it is necessary to first measure its parameters, such as splitting ratios, accurately. In most cases this is done by measuring the output profile for a full range of inputs and configuration settings, however, this is prohibitively time-consuming for large circuits, particularly if carried out in the single-photon regime.

An alternative to this is to build up a larger network out of smaller modules, which may then be tested individually. Not only does this permit the system characteristics to be determined much more efficiently, it can also enable a design to be matched more closely by selecting those modules closest to ideal. The use of identical, fully configurable, modules further simplifies the design and can permit a single device to be used for a range of experiments. The use of universal networks enables alternative mapping schemes to

be used such as that of Miller *et al.*, in which an iterative adjustment procedure is used to obtain the desired response from an imperfect network [3]. Additionally, extra degrees of freedom in device configuration should permit alternative configurations for a given unitary, which may provide higher fidelity given the system's residual imperfections. A further benefit to this approach concerns the UV-writing technique adopted here, for which outgassing of the in-diffused hydrogen gradually alters the writing process over time; the production of multiple smaller chips instead limits this effect.

This approach does have two drawbacks however. Firstly, some interface loss will inevitably be present between modules, which will scale with the number of modules; clearly this must be small relative to the module loss for the approach to be beneficial. Secondly, the overall device length of a circuit composed of modules will necessarily be larger than a similar monolithic chip, providing a corresponding increase in total material loss, due to a small additional waveguide length required at the input and output of each module. This additional length is necessary partly because in this scheme all waveguides must match a standard pitch at the input and output, but also due to the strengthening bar on the top surface, required for mechanical support of the chip-chip bond. As described in chapter 2, the base of the strengthening bar can't be much narrower than 750 µm.

5.1.2 Viability of a Modular Approach

A key factor in assessing the viability of such an approach is the achievable inter-chip excess loss, both for a single channel and for an array of tens of waveguides. Due to the low-index nature of silica waveguides, and the uniformity of FHD layers, it would be expected that low coupling losses should be achievable; with the largest variation being due to drift in the UV-writing conditions.

A study was undertaken to determine the significance of coupling losses in practice with the use of two duplicate chips, having a matching set of 16 waveguides. These devices were UV-written one after the other in chips from adjacent positions on the source wafer, minimising the effects of alignment and layer variation. Each waveguide had a series of Bragg gratings centered at 780 nm, with a 0.5 nm offset in wavelength between gratings on the two chips. Strengthening bars were glued to both facets of the chips and each chip pigtailed with a 16 port, 250 um pitch v-groove assembly. The chips were than aligned for maximum throughput in the two end waveguides using a 5-axis stage system with piezo feedback, before bonding with UV cured glue.

Initial measurements with purely diced facets showed relatively poor coupling loss values of 0.5 dB, believed to be due to wedge on the facet from the dicing procedure leading to tilting of the pigtail. The samples were thus end polished using the method of section 2.8.2, mounting the samples in a stack such that the facets to be coupled were

parallel. A repeat of this measurement provided an improved loss value of 0.2 dB, which we may compare with the typical optical-fibre splice loss of ~ 0.1 dB.

5.2 System Design

5.2.0.1 Initial Concept

The ultimate goal of the BLoQS project is the creation of a 10-photon, 20-mode Quantum circuit. As shown in section 3.1.5, the infrequency of N-photon coincidence events from parametric sources for larger photon numbers makes operation of such a system prohibitively slow with even optimistic device losses; necessitating the use of either quantum memories, for source synchronisation, or source multiplexing schemes. Despite this, the modular work was designed to scale to arbitrary experiments with 10 concatenated modules, should such experiments become practical in the near future.

5.2.0.2 Module composition

In this system each module provides a set of configurable beam-splitters that go to form a larger linear network. The tunable element here was selected to be a MZI, since the required configurability may readily be obtained with thermo-optic tuning; an alternative to this would be a tunable coupler, which may be more compact. An array of single MZI elements was selected as the modular unit, since this provides maximum flexibility and should permit any desired unitary circuit to be produced. Sequential elements may simply be offset by the width of one port to connect adjacent MZIs together to form a network. The resulting layout is displayed in figure 5.1. Additional straight waveguide channels either side of the MZIs ensure a pair of unconnected paths is present through the offset module chain for loss-measurement and alignment purposes.

There is a trade-off in moving to more complex modules; these could provide reduced total losses as there can be fewer modules overall and thus fewer couplings, however they also increase the difficulty of initial characterisation as well as potentially reducing the flexibility of the system. In particular an alternative layout considered is a pair of concatenated MZIs; this may be used to improve the accessible range of the tunable beamsplitter at its extremes, which can become limited if the couplers deviate from the ideal 50:50 ratio.

Specialised modules may of course be combined with the standard modules to make up a larger system. Indeed while the use of homogenous modules may offer the best overall performance for an arbitrary unitary, it is as-yet unclear whether some alternative arrangement will prove optimal if the range of unitaries to be reproduced faithfully is restricted to those most interesting, or most commonly used in experiments.

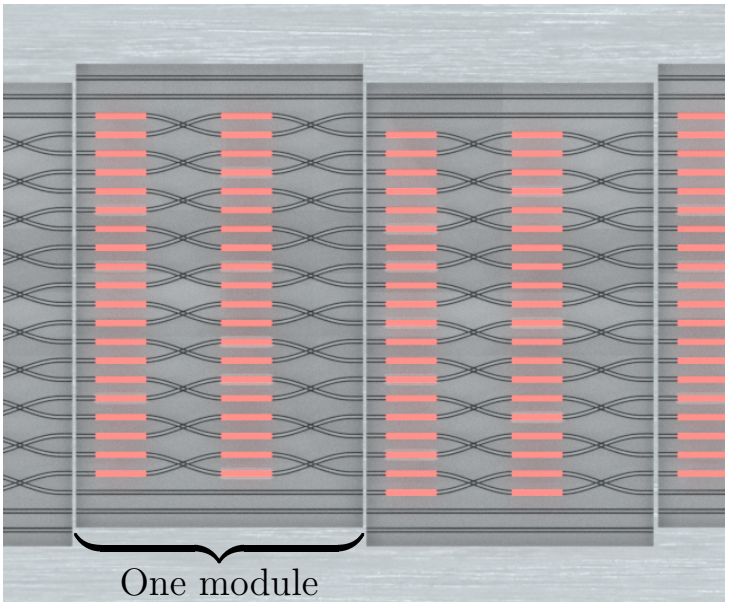
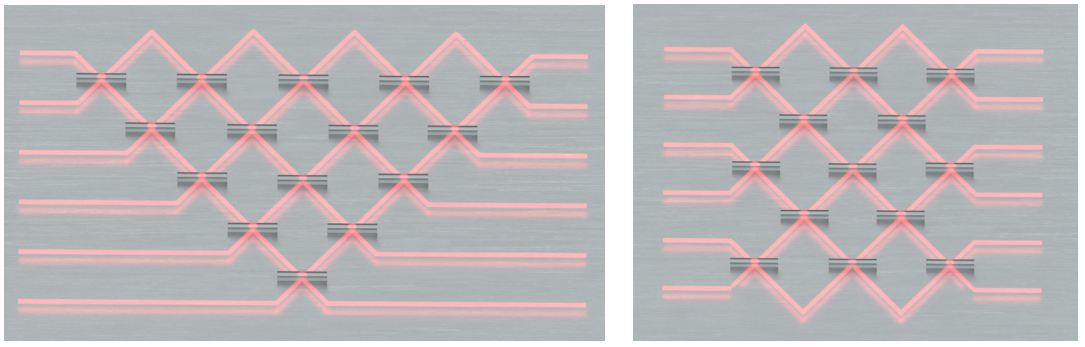


Figure 5.1: Layout of the modular devices, each is an array of ten MZIs with straight waveguides at either end. Sequential modules are offset by the waveguide pitch to connect adjacent channels. Note that the lateral dimensions here have been greatly exaggerated for clarity.



(a) (b)

Figure 5.2: The Reck (a), and Clements (b) circuit decomposition schemes (beam folding mirrors have been omitted). Each crossing point is the site of a beam-splitter of configurable phase and reflectivity, implemented in our case with a MZI.

A new circuit decomposition was developed based on this layout by Clements *et al.* [4] and has been shown to perform better than the more traditional Reck scheme [5] in the presence of losses; both schemes are illustrated in figure 5.2.

For this work ten MZIs, and thus 20 modes, was selected as the size of each module, since ten photons is the limit of what might be expected to give significant count rates from sources in the near future, without memory-based synchronisation or multiplexed source schemes. With further development, as module losses are reduced, the complexity of

individual modules may be increased to reduce the relative loss contribution from module interfaces.

5.2.0.3 Optical design

A 127 µm waveguide pitch was selected, smaller than typical for previous devices (250 µm) but offered by commercial suppliers for PM 780 nm fibre. This allows for shorter cross-couplers for the same excess loss, and thus more compact modules. A narrower pitch than this would potentially be possible with custom pigtails using thinner cladding fibre, though at significantly increased cost, with the main limit being the increasing thermal crosstalk between elements closer than 100 µm.

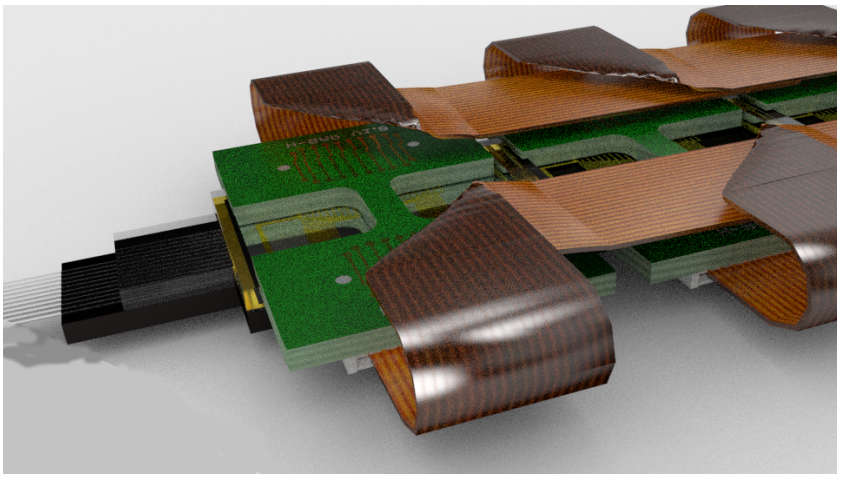
Bragg gratings were incorporated to permit classical characterisation of the modules; six unique gratings were used at sites within the MZIs to extract coupling ratios; these wavelengths were duplicated for all MZIs in all chips to simplify characterisation, since these would only be used for single-module measurements. In measuring inter-module coupling losses unique gratings are required in each chip, unless a time-resolved measurement can be made with the use of an optical backscatter reflectometer (OBR), however, these are not available at 780 nm. A unique set of grating wavelengths was thus used in the loss-measurement waveguides, at each end of the network, for each chip to permit such multi-module measurements.

5.2.0.4 Thermo-optic modulators

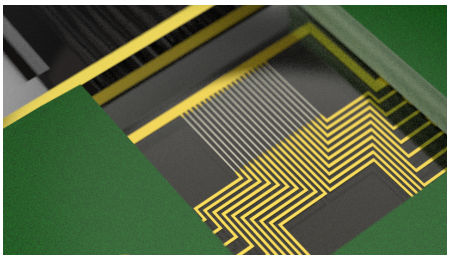
Thermo-optic elements were selected as the modulator for these devices, as this technology is well developed. Several of the efficiency improvements developed in chapter 4 were incorporated into the phase-shifters used in this work, specifically the overcladding thickness reduction and element width. Heaters on both arms of each MZI were used since this offers a number of advantages; it provides both redundancy and increased tuning range for the same operating voltage. Additionally, when operated in a complementary fashion, this provides a constant heat flow into the chip which should improve the stability during operation and reduce thermal crosstalk.

5.2.0.5 Electrical Interfacing

Mounting of the connector PCB above the optical chip was chosen to permit reflow solder-bump bonding, as well as heat-sinking of the chip's silicon bottom surface. Slots were added to the PCB to enable optical inspection of the top surface of the chip; as a result connections could not be made across the two halves of the chip and a separate connector was needed for each half. The resulting concept is shown in figure 5.3. It was



(a)



(b)

Figure 5.3: (a) Concept render of the modular system; a set of quantum circuit elements are coupled together with thermo-optic phase shifters (closeup in (b)) for reconfigurability. Electrical connections are made via a PCB board solder bump bonded to each chip.

desirable that the connectors to the modules be small since these limit the minimum length of the PCBs and thus the modules themselves; the connected cables were also chosen to avoid significant mechanical loading of the modules, which would be troublesome during optical alignment. Based on these requirements 0.3 mm pitch flat flexible cables (FFCs) were selected, one either side of the chip, each providing 25 connections in a thin flexible ribbon with a 10 mm long, 1 mm high connector. These connectors were placed on the underside of the PCB, being the same thickness as the optical chip. The FFC ribbon cables can only be sourced in relatively short fixed lengths, thus an additional breakout board was required to connect between these and a set of larger (50-wire) IDC ribbon cables connected to the module controllers.

5.3 Fabrication Approach

Complete details of the final fabrication process with recipes for each step can be found in appendix D

5.3.1 UV Writing

The wafer fabrication process does not differ from that detailed in chapter 2, and the parameters of the wafers used may be found in appendix C. After dicing and hydrogen loading of the chips each module was UV-written. While provision was made for the use of alignment marks to maintain register between the inscribed waveguides and heater elements, it was found that the ~ 5 µm level of positioning common with UV-writing provided sufficiently good alignment with respect to the chip edges, and fine alignment of the elements to the waveguides was possible with the mask aligner during their patterning. As a result, these marks were not used, saving an additional processing step.

5.3.2 Heater Element Fabrication

The design of the various patterned layers of a 12 mm module is displayed in figure 5.4.

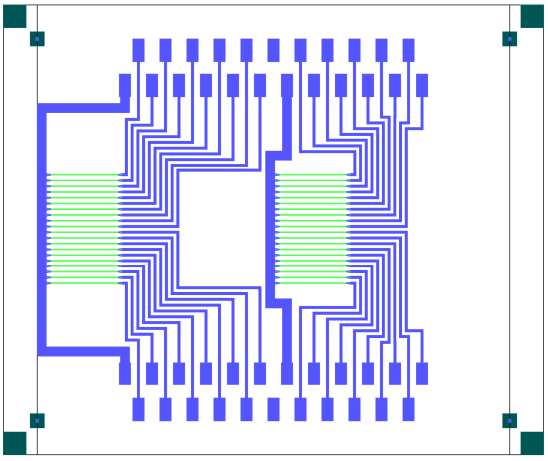
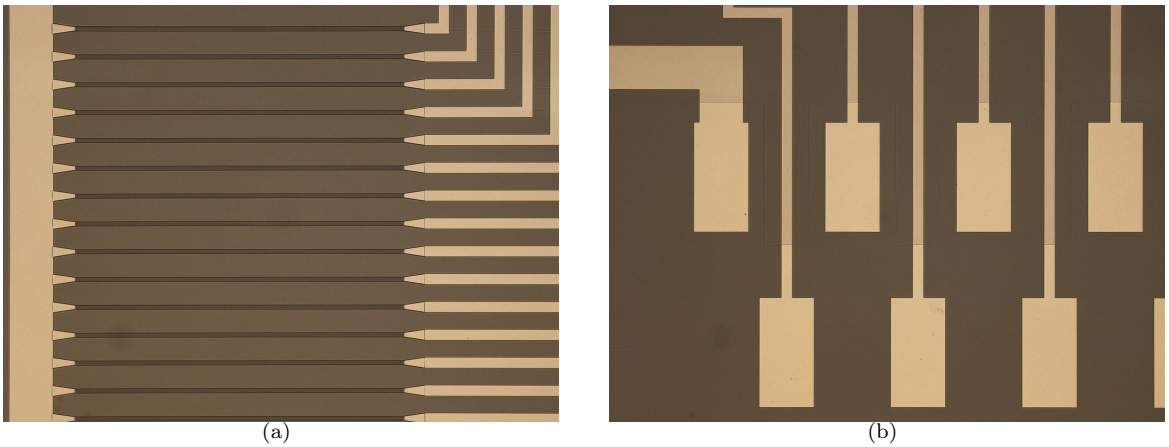


Figure 5.4: Schematic of a 12 mm Mach Zehnder module showing the heater element (green), wiring (blue), and capping (grey) layers.

Nichrome heater elements were e-beam deposited and patterned via lift-off in the manner described in section 4.3.3. This was followed by a wiring layer patterned by the same approach, initially in gold, however copper was later found to provide a much faster deposition rate while avoiding defects caused by spitting from the crucible. Finally, a silica capping layer is fabricated to protect both wiring and heater elements; example images of the resulting structures are shown in figure 5.5.

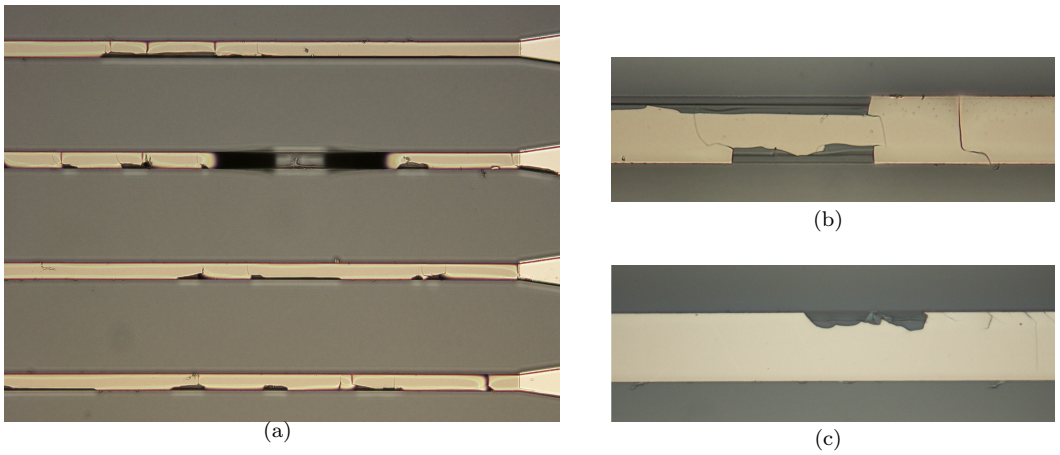


(a) (b)

Figure 5.5: Microscope images of (a) the nichrome heating elements and (b) the copper wiring and pads; the silica capping layer is also visible.

5.3.2.1 FHD Layer Cracking

During heater element fabrication an issue was encountered in which cracks were forming in the FHD layers, following the boundaries of the nichrome coated regions. This was found to be caused by a plasma cleaning step carried out after patterning of the wiring layer; this same step had previously been carried out on test-structures of the same design but formed entirely of NiCr without incident. It is believed that RF fields coupled into the wiring layer led to local heating within the resistive NiCr elements, creating high stress regions along their edges which led to the cracking.



(a) (b) (c)

Figure 5.6: Images of cracking in the FHD layers following edges of NiCr patterned regions.

This additional plasma cleaning step was found to be unnecessary, and avoided in later devices after deposition of the wiring layer. The cracking observed in the FHD layers is, however, believed to be the main power-limiting failure mechanism for the 20 µm wide

heaters used in these modules. Heating of the entire chip to up to 400°C, exceeding the peak temperature of the heaters during operation, had no such detrimental effect.

5.3.2.2 Titanium layer oxidisation

In the initial layer deposition sequence the titanium layer required for adhesion of the silica cap was put down after both the element and wiring layers; it was found that devices constructed in this way suffered from unexpectedly high electrical resistances with significant variability. The application of a small voltage (5V) to these devices was found to reduce this resistance to a usable range, albeit still higher than the design value and thus leading to a reduced tuning range.

After numerous tests it was found that this behaviour was the result of the titanium layer oxidising between deposition runs, resulting in a thin (5 nm) oxide between the wiring and heater layers; the application of a voltage was resulting in breakdown of this oxide. The issue was resolved by a reordering of the depositions to avoid this intermediate layer, evaporating the titanium directly before the silica cap and thus coating everything but the pads. This was avoided initially since it was thought that it could potentially produce a conductive short between elements, however testing revealed that this was not the case.

5.3.3 Under-bump Metallisation Layer

In order to permit solder-bump bonding, an additional metallisation layer is required between the pads and the solder bumps as shown in figure 5.7; this layer prevents the molten solder from dissolving the relatively thin pad layer during the soldering process. The layer material must be capable of forming intermetallic compounds with the solder used, to permit the solder to wet to the layer and a joint to be formed; furthermore it must be thicker than the intermetallic layer formed during the soldering process, or dissolution of the layer will result. This layer is commonly nickel or copper, both of which form intermetallic layers with tin solder that terminate at a depth of ~ 2 µm. Such layer thicknesses are difficult to achieve through evaporation due to the low deposition rates for these materials, instead, a wet chemical electroless deposition process is commonly used based on a reduction reaction, or the material is sputtered.

Initial tests with electroless deposition were conducted, however uniform deposition was difficult to achieve and significant optimisation of the bath composition was required. Instead, various metals were considered and a material that could be evaporated to form thick layers relatively quickly was found, namely silver.

It was found that silver may be deposited through e-beam evaporation with rates of $\sim 1\text{nm} \cdot \text{s}^{-1}$. The main challenge with this material was obtaining adequate adhesion

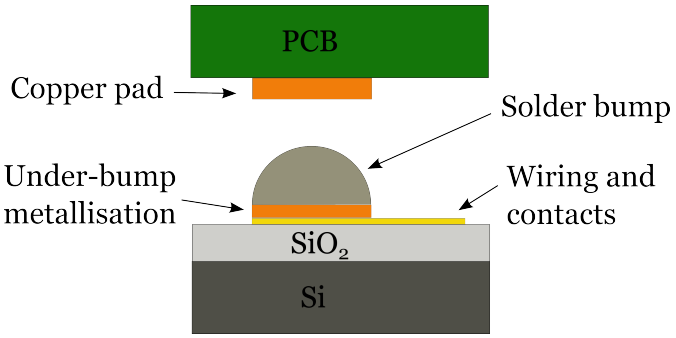


Figure 5.7: Diagram of the solder bump bonding approach.

to the substrate; several metals were tested as adhesion promoting layers to the FHD substrate, with chromium, titanium and aluminium providing little benefit. Since silver readily alloys with copper, and well-adhered copper layers had already been achieved for the wiring layer, a three-layer Ti/Cu/Ag structure was selected.

5.3.4 Facet Polishing

After attachment of the strengthening bars the chips were mounted for polishing as a stack, oriented such that any wedge error in the polish would be shared by the following chip; ideally helping to minimise the coupling loss. The stack was lapped flat with successive 3 µm and 1 µm lapping films, removing $\sim$ 100 µm of material, before polishing for 4 minutes with a 0.5 µm polishing solution.

In order to protect the heater elements during polishing, from the binding wax in particular, the top surface of each module was coated in photoresist (S1800 series) by pipette and cured on a hotplate. The thick resulting layer did however prove difficult to remove, since immersion in acetone or similar solvents was found to also remove the strengthening bars; as a result some surface damage was caused to the wiring on the first two modules. A number of alternative coatings were tested however the requirements of being easily removed, leaving no residue, and being insoluble in water for the duration of the polishing process proved to be difficult to meet. For later modules a spray-on photoresist was found to be much more suitable, providing a thin layer that was readily removed with a brief acetone wash followed by IPA and DI water. This resist did not wet to the e-beam evaporated silica however; in order to obtain a complete coating it was thus necessary to cover the top surface of the chip in lens tissue prior to spraying.

5.3.5 Module Assembly

In initial tests the connectorised PCBs were glued adjacent to each modular chip on a silicon carrier plate, as shown in figure 5.8, and connections made via wire bonding. As expected the large number of fragile connections did lead to breakages during use;

encapsulation of the bonds would mitigate this, though would be difficult to achieve without also covering the heater region.

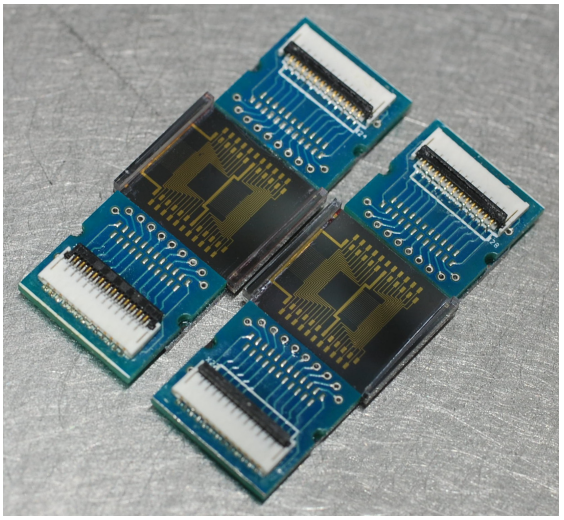


Figure 5.8: A pair of fabricated 12 mm MZI modules prior to wire-bonding.

Once deposition of 2 µm silver pads was possible, the originally intended reflow solder bonding process was used, producing the device of figure 5.9. For this variant the h-bar PCB is diced to match the spacing between the two strengthening bars on the chip to within 50 µm. A low-temperature solder paste (140°C) is then applied to the pads and the chip heated to 150°C on a hot plate, causing the solder paste to ball-up to form bumps. The use of low-temperature solder allows the chip to be bonded to the PCB without desoldering the connectors on the PCB, or damaging the glue used to attach the strengthening bars. After cooling, the PCB is positioned, making use of the alignment holes to set the lateral positioning, and the sample returned to the hot plate. A small amount of pressure is applied to the top of the PCB to ensure all of the bumps make contact; this is necessary since any variation in the amount of solder deposited on the pads leads to bumps of varying heights. Use of this approach has thus far been limited to test devices, since it has yet to produce reliable contacts due to the variability in bump size. It is believed that further optimisation of the solder paste application will remedy this.

5.4 Control Electronics

The large number of heaters to be controlled simultaneously makes the operation of these modules a non-trivial task, placing a number of requirements on the controller; custom drive electronics were developed by the author to fulfill this role.

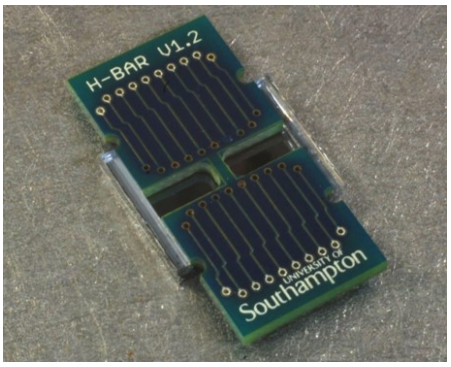


Figure 5.9: A prototype solder-bumped assembly without waveguides, the process was unoptimised, resulting in incomplete connectivity in this device.

5.4.1 Requirements

Based on the heater elements developed in chapter 4, the target resistance here was selected to be 1 KΩ; in test devices a heater power dissipation of 220 mW was found to provide a suitable π phase shift, thus a minimum drive voltage of 15 V is desired, with a drive current of 15 mA. The ability to supply higher voltages would be beneficial for a future move to 1550 nm operation, since V_π for devices at this wavelength would be higher than that for 780 nm devices. The heaters were to be configured by computer control to permit automated experiments, with setting updates carried out in less than a second. The relatively slow response of the heaters (suggested by modelling to be $\sim$ 5 kHz) does permit some fluctuation in the output level, since any higher frequency variation will be low-pass filtered by the heater itself. The large number of heaters required, up to 400 (20 complementary pairs, up to 10 modules), makes simplicity of the heater drive circuitry also preferable; minimising the number of additional components per heater should simplify the task of PCB layout and routing.

5.4.2 Implementation

A digital pulse-width modulation (PWM) approach was selected for control of the heater powers, due to its relative simplicity and flexibility. A timing diagram of typical PWM control patterns is shown in figure 5.10; the analogue switches switch between the supply and floating according to this waveform, resulting in power dissipation in the heater which varies linearly with the control signal duty-cycle.

A field-programmable gate array (FPGA) was used to generate a set of 40 arbitrary PWM outputs, used to activate 40 pairs of analogue switches (one in each pair inverted) to provide the necessary drive current and voltage for 80 phase shifters. Interfacing and configuration of the PWM settings was implemented using an 8-bit ATmega microcontroller with built in USB interface, communicating with the FPGA via a two-wire i^2C interface. The resulting PCB is displayed in figure 5.13. The control board was

designed to stack, allowing for a set of boards to operate with a single USB connection, the master board relaying commands to connected boards via a common i^2C bus.

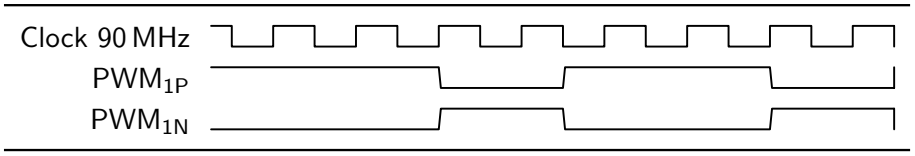


Figure 5.10: Example PWM control patterns, with two complementary outputs P and N.

Running each pair of complimentary heaters with a single control signal does reduce the system's flexibility somewhat but halves the necessary IO pins on the FPGA, as well as drastically simplifying the PCB layout. The resulting limitations were avoided by organising the 80 heater switch lines into a set of 8 banks, each with an additional supply switch. This arrangement permits sets of heaters to be disabled when necessary with little added complexity.

A Lattice MachXO2 FPGA was selected for generation of the PWM signals, meeting the necessary IO requirements as well as offering a range of built-in peripheral functionality—in particular, its hardened i^2C component simplified interfacing with other devices. The FPGA was programmed in Verilogp; a block diagram of its operation is shown in figure 5.11. All PWM signals are generated from a single 10-bit master counter, the desired duty cycle for each of the 40 outputs is stored as a 10-bit value in a two-page 10×20 register. Each output is generated by a less-than comparison between the corresponding row in the register and the master counter value. In order to reduce routing and logic resource requirements sufficiently to fit the design onto the chosen device, the output values are registered and each of the two ports is updated every other clock cycle; a single set of comparison logic is used for both and the register page address is changed each clock cycle. As a result the FPGA must be clocked at twice the PWM update frequency, though this does not restrict operation since the design has a maximum clock frequency of 96 MHz, well above that of the analogue switches. Control commands and PWM set-point values are received from the microcontroller via the FPGA's hardware i^2C component and are used to update the PWM set-point register, as well as the bank-enable and LED-output registers.

The microcontroller, an ATmega32U4, was programmed in C. A USB library provided by Atmel was used to handle USB communication, operating as a HID—this is a generic USB device class suitable for the relatively low data rates used in this application and allows existing operating system HID drivers to be used. Commands received by the USB interface are interpreted and dispatched to the FPGA when necessary. The microcontroller also handles measurement of the heater elements electrical time constants, allowing their resistances to be calculated. Additionally, a separate two-wire interface is used to set the board's heater supply voltage.

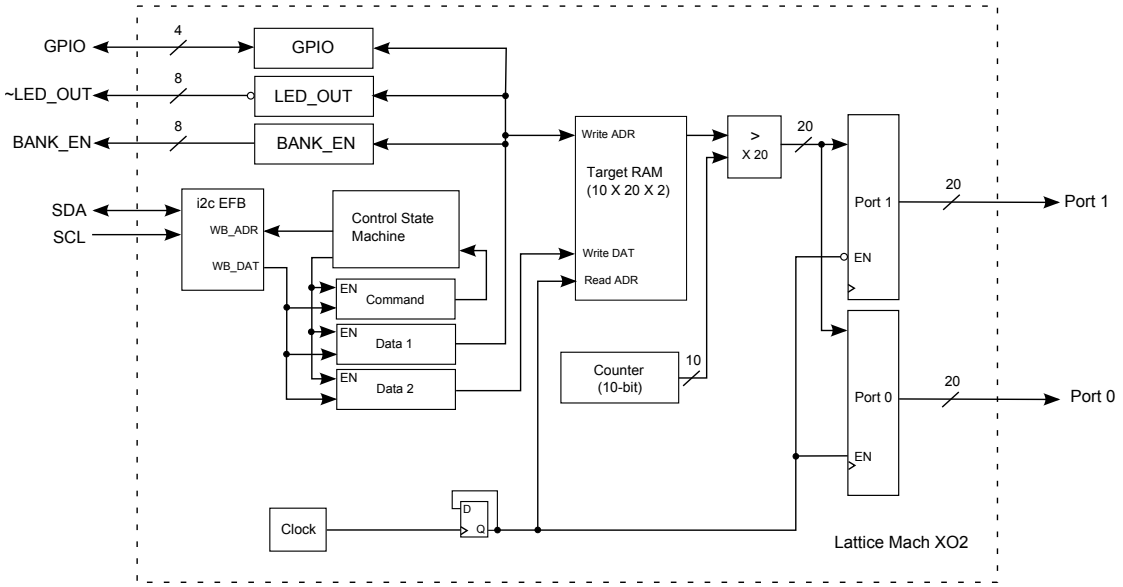
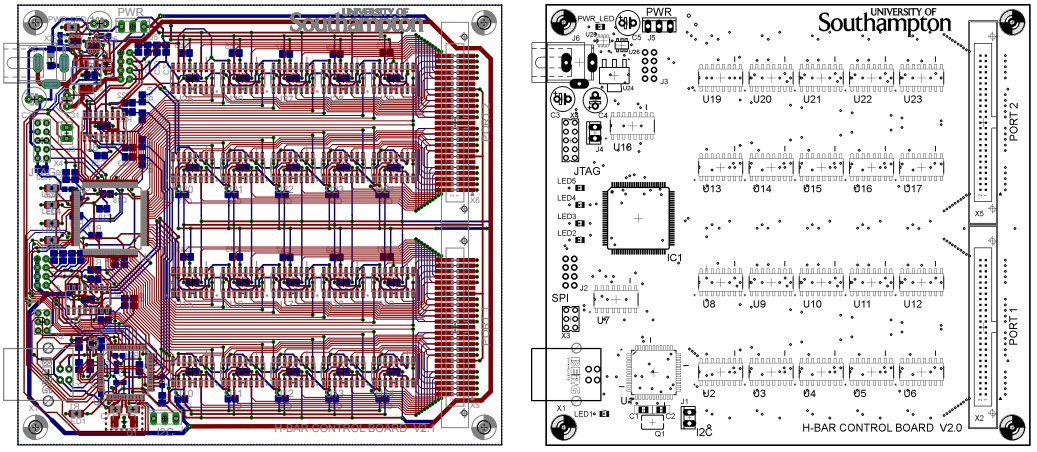


Figure 5.11: Block diagram of the FPGA firmware for the v2.1 control board.

The heater supply is provided by an LM317DCY adjustable regulator, controlled using a digital potentiometer combined with a current mirror formed from a pair of BJTs.



(a) (b)

Figure 5.12: (a)PCB layout of the control board, capable of generating the PWM signals for two MZI modules. (b) Top silkscreen layer of the same, highlighting the layout on the main component side.

The final two-layer PCB layout is displayed in figure 5.12, while the full schematics can be found in section E.8; the assembled prototype is shown in figure 5.13.

A Matlab library was written to interface with the control board, providing a mapping between the numbered target heaters and the physical connections, to the switches and between the controller and individual heater elements, via the breakout board. Additional details of the library operation, FPGA hardware description and microcontroller software are included in appendix E.

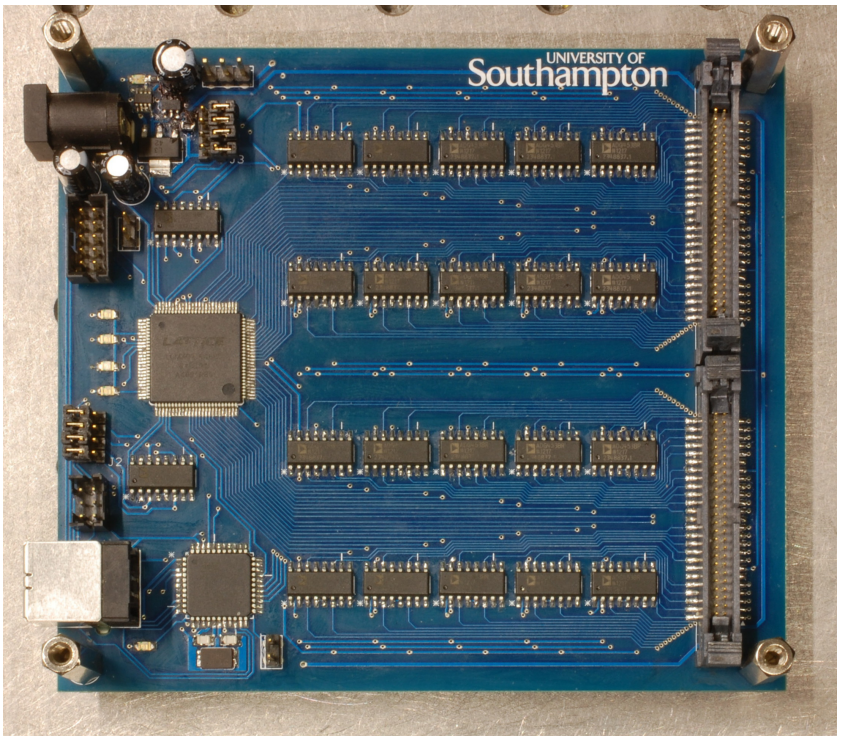


Figure 5.13: Assembled control board PCB v2.0.

5.5 System operation

5.5.1 Switching Speed Limitations

In the first generation of controller, ADG453 analogue switches were used; it was found, however, that due to an unexpectedly short time response of the thermal elements (15 kHz) the required FPGA clock frequency of 8 MHz was too fast for the slew rate of these switches. As a result the decay on switch off lasted longer than a clock period, causing heater settings at the extremes of the range to be ineffectual and thus reducing the dynamic range slightly. A SPICE model based on the device specification suggested a 90% switching speed of 80 ns should be obtained for the drive voltage of 3.3 V, in contrast with the somewhat larger measured falling value of 200 ns (40 ns rising). A range of alternative switches were tested and the DG643 found to provide the fastest switching speed of 100 ns (100 ns rising); this device was thus used on the v2.1 control board, having the drawback of a reduced maximum switching voltage of 21 V in addition to a larger ON resistance of 40 Ω.

5.5.2 Optical alignment and Assembly Procedure

Prior to assembly, each module is characterised with the aid of a pair of 24-port v-groove assemblies that are coupled to its input and output sides with a pair of 6-axis NanoMax

stages. The chip and pigtail facets are first made parallel with the use of a force sensor on the chip holder that is used to detect when the two come into contact; the pigtail pitch and tilt are optimised to permit the greatest translation before contact, corresponding to parallel facets. After approximate alignment using visible light, broadband light from a 790 nm SLED is launched into the two end waveguides and the remaining axis optimised to give the greatest transmitted power in these two waveguides.

Upon completion of this characterisation procedure on a set of modules they may be combined by first pigtailing one of them, aligning it in the manner explained previously, and then coupling the second chip to the first by optimising the reflected power of the Bragg gratings in the two peripheral waveguides. Every alternate chip is offset by the waveguide pitch, 127 µm, so as to connect adjacent MZIs. This continues until sufficient modules have been connected, at which point the output pigtail is attached, as described previously.

5.5.3 Module testing

Characterisation proceeds by launching into each of the waveguides in the network in turn in both forward and reverse directions, for straight waveguides the reflection spectrum and transmitted power for both TE and TM polarisations are recorded, while for the MZIs the power in the two output ports is recorded for a range of heater settings, producing a plot such as figure 5.14. From this information the coupling ratios, accessible tuning range and insertion losses may be determined. The input phase-shifters, however, cannot easily be tested without connecting the chip to another module.

In the scan of figure 5.14 we find that the maximum and minimum of the two outputs do not correspond to the same phase setting, this undesirable behavior may be explained if a phase-dependent loss is present within the MZI. It is believed that the multimode nature of the waveguides is the cause for this phase-dependent loss, in which case adjusting the waveguide dimensions to ensure truly single-mode operation would resolve the issue.

In optical tests, typical propagation losses for these devices were 0.3 dB/cm, measured using the Bragg grating approach. From measurements of 20 couplers on a modular chip it was found that a random error in splitting ratio of $\pm 4\%$ was present. This is likely due to laser power fluctuation during fabrication, and to a lesser extent FHD layer variability. The systematic deviation of the coupling ratio from design has yet to be determined.

Measurement of any crosstalk present was conducted by setting a MZI to its most sensitive region of operation, at the steepest point of its phase curve, and modulating an adjacent element while monitoring the transmission. The resulting measured variation corresponds to a crosstalk of 0.01π between adjacent MZI channels and 0.007π to the next nearest MZI. This process was repeated with half of the heater banks disabled,

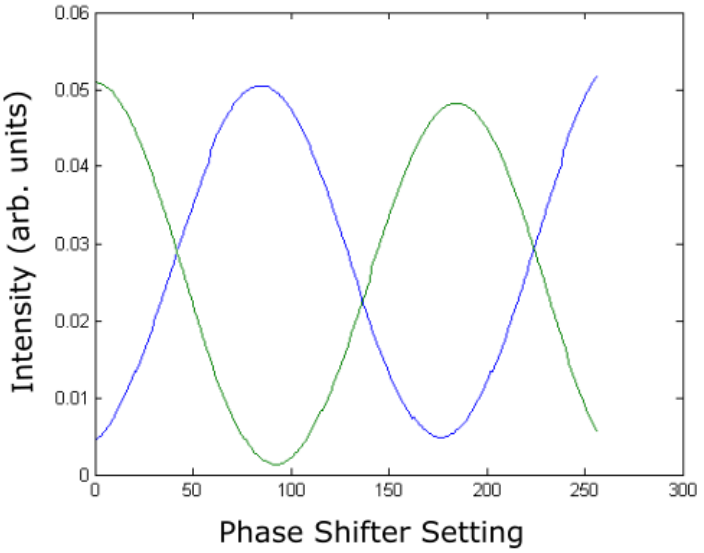


Figure 5.14: Optical output intensities from a single MZI on a module over the range of 8-bit phase shifter settings (0-255).

simulating the traditional single-heater design, in this case the effect of crosstalk was found to be twice as great.

The stability of a three-chip modular setup was determined by again configuring it to operate at its most sensitive point, implementing a 3 dB coupler, with a broadband SLED source as input to one port. The transmission at both corresponding output ports was monitoring for a period of three days, which is of the order of the time required to carry out a typical experiment. The measured fluctuations, displayed in figure 5.15, show a relative variation of 2.6% for the two outputs over this period. Much of the higher frequency noise is likely to be associated with fluctuations in the source intensity rather than phase drift in the interferometer itself. Unfortunately this contribution cannot be separated out since measurements in the two arms were made by switching sequentially to a single power meter, had collection been carried out using two power meters this would not be the case. The low frequency variation visible in the plot is likely the result of long term temperature changes in the laboratory, altering the cooling rate of the chip. In this experiment purely passive cooling was used; the chip was mounted with thermal paste on a heatsink, itself in contact with an optical table. This effect might be remedied through use of active cooling, such as water cooling of the heatsink as originally planned. The thermal output of these devices is significant, at the maximum supply voltage of 21V and nominal element resistance of 1 kΩ the power dissipated by each heater power independent of setting is 440 mW, the dissipation of all 20 pairs on a chip is thus 8.8 W.

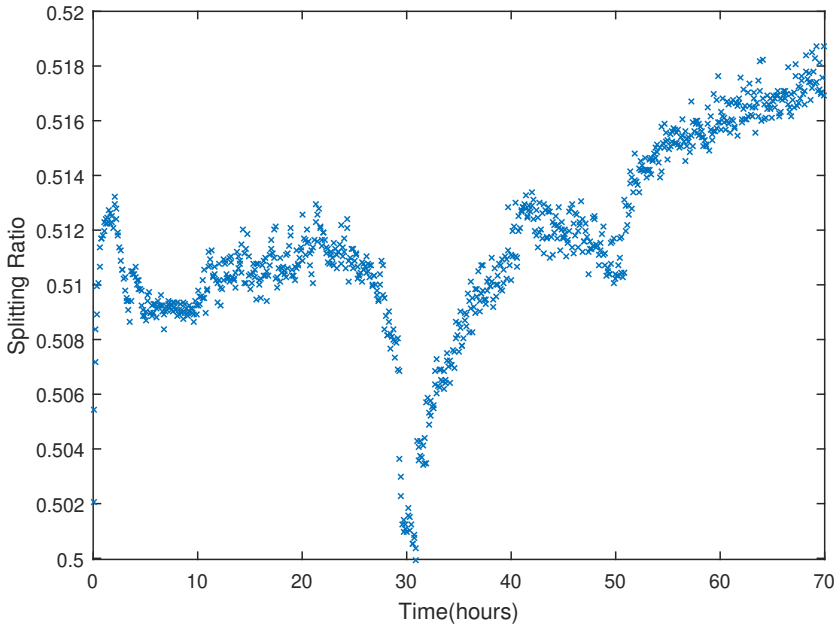


Figure 5.15: Output intensity fluctuation in a three-module setup configured as a 3 dB splitter, its most sensitive arrangement, over a period of three days.

5.5.4 Built-in self-test

In order to simplify resistance measurement of a large number of heater elements a means of performing such measurements automatically was included in the control boards, permitting monitoring of resistance drift; this was accomplished with the use of the bank enable switches combined with an additional capacitor on each bank. Measurement begins by connecting the capacitor to the supply via the bank enable switch, charging it to V_{DD}, the channel to be measured is then selected by activating the corresponding element's analogue-switch; this permits the capacitor to discharge to ground through the element. The time taken for this discharge to take place is a measure of the RC time constant and thus the resistance. A 10-bit analogue-to-digital converter (ADC) on the microcontroller is used to measure the supply voltage and an on-board digital-to-analogue converter (DAC) used to produce a voltage $1/e$ of the supply. This value and the capacitor voltage are then used as inputs to a comparator on the microcontroller, set to give an interrupt when the capacitor voltage drops below the $1/e$ value. A 16-bit counter on the microcontroller is used to record the time associated with this discharge and the counter value returned to the Matlab software for calculation of the resistance.

5.5.5 Three-module Demonstration

A set of three wire-bonded modules was assembled using the procedure of section 5.5.2. It was found that the coupler excess losses in these modules were unexpectedly high compared with those fabricated previously, thought to be due to spot size variation

on the UV writing system. Nevertheless, a useful tuning range of 2π was obtained in phase shifters of all three chips, allowing proof-of-principle experiments to be carried out. To verify the device performed as intendid, three different tests were performed. The modules were configured first to direct light to each of the six output ports in turn, this was followed by a tritter configuration—the results of these tests are displayed in figure 5.16. The system was next programmed with a set of randomly selected 3×3

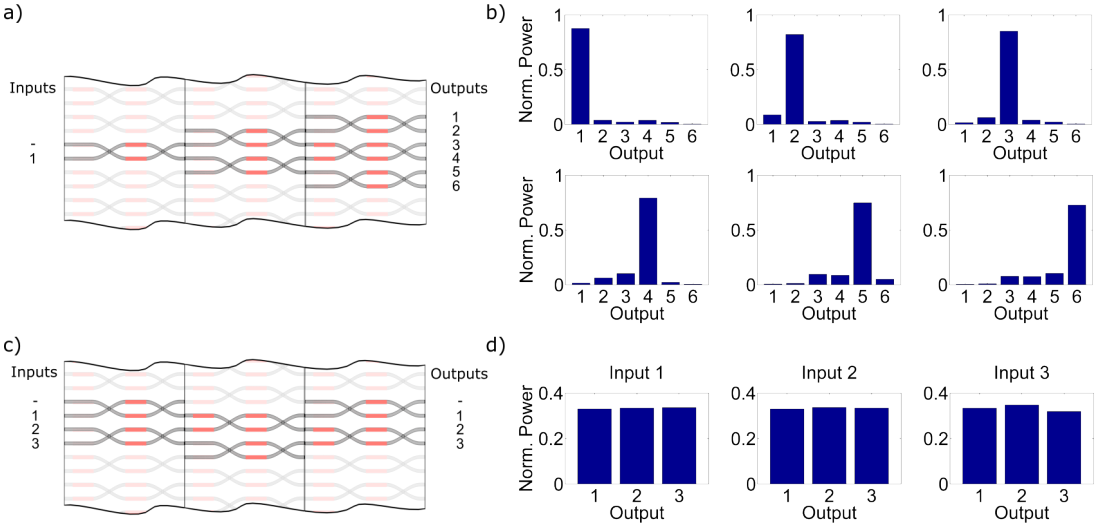


Figure 5.16: a) A three-module network configured to direct light to one of six output ports based on the setting-phase relationships obtained through module characterisation, b) the resulting normalised output intensities. c) The same system configured as a tritter via the adaptive approach of [3], d) the resulting normalised output intensities.

unitaries based on the phase response curves measured in single module tests. In each case the resulting transfer function was measured, normalised to account for loss, and compared with the intended response. The mean fidelity for this set of unitaries was 97.5%, which is comparable to other integrated platforms for quantum optics [2, 6].

5.6 Migration to Telecommunications Wavelengths

In order to reduce device losses, allowing larger experiments to be carried out, it is desirable to operate these devices at 1550 nm, where material and coupling losses will be lowest; in making this move to longer wavelengths there are a number of elements of this system that could pose a potential problem. Firstly, the reduced tuning range may lead to longer heater elements being required, secondly the couplers will need to be longer to achieve the same excess loss; finally the reduced overcladding thickness, used to increase the phase-shifter efficiency, may lead to additional loss at longer wavelengths if the larger mode begins to interact with the metal layers at the surface. The first two of these considerations were take into account in the initial design, the mask layout

also included longer 2 mm phase shifters, as well as designs with increased spacing to account for longer couplers; in all cases the same contact layout is used such that the electrical connections remain unchanged. For the third potential issue, FIMMWAVE modeling was necessary to determine the extent of the interaction; it was found that the additional loss was negligible in comparison with the normal waveguide propagation loss for overcladding thicknesses down to 7 µm. This will need to be tested in practice however due to uncertainty in the precise refractive index profile of fabricated devices.

5.7 Conclusion

A modular reconfigurable system for on-chip quantum optics experiments has been developed composed of duplicate UV-written waveguide chips with thermo-optic phase shifters, interfacing and control circuitry, and allied software. This system has thus-far been demonstrated with wire-bonded modules at 780 nm; efforts have been made to replace these modules with a more robust solder bump bonded variant, however further optimisation of the reflow process is necessary. To-date chip-chip coupling losses of 0.2 dB have been shown along with a propagation loss of 0.3 dB/cm, which would be sufficient for initial experiments to be carried out with four heralded photons using three coupled modules. The stability of the system, while acceptable, has significant room for improvement; efforts to identify and minimise the sources of this variation in the future would be beneficial. The key step in moving this work forward is to shift the operating wavelength of these devices to 1550 nm, in order to further reduce losses. The feasibility of this has been investigated and there are no significant challenges expected in making this transition.

References

[1] P. J. Shadbolt, M. R. Verde, A. Peruzzo, A. Politi, A. Laing, M. Lobino, J. C. F. Matthews, and J. L. O'Brien, "Generating, manipulating and measuring entanglement and mixture with a reconfigurable photonic circuit," *Nature Photonics*, vol. 6, no. 1, p. 6, Dec 2011.

[2] J. Carolan, C. Harrold, C. Sparrow, E. Martin-Lopez, N. J. Russell, J. W. Silverstone, P. J. Shadbolt, N. Matsuda, M. Oguma, M. Itoh, G. D. Marshall, M. G. Thompson, J. C. F. Matthews, T. Hashimoto, J. L. O'Brien, and A. Laing, "Universal linear optics," *Science*, vol. 349, no. 6249, pp. 711–716, Aug 2015.

[3] D. A. B. Miller, "Perfect optics with imperfect components," *Optica*, vol. 2, no. 8, pp. 747–750, Aug 2015.

[4] W. R. Clements, P. C. Humphreys, B. J. Metcalf, W. S. Kolthammer, and I. A. Walmsley, "Optimal design for universal multiport interferometers," *Optica*, vol. 3, no. 12, pp. 1460–1465, Dec 2016.

[5] M. Reck, A. Zeilinger, H. J. Bernstein, and P. Bertani, "Experimental realization of any discrete unitary operator," *Physical Review Letters*, vol. 73, no. 1, pp. 58–61, Jul 1994.

[6] Y. Shen, N. C. Harris, S. Skirlo, M. Prabhu, T. Baehr-Jones, M. Hochberg, X. Sun, S. Zhao, H. Larochelle, D. Englund, and M. Soljačić, "Deep learning with coherent nanophotonic circuits," *Nature Photonics*, vol. 11, no. 7, p. 441, 2017.

Chapter 6

Integrated Single Photon Detectors

6.1 Introduction

In previous collaborative work by the group, an on-chip photon number resolving detector was demonstrated [1], operating in the telecommunications C-band. This work made use of a TES evanescently coupled with a UV-written silica-on-silicon waveguide. UV-written waveguides are highly suited to this application since they are inherently planar, avoiding difficulties with conformity of the thin TES film over the less uniform surface of waveguides produced by many other techniques. An on-chip detection efficiency of 7.2% was demonstrated for the TM mode, and 0.65% in the TE case.

In order to integrate TES detectors, the thin metal film is deposited atop a waveguide with no overcladding, as illustrated in figure 6.1. Since a portion of the propagating optical mode is exposed at the surface it is able to interact with the superconducting film. Tungsten is used as the superconductor due to its high refractive index, this causes the mode to be drawn into the film, where it is absorbed and can trigger a detection event.

Throughout the work of this chapter all optical fabrication and classical chracterisation was carried out by the author at Southampton, while TES fabrication and quantum efficiency measurements were conducted by collaborators at NIST.

6.2 Single Photon Detectors

As on-chip single photon detectors play a major role in this project, a brief background on single photon detection methods is included here. A range of techniques exist for

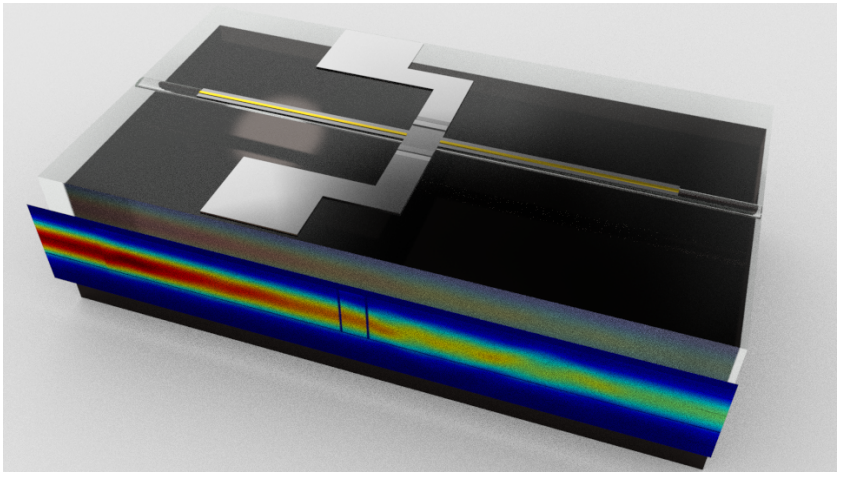


Figure 6.1: Integrated high aspect ratio TES detector concept. The included modal propagation profile is the modelled value for the TM mode of a 200 µm device and was provided by collaborators at Oxford University.

single photon detection, historically the most common have been photo-multiplier tubes and avalanche photodiodes though a range of superconducting thin film based detectors are increasingly being used [2]. Avalanche photodiodes have poor characteristics at telecommunications wavelengths, having high dark count rates and low efficiencies of $\sim 10\%$ [2]; at such wavelengths superconducting detectors offer clear advantages.

6.2.1 Telecom-band Single Photon Detection

There are a number of single-photon detector technologies operating in the telecommunications C-band, where photomultiplier tubes are not available. The most established of these is the InGaAs APDs, though superconducting single photon detectors (SSPDs) are becoming increasingly common in quantum optics laboratories, and there is much research interest in detection via wavelength conversion.

6.2.1.1 Avalanche Photodiodes

An APD is a highly reverse biased P-N junction in which a photon absorption creates a cascade of electron-hole pair generation that leads to breakdown. Efficient silicon based detectors of this type have long been available for operation up to ~ 850 nm and more recently InGaAs based devices for use at 1.5 µm have seen significant improvements. APDs generally have a rather limited bandwidth and suffer from relatively high dark count rates at longer wavelengths, though this is mitigated somewhat through cooling.

6.2.1.2 Up-conversion Based Detection

A perhaps less obvious approach to the detection of longer wavelengths is to upconvert photons to shorter wavelengths where efficient detectors are available. This approach requires a high conversion efficiency to obtain a benefit from higher efficiency detectors.

6.2.1.3 Superconducting Single Photon Detectors

SSPDs make use of the small heat capacity of a thin superconducting film to provide a measurable electrical change as a result of the modest thermal energy obtained through the absorption of a single photon. There are two types of SSPD, SNSPDs and TESs; the key difference being that the former is a 'click' type detector while the latter provides a quantised proportional output with photon number.

6.2.2 Superconducting Nanowire Single Photon Detectors

The superconducting nanowire detector operates on the principle that an absorbed incident photon will cause a local region to exceed the critical temperature and transition into a non-superconducting state [3]. These devices are operated with a bias current near its critical value; the resistive region resulting from an absorption confines the super-current to a narrower region of the nanowire. The device is designed such that this restricted super-current exceeds the critical current density, causing a section of the wire to lose superconductivity and subsequently providing a measurable resistance and hence voltage drop [3].

6.2.3 Transition Edge Sensors

The Transition Edge Sensor is a highly sensitive calorimeter composed of a superconducting thin film held at its critical temperature [4]. An absorbed photon will locally heat the film leading to a measurable increase in resistance, due to the sharp resistance variation associated with the superconducting transition. An important feature of this operation is that the absorption of multiple photons will lead to a cumulative shift in resistance, thereby permitting photon number resolution. This type of detector currently provides the highest recorded fibre-coupled detection efficiency in the near infrared, 95% [4].

The TES is a superconducting film held at its critical temperature; typically, electrothermal feedback is used to achieve this. The TES is cooled well below is critical temperature (T_C) with a voltage bias applied. At the transition temperature, Joule heating of the finite resistance is balanced with the cooling power of the refrigerator through tuning of the bias.

A key aspect of TES design is the choice of material; here a low operating temperature, and hence T_C, is desirable. This determines, in particular, the specific heat capacity of the material, which is critical to the energy resolution. For individual photons to be resolved unambiguously, the thermal energy contributed by each must heat the TES sufficiently to overcome the thermal noise present within the system. The optical absorption spectrum of this material, and any connected absorbers, determine the operating wavelength range of the detector. Tungsten is used exclusively throughout this work, offering a low T_C of $\sim$ 100 mK and high imaginary part of refractive index (n=2.2 k=4.8 at 1550 nm).

6.2.4 Benefits of single photon resolution

Photon-number resolution can permit post selection to remove unwanted multi-photon events, allowing a parametric source to be pumped harder without introducing multi-photon noise, which may in turn permit an experiment to be run faster. Furthermore this capability can permit a new range of experiments, state manipulation through photon subtraction for example by selecting on a weak transmissive photon number resolution (PNR) detector.

6.3 Unclad UV-written Waveguides

As stated previously the detector design makes use of a waveguide structure without an overcladding, which is not commonly used with the UV-writing technique. In order to ascertain more fully the properties of the unclad FHD wafer in use for this work, a fluence test was conducted. A test chip with a series of waveguides with single 1.5 mm gratings at a fixed wavelength was UV-written at a range of fluences; the waveguide length was minimised in order to reduce the writing time and hence the effect of hydrogen out-diffusion over this period. Additional waveguides were added before and after these to permit measurement of sample misalignment.

Characterisation of the fabricated sample under reflection was carried out using a broadband input spectrum provided by an EDFA based ASE source. A 3-dB coupler was used to separate the input from the reflection, the spectrum of which was monitored on an OSA.

Fitting of the Gaussian Bragg peaks in the reflection spectrum for each waveguide allowed the centre wavelengths to be determined for both TE and TM polarisations. From these values and using the known grating period the effective index of each waveguide was determined, the results of which are displayed in figure 6.2 (left), which demonstrate that the fluence range covered is in the linear range of the response.

The difference between the n_{eff} value at a particular fluence and the 'zero-fluence' value, obtained by extrapolating the curve of figure 6.2 to the y-axis, provides an estimate of the UV induced refractive index change; in this case $\sim 1 \times 10^{-3}$ for a fluence of 16 kJ $\cdot$ cm^{-2}.

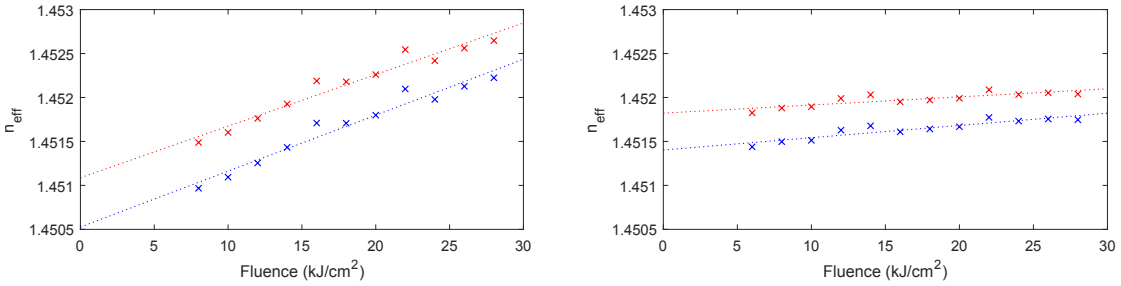


Figure 6.2: The measured fluence dependence of n_{eff} for TM (blue) and TE(green) polarisations for a hydrogen loaded sample (left) and a sample that had been thermally locked at 1100°C (right).

The rate of hydrogen out-diffusion was measured in a similar experiment, providing a shift in n_{eff} of $2 \times 10^{-6} \text{min}^{-1}$ after taking into account the effects of sample misalignment. This rate is significantly faster than in waveguides with an overcladding, for which outgassing only becomes significant after several hours, and would be prohibitive when producing the large, complex circuits which are the eventual goal of this project.

A number of alternatives exist for reducing the effect of out-diffusion, each of which was investigated to some degree; these are the reduction of the outgassing rate during the writing process, reducing the write time required and increase of the FHD layer photosensitivity. One option for completely eliminating outgassing is the process of thermal locking, in which a hydrogenated sample is briefly heated to $\sim$ 1000°C, trapping the hydrogen in the lattice and hence preventing out-diffusion.

Initial thermal locking experiments were carried out on hydrogenated topless samples using a rapid thermal annealer (RTA). The recipe used was developed in other work [5], having a 1 second soak at 1100°C with a 7 second ramp up. After thermal locking a fluence test was again conducted, the results of which are presented in the right plot of figure 6.2. This shows markedly reduced fluence sensitivity compared with the hydrogen loaded case, which is consistent with previous work [6]. Unfortunately the grating strength was found to be $\sim$ 10 dB lower than in the hydrogenated case, and the estimated induced index change was only $\sim 2 \times 10^{-4}$. This would make it difficult to achieve the high grating strengths and low bend losses desired.

Cooling of the chip during the writing process was also attempted in order to reduce the rate of out-diffusion. A modified vacuum chuck was constructed with a Peltier cooler, the hot side of which was in turn cooled via a gravity fed water cooling loop. In similar work by Svalgaard using a single beam setup, cooling to a temperature of -7°C was found to provide a factor of 10 reduction in outgassing rate [7]. The difficulty with

this approach is that ice build-up on the surface of the chip must be prevented, since it would lead to scattering of the UV writing beams. Since complete enclosure of the sample requires a window, which proved problematic in previous work with the dual beam system [5], a nitrogen flow was passed over the sample surface instead to displace water vapour. While ice-free operation was achieved in this way, the correct positioning of the flow was difficult; it had to exclude ice from the entire chip without using such a large flow rate that the chip surface was significantly warmed.

A test chip was written using this system to maintain a surface temperature of $-8°C$, measured using a thermocouple. Characterisation of the sample revealed only a factor of two reduction in out-diffusion. The discrepancy between this value and that expected is likely due to the warming action of the nitrogen flow on the surface. It is believed that CO_2 provided by dry ice boil-off would prove to be a more reliable alternative, since its density should cause it to pool in a partial enclosure around the chip, providing improved water vapour displacement with a reduced flow rate. In initial experiments to this end, moisture in the CO^2 boil-off was found to be a problem; though drying of the vapour should rectify this.

6.4 Integrated TES Detectors

The efficiency of these detectors is governed by the overlap of the mode with the tungsten layer and the interaction length, suggesting that a large TES region will be beneficial. This drive must, however, be balanced with a constraint on the absorber volume, imposed by the fact that the heat capacity of the detector must be small enough to provide the desired single photon resolution. This leads to an optimal geometry that is long and narrow. To further increase the available interaction area without reducing the energy resolution additional absorbers may be added in contact with the TES, again composed of tungsten due to its suitable optical properties.

A further limitation, however, is that longer devices take additional time to thermalise after the absorption of a photon, resulting in poorer temporal characteristics, with a greater timing jitter and dead time. More importantly, if the device takes too long to thermalise, enough energy may be lost to the substrate during this period to prevent correct determination of the photon number, or even prevent a detection. To rectify this, modelling conducted by NIST demonstrated that narrow gold strips may be added in contact with the tungsten to improve thermalisation.

6.4.1 Alignment Approach

A key challenge in fabricating these devices is that of aligning the detector layers relative to the waveguides with sufficient accuracy. This was accomplished by measuring the

back-reflected light from the surface of the chip via a photodetector. Metallic alignment marks were patterned photolithographically prior to hydrogen loading; translation of the beam across the edges of these alignment marks then provided a means of locating the beam relative to these structures. In this case only the position in the direction transverse to the waveguide was necessary, thus alignment mark detection was only carried out in this axis. Initially, these edges were detected with the use of a hardware thresholding circuit, however this proved to be sensitive to particulates on the surface. This was mitigated to a degree by multiple measurements along each edge, but ultimately an alternative approach was pursued. The photodetector output was sampled as the beam was translated across the edge and an error function fitted to the resulting data, allowing the edge to be identified. The scanning pattern was selected to minimize the effect of errors, each pair of alignment marks was scanned in opposite directions and the difference in the resulting positions taken to be the centre of the chip, cancelling out any systematic error in the positional measurement.

A further difficulty encountered was that of ablation of the alignment marks during the edge detection process, in several early devices a waveguide misalignment of up to $\sim$ 10 µm was found, attributed to ablation of the chromium alignment marks during the detection process. After some experimentation it was found that an aluminium layer provided much improved ablation resistance, due to its greater reflectivity at 244 nm. Alignment marks in later devices were thus deposited in aluminium rather than chromium.

This approach proved to be much more robust than previous methods, ultimately permitting a standard error in position of < 200 nm to be achieved reliably, and providing an error estimate. This is particularly important for the high aspect ratio devices described in the next section, since they are highly sensitive to positional misalignment.

6.4.2 High Aspect Ratio Devices

For the purpose of investigating large aspect ratio absorbers and gold thermalisers a new device was to be produced by the collaboration, having TES absorbers of varying length, as well as various thermalising arrangements. To further improve the detection efficiency, a Bragg reflector was to be added to increase the effective absorption length.

In order to measure both the single pass and double pass detection efficiencies it is necessary to characterise with two sources, one at the centre wavelength of the Bragg grating and one out of band. Since the available sources at NIST were spectrally separated by only 0.8 nm, the Bragg grating was required to have a bandwidth significantly below this value. A reflectivity of 100% was also desired, making the grating design more challenging than usual due to the spectral broadening which occurs as a grating saturates. Furthermore, the laser sources were not tuneable and hence the centre wavelength was

to match that of the source after cooling the chip to the operating temperature below 100 mK.

A calibration device was produced to establish the required grating parameters; a length of 4 mm was initially selected to achieve the desired bandwidth, based on previous work. Characterisation revealed a 3 dB bandwidth of 0.6 nm but only a 10% reflectivity, it was also found that the outgassing had led to an n_{eff} value which differed from that measured previously; hence the actual peak wavelength was 0.6 nm less than desired. In the next attempt it was ensured that writing commenced with the same delay after removal of the chip from the liquid nitrogen.

The final device layout is displayed in figure 6.3. Additional weak gratings either side of the detectors allow in-situ grating based loss and absorption measurements to be carried out. Accurate positioning of the waveguides was achieved using a set of chromium alignment marks deposited at NIST, also displayed in the diagram. The positions of these marks were detected by monitoring the back-reflection of the UV beam with a photodetector and thresholding circuit; three measurements were made at each corner and the averages used to set the start position and writing angle.

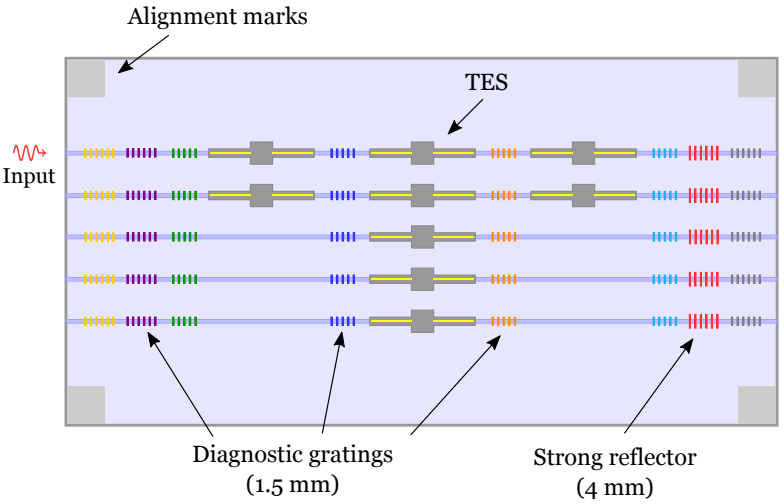


Figure 6.3: Final layout of the high aspect ratio device test chip.

The reflection spectrum of the produced device is presented in figure 6.4. Although the exact reflector wavelength required was not known at this point, the device was suitable for single pass measurements. Deposition of the TES layers was carried out at NIST, prior to mounting of the device at Southampton and PM fibre pigtailed one waveguide at both ends, ready for it to be cooled down at NIST and tested; the final device is displayed in figure 6.5.

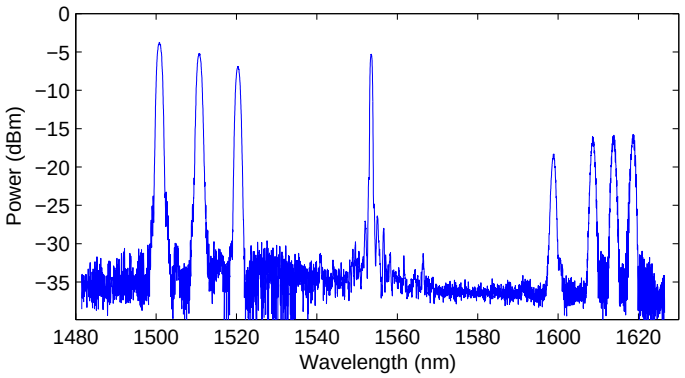
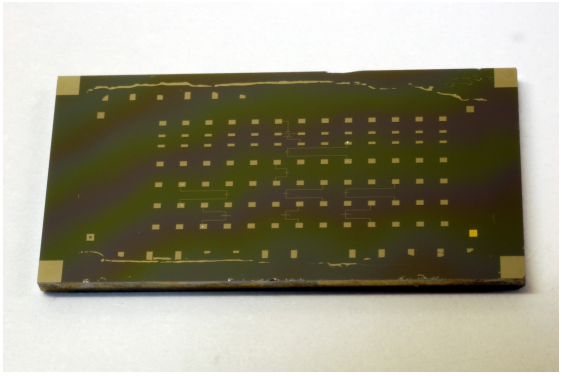
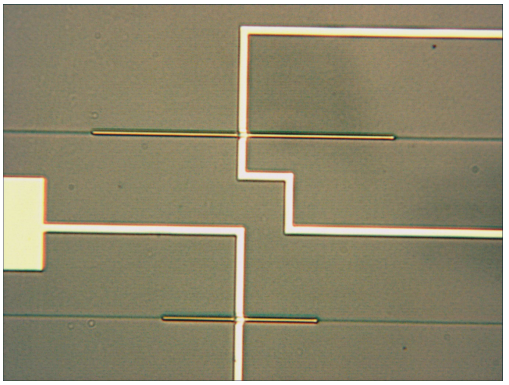


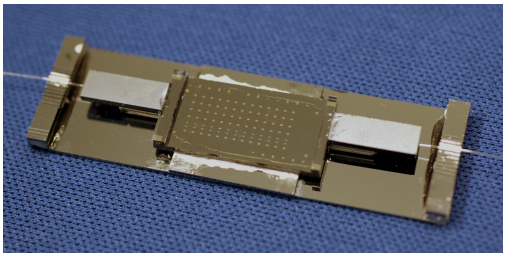
Figure 6.4: Normalised reflection spectrum of a waveguide from the high aspect ratio device test chip before TES deposition (TM polarisation).



(a)



(b)



(c)

Figure 6.5: (a) High aspect ratio device test chip with deposited TESs, clearly visible is the array of wire bond pads. (b) Microscope image of a section of the device, showing TESs of different lengths and the niobium wires. (c) The same device mounted and pigtailed, ready for testing.

6.4.3 Grating Based Absorption Measurements

As a measure of the expected detection efficiency of the device, the classical absorption for each of the detectors was measured using the set of seven interrogation gratings and the grating based loss measurement technique [8]. The reflection spectrum was obtained when launching into each end of the waveguide with an SLED source and a ratio taken to yield the relative power profile, both prior to and after the TES deposition step. The former of these measurements allowed the waveguide loss to be obtained, while the latter permitted the absorption within each detector region to be determined after taking into account the measured waveguide loss. The resulting power profiles for the optimally absorbed TM polarisation are displayed in figure 6.6.

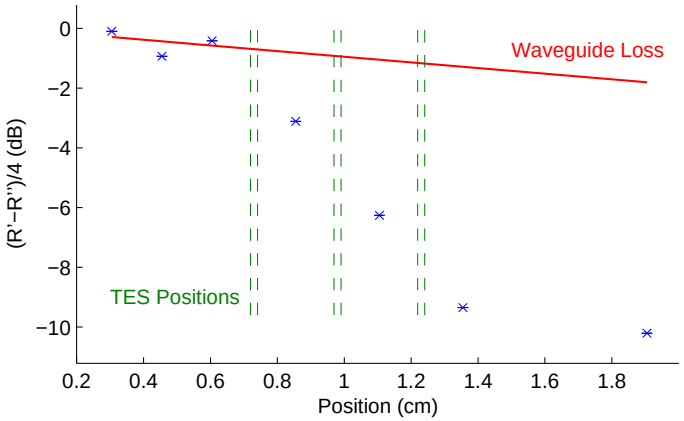


Figure 6.6: The relative power profile obtained for the TM-like mode of the device, each point corresponding to a grating. The TES positions and measured waveguide loss are also shown.

The waveguide loss values obtained in this way were 0.920 dB/cm and 0.947 dB/cm for TE and TM polarisations respectively. The resulting measured absorption values for the three detection regions were 45%, 47%, 50% for TM and 6.8%, 4.4%, 5.8% for TE.

6.4.4 Quantum Efficiency Measurements

The device was cooled down at NIST in an adiabatic demagnetization refrigerator (ADR) to ~ 50 mK, and a calibrated attenuated pulsed 1570 nm laser source used as an input; both the input and transmitted power were measured with a calibrated power meter. A system of over-constrained equations was set up involving the observed count rates at each detector, the three detection efficiencies, two coupling efficiencies, and the waveguide absorption. These were then solved to yield the five unknown parameters for each polarisation, summarised in table 6.1[1]. These values are in good agreement with both the classically obtained values and the values expected from modelling.

[1] Courtesy of collaborators at NIST.

Table 6.1: Individual detection efficiencies η_1, η_2, η_3, and fibre-waveguide coupling efficiencies η_A, η_B obtained by NIST.

Polarisation	η_1	η_2	η_3	η_A	η_B
TM	$46.7 \pm 0.7\%$	$46.6 \pm 0.5\%$	$46.2 \pm 0.6\%$	$36.8 \pm 1.3\%$	$25.6 \pm 1.7\%$
TE	$11.4 \pm 1.9\%$	$11.5 \pm 1.7\%$	$11.2 \pm 1.6\%$	$48 \pm 11\%$	$52 \pm 11\%$

Example output pulse traces for the three sequential detectors are displayed in figure 6.7, clearly demonstrating both photon number resolution, with up to four photons visible in the first detector, and reduction in the average photon number along the length of the device as photons are absorbed.

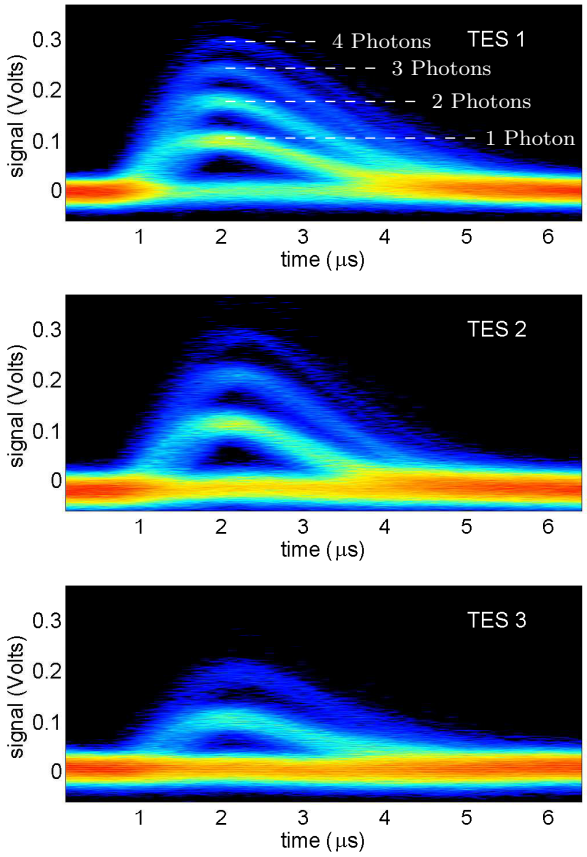


Figure 6.7: A plot showing measured output pulses from each of the three on-chip detectors for an input state with an average photon number > 1, clearly showing the number resolving ability.

6.5 Device Mounting and Coupling

Due to the cryogenic operating temperature of these detectors, < 100 mK, the coupling and mounting of these devices poses a significant problem, requiring a good thermal

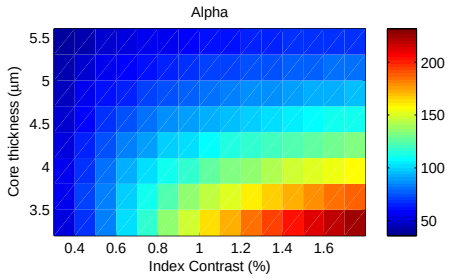
contact between the refrigerator's cold stage and both the planar chip and optical fibres. For this reason, fused quartz strengthening bars were bonded to the top surface of the chip end, using a low index UV-cured glue as shown in figure 2.10, with the purpose of reducing the degree of tilting of the pigtails as the chip is cooled down. The chip was then mounted on a silicon plate with supports for each pigtail; these also had the function of thermally anchoring the fibres to speed up the cool-down process. In devices with multiple waveguides, including those of section 6.4.2, a water-soluble silver paste was used as a thermally conductive adhesive between the chip and baseplate, permitting separation and remounting as necessary.

The stability of the coupling during the cryogenic cooling process may be improved by more closely matching the thermal expansion coefficients where possible. The fused silica strengthening bar in particular has a thermal expansion coefficient of 0.5×10^{-6} °C^{-1}, compared with 3×10^{-6} °C^{-1} for silicon and 3.3×10^{-6} °C^{-1} for the borosilicate v-groove capping layer. The use of a borosilicate strengthening bar was thus trialled, however this higher refractive index layer in contact with the waveguide surface led to a significant additional coupling loss of 1.05 dB. To remedy this, a series of 50 µm deep trenches were diced into the lower surface of the bar, aligned to the waveguides of a test chip. The chip was then pigtailed and mounted, before being cooled to a temperature of $\sim$ 70 K on a cold plate in a bath of liquid nitrogen. This trial did not appear to provide the desired result, with little measurable difference compared with the previous approach. The pigtail did however shift during the curing process, indicated by a change in coupling, likely due to an uneven glue layer and thus differential shrinkage during curing, tilting the pigtail. An uneven glue layer such as this would produce further tilting due to thermal shrinking of the glue as the device is cooled down, which may dominate over thermal expansion mismatch. The relative importance of this effect may be determined by polishing the sample to ensure that the waveguide is normal to the facet and minimising the amount of glue used.

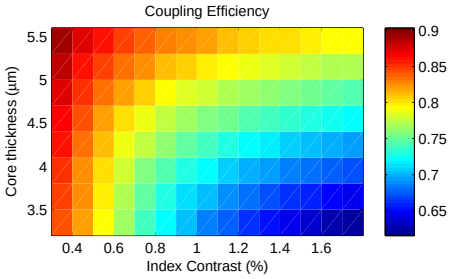
6.6 FHD Parameter Optimisation

A further option for improving device efficiency is the alteration of the core layer properties to increase the absorption in the tungsten layer. This will, however, additionally affect the coupling loss to the input optical fibre, as demonstrated in the simulation results of figure 6.8. In this case a constant absorber width was used, rather than varying with length as in the fabricated devices.

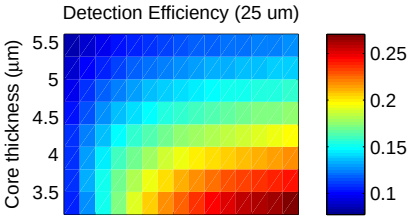
It is found that for short detectors with low efficiency a thinner core is desirable, while for long, high efficiency, detectors the overall device efficiency is dominated by the coupling loss.

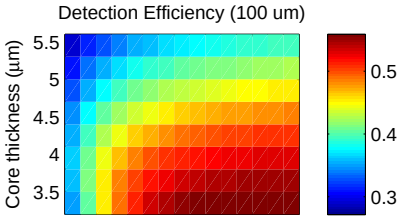


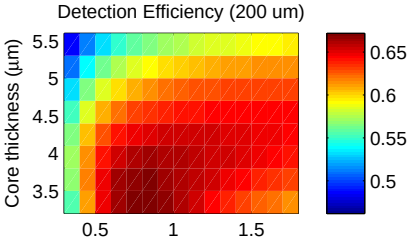
(a)

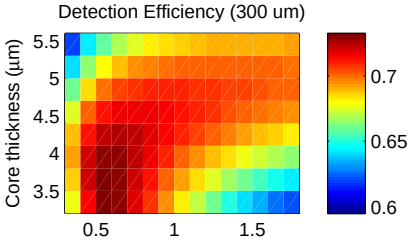


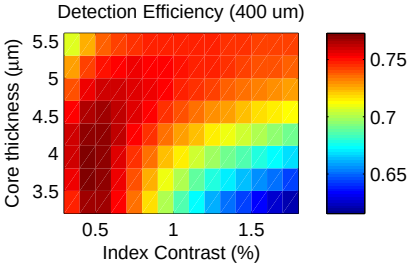
(b)

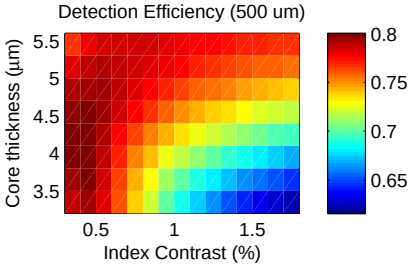










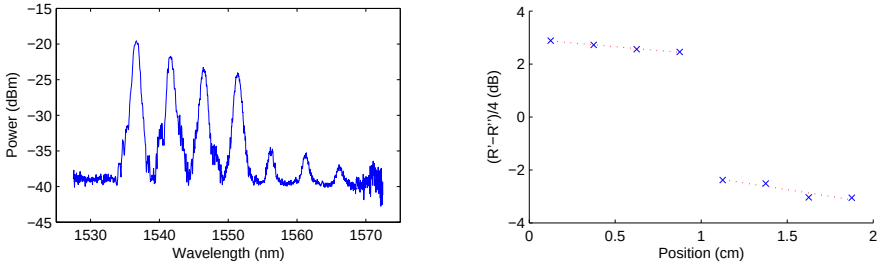


(c)

Figure 6.8: (a) Modelled modal absorption and (b) coupling efficiency with an SMF28 fibre. (c) Total device efficiency for a range of waveguide parameters and detector lengths (TM polarisation).

In order to verify the accuracy of these simulations an absorption test chip was produced using a 4.2 µm core wafer of 1.2% index contrast. A set of ten waveguides was patterned via UV writing, each with a series of weak gratings evenly spaced along the length, and a 100 µm tungsten strip was deposited along the centre of the device at NIST. The grating based loss measurement method [8] was then used to determine the additional loss in the tungsten clad region, allowing an absorption value to be obtained.

The resulting power profile for one of these waveguides is presented in figure 6.9(b), the average absorption value for the set of waveguides was calculated using Beer's law to be 108 cm^{-1}, which may be compared with the value of 54.6 cm^{-1} measured for the previous devices [1]. This shows reasonably good agreement with the simulated value for these wafer parameters, 127 cm^{-1}, suggesting that this new wafer design will indeed significantly improve the TES detection efficiency.



(a) (b)

Figure 6.9: (a) Normalised reflection spectrum and (b) loss profile of an absorption measurement waveguide on a chip with 4.2 µm core thickness (TM polarisation).

6.7 Overcladding layer

A significant disadvantage of device structure used here, without an overcladding, is the increased losses observed; between 0.7 and 1 dB/cm compared with $\sim$ 0.2 dB/cm for typical wafers with an overcladding. This is believed to be due to the sensitivity of the mode to surface defects. A potential solution to this problem would be the addition of a cladding layer after the deposition of the TES layers, however this must be carried out at relatively low temperature (< 150 °C) to avoid increasing the T_C of the tungsten layer. Suitable materials, with a sufficiently low refractive index, include flouro-polymers and MgF.

A further advantage of the addition of an overcladding is the increase in modal overlap with the absorber that would result, This was explored through FIMMWAVE modelling, in which the air surrounding the TES was replaced with a uniform refractive index more closely matched to silica. It was found that in the case of the 5.5 µm core design, a layer index of 1.4 provided an absorption of 98 cm^{-1}, compared with the original 54.6 cm^{-1}.

Adding an overlayer to the 4.2 µm design, again with index 1.4, similarly showed a drastic increase in the absorption, from 127 cm^{-1} to 226 cm^{-1}.

In order to verify this behaviour for an actual device, the absorption of the tungsten test chips was re-measured with a layer of index matching oil, of index 1.4 at 1550 nm, above both the waveguide and absorber. Measurements conducted as previously provided an absorption value of 156 cm^{-1}, demonstrating that the modal absorption had indeed greatly increased, though not to the same degree as suggested by the model; the cause of this discrepancy is as yet unknown.

These results certainly warrant further study, though the approach does complicate the fabrication process somewhat, requiring an extra photolithography and lift-off step in the simplest case.

6.8 Hong-Ou-Mandel Interference Device

A key experiment in the field of quantum optics was the demonstration of non-classical interference of two indistinguishable photons at a beam-splitter, first conducted by Hong et al. in 1987 [9]. Detectors are placed at each output of the beam-splitter and the relative delay between the input photon at each input port is adjusted. For zero phase shift the photons are indistinguishable and the resulting interference causes both to bunch at a single output port, in turn causing the coincidence count rate to drop to zero.

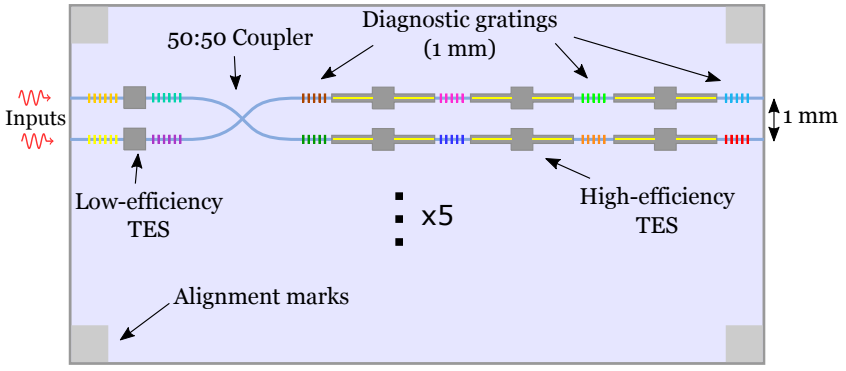


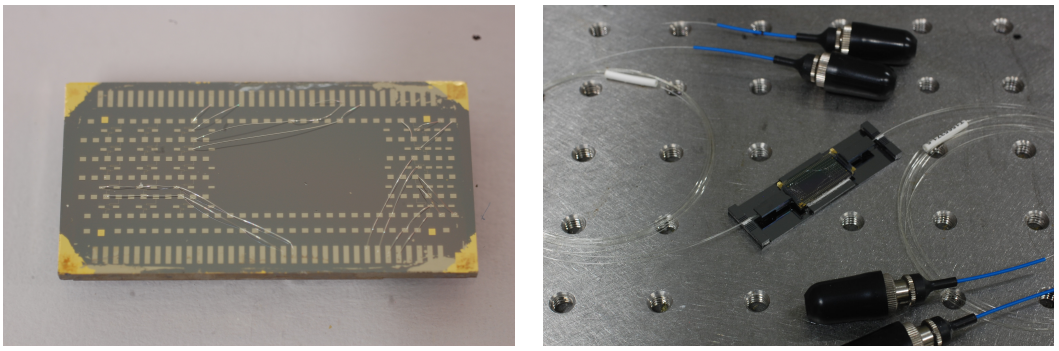
Figure 6.10: The layout of the HOM/photon subtraction test chip. Three high-efficiency detectors are concatenated to maximise detection efficiency in each arm. The weak detector on the input side permits photon subtraction to be carried out through post-selection on output pulses from this detector.

The reproduction of this experiment in an integrated format with on-chip single photon detectors would be an excellent demonstration of this technology, hence efforts were made to achieve this. Since no phase shifter compatible with cryogenic temperatures was available, this element of the experiment was to be implemented off-chip.

As in chapter 5, cross-couplers were selected to implement the beam-splitter over directional couplers, and a compact version of the cross-coupler was again used [10].In this type of experiment a coupling ratio close to 50:50 is desirable so as to maximise the interference dip visibility. Modelling of the cross-coupler arrangement using a split-step BPM program, as outlined in [11], was thus carried out with the aim of determining the crossing angle required to obtain this coupling ratio. Based on this modelling, several test devices were produced to iterate to the required coupling ratio. Coupling ratios were determined through the use of Bragg gratings placed in each arm of the coupler, measurements of the reflection spectrum from each of the four ports were used as detailed in appendix B.

The layout of figure 6.10 was selected, providing a set of couplers with a slightly varying parameters, to improve the chance of achieving the optimal 50:50 coupling ratio and allow for the imperfect yield of the detector fabrication process. In this design, each output has a set of three series detectors with the same high aspect ratio design that was previously successful. A single low-efficiency detector is also present at each input, permitting a broader range of experiments to be conducted.

The final device, shown in figure 6.11, was measured to have a coupling ratio of 55:45 with a crossing angle of 2.05° and an excess coupler loss of 0.4 dB, measured using an additional s-bend waveguide and the grating based loss measurement technique.



(a) (b)

Figure 6.11: (a) The fabricated HOM chip with TES detectors, ready for mounting. 6.11(b) The same chip mounted and pigtailed at input and output with two-port PM fibre V-groove arrays, ready for testing.

6.9 Conclusion

The integration of detectors on-chip avoids losses associated with coupling light out of a waveguide circuit into fibre and back into a detector, as well as enabling detectors to be placed within a network. In this chapter we saw a number of developments to the integrated TES detector; improvements to its on-chip detection efficiency by

increasing the absorption length, both through a novel TES design with additional absorbing regions, and spatial multiplexing of detectors on a waveguide. Tuning of the FHD layer structure, has also been shown to enable higher detection efficiencies to be achieved, though this has yet to be fully exploited; the low-temperature deposition of an overcladding after TES fabrication on a zero-delta waveguide should provide both reduced fibre-coupling losses and increased modal overlap with the active region. The utility of UV-written Bragg gratings in combination with these detectors has also been illustrated, via a modest two-pass efficiency improvement; a more extensive exploitation of this capability, through the design of cavities around weak detectors, is likely to prove fruitful.

While the limited on-chip detection efficiency demonstrated to-date means that as stand-alone detectors these do not improve upon traditional normal incidence TES detectors, with their small fibre-coupling losses, the added flexibility offered by the ability to include partially-transmissive detectors at arbitrary points in a circuit is a clear advantage. Steps have been taken to demonstrate this capability by implementing an integrated HOM and photon subtraction experiment, which should yield exciting results in the near future.

References

[1] T. Gerrits, N. Thomas-Peter, J. Gates, A. Lita, B. Metcalf, B. Calkins, N. Tomlin, A. Fox, A. Linares, J. Spring, N. Langford, R. Mirin, P. G. Smith, I. Walmsley, and S. W. Nam, "On-chip, photon-number-resolving, telecommunication-band detectors for scalable photonic information processing," *Physical Review A*, vol. 84, no. 6, pp. 1–4, Dec 2011.

[2] R. H. Hadfield, "Single-photon detectors for optical quantum information applications," *Nature Photonics*, vol. 3, no. 12, pp. 696–705, Dec 2009.

[3] A. Gaggero, S. J. Nejad, F. Marsili, F. Mattioli, R. Leoni, D. Bitauld, D. Sahin, G. J. Hamhuis, R. Notzel, R. Sanjines, and A. Fiore, "Nanowire superconducting single-photon detectors on GaAs for integrated quantum photonic applications," *Applied Physics Letters*, vol. 97, no. 15, p. 151108, 2010.

[4] A. E. Lita, A. J. Miller, and S. W. Nam, "Counting near-infrared single-photons with 95% efficiency," *Optics Express*, vol. 16, no. 5, pp. 3032–3040, 2008.

[5] C. Holmes, "Direct UV Written Planar Devices for Sensing and Telecommunication Applications," Ph.D. dissertation, University of Southampton, 2009.

[6] I. J. G. Sparrow, G. D. Emmerson, C. B. E. Gawith, S. P. Watts, R. B. Williams, and P. G. R. Smith, "Assessment of Waveguide Thermal Response by Interrogation

of UV Written Planar Gratings," *IEEE Photonics Technology Letters*, vol. 17, no. 2, pp. 438–440, 2005.

[7] M. Svalgaard, "Effect of D2 outdiffusion on direct UV writing of optical waveguides," *Electronics Letters*, vol. 35, no. 21, pp. 1840–1842, 1999.

[8] H. L. Rogers, S. Ambran, C. Holmes, P. G. R. Smith, and J. C. Gates, "In situ loss measurement of direct UV-written waveguides using integrated Bragg gratings," *Optics Letters*, vol. 35, no. 17, pp. 2849–2851, Sep 2010.

[9] C. Hong and Z. Ou, "Measurement of subpicosecond time intervals between two photons by interference," *Physical Review Letters*, 1987.

[10] D. Kundys, J. Gates, S. Dasgupta, C. Gawith, and P. Smith, "Use of Cross-Couplers to Decrease Size of UV Written Photonic Circuits," *IEEE Photonics Technology Letters*, vol. 21, no. 13, pp. 947–949, Jul 2009.

[11] K. Okamoto, *Fundamentals of Optical Waveguides*, 2nd ed. London: Elsevier, 2006.

Chapter 7

Conclusions and Outlook

The aim of this work has been the further development of the UV-written silica on silicon platform for integrated quantum optics experiments; to this end a range of components have been demonstrated at the traditional operating wavelength of 780 nm. Along with this, efforts have been made to migrate the operating wavelength of the various components to 1550 nm, where lower material losses and improved performance may be obtained.

7.1 Sources

A new range of high-purity single-photon waveguide sources based on birefringence matched FWM in UV-written silica has been demonstrated, with manipulation of the FHD layer birefringence permitting production at a range of wavelengths, at both 780 nm and 1550 nm. Arrays of these sources have been shown to have excellent matching, verified through HOM interference measurements. The excellent purity and high brightness of the current source array has already enabled heralded three-photon experiments to be carried out at faster data rates than previously possible; with minor improvements it should be possible to extend this to four heralded photons in the near future. The next step with this type of source is further integration, with the addition of on-chip pump distribution and a fibre-coupled output, reducing the amount of bulk optics and permitting more sources to be used concurrently. The high coupling efficiency of these devices to fibre means that no further integration beyond this is necessary in the near term, since the signal and idler splitting and pump suppression may be carried out in fibre up to the ~ 10 photon regime, before coupling into a further chip where the experiment is conducted. The broad range of operating wavelengths of the 1550 nm sources demonstrated, pumped at 1 µm with generation at 780 nm and 1500 nm, means that simultaneously achieving high fibre coupling efficiency at all three wavelengths is challenging and requires further work. The use of on-chip directional couplers for signal-idler

splitting would greatly reduce the number of fibre components, as well as permitting different fibres to be used for signal and idler, thereby improving the coupling efficiency for the 1550 nm source where they are spectrally widely separated. Alternatively, this mode-matching issue may be avoided by pumping closer to 1500 nm at the cost of requiring telecoms band detectors for both signal and idler photons, which has become less of a problem with the recent wider availability of SSPDs.

7.2 Modulators

In chapter 4, we saw improvements to the thermo-optic based modulators that have become the workhorse of quantum optics in silica; with efficiency increases achieved through optimisation of the heater geometry and reduction of the FHD overcladding thickness. These modulators were then utilised in the modular architecture developed in chapter 5. Alternatives to microheaters were explored for their ability to operate at low temperatures and a piezoelectric stress based modulator produced with this capability; in this case however, the large size of the piezo element is a significant limitation. It would be difficult to incorporate enough modulators on a single chip to produce interesting results using the current approach. An alternative that may be pursued would be the thick film deposition of piezoeletric layers in localised regions; either directly on the waveguide surface or on a separate substrate that is then positioned in contact with and aligned to the waveguide chip. The latter of these options is the most promising in the case of UV written waveguides due to the high temperature annealing requirements of the PZT films, which would be detrimental to the waveguide.

7.3 Circuits

The modular architecture developed in chapter 5 enables a network to be built up of reconfigurable units, that may be characterised individually. This novel approach was both proposed and implemented, along with a computer controlled PWM-based heater driver capable of running ten modules. Proof of principle experiments have been carried out with up to three modules, demonstrating their utility, although quantum experiments have yet to be carried out with these devices. The key next step in this work is to reduce losses by moving to C-band operation, thereby allowing larger networks to be used.

7.4 Detectors

A portion of this work has been concerned with collaborative efforts to improve the integrated number resolving TES detector; chapter 6 detailed the production of a device with multiple high-aspect-ratio TES detectors in series, shown to provide 50% detection per element and a total on-chip quantum efficiency of greater than 87%, with photon number resolution. This device further demonstrates the use of both in-band reflectors to enhance detection efficiency and out-of-band Bragg gratings for the classical characterisation of quantum devices, which highlights the benefit of using Bragg gratings for the interrogation of potentially complex quantum circuits. While this efficiency is respectable, a value close to unity in a single detector element is still desirable. Several promising methods of further improving the detection efficiency were investigated through modelling, including optimisation of the waveguide parameters and the addition of an over-layer. This latter option has the additional benefit of avoiding the elliptical mode-shape seen in these devices, and should improve fibre coupling as a result. A device has also been produced for on-chip HOM and photon subtraction experiments utilising our improved integrated TES detector design, this should provide particularly exciting results in the near future.

7.5 Areas for further investigation

An area in which there is still much to be explored is that of phase shifters suitable for use in the cryogenic environment required by on-chip SSPDs. In such a situation the thermo-optic phase shifters used thus far are unsuitable, as discussed in chapter 4. Experiments should be conducted with elctro-optic polymer modulators for this application. This should eventually lead to devices with both integrated modulators and detectors, which would enable a wider variety of on-chip experiments to be carried out.

Further tests of the UV-poling approach outlined are also likely to prove fruitful, ideally leading to the development of functional on-chip sources. It is believed that absorption in the top contact was limiting the heating in the core layer, and thus the use of alternative contact materials with reduced absorption at 244 nm should be explored, ITO being one possibility.

Appendix A

Publication List

Peer-reviewed Journal Papers

Lead Author (Southampton)

P.L.Mennea, W.R.Clements, D.H.Smith, J.C.Gates, B.J. Metcalf, R.H.S.Bannerman, R.Burgwal, J.Renema, W.S.Kolthammer, I.A.Walmsley, P.G.R.Smith "Modular linear optical circuits," Optica 2018 Vol.(5) pp.1087-1090

J.B.Spring, P.L.Mennea, Metcalf, B.J.Metcalf, P.C.Humphreys, J.C.Gates, H.L. Rogers, C.Soller, B.J. Smith, W.S.Kolthammer, P.G.R.Smith, and I.A.Walmsley, Chip-based array of near-identical, pure, heralded single-photon sources, Optica, 4, (1), pp. 90-96. (2017)

B.Calkins, P.L.Mennea, A.E.Lita, B.J.Metcalf, W.S.Kolthammer, A.Lamas-Linares, J.B.Spring, P.C.Humphreys, R.P.Mirin, J.C.Gates, P.G.R.Smith, I.A.Walmsley, T.Gerrits, S.W.Nam, "High quantum-efficiency photon-number-resolving detector for photonic on-chip information processing," Optics Express 2013 Vol.21(19) pp.22657-22670

Contributor

P.A.Cooper, L.G.Carpenter, P.L.Mennea, C.Holmes, J.C.Gates, P.G.R.Smith, "Integrated optical dual-cantilever arrays in silica on silicon," Optics Express 2014 Vol.22(26) pp.3180131813 C.Sima, J.C.Gates, C.Holmes, P.L.Mennea, M.N.Zervas, P.G.R.Smith, "Terahertz bandwidth photonic Hilbert transformers based on synthesized planar Bragg grating fabrication," Optics Letters 2013 Vol.38(17) pp.3448-3451

C.Sima, J.C.Gates, H.L.Rogers, P.L.Mennea, C.Holmes, M.N.Zervas, P.G.R.Smith, "Ultra-wide detuning planar Bragg grating fabrication technique based on direct UV grating

writing with electro-optic phase modulation," Optics Express 2013 Vol.21(13) pp.15747-15754

C.Sima, J.C.Gates, H.L.Rogers, P.L.Mennea, C.Holmes, M.N.Zervas, P.G.R.Smith, "Phase controlled integrated interferometric single-sideband filter based on planar Bragg gratings implementing photonic Hilbert transform," Optics Letters 2013 Vol.38(5) pp.727-729

Conference Papers

P.L.Mennea, W.Clements, M.T.Posner, R.H.S.Bannerman, D.H.Smith, J.Renema, J.C.Gates, W.S.Kolthammer, I.A.Walmsley, P. G. R. Smith, A Reconfigurable Modular System for On-chip Quantum Optics, CLEO/Europe - EQEC 2017, Munich, Germany. 25 - 29 Jun 2017 (Poster)

P.L.Mennea, B.J.Metcalf, J.B.Spring, A.E.Lita, B.Calkins, P.C.Humphreys, T.J.Bartley, T.Gerrits, M.T.Posner, J.C.Gates, W.S.Kolthammer, S.W.Nam, I.A.Walmsley, and P.G.R.Smith, "UV-written Silica Waveguide devices for Integrated Quantum Optics," CLEO/Europe-EQEC 2015 (Poster)

P.L.Mennea, J.B.Spring, J.C.Gates, B.J.Metcalf, P.C.Humphreys, M.Moore, M.T.Posner, W.S.Kolthammer, I.A.Walmsley, P.G.R. Smith, "Engineering waveguide arrays for high-purity matched four-wave mixing photon sources," European Conference on Integrated Optics (ECIO) Nice 24-27 June 2014

P.L.Mennea, B.Calkins, B.J.Metcalf, T.Gerrits, A.E.Lita, J.C.Gates, W.S.Kolthammer, J.B.Spring, P.C.Humphreys, N.A.Tomlin, A.E.Fox, A.Lamas-Linares, R.P.Mirin, S.W.Nam, I.A.Walmsley, P.G.R.Smith, "High-efficiency Bragg grating enhanced on-chip photon-number-resolving detectors," CLEO/Europe-IQEC 2013 Munich 12-16 May 2013

B.Calkins, P.Mennea, A.Lita, B.Metcalf, W.S.Kolthammer, A.Lamas-Linares, J.Spring, P.Humphreys, R.Mirin, J.C.Gates, P.G.R.Smith, I.A.Walmsley, G.Thomas, S.W.Nam, "High quantum efficiency photon-number-resolving detector for photonic on-chip information processing," CLEO/QELS 2013 San Jose 9-14 Jun 2013 QM4L.1

J.B.Spring, P.L.Mennea, B.J. Metcalf, P.C.Humphreys, M.Moore, J.C.Gates, W.S.Kolthammer, B.J.Smith, P.G.R.Smith, I.A.Walmsley, "Six-photon experiments using an on-chip array of heralded, pure single photons," CLEO/Europe-EQEC 2015

M.T.Posner, P.L.Mennea, N.Podoliak, P.Horak, J.C.Gates, P.G.R.Smith, "45 tilted gratings for silica-based integrated polarizers," CLEO/Europe-EQEC 2015

J.C.Gates, P.L.Mennea, P.G.R.Smith, N.Thomas-Peter, B.J.Metcalf, J.B.Spring, N.K.Langford, I.A.Walmsley, T.Gerrits, A.E.Lita, B.Calkins, N.A.Tomlin, A.E.Fox, A.Lamas-Linares,

R.P.Mirin, S.W.Nam, "Integrated optical platform for photon-number resolving telecom-band detectors for photonic information processing," European Conference on Integrated Optics (ECIO) Sitges Barcelona 18-20 April 2012 Poster

L.G.Carpenter, P.L.Mennea, H.L.Rogers, C.Holmes, J.C.Gates, P.G.R.Smith, "Integrated corner mirrors as a platform for miniaturized planar strain sensing," European Conference on Integrated Optics (ECIO) Sitges Barcelona 18-20 April 2012 (Poster)

J.B.Spring, P.Salter, P.Mennea, B.Metcalf, P.C.Humphreys, M.Moore, J.C.Gates, N.Thomas-Peter, M.Barbieri, X.Jin, N.K.Langford, S.W.Kolthammer, P.G.Smith, M.Booth, P.G.Smith, M.Booth, B.J.Smith, I.A.Walmsley, "Quantum Interference of multiple on-chip heralded sources of pure single photons," Quantum Information and Measurement Messe Berlin, Germany 18-20 Mar 2014

C.Holmes, C.Sima, P.L.Mennea, L.G.Carpenter, J.C.Gates, P.G.R.Smith, "Fabricating fiber Bragg gratings using phase modulated direct UV writing," SPIE Photonics West San Francisco 1-6 Feb 2014

P.A.Cooper, L.G.Carpenter, P.L.Mennea, C.Holmes, J.C.Gates, P.G.R.Smith, "Optomechanical cantilever device for displacement sensing and variable attenuator," Photonics West 2014 San Francisco 1-6 Feb 2014

J.C.Gates, S.G.Lynch, P.L.Mennea, P.A.Cooper, S.Ambran, H.L.Rogers, L.G.Carpenter, C.Sima, D.J.Wales, C.Holmes, P.G.R.Smith, "UV written planar Bragg grating sensors - an overview of fabrication geometries and applications," Advanced Photonics 2013 Puerto Rico 14-17 Jul 2013 (Invited)

H.L.Rogers, C.Holmes, P.L.Mennea, J.C.Gates, P.G.R.Smith, K.R.Daly, G.D'Alessandro, "Experimental observation of coupling between physically separated planar waveguides utilising tilted Bragg grating structures," European Conference on Integrated Optics (ECIO) Sitges Barcelona 18-20 April 2012

M.T.Posner, R.H.S.Bannerman, D.H.Smith, P.L.Mennea, J.C.Gates and P.G.R. Smith. , High-birefringence direct-UV-written silica waveguides for heralded single-photon sources at telecom wavelengths, CLEO/Europe - EQEC 2017, Munich, Germany. 25 - 29 Jun 2017 (Poster)

R.H.S.Bannerman, J.C.Gates, C.Holmes, P.L.Mennea, C.Sima, P.G.R.Smith, "Small-spot UV-written Apodised Fibre Bragg Gratings at 780 nm," CLEO/Europe-EQEC 2015

C.Sima, J.C.Gates, H.L.Rogers, P.L.Mennea, C.Holmes, M.N.Zervas, P.G.R.Smith, "Phase modulated direct UV grating writing technique for ultrawide spectrum planar Bragg grating fabrication," SPIE Photonics West San Francisco 2-7 Feb 2013

C.Sima, J.C.Gates, H.L.Rogers, P.Mennea, C.Holmes, M.N.Zervas, P.G.R.Smith, "Interferometric integrated planar Bragg filter for all-optical single-sideband suppression," European Conference on Integrated Optics (ECIO) Sitges Barcelona 18-20 April 2012

P.Cooper, C.Holmes, L.Carpenter, C.Sima, P.Mennea, J.C.Gates, P.Smith, "Silica microbeams for tunable Bragg gratings," CLEO-Europe/IQEC 2013 Munich 12-16 May 2013

J.C.Gates, S.Lynch, C.Holmes, C.Sima, P.Mennea, "Integrated planar Bragg grating stabilized diode lasers," CLEO-Europe/IQEC 2013 Munich 12-16 May 2013 CK-P.33 (Poster)

C.Sima, J.C.Gates, C.Holmes, H.L.Rogers, P.L.Mennea, M.N.Zervas, P.G.R.Smith, "Phase modulation technique for high modulation wide band planar Bragg grating fabrication," CLEO/Europe-IQEC 2013 Munich 12-16 May 2013 CI-P.16 (Poster)

P.G.R.Smith, J.C.Gates, C.Holmes, L.G.Carpenter, D.O.Kundys, P.L.Mennea, M.T.Posner, "At the Cross-Roads of Effective Quantum Information Processing with Integrated Optical Gates," Photonics North Montral, Canada 28-30 May 2014

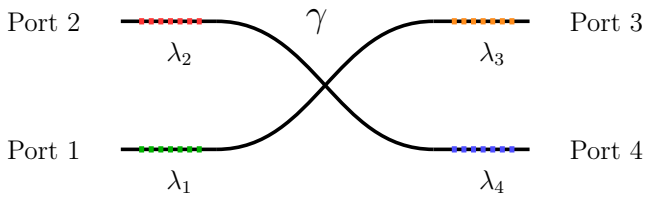
P.G.R.Smith, J.C.Gates, C.Holmes, L.G.Carpenter, D.O.Kundys, P.L.Mennea, M.T.Posner, "Integrated optical circuits for quantum information processing," International Conference on Optics & Optoelectronics (ICOL) Dehradun India 5-8 Mar 2014 (Invited)

C.Holmes, H.Rogers, K.Daly, L.Carpenter, C.Sima, P.Mennea, J.C.Gates, G.D'Alessandro, P.G.R.Smith, "Tilted planar Bragg grating refractometers," CLEO-Europe/IQEC 2013 Munich 12-16 May 2013 CH-P.1 (Poster)

T.Hiemstra, A.Eckstein, U.Hoff, J.Spring, B.Metcalf, P.Humphreys, T.Bartley, P.L.Mennea, J.C.Gates, P.G.R.Smith, S.Kolthammer, I.A.Walmsley, "Generating Telecom-Band Pure Heralded Single Photons On A Silica Chip," CLEO/Europe-EQEC 2015 (Poster)

Appendix B

Coupling Ratio Derivation



We model the reflected power from a grating at a point i on the path $1 \rightarrow 4$ in the forward (R_{14i}) and reverse (R'_{14i}) launch directions as

$$R_{14i} = I_i \eta_1^2 e^{-2\alpha x_i} \cdot \gamma^2 \mathrm{H}(x_i - a) \tag{B.1}$$

$$R'_{14i} = I_i \eta_4^2 e^{-2\alpha(L - x_i)} \cdot \gamma^2 \mathrm{H}(L - x_i - a), \tag{B.2}$$

where I_i is the product of source intensity and reflectivity for grating λ_i at x_i, η_i is the coupling efficiency of port i, α is the loss coefficient in cm^{-1}, γ is the splitting ratio of the crossing region at position a and $\mathrm{H}(x)$ is the Heaviside step function.

Taking the ratio of forward and reverse reflected powers as follows gives a measure of the relative power along the path, working in logarithms and expressing the power in nepers for brevity,

$$\ln(R_{14i}) = \ln(I_i) + 2\ln(\eta_1) - 2\alpha x_i + 2\ln(\gamma)\mathrm{H}(x_i - a) \tag{B.3}$$

$$\ln(R'_{14i}) = \ln(I_i) + 2\ln(\eta_4) - 2\alpha(L - x_i) + 2\ln(\gamma)\mathrm{H}(L - x_i - a) \tag{B.4}$$

$$P_{14i}[\text{Np}] = \ln(R_{14}) - \ln(R'_{14}) \tag{B.5}$$

$$= 2\ln(\eta_1) - 2\ln(\eta_4) + 2\alpha(L - 2x_i) + 2\ln(\gamma)\text{H}(x_i - a) - 2\ln(\gamma)\text{H}(L - x_i - a) \tag{B.6}$$

$$= 2\ln(\eta_1) - 2\ln(\eta_4) + 2\alpha(L - 2x_i) + 2\ln(\gamma)(\text{H}(x_i - a) - \text{H}(L - x_i - a)) \tag{B.7}$$

$$= \frac{P_{14i}[\text{dB}]}{10\log_{10}(e)} = \frac{1}{4.34}P_{14i}[\text{dB}]. \tag{B.8}$$

Similarly we have:

$$P_{13i} = 2\ln(\eta_1) - 2\ln(\eta_3) + 2\alpha(L - 2x_i) + 2\ln(1-\gamma)(\text{H}(x_i - a) - \text{H}(L - x_i - a)) \tag{B.9}$$

$$P_{24i} = 2\ln(\eta_2) - 2\ln(\eta_4) + 2\alpha(L - 2x_i) + 2\ln(1-\gamma)(\text{H}(x_i - a) - \text{H}(L - x_i - a)) \tag{B.10}$$

$$P_{23i} = 2\ln(\eta_2) - 2\ln(\eta_3) + 2\alpha(L - 2x_i) + 2\ln(\gamma)(\text{H}(x_i - a) - \text{H}(L - x_i - a)) \tag{B.11}$$

The difference in power either side of the coupler is given by,

$$\Delta P_{14} = P_{14\lambda_4} - P_{14\lambda_1} \tag{B.12}$$

$$\begin{aligned} &= 2\ln(\eta_1) - 2\ln(\eta_4) + 2\alpha(L - 2x_4) + 2\ln(\gamma) \\ &\quad - 2\ln(\eta_1) + 2\ln(\eta_4) - 2\alpha(L - 2x_1) + 2\ln(\gamma) \end{aligned} \tag{B.13}$$

$$= 4\alpha(x_1 - x_4) + 4\ln(\gamma). \tag{B.14}$$

This removes the dependence on coupling efficiency. Similarly,

$$\Delta P_{13} = 4\alpha(x_1 - x_3) + 4\ln(1-\gamma), \tag{B.15}$$

$$\Delta P_{24} = 4\alpha(x_2 - x_4) + 4\ln(1-\gamma), \tag{B.16}$$

$$\Delta P_{23} = 4\alpha(x_2 - x_3) + 4\ln(\gamma). \tag{B.17}$$

We can further eliminate the loss terms by assuming these losses are the same for two arms, i.e. $\alpha(x_1 - x_4) = \alpha(x_2 - x_4)$, as follows:

$$\Delta P_{14} - \Delta P_{24} = 4\alpha(x_1 - x_4) + 4\ln(\gamma) - 4\alpha(x_2 - x_4) - 4\ln(1-\gamma) \tag{B.18}$$

$$= 4\ln(\gamma) - 4\ln(1-\gamma) \tag{B.19}$$

$$= 4\ln\left(\frac{\gamma}{1-\gamma}\right) \tag{B.20}$$

$$\Rightarrow \frac{\gamma}{1-\gamma} = \exp\left(\frac{1}{4}(\Delta P_{14} - \Delta P_{24})\right) \tag{B.21}$$

$$\Rightarrow \frac{1}{\gamma} - 1 = \frac{1}{\exp\left(\frac{1}{4}(\Delta P_{14} - \Delta P_{24})\right)} \tag{B.22}$$

$$\Rightarrow \gamma = \frac{1}{1 + \exp\left(-\frac{1}{4}(\Delta P_{14} - \Delta P_{24})\right)} \tag{B.23}$$

Here we have not included a term representing the excess loss of the coupler, but this would similarly be cancelled out at this stage. Finally, converting from nepers to dB gives,

$$\gamma = \frac{1}{1 + \exp\left(-\frac{10}{4}\log_{10}(e)(\Delta P_{14} - \Delta P_{24})\right)} \tag{B.24}$$

$$\approx \frac{1}{1 + \exp\left(-1.086(\Delta P_{14} - \Delta P_{24})\right)}. \tag{B.25}$$

Appendix C

Wafer Parameters

Table C.1: Measured parameters of the wafers used throughout this work.

Identifier	Design Wavelength	n Core	Core Thickness	n Cladding	Overclad Thickness	Subtrate Thickness	Propagation Loss	Notes
NB88	780 nm	1.460 @ 633 nm	4.9 µm		7 µm	650 µm	0.4 dB/cm	Wafer used for initial modular chips & the 760 nm FWM source array.
NB100	780 nm	1.461 @ 633 nm	4.9 µm		7 µm	1 mm	0.4 dB/cm	Used for the high-birefringence telecom FWM source.
NB215	780 nm	1.465 @ 633 nm	4.0 µm		7 µm	1 mm	0.35 dB/cm	Second generation of modular chips.
NB254	780 nm	1.458 @ 633 nm	3.0 µm		7 µm	1 mm	0.35 dB/cm	Third generation of modular chips.
DN127	1550 nm	1.453 @ 1553 nm	5.4 µm	N/A	N/A	1 mm	0.9 dB/cm	Used for the high efficiency TES detector.
NB38	1550 nm	1.461 @ 1553 nm	4.2 µm	N/A	N/A	650 µm	0.75 dB/cm	TES layer absorption tests.
NB99	1550 nm	1.490 @ 633 nm	6.4 µm	N/A	N/A	1 mm	0.7 dB/cm	Phosphogermanate, used for the HOM & photon subtraction test chip.

Appendix D

Modular Unit Fabrication Guide

D.1 Sample Preparation

Chips are first diced from the required wafer in the typical fashion, facet quality is not critical at this stage since they will be subsequently polished. Chips are diced with a width of 10 mm, the minimum required for the wiring layout, and 0.5 mm longer than the final desired length to compensate for material lost during the polishing process, the actual length depending on the operating wavelength. Samples are then labeled with a diamond scribe on the back surface and wrapped in lens tissue for hydrogen loading, which proceeds for a minimum of three days at 120 Bar.

D.2 UV Writing

Upon removal from the hydrogen cell the chip is stored in liquid nitrogen prior to writing. Care should be taken to ensure that any angular misalignment is corrected relative to the X-axis (long edge) of the chip, since the facets will be polished orthogonal to this edge.

D.3 Lift-off Processes

Photolithography

The sample is first solvent cleaned, followed by a brief (5 minute) plasma clean in an oxygen atmosphere. The photolithography recipies for the heater, wiring and capping layers are the same; the target resist thickness is 2µm, achieved using S1813 spun at 4000 rpm for 30 s. Exposure is via hard contact with a dose of 120 $\mathrm{mJ \cdot cm^{-2}}$. A 3 minute pre-development chlorobenzene soak is used to introduce an undercut in the resist, making lift-off easier; excess chlorobenzene is evaporated with a nitrogen gun. Development is 90 s in MF319, agitated between 30 and 60 seconds, rinsed with DI water and nitrogen blow dried.

In the case of the pads a two-layer resist is used to achieve a significant undercut, required due to the thickness of metal required. First a layer of LOR-30B is spun on at 3500 rpm, the thickness of this resist leads to significant edge beading on chips, which must be removed since it interferes with alignment during the subsequent exposure step, adhering to the mask. Edge beading may be removed by running a pair of plastic tweezers around the edge of the chip while taking care not to damage any features. This layer is baked on a hotplate at 120°C for 90 s to set the degree of undercut that will be achieved during development. We follow this by spin coating a layer of S1813 at 4000 rpm as with the previous liftoff processes.

Lift-off

Lift off is carried out by immersing the sample in SVC-14, a DMSO based positive resist stripper, within an ultrasonic bath. Multiple chips can be handled at the same time but as the Petri dish fills with floating particulates these should be skimmed off to reduce the chance of redeposition on the substrate. Once all desired areas have been removed the sample should be removed under a stream of solvent, ensuring particulates are not collected as the sample is drawn through the surface, before rinsing with DI water and blow-drying with nitrogen.

Lift-off I: NiCr Heaters

The e-beam deposition parameters with typical beam currents and rates are given in table D.1. Extra care should be taken when ramping the beam current between 30 and

Table D.1: E-beam deposition parameters for the heater elements.

Material	T	I (Typical)	Rate (Typical)
Ti	5 nm	55 mA	0.03
NiCr	300 nm	80 mA	0.1

40 mA since this corresponds to the melting point of NiCr. This transition must occur slowly to allow the crucible to thermalise fully, otherwise an eruption can occur causing loss of a large amount of material from the crucible.

Lift-off II: Cu Wiring

Table D.2: E-beam deposition parameters for the wiring layer.

Material	T	I (Typical)	Rate (Typical)
Ti	5 nm	55 mA	0.03
Cu	200 nm	20 mA	0.1

Lift-off III: Ag Pads

Table D.3: E-beam deposition parameters for the pad layer.

Material	T	I (Typical)	Rate (Typical)
Ti	5 nm	55 mA	0.03
Cu	20 nm	20 mA	0.1
Ag	2 µm	25 mA	0.18

This deposition uses almost an entire crucible of silver, ensure that the crucible is $\frac{3}{4}$ filled before use.

Lift-off IV: SiO2 Capping Layer

Table D.4: E-beam deposition parameters for the capping layer.

Material	T	I (Typical)	Rate (Typical)
Ti	5 nm	55 mA	0.03
SiO2	300 nm	15 mA	0.1

This deposition is carried out without an oxygen flow, as an oxygen deficient layer is acceptable in this case.

D.4 Facet Polishing

Prior to polishing it is necessary to glue on the strengthening bars, these are positioned one at a time with the use of an engineers square. Once the bar is aligned to the edge a drop of OP-4 20632 UV cured glue should be applied to the narrow edge of the bar on each side, using a 24 swg wire. Allow the glue to wick for 5 minutes before curing with a UV gun for 50 s. Once all bars are tacked in place further glue may be applied to the long edge of each bar and allowed to wick in and create a uniform layer between the chip and bar; this process may be sped up by heating the sample to 40°C. This glue layer should then be cured as before. Once the strengthening bars are in place a protective layer of photoresist must be formed over the top surface of the sample prior to polishing, to prevent polishing compounds from damaging the metal layers or leaving any residue. This is necessary since removal of the resulting residue would otherwise require use of solvents that would also attack the glue layer holding the strengthening bars on.

Lapping and polishing are carried out on an Allied Technology Opti-Prep with the recipe of table D.5. Samples should be mounted in a stack with a sacrificial chip at the top and bottom, since some form error is expected at these edges. Lapping is followed with

Table D.5: Sequence of lapping films used in polishing modular chips.

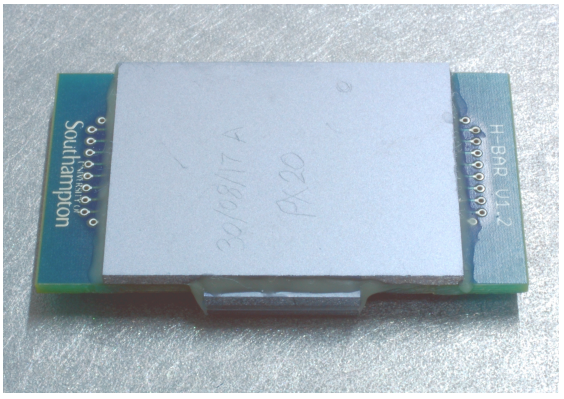
Type	Grit	Material	Termination condition
Film	15 µm	SiC	Samples flat
Film	9 µm	SiC	45 µm removed
Film	5 µm	SiC	20 µm removed
Film	5 µm	AlO_3	15 µm removed
Film	3 µm	AlO_3	15 µm removed
Film	1 µm	AlO_3	3 µm removed

4 minutes of polishing using OpTec 0.5 µm alumina suspension.

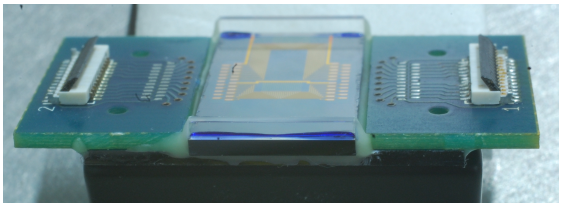
D.5 Mounting and Electrical Connection

In the case of the wirebonded variant the chip is mounted on a 23 × 10.5 mm piece of 1 mm thick silicon. The PCB is cut to a width of 10.5 mm with a dicing saw and its central bridge removed and filed flat. The construction is such that disassembly is possible if required, should the facets require repolishing for example. UV-cured glue is thus used, rather than epoxy, which must be applied in light accessible areas to permit curing.

The chip is positioned in the middle of the mount on a small drop of thermal paste, ensuring that it is square to the mount. A narrow strip of Dymax OP-67 opaque UV-glue is applied along each side of the chip and cured to hold it in place. The two PCB halves are then positioned either side of the glue strips and more glue added to fill in the gaps between the PCBs and the chip. Once this is cured the assembly is flipped upside down and a strip of glue applied to the edges of both chip and PCBs visible from the underside, as seen in figure D.1. Finally, a small drop of glue is added to support each the strengthening bars on each of their narrow edges, to prevent them breaking off during de-pigtailing. The mount may then be wirebonded via aluminium wedge bonding.



(a)



(b)

Figure D.1: (a) Bottom and (b) end view of a mounted modular chip, showing the gluing locations.

For the flip-chip variant the first step is the application of the solder bumps to the h-bar PCB. The solder stencil is aligned to the PCB via the alignment holes and a strip of low temperature solder paste (138°C Bi80/Sn20) applied next to the pad strip. Solder paste should be kept refrigerated and must be allowed to warm to room temperature before

use. A steel squeegee is used to draw the paste across the pads, filling the thickness of the stencil. The stencil is then removed and the results inspected; if any of the pads have been left connected the paste should be removed with methanol and the process repeated. The PCB should then be placed on a hotplate at 150°C until the paste at all pads has visibly balled up, taking $\sim$ 5 minutes. Next the h-bar is carefully diced to a width of 10.5 mm, ensuring the pads are central and the diced edges are square. The PCB is positioned on top of the modular chip and should fit exactly between the two strengthening bars, transverse alignment is verified using the 1 mm alignment holes, which should line up with the edges of the chip. The assembly is then placed on a hotplate at 150°C and after warming a small amount of pressure applied to the top of the PCB to ensure connection of all of the pads; the assembled chip should then be promptly removed and allowed to cool. It is necessary to perform a connectivity test since inspection of the bonds is not possible without X-ray imaging.

Appendix E

Modular System Operating Manual

E.1 System Components

The modular system is made up of a number of components: the modular chips themselves, which have an attached h-bar PCB for electrical connections, breakout boards, control boards and allied firmware, and a MATLAB library for software control.

Modular h-bar chips

These modules have two 25-contact FFC connectors carrying the 40 control signals for the on-chip phase shifters.

Breakout boards

Each of these boards has a set of ten 25-contact FFC connectors for connecting both sides of 5 modules, which are routed in pairs to five 40-pin 1.27 mm pitch IDC connectors used to connect to the control boards.

Control boards

Each control board generates 80 control signals, for two chips, output via the two 40-pin IDC connectors. The board has three main components, a microcontroller which receives commands over a USB interface, an FPGA which generates the corresponding PWM signals, and an analogue switch bank controlled by these signals which provides the heater drive outputs. The control boards are stackable and communicate via a three-pin i2c connector (J1), requiring a single USB connection; when multiple boards are connected the board detecting a USB connection behaves as a master and enumerates all other controllers on the bus, before routing incoming USB commands to the required slave board.

FPGA firmware (HBarContFPGA)

The FPGA maintains a register of setpoints for the 40 phase shifter pairs, arranged in two pages for the two ports. Each value is used in a less than comparison with a 10-bit counter to produce a corresponding PWM output signal, the two ports are tested and registered on alternate clock cycles to reduce hardware requirements. The setpoints and other registers are configured by commands received from the master microcontroller via i2c. The FPGA clock is generated on-chip using a built-in PLL.

Microcontroller firmware (HBarContAVR)

This component handles USB communication with the computer and issues commands to the FPGA via i2c, it also handles heater resistance measurements as described in section 5.5.4, and configuration of the power supply (see section E.2.1). The microcontroller operates at a clock frequency of 8 MHz, generated with an on-board crystal oscillator.

Matlab Package (HBar)

The MATLAB library contains a class representing the interface (HBar.Interface), having functions to configure the control boards and set the phase shifters. Since it is difficult to keep track of which controller channel corresponds to which phase shifter in a multi-chip experiment an additional class (PhysicalMapping) was implemented to aid with this. The mapping is configured with the use of a GUI which allows chips, controllers and breakout boards to be added and connected together by port number, according to the experiment in progress. SetHeater commands can then be given the chip and element IDs and the physical channels determined automatically based on this mapping.

E.2 Operating Guidelines

V2.0 of the h-bar controller is fitted with ADG453 analogue switches, which are capable of switching voltages up to 36V. In V2.1 of the board these switches were replaced with DG613s for the purpose of improving the switching speeds, these have a reduced maximum supply voltage of 21V. The maximum operating current while running multiple switches is limited by the maximum switching current of the bank control switches, 100 mA, the total current for all switches on a bank should not exceed this value. If higher currents are necessary the bank bypass jumpers may be used, in which case the maximum drive current is limited by the ground lines on the FFC ribbon cable (200 mA). There are two ground connections per port, giving a maximum channel current of 40 mA. At the maximum drive voltage this requires the heater element resistances to exceed 525 Ω. In the event of a short circuit or other fault this IC will fail first and may easily be replaced. The recommended operating limits of the system are summarised in table E.1.

E.2.1 Power Supply Adjust

The hBar controller v2.1 has a programmable power supply capable of providing a regulated analogue-switch supply voltage with 64 levels in the range 0–V_{in}. This is

Table E.1: Recommended operating limits for the modular system components.

Parameter	Conditions	Limit v2.0 [1]	Limit v2.1 [2]	Unit	Limiting Component
V_{supply}		37	22	V	Main analogue switches
I_{supply}		1.5	1.5	A	LM317 regulator
I_{Out} (Bank total)	Bank enable bypass jumpers not fitted	100	100	mA	Bank analogue switches
I_{Out} (Any channel)		100	30	mA	Main analogue switches
I_{Out} (Any channel)		40	40	mA	FFC ribbon ground lines

[1] ADG453 variant [2] DG613 variant

accomplished with the use of a digital potentiometer configured via a peripheral two-wire interface (`PSA_UD, PSA_CS`) by the microcontroller. The 6-bit setting code may be selected using hBar.setSupplyLevel(value); this setting is stored in non-volatile memory and will persist after a power-cylce. It should be noted that the supply voltage is not linearly related to this value, with more values corresponding to the upper portion of the voltage range than the lower.

E.3 Mapping Configuration

The mapping configuration GUI displayed in figure E.1 is used to define the connections present in a setup, allowing the library to determine the address of a given heater pair. A mapping may be configured by first adding the devices present in the system (five controllers, two breakout boards, etc.) it will place the ports of these in the list on the left. The lists at the bottom refer to A-type connections, the 25-contact FFC ribbons, while those at the top correspond to B-type, the 40-pin IDC ribbons.

For each physical connection in the system the two end ports are selected from the lists and the connect (>) button pressed to add a new connection to the connections list on the right. Ports in use are removed from the free ports list on the left. If a connection is inverted (i.e. the connector is flipped round) the corresponding list entry may be selected and the invert button pressed, which will add an inversion indicator (i) to the entry. Individual connections may be removed by selecting them and pressing disconnect (<), while all connections may be disconnected with the << button.

When ready the mapping may be saved with the Save button and set as the active mapping with the Set button. A previously created mapping may also be used with the Load button.

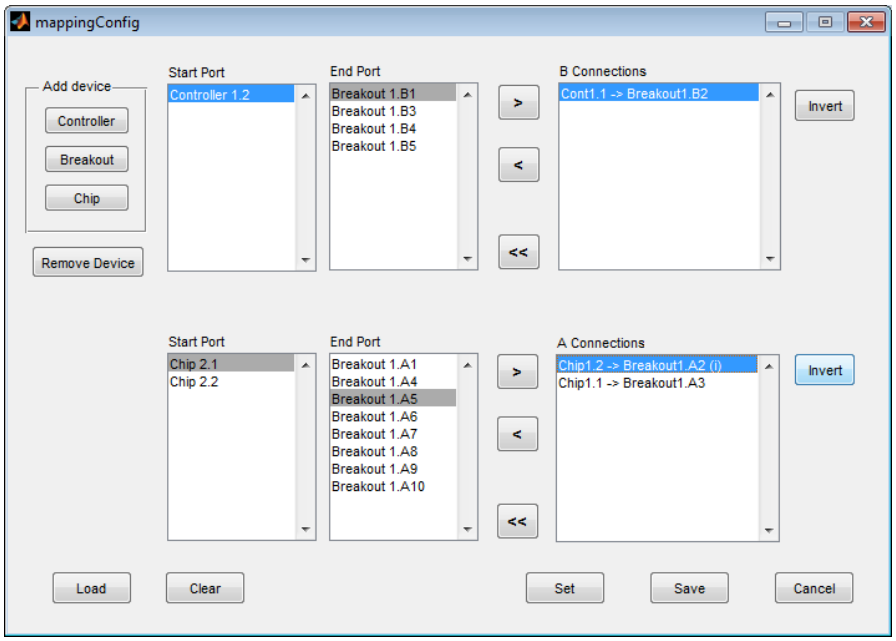


Figure E.1: Mapping configuration GUI (part of the HBar Matlab package).

E.4 Firmware Updating

E.4.1 Microcontroller

The ATMega32U4 microcontroller used has a pre-programmed USB bootloader for in-system programming via USB, the application must thus jump to the bootloader section for this to take place. This is accomplished by sending a special instruction to the controller '00, 55, AA, 55, AA', this will cause the device to reset in bootloader mode and appear as a separate USB device which can then be programmed. A specific command, UpdateFirmware, is included in the MATLAB library for firmware upgrades, this sends the bootloader jump command followed by running a windows batch file that programs the device with the given hex file. It then resets the controller to start normal operation and reconnects to it. All controllers run the same firmware, capable of acting as both master and slave, though each requires a different device ID since this determines the address on the bus. Each board must thus be programmed separately; remove the cover from the stack and for each board in turn connect a USB-B cable and run the firmware upgrade command.

E.4.2 FPGA

Reprogramming of the FPGA is conducted as follows:

1. Connect the USB or parallel port programmer to the JTAG port on the board, referring to figure E.2.

2. Open Lattice Diamond and load the .ldf project in `Firmware\HbarControllerFPGA_v2-1`

3. Click the Programmer button (second row, orange down arrow icon), you should be able to use the default options to load the programmer project.

4. In the new tab click the program icon (see figure E.3) to start the process.

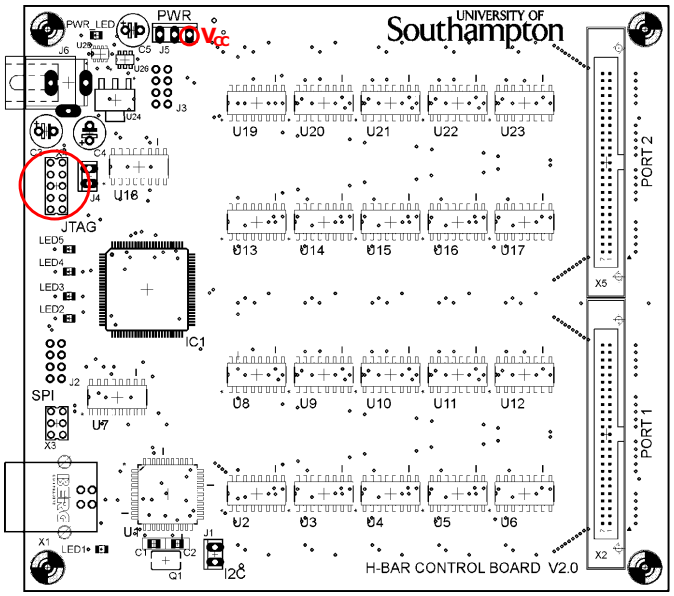


Figure E.2: JTAG header location for FPGA programming.

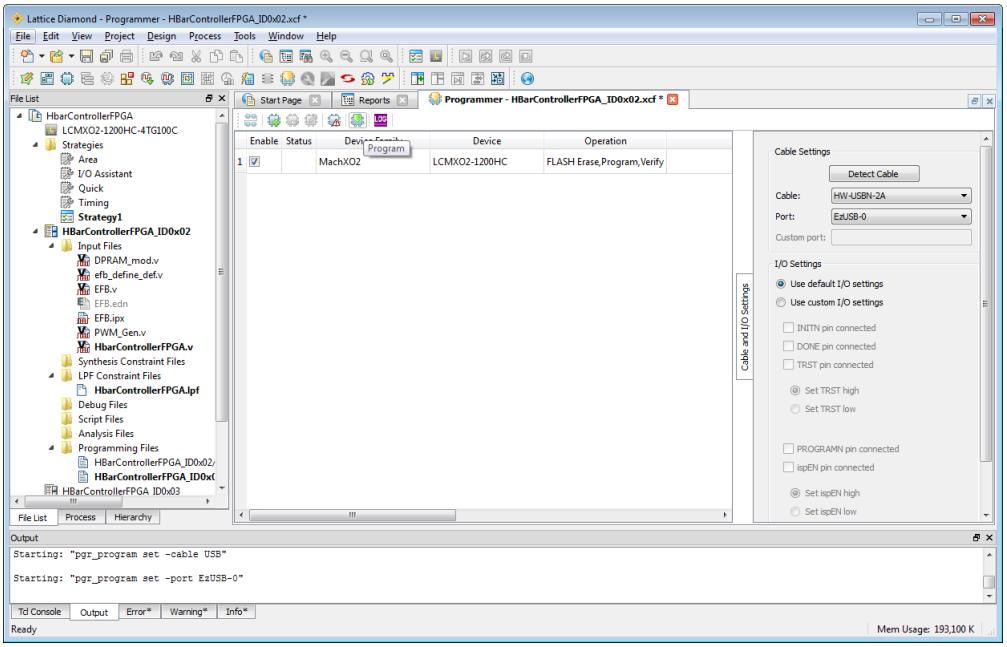


Figure E.3: Programming the FPGA in Lattice Diamond.

E.5 Bank-bypass Jumpers

The analogue switches are arranged in 8 banks that can be enabled/disabled independently via the analogue switches of U3 and U8. Jumpers J2 and J4 are provided to bypass this operation if necessary, since the additional resistance of the bank control switch is shared by all switches on the bank and thus can be a source of crosstalk.

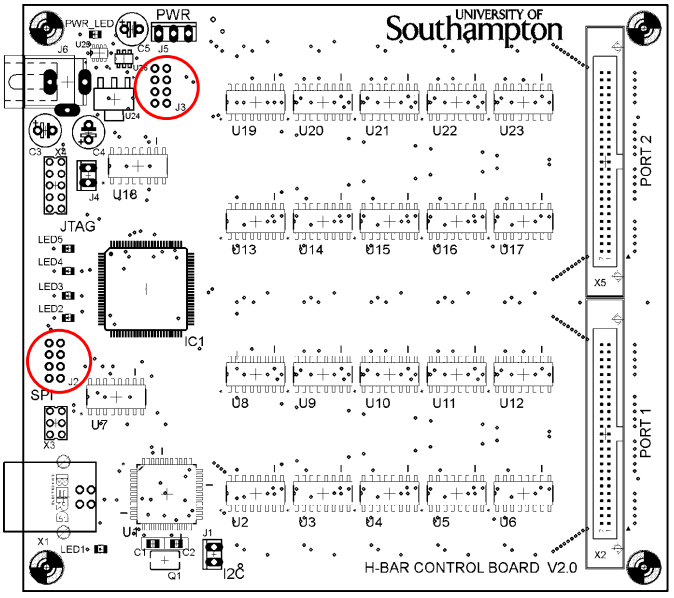
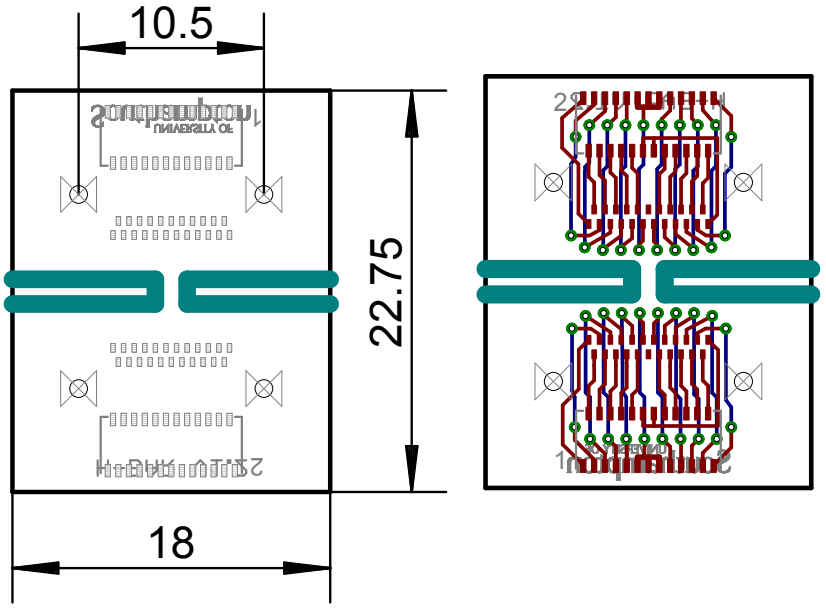


Figure E.4: Bank bypass jumper location.

E.6 H-Bar PCB



(a) (b)

Figure E.5: (a)H-Bar PCB v1.2 Dimensions (Silkscreen layers). (b) H-Bar PCB v1.2 Layout (Top copper layer red, bottom copper layer blue).

E.7 Breakout PCB

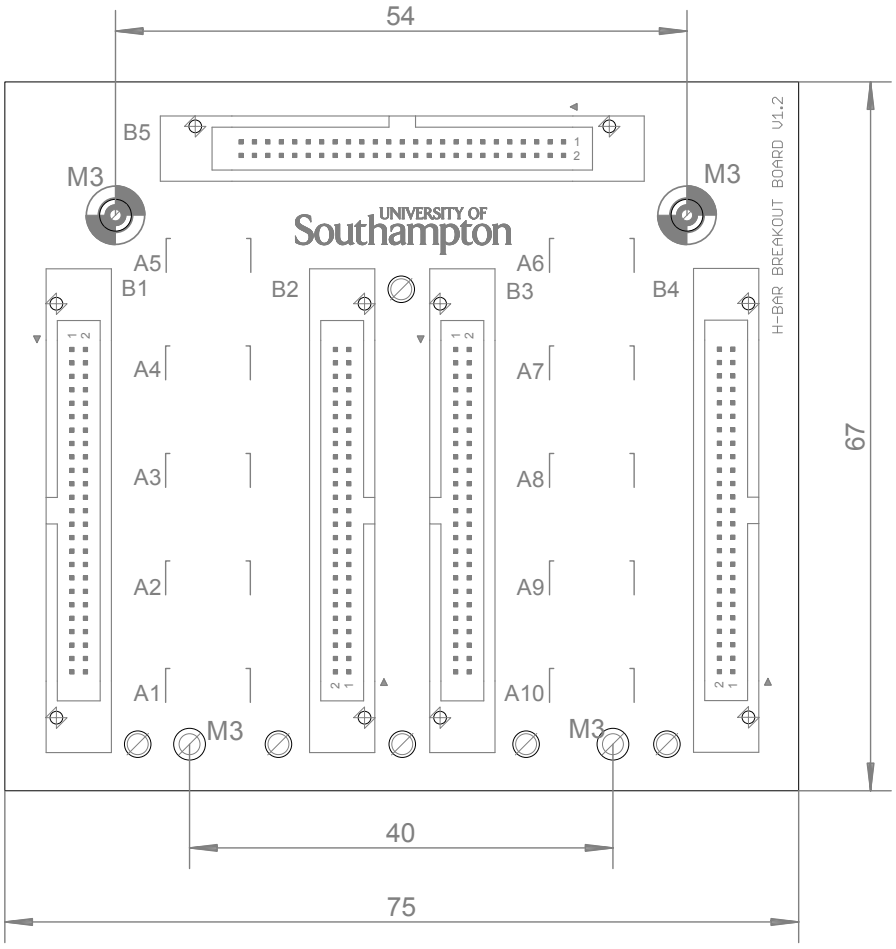


Figure E.6: Breakout PCB v1.2 Dimensions (Top silkscreen layer)

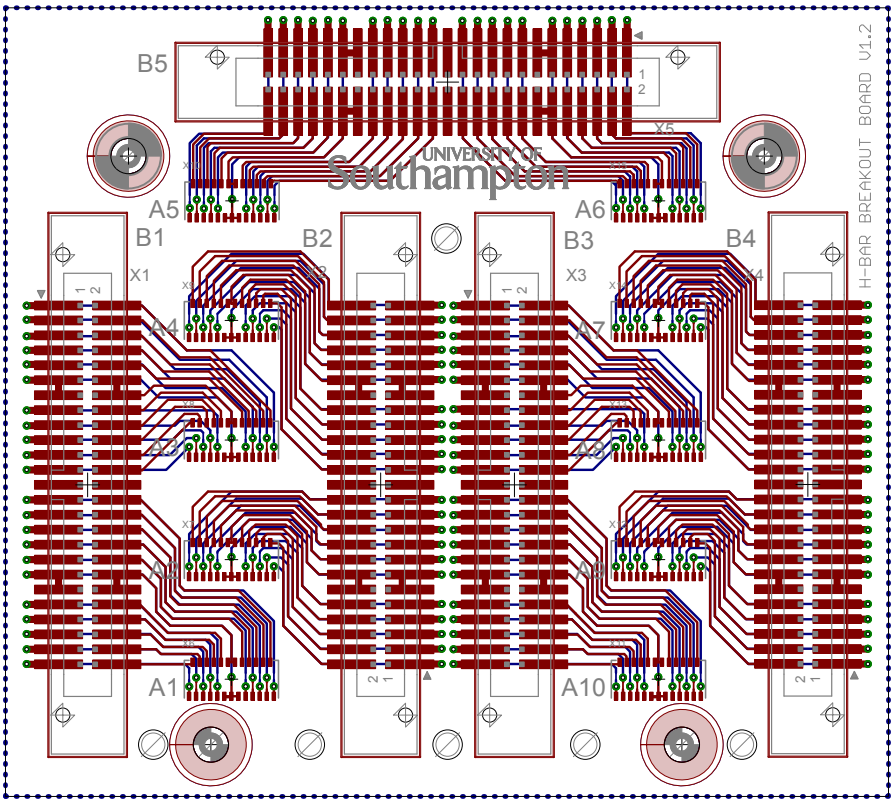


Figure E.7: Breakout PCB v1.2 Layout (Top copper layer red, bottom copper layer blue)

E.8 Controller PCB

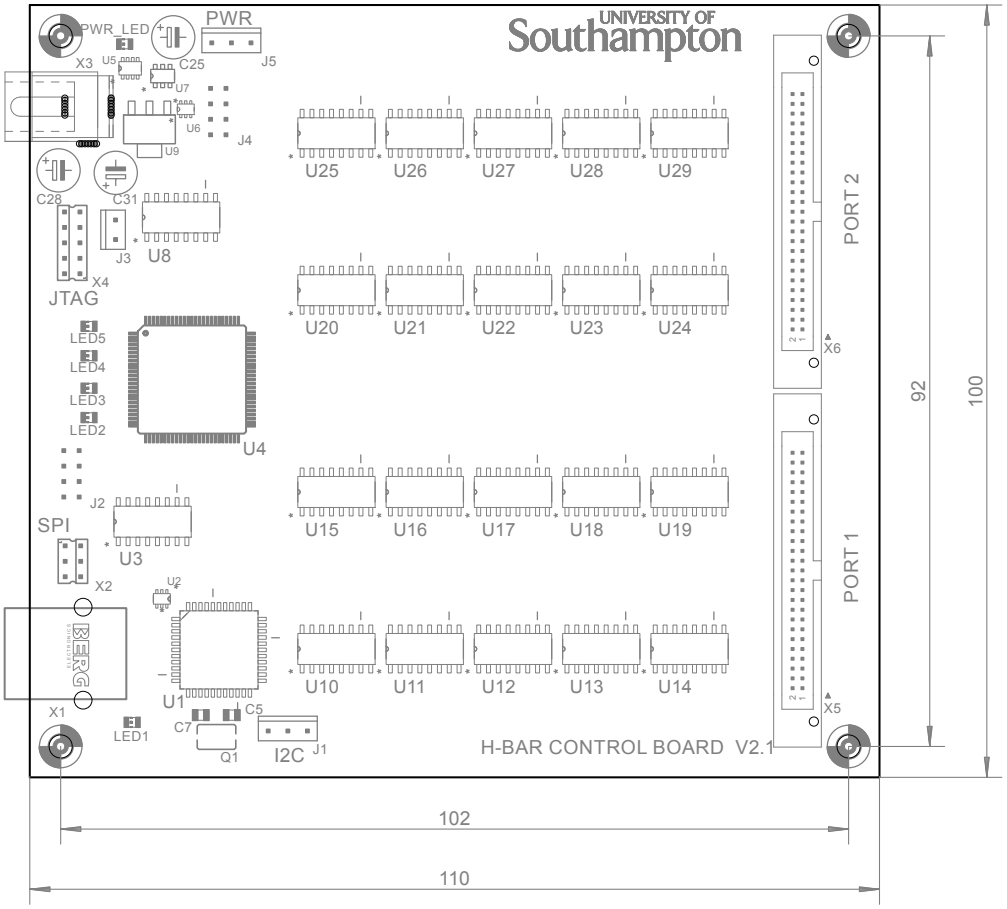


Figure E.8: Controller PCB v2.1 dimensions (Top silkscreen layer)

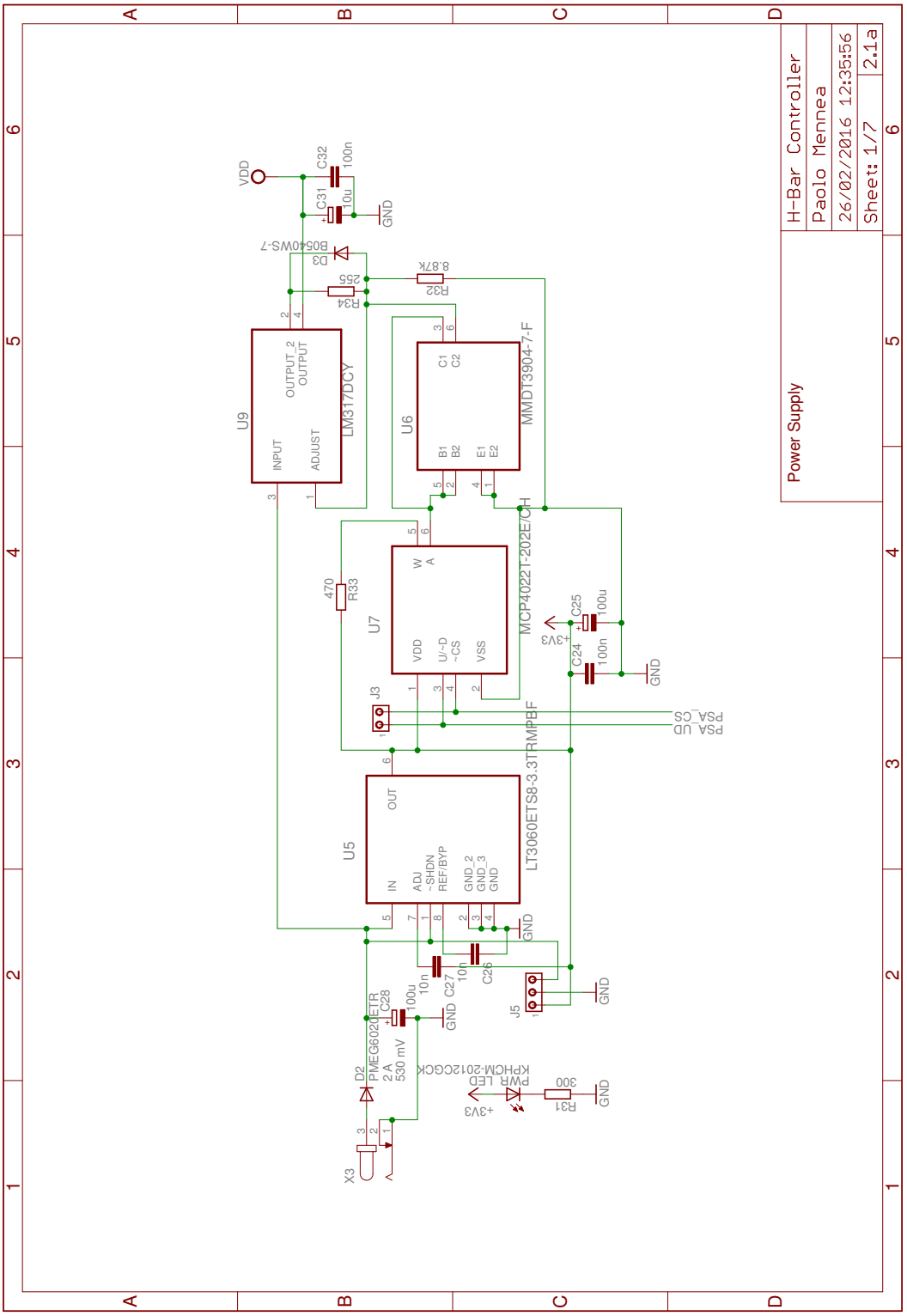


Figure E.9: Controller v2.1 schematic: Power Supply

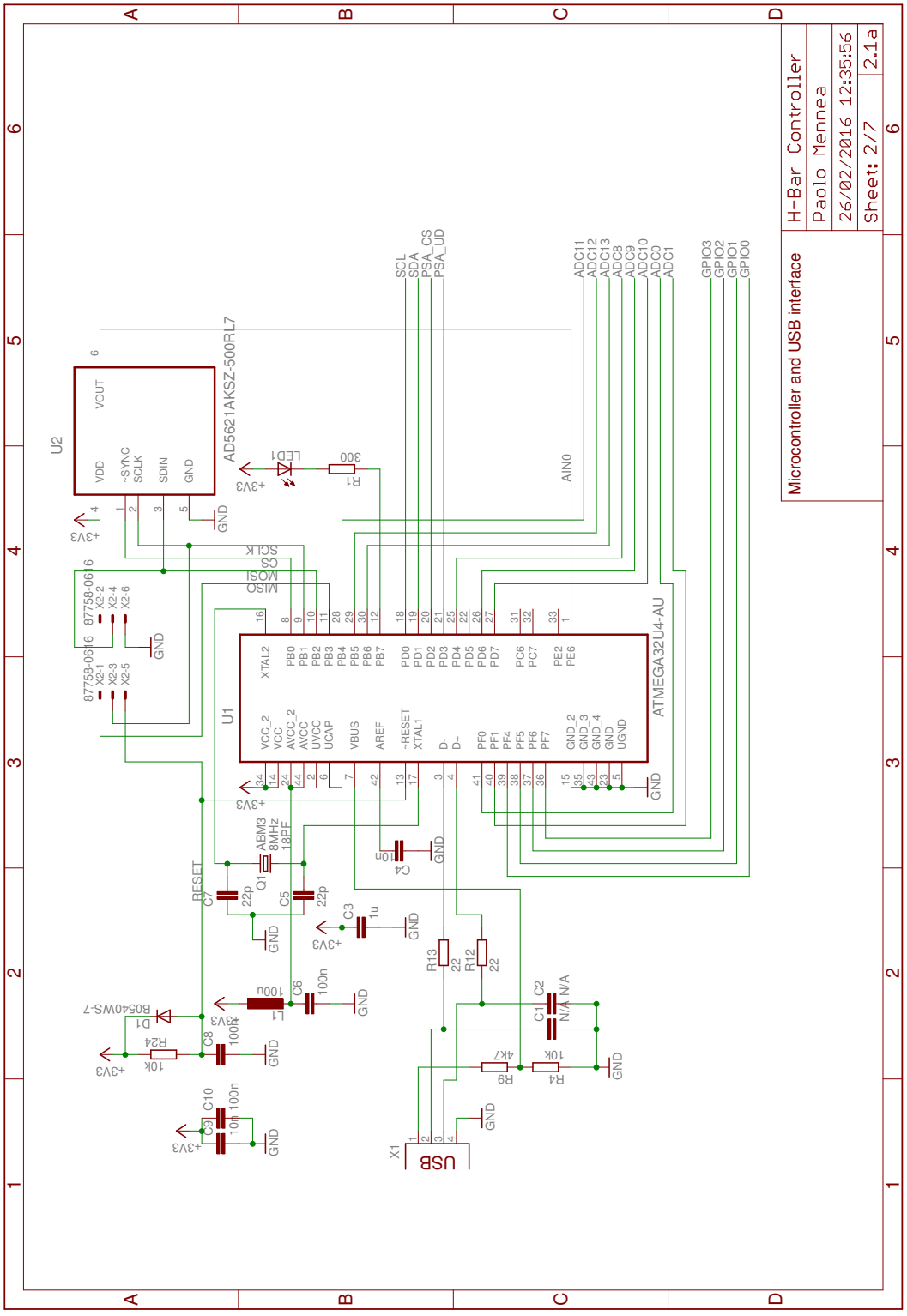


Figure E.10: Controller v2.1 schematic: Microcontroller and USB Interface

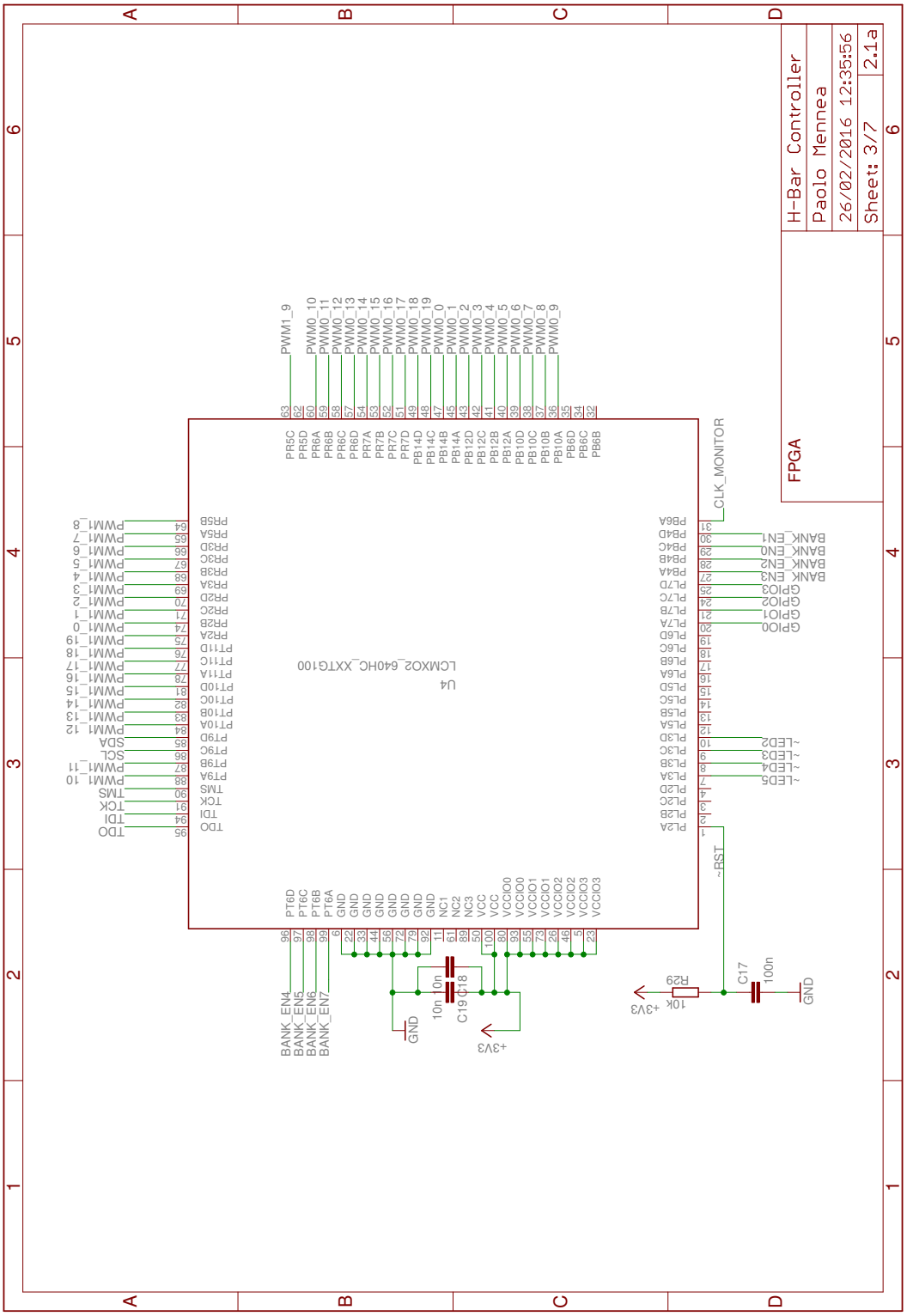


Figure E.11: Controller v2.1 schematic: FPGA

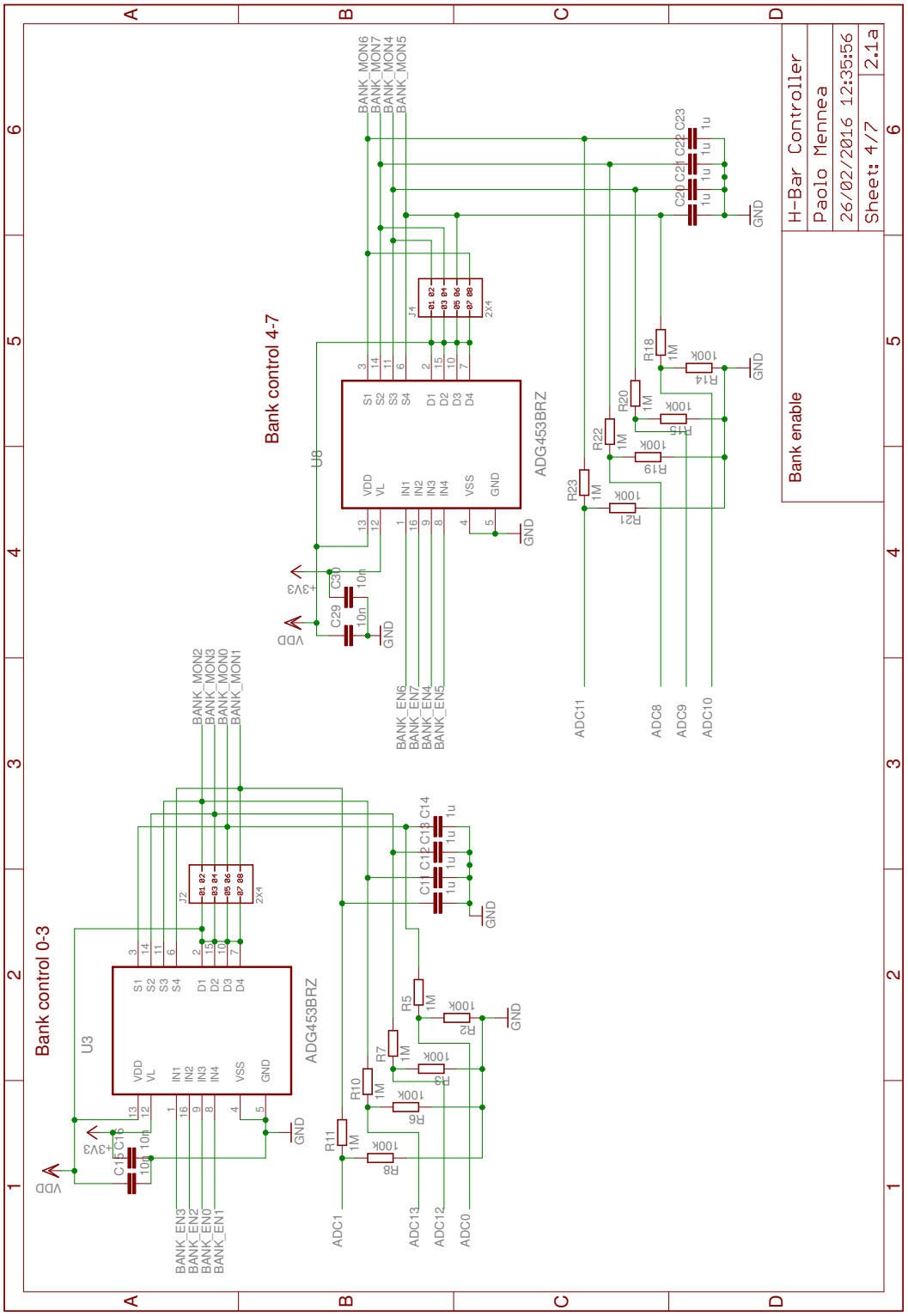


Figure E.12: Controller v2.1 schematic: Bank enable switches

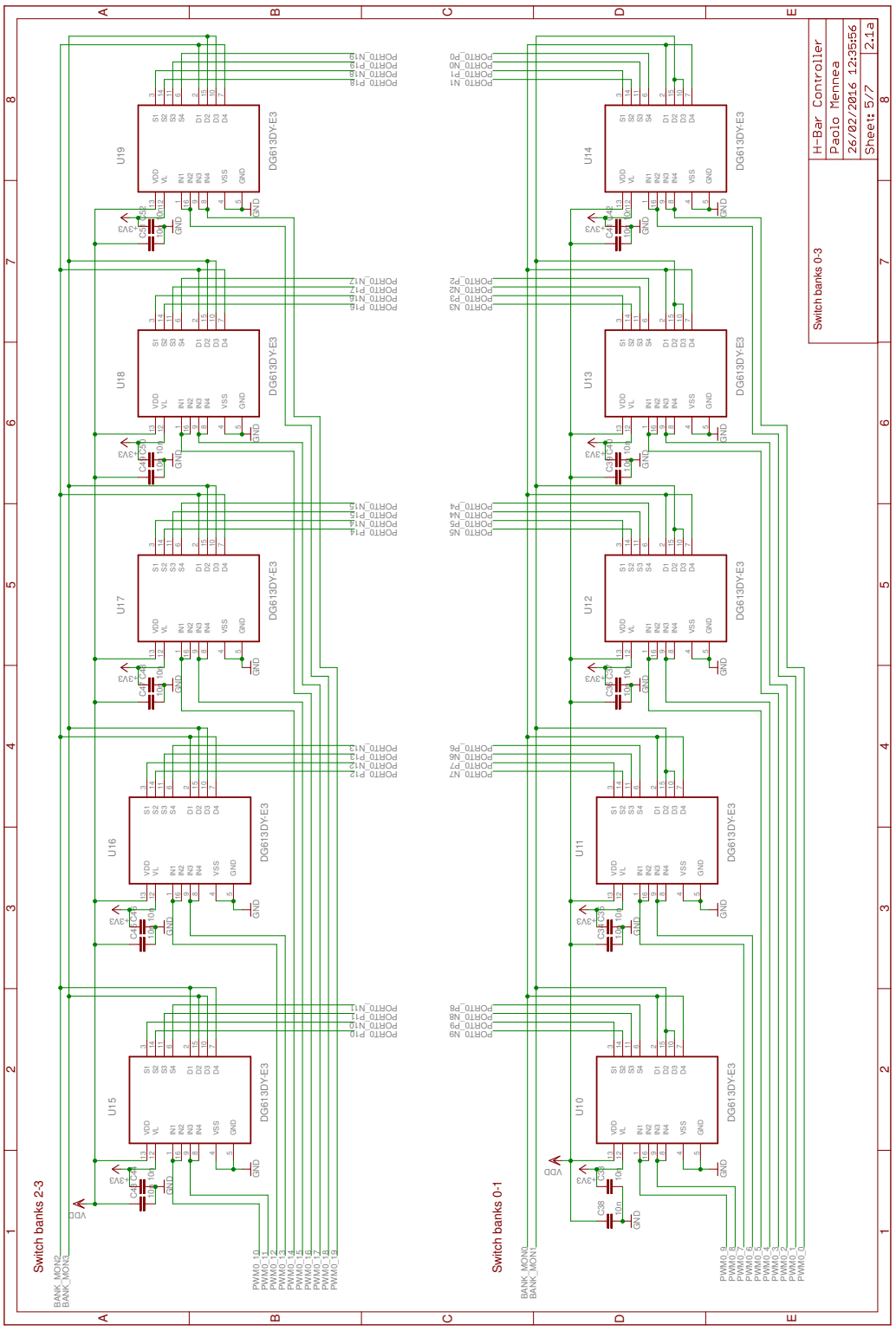


Figure E.13: Controller v2.1 schematic: Switch banks 0–3

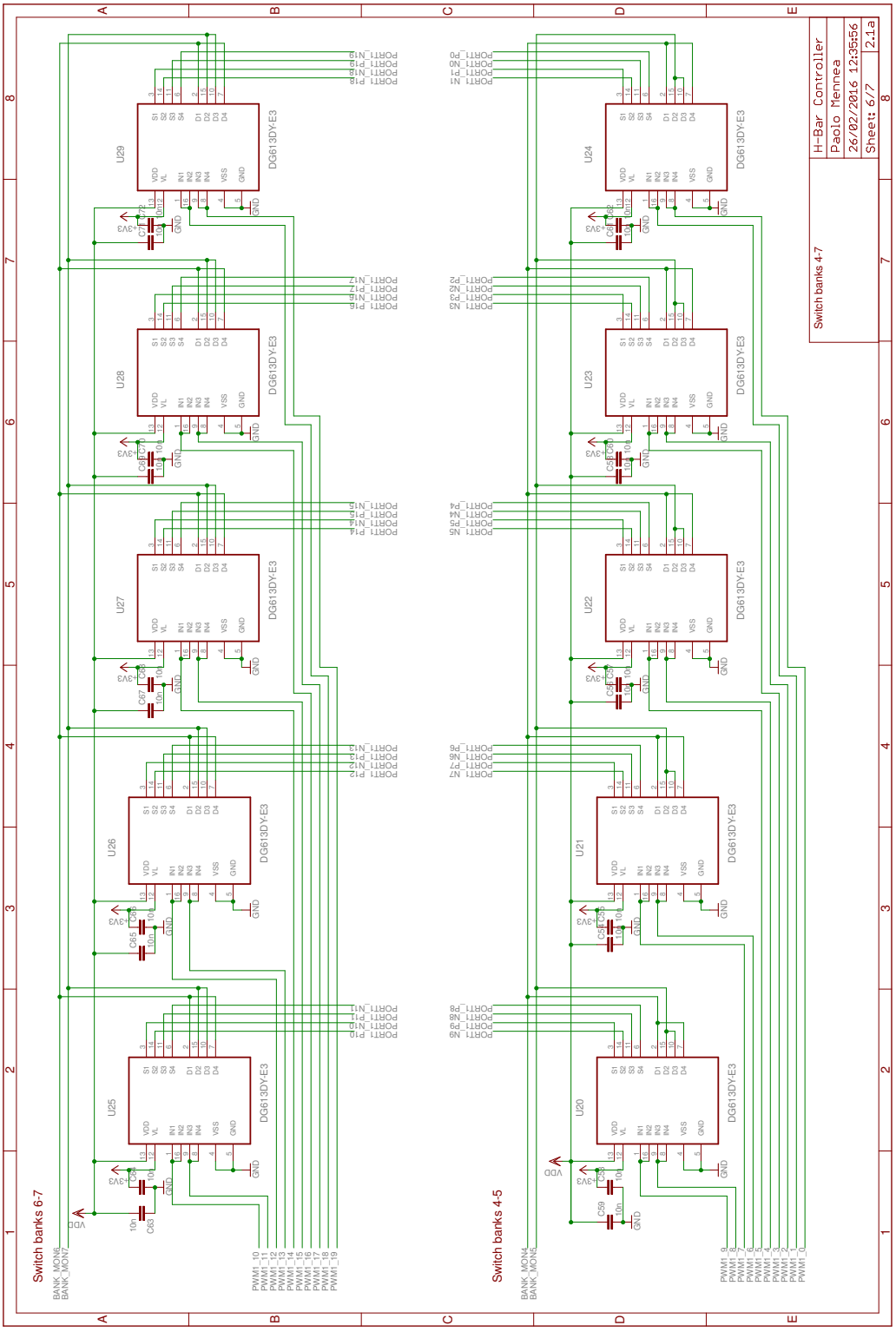


Figure E.14: Controller v2.1 schematic: Switch banks 4–7

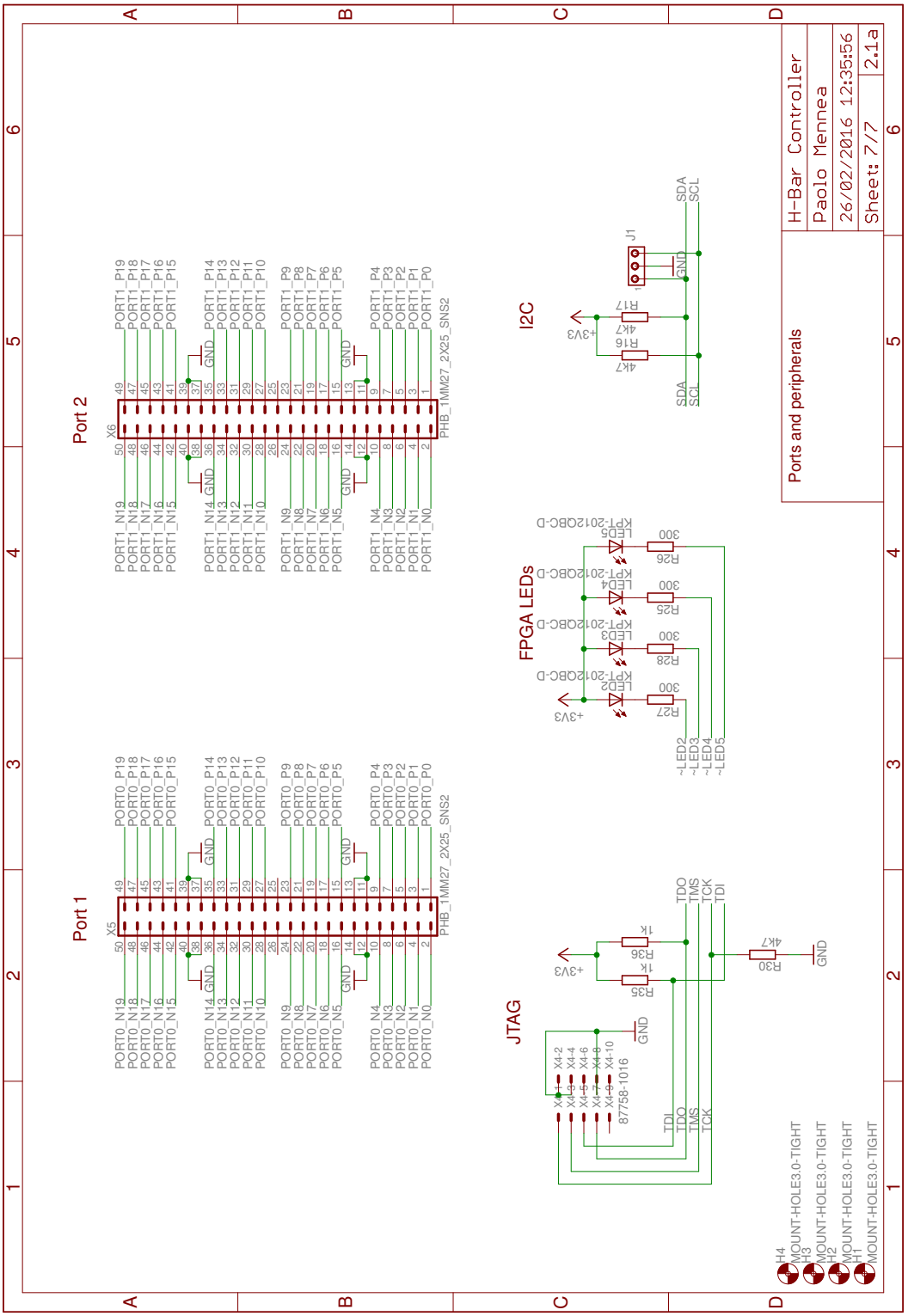


Figure E.15: Controller v2.1 schematic: Ports and peripherals