Silicon erasable waveguides and directional couplers by germanium ion implantation for configurable photonic circuits

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**Abstract:** A novel technique for realization of configurable/one-time programmable (OTP) silicon photonic circuits is presented. Once the proposed photonic circuit is programmed, its signal routing is retained without the need for additional power consumption. This technology can potentially enable a multi-purpose design of photonic chips for a range of different applications and performance requirements, as it can be programmed for each specific application after chip fabrication. Therefore, the production costs per chip can be reduced because of the increase in production volume, and rapid prototyping of new photonic circuits is enabled. Essential building blocks for the configurable circuits in the form of erasable directional couplers (DCs) were designed and fabricated, using ion implanted waveguides. We demonstrate permanent switching of optical signals between the drop port and through port of the DCs using a localized post-fabrication laser annealing process. Proof-of-principle demonstrators in the form of generic 1×4 and 2×2 programmable switching circuits were fabricated and subsequently programmed.

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1. Introduction

Silicon photonics is regarded as one of the most promising technologies to realize large-scale integration of optical circuits [1-3]. Due to its capability for high-density integration and low fabrication cost at high volume, silicon photonics is widely used as a high-speed and low-cost solution for short reach interconnects [4-6]. It is also proposed that silicon photonics can be potentially used in a much wider range of applications, such as sensing and computing [7-11].

In this paper, we demonstrate a new technology for building configurable or one-time programmable (OTP) silicon photonics circuits, in which the system architecture can be permanently programmed on demand by a post-fabrication, localised laser annealing process. This is analogous to the OTP ROM (Read-Only Memory) or OTP microcontroller chip widely used in electronic industry, where many logic blocks can be “wired” on demand into a desired configuration after device fabrication, in order to suit different applications. We have demonstrated high-efficiency erasable direction couplers (DCs) for silicon photonics circuits, and have used them to construct more sophisticated photonic switching circuits. By utilising this technology, after wafer fabrication, one single silicon photonics chip could be programmed to perform various functions.

The high cost caused by comparatively low production volume has been hindering the commercialisation and expansion of silicon photonics [12]. One major envisaged impact of our proposed technology is to standardise the photonic circuit design for a variety of applications and therefore reduce the cost per chip. One multi-purpose chip can be designed and fabricated with many functional components, and later be programmed for specific applications. Such a photonic chip can then be fabricated in a much larger volume, and the cost for each chip can therefore be reduced by a few orders of magnitude, according to the JePPIX roadmap in 2015 (http://www.jeppix.eu).

For example, there are many subcategories of data communication links in broadband optical communication networks and high-performance computing systems that impose different requirements on the silicon photonics transceivers [13] currently employed, in terms of bandwidth, link distance, power budget, cost per bit etc. In order to meet those requirements, different types of silicon photonic transceivers are available, such as 100G PSM4 (Parallel Single Mode fibre 4-lane) optical transceiver, 4×25G WDM4 (4 channels Wavelength-Division Multiplexing) transceiver, or the more advanced QAM16 (16-ary Quadrature Amplitude Modulation) [14]. Architectures of the silicon photonic transmitter chip that is required for the transceivers in each of these cases are all different. The production volume of each silicon photonic chip is therefore hindered by this market segmentation. However, with the technology demonstrated in this paper, it is now possible to make one single silicon photonic chip design in large volume, and then programme it to suit various applications.

The proposed OTP photonic circuits facilitate deployable and practical programmable circuits for the first time in a format that does not require huge amounts of electrical power to sustain them. Conventional programmable photonic circuits [15-28] are attracting a lot of interest recently for computing, microwave photonics, and quantum applications. Most previous programmable or reconfigurable photonic circuits use separate heaters to precisely control the temperature of each switching unit. Therefore, very large numbers of heaters are included in these circuits, leading to large power consumption. This may be necessary to achieve reconfigurable/full programmable photonic circuit. However, those approaches are not practical to achieve OTP photonic circuits, especially when we scale the photonic circuits up to hundreds or thousands of switching units, as most of the power will be used to maintain the operating point of each individual heater, and hence the configuration of the photonic circuits. Free-carrier dispersion effects can also be utilised to realise programmable photonic circuits, however a constant voltage supply is required for each component during operation. Comparatively, our technique involves physically changing the routing of the photonic waveguide, requiring no additional power to retain the configuration when programmed.

In this work, integrated sub-micron erasable waveguides were realized for the first time on a silicon-on-insulator (SOI) platform. The waveguides were formed by ion implantation induced damage, which can be subsequently processed with a localized laser treatment step to repair the crystalline structure. By employing such implanted waveguides, erasable directional couplers have been demonstrated with high coupling efficiency, which form the basic building block of an OTP photonic circuit. As a proof-of-principle demonstration, we successfully realised 1×4 and 2×2 OTP switching circuits on an SOI wafer.

1. Erasable waveguides and directional couplers

Directional couplers (DCs) are one of the most basic elements that can enable a configurable/OTP photonic circuit. Compared to other options for making switches, such as MZIs [29] and ring resonators [16], they can be much smaller in size, and footprint is a major consideration for measuring the cost in the semiconductor industry. Furthermore, the performance of DCs is insensitive to temperature fluctuations [30]. A typical cross section of a proposed device is shown in Fig. 1a. Implanted waveguides are successfully formed in the slab region of the conventional rib waveguide to couple light in/out, which can be erased by a laser annealing process. The laser annealing setup was the same as presented in our previous work [29].

The ion implantation induced refractive index change was previously utilised to demonstrate wafer-scale testing [31, 32] and post-fabrication trimming applications [29, 33-35]. However, for those works, the optical modes were guided in conventional etched silicon waveguides. No integrated waveguide has been demonstrated in silicon photonics, which is formed solely by an ion implantation process. The depth of the implanted waveguide is 140 nm into the silicon layer according to our calculation (Fig. 1b). Two types of DCs were designed and fabricated, as shown in Fig. 1c (single-stage DC) and Fig. 1d (two-stage DC). Optical microscope images of a typical fabricated single-stage DC and two-stage DC are shown in Fig. 1e and Fig. 1f, respectively. For the ion implantation process, we have chosen only to consider ion species that are CMOS compatible. Furthermore, light ion species, such as hydrogen and oxygen, would require very high doses to induce enough defects in order to create amorphous silicon. We also want to avoid those ion species that may induce additional free carriers after laser annealing, such as boron. Therefore, Silicon itself would be a good candidate for implantation as it causes no doping or contamination. Germanium is even better as it is also a Group IV element, but is heavier than Silicon, causing more damage per ion, and hence minimising the implantation dose. Therefore Ge ions were used for our work [29].

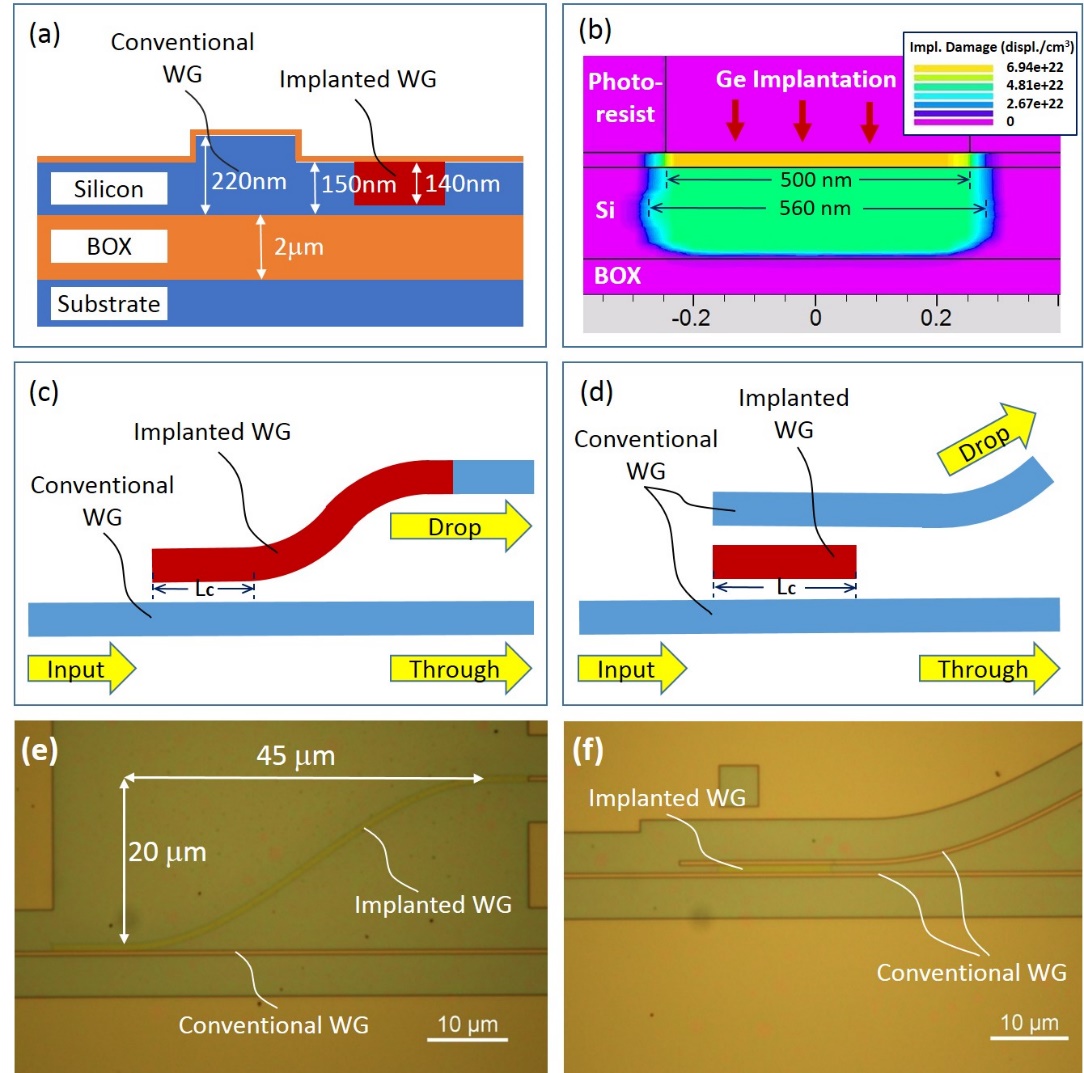


Fig. 1. Structures of the implanted waveguides (WGs) and DCs. (a) Cross sectional view of the erasable DC with a conventional rib waveguide and an ion implanted waveguide. (b) Simulation result for the Ge implanted process using the Silvaco software, the density of damage to the crystal lattice is shown in the figure. (c) Illustration of the single-stage DC. (d) Illustration of the two-stage DC. Optical microscope images of (e) a fabricated single-stage DC and (f) a two-stage DC on a SOI wafer.

A variational FDTD solver from Lumerical MODE solutions was employed to calculate the performance of the DC designs at a wavelength of 1550 nm. A 10 nm mesh size around the waveguide core was used in our calculations. The real part of the refractive index of the implanted silicon is approximately 3.96 yielding a Δn of 0.48, which is in good agreement with the expected Δn from the literature at a wavelength of 1.55 μm. The imaginary part of the refractive index of the Ge implanted Si is calculated to be 0.00085. This is calculated based on the 33 dB/mm propagation loss experimentally measured for the ion implanted waveguides. The profile of the implantation damage density in silicon is calculated by Silvaco software.

A single-stage DC consists of a 500 nm wide conventional input waveguide, a straight implanted waveguide for light coupling, an S-bend made of an implanted waveguide and a conventional output waveguide (Fig. 1c). 500 nm is a common width for conventional single-mode silicon photonic waveguides (at 1550 nm wavelength) on a 220 nm SOI platform. According to our previous measurement results, this choice of waveguide width represents a good trade-off between the single-mode condition and the propagation loss. The length of the straight implanted waveguide is defined as the coupling length Lc. The S-bend is in the shape of a sinusoidal curve of 45 m in length and 20 m in displacement as shown in Fig. 1e. Approximately 93% (-0.32 dB) coupling efficiency can be achieved according to our simulation results for a coupling length of 8 m and an ion implanted width of 540 nm, and a 200 nm wide (edge-to-edge) gap between the conventional and implanted waveguide. A two-stage DC, as shown in Fig. 1d, consists of a conventional input waveguide, a straight ion implanted waveguide for coupling the light and transferring it to another conventional waveguide coupling to the drop port. The gap between the input waveguide and the implanted waveguide is the same as the gap between the implanted waveguide and the output waveguide to the drop port. Our simulations suggest that a coupling efficiency of over 95% (-0.22 dB) is achievable for such two-stage coupling structures with a 200 nm gap, a 15 m coupling length and a width of 560 nm for the implanted waveguide. For both DCs, 200 nm is the minimum achievable trench width using our DUV lithography scanner. The implantation width was also optimized by simulations. Furthermore, DCs with various widths of the implanted waveguide were fabricated and tested, and the above mentioned designs achieved the best efficiency. The simulation result for this two-stage DC is shown in Fig. 2. The calculated effective index for the optical mode is 2.61 for the convention silicon waveguide, and is 2.79 for implanted waveguide.

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Fig. 2 (a) Calculated fundamental optical mode for the 500 nm wide silicon waveguide. (b) Calculated fundamental optical mode for the 560 nm wide germanium implanted silicon waveguide. (c) Top view of the simulation result for the optimized two-stage directional coupler.

In our simulation, we defined a step-index profile for the implanted waveguide, where the refractive index is 3.96 in the implanted region and then changed to crystal silicon (3.48 for 1550 nm wavelength) outside the implanted region. The width of the implanted region was defined by considering the region with over 80% crystal lattice displacement, which is 30 nm wider than the actual opening of the implantation mask at each edge according to our calculations, as illustrated in Fig. 1b.

All devices were fabricated on an SOI platform, with a 220 nm top silicon layer and a 2 μm thick buried oxide (BOX) layer (Fig.1a). Conventional 500 nm wide SOI rib waveguides were formed by a 70 nm partial etch (leaving a 150 nm thick silicon slab layer) to support only single-mode propagation, which is typically used for silicon photonic circuits. The conventional waveguides were fabricated by electron beam lithography and a plasma etching process. A 25 nm thick oxide layer was then deposited by Plasma-Enhanced Chemical Deposition (PECVD) as a protective layer. After this fabrication step, a 400 nm thick photoresist layer was deposited as a mask layer for Ge ion implantation. An ion energy and fluence of 130 keV and 1x1015 ions/cm2 were used, respectively. The implanted waveguides were then formed in the slab layer next to the conventional waveguide.

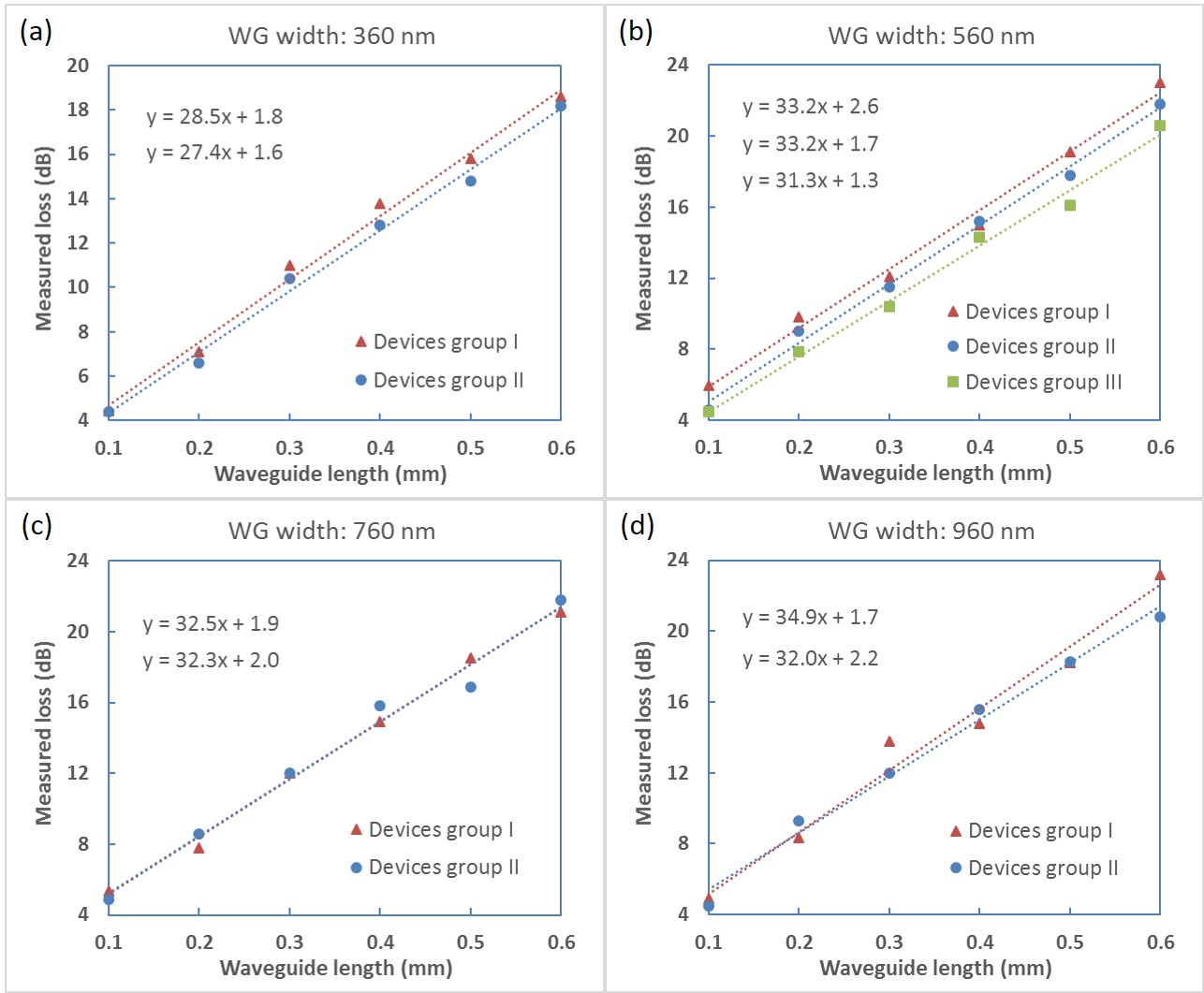


Fig. 3. Measured propagation losses of the implanted waveguides. A linear dotted line was fitted to each device group measured. Each device group includes waveguides from the same silicon chip. The corresponding function equations are shown in the figure. The width of the implanted waveguides are: (a) 360 nm, (b) 560 nm, (c) 760 nm, and (d) 960 nm.

The propagation loss of germanium ion implanted waveguides with various widths were first characterised using the cut-back method. For each width, implanted waveguides with different lengths were fabricated and characterised. Grating couplers and conventional waveguides were employed as optical input/output, which were butt-coupled (direct end-to-end connection) with the implanted waveguides. Experimental results are shown in Fig. 3. A linear dotted line was fitted to each device group measured, and the function equations shown in the figure in the corresponding order. According to our measured results, the average propagation loss of the implanted waveguides are 28 dB/mm, 32.6 dB/mm, 32.4 dB/mm and 33.5 dB/mm for the 360 nm, 560 nm, 760 nm and 960 nm widths, respectively. This loss is very high compared to conventional waveguides. However, only a short section of implanted waveguide (~10 m) is needed for each switching device, corresponding to a total propagation loss of only 0.3 dB. The loss may be further reduced by optimising the implantation dose or device design. The average transition loss between conventional and implanted waveguides is approximately 0.9 dB. We believe that this loss is mainly caused by absorption within the implanted silicon. The loss is therefore lower for narrower waveguides as more optical power will propagate in the low-loss crystal silicon slab surrounding the implanted waveguide. The propagation loss increases with waveguide width as more light will be guided in the waveguide core of the implanted silicon.

For all measurements, the optical transmissions were normalised to the fibre-to-fibre optical loss of a reference waveguide in each case, which consists of only the grating coupler at the input and output, and a conventional waveguide with the same length as that was used for coupling light to the implanted waveguides or the photonics devices. For the fabricated devices, each grating coupler has an insertion loss of approximately 4 dB, and the propagation loss of the conventional waveguide is approximately 3 dB/cm. Only the fundamental TE mode is coupled to the waveguides. When characterizing the single-stage DCs, the additional propagation loss in the S-bend and the transition loss to conventional waveguide were deducted.

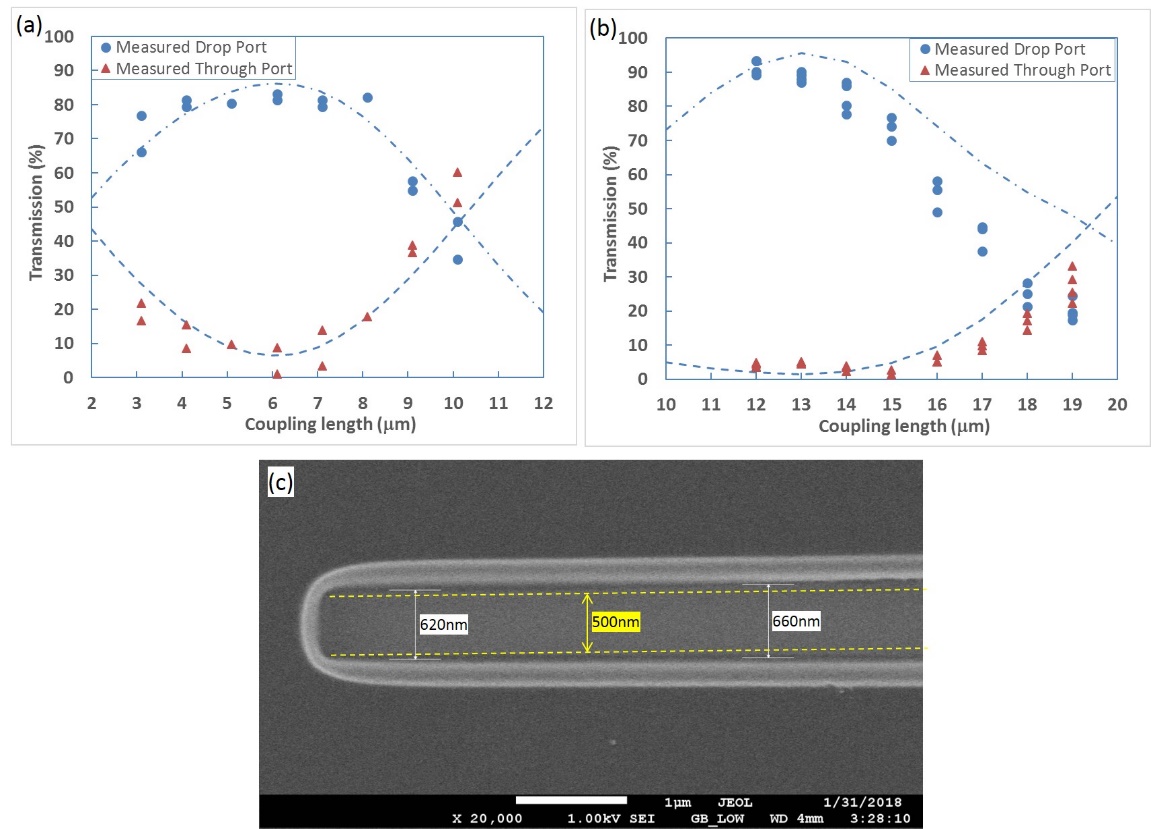
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Fig. 4. Measured optical transmission of the: (a) single-stage DCs with various coupling lengths, and (b) two-stage DCs with various coupling lengths. Simulated results (dotted line), with a step-index profile assumed for the implanted waveguides, are plotted as a reference. (c) SEM image of a typical opening in the implantation mask after Ge ion implantation. The original designed width of the opening is 500nm (marked in yellow). However, the width was increased to around 620 - 660 nm after ion implantation.

The measured results of single-stage DCs and two-stage DCs are plotted in Fig. 4a and Fig. 4b, respectively. Over 80% coupling efficiency was experimentally obtained for a coupling length of around 6 m for the single-stage DCs. Calculated results are plotted as a reference. Over 90% coupling efficiency was obtained for coupling lengths around 12 m for the two-stage DCs. It worth noting that in the case of a single-stage DC, the power coming out from the drop and through port will ideally sum up to about 100% of the input optical power, in the absence of any waveguide propagation loss. However, it is not the same case for a two-stage DC. As shown in Fig. 4b and the calculated optical field pattern in Fig. 2c, during the coupling process from the bottom input waveguide to the upper output waveguide, light needs to pass through the ion implanted waveguide in the middle. In this ion implanted waveguide, if there is any part of optical power left when reaching the end of the waveguide, this part of optical power will be eventually scattered leading to additional optical loss.

Compared to our initial simulation results, we found that the measured coupling lengths were shorter for both types of DCs. Such reduction of the coupling length is most likely caused by an increased overlap of the optical mode in the two coupled waveguides, which means that the actual optical mode in the implanted waveguide is wider than the optical mode used in our simulations. We noticed through SEM measurements that the E-beam resist, which was used as the implantation mask, shrank during the implantation process as shown in Fig. 4c. A 500 nm wide opening developed for Ge implantation was increased to around 620 nm - 660 nm in width after implantation according to our measurement. This will lead to a wider implanted waveguide with a graded index profile, and therefore a reduced coupling length as we measured. Our simulation results were adjusted accordingly, and plotted in Fig. 4a and 4b. For example, we increased the width of the step-index implanted waveguide from 540 nm to 680 nm (70 nm added each side) for the single-stage DCs, and slightly reduced the refractive index of waveguide core from 3.96 to 3.92, in order to approximate the graded-index profile actually created by the Ge implantation because of the shrinking mask. The shrinkage of the resist layer could be caused by the heat induced by the ion implantation process. Replacing the resist-based implantation mask with a hard mask would eliminate this uncertainty in the fabrication process.

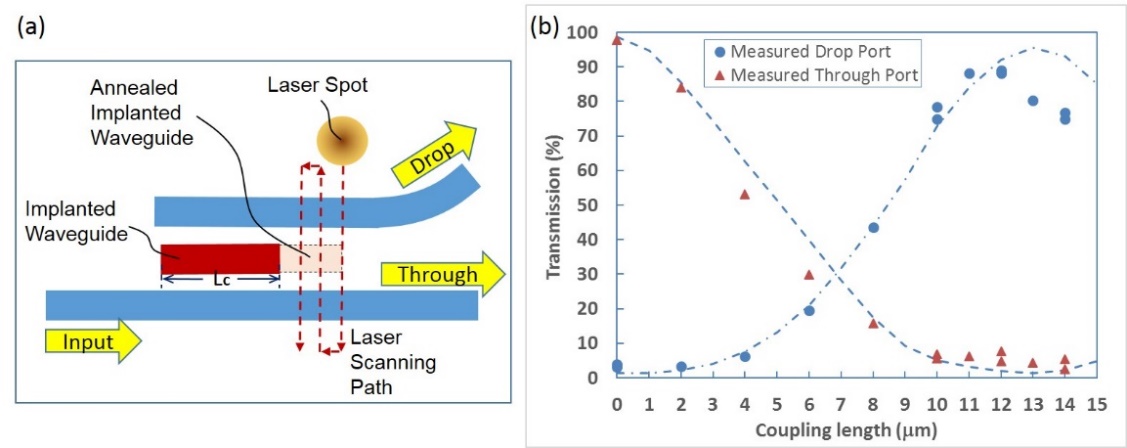
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Fig. 5. (a) Illustration of the laser annealing process for the two-stage DCs. (b) Measured results for the two-stage DCs with various coupling lengths after laser annealing. The original coupling length for the directional couplers used for this test are 20 m. Simulation results (dotted line) were plotted as a reference.

An OTP optical switch was demonstrated by localized laser annealing of a two-stage DC, which is the most basic component for photonic programmable circuits. An illustration of the localized laser annealing process is shown in Fig. 5a. The implanted waveguide was annealed by a focused laser spot in a step by step fashion, in order to maximize the coupling efficiency to the drop port with an optimum coupling length Lc. The raster scan step of the laser was 1 µm, to ensure uniform coverage of the area. Light propagating through the device will be mostly guided to the through port when the implanted waveguide is annealed completely (Lc = 0). After annealing, the implanted silicon was almost completely recrystallized, which was confirmed by Raman spectroscopy measurements. We estimate the residual index differences (both the real and imaginary parts) between crystalline silicon and the implanted silicon after recrystallization are negligible, as the peak germanium concentration in the silicon is less than 0.3% after implantation according to our simulations. We did not detect any difference in performance between the annealed silicon and the original crystal silicon during our experimental characterization of the photonic devices.

A continuous wave (CW) Argon ion laser was used for the annealing process. The laser output signal is a mix of all lasing lines in the argon ion spectrum, dominated by 488 nm and 514.5 nm in almost equal parts. CW laser-based annealing has been shown to produce larger silicon crystal grain sizes with fewer defects than those obtained by pulsed laser source systems, resulting in a qualitative improvement in the crystallization of the amorphous silicon for enhanced material quality [36, 37]. This has been attributed to the lower cooling rate after laser irradiation from continuous wave sources. The laser beam was guided to the surface of the silicon chip in a controlled and precise manner. A half wave plate and a polarization beam cube splitter were used to adjust the laser power. The laser beam was focused onto the chip surface using a 20× microscope objective lens, which produced a spot size of approximately 2 µm in diameter. The launched laser power was 45 mW for annealing experiments. The sample was scanned under the laser beam using a set of linear micro-precision stages whilst a pellicle beam splitter and a CCD camera were used for imaging and control. The laser scanning speed was 10 m/s. The laser spot was aligned by visual referencing to an alignment mark. Such a visual system can typically achieve an accuracy of 0.5 µm [29]. More importantly, the accuracy of the step movement of the laser spot can be as good as 0.1 µm (such as the stepper motor NRT100/M from Thorlabs).

The experimental results of the laser annealing test for the two-stage DCs are plotted in Fig. 5b. For all the DCs measured in this experiment, the original coupling lengths (before annealing) were 20 µm. Several devices were characterised with various lengths of the implanted waveguide left unannealed (coupling length Lc). The measured results are in good agreement with our simulation results. A coupling efficiency of 89% (-0.5 dB) is achieved with a coupling length of approximately 11 or 12 µm, with an average residual transmission of 5% (-13 dB) to the through port. When the implanted waveguide is fully annealed, there is approximately 3% (-15 dB) cross coupling to the drop port, with 97% (-0.13 dB) transmission in the through port. For the above mentioned DCs, we only experimentally demonstrated one-time on-off switching, which is targeted for OTP burn-in photonic device. However, it is possible to switch the device on and off a few more times with a longer implanted waveguide section (and hence multiple coupling lengths), which will meanwhile induce a slightly higher insertion loss.

1. Demonstration of OTP photonics circuits

Based on the permanent programming of the optical coupling described previously, we have demonstrated 1×4 and 2×2 OTP switching circuits as proof-of-principle demonstrations of the OTP photonic circuit implemented with our proposed technology. The microscopic images of the switching circuits are shown in Fig. 6a and 6b.

The 1×4 switching circuit comprises three two-stage DCs in series. The drop ports of those DCs lead to outputs P1, P2, and P3, respectively. The through port leads to output P4. After device fabrication, the optical signal can be permanently programmed to output at any of the four output ports, depending on the specific requirements arising from the application. For the fabricated device, the coupling length was designed to be 13 µm for all of the DCs. This coupling length is not yet optimised to the best efficiency to the drop port. Therefore, we need to anneal the coupling length to 11.5 µm to maximize the coupling efficiency, as suggested by the previous results (Fig. 5b). This optimal coupling length can be directly fabricated in the future, then the initial annealing step can be avoided.

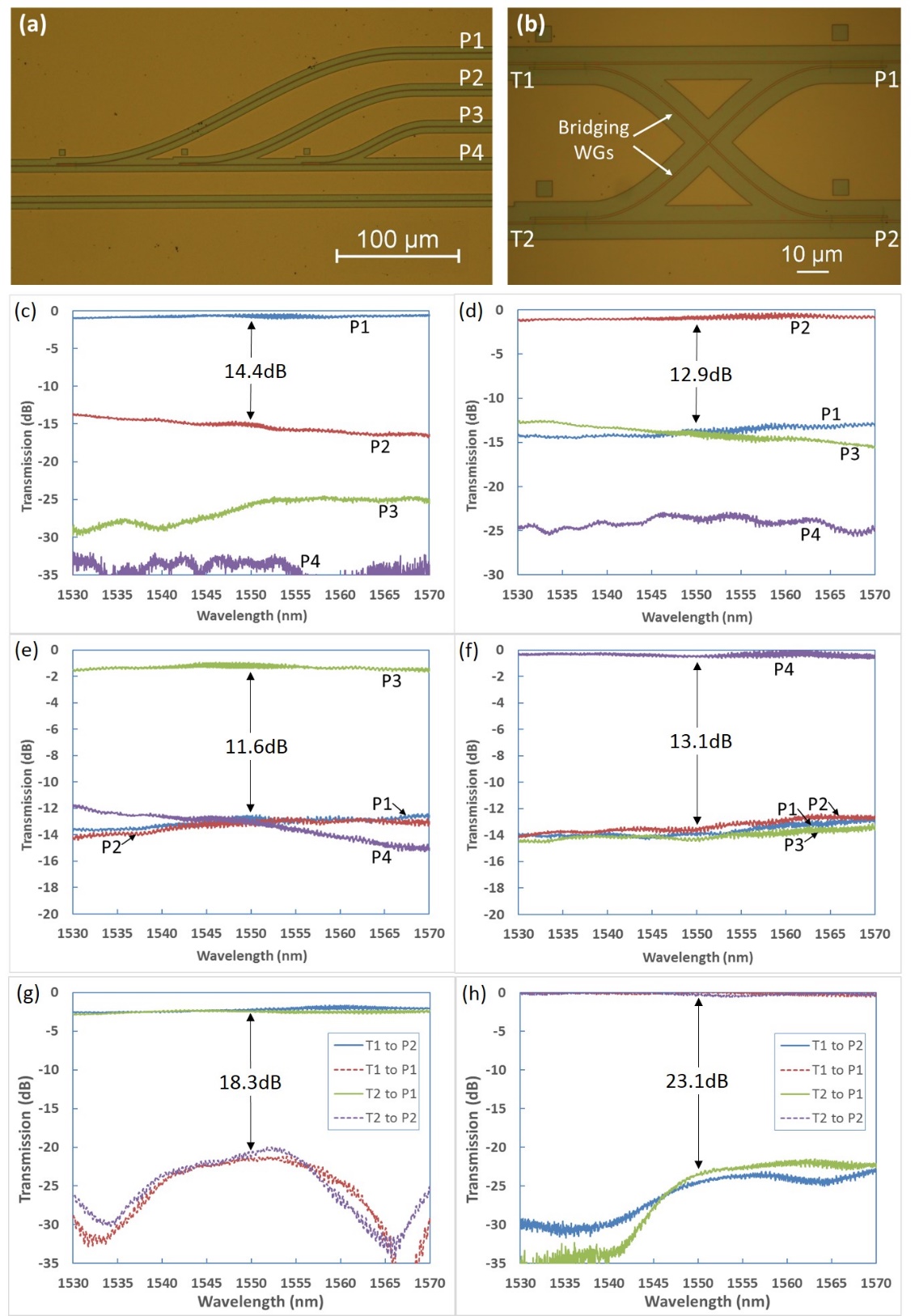


Fig. 6. (a) Optical microscope images of a 1×4 programmable photonic switching circuit and (b) a 2×2 photonic switching circuit. Measurement results for the photonic switching circuits. The 1×4 photonic switching circuit was programmed by laser annealing to produce an output at one of the four ports sequentially (c, d, e and f). (c) Measured results when P1 is set to be the output port. (d) Measured results when P2 is set to be the output port. (e) Measured results when P3 is set to be the output port. (f) Measured results when P4 is set to be the output port. The 2×2 switching circuit was programmed to operate in two modes by laser annealing: (g) cross-coupling modes or, (h) through-coupling mode.

The algorithm for programming the output to port P1 is simply trimming the first DC to its maximum coupling efficiency to the drop port. The measured results for all the four output ports are shown in Fig. 6c. The transmission is about -0.5 dB for P1, which matches well with our previous results for the discrete two-stage DC devices. The crosstalk to P2 is -14.4 dB at 1550 nm wavelength, as plotted in the figure. For programming the output to port P2, we annealed the whole implanted waveguide for the first DC, and then annealed the coupling length to 11.5 µm for the second DC to optimise its coupling efficiency to P2. As shown in Fig. 6d, the transmission to P2 is approximately -0.8 dB, which includes a 0.13 dB residual coupling loss at the first DC and a 0.5 dB loss while coupling to the drop port at the second DC. There is a 0.17 dB discrepancy between the expected loss values and the measured result at 1550 nm, which could be attributed to the measurement uncertainty and the imperfections associated with the fabrication process. Similarly, we can programme the output to port P3 and P4 by optimizing the coupling efficiency of the third DC, or anneal all the three DCs by laser annealing, respectively. The measured results in these cases are plotted in Fig. 6e and Fig. 6f.

The 2×2 OTP switching circuit is comprised of a 2×2 array of two-stage DCs arranged in a pattern as shown in Fig. 6b to enable cross coupling between two signal paths. There are two signal inputs T1, T2 and two outputs P1, P2. Although a simple 2×2 switch can be made using the two outputs and inputs of a single DC, our design with the 2×2 array of DCs can offer a much lower crosstalk [38] and more functionality. After device fabrication, the optical signal can be permanently programmed into two operating modes: a cross-coupling mode and a through-coupling mode, depending on the requirements arising from the applications.

When all the DCs are operating at the optimum coupling point to the drop port (with Lc = 11. 5 µm), the 2×2 switching circuit is operating in cross-coupling mode. The optical signal inserted in T1 will be coupled to a bridging waveguide (conventional shallow-etched waveguide) at the first DC, and then coupled over to P2 at the next DC. Similarly, the optical signal inserted in T2 will be coupled to P1. The measured results are shown in Fig. 6g. The transmission losses of T1-P2 and T2-P1 channel are about 2.3 dB on average, which includes approximately 0.5 dB insertion loss at each two-stage DCs in addition to the insertion loss of the waveguide cross in the middle of the bridging waveguide. The loss of the waveguide cross was characterised to be 0.6 dB with separate testing structures. However, this loss figure can be potentially improved to 0.16 dB with a better design [39-41][14]. There is -20.6 dB crosstalk at 1550 nm according to the measurement results for both transmission channels, corresponding to an -18.3 dB crosstalk (Fig. 6g).

When all the implanted waveguides of the two-stage DCs are annealed by the laser, the 2×2 switching circuit is working in a through-coupling mode, when the light signals can go straight through the two DCs at each side from T1 to P1, or from T2 to P2. The measured results are shown in Fig. 6h. The transmission of both channels (T1-P1 and T2-P2) is around -0.2 dB on average, which is also expected due to the insertion loss of the two fully annealed DCs. The crosstalk in this through-coupling mode is approximately -23.1 dB.

1. Discussion and conclusion

More generic photonic programmable circuits can also be built based on more advanced algorithms [20-23]. For most applications, energy consumption is one of the key metrics for photonic devices. Previously demonstrated integrated linear photonic circuits require constant power to maintain each switching component, and the power consumption will grow exponentially with the number of inputs and outputs the linear circuit has. Comparatively, the technology proposed here requires no additional power after it has been programmed into the target configuration, making it a potentially key technology that enables low cost and low power consumption silicon photonic devices.

In order to successfully implement the proposed technology, additional processing steps (ion implantation and laser annealing) are required, which add to process complexity. Ion implantation is a CMOS compatible process which is widely available in semiconductor fabrication facilities, and modification for Germanium implantation is feasible, but not yet commonplace. The additional costs associated with this implantation process, once implemented for Germanium, are not significant, compared with the tens of fabrication steps usually required for separate production process of a series of different silicon photonics chips, each for a different application. The laser annealing process can be implemented at both wafer and chip scale using a machine similar to the those widely used for automated testing of photonic devices and circuits, in research laboratories and commercial foundries. By employing a 3-axis positioning stage, it is possible to accurately position optical probe and fibre arrays to specific locations of the chip. Therefore, it is possible to deliver the annealing laser power with a standard optical fibre and illuminate the top silicon surface. Our annealing system can achieve an accuracy of about 0.5 m [29] for positioning the laser spot. Should higher accuracy is required, an active feed-back system can be implemented [35] to control the laser spot movement. Furthermore, it is also possible to use an electrical heater to realise localised electrical annealing [42] instead of the laser. Hence, the additional cost to implement our proposed technology can be minimized.

In summary, the essential building blocks, in the form of a single-stage and two-stage DCs, were designed and fabricated for configurable/OTP silicon photonic circuits. By using waveguides formed by ion implantation induced damage, the output light can be switched permanently between the drop port and through port by a localised laser annealing process. Approximately 89% (-0.5 dB) and 97% (-0.13 dB) coupling efficiency was experimentally demonstrated while coupling to the drop port and through port, respectively, for a two-stage DC. Further reduction of the transmission loss of the DCs is possible if we can reduce the coupling length and implantation dose, in order to reduce the optical absorption due to the defect states, whilst keeping the high coupling efficiency. 1×4 and 2×2 OTP switching circuits were fabricated and characterized as proof-of-principle demonstrations. The circuits have been successfully programed using laser annealing to operate in all the possible configurations. It is possible to achieve a transmission of better than -1 dB for all the channels with an improved waveguide propagation and crossing loss.

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Disclosure

The authors declare that there are no conflicts of interest related to this article.

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