The influence of substrate on SOI photonic crystal thermo-optic devices

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Abstract: We investigate the influence of the substrate on a photonic crystal thermo-optic device on a silicon-on-insulator (SOI) platform. The substrate-induced thermo-optic tuning is obtained as a function of key physical parameters, based on a semi-analytic theory that agrees well with numeric simulations. It is shown that for some devices, the substrate's contribution to the thermo-optic tuning can exceed 10% for a heater located in the waveguide core and much higher for some other configurations. The slow response of the substrate may also significantly slow down the overall response time of the device. Strategies of minimizing the substrate's influence are discussed.

OCIS codes: (130.5296) Photonic crystal waveguides; (120.6810) Thermal effects; (130.4815) Optical switching devices; (350.4238) Nanophotonics and photonic crystals.

References and links

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1. Introduction

Silicon is an attractive material for making photonic integrated circuits due to its excellent compatibility with the well-developed CMOS technology [1,2]. The SOI platform provides additional benefits for the integration of photonic devices, such as low optical loss, low power consumption, high stability, and high speed [3]. Key components of silicon photonic circuits include optical switches, delay lines, and modulators. The thermo-optic (TO) effect is an attractive option to implement optical switches and tunable delay lines if high speed is not a requirement, because it avoids free carrier absorption of light that is present in the electro-optic devices. Furthermore, understanding of the TO effect also helps in the design of silicon electro-optic modulators because the current flow associated with carrier movement is usually accompanied by heat generation [4]. The incorporation of photonic crystal (PC) structures in these devices results in significant reduction of the interaction length due to the slow light effect [4–12]. Ultra-compact optical switches and modulators utilizing different PC structures have been widely studied recently.

A thermo-optic PC device is based on the principle that the temperature variation in the structure induces a change of its refractive index, which in turn leads to a phase shift and a time delay for an optical signal. In an SOI PC structure, the total temperature rise (and thus the total phase shift or time delay) comprises contributions from the temperature rise across the oxide layer as well as that in the substrate. In prior simulations and theoretical studies, the substrate effect is usually assumed to be small and only a relatively thin substrate layer (e.g. <20μm) is included in simulations [8]. The effect of a full substrate (e.g. ~500μm in actual SOI wafers) has not been studied. In this work, we investigate the influence of the substrate as a function of a number of key physical parameters such as the heater length, the substrate thickness (t_{sub}) and the thickness of the buried oxide layer (t_{ox}). Our results reveal some important aspects/scenarios in which the influence of the substrate can be surprisingly high and cannot be neglected in device design. As numerical simulation of a full substrate can be extremely time-consuming, we have developed a semi-analytic theory that can be used for quick assessment of the substrate effect in thermo-optic device design. Guided by this theory, strategies of minimizing the influence of the substrate will be discussed.

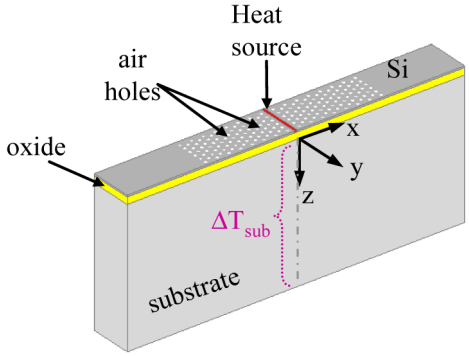

Fig. 1. Schematic configuration of an active Si photonic crystal waveguide structure on SOI (not drawn to scale).

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2. Substrate temperature profile

Figure 1 shows the schematic of an active PC structure on an SOI wafer with a heat source of width W and length L embedded in the core of the photonic crystal waveguide (PCW). The heat source can be constructed from a lightly doped (e.g. ~10^{14}cm^{-3}) Si strip surrounded by relatively highly doped (e.g. ~10^{17}cm^{-3}) silicon on both sides [5,12]. Concentrated ohmic heating can be produced in the center strip by passing current laterally through this structure. The top PCW layer can be modeled by an equivalent hole-free homogeneous slab with an effective thermal conductivity κ_{eff}, which is determined by the PCW structure [12]. This method helps to significantly mitigate the simulation difficulties for such a multi-scale structure and makes it possible (albeit still very time-consuming) to simulate a structure with a full substrate thickness of 500μm. A typical 3-D steady state FEM simulation result is shown in the inset of Fig. 2(a). The bottom surface of the chip is kept at T_0 = 300 K to emulate a heat sink under the substrate. Because the heat dissipation from the top and side surfaces is negligible due to the small thermal conductivity and a small heat transfer coefficient in natural convection of air, adiabatic boundary conditions are used for these surfaces [6,12–14]. The values of the thermal conductivities of silicon (κ_{Si}), silicon oxide (κ_{ox}) and photonic crystal κ_{eff} are from Ref. [12].

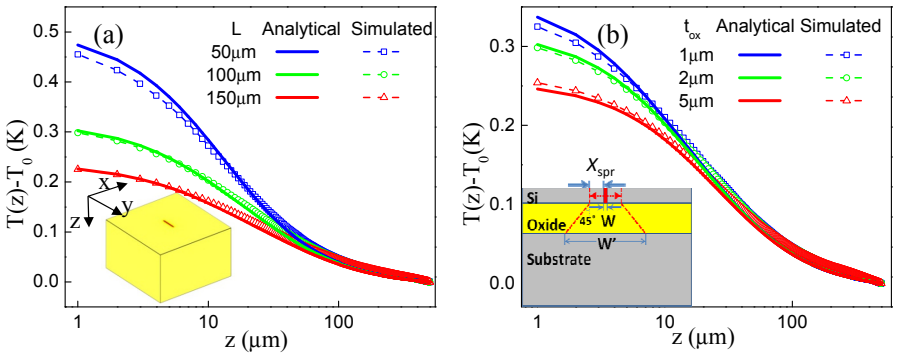

Fig. 2. Temperature profile in the substrate along z-axis with the temperature at the bottom surface of the substrate as the reference, T_0; for a heating power of 5mW. (a) Results for a chip with t_{ox} = 2μm, t_{sub} = 500μm and L as a parameter; the inset shows a typical structure and steady state 3-D FEM simulation result for a simulation chip area of 800μm × 800μm with t_{Si} = 250nm, t_{ox} = 2μm, t_{sub} = 500μm, L = 150μm, and W = 400nm. The corresponding photonic crystal structure has a hole radius $r = 0.25a$, where a is the lattice constant. (b) Results for a chip with L = 100μm, t_{sub} = 500μm and various t_{ox}; the inset shows the schematic of heat spreading in the cross section of the device.

To gain insight into heat conduction in the substrate and develop a semi-analytic model, we first consider the effective cross-sectional area (in the x-y plane) of the vertical heat flux, and then utilize an electric field analogy to obtain the vertical temperature profile in the substrate. Our previous work showed that the heat flux at the top surface of the buried oxide layer has an effective width of $W + 2X_{spr}$ due to lateral thermal spreading in the silicon PCW cladding, where X_{spr} is given by $X_{spr} = \sqrt{t_{Si} t_{ox} \kappa_{eff} / \kappa_{ox}}$ and t_{Si} is the thickness of the top Si layer. As the heat flows down through the oxide layer, it also spreads laterally. With a fixed-angle heat spreading model, we can readily show that the effective width and length of the heat flux cross-section are increased by $\Delta W = \Delta L = 2t_{ox}\tan 45°$ after passing through the oxide layer and reaching the top surface of the substrate [15,16]. A schematic diagram of the cross-section of this model is shown as the inset of Fig. 2(b). On the top surface of the substrate, the effective heat flux cross-section has the dimensions of

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$$W' = (W + 2X_{spr} + 2t_{ox}) \text{ and } L' = (L + 2t_{ox}). \quad (1)$$

Using the above effective width and length of the heat flux at the top surface of the substrate, the temperature distribution in the substrate can be modeled separately using an electric field analogy. In electrostatics, the potential drop along the z-axis due to a finite sheet of charge uniformly distributed on the x-y plane and centered at the origin is given by [17]

$$V(z) - V(0) = -\int_0^z \frac{\rho_s}{\pi\varepsilon} \arctan\left[\frac{(L/2)(W/2)}{z'\sqrt{(L/2)^2 + (W/2)^2 + z'^2}}\right] dz'. \quad (2)$$

where ρ_s is the charge density, ε is the permittivity, and W and L are the width and length of the sheet. It is well known that the steady state heat conduction equation resembles the static electric field equation as both are Poisson's equations [18]. By the thermal-electrical analogy,it can readily be shown that for a similar heat source of width W' and length L', the temperature profile along the z-axis in a semi-infinite (z>0) homogeneous medium is given by

$$T(z) - T(0) = -\frac{2Q/W'L'}{\pi\kappa} \int_0^z \arctan\left[\frac{(L'/2)(W'/2)}{z'\sqrt{(L'/2)^2 + (W'/2)^2 + z'^2}}\right] dz'. \quad (3)$$

where Q is the power of the source, and κ is the thermal conductivity of the medium. Note the z axis points downward and z = 0 is assumed to be on the top surface of the substrate. The factor 2 is due to the semi-infinite medium (the mirror image of the half space of z>0 in the other half space of z<0 that will add a source at $z = 0^-$ so that this half space problem corresponds to a full space problem with a source of 2Q). The integration in Eq. (3) has a fairly lengthy result,

$$\begin{aligned}\{z \arctan[(L'/2)(W'/2)/z\mu(z)] - (L'/2)arc\coth[\mu(z)/(W'/2)] \\ -(W'/2)arc\coth[\mu(z)/(L'/2)]\}\Big|_0^z,\end{aligned} \quad (4)$$

where $\mu(z) \equiv \sqrt{(L'/2)^2 + (W'/2)^2 + z^2}$.

The FEM simulation and semi-analytic results for the temperature profile in the substrate along the z-axis are plotted in Fig. 2(a) for three different values of heat source length. Note that the temperature of the substrate bottom surface, $T(t_{sub}) = T_0$, is used as the reference. In addition, simulations are performed for different values of t_{ox}, as plotted in Fig. 2(b) along with the analytic results. Evidently, the vertical temperature profiles given by semi-analytic theory agree fairly well with the FEM simulations. As could be expected, the (total) temperature rise in the substrate, $\Delta T_{sub} \equiv T(0) - T(t_{sub})$, increases as L or t_{ox} decreases.

3. Fractional thermo-optic tuning due to the substrate

Estimation of the temperature rise in the substrate is important because the temperature change in the top silicon device layer is affected by the temperature rise across the buried oxide layer as well as that of the substrate ($\Delta T_{tot} = \Delta T_{ox} + \Delta T_{sub}$). For example, in thermo-optic tunable delay lines, the total change of the delay time in the PCW ($\Delta\tau_{tot}$), which is proportional to the total temperature rise in the waveguide (for small change of refractive index Δn<<1), is also affected by the temperature rise in the substrate. Assume $\Delta\tau_{tot} = \mu\Delta T_{tot}$, where μ is a constant depending on the thermo-optic coefficient of silicon. Because $\Delta\tau_{tot} = \mu\Delta T_{ox} + \mu\Delta T_{sub}$, we can define the substrate-induced delay tuning as $\Delta\tau_{sub} = \mu\Delta T_{sub}$ (note that $\Delta\tau_{sub}$ does not mean the time delay of light in the substrate, but the delay in the waveguide due to the substrate temperature). Note that ΔT_{ox} can also be analytically expressed as [12]

$$\Delta T_{ox} = Qt_{ox}/(\kappa_{ox} L[W + 2X_{spr}]). \quad (4)$$

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To assess the substrate's contribution in a general manner, it is more convenient to introduce a relative quantity, fractional thermo-optic tuning $f_{sub} = \Delta\tau_{sub}/\Delta\tau_{tot}$.

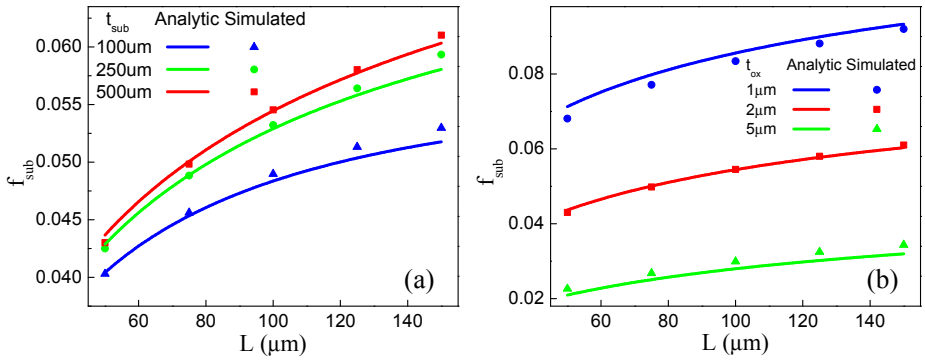

Fig. 3. Fractional delay perturbation due to the substrate as a function of L; (a) For t_{ox} = 2μm with t_{sub} as a parameter; (b) For t_{sub} = 500μm with t_{ox} as a parameter.

Simulations are performed to estimate the fractional thermo-optic tuning due to the substrate. First, the influence of the substrate thickness is investigated. Simulations and semi-analytic calculations are carried out for three different substrate thicknesses and varying heat source lengths. As shown in Fig. 3(a), analytic results agree well with the FEM simulation. Their difference in f_{sub} is less than 5%. From the plot, it is evident that as the substrate thickness increases, f_{sub} increases as expected. In Fig. 3(b), simulation and analytic results are plotted for different buried oxide layer thicknesses. As t_{ox} increases, ΔT_{sub} decreases (and ΔT_{ox} increases); consequently f_{sub} decreases.

For some slow-light delay line applications in the nanosecond range or beyond, the PCW length may reach the millimeter scale or beyond, assuming group indices n_g in the range of 30~100 [12,19]. For thermo-optic delay tuning, similar heater lengths are required. It can be observed in Fig. 3(b) that the value of f_{sub} increases as the heater becomes longer. To explore its upper limit for very long heaters, f_{sub} is calculated semi-analytically for L up to 10mm and the trend is shown in a semi-log plot in Fig. 4.

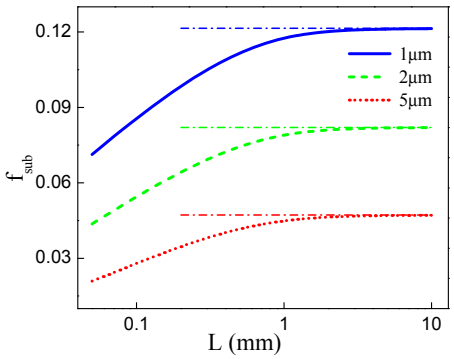

Fig. 4. The trend of fractional delay perturbation: Semi-analytic results for finite L with different oxide layer thicknesses for t_{sub} = 500μm.

Interestingly, as L continues increasing, f_{sub} increases asymptotically towards a finite upper limit whose value depends on t_{ox}. This upper limit occurs because for $L \to \infty$, the structure can be treated as a two-dimensional problem in the x-z plane. For $L \to \infty$, it is

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necessary to define the linear power density as $Q_{Den} = \lim_{L\to\infty} Q/L$. From Eq. (3), by some calculation, the temperature rise across the substrate for $L\to\infty$ can be expressed as

$$\Delta T_{sub,L\to\infty} = \frac{Q_{Den}}{\pi\kappa_{Si}}\left[\frac{t_{sub}}{W'/2}arc\tan\left(\frac{W'/2}{t_{sub}}\right)+\frac{1}{2}ln\left(1+\left(\frac{t_{sub}}{W'/2}\right)^2\right)\right]. \quad (5)$$

Horizontal dashed lines in Fig. 4 show the upper limit of f_{sub} calculated with Eq. (5). Evidently, they agree very well with the results from Eq. (3) at long L. In typical SOI devices, t_{sub} is on the order of hundreds of microns and W' is on the order of tens of microns, thus $t_{sub}>>W'$. This can be used to further simplify Eq. (5) to

$$\Delta T_{sub,L\to\infty} \approx \frac{Q_{Den}}{\pi\kappa_{Si}}\left(1+ln\frac{2t_{sub}}{W'+2X_{spr}+2t_{ox}}\right). \quad (6)$$

Calculations show that the Eq. (6) is a good approximation for Eq. (5). The difference between them is typically very small (e.g. <1%) for $t_{sub}>3W'$. Thus, Eq. (6) is useful in estimation.

4. Minimizing the substrate-induced thermo-optic effect

Although 10% contribution from the substrate might be inconsequential in some digital applications, it can be a significant issue for many analog applications. For example, for tunable optical delay lines used in phased array antennas, the beam angle is proportional to the delay difference between adjacent elements [20]. A 10% variation of the delay difference (which is tuned thermo-optically) will cause a 10% deviation of the beam angle, which represents a significant issue for high-resolution radars (requiring accuracy of ~0.25° for up to 60° scanning angles [21]).

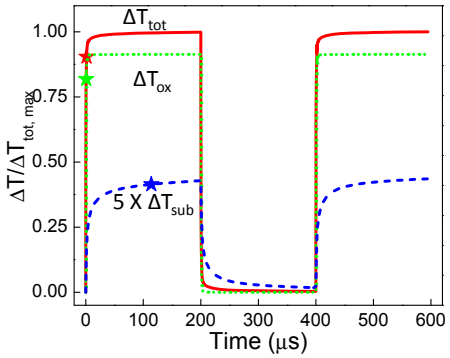

Fig. 5. Transient temperature response to a square-wave heating power with a period of 400μs, a duty cycle of 50%. L = 150μm, t_{sub} = 250μm, and t_{ox} = 1μm. All temperature values are normalized by the steady-state temperature $\Delta T_{tot,max}$. The ΔT_{sub} trace is magnified 5 times for ease of view. For each trace, the 90% point of the rising edge is marked with a star. (10% points of the rising edges of these curves are all close to t = 0, they are not marked to avoid cluttered view).

Furthermore, in transient from one delay state to another state, the substrate temperature profile generally takes a very long time to reach its steady state whereas the oxide temperature profile stabilizes very fast. For precision analog applications, the slow response of the substrate may play a dominant role in determining the overall response time of the device. Consider the example shown in Fig. 5, where the time-dependent ΔT_{ox}, ΔT_{sub}, and

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ΔT_{tot} data are extracted from a FEM simulation of the transient response of a structure. Note that ΔT_{ox} and ΔT_{sub} defined in this work do not refer to a uniform temperature increase in the oxide and the substrate, but the temperature difference between the upper and lower surfaces of these two regions. The rise time (10% to 90%) for ΔT_{sub} is on the order of 100μs whereas the rise time (10% to 90%) for ΔT_{ox} is on the order of 1μs. Note that the 10% point of these traces are all very close to $t = 0$ and their difference in time is very small. On the other hand, the time difference of the 90% points of the ΔT_{sub} and ΔT_{ox} traces is very large; thus only the 90% points are marked. The fall time of each curve is on the same order as its respective rise time. The rise/fall time can be estimated from $\tau \sim Z^2 \rho c / \kappa$ where ρ is the density and c the specific heat capacity of the material and Z is the heat conduction length in this material [12]. For ΔT_{ox}, the pertinent material is the oxide, Z is the thickness of the buried oxide layer. For ΔT_{sub}, the pertinent material is silicon, Z is on the order of the substrate thickness. Silicon and SiO_2 have comparable ρc; and κ_{Si} is about two orders of magnitude higher than κ_{ox}. The substrate thickness is usually two orders larger than the buried oxide thickness. Based on these values, the transient response of the substrate is expected to be roughly two orders of magnitude slower than the buried oxide layer. Assume an analog application requires 1% delay tuning accuracy. Then the device analyzed in Fig. 5 is considered stable only after ΔT_{sub} reach ~90% of its steady-state value (so that ΔT_{tot} reaches 99% of its steady-state value because this device has $\Delta T_{sub} \sim 0.09 \Delta T_{tot}$ in the steady-state). Therefore, for this analog application, the device response time is practically ~100 μs. This is much longer than the intrinsic response time of the oxide layer.

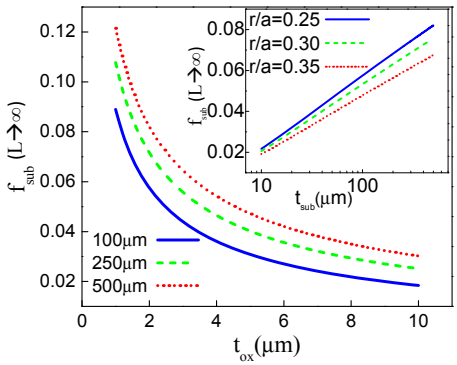

Fig. 6. Trend for $f_{sub}(L \to \infty)$ with t_{ox} as the variable for different substrate thicknesses. The inset shows the influence of the hole radius (with t_{ox} = 2μm).

According to the above discussions, it would be desirable to minimize the influence of the substrate in order to speed up the device response and improve the device stability/precision for many analog applications. To this end, it would be useful to analyze how the upper limit of f_{sub} $(L \to \infty)$ varies with key physical parameters. Results are plotted in Fig. 6 for different substrate thicknesses and oxide thicknesses. It can be seen that the influence of the substrate can be reduced by increasing the thickness of the buried oxide layer. This reduction can be attributed to two trends: ΔT_{ox} increases as $t_{ox}^{1/2}$ and ΔT_{sub} decreases with t_{ox} due to the term $\ln[2t_{sub}/(W + 2X_{spr} + 2t_{ox})]$ in Eq. (6) [12]. When the oxide layer is thicker than 5μm, f_{sub} is less than 5% for all cases shown in Fig. 6. Furthermore, reducing the substrate thickness can also reduce ΔT_{sub} according to Eq. (5). It can be readily shown that f_{sub} varies faster than $t_{ox}^{-1/2}$ with respect to the oxide thickness and varies logarithmically with t_{sub}. Thus, mathematically, f_{sub} can be more effectively reduced by increasing t_{ox}.

However, in practice, thicker oxide layers are less preferable for a number of reasons. First, it would be challenging and costly to achieve t_{ox} >5μm in making high-quality SOI wafers. Second, by increasing t_{ox}, the heat conductance between source and sink becomes

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smaller, which hampers device heat dissipation. Third, thicker oxide will lead to an increase of response time [12], which is not desirable for many active devices. On the other hand, a thinner substrate will provide better heat conductance and thus reduce the response time. Moreover, with the recent advance of membrane technology [22,23], the substrate can be easily reduced to less than 10μm . Thus membrane based devices could help to reduce the substrate-induced thermo-optic tuning.

It should be noted that the structure shown in Fig. 1 is optimal. If the heater is located on a lateral edge of the PCW (e.g. heater located at x_{heater} = 7μm, and the PCW core located at x_{core} = 0), then the temperature rise in the PCW core ΔT_{core} could be 2~3 times smaller than the ΔT_{tot} at the heater due to the exponential temperature drop along x [12]. This can affect f_{sub} in the PCW core. To analyze such a case, we need to consider the total temperature rise in the top Si layer ΔT_{tot}, the vertical temperature difference between top and bottom surfaces of the substrate ΔT_{sub}, and the vertical temperature difference in oxide ΔT_{ox} in *two different vertical planes* at $x = x_{\text{heater}}$ and $x = x_{\text{core}}$, respectively. Obviously, the temperature rise in the core is just ΔT_{tot} in the plane at $x = x_{\text{core}}$, $\Delta T_{core} \equiv \Delta T_{tot}(x_{\text{core}})$. The actual delay tuning is determined by ΔT_{core}. Because ΔT_{core} is much lower than $\Delta T_{tot}(x_{\text{heater}})$, the fractional thermal tuning in the PCW core due to the substrate in this case $f_{sub}(x_{\text{core}}) = \Delta T_{sub}(x_{\text{core}})/\Delta T_{core}$ could be much larger than $\Delta T_{sub}(x_{heater})/\Delta T_{tot}(x_{heater})$ given in preceding sections. In the worst case, $f_{sub}(x_{\text{core}})$ may exceed 20% in a non-optimal structure.

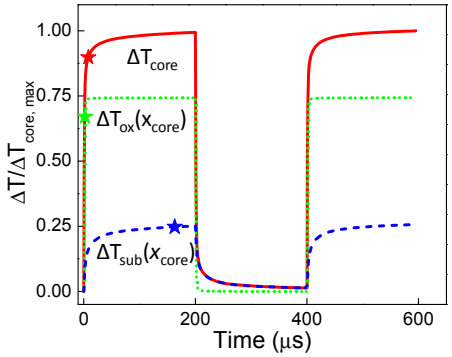

Fig. 7. Simulation result for a non-optimal case where the heater is located at the PCW lateral edge, 7μm from the PCW core (other parameters of this structure are same as in Fig. 5). All temperatures are evaluated in the vertical plane at $x = x_{\text{core}}$. Note $\Delta T_{core} \equiv \Delta T_{tot}(x_{\text{core}}) = \Delta T_{ox}(x_{\text{core}}) + \Delta T_{sub}(x_{\text{core}})$

For example, for the structure simulated in Fig. 5, if the heater is moved to a lateral edge about 7μm from the PCW core, $f_{sub}(x_{\text{core}})$ will reach ~25%, as shown in Fig. 7. Because $f_{sub}(x_{\text{core}})$ is far above 10%, the 10%-90% rise/fall time of $\Delta T_{tot}(x_{\text{core}})$ also elongates to ~12μs (compared to ~1μs rise/fall time from 10% to 90% for ΔT_{tot} in Fig. 5). This can explain the long rise time observed in prior experiments where the heater is located at the PCW edge (for example Ref. [8]). Note that 20% contribution is not negligible in many digital applications, as well as analog applications. This illustrates the importance of design optimization in a wide range of thermo-optic tuning/switching applications. In some cases, configurations with a heater at the PCW edge may be desirable for ease of fabrication, but the performance trade-off needs to be considered for a specific application. The formulas given in this work are useful to guide the design optimization and evaluate the substrate-induced thermal tuning. Note that this theory also indicates that many factors have relatively weak influence on the device performance. For example, the hole radius of the photonic crystal structure, in its typical range (r/a = 025~0.35), has a relatively weak influence on f_{sub}, as shown in the inset of Fig. 6. The heater width W is usually recommended to be relatively small to improve the heating efficiency [12]. As such, typically $W << 2X_{spr}$, and the influence of W on the ΔT_{sub} is

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fairly small according to our calculation. Also note that due to the complex anisotropic structure of a narrow heater embedded in a photonic crystal waveguide, the traditional fixed-angle spreading model is not applicable to this entire structure. The fixed-angle model can, however, be useful for a single *thin* layer such as the buried oxide layer. Within the top silicon layer the temperature variation is very small along y and z axes [12].

Note that there exist small discrepancies between the analytic results and FEM simulation results. The maximum discrepancy of ΔT_{sub} between two approaches is less than 5% in all cases we have simulated. The discrepancy can be attributed to several models used in this semi-analytic theory, including the quasi-1D model for heat transfer in a SOI PCW [12] and the fixed angle spreading model in buried oxide layer [15,16]. Each of these models has been validated in proper conditions with reasonable accuracy (e.g. <6% in Ref. [12]). Also note that in most cases, ΔT_{sub} contributes less than ~12% of ΔT_{tot}. Therefore, 5% discrepancies of ΔT_{sub} contribute less than 0.6% of the discrepancies of the overall temperature ΔT_{tot}. Such discrepancies of ΔT_{tot} are considered very small and very difficult to further improve upon. Furthermore, it should be noted that our motivation for developing a (semi-)analytic theory to describe a phenomenon is not to achieve best accuracy, but to gain physical insight that cannot be obtained through numerical simulations, such as how ΔT_{sub} scales with many key physical parameters given in an analytic expression. It would be highly challenging to obtain such scalings or trends through FEM simulations when multiple parameters are involved and some parameters are varying over a large range. For example, to obtain the asymptotic trend shown in Fig. 4 through FEM simulations, it would require a prohibitive amount of computational resources because it would be necessary to simulate many instances of extremely long/large devices with both L and t_{ox} varying.

It would be interesting to extend this theory to study the substrate-induced effect in other device geometries including air-bridge PCWs or non-photonic crystal structures. For some photonic structures, the ratio of the device dimension along y-axis over that along x-axis is not as large as in PCWs. It can be expected that the substrate-induced effect in such structures will resemble short PCWs, which suggests f_{sub} is typically a smaller value according to Fig. 4. It may also be interesting to extend this work to integrated circuits on a SOI wafer. Because the transistors generally have smaller dimensions along x and y axis, it is expected that the substrate temperature rise due to a single transistor is fairly small. For a complicated circuit including many transistors and metal interconnects in multilayer 3D configurations, it remains a challenging problem to investigate the substrate-induced thermal issues. Detailed discussion of these further research topics is beyond the scope of this work.

5. Conclusion

In conclusion, the influence of the substrate on SOI thermo-optic photonic crystal devices is studied in terms of key physical parameters. The temperature rise in the substrate is calculated semi-analytically. The accuracy of the semi-analytic results is verified by the FEM simulations. The upper limit of the fractional delay tuning due to the substrate is obtained as a function of key physical parameters. For long delay lines, the substrate-induced fractional delay tuning could exceed 10% for heaters in the PCW core and exceed 20% for heaters at the PCW lateral edge. The slow response of the substrate may cause the device to take a long time to stabilize, which may significantly elongate the de facto response time of the device (by 10~100 fold). This could explain slow response observed in some non-optimal device structures and help guide further device optimization. Scaling of the substrate's influence with key structure parameters is analyzed. Strategies of minimizing the influence of the substrate are discussed.

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