Channel Mobility and Contact Resistance in Scaled Zno Thin-Film Transistors

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ABSTRACT

Zno thin-film transistors (TFTs) with scaled channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm are fabricated by a top-down approach using remote plasma atomic layer deposition technique. Current-voltage measurements indicate an *n*-type channel enhancement mode transistor operation, with threshold voltages in the range of 8.4 V to 5.3 V, maximum drain currents of 4.6 μA/μm, 9.7 μA/μm, 19.4 μA/μm, and 24.7 μA/μm, and breakdown voltages of 80 V, 70 V, 62 V, and 59 V with respect to the channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm. Contact resistance, effective electron mobility (including contact resistance) and channel electron mobility (excluding contact resistance) electron mobility extracted using the transmission line method (TLM) demonstrated a dependency on the channel length as a function of gate bias. The channel electron mobility for the 10 μm channel length TFT is 0.782 cm^2/Vs (0.83 cm^2/Vs) at a gate bias of 10 V (15 V) increasing to 8.9 cm^2/Vs (19.04 cm^2/Vs) when the channel length is scaled down to 2 μm. Finally, the contact sheet resistance of 4.6×10^5 Ω/sq extracted from measurements is 3.5$\times$ larger than the contact sheet resistance of 1.3×10^5 Ω/sq obtained from DFT calculation and 1D self-consistent Poisson-Shrödinger simulation showing an increase in the drive current.

1. Introduction

Zno is intensively studied as an alternative channel material for semiconductor TFTs due to its distinctive material properties having a direct wide band gap of 3.37 eV [1], an electron mobility in the range of 1-100 cm^2/Vs at room temperature, and a relatively large breakdown voltage in the range between 50 V-75 V [2]. The most appealing advantages of Zno are low cost fabrication, low thermal resistance, low temperature processing, high resistance to radiation damage, piezoelectricity, and technological compatibility with Si [3]. Lately, Zno was considered as a promising semiconductor material for complementary metal oxide semiconductor (CMOS) technology [4] and integrated circuits [5]. However, many challenges remain that hold back the actual implementation of this promising material. One of the major challenges is a low effective (including contact resistance) electron mobility as well as a low channel (excluding contact resistance) electron mobility in TFTs [5, 6]. Currently, there is no full comprehension of the physical mechanisms behind a relatively low electron mobility despite a known presence of high density of interface traps [7, 8].

In this paper, we study electrical characteristics of Zno TFTs with various channel lengths (10 μm, 5 μm, 4 μm, and 2 μm) fabricated by a top-down approach [4] using remote plasma atomic layer deposition (ALD). Our Zno TFTs exhibit an *n*-channel enhancement mode operation with a large drain current saturation in the range of 5–25 μA/μm. The set of channel lengths allows us to extract a contact resistance, and effective (which includes an external resistance) and channel (which excludes a channel resistance) electron mobility as a function of the gate voltage. The extracted channel mobility is a better representative of device performance because a typically reported low electron mobility in Zno TFTs using transconductance method [6] is due to a large contact resistance. Our study investigates the impact of scaled channel length at two gate voltages on significant device parameters such as threshold voltage (V_{Th}), drain induced barrier lowering (DIBL), subthreshold swing (SS), on-current (I_{On}), leakage current (I_{Off}), on/off ratio, contact resistance, and channel and effective electron mobility. The channel electron mobility indicates some improvement in Zno TFTs as compared to previously reported values for such devices [20, 21, 22, 23, 24]. The channel electron mobility and contact resistance are extracted by using the TLM with different channel lengths. Finally, physically based simulations provide a theoretical limit of the contact resistance using a new approach combining density functional theory (DFT) calculations with the quantum transport at the interface between metal and semiconductor.

2. ZnO Thin-Film Transistors Fabrication Process

The Zno TFTs are fabricated on a *p*-type silicon wafer acting as a back-gate as shown in Fig. 1(a). A 100 nm SiO_2 layer is grown by dry thermal oxidation as a gate insulator. Zno is deposited at 190°C using remote plasma ALD by Oxford Instrument Plasma Technology (OIPT) Flex Al system with diethyl zinc as a precursor with a RF power of 100 W, a pressure of 80 mTorr, and an O_2 flow of 60 sccm as shown in Fig. 1(b). The advantage of using the remote plasma ALD technique compared to water-based oxidation [4] is the reduction of OH impurities which can increase film resistiv-

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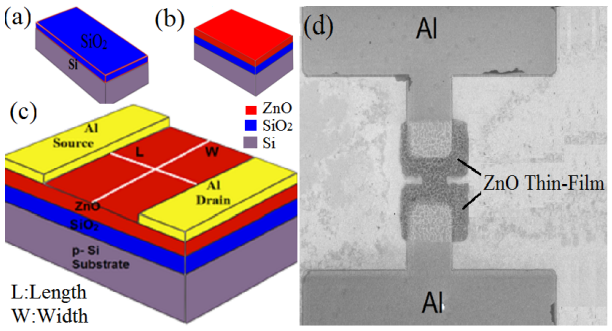

Figure 1: Top-down fabrication process of Zno TFTs: (a) SiO_2 thermally grown through a dry oxidation of 100 nm, (b) Zno thin film deposited in the remote plasma technique, (c) a schematic structure of the Zno TFT fabricated via a remote plasma atomic layer deposition (ALD), (d) SEM images of Zno TFTs with Al pads which serve as contacts.

ity [4]. The Zno thin film is defined by photo-lithography and anisotropic inductive coupled plasma (ICP) etching based on CHF_3 gas chemistry. Finally, a 500 nm thick Al metal electrode is deposited by an electron beam evaporation and lift-off as top source and drain contacts. A scanning electron microscope (SEM) image of the fabricated device is shown in Fig. 1(d) [4].

3. Device Characteristics and Mobility

Fig. 2 shows output (I_D-V_D) characteristics of Zno TFTs with different channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm measured at room temperature. The devices exhibit an *n*-type operation mode in the range of V_D = 0-20 V [9]. The output characteristics show a well-distinguished linear region at a low drain bias and a saturation region at a high drain bias [10]. At a high gate bias (V_G = 20 V), the maximum attainable (I_D) values increase proportionally with a decrease in the channel length (L_{ch}) from 10 μm to 2 μm. The maximum drain currents for 10 μm, 5 μm, 4 μm, and 2 μm are 4.6 μA/μm, 9.7 μA/μm, 19.4 μA/μm, and 24.7 μA/μm, respectively. As the source/drain voltage increases, the channel/drain depletion region shifts to the source side and electrons in the channel are quickly drifted to the drain. When the channel length of the Zno TFTs is scaled down by decreasing the distance between the source and the drain, the electric field along the channel increases leading to an increase in acceleration of electrons by the electric field in the channel. Consequently, the injection of electrons from the source into the channel becomes a more efficient due to the increase in electric field. Since the electrons gain a larger kinetic energy to overcome Schottky barrier height between the source and the drain by thermionic transport and tunnelling through the Schottky barrier. This increase in the electron velocity due to electron acceleration accompanied by an increase in electron density is also the main reason for the increase in a maximum drain current [9].

To study the impact of the channel length scaling on device performance, Fig. 3 illustrates the transfer characteristics (I_D-V_G) at a fixed drain bias of 5 V for different channel lengths of L_{ch} = 10 μm, 5 μm, 4 μm, and 2 μm. The sub-threshold region exhibits approximately a linear behaviour of the drain current on logarithmic scale which indicates well behaved transistor characteristics with a small leakage current. Transistors with channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm have sub-threshold slopes of 1.67 V/dec, 0.75 V/dec, 0.57 V/dec, and 0.41 V/dec, respectively. These sub-threshold slopes are relatively large when compared to the ideal slope of Si MOSFET of 60 mV/dec at room temperature but will provide a relatively low leakage current and a good on/off ratio in low-power applications (with respect to the on-current and the breakdown voltage). The decrease in the sub-threshold slope follows the decrease in the channel length [9]. In the sub-threshold region, drain current (I_D) is dominated by a diffusion transport of carriers and is inversely proportional to L_{ch} [9]. To evaluate a performance of the scaled Zno TFTs in circuits, the I_{On}/I_{Off} ratio is extracted by comparing the maximum drain current (I_{On}) as a function of the gate voltage (V_G) against the drain current (I_{Off}) at the gate voltage equal to zero (all the TFTs are enhancement mode). The I_{On}/I_{Off} ratios are 1.5 $\times 10^4$,

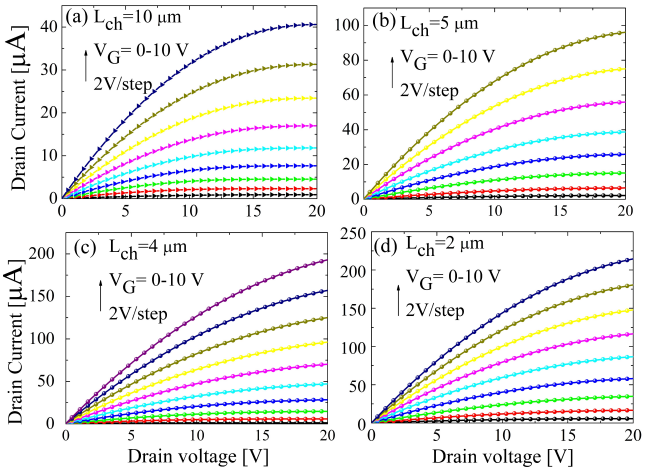

Figure 2: Output I_D-V_D characteristics from V_G = 0 V to 10 V with a step of 2 V for Zno TFTs with different channel lengths (L_{ch}) of (a) 10 μm, (b) 5 μm, (c) 4 μm, and (d) 2 μm.

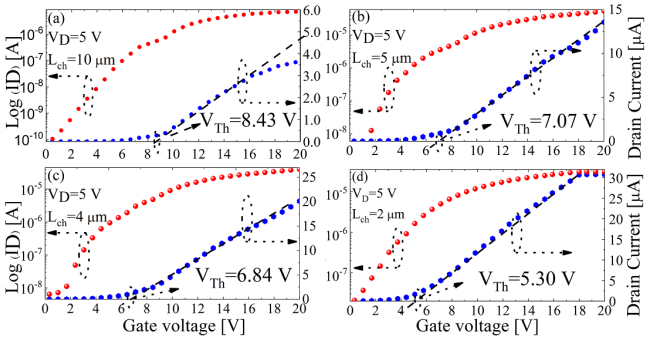

Figure 3: Transfer I_D-V_G characteristics under a fixed drain bias of 5 V for (a) 10 μm, (b) 5 μm, (c) 4 μm, and (d) 2 μm channel length Zno TFTs. The width of the all TFTs is 10 μm.

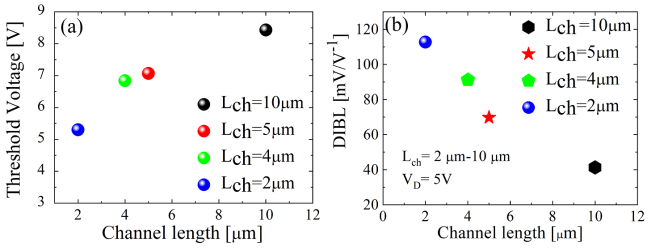

Figure 4: (a) Variation of threshold voltage (V_{Th}) as a function of the channel length. (b) The drain induced barrier lowering (DIBL) of Zno TFTs versus the channel length of $L_{ch} = 10\ \mu$m, 5 μm, 4 μm, and 2 μm.

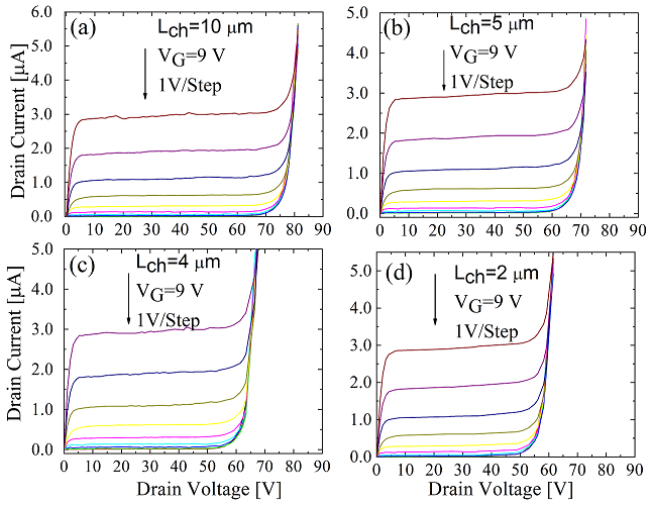

Figure 5: Output I_D-V_D characteristic of a Zno TFTs with a channel length $L_{ch} = 10\ \mu$m, 5 μm, 4 μm, and 2 μm exhibiting a breakdown voltage of 79.91 V, 70.07 V, 64.68 V, and 58.85 V.

4.2 $\times 10^4$, 5.3 $\times 10^4$, and 8.3 $\times 10^4$ for channel lengths of $L_{ch} = 10\ \mu$m, 5 μm, 4 μm, and 2 μm, respectively, which provides solid on/off ratios for switching in digital and analogue low-power applications. The I_{On}/I_{Off} ratio decreases with the channel length decrease also because the threshold voltage shifts toward larger positive values [10]. Fig. 4(a) shows an extracted threshold voltage (V_{Th}) versus the channel length. The threshold voltage for the 10 μm and the 5 μm channel length Zno TFTs are 8.43 V and 7.07 V, respectively. When the channel length decreases further to 4 μm and 2 μm, the threshold voltage decreases to 6.84 V and to 5.30 V, respectively. The decrease in a sub-threshold voltage with a decrease in the channel length is caused by the increase in electron density in the channel. Thus, it becomes easier to create an accumulation channel for a given gate bias that results in a decrease in V_{Th} [11]. When the long channel length (10 μm) transistor is compared to the short channel length (2 μm) transistor, the threshold voltage decreases by 37 %. The charge distribution in the channel is strongly influenced by the field originating from the source/drain and the depletion region around the source and the drain becomes larger [11]. The barrier for electron injection from the source to the channel is thus slightly decreased. Therefore, a conduction between the source and the drain occurs at a smaller gate overdrive leading to the reduction in the threshold voltage during the scaling [12].

The Schottky barrier height in the transistor channel is controlled by both the gate-to-source voltage (V_G) and the drain-to-source voltage (V_D). If the drain voltage is increased, the potential barrier in the channel decreases, leading to a drain-induced barrier lowering (DIBL). The experimental results for the DIBL versus channel lengths (L_{ch}) for 10 μm, 5 μm, 4 μm, and 2 μm of Zno TFTs are plotted in Fig. 4(b). As the channel becomes shorter, the DIBL becomes more pronounced. When the channel length is sufficiently large, the source and the drain junctions will be apart from each other with no effect on Schottky barrier between them [9]. By decreasing the channel length, the space charge at the drain will interact with that at the source which leads to a potential barrier lowering in a space between the source to the channel [11].

Finally, the breakdown voltage has been measured in carefully designed experiments to protect device functionality from unexpected burn out due to undue large applied bias [4]. A drain bias (V_D) has been increased slowly until the drain current promptly increased. The results from these investigations of a breakdown voltage for the TFTs are shown in Fig. 5. Devices with channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm have exhibited breakdown voltages of approximately 79.91 V, 70.07 V, 61.68 V, and 58.85 V, respectively. These are relatively high breakdown voltages which are very promising for circuit applications with high drive voltage requirements such as a display panel and a diode [4].

The total on resistance, R_{Tot}, has been extracted from the linear region of I_D-V_D characteristics for different channel lengths of L_{ch} 10 μm, 5 μm, 4 μm and 2 μm TFTs at two gate biases (10 V and 15 V). In order to normalise the total resistance, the value of R_{Tot} is multiplied by the width ($W = 10\ \mu$m) to obtain a value in Ω.cm^2. Fig. 6(a) shows the normalised total resistance for all transistors for the 10 μm, 5 μm, 4 μm, and 2 μm channel lengths at two gate biases of 10 V and 15 V which will be used in the transmission line method (TLM) [12] to extract carrier mobility. The normalised total resistances is found to be decreasing from 0.3659 Ω.cm^2 at $V_G = 10$ V to almost 0.297 Ω.cm^2 when compared to the one measured at $V_G = 15$ V. The normalised total resistance for the 10 μm channel length Zno TFT is three times larger than the total resistance resistance for the 2 μm channel length device (the normalised total resistance becomes proportional to the channel length). When electric field increases in the channel region as the result of scaling down the source-to-drain distance or as the result of increase in the drain bias, electrons in the channel will gain a large kinetic energy. Electrons with a large kinetic energy will overcome Schottky barrier between metal and semiconductor more efficiently thus lowering access resistance [9, 13]. The lower access resistance leads to more electrons to contribute to the channel transport, increasing

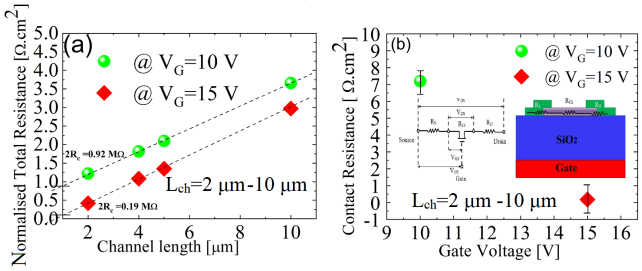

Figure 6: (a) Total on and (b) contact resistance versus the gate voltage at two different gate biases (V_G=10 V and 15 V). The inset schematic (a) shows the TLM of structure and the schematic diagram (b) the contact and the channel resistances in Zno TFTs.

electron density in the channel.

The total on resistance is proportional to a channel length so the decrease in the channel length will decreases the total resistance. Thus, R_{Tot} can be expressed linearly with dependence on the channel length. The contact resistance R_{C} can be calculated using results from the TLM assuming that the normalised total resistance is independent of the potential drop across the contacts at the source and the drain [13] and its change is only proportional to the channel length. Contact resistance per channel length presented in Fig. 6(b) is extracted from the slope of the drain current versus the drain voltage (I_D-V_D) at two different gate voltages (10 V and 15 V). The contact resistance is about 7.2 $\times 10^{-2}$ Ω.cm^2 at a gate voltage of 10 V. When the gate voltage is increased to 15 V, the contact resistance reduces to 0.177 $\times 10^{-2}$ Ω.cm^2, a decrease of 106.78 %. When the gate voltage increases from 10 V to 15 V, the Schottky barrier height reduces at the source/drain resulting in a more efficient accumulation of charge thanks to increased kinetic energy of electrons that contribute into carrier transport along the channel [14, 15] as described before.

The effective mobility, μ_{eff}, was determined in the linear regime using the conventional MOSFET equation for $V_D << (V_G - V_{\mathrm{Th}})$ [9]:

$$I_D = \mu_{\mathrm{eff}} C_{\mathrm{Tot}} \frac{W}{L}[(V_G - V_{\mathrm{Th}})V_D - \frac{V_D^2}{2}] \quad (1)$$

Eq. (1) can be simplified in a linear region by neglecting a quadratic term as:

$$I_D = \mu_{\mathrm{eff}} C_{\mathrm{Tot}} \frac{W}{L}(V_G - V_{\mathrm{Th}})V_D \quad (2)$$

and then re-written as:

$$\mu_{\mathrm{eff}} = \frac{I_D}{V_D}\frac{L}{W C_{\mathrm{Tot}}}\frac{1}{[V_G - V_{\mathrm{Th}}]} \quad (3)$$

or:

$$\mu_{\mathrm{eff}} = \frac{1}{R_{\mathrm{Tot}}}\frac{L}{W C_{\mathrm{Tot}}[V_G - V_{\mathrm{Th}}]} \quad (4)$$

where $R_{\mathrm{Tot}} = \frac{I_D}{V_D}$ is the slope, W is the width of the device, L is the channel length, and C_{Tot} is the total gate capacitance. In the depletion region, the total capacitor consists of two capacitors in series, the oxide capacitor, C_{ox}, and the depletion layer capacitor, C_{Si}. Therefore, the total capacitance for the device can be described as:

$$\frac{1}{C_{\mathrm{Tot}}} = \frac{1}{C_{\mathrm{ox}}} + \frac{1}{C_{\mathrm{Si}}} \quad (5)$$

The total gate capacitance C_G is related to the total capacitance per unit area C_{Tot} as [4]:

$$C_G = C_{\mathrm{Tot}} A, \;\; C_{\mathrm{Si}} = \frac{\varepsilon_{\mathrm{Si}}\epsilon_0}{t_{\mathrm{Si}}} \;\; \text{and} \;\; C_{\mathrm{ox}} = \frac{\varepsilon_{\mathrm{Si}}\epsilon_0}{t_{\mathrm{ox}}} \quad (6)$$

where A is the area of the bottom gate, ε_r is the relative static permittivity (also called the dielectric constant) of the material (for a vacuum, $\varepsilon_r = 1$), ε_0 is the permittivity of vacuum ($\varepsilon_0 \approx 8.854 \times 10^{-12}$ F.m^{-1}), t_{Si} is the thickness of Si substrate and t_{ox} is the oxide thickness.

The effective electron mobility extracted for 10 μm, 5 μm, 4 μm, and 2 μm channel length TFTs at two different biases (10 V and 15 V) is plotted in Fig. 7(a). The mobility increases with a decrease in the channel length at both gate biases of V_G=10 V and 15 V. When a gate bias increases from 10 V to 15 V, the electron effective mobility increases from 0.11 cm^2/Vs to 0.38 cm^2/Vs (about 71.05 %) for the 10 μm channel length TFTs as well as increases from 1.28 cm^2/Vs to 2.86 cm^2/Vs (about 55.24 %) for the 5 μm channel length, from 1.77 cm^2/Vs to 3.25 cm^2/Vs (about 45.54 %) for the 4 μm channel length, and from 2.9 to 4.04 cm^2/Vs (about 28.22 %) for the 2 μm channel length TFTs, respectively. The electron mobility increases with the gate voltage increase due to the increase in kinetic energy of electrons and also leads to a more efficient de-trapping of electrons from surface traps [8]. The electrons trapped at a surface act as scattering centres that interact with the flow of mobile carriers in the channel due to remote Coulomb scattering.

The electron channel mobility is obtained using the conventional MOSFET equation for channel mobility [9]. The total resistance has two contributions from the contact resistance and the channel resistance as [9]:

$$R_{\mathrm{Tot}} = R_{\mathrm{C}} + R_{\mathrm{ch}} = R_{\mathrm{C}} + \frac{L}{W C_{\mathrm{ox}} \mu_{\mathrm{ch}}}\frac{1}{(V_G - V_{\mathrm{Th}})} \quad (7)$$

where the channel resistance can be expressed using Eq. (4) in which R_{Tot} is replaced by the channel mobility R_{ch} and the effective electron mobility μ_{eff} is replaced by the channel electron mobility μ_{ch}.

Since we have extracted the contact resistance plotted in Fig. 6(b) at a channel length of zero ($L = 0$), the channel electron mobility (μ_{ch}) can be expressed by re-arranging Eq. (7) as:

$$\mu_{\mathrm{ch}} = \frac{L}{W}\frac{1}{Q_{\mathrm{inv}}(R_{\mathrm{Tot}} - R_{\mathrm{C}})} \quad (8)$$

where Q_{inv} is the inverse charge in the channel region. When $V_G \gg V_{\mathrm{Th}}$, the inverse charge is given by:

$$Q_{\mathrm{inv}} = C_{\mathrm{ox}}(V_G - V_{\mathrm{Th}}). \quad (9)$$

Table 1
Effective and channel electron mobility extracted using Eq. (8) at two different gate biases of V_G=10 V and 15 V.

L_{ch}	10μm	5μm	4μm	2μm
μ_{eff} @ V_G=10 V (cm^2/Vs)	0.11	1.28	1.77	2.9
μ_{eff} @ V_G=15 V (cm^2/Vs)	0.38	2.86	3.25	4.04
μ_{ch} @ V_G=10 V (cm^2/Vs)	0.78	8.28	8.30	8.9
μ_{ch} @ V_G=15 V (cm^2/Vs)	0.83	9.86	10.25	19.04

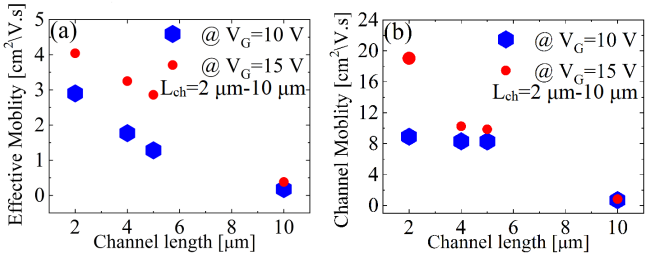

Figure 7: Effective (a) and channel (b) electron mobility extracted using the TLM versus the channel length at two different gate biases of V_G = 10 V and 15 V. Channel mobility excludes a contact resistance.

Fig. 7(b) shows that the extracted channel electron mobility of Zno TFTs, which is also summarised in Table 1, increases with the decreasing of the channel length. The channel mobility also increases when comparing values at gate biases of 10 V and 15 V. The channel mobility will increase from 0.782 cm^2/Vs to 0.83 cm^2/Vs by about 6 % for the 10 μm channel length TFT, from 8.28 cm^2/Vs to 9.86 cm^2/Vs for the 5 μm channel length TFT by about 16 %, from 8.30 cm^2/Vs to 10.25 cm^2/Vs (about 13 %) for the 4 μm channel length TFT, and from 8.9 cm^2/Vs to 19.04 cm^2/Vs (around 53 %) in the 2 μm channel length transistor. The increase of the channel electron mobility during the channel scaling is indicative of a less frequent scattering due to the increase in kinetic energy of electrons resulting from the increase in electric field along the channel [8, 16].

4. DFT Calculations of Zno Electron Effective Mass and Density of States

Density functional theory (DFT) is used to calculate electron band structure of hexagonal Zno using a software package QuantumATK by Synopsys [25]. In the calculations, the lattice constants are set to a = 3.249 ∀ and c = 5.207 ∀. The meta generalized gradient approximation (MGGA) [26] is selected to obtain a material band gap instead of a more common generalized gradient approximation (GGA). The band gap between the maximum of the valence band (green line in Fig. 8(a)) and the minimum of the conduction band (red line in Fig. 8(a)) is calculated to be 3.32 eV, which is close to the experimental value of 3.37 eV [1]. The density of states (DoS) is shown in Fig. 8(b), where angular quantum numbers 0, 1, 2 correspond to s, p, d orbitals, respectively. Electron effective mass at Γ point is calculated to be 0.25 m_0 using a hybrid functional, where m_0 is the free electron mass. This extracted electron effective mass in Zno will be used in the next section to calculate sheet resistance of the Al contact to the Zno thin film as schematically shown in Fig. 9(b).

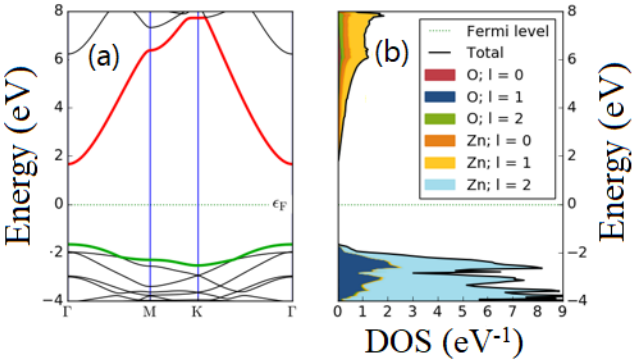

Figure 8: (a) The band gap structure of Zno with indicated minimum of the conduction band (red line) and maximum of the valence band (green line) and (b) the density of states (DoS) obtained from DFT calculations. Fermi level is set at zero energy.

5. 1D Transport Simulation of the Zno Source-Drain Contact

The sheet resistance of the Al contact to the Zno thin film is schematically illustrated in Fig. 9(a). Carrier transport through the structure is modelled using self-consistently coupled 1D Poisson-Shrödinger equations (PS) [27]. Fig. 9(b) shows a schematic of energy band diagram for the Al/Zno/SiO_2 heterostructure at equilibrium. The electron band structure considered in the simulations is chosen to match the size and the composition of the experimental structure [4] depicted in Fig. 9(c). The thicknesses of the layers, depicted in Fig. 10(a), are collected together with doping concentration, energy band gap, conduction band offset, mobility, electron effective mass, and permittivity of the materials in Table 2. Fig. 10(b) shows the conduction and valence bands, and Fermi level from the solution of 1D PS equations. We assume a metal work function of Al (4.28 eV) and calculate Schottky barrier height (SBH) as the potential difference between the work function and the electron affinity [28]. The electron effective mass is extracted from the DFT calculations shown in Fig. 8(a).

The 1D PS simulations assume that the contact sheet resistance of the Zno TFTs is determined by electron transport through the top source and drain contacts into the Zno thin film channel. Therefore, only Al/Zno layer structure is considered in simulations of a sheet source/drain contact resistance. The calculated contact sheet resistance is 1.286×10$^5\Omega$/sq.

Table 2
Zno, SiO_2 and Si material parameters: layer thickness, *n*-type doping, band gaps, conduction band offset, electron mobility, electron effective mass, (m_0 is the electron mass in vacuum), and relative material permittivity used in the modelling of the source/drain contact.

Material	Thickness [nm]	*n*-type doping [cm^3]	E_G [eV]	ΔE_C [eV]	μ [cm^2/Vs]	m_e [× m_0]	ε_r [%]
Zno	80	1×10^{17}	3.37	0.25	50	0.25	8.5
SiO_2	100	1×10^{16}	8.9	0.75	2500	0.33	8.0
Si	625,000	1×10^{16}	1.12	0.35	450	0.17	11.9

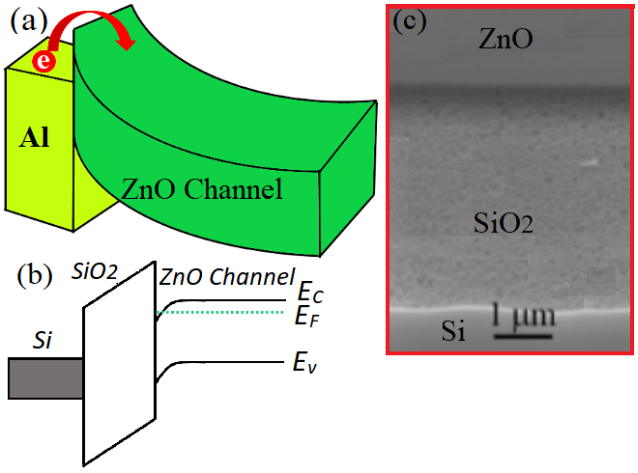

Figure 9: (a) A schematic showing electron transport through the barrier created at the Al/Zno interface, (b) a schematic of electron band structure of $ZnO/SiO_2/Si$ layers, and (c) cross-sectional SEM image of the fabricated $Zno/SiO_2/Si$ layers.

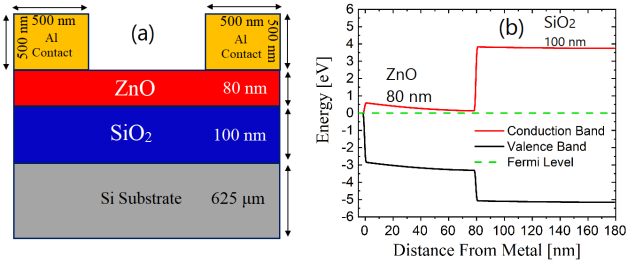

Figure 10: (a) Schematic of layer structure for $Al/Zno/SiO_2$ heterostructure. (b) Conduction and valence band profiles at equilibrium of the $Al/Zno/SiO_2$.

This value is smaller (3.5× smaller) than the contact sheet resistance of 4.6×10^5 Ω/sq obtained from experimental measurements by the TLM. The simulated smaller sheet resistance is a result of assuming ideal Schottky contact which neglects any traps or voids at the contact which increase the sheet resistance but the simulated sheet resistance is in a close order of magnitude of the measured one.

6. Conclusion

Zno TFTs have been fabricated by a top-down approach using the remote plasma ALD technique with different channel lengths (2 μm, 4 μm, 5 μm, and 10 μm). Current-voltage measurements demonstrated an *n*-type channel enhancement mode transistor operation, with threshold voltages in the range of 8.4 V to 5.3 V, maximum drain currents of 4.6 μA/μm, 9.7 μA/μm, 19.4 μA/μm, and 24.7 μA/μm, and breakdown voltages of 80 V, 70 V, 62 V, and 59 V with respect to channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm, respectively. Transistors with different channel lengths in the range 2 μm to 10 μm have demonstrated a good performance for electronic applications, such as display panel and diode.

We have observed a decrease in the sub-threshold slope in TFTs with channel lengths of 10 μm to 5 μm, 4 μm, and 2 μm from 1.67 V/dec to 0.75 V/dec, 0.57 V/dec, and 0.41 V/dec, respectively. The dependence of the total contact resistance on the channel length at two gate voltages (10 V and 15 V) has been also studied. We have found that the total contact resistance decreases with increasing gate voltage. We have shown that the effective (μ_{eff}) electron mobility increases with scaling the source-to-drain distance. In addition, we have demonstrated that the channel (μ_{ch}) electron mobility increases from 0.78 cm^2/Vs to 8.28 cm^2/Vs, 8.30 cm^2/Vs, and 8.9 cm^2/Vs at $V_{\text{G}} = 10$ V (from 0.83 cm^2/Vs to 9.86 cm^2/Vs, 10.25 cm^2/Vs, and 19.04 cm^2/Vs at $V_{\text{G}} =$ 15 V) with the decrease in a channel length from 10 μm to 5 μm, 4 μm, and 2 μm, respectively. The effective electron mobility in Zno TFTs is found to be in the range of 0.6 cm^2/Vs to 13.6 cm^2/Vs [18] and the channel electron mobility has been reported to be about 25 cm^2/Vs [19]. The effective and channel electron mobility summarised in Table 1 is comparable to those reported in the literature for the Zno TFTs [20, 21, 22, 23, 24]. The increase in effective mobility also causes an increase in the I_{On} current. The I_{On} in the Zno TFT with a channel length of 2 μm is larger by 82 % than the I_{On} in the TFT with a channel length of 10 μms because of lower parasitic series resistance.

The increase in the channel electron mobility in the scaled Zno TFTs is caused by electron kinetic energy increase due to the increase in electric field along the channel, which also leads to less electron scattering with phonon and interface roughness, and reduced trapping. Since the electron scattering occurs close to the conduction band edge, the increase in the applied bias (from 10 V to 15 V) will result in increased kinetic energy of electrons which will be able to move effectively along the channel. Therefore, for example, the channel electron mobility observed in the 2 μm channel length device at 15 V is more than one times larger than the mo-

bility at 10 V. This relatively large electron mobility can be further increased by surface passivation which can mitigate a large density of traps at the surface of Zno TFTs.

Finally, we have also calculated the contact sheet resistance using 1D self-consistent PS simulations. The electron effective mass in these PS simulations has been extracted from the Zno band structure obtained in DFT calculations. The calculated contact sheet resistance from the simulations is 1.286×10^5 Ω/sq which is smaller than the value of 4.6×10^5 Ω/sq obtained experimentally by the TLM measurements. The smaller value ($\sim 3.5\times$ smaller) is a reflection of assuming ideal Schottky contact which neglects any contact defects like traps or voids.

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Declaration of interests

 The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: