UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES

School of Electronic and Computer Science

Sustainable Electronic Technologies Group

Hot-Wire Chemical Vapour Deposition (HWCVD) Hydrogenated Amorphous Silicon (a-Si:H) Compact 3D Slope Waveguide Interconnect for Vertical Coupling in Multilayer Silicon Photonics Platform

by

Dk Rafidah Pg Hj Petra

Thesis for the degree of Doctor of Philosophy

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UNIVERSITY OF SOUTHAMPTON

Abstract

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This research project investigates three-dimensional (3D) waveguide interconnects for vertical integration in multilayer silicon photonics (SiP). Multilayer configuration permits the freedom for stacking up a large number of optical components on a single chip to obtain a dense circuit footprint. However, the challenge in realizing multilayer technology is making 3D vertical optical vias through depositable material that is compatible with a complementary metal-oxide-semiconductor (CMOS) fabrication line. The main requirement for a 3D vertical via is a compact design, preferably using a high index waveguide material, for efficient utilization of silicon real estate.

An interlayer slope waveguide coupler which directly couples light from one signal plane to another is proposed. The design of the interlayer coupler was inspired by electrical interconnects in CMOS circuitry, with device structure analogous to an S-bend waveguide. The proposed 3D coupler is compact to allow for high-density integration within a small footprint area. The structure comprises a waveguide placed at a low-level plane and another waveguide at an upper-level plane, connected by a waveguide on a slope. The slope with bending geometry is employed to allow gradual transition of light propagation at the slope interfaces. This avoids large scattering losses due to abrupt change at the slope junctions. The inclination angle of the slope determines the characteristics of the device. The interlayer slope waveguide is characterised in terms of loss in dB per slope. Similar to any waveguide bend, minimal slope loss can be achieved at a large bend radius which effectively means a small inclination slope angle. Thus it is necessary to work at the smallest possible inclination slope angle, while maintaining compactness.

The novelty in this work is the fabrication of a slope structure, designed to be used as a platform for transporting the optical signal directly from one plane to another. Silicon dioxide (SiO_2) deposited by plasma-enhanced chemical vapour deposition (PECVD) at 350^{o}C was used as the slope platform. The slope structure was obtained by wet etching the PECVD SiO_2 in buffered hydrofluoric acid,

NH_4:HF (7:1), using S1813 as the optical lithography resist. By varying the parameters during the optical lithography process, four slope angles were obtained: 11.8°, 16.7°, 20.8° and 25.3°. Subsequently, a hot-wire chemical vapour deposition (HWCVD) tool was used to deposit hydrogenated amorphous silicon (a-Si:H) film as the guiding material. Two sets of waveguide were fabricated, having dimensions of (i) 400 nm (*w*) by 400 nm (*h*), and (ii) 600 nm (*w*) by 400 nm (*h*). From the measurements, the lowest loss equal to 0.17 dB/slope was obtained from the 11.8° slope angle for 600 nm (*w*) by 400 nm (*h*) waveguide dimensions. The highest loss equal to 0.47 dB/slope was obtained from the 25.3° slope angle for 400 nm (*w*) by 400 nm (*h*) waveguide dimensions. The increase in loss is apparent to be originated from the significant mode-mismatch, which in turn was caused by a high effective index difference and a substantial change in the direction of propagation through the bend in the higher slope angle.

As part of the research on making the interlayer slope waveguide coupler, an experiment was conducted to measure crosstalk between two waveguides placed orthogonally to each other. The two waveguides were separated by a PECVD SiO_2 cladding layer of varying different thickness. The aim of this experiment was to investigate the minimum cladding thickness required to isolate two waveguides placed orthogonally on top of each other, and to demonstrate the ability of the interlayer slope waveguide to function in a multilevel optical network. In the measurement, crosstalk isolation of 22 dB was achieved from a thickness of 200 nm for waveguide dimensions of 400 nm (*w*) by 400 nm (*h*). Furthermore, waveguide dimensions of 1000 nm (*w*) by 400 nm (*h*) were isolated by 21 dB with 50 nm waveguide separation. The measured results conform to the theory and simulated results, in which smaller waveguides require higher isolation than larger waveguides. All measurements were obtained for a wavelength of 1550 nm with transverse electric (TE) mode polarization.

In demonstrating the interlayer slope waveguide to function as an actual waveguide coupler in a multi-level platform, a device called a fly-over slope waveguide was designed and fabricated. The development of this device is still at a preliminary stage due to time constraints. The first finding from this experiment was that crosstalk isolation with an average value of 45 dB was achieved when the separation between the two crossing waveguides was larger than 10 μm in the *x*-direction and 1 μm in the *z*-direction. Second, coupling increased to 18 dB when the underlying waveguide was placed 0 μm in the *x*-direction and 290 nm closer to the slope interface in the *z*-direction. These results conformed to the previous crosstalk experiment, in which minimum cladding thickness required to isolate two crossing waveguides was 200 nm for waveguide dimensions of 400 nm (*w*) by 400 nm (*h*). Therefore, the proposed interlayer slope waveguide can be used as a 3D vertical optical via for a multilayer SiP platform.

Table of Contents

Table of Tables

Table of Figures

Table of Figures

Table of Figures

Research Thesis: Declaration of Authorship

Print name:	Dk Rafidah Pg Hj Petra

Title of thesis:	Hot-Wire Chemical Vapour Deposition (HWCVD) Hydrogenated Amorphous Silicon (a-Si:H) Compact 3D Slope Waveguide Interconnect for Vertical Coupling in Multilayer Silicon Photonics Platform.

I declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. Parts of this work have been published as shown in the List of Publications that follows:

Signature:		Date:	10th March 2019

List of Publications

Journals

1. **HWCVD a-Si:H interlayer slope waveguide coupler for multilayer silicon photonics platform (Submitted on 14th January 2019 to Optics Express – Under review)**

   Rafidah Petra, Swe Zin Oo, Antulio Tarazona, Robert Cernansky, Scott Reynolds, David J Thomson, Ali Z Khokhar, Alberto Politi, Goran Z Mashanovich, Graham T Reed, Harold MH Chong, *Optics Express.*

2. **HWCVD a-Si:H 3D flyover slope waveguide (Written and ready for submission to Optics Express)**

   Rafidah Petra, Swe Zin Oo, Antulio Tarazona, Scott Reynolds, David J Thomson, Ali Z Khokhar, Goran Z Mashanovich, Graham T Reed, Harold MH Chong, *Optics Express.*

3. **Hot-wire CVD low-loss a-Si:H waveguides for silicon photonic devices (published)**

   Swe Zin Oo, Antulio Tarazona, Ali Z Khokhar, **Rafidah Petra**, Yohann Franz, Goran Z. Mashanovich, Graham T. Reed, Anna C. Peacock and Harold M. H. Chong, *Photonics Research*, vol. 7(2), 2019.

4. **Low-Loss Silicon Waveguides and Grating Couplers Fabricated Using Anisotropic Wet Etching Technique**

   Kapil Debnath, Hideo Arimoto, Muhammad Khaled Husain, Alyssa Prasmusinto, Abdelrahman Al-Attili, **Rafidah Petra**, Harold M. H. Chong, Graham T. Reed, and Shinichi Saito, *Frontiers in Materials*, vol. 3, 2016.

Conferences

1. **HWCVD a-Si:H interlayer slope waveguide coupler for multilayer silicon photonics platform**

   Rafidah Petra, Swe Zin Oo, Antulio Tarazona, Robert Cernansky, Scott Reynolds, David J Thomson, Ali Z Khokhar, Alberto Politi, Goran Z Mashanovich, Graham T Reed, Harold MH Chong,

   IEEE 14th International Conference on Group IV Photonics (GFP) 2017, 23rd – 25th August 2017, Berlin, Germany.

2. **Hot-wire CVD a-Si:H for low loss silicon photonic waveguides**

   Swe Zin Oo, Antulio Tarazona, **Dk Rafidah Pg Hj Petra**, Ali Khokhar, Graham Reed, Anna Peacock and Harold Chong,

   Conference on Lasers and Electro-Optics 2018, 29th July 2018 – 3rd August 2018, Hongkong, China.

3. **HWCVD for silicon photonics: A new industrial application**

   Antulio Tarazona, Swe Zin Oo, Thalia Bucio Dominguez, **Dk Rafidah Pg Hj Petra**, Ali Khokhar, Vinita Mittal, Frederic Gardes, Graham Reed and Harold Chong,

   10th Hot Wire (Cat) Chemical Vapour Deposition Conference, 3rd – 6th September 2018, Kitakyushu, Japan.

4. **Effect of deposition temperature on the propagation loss of polysilicon waveguides using hot-wire CVD**

   Taha Ben Masaud, Antulio Tarazona, **Rafidah Petra**, Goran Z. Mashanovich, Graham T. Reed, Harold M. H. Chong,

   Conference on Lasers and Electro-Optics 2015, 21st – 25th June 2015, Munich, Germany.

5. **Broadband 2D diamond grating couplers with variable pitch**

   Taha Ben Masaud, Antulio Tarazona, **Rafidah Petra**, Ali Z. Khokhar, Graham T. Reed, Harold M. H. Chong,

   IEEE 6th International Conference on Photonics (ICP) 2016, 14th – 16th March 2016, Kuching, Malaysia.

6. **Low-loss silicon rectangular waveguides fabricated by anisotropic wet etching for roughness reduction**

   Hideo Arimoto, Muhammad K Husain, Alyssa Prasmusinto, Kapil Debnath, Abdel Rahman Al-Attili, **Rafidah Petra**, Harold MH Chong, Graham T Reed, Shinichi Saito,

   IEEE 12th International Conference on Group IV Photonics (GFP) 2015, 26th – 28th August 2015, Vancouver, British Columbia, Canada.

Patent

1. **Waveguide for an Integrated Photonic Device**

   Harold M. H. Chong, **Rafidah Petra**, Swe Zin Oo, Antulio Tarazona, Graham T. Reed. “Waveguide for an integrated photonic device”.

   U. S. Patent 15/999071, Aug. 17, 2018.

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Especially Dedicated To My Three Wonderful Daughters

AK NA MF

Self-Reminder **|** *The 8 Key Elements to Success – Guided by HMHC & Adapted from David J. Schwartz Motivational Book:*

1. *Aims*
2. *Believe*
3. *Knowledge*
4. *Opportunity*
5. *Effort*
6. *Experiment*
7. *Perseverance*
8. *Luck*

Definitions and Abbreviations

Three-dimensional	3D
Aluminium	Al
Ammonia	NH_3
Ammonium fluoride	NH_4F
Amorphous silicon	aSi
Argon	Ar
Atomic force microscopy	AFM
Automated teller machines	ATM
Average roughness	R_a
Back-end-of-line	BEOL
Buffered hydrofluoric acid	NH_4:HF
Buried oxide	BOX
Capacitance	C
Catalytic chemical vapour deposition	cat-CVD
Chemical mechanical polishing	CMP
Chemical vapour deposition	CVD
Complementary metal-oxide-semiconductor	CMOS
Copper	Cu
Crystalline silicon	c-Si
Design of experiment	DOE
Electromagnetic	EM
Electron beam	e-beam
Electronic integrated circuits	EICs
Fibre-to-the-home	FTTH
Finite-difference time-domain	FDTD
Fluorosilicate glass	SiOF
Fundamental mode of transverse electric	TE_0
Gallium arsenide	GaAs
Germanium	Ge
Hafnium oxide	HfO_2
Hot-wire chemical vapour deposition	HWCVD
Hydrofluoric ions	HF^{2-}
Hydrogen	H_2
Hydrogenated amorphous silicon	a-Si:H

Indium phosphide	InP
Inductively coupled plasma	ICP
Integrated circuits	ICs
International Technology Roadmap for Semiconductors	ITRS
Isopropyl alcohol	IPA
Lithium niobate	$LiNbO_3$
Low pressure chemical vapour deposition	LPCVD
Mean squared error	MSE
Metal oxide semiconductor field-effect transistor	MOSFET
Metal-oxide-semiconductor	MOS
Microprocessor unit	MPU
Mode field diameter	MFD
N-Methyl-2-pyrrolidone	NMP
Oxide ions	O^{2-}
Photonic application suite	PAS
Photonic integrated circuits	PICs
Plasma-enhance chemical vapour depostion	PECVD
Polycrystalline silicon	Polysilicon
Radio frequency	RF
Radio frequency	RF
Reactive ion etching	RIE
Resistance	R
RMS surface roughness	R_q
Root mean square	RMS
Scanning electron microscope	SEM
Silane	SiH_4
Silicon	Si
Silicon dioxide	SiO_2
Silicon nitride	Si_3N_4
Silicon photonics	SiP
Silicon-on-insulator	SOI
Silyl	SiH_3
Southampton Nanofabrication Centre	SNC
Sulfur hexafluoride	SF_6
Tantalum	Ta
Temperature of filaments	T_f
Temperature of substrate	T_s
Tetragonal silicate	SiO_4

Tetrathyl orthosilicate	TEOS
Transverse electric	TE
Transverse electromagnetic	TEM
Transverse magnetic	TM
Transverse optical	TO
Trifluoromethane	CHF_3
Tungsten	W
Very large scale integration	VLSI
Water	H_2O
Wavelength division multiplexers	WDM

Nomenclature

Angle of incidence	θ_i
Angle of refraction	θ_t
Bandgap energy	E_g
Bend mode	φ_b
Conductivity	σ
Confinement factor	Γ
Coupling coefficient	κ
Critical angle	θ_c
Decay constant of the cladding in the x-direction	k_{xc}
Effective index of a mode	N or n_{eff}
Effective propagation constant of a confined mode	β
Electric field	E_x
Electric field at the lower cladding	E_l
Electric field at the upper cladding	E_u
Electric field in the core	E_c
Full energy transfer	L_π
High index	n_2
Low index	n_1
Number of modes	m
Order of mode	m^{th}
Overlap integral	Γ
Phase shift	ϕ
Phase shift at lower boundary	ϕ_l
Phase shift at upper boundary	ϕ_u
Propagation constant at the lower cladding	k_{yl}
Propagation constant at the upper cladding	k_{yu}
Propagation constant in free space	k_o
Propagation constant in the core	k_{yc}
Propagation constant in y-direction	k_y
Propagation constant in z-direction	k_z
Propagation constant of the core in the x-direction	k_{xg}
Resistivity	ρ
Thickness of core layer	h
Total phase shift	ϕ_t

Waveguide separation	s
Width of waveguide	w
Working wavelength	λ_o

Chapter 1 Introduction and Motivation

1.1 Introduction

In the past decade, silicon photonics (SiP) has been identified as a potential platform to revolutionise various areas of technology. These areas include telecommunications, high performance computing, security and sensing [1, 2]. The reason behind the growth of SiP lies in the advantages that crystalline silicon-on-insulator (SOI) offers. This includes the realization of small waveguide devices, due to the high refractive index difference (Δn) compared to its native oxide, silicon dioxide (SiO_2), with Δn = ~2.4 (Si/SiO_2=3.45/1.45), which produces strong optical confinement. This results in high integration of photonic components, which is important for compact IC design [3, 4]. In addition, the making of SOI photonic devices benefits from the matured fabrication of complementary metal-oxide-semiconductor (CMOS) electronics, which, reduces the cost of developing new fabrication methods [1].

However, the development of SiP platforms is restricted to being planar. This results in SiP integrated circuits (ICs) having a large footprint, compared to electronic ICs (EICs) [1]. The reason is that EICs use multilayer stack and interconnects, which SiP currently lacks. This is mainly due to the restriction of growing c-Si film on multiple layers [5, 6].

As SiP ICs mature, the demand for greater functionality on a chip increases. Effectively, this requires higher circuit density, which can be realized through different methods – including miniaturizing photonic components and multilayer configuration [7]. Stacking the photonics components on a single chip strongly increases the circuit's footprint efficiently, with the use of additional degrees of freedom. Therefore, three-dimensional (3D) optical waveguide interconnects are necessary, and this topic has simulated recent research interest in 3D photonics.

1.2 Silicon Photonics

The use of crystalline silicon (c-Si) waveguides could revolutionise the semiconductor IC industries by implementing the significant advances made within SiP. As reported by Zilkie at Rockley Photonics Inc. [7], SiP technology has succeeded in producing devices for a wide range of applications. However, despite the ongoing success of silicon photonics, it remains an emerging technology with significant potential. If the technology is to be used at processor level, several hurdles must be overcome, especially in circuit density. If this challenges are not addressed in the near future they could become a serious concern, especially with the increasing demand for higher bandwidth.

The main problem with SiP is its large circuit footprint to accommodate large numbers of optical devices and the space reserved for fibre-to-photonic integrated circuit (PIC) coupling [7-9]. Currently, active optical devices such as – electro-optic switches and modulators – use structures like a Mach Zehnder Interferometer (MZI) and micro-ring resonators, which tend to have large device dimensions [7, 8]. Packing many of these discrete optical components into a single IC chip would result in the optical components and interconnect circuitry being placed in too close proximity to each other. Ultimately, this would cause crosstalk and significant signal degradation, thus, creating a serious problem and hindering SiP's potential as a disruptive technology. In addition, the current size PICs is large enough to limit their potential for integration onto a high-performance CMOS wafer [9]. Thus, the need to reduce the SiP circuit footprint containing high density optical components is increasing.

1.3 Multilayer Silicon Photonics Architecture

One possible solution is to extend the PIC architecture to 3D. 3D multi-layered configurations permit an additional degree of freedom. This enables more active and passive optical components to fit within a given area, increasing PIC density. The main increase in circuit density derives the ability to provide a separate transport layer; in addition, waveguides can be crossed, permitting greater utilization of silicon real estate [10-12]. Subsequently, high density integration through the use of an additional degree of freedom has the potential to increase the market share of SiP in the near future. There are many application areas, especially data centres, high-performance computing and fibre-to-the-home (FTTH) telecommunication [7].

When realizing 3D multilayer architecture, interconnect circuitry between layers plays a main role. The 3D interconnect must have a compact design, preferably exploiting a high index waveguide material with small, short waveguide dimensions; these features are efficient in real estate and insertion loss. Achieving this design remains a challenge due to the limitation of c-Si when used as a 3D vertical interconnect. This is due to the complexity in the film growth through a bottom –up approach requiring deposition temperature as high as 1400^{o}C. The extremely high temperature defeats the thermal budget required by back-end-of-line (BEOL) CMOS fabrication line. In addition, the growth from silicon crystals restrict the flexibility of multilayer stacking [5, 6, 13, 14]

1.4 The Interlayer Slope Waveguide Coupler

In this work, an interlayer slope waveguide coupler is proposed. The device is designed to directly couple light up or down within a multilayer SiP platform. The interlayer coupler is fabricated from hydrogenated amorphous silicon (a-Si:H) film, deposited at low temperature using a hot-wire chemical vapour deposition (HWCVD) tool [15]. The use of a-Si:H film is promising because of its compatibility with CMOS processes, enabling device fabrication on electronic circuit layers. In

addition, the material has good optical properties similar to c-Si [16]. The material is known to have low absorption loss that can be achieved at low deposition temperature below 300°C [17]. It has an energy bandgap equals to ~1.7 eV [16], which allows near infra-red photons with ~0.79 eV (hv) to be transmitted with minimum interferences. In addition, the high refractive index of the material results in strong optical confinement within the waveguide core facilitating ultra-compact interconnect devices.

As part as the research on the interlayer slope waveguide, crosstalk experiments were performed to investigate the minimum isolation cladding thickness required to isolate two waveguides, placed orthogonally on top of each other. This experiment demonstrated the capacity of the interlayer slope waveguide to function as a proper multi-layer interconnect.

1.5 Research Objectives

The development of SiP technology is growing steadily and the need for multilayer functionality is increasing [5]. This project was aimed at developing an interlayer coupler that was capable of transporting and distributing optical signals from one level to another in the SiP platform. The proposed interlayer 3D interconnect circuitry platform is illustrated in Figure 1.1.

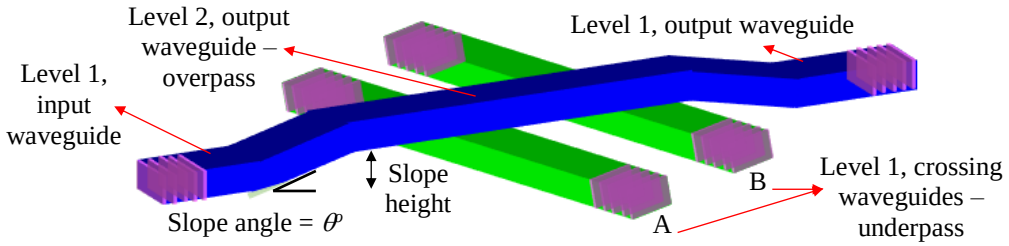


Figure 1.1 Schematic diagram of the proposed interlayer 3D interconnect circuitry platform featuring the interlayer slope waveguide coupler.

Given this arrangement, optical components – such as lasers, modulators, photodetectors and wavelength division multiplexers (WDM) – can be placed on several levels, without space restrictions.

The objectives of the work were as follows:

1) Develop a high-quality a-Si:H film deposited within thermal budget requirements for CMOS technology. This work was conducted in collaboration with Dr Swe Zin Oo and Dr Antulio Tarazona.
2) Explore, by simulation, the optimum slope angle for the proposed interlayer slope waveguide, with respect to the slope height, while providing optimized transmission.
3) Develop a fabrication process for producing a slope platform through etching of deposited PECVD silicon dioxide.
4) Fabricate and measure interlayer slope waveguide transmission, and characterize the device in terms of loss in dB per slope.

5) Demonstrate the capacity of the proposed interlayer slope waveguide coupler either to isolate optical light from any crossing waveguides or to couple optical light into neighbouring waveguides.
6) Fabricate the interlayer slope waveguides and demonstrate a real 3D vertical optical interconnect for multilayer platforms.

1.6 Thesis Structure

The thesis is organized as follows. Chapter 2 presents a detailed literature review that initially describes the journey of silicon photonics (SiP) technology. This is followed by a discussion on the properties of a-Si:H film and the differences between HWCVD and PECVD tools. Thereafter, the different methods for coupling light vertically in a 3D multilayer SiP platform are discussed. Chapter 3 describes the background and theory of the fundamental operation of an optical waveguide, waveguide bends and interlayer slope waveguides. Loss mechanisms in an optical waveguide are also discussed briefly. Chapter 4 presents the simulation model for the interlayer slope waveguide, followed by the modelling of crosstalk between waveguides. Chapter 5 comprehensively discusses the process development for fabrication and presents the characterization method for the interlayer slope waveguide; discussion of the results and measurements is included. Chapter 6 presents the fabrication and characterization of the crosstalk experiment, and describes the development and characterization of a demonstrator device based on the interlayer slope waveguide structure. Finally, Chapter 7 summarizes the use of the interlayer slope waveguide fabricated from HWCVD a-Si:H, and offers conclusions regarding future implementation for a multilayer SiP platform.

Chapter 2 Literature Review

2.1 Scaling Technology in the Semiconductor Industry

During the last five decades, scaling technology has positively influenced the performance of microprocessors [18]. Figure 2.1 illustrates the trend in increasing processor clock speeds (MHz) by year, with the number of transistors per microprocessor-chip doubling every two years [19]. The basis for this advancement is Moore's Law combined with Dennard's scaling, as observed and formulated by Gordon E. Moore and Robert H. Dennard and introduced in 1965 and 1974 respectively [18-21]. Through scaling, the physical properties of miniaturized transistors allow electrons to move faster in smaller circuits, resulting in faster transistor switching.

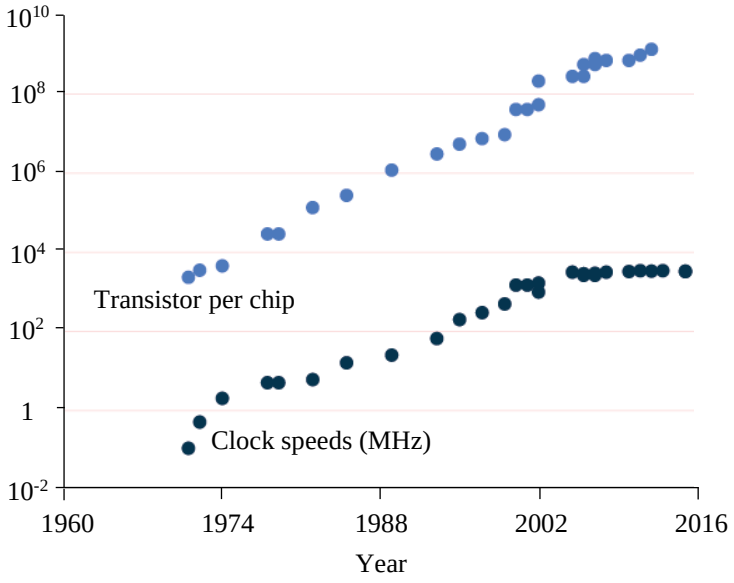


Figure 2.1 Increase in number of transistors per microprocessor-chip by year: processor power doubled roughly every two years, over five decades (reproduced from [19]).

During the 1970s, microprocessors operated at a clock speed of hundreds of kHz, which at that time meant they were able to run minicomputers, as shown in Figure 2.2. From the 1980s to the late 1990s, the performance of microprocessors accelerated rapidly. Transistors became even smaller, allowing the clock speed to run at hundreds of MHz. This capacity led to the commercial production of devices such as multi-functional handheld calculators, personal computers and laptop [18, 19]. However, during the mid-2000s, the performance of microprocessors plateaued with the breakdown of Dennard's scaling.

The 2000s was the period when the technology node reached below 100 nm, and transistor dimensions became so small that the fast-moving electrons turned into leakage current. This problem later become significant problem as power was mostly dissipated, causing devices to heat up too easily.

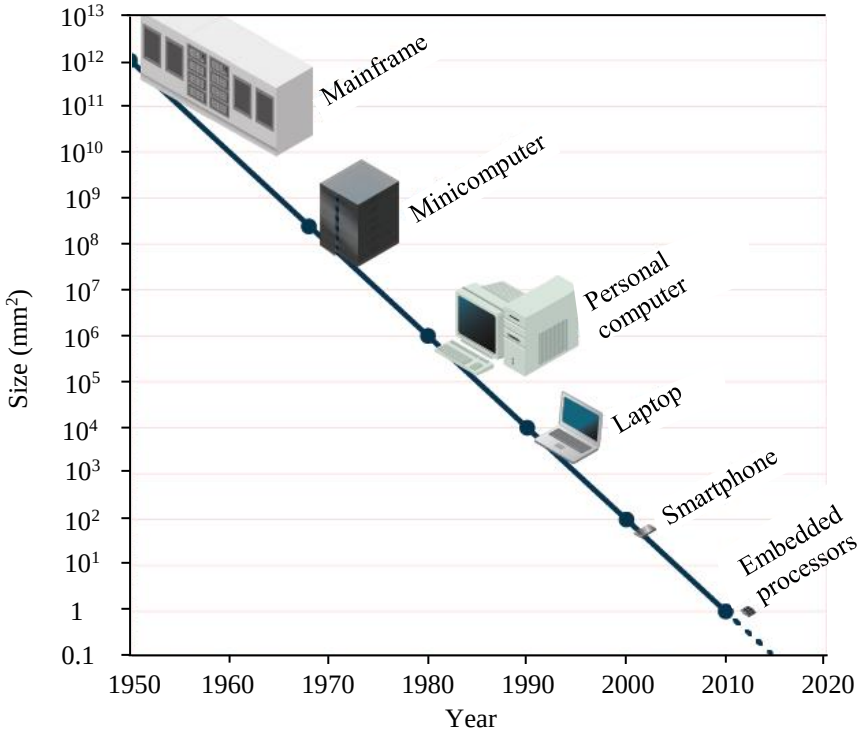


Figure 2.2 Increase in the power of computers with decreasing microprocessor sizes – resulting in the emergence of a new class of machines roughly every ten years (reproduced from [19]).

The power leakage was mainly caused by the effect of quantum mechanical tunnelling, due to the fast-moving electrons leaking into the thin gate oxide channel [19-22]. To counteract this issue, the clock speed of microprocessors remained stagnant for years as producers tried to limit the heat generation, as shown in Figure 2.1 [19].

Over time, researchers and industries have tackled the problem of electron leakage. Initially, they introduced strained silicon technology to replace germanium (Ge) as the source and drain material of the metal oxide semiconductor field-effect transistor (MOSFET) [23, 24]. This revolutionary approach was followed by the use of high-k material such as hafnium oxide (HfO_2), to replace silicon dioxide (SiO_2) as the gate oxide material [25, 26]. Later, the internal circuitry of microprocessors was redesigned so that each chip contained more than one microprocessor, through multiple processor core architecture [19]. In yet another breakthrough, vertical transistors were developed. This meant that many transistors could be packed onto a single chip, which ultimately made computers perform faster [27-29]. The state-of-the art 14-nm technology node produced by Intel, based on the vertical transistor structure, can accommodate up to 1.3 billion transistors per chip. It has been demonstrated that this technology performs 50% faster than the previous 22-nm technology node, operating at a low supply voltage [30].

The use of all the listed technologies have led to increased performance in microprocessors, in terms of reduced power leakage of the MOS devices [27-30]. Subsequently, this has led to the progressive development of supercomputers and sophisticated mobile devices such as smartphones and tablets. However, as the scaling of transistors successfully continues into the nanometre era, interconnects

have become a serious hindrance. The following section provides details on the dilemma faced by the interconnect circuitry as billions of transistors are packed into a single silicon chip.

2.2 Migration Phases of Interconnect Circuitry

Interconnect circuitry is as important as transistors in allowing continued improvements of circuit performance. Interconnects are a key element in integrated circuits, which are used to route and distribute data signals. Whereas transistors benefit from the scaling trend, interconnects degrade as the dimensions are scaled down. Essentially, packing more transistors into a chip through scaling down the transistor's dimensions improves the chip's performance. However, this results in interconnects being tightly placed next to each other, with the wires (interconnects) becoming densely packed. Trade-off in the design of interconnect circuitry cannot be compromised. Reducing the cross-sectional area of the individual wire to allow sufficient separation to the neighbouring wire, to avoid crosstalk, results in increased resistance (R). However, enlarging the cross-sectional area of the wire and maintaining proximity to the neighbouring wire for high density results in the occurrence of parasitic capacitance (C). Either way, signal propagation delay occurs, which affects the circuit's reliability [31]. In the earliest generation of transistor technology, aluminium (Al) was commonly used as the on-chip interconnect metal [31]. In the 1990s, transistor feature sizes started to shrink to deep sub-micron level and new metal alternatives were explored to replace Al. At that time, the interconnect evolution started with the migration from Al to copper (Cu).

For several transistor technology generations, interconnect circuitry benefited from the high conductivity (σ) of Cu. Wires could be made thinner, due to low film resistivity (ρ), than was possible to Al, and this alleviated signal delays. In addition, Cu has a higher melting point than Al, which means it is more resistant to electro-migration. These properties allow for further circuit miniaturization. However, the performance of Cu interconnect circuitry did not last long. As soon as the technology node started to reach 100 nm, with processors operating at a clock speeds of giga-hertz (GHz), the benefits of miniaturization failed. At such high clock frequency, Cu interconnect performance is limited due to the severity of the skin effect, where the skin depth of the wire becomes so thin that current distribution is higher at the surface of the conductor than at the centre. As a result, the resistance of the wire increases, increasing signal delays and dissipating power. This interconnect dilemma, which started around the same time as the downfall of Dennard scaling, became a serious issue in the microelectronic integrated circuits (ICs) industry at that time [19, 31].

Soon afterwards, researchers and industries found another solution to tackle the interconnect dilemma. The use of low-k dielectric material, offering much lower interconnect parasitic capacitance, was explored. This technology was introduced to address the issue of interconnect bottlenecks. Low-k dielectric materials such as fluorosilicate glass (SiOF) have been widely used and are commonly combined with copper metal layers for the fabrication of ICs. Figure 2.3 shows

the cross-sectional scanning electron microscope (SEM) images of microprocessor unit (MPU) interconnects for various technology nodes, as follows: (a) 90 nm [32], (b) 22 nm [30], and (c) 14 nm [30]. The 7, 9 and 11 interconnect layers, respectively, are stacked. Because of the revolution in interconnect technology, current modern microprocessors feature as many as 12 to 14 layers of hybrid interconnects, allowing room for highly packed chips and providing improved circuit's performance [18].

With technology pushing for ever smaller feature size, both Cu and the low-k dielectric interconnect remain unable to fulfil the requirement for robust high-speed interconnects. The issues of increased signal delay, power dissipation, bandwidth limitation and the occurrence of cross-talk signals are challenges that must yet be overcome.

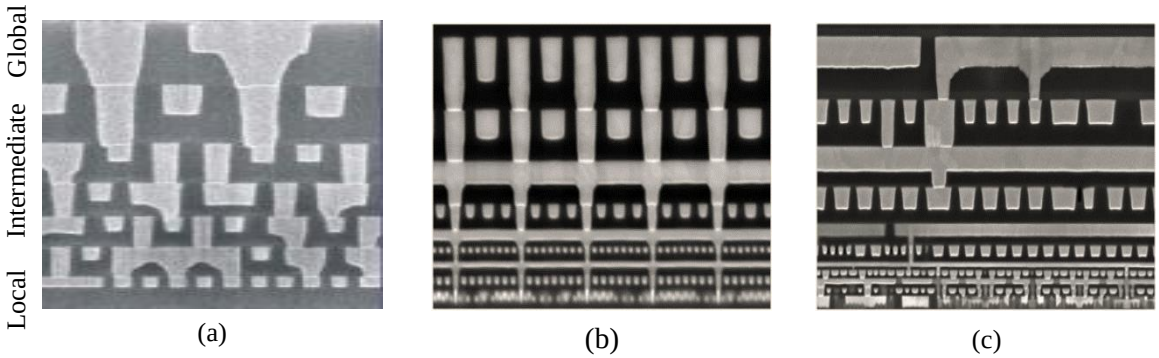


Figure 2.3 Cross-sectional SEM image of Intel technology nodes: (a) 90 nm (reproduced from [32]), (b) 22 nm (reproduced from [30]), and (c) 14 nm (reproduced from [30]).

According to the International Technology Roadmap for Semiconductors (ITRS) [33], the microelectronic semiconductor industry has identified several options to alleviate the interconnect issue. These include the use of carbon nanotubes, graphene nanoribbons and optical interconnects. Among these options, optical interconnect has the potential to replace Cu and low-k dielectric interconnects due to its capacity to carry a large bandwidth at the speed of light, with minimal crosstalk between signal transmission paths. In addition, a single optical interconnect can accommodate multiple wavelengths, thus increasing the capacity to carry multiplied data – which is not achievable by electrical means [33]. Furthermore, optical interconnects can be manufactured in a simple and cost-effective way. Most importantly, they are compatible with complementary metal-oxide-semiconductor (CMOS) fabrication processes.

The following section further discusses the benefits and challenges faced by optical interconnects used in the microelectronics industry.

2.3 Optical Interconnect – Advantages and Challenges

The use of optics to transmit data signals from one place to another through optical fibre, started in the 1970s [34]. Since then, optical fibre has revolutionized the telecommunication industry, with success on a large scale. Initially, optical fibre was used to transmit telephone signals and cable

television signals and to provide links for Internet protocols and in automated teller machines (ATMs). The fibre lengths ran to many kilometres. A decade later, in the1990s, optical fibre was advanced into ethernet cables, which were mainly used in data centres and had lengths from 10 m to 300 m. Soon after, optical fibre advances further for the inter- (off) and intra- (on) chip integrated circuits applications with shorter lengths regime [35].

The use of optical interconnect to replace electrical wires, either off-chip or on-chip, arose from several of its benefits [36]:

1) Optical wire is free from capacitive loading effects; technically, this means it does not suffer from resistance (R) and capacitance (C) propagation delays. This is because optical signals travel at the speed of light.
2) Optical interconnect is immune from electromagnetic interference effects, due to the absence of electrons associated with the propagating medium. In electrical interconnect, cross-coupling of information (crosstalk) is a serious issue because stray capacitance occurs through the close proximity of electrical pathways.
3) Optical interconnect benefits from highly compact integrated routing, where waveguides can pass through other crossing waveguides without significant cross-coupling. The only condition is that the angle of intersection must be larger than 10^{o}.
4) Optical signals can be directly transmitted into electronic logic devices, through optical-to-electronic pulse conversion. This can greatly simplify circuit integration.
5) Optical interconnect is compatible with silicon CMOS processes. This is one of many reasons why the optical interconnect based on c-Si has been a favourite material to work with.

For optical interconnect to fully replace electrical interconnect, however, there are certain challenges which need to be overcome. Integrating optical interconnect with active optical components, poses a number of complications. The major limitations lies in the production and integration cost of optical components with existing CMOS circuits, in terms of size and power consumption of the optical components such as the optical source, the electro-optic modulator and the photodetector [37].

Conventional active optical devices are dominated by compound semiconductor materials, for example gallium arsenide (GaAs), indium phosphide (InP) and lithium niobate ($LiNbO_3$) [37, 38]. Active optical components which are fabricated from these ‘exotic’ materials have demonstrated exceptional performance when heterogeneously integrated on a silicon-on-insulator (SOI) platform. It has been shown that optical devices such as photodetector, modulator and in particular laser can be well waveguide coupled and routed to the rest of the photonics integrated circuit (PIC) with very low loss [39, 40]. However, the device structure can be relatively large that it significantly increases the circuit footprint. They also suffer from high cost by which these properties relate to complex processing, low yield and complexity to integrate. Thus, common material platform for both electronics and optics is necessary to reduce the production cost and to increase the feasibility of opto-electronic integration.

In terms of power consumption, the power in an optical interconnect is mostly consumed by the active optical components, such as optical source, modulator and photodetector. For optical waveguides to be able to replace electrical interconnects for short distance communication, the energy consumption of optical devices has to be very low [37] .

For optical interconnect to efficiently replace electrical interconnect, active components (such as the optical source, modulator and photodetector) must display minimal power dissipation. According to the ITRS projections for 2022 for inter-chip integration, overall system energy consumption should be less than 1 pJ/bit, with individual components not using more than 20fJ/bit. At intra-chip level, the energy limit for the whole system is fixed at 200 fJ/bit, with individual device energy requirements not exceeding 10 fJ/bit [37]. Only once these power consumption issues are solved will the use of silicon optical interconnect in very large scale integration (VLSI) electronic chips reach its full potential.

The challenges imposed by the optical interconnect circuitry was the driving force behind the emergence of silicon photonics (SiP). Through SiP, monolithic opto-electronic integration based on CMOS infrastructure became viable in terms of established processes and materials, at reasonable production costs with high yield. The following section briefly describes the evolution of SiP designed to specifically for semiconductor communication technology. Through SiP, it is anticipated that the interconnect bottleneck in microprocessors can be alleviated so that enormous quantities of data can be delivered at high speed.

2.4 Silicon Photonics

The beginning of SiP can be dated back to 1986, with the demonstration of planar and channel waveguides fabricated from c-Si film, by Soref and Lorenzo [41]. Since then, the technology has prospered, with explosive growth demonstrating the rapid development of optical components, ranging from passive interconnect devices to light sources, optical modulators, photodetectors and light amplifiers. The main advantage of using c-Si in photonic technology is the abundance and availability of high-quality silicon-on-insulator (SOI) wafers; these have the lowest cost per unit area, containing the highest crystal quality, among all semiconductor materials. In addition, the photonic SOI platform fabrication framework is compatible with CMOS technology, leading to a cost-effective, high-yield and replicable process. Another attraction of c-Si is its advantageous optical properties around the telecommunication wavelength, which provide an excellent property for building planar waveguide circuits. The material has a large energy bandgap of ~1.12 eV [3], allowing it to be transparent in the near- and mid-infrared spectrum. In addition, its high index contrast with silicon dioxide (n Si/SiO_2=3.45/1.45) facilitates the building of miniaturized curved waveguide devices, which is fundamental to IC processing [42]. However, c-Si is a poor light-emitting material due to its indirect bandgap. Hence, the charge carrier electron needs a change in

energy and momentum to emit a photon. Researchers have explored potential ways to modify the c-Si structure so that it emits optical light [43].

The consensus about the benefits of SiP is its compatibility with established and mature CMOS processes. Thus, SiP is viewed as having sound potential when integrated with established high-speed electronics. According to Reeds *et al*. [43], there are two ways in which SiP provides benefits. First, it works with SiP devices to overcome the weakness of c-Si to serve as light emitting devices, such as in lasing and photo-detection. Eventually, this should mean that the vision of monolithic integration can be achieved. Second, exploration to create light-emitting devices by combining c-Si with other III-V materials can open up the possibility of integrating them with existing electronics, to achieve hybrid opto-electronic circuit integration.

In early documentation of the progress of SiP, Soref [44] reported in 2006 that a monolithically integrated opto-electronics chip had been built and demonstrated by a CMOS photonics technology foundry, Luxtera. The chip contained up to 100 photonic components and around 200 000 transistors. Luxtera had developed a 10 Gb/s fibre-optic transceiver opto-electronic circuit that contained a silicon 10 Gb/s modulator, a flip-chip bonded III-V laser, a high speed germanium (Ge)-on-silicon photodiode, and a highly efficient waveguide to couple into the fibre. In the same report, Soref referred to Kimerling's vision on converging optics and electronics. Kimerling (from MIT) had partnered with BAE Systems to demonstrate a prototype employing vertically stacked photonic circuits on top of a CMOS platform, for unique opto-electronic integration. The advantage of this approach was the achievement of dense 3D integration of photonic components on a small footprint chip. Luxtera and Kimerling's approaches are practical for preserving the transistors beneath the photonics. This is because an overall fabrication thermal budget not exceeding 450^{o}C is a main requirement in opto-electronic circuit integration. It ensures that fabrication processes do not harm the active components in the CMOS layer or in the previously deposited metal layers, if any.

The development of SiP prospered further over time. In 2016, the renowned chip maker Intel [45] announced the volume production of its optical transceiver module, which was based on fully integrated silicon-based optical and electrical components. These are fabricated on the same chip using standard CMOS-compatible technology. The module delivers bandwidths as high as 100 Gb/s over 2-km cable links, with low power consumption. This module is designed to be used in data communications, especially in data centres and high-performance computing applications.

2.5 Multilayer Silicon Photonics

SOI has been used as a universal platform for developing SiP technology. This is mainly due to its compatibility with CMOS fabrication processes and its excellent waveguiding optical properties. However, the current development of SiP is restricted to being planar, which limits how many additional layers of optical components can be added to the integrated chip.

In general, 3D SiP is advantageous as it offers a dense footprint with an area so large that integrating optical components per chip can be limitless. Through this circuit configuration, computational systems having new functionality and higher optical data-processing capacity are expected to meet the growing demand for bandwidth in silicon electronics technology [17, 46-48]. However, the element that hinders SiP from moving forward to 3D circuit development is the complex fabrication of c-Si. Despite demonstrating excellent optical properties, c-Si has major weakness. It can only be fabricated by a bottom-up approach that requires the growth of silicon crystals under extreme temperatures of up to 1400^{o}C [6, 13, 14]. The high processing temperature defeats the thermal budget required by back-end-of-line (BEOL) CMOS fabrication technology. It is also impossible for c-Si to be deposited on stacking layers for the multilayer circuit platform. Thus, depositable materials that have similar properties to those of c-Si are required.

In the next section, materials that could potentially be used as 3D vertical optical interconnects are discussed.

2.5.1 Optical Waveguide Materials for Multilayer Architecture

Crystalline silicon (c-Si) has been a popular material platform for making waveguide devices. Transmission loss of less than 1dB/cm has been reported for nanometre-scale c-Si waveguides [41, 49-52]. Although known for its remarkable optical properties, c-Si is known to be unsuitable for multilayer circuitry due its complex growth process. Standard manufacturing procedures to grow c-Si film require seeding the single-crystalline silicon under high processing temperatures (up to 1400^{o}C) [6, 14]. Hence, materials that are depositable under low temperatures and have similar characteristics to c-Si are needed. To address this issue, various silicon-based materials – such as polycrystalline silicon (polysilicon), silicon nitride (Si_3N_4) and amorphous silicon (a-Si) – have been widely studied to investigate their suitability for 3D waveguide coupling devices [13, 53, 54].

Polysilicon has been an important material in the electronics industry. Its first widespread application as a material for the gate-electrode occurred in metal-oxide-semiconductor (MOS) technology [55]. Polysilicon is commonly obtained by chemical vapour deposition (CVD) methods. The film has large bandgaps viable for near infra-red transmission, and possesses a high refractive index with *n* equal to 3.5 at 1550 nm, similar to c-Si [56]. In its natural form, polysilicon film comprises randomly-sized crystalline grains, ranging from tens to hundreds of nanometres (nm). This feature significantly affects the optical properties of the material and is controllable, depending on the deposition parameters [57]. In most applications, post-processing the film with high-temperature treatment is necessary to improve the inhomogeneous crystallinity of the film. Under high-temperature treatment (up to 1100^{o}C) to recrystallize the film, propagation loss – which is otherwise as high as 13.4 dB/cm – can be reduced to 6.5 dB/cm. This point was reported by both Selvaraja *et al*. [58] and Fang *et al*. [59]. However, the high-temperature post-processing step is considered too high for BEOL CMOS

applications. Therefore, unless an alternative way to improve the film properties is found, polysilicon has limited potential for use as 3D optical vias.

The substance Si_3N_4 can be deposited through CVD methods under low deposition temperatures. This has been demonstrated as a prospective material for the multilayer platform [54]. It is known as a low-loss material, with a reported waveguide propagation loss of less than 1.5 dB/cm [60-64]. However, its low index contrasts with silicon dioxide ($\Delta n \cong 0.85$) make device footprints larger. Nonetheless, large waveguide dimensions can be advantageous for coupling in light from a fibre.

Among these silicon-based materials, a-Si has been shown to be a promising candidate for interconnect circuitry in the multilayer SiP platform. The deposition of the material is compatible with BEOL CMOS, enabling device fabrication on the electronic circuit layers. The material exhibits low absorption loss, with an energy bandgap of ~1.7 eV [16]. This property benefits the material by making it largely transparent at the near-infra-red spectrum, allowing photons with ~0.79 eV (hv) energy to be transmitted with minimum interferences. In addition, the high refractive index of the material results in strong optical confinement within the waveguide core facilitating ultra-compact interconnect devices. The disadvantage of using a-Si is the need to maintain the material's stability through sufficient hydrogenation to passivate the dangling bonds [5]. Therefore, in processes such as plasma-enhanced chemical vapour deposition (PECVD) and hot-wire chemical vapour deposition (HWCVD), silane (SiH_4) gas is used as a precursor gas to produce hydrogen radicals through pyrolysis reaction. The radicals then bond with the unpaired covalent bonds of the silicon atoms [65]. This results in passivation of the film, forming hydrogenated amorphous silicon (a-Si:H).

To date, several research groups – including Selvaraja *et al*. [5], Zhu *et al*. [66], Furuya *et al*. [67] and Takei *et al*. [68] – have reported on their work with high-quality PECVD a-Si:H film. These researchers have demonstrated sub-micron waveguide structures with propagation losses between 0.6 dB/cm and 3.45 dB/cm, which is fundamental for the realization of 3D interconnect [42].

In such work, an HWCVD tool is used to deposit the a-Si:H film. This choice is mainly because of the effective dissociation of the precursor gas, namely silane (SiH_4), into atomic silicon (Si) and hydrogen (H_2) molecules. The hot filaments cause this dissociation, which reduces film stress due to the absence of plasma ion bombardment [69]. Thus, high-quality HWCVD a-Si:H thin film becomes attainable at low temperatures (below 400^{o}C) for BEOL process compatibility.

In a separate project, our group demonstrated low-loss a-Si:H waveguide deposited by the HWCVD system. The work was based on a design of experiments with varying temperature, ranging from 190^{o}C to 320^{o}C. Propagation loss equal to 0.8 dB/cm was obtained for waveguide dimensions of 650 nm (w) by 400 nm (h). These reported losses were fabricated from 230^{o}C substrate temperatures with an SiH_4 and hydrogen gas (H_2) mix ratio of 2.4:1. The pressure was set to a fixed value, equal to 0.01 mBar (7.5 mTorr). Raman measurement was conducted by Dr Swe Zin Oo, revealing a transverse optical (TO) peak at 481 cm^{-1}, suggesting a highly dense amorphous silicon bond network [15]. The

surface roughness of the film was measured using atomic force microscopy (AFM) and revealed a root mean square (RMS) roughness of 0.91 nm.

Table 2-1 shows a comparison of the propagation losses and deposition methods for the three materials, namely polysilicon, Si_3N_4 and a-Si:H. The next section briefly introduces the HWCVD and where it differs from PECVD, in terms of film growth.

2.5.2 Introduction to HWCVD System

The HWCVD system, also known as catalytic chemical vapour deposition (cat-CVD), is one of many types of CVD methods used to obtain amorphous silicon (a-Si) films and polycrystalline silicon films. Like any other CVD tool, the mechanism of HWCVD for growing a-Si film involves the dissociation of precursor gases such as SiH_4 to form elemental silicon (Si) and molecular hydrogen (H_2). In HWCVD, the decomposition of these atomic molecules occurs at the surface of the heated filament at significantly high temperatures (above 1500^{o}C). Materials commonly used for the filament wires are tantalum (Ta) and tungsten (W) as they have extremely high melting points. To obtain a good quality a-Si film, a balance is needed between high filament temperatures and the correct pressure applied to the system during the deposition process, to enable an adequate deposition rate with prominent amorphous features. Essentially, the pressure should represent a decrease of two orders of magnitude millibar (mbar), with typical pressure value of less than 0.02 mbar. The distance between the filaments and the substrate also plays an important role in maintaining the film deposition rate. Typically, the substrate is placed a few centimetres away above the hot filaments to avoid significant gas-phase polymerization [70]. Aggressive gas-phase polymerization is undesirable as it can lead to a fast rate of Si atoms reaching the surface of the substrate, which results in the film suffering from the formation of large concentration of voids and an obvious micro-crystallinity structure. As important as any other parameters, the quality of the filament wire strongly defines the characteristics of the grown amorphous Si film. The way filaments are mounted, the diameter of the filament wire, the material of the wires, and the preconditioning of filament wires with H_2 gas before the deposition process, all affect the performance of the filaments. They can contribute to a high-quality amorphous silicon film [71].

2.5.2.1 Differences between HWCVD and PECVD Film Growth

The HWCVD method has been well investigated and widely used by the solar-cells community to obtain a-Si:H and polysilicon films deposited at low temperature [71]. This project explored the use of the HWCVD system to produce device-quality a-Si:H film for photonic applications. The operation of the HWCVD system differs from the PECVD tool and has certain advantages and disadvantages, as follows:

Table 2-1 Reported propagation losses of polycrystalline silicon (polysilicon), silicon nitride (Si_3N_4) and amorphous silicon (a-Si) waveguides.

Author	Year	Material	Deposition method	Deposition temperature	Width (nm)	Height (nm)	Loss (dB/cm)	Wavelength (nm)
S. K. Selvaraja *et al.* [58]	2007	Polysilicon	LPCVD	560°C + Anneal at 850°C	500	220	13.4	1550
Q. Fang *et al.* [59]	2008	Polysilicon	LPCVD	550°C + Anneal at 575°C and further 1100°C	700	250	6.5	1520 - 1565
T. M. B. Masaud *el al.* [72]	2013	Polysilicon	HWCVD	350°C	600	220	13.5	1550
M. Melchiorri *et al.* [60]	2005	Si_3N_4	LPCVD	550°C - 600°C	1000	500	1.5	1550
M. Shaw *et al.* [61]	2005	Si_3N_4	LPCVD	Anneal at 1200°C	Not reported	Not reported	0.1	1550
A. Z. Subramanian *et al.* [62]	2013	Si_3N_4	PECVD	400°C	800	220	<1	900
Y. Huang *et al.* [63]	2015	Si_3N_4	LPCVD	Not reported	800	900	0.8	1550
T. D. Bucio *et al.* [64]	2016	Si_3N_4	PECVD	350°C	1000	300	1.5	1550
S. K. Selvaraja *et al.* [5]	2009	a-Si:H	PECVD	300°C	480	220	3.46	1550
S. Zhu *et al.* [66]	2010	a-Si	PECVD	400°C	500	200	3.2	1550
K. Furuya *et al.* [67]	2012	a-Si:H	PECVD	250°C	470	220	1.1	1550
R. Takei *et al.* [68]	2014	a-Si:H	PECVD	250°C	750	440	0.6	1550
S. Z. Oo *et al.* [15]	2018	a-Si:H	HWCVD	230°C	650	400	0.8	1550

1) In PECVD, film deposition is initiated by the use of plasma which is excited by high frequency power to dissociate the source gases, SiH_4, into reactive species. The collisions between electrons present in the plasma and SiH_4 gas result in the formation of positive (+) and negative (-) ions. The positive ions are given up to the cathode, by drifting out of the plasma, to preserve charge neutrality. This leaves the negative ions to become trapped in the plasma by sheath fields. The trapped (-) ions react rapidly with reactant ions present in the plasma, and accumulate, resulting in the generation of particles having a radius of 2 nm to 15 nm [71]. These particle traps greatly affect the quality of the film, as they can be deposited on the surface of the wafer [73]. By contrast, in HWCVD the risk of creating trapped negative charged ions is lower, due to the absence of plasma. Instead, in HWCVD, the dissociation of reactive species is induced effectively by hot filaments operating under a low pressure condition [71, 73, 74].
2) In HWCVD, precursor gas is dissociated in the absence of plasma or any applied high-voltage condition. This benefits the film deposition because no ion bombardment is experienced from high-energy ions. By contrast, in PECVD, reactive ions in the plasma acquire enough energy from the high radio frequency (RF) power (13.56 MHz) to cause substantial ion bombardment. Significant ion bombardment damages to the film that is being grown [71, 73, 74].
3) Obtaining a high deposition rate in PECVD is achievable but is not straightforward; trade-offs exist in adjusting any of the deposition parameters. For example, placing the substrate close to the metal showerhead can increase the deposition rate because the reactant radicals reach the surface substrate efficiently. However, placing the showerhead electrode very close to the substrate causes the high energy ions to repeatedly bombard the film layers, which results in film stress, causing the presence of voids. In addition, increasing the RF power to obtain a high deposition rate results in non-uniformity of the film over large areas [71]. By contrast, high deposition rates are achieved in HWCVD by increasing either the temperature of the filaments or the number of filaments used. Film uniformity over large areas is achievable and the odds of growing film experiencing high-energy ion bombardment are lower.
4) Unlike in PECVD, in the HWCVD process the coverage of the deposited film is more conformal as there is almost no electric field. Thus, complex structures having a high aspect ratio are attainable.

The drawbacks to the HWCVD system are as follows:

1) The heated filaments serve two functions. First, they dissociate the precursor gas being introduced into the chamber, and second, they provide radiative heating to the substrate. Thus the time required for the substrate temperature to become stable can be lengthy. Proper planning for performing the deposition work must be managed accordingly.

2) The temperature of the substrate is determined by the heat radiated by the filaments. The temperature of the filaments largely depends on their size and the number of filaments mounted on the filament holder. The Echerkon 301 HWCVD system at the Southampton Nanofabrication Centre (SNC) uses tungsten (W) filaments with three diameters. Table 2-2 shows the filament heating conditions and the resulting heat radiated to the substrate.

Table 2-2 Filaments and substrate temperature for Echerkon 301 HWCVD system at the Southampton Nanofabrication Centre (SNC).

Size of filaments (mm)	Number of filaments mounted	Temperature of filaments, T_f (ºC)	Temperature of substrate, T_s (ºC)
0.125	15	1850	190
0.178	15	1850	230
0.178	30	1850	320
0.2	30	2100	350

Varying the filament size and the number of filaments used results in different values of substrate temperature. This variation is advantageous, for instance when designing experiments with differing substrate temperatures for a broad analysis of temperature. However, it can be inconvenient to replace the filaments every time the temperature must be altered.

3) The lifetime of a filament depends on the filament material type, the temperature and the precursor gases. Materials such as tantalum (Ta) wire can withstand high temperatures but are prone to being oxidized. Certain precursor gases create silicides, which are readily deposited onto the wires. This makes the wires brittle and they break easily. Thus, a precondition step is important when performing a deposition processes, as described in Section B.1.1.1 of Appendix B. In addition, the filaments must be replaced regularly.

2.6 Interlayer Interconnect Devices for Multilayer Silicon Photonics Platform

As discussed earlier, the challenge in realizing multilayer technology lies in creating 3D vertical optical vias to connect the vertically stacked optical components, using depositable material that is suitable for CMOS processes. In light of this challenge, researchers have proposed various structures, with several groups reporting methods of vertical coupling. Takei *et al*. [17], Shang *et al*. [54] and Itoh *et al*. [75] utilized evanescent fields. Zhang *et al*. [76] and M. Sodagar *et al*. [77] utilized phase-matching conditions, all based on silicon (Si) thin films to couple light vertically. They reported coupling losses of 0.87 dB, 0.01 dB, 0.49 dB, 7.45 dB and 2 dB, respectively. Khan *et al*. [78] used vertical directional couplers fabricated from polymer-based material, and reported a coupling loss of 0.45 dB. Other interlayer coupling methods using polymer-based materials were demonstrated by Garner *et al*. [47] and Ni *et al*. [79] who used direct coupling through a vertical S-bend waveguide. Those studies demonstrated an excess loss of 0.3 dB and a propagation loss of 0.25 dB/cm. Table 2-

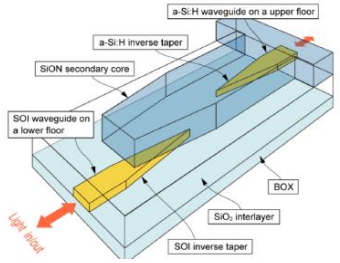
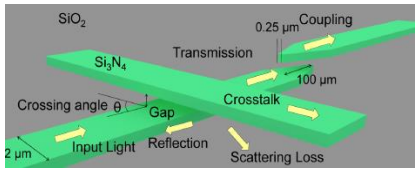
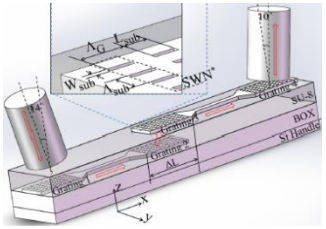
3 shows a summary of various structures of the reported vertical coupler. The reported 3D interconnect structures [17, 47, 54, 75-79] all demonstrated a vertical coupling capacity that is suitable for multilayer integration. However, problems related to these devices are such that the use of evanescent field and phase-matching conditions in taper-to-taper and grating-to-grating interlayer couplers may cause challenges in fabrication. High precision in fabrication alignment is required. Also, structures with large tolerances must be considered when making the 3D couplers.

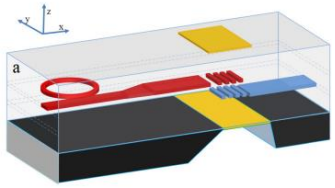
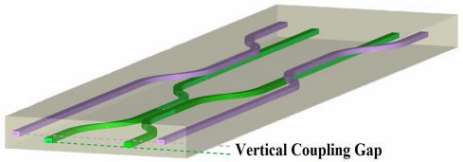
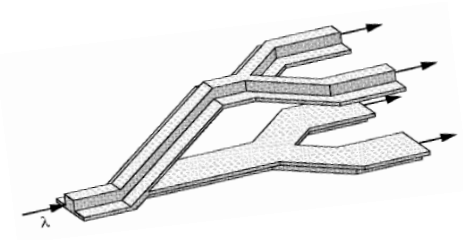
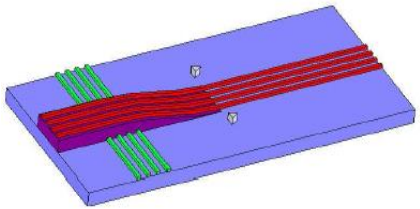
The low-index polymers in the S-bend waveguide require large waveguide dimensions of up to 100 μm^2. Additionally, to transfer optical signals from one plane to another in the vertical directional coupler polymeric-based material requires an interaction coupling length of up to 2000 μm. Large waveguide dimensions can be beneficial for feasibility in coupling light in from a fibre. However, the disadvantage would be that the device footprint increases. In addition, polymeric-based materials have low melting point, making them to be incompatible with CMOS thermal processes.

A 3D optical vias with a compact structure is beneficial to fully exploit the real estate of silicon chips. With regard to the polymeric-based vertical S-bend coupler used to guide light from one layer to another through direct coupling, shows limited report on the use of CMOS compatible silicon-based materials operating at the 1550 nm working wavelength. Therefore, this thesis proposes an interlayer slope waveguide coupler with a structure adapted from the S-bend waveguide. The guiding material used was high index HWCVD a-Si:H, with n = 3.55, to obtain high optical confinement for bending of sub-micron waveguides [72]. The interlayer coupler was designed to achieve vertical freedom for direct coupling, allowing transport of light up or down the multilayer SiP platform over a relatively large cladding height. The presence of large cladding height is necessary in the design of any 3D optical interconnect, to ensure that waveguides placed on one level do not couple with waveguides placed on another level (or at a higher level). The device design is simple and robust in terms of fabrication, making it feasible to control the waveguide dimensions during fabrication. The ability to control the waveguide dimensions is helpful for minimizing fluctuations in the effective index of the optical mode (n_{eff}) across the slope waveguide. In addition, the nature of direct coupling of the interlayer slope waveguide renders the device adaptable to polarization change. Finally, it offers a broad bandwidth similar to any planar waveguides [7].

The design parameters of the proposed device can all be chosen; these include the guiding core dimensions, slope angle, slope height and slope length. Parameters are usually selected according to practical considerations regarding functionality and fabrication. For example, guiding core dimensions of 400 nm (w) by 400 nm (h) are mainly used. As discussed in Chapter 4, this core dimension support fundamental mode only. Importantly, its ability to confine high optical confinement is higher than that of a 400 nm (w) by 250 nm (h) guiding core. The use of guiding core that provides high optical confinement is necessary to prevent an evanescent field radiating into the cladding. If that were to happen, the performance of the interconnect circuitry would deteriorate as a result of the crosstalk between close-proximity waveguides.

Table 2-3 Summary of various structures of 3D vertical coupler devices.

Types of Coupling Technology	Authors	Device Properties	Coupling Mechanism	Device Footprint - Volume	Results
	R. Takei *et al*., Opt. Express, 23, 14, (2015) [17]	c-Si/a-Si:H Vertical Interlayer Taper Coupler	Taper Coupler	Vertical gap = 0.6 μm Transitional coupling length = 650 μm Transitional coupling width = 3 μm Waveguides core height = 0.2 μm Volume = 1950 μm^3	Coupling Loss 0.87 dB
	K. Shang *et al*., Opt. Express, 23, 16, (2015) [54]	Si_3N_4 Interlayer Inverse Tapers	Taper Coupler	Vertical gap = 0.2 μm Transitional coupling length = 100 μm Transitional coupling width = 2 μm Waveguides core height = 0.2 μm Volume = 120 μm^3	Coupling Loss 0.01 dB
	K. Itoh *et al*., IEEE J. Sel. Topics Quantum Electron., 22, 6, (2016) [75]	c-Si/a-Si:H Vertical Trident Coupler	Taper Coupler	Vertical gap = 0.15 μm Transitional coupling length = 75 μm Transitional coupling width = 0.45 μm Waveguides core height = 0.22 μm Volume = 19.9 μm^3	Coupling Loss 0.49 dB
	Y. Zhang *et al*., Appl. Phys. Lett, 102, 21, (2013) [76]	c-Si Interlayer Grating Coupler	Grating Coupler	Vertical gap = 3.7 μm Transitional coupling length = 1029 μm Transitional coupling widths = 10-13 μm Waveguides core height = 0.25 μm Volume = 56,183 μm^3	Coupling Loss 7.45 dB

Types of Coupling Technology	Authors	Device Properties	Coupling Mechanism	Device Footprint - Volume	Results
	M. Sodagar *et al.*, Opt. Express, 22, 14, (2014) [77]	c-Si/a-Si:H Vertical Trident Coupler	Grating Coupler	Vertical gap = 1.6 μm Transitional coupling length = 234.4 μm Transitional coupling width = 12 μm Waveguides core height = 0.25-0.4 μm Volume = 248.7 μm^3	Coupling Loss 2 dB
	M. U. Khan *et al.*, Opt. Express, 23, 11, 2015 [78]	Polymer	Vertical directional coupler	Vertical gap = 5 μm Transitional coupling length = 1800 μm Transitional coupling width = 5 μm Waveguides core height = 4-5.6 μm Volume = 117,000 μm^3	Coupling loss 0.45 dB
	Garner *et al.*, IEEE J. Quant. Electron., 35, 8, (1999) [47]	Polymer Vertical Waveguide Bend	Directional	Vertical gap = 5 μm Transitional coupling length = 110 μm Transitional coupling width = 6 μm Waveguides core height = 2 μm Volume = 5940 μm^3	Excess Loss < 0.3dB
	Ni *et al.*, Opt. Express, 17, 3, (2009) [79]	Polymer Layer-to-Layer Waveguide	Directional	Vertical gap = 100 μm Transitional coupling length = 2000 μm Transitional coupling width = 50 μm Waveguides core height = 50 μm Volume = 15 x 10^6 μm^3	Propagation Loss 0.25 dB/cm

The parameters of the slope structure were chosen based on the following criteria;

1) The functionality of the interlayer waveguide to propagate light signals from one layer to another, with the highest transmission possible, and
2) The compactness of the device to increase circuit density in terms of footprint.

The slope parameters are shown in Table 4-1 of Chapter 4. As noted in the table, the slope length decreased with an increase in slope angle, at a fixed value of slope height equal to 1.5 μm. The value of the slope height was adjustable depending on the etching parameters. Figure 4.4 shows the increase in the loss as the slope angle increases. This is a trade-off in designing the interlayer coupler – that is, whether to opt for lower loss or for device compactness, such as for the 5° and the 45° slope angle. The fabrication of the interlayer slope waveguide coupler results in sharp bends with small curvature at the slope interfaces. This can be observed in the cross-sectional SEM images as shown in Figure 2.4 for, (a) 10° slope angle, and (b) 25° slope angle.

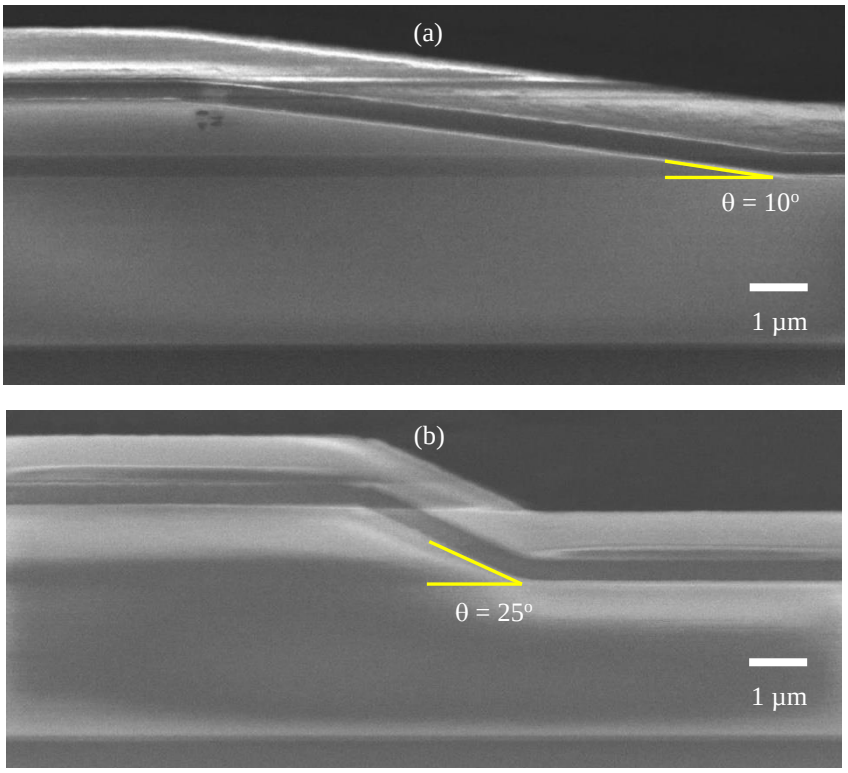


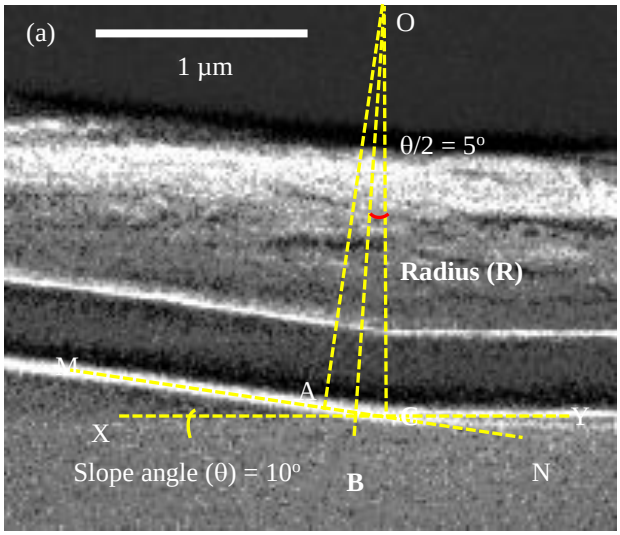
Figure 2.4 Cross-sectional SEM images of fabricated interlayer slope waveguide with slope angle (θ) equals to (a) 10°, and (b) 25°.

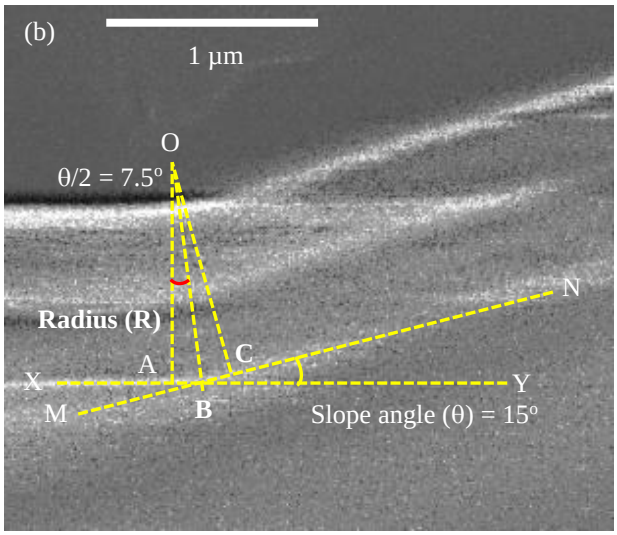
Knowing the radius of the curvature can be useful to gain mathematical estimation of mode transition at the slope interface. To estimate the radius of the curvature at the slope interface, the following procedures were used:

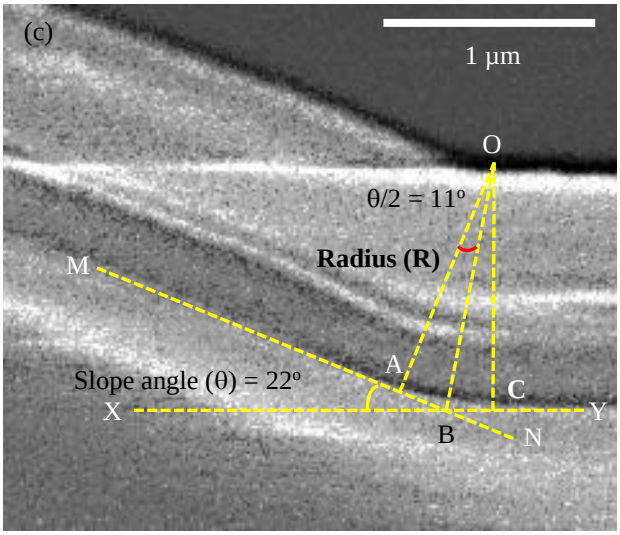
1. Draw two tangent lines (MN and XY),
2. Construct bisector at the curvature (OB),
3. Draw two perpendicular lines (OA and OC),
4. Measure the length of the arc (AC) and divide by 2,

5. Calculate the radius (R) using trigonometry formula, $R = \frac{BC}{Sin\,(\theta/_2)}$

The method of estimation is shown in Figure 2.5 for four fabricated slope angles for, (a) 10º, (b) 15º, (c) 22º and (d) 25º.







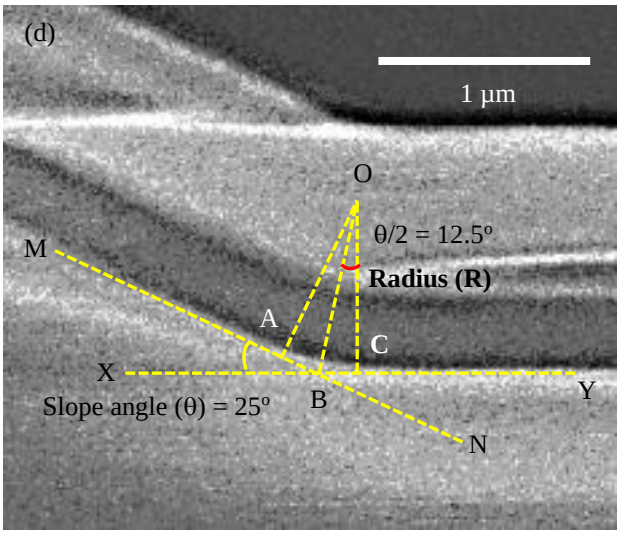


Figure 2.5 Method of calculation to estimate the radius at the slope curvature. Slope angle of (a) 10°, (b) 15°, (c) 22°, and (d) 25°.

Further, the slope length can be determined based on Pythagoras' theorem using known slope angle and slope height. The slope height was kept constant at 1.5 µm. Table 2-4 summarizes the calculated and estimated parameters of the slope structure.

Table 2-4 Design parameters of slope structure for proposed interlayer slope waveguide coupler.

Fixed slope height (µm)	Slope angle (°)	Calculated slope length (µm)	Calculated radius of the bend (µm)
1.5	10	8.5	1.8
	15	5.6	1.44
	22	3.7	1.09
	25	3.2	0.78

With the design of the interlayer slope waveguide being analogous to an S-bend waveguide, the parameters in Table 2-4 were used as a reference to compare the losses with those reported for planar S-bend waveguides. Table 2-5 shows the reported losses of bend waveguides.

Table 2-5 Reported losses of bend waveguides.

Author	Guiding material	Bend radius (µm)	Reported bend loss (dB per 90° bend)
Y. A. Vlasov *et al*., Opt. Express, 12, 8, 2004 [80]	c-Si	$R_1 = 1$ $R_2 = 2$	$R_1 = 0.086$ $R_2 = 0.013$
W. Bogaerts *et al*., Photon. J, 3, 3, 2011 [81]	c-Si	$R_1 = 2$ $R_2 = 4.5$	$R_1 = 0.04$ $R_2 = 0.005$
M. Cherchi *et al*., Opt. Express, 21, 15, 2013 [82]	c-Si	R = 10	R = 0.02
S. R. García *et al*., Opt. Express, 21,12, 2013 [83]	Si_3N_4	R = 35	R = 0.05
T. Lipka *et al*., J. Europ. Opt. Soc. Rap. Public. 7, 2012 [84]	a-Si:H	R = 5	R = 0.025

A main concern in multilayer technology is the potential for crosstalk between waveguides. Therefore, it is essential to design the structure with isolation in mind. Several research groups have investigated optical coupling behaviour between two waveguides, characterized in the C-band wavelength. Donzella *et al*. [19] reported -20 dB crosstalk between two crystalline silicon (c-Si)

waveguides placed side by side, separated by a 500 nm gap. Atsumi *et al*. [85] demonstrated their interlayer polarization beam splitter, characterized with a crosstalk of less than -20 dB with a vertical cladding thickness of 650 nm. Both Furuya *et al*. [86] and Suzuki *et al*. [87] reported a crosstalk value of -50 dB from cladding thicknesses of 400 nm and 1.5µm, respectively.

The distinct feature of the designed interlayer slope waveguide is the direct coupling of optical signals over a relatively large cladding thickness of 1.5 µm, permitting ample isolation. Subsequent to fabricating the interlayer slope waveguide, a crosstalk experiment was performed to confirm that the cladding height modelled in the designed interlayer slope waveguide was sufficient to optically isolate the input and output waveguides. This experiment demonstrated the capacity of the interlayer slope waveguide to function as a proper multi-layer interconnect, isolating optical light from any crossing waveguides, while routing optical signals in the most efficient way in terms of footprint. In addition to fabricating the interlayer slope waveguide, followed by characterizing its ability to isolate other crossing waveguide, a device was fabricated with a structure based on the slope platform. The device was called the “fly-over slope waveguide” and is illustrated Figure 1.1. The function of the device was to bring light up from Level 1 to Level 2 and back down to Level 1, so that it crossed over waveguides placed below at Level 1. The characteristics of the device were assessed in terms of its capacity to avoid crosstalk with the underlying waveguides.

2.7 Summary

The use of c-Si waveguides, as an optical interconnect to replace Cu, has shown ongoing success in SiP technology for a wide range of applications. For SiP to revolutionize the telecommunication IC industry, the issue of circuit density must be solved. The current SiP has a large circuit footprint to accommodate large numbers of optical devices with large dimensions. Multilayer circuit configuration has been identified as a possible solution to alleviate the space issue. To realize multilayer configuration, 3D optical vias must be created to connect the vertically stacked optical components. The main requirements are that the device should have compact dimensions and must be fabricated from CMOS-compatible Si-based depositable materials. In this project, the interlayer slope waveguide fabricated from HWCVD a-Si:H is proposed to connect an optical device from one signal plane to another by directly coupling the light up or down the multilayer platform. The characteristics of the proposed interlayer coupler are similar to waveguide bends, characterised in terms of loss in dB per slope. The isolation separation between the lower level waveguide and the upper level waveguide of the device is sufficient to avoid crosstalk. With these characteristics, the proposed interlayer slope waveguide coupler would alleviate the problems associated with the large circuit footprint of SiP and would be effectively used in a 3D SiP integrated chip. Further description of the design, modelling through FDTD simulation, fabrication and characterisation of the device are presented in the following chapters.

Chapter 3 Background and Theory

3.1 Introduction

The aim of this research was to design and develop an interlayer slope waveguide to route optical signals up and down within a multilayer platform. The way light propagates in the interlayer slope waveguide is similar to a waveguide bend. Thus, this chapter begins with an introduction to the physical principle that applies to a straight waveguide. Waveguide theory is then extended to the way in which light propagates in a bend and ultimately to the interlayer slope waveguide. Waveguide loss mechanisms in straight and bent waveguides are discussed along with ways to improve them. As an extension to this chapter, the theory of optical coupling is briefly described. This information is useful for understanding crosstalk between two identical waveguides placed in close proximity to each other.

3.2 The Physics of Optical Waveguides

The operation of the interlayer slope waveguide is similar to that of a bent waveguide. Therefore, it is useful to examine the physical principles that apply to a straight waveguide and to extend these to a waveguide bend, and ultimately to understand the theory of the interlayer slope waveguide. In this section, the fundamental operation of an optical waveguide is introduced. The ray optics model combined with electromagnetic theory describes how light propagates along the core of a waveguide. This model is used to determine several parameters, such as the allowed number of modes and the types of modes present in a specific waveguide structure. This is followed by determining the effective propagation constant for confined modes and the effective indices of the modes. The next sub-section discusses how the optical field distributes in an optical waveguide; thereafter an explanation is given about how optical modes are confined within a waveguide structure.

3.2.1 Mechanism of Light Propagation in an Optical Waveguide through Ray-Optics Approach

Figure 3.1 depicts how light that travels from a high-index (n_2) to a low-index (n_1) medium is reflected. Not all of the light travelling from an n_2 medium to an n_1 medium is reflected. Depending on the angle of incidence (θ_i), a fraction of light can be refracted out of the n_2 material [88, 89]. The relationship between refractive indices n_1 and n_2, and the angles of incidence (θ_i) and refraction (θ_t) is based on Snell's law [88, 89]. This law is stated as follows,

$$n_2 sin\theta_i = n_1 sin\theta_t \tag{3.1}$$

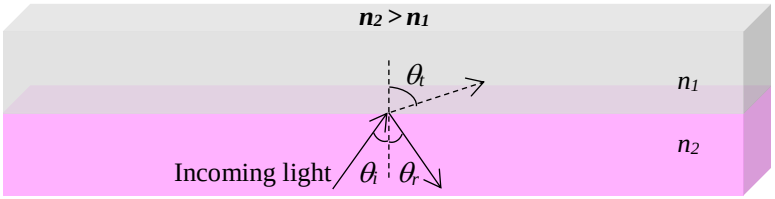


Figure 3.1 Propagation of light rays through two media, where $n_2 > n_1$ (reproduced from [88, 89]).

For the injected light to be entirely reflected, θ_i must be larger than the critical angle (θ_c) of the waveguide. The critical angle (θ_c) occurs when deviating θ_i far enough away from the normal, causing the refracted angle (θ_t) to approach 90°. At this point, light is no longer be refracted into n_1, as shown in Figure 3.2 (a). The value of θ_c for any material is, calculated from equation 3.2, which becomes equation 3.3 [88, 89]:

$$n_2 sin\theta_i = n_1 \sin(90^o) \tag{3.2}$$

$$n_2 sin\theta_i = n_1 \tag{3.3}$$

Hence, the formula to calculate θ_c for any material, can be simplified to equation 3.4 [88, 89]:

$$\theta_c = sin^{-1}\frac{n_1}{n_2} \tag{3.4}$$

Increasing θ_c further will result in the entire incidence ray reflecting, as shown in Figure 3.2 (b). At this point, the phenomenon of total internal reflection occurs. Provided the refractive index of the material at the lower boundary is less than or equal to that of the upper material, the light ray will be reflected many times within the waveguide core, and propagation of light occurs. The value of θ_c differs with different materials used for the waveguide.

The waveguide material studied in this thesis was hydrogenated amorphous silicon (a-Si:H), cladded with silicon dioxide (SiO_2) films. The refractive index of the a-Si:H film was similar to that of crystalline silicon (c-Si) at 1550 nm wavelength. Light propagation in the a-Si:H waveguide, cladded with SiO_2 film, with refractive indexes of ~3.55 and 1.45, respectively, required $\theta_i > 24.1^o$ to achieve total internal reflection. Silica fibre used in telecommunications, having a smaller index contrast with its cladding, with n equals to 1.4475 and 1.444, for the doped silica core and pure silica cladding, respectively, will have θ_c value equals to 86° [90].

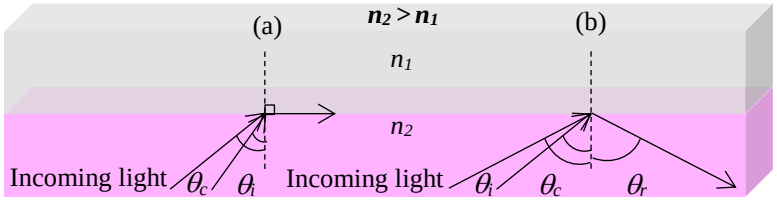


Figure 3.2 Demonstration of (a) critical angle, and (b) total internal reflection (reproduced from [88, 89]).

3.2.2 Extension to the Fundamental Operation of Optical Waveguide

In general, the process of total internal reflection describes the mechanism of light propagation in an optical waveguide. In an ideal case, light can be guided indefinitely by reflecting off the walls of the core layer until it reaches its destination. However, in practice this is not the case and other parameters need consideration. Light is made up of photons and behaves like any other electromagnetic (EM) wave in the EM spectrum, containing electric and magnetic field components. Thus, to guide light within the waveguide core, additional conditions must be met. The boundary conditions for electric and magnetic fields of the transverse electromagnetic (TEM) wave must be considered. A light wave can either be transverse electric (TE) or transverse magnetic (TM) polarized mode. This characteristic depends on the orientation of electric and magnetic fields of the TEM wave with respect to the plane of incidence. Here, the plane of incidence refers to as light rays bouncing off in the *y*-direction and propagating along the *z*-direction. It is known that the TE mode configuration occurs when the electric fields of TEM waves are perpendicular to the plane of incidence. The TM mode occurs when the magnetic fields are perpendicular to the plane of incidence. Figure 3.3 illustrates the orientation of electric fields in TE mode polarization. The black dots represent electric field emanating from the plane of the paper or, perpendicular to the plane of incidence, whereas the magnetic field is parallel to the field of incidence. This configuration is the same for TM mode, with the magnetic fields being perpendicular to the plane of incidence and the electric field being parallel to the plane of incidence [88]. In general, this would mean that in TE mode configuration, loss is mainly dominated from the optical mode overlap with the sidewall roughness of the waveguide. By contrast, in TM mode, loss is mainly contributed by the optical field interacting with the top and bottom surface of the waveguide.

Combining ray optics and electromagnetic theory grants insight to the behaviour of light propagating in an optical waveguide. The following sections describe some of the important parameters to consider when studying an optical waveguide.

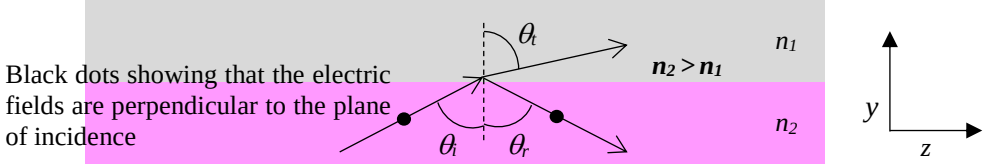


Figure 3.3 One dimensional (1D) illustration of the direction of electric fields in a transverse electric (TE) mode (reproduced from [88]).

3.2.2.1 Electromagnetic Model

As a continuation to the above discussion, it is worth looking into electromagnetic theory which is used as a tool to provide knowledge on field distribution of mode propagating in an optical waveguide. The electromagnetic model requires the solving of wave equation, the Helmholtz. The wave equation for electromagnetic waves is a sinusoidal function containing [91]:

1. ω, the frequency, which defines time variation ($\omega = 2\pi f$), and
2. k, the wave-vector or propagation constant, which defines the spatial variation of the wave ($k = {}^{2\pi}/_{\lambda}$).

Wave equation is written in the form [91]:

$$\nabla^2 E = \frac{1}{v^2}\frac{\delta^2 E}{\delta t^2} \tag{3.5}$$

Where E is the electric field, v is the velocity ($= {}^{c}/_{n}$) and t is the time.

When the wave is propagating in free space, $k = k_o$. And when the wave travels through a medium, they are related by the refractive index of the material, n. This gives $k = nk_o$. Having knowledge on the field distribution is important, especially to calculate the overlap integral for coupling out of a waveguide or to determine confinement factor [91].

It can be assumed that a uniform plane wave propagating in the z direction is expressed in the form [92]:

$$E(r) = E(x, y)\exp(-i\beta z) \tag{3.6}$$

Where E is the electric field vector, r is the radius vector and β being a propagation constant. Knowing the β value can be useful to determine: 1) the interaction of modes with its surrounding, and, 2) the shape of the field for coupling to another optical structure. There are four general conditions of possible modes in a planar waveguide, with mode shape changes as a function of β, as shown in Figure 3.4. A common condition for waveguiding requires the guiding layer n_2 be greater than the substrate n_3 and the top cladding layer n_1 ($n_2 > n_3 > n_1$) [91, 92].

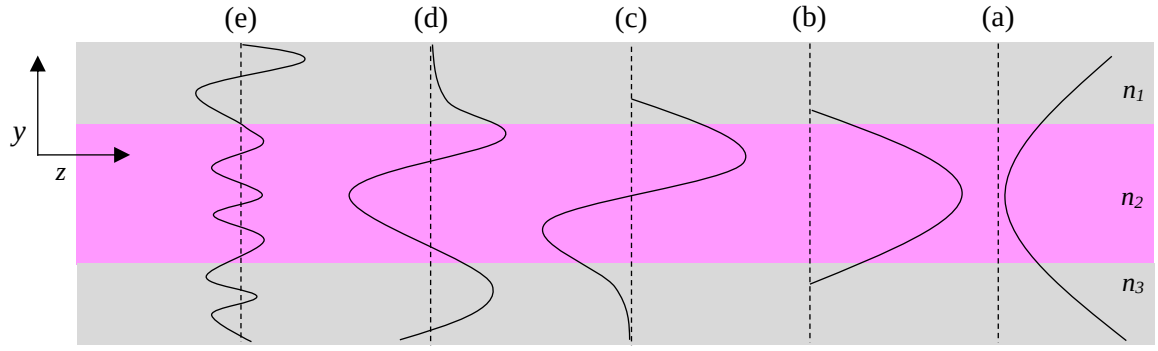


Figure 3.4 Schematic diagram of the possible modes in a planar waveguide (reproduced from [92]).

1) When $\beta > k_o n_2$: The function $E(y)$ must be exponential in all three regions and only the mode shape shown in Figure 3.4 (a) could satisfy the boundary conditions of $E(y)$ and $\delta E(y)/\delta y$ being continuous at the interfaces. These exponentially decaying solutions imply that no wave propagates in the waveguide, and any injected mode will decay to zero.

2) For values of β between $k_o n_2$ and $k_o n_3$ ($k_o n_2 > \beta > k_o n_3$), such modes can be supported. The guiding region has a propagating sinusoidal solution. Modes in Figure 3.4 (b) and (c) are the well confined guided modes, referred to as the zeroth order (fundamental) and first order TE modes, TE_0 and TE_1, respectively. In the top cladding and substrate, the solutions are still exponentially decaying.

3) If β is greater than $k_o n_1$ but less than $k_o n_3$ ($k_o n_1 < \beta < k_o n_3$), a mode shown in Figure 3.4 (d) will result. This type of mode, which is often called a substrate radiation mode, is confined at the air interface but sinusoidally varying at the substrate. In some circumstances, this mode can be supported by the guiding core, but because it is continually losing energy from the top cladding and the substrate regions as it propagates, the mode tends to be damped out over at short distance.

4) If β is less than $k_o n_1$ ($\beta < k_o n_1$), the solution for $E(y)$ is oscillatory in all three regions of the waveguide structure. Such a situation of oscillatory behaviour in all layers implies that there is no guiding, and this is generally referred to as the air radiation modes as shown in Figure 3.4 **(e)**.

Another important criteria in optical waveguiding is the ability for the mode to continue to propagate with the highest coupling efficiency. This can be determined by how well the excitation fields and the waveguide modes match, in terms of its β values. Additionally, this can be measured through fields overlap between the two field profiles (modes). Consequently, the overlap integral (Γ) is evaluated between the input field (E) and the fundamental mode (ε) of the waveguide, and is given by the equation [88]:

$$\Gamma = \frac{\int_{-\infty}^{\infty} dy \int_{-\infty}^{\infty} E\varepsilon dx}{\left[\int_{-\infty}^{\infty} dy \int_{-\infty}^{\infty} E^2 dx \,.\, \int_{-\infty}^{\infty} dy \int_{-\infty}^{\infty} \varepsilon^2 dx\right]^{\frac{1}{2}}} \tag{3.7}$$

The denominator is a normalising factor. The Γ value lies between 0 and 1, which represent the range between entirely no mode coupling and total coupling due to fields overlap [88]. The reduction in the power coupling can be caused by several factors such as index change at the interface, coupling to higher-order modes and change in guiding structure such as bents.

3.2.2.2 **Number of modes**

Figure 3.5 shows that the light ray of the TEM wave constitutes several plane waves, propagating in the *z*-direction, with light being confined in the *y*-direction through total internal reflection [88]. For light to be successfully guided, plane waves from Point A must at least have two reflections at the core-cladding interface. The waves must be in phase and superimpose with the part that was not

reflected, in this case, plane waves from Point B. When these conditions are met, the waves form constructive interference and continue to propagate along the waveguide core. As a result, only certain values of θ_i with a limited number of electromagnetic plane waves are allowed to guide in the waveguide structure [91].

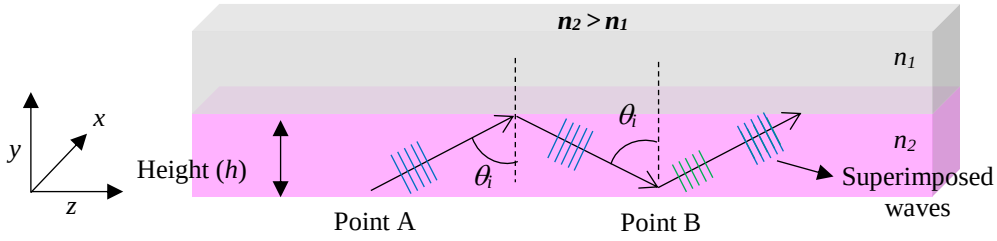


Figure 3.5 Geometric representation showing the phase-matching condition of a reflected wave propagating in a waveguide, after two reflections at the core-cladding interface (reproduced from [91]).

Waves travelling in free space have the propagation constant shown in equation 3.5 below [91].

$$k = n_{air}\, k_o = n_{air}\, \frac{2\pi}{\lambda_o} \tag{3.8}$$

Assuming that the refractive index of the medium is air, with n = 1, the equation is more simply written as follows:

$$k_o = \frac{2\pi}{\lambda_o} \tag{3.9}$$

If the wave propagates inside a higher index medium, the propagation constant is affected by the refractive index of the medium it travels into. To analyse wave behaviour, the TEM wave is decomposed into two components, as shown in Figure 3.5.

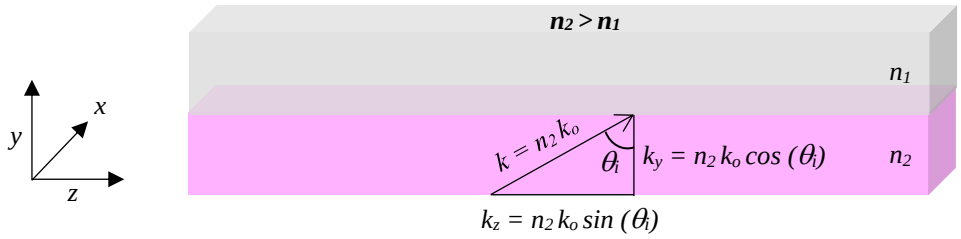


Figure 3.6 Relationship between propagation constant, k_o = 2π / λo, in free space and actual propagation constant in a waveguide with refractive index n_2 (reproduced from [88, 91]).

The propagation constants of the wave in the y and z directions are expressed as follows [88]:

$$k_y = n_2\, k_o \cos(\theta_i) \tag{3.10}$$

$$k_z = n_2\, k_o \sin(\theta_i) \tag{3.11}$$

The waves propagating along the z-direction and zig-zagging in the y-direction are not purely reflective. Waves reflecting at the waveguide boundary in the y-direction experience a change in phase. This phase change or phase shift (ϕ) causes a fraction of the electric and magnetic field components of the propagating waves to decay into the cladding layers. As a result, a fraction of the fields sit outside the waveguiding core occurring as evanescent field.

For a waveguide with a core thickness of equal to h, the phase shift (ϕ_h) introduced by a complete round trip (in this case, two reflections at the core-cladding interface) is given by equation 3.9 [88]:

$$\emptyset_h = 2hk_y = 2hn_2\, k_o \cos(\theta_i) \tag{3.12}$$

For waves reflecting at the upper (ϕ_u) and lower (ϕ_l) boundaries, the total phase shift is represented as follows [88]:

$$\emptyset_t = 2hn_2\, k_o \cos(\theta_i) - \emptyset_u - \emptyset_l \tag{3.13}$$

To preserve the wave reflecting in full cycle across the waveguide, the total phase shift is equated by 2π, giving the equation 3.11 [88]:

$$2hn_2\, k_o \cos(\theta_i) - \emptyset_u - \emptyset_l = 2\pi m \tag{3.14}$$

where m is an integer. The integer m corresponds to a parameter called the m_{th} mode, with m equal to 0, 1, 2, 3 and so on.

Earlier in this sub-section, it was mentioned that only certain values of θ_i of light waves are allowed to guide in the waveguide structure. The allowed θ_i is referred to as θ_m, which determines the allowable number of modes that can propagate in a waveguide. In turn, this depends largely on the thickness of the core layer (h), the working wavelength (λ) and the refractive index difference of the materials used in the waveguide [89, 91]. The expression for calculating the number of modes is shown in equation 3.12 [89],

$$m = 2\frac{h}{\lambda_o}\sqrt{{n_2}^2 - {n_1}^2} \tag{3.15}$$

At a wavelength equals to 1550 nm, an a-Si:H waveguide cladded with silicon dioxide, having a waveguide core thickness of 250 nm, 500 nm or 1000 nm, has the capacity to support one mode, two modes and four modes, respectively. By contrast, Si_3N_4 having a refractive index of 2.3 is unable to support the same number of modes as the high-index material waveguide. For a core thickness of 250 nm, no mode can be supported, for 500 nm and 1000 nm, the Si_3N_4 waveguide can support only one mode and two modes, respectively. The modes are described using a notation according to the mode number. For example, the first guided TE mode is referred to as TE_0, which is the fundamental mode; the first-order mode isTE_1; the second-order mode is TE_2; the third-order mode is TE_3, and so on. The TE_0 mode is critical as it produces a strong optical mode. This mode has the largest θ_i and thus, creates the fewest reflections. TE_0 contains the highest optical power within the waveguide. By contrast, TE_3 has the most reflections at the core-cladding interface due to θ_i becoming smaller. The number of times the mode penetrates the cladding layers is higher, making the mode in the waveguide lossy.

In addition, there is a limiting factor that determines how many modes can be supported in a waveguide structure [88]. This is also referred to as the cut-off conditions where a certain number of

modes that can be supported, largely depends on the values of n_2 and n_1, and the thickness of the core layer, for a given wavelength, λ_o [92]. Here, the θ_i of the propagating waves cannot be smaller than θ_c of the waveguide materials [88]. A small θ_i caused by low index difference between the core and cladding materials, reduces the effective index of the mode propagating in a waveguide. When the effective index of the mode is close to the refractive index of the cladding, no optical mode can be guided or supported. The effective index of the mode is discussed further in the following section.

3.2.2.3 **Effective Propagation Constant and Effective Index of the Mode**

In addition to the allowable number of modes for a given waveguide dimension, it is necessary to know the effective propagation constant of the propagated waves. Waves travelling in a high-index medium have a propagation constant that is affected by the refractive index of the medium they travel into. Each mode that propagates inside the core of the waveguide has its own propagation constant. In Figure 3.6, the effective propagation constant (β) of a confined mode is the propagation constant of the wave travelling in the *z*-direction. This can be written as follows [88]:

$$k_z \equiv \beta = n_2 \, k_o \sin(\theta_i) = N \, k_o \tag{3.16}$$

The term *N* is a parameter defined as the effective index of the mode. To describe it clearly, *N* can be written as follows [88]:

$$N = n_{eff} = n_2 \sin(\theta_i) \tag{3.17}$$

In principle, every optical mode propagating in a waveguide core has its own value of *N*. Generally, the following two factors influence the *N* of a mode propagating in a waveguide:

1) The dimensions of the waveguide core. Equation 3.14 indicates the reliance of θ_i on the height (h) of the waveguide core. Substituting the value of θ_i into equation 3.17 yields the value of *N*. At a fixed value of m, decreasing the h of the waveguide core will decrease θ_i, thus decreasing the *N*.
2) The order of mode (m^{th}) propagating in the waveguide core. Increasing the value of m in equation 3.14 to allow for more modes to propagate results in a smaller θ_i. Similarly, the value of θ_i is substituted into equation 3.17. Increasing the mode number (m) decreases *N*, compared to when $m = 0$. This was confirmed by simulation and is discussed in Chapter 4.

In both cases, a small θ_i would result in a small *N*. The waveguide would thus be unlikely to support a strong optical mode, or might not support any modes at all. In a 2D waveguide analysis, the dimension dependency extends to both the h and the width (w) of the waveguide core. This is because in 2D analysis, the polarisation of electric fields for both TE and TM must be considered.

3.2.2.4 **Confinement Factor**

The amount of optical power that a waveguide can carry is represented as a quantity referred to as the confinement factor (Γ). The Γ describes how much energy is contained in the core of a waveguide, in relation to the refractive index values of the core (n_2) and the cladding (n_1), the thickness of the core layer (h) and the working wavelength (λ_o) [88, 91]. The Γ value can be calculated from the following formula [88]:

$$\Gamma = \frac{\int_{-\frac{h}{2}}^{\frac{h}{2}} {E_x}^2\,(y)\,dy}{\int_{-\infty}^{\infty} {E_x}^2\,(y)\,dy} \tag{3.18}$$

where, E_x is the electric field for TE mode propagating along the z-direction and reflecting sinusoidally in the y-direction [91]. To determine Γ, the wave equation (equation 3.16) is solved using the boundary conditions in the y-direction of the waveguide structure [91]:

$$E_x = E_x(y)e^{-j\beta z}e^{j\omega t} \tag{3.19}$$

In solving equation 3.19, the electric fields from three regions of the waveguide must be considered. They are the upper cladding (E_u), the core (E_c) and the lower cladding (E_l), with each having different electric fields expressions [88]. These electric fields can be represented by the following equations [88]:

For upper cladding
$$E_x(y) = E_u \exp[-k_{yu}(y - \frac{h}{2})] \qquad y \geq \frac{h}{2} \tag{3.20}$$

For core
$$E_x(y) = E_c \exp[-\mathrm{j}k_{yc}\mathrm{y}] \qquad -\frac{h}{2} \leq y \leq \frac{h}{2} \tag{3.21}$$

For lower cladding
$$E_x(y) = E_l \exp[k_{yl}(y + \frac{h}{2})] \qquad y \geq -\frac{h}{2} \tag{3.22}$$

Here, k_{yu} and k_{yl} represent the decay constants for the upper and lower cladding, and k_{yc} represent the propagation constant of the mode in the core region, with respect to the y-direction [88]. The equations for the propagation constant and decay constants of the mode in the y-direction are expressed as follows [91]:

For upper cladding
$$k_{yu} = k_o\sqrt{N^2 - {n_1}^2} \tag{3.23}$$

For core
$$k_{yc} = k_o\sqrt{{n_2}^2 - N^2} \tag{3.24}$$

For lower cladding
$$k_{yl} = k_o\sqrt{N^2 - {n_3}^2} \tag{3.25}$$

where:

k_o is the propagation constant of waves travelling in free space

N is the effective index of the mode propagating in the waveguide core

n_1 is the refractive index of the upper cladding

n_2 is the refractive index of the core

n_3 is the refractive index of the lower cladding

Having solved equation 3.18, the Γ demonstrates reliance on the thickness of the waveguide core. Figure 3.7 graphically illustrates Γ versus core thickness (nm) for a-Si:H waveguide cladded with SiO_2, and for an Si_3N_4 waveguide cladded with SiO_2. The source was an estimation by Botez [93].

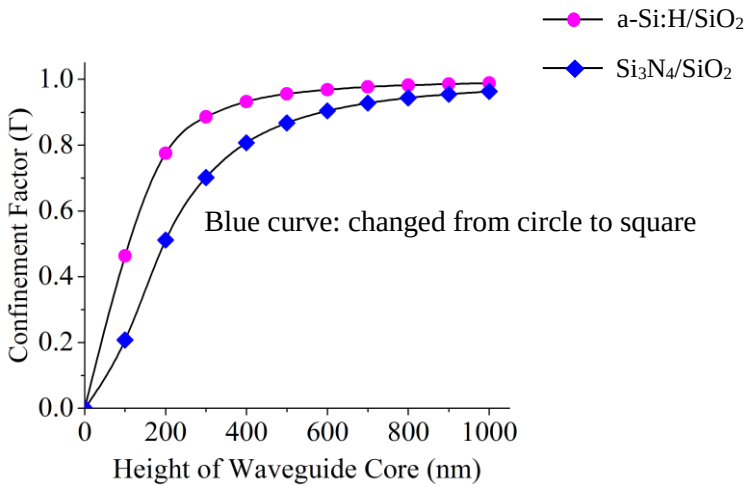


Figure 3.7 Graph of confinement factor (Γ) against height of waveguide core (nm) for hydrogenated amorphous silicon (a-Si:H) waveguide cladded with silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) waveguide cladded with silicon dioxide (SiO_2).

The graph shows that as the thickness of the core increases, more power can be confined in the waveguide core. Comparing the two core materials shows that better confinement was achieved by a-Si:H film than Si_3N_4, due to the large index difference between a-Si:H and SiO_2.

3.2.2.5 **Waveguide Structure**

In the previous section, a slab waveguide alone was considered in the theoretical analysis. To realize a wire-like structure for interconnect applications, the width of the waveguide must be assigned a discrete value so that light can be confined in both the *x* and *y* directions, travelling in the *z*-direction. Two fundamental etched waveguide structures are commonly used, namely the ridge structure and the rib structure. The schematic structure of each type of waveguide is shown in Figure 3.7 (a) and (b), respectively [94].

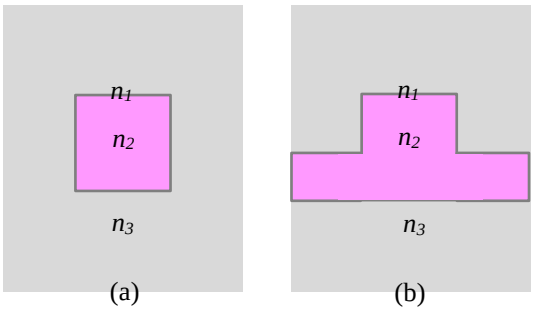


Figure 3.8 Schematic structure of waveguides: a) ridge, and b) rib (reproduced from [94]).

The ridge waveguide structure is suitable for interconnect applications due to its small dimensions. The advantage of using this structure is that the optical mode has greater confinement in submicron waveguides, which minimises crosstalk and bending loss. By contrast, the rib structure waveguide can be useful when higher-order modes are required. In principle, higher composition of core material results in an increased *N*, which allows more modes to propagate.

3.3 Fundamental Operation of a Waveguide Bend

This thesis focuses on the development of an interlayer slope waveguide, in which the working principle is analogous to a waveguide bend. In this section, the fundamental operation of the waveguide bend and the loss mechanisms associated with it are introduced. Then the physical theory of waveguide bends is applied to the interlayer slope waveguide.

3.3.1 Mechanism of Light Propagation in a Curved Waveguide

One of the many advantages of using a-Si:H as waveguide material is its high index contrast with SiO_2. This facilitates tight waveguide bends without incurring significant loss, which is an important element in photonic integrated circuits (PICs). Waveguides on a PIC are typically used to transport signals between components. To efficiently use chip real-estate, bends connect components that are positioned optimally, minimising the footprint [51, 94-96]. Curved or S-bend waveguides have also been used in specialized components such as ring resonators, directional couplers, y-splitters and the Mach-Zehnder [96, 97]. This section describes the mechanism of light propagating in a waveguide bend and the associated loss that is induced.

The way light propagates in a bend follows the fundamental principle of total internal reflection as discussed in Section 3.2. Effectively, modes propagating at the straight section and at the straight-bend junction of the waveguide propagate at different β values. The difference in β values travelling at different phase velocities, with dissimilar mode shape, results in mode-mismatch. This reduces the overlap coupling between the fundamental mode at the straight section and the bend mode at the straight-bend interface. Ultimately, this gives rise to radiative losses occurring between the straight and the waveguide bend [98].

As illustrated in Figure 3.9 [99], light injected into the waveguide travels along the core layer by reflecting off the walls of the core-cladding interface at an incident angle θ_i.

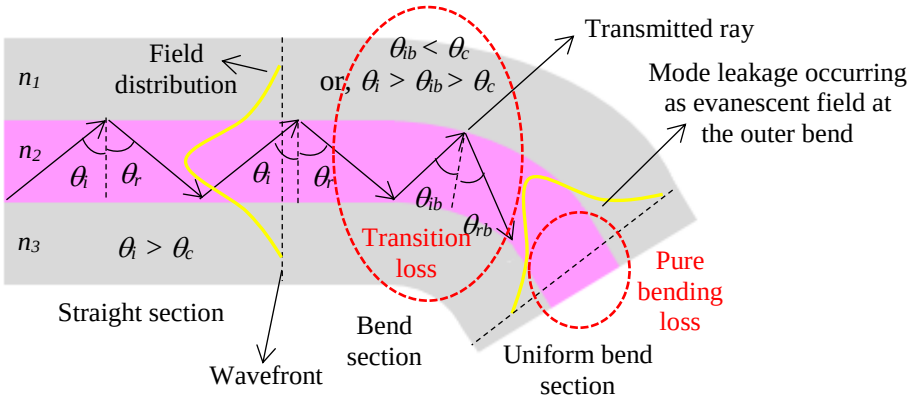


Figure 3.9 Schematic diagram of light propagation in a bend waveguide (reproduced from [98]).

If the light encounters a bend, light rays propagating inside the core layer change direction according to the shape of the interface curvature. The zig-zagging ray suddenly incurs an angle of incidence, θ_{ib} that is narrower than the original θ_i. If θ_{ib} is much smaller than θ_c ($\theta_{ib} < \theta_c$), total internal reflection does not occur and vast optical power is leaked into the cladding and is lost through radiation [99].

Depending on the radius of the curvature, light may continue to propagate in the core layer under the new θ_{ib} with some rays being transmitted into the cladding. The sudden change in the angle of incidence, from θ_i to θ_{ib}, changes the effective index (n_{eff}) and the effective propagation constant (β) of the propagating mode. This leads to the propagating mode having an entirely different electric-field distribution. The shape of the optical mode becomes distorted, with some of the mode field penetrating into the cladding layer and being lost through radiation. Then the distorted mode with an evanescent tail is extended into the cladding at the outer bend and continues to propagate in the uniform section of the bend, as indicated in Figure 3.9. The mode continues to radiate its energy at a constant rate, resulting in further loss in the waveguide. At some point, the extended field at the outer bend must keep up with the field at the inner bend, to maintain the phase relationship across the mode by travelling faster. However, due to the fundamental principal where the speed of light is constant in a given material, it is impossible for the fields to conserve the phase relationship across the mode. As a result, light continues to shed its energy and increases the overall loss [99-101].

The above description shows that two types of loss are induced in a waveguide bend. The first is the transition loss which is due to mode conversion occurring at the start of the bend. Transition loss becomes more pronounced if the radius of the curvature continues to change progressively and if there is a change in the curvature sign, as in the S-bend structure. Generally, transition loss is minimized through a gradual increase in the radius of curvature, to allow minimal change in the n_{eff} of the mode, and thus to tightly confine the optical field propagating inside the core [95, 97, 100]. The second type of loss is pure bending loss, which occurs in the uniform section of the waveguide bend, where light radiates uniformly. This phenomena is the result of the decayed field occurring as

an evanescent field situated in the cladding of the outside bend [99, 101, 102]. Pure bending loss can be minimized by a large bend radius to reduce the odds of the leaky mode radiating its energy away.

3.4 Working Principle of the Interlayer Slope Waveguide

Figure 3.10 shows a schematic diagram of the interlayer slope waveguide coupler. The device comprises a lower level waveguide as the input, and an upper level waveguide as the output, connected by a waveguide on the slope. In the design, the slope angle θ is adjusted from 5° to 85° to determine the lowest loss by simulation. The slope height is equal to 1.5 μm to sufficiently isolate the input and the output waveguides, with the slope height being adjustable depending on the required etching parameters. Both the slope angle and the slope height give the corresponding value of the slope length, which can be obtained by calculation based on Pythagoras' theorem.

The fundamental operation of the interlayer slope waveguide is analogous to a waveguide bend having a structure similar to an S-bend waveguide as discussed in Section 3.3.1. Light rays entering the straight input waveguide travel along the core layer by reflecting back and forth at the core-cladding interface through total internal reflection. When the optical mode encounters the slope interface, the direction of light propagating inside the core instantly changes with respect to the shape of the slope curvature.

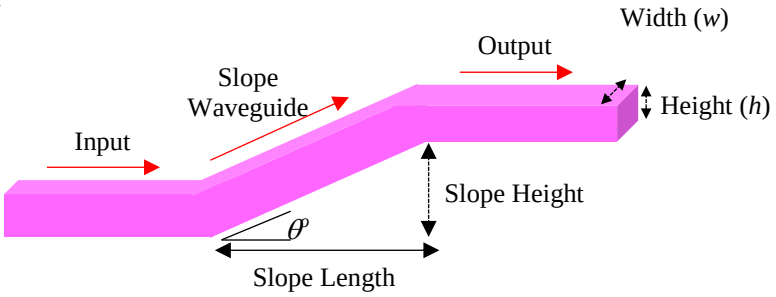


Figure 3.10 Schematic diagram of the interlayer slope waveguide coupler.

The change in the direction of light propagation induces a change in n_{eff} of the mode and thus also the effective propagation constant (β) of the propagating mode. This changes the distribution of the electric field and thus, the shape of the modes. The modes which are now propagating at different phase velocities due to dissimilar β values result in bending mode that extend into the lower SiO_2 cladding. This gives rise to smaller fraction of overlap mode coupling, resulting in power lost through radiation at the slope junction.

The disturbed mode continues to propagate along the slope waveguide, inducing pure bending loss at a constant rate. As the mode climbs up to the upper level waveguide, the disturbed mode experiences another mode conversion at the upper slope interface, resulting in further reduction of power intensity of the mode.

As in any optical devices, the design of the interlayer slope waveguide requires careful selection of parameters to reduce various loss mechanisms. Generally, losses in bend waveguide depend largely

on parameters such as the radius curvature and the n_{eff} change of the propagating mode [99]. This also applies to the interlayer slope waveguide, where the slope angle must be small to reduce loss. However, for compact device design, the slope angle cannot be too small, or the slope length would be too long. Thus, a trade-off in the design must be considered, to achieve a low-loss interlayer slope waveguide as well as device compactness. An elaborative simulation to investigate the optimal slope angle, incorporating other loss contributions – such as sidewall, top and bottom surface roughness – was performed using Lumerical FDTD software. The simulation results are presented in Chapter 4.

3.5 Loss Mechanisms in Optical Waveguides

In Section 3.2, methods of optimising the performance of an optical waveguide in terms of refractive index values, waveguide dimensions and structures were discussed. Another important parameter to consider when designing an optical waveguide is the loss mechanisms. Losses in an optical waveguide are contributed from three main sources: scattering, absorption and radiation [88, 91]. This section introduces these losses with reference to sub-micron-sized silicon-based waveguides.

3.5.1 Scattering Loss

In general, scattering loss arises from the imperfect physical nature of the waveguiding material, either at the interfaces of the waveguide or within the waveguiding medium. The former, commonly referred to as interface scattering, occurs as a result of the interaction of photons with the roughness of the waveguide's surfaces and sidewalls. There are four sides of interfaces with which propagating photons can interact: the top surface, bottom surface and the two waveguide sidewalls. The profile of the interface roughness can be quantified by an atomic force microscopy (AFM) tool to characterize the root mean square (RMS) roughness. The RMS roughness values of the interfaces normally differ and are highly dependent on the fabrication process parameters. Because of this, losses in the waveguide, operating either in TE or TM mode polarization, can also differ [66, 103].

A typical way of fabricating a rectangular waveguide structure is by dry etching method. Dry etching often leaves waveguides with substantial sidewall roughness. As an example, a crystalline silicon (c-Si) waveguide with a typical surface-roughness value of less than 1 nm, having sub-micron-sized rectangular structure, would have a higher propagation loss for TE mode than TM mode polarization [103] . In another example where a-Si:H was fabricated to a 500 nm width (w) by 200 nm height (h), width and height, losses of 3.2 dB/cm and 2.3 dB/cm were produced for TE and TM mode polarization, respectively [66]. Primarily, this was caused by the large interaction of TE mode with the rough waveguide sidewalls, caused during the process of fabrication.

The other type of scattering loss, which occurs within the waveguiding medium, is also known as "volume scattering"and arises through the occurrence of crystal lattice defects. Volume scattering is minimal in c-Si waveguides due to the regularity of the atomic bonding and the perfectly ordered

crystal structure. However, in a-Si and polysilicon waveguides, volume scattering can be substantial due to the presence of unpassivated dangling bonds and grain boundaries. Effectively, when photons encounter these defects, they become scattered and do not propagate.

3.5.2 Absorption Loss

Absorption loss occurs as a result of variance in material properties. There are two types of absorption, namely inter-band absorption and intra-band absorption. Inter-band absorption is the result of photons having energy much higher than the bandgap energy of the guiding core. Photons with energy larger than the bandgap energy ($h\nu > E_g$) transfer their energy to the electrons present in the valence band. As a result, the photons have insufficient energy to travel further and are unable to propagate along the core of the waveguiding medium. In telecommunications operating at the 1550 nm wavelength, c-Si waveguide is an ideal guiding material due to the large difference between the bandgap energy ($E_g \cong 1.2$ eV) and photons' energy ($h\nu = 0.79$ eV). This difference causes light to be transparent and to propagate continuously within the guiding core with minimal interference [92]. This is similar to a-Si:H, in which the film has an $E_g \cong 1.7$ eV, allowing photons travelling at a wavelength of 1550 nm to propagate without interference [104].

Intra-band absorption is the result of the giving up of energy from photons to electrons or holes, which are readily present at the edges of the covalent band, such as in doped silicon material. As the photons give up their energy to the dopant free carriers, they have insufficient energy to propagate in the guiding core medium and eventually die off [92].

3.5.3 Radiation Loss

Another loss mechanism in optical waveguides occurs through radiation caused by the decaying of light into the cladding layer as an evanescent field. Radiation loss is highly dependent on the design of the physical structure and dimensions of the waveguide. Light propagating in a waveguiding core travels under total internal reflection. When the propagating light encounters surface perturbation along the guiding core, such as surface roughness or bending, the light becomes scattered and decays out into the cladding layer. The decayed mode cannot be guided within the waveguiding core but instead is lost through radiation [92]. Radiation loss is minimal in a straight waveguide but becomes pronounced in waveguides with bends, such as in the curved waveguide and interlayer slope waveguide (see Sections 3.3 and 3.4). In addition, mode travelling through optical waveguides with thickness below the cut-off limit would expand and radiate out of the guiding core. Thus, in fabricating silicon-based waveguides it is important to ensure sufficient thickness of buried oxide (BOX) to prevent mode leakage to the silicon substrate. In this project, two bottom cladding thicknesses, 3 μm and 4.5 μm, were used.

3.6 Coupling between Two Waveguides

Crosstalk is undesirable in any waveguiding network system, especially multilayer photonics, as it can result in poor signal distribution. Thus, it is essential to study the characteristics that cause optical crosstalk. As discussed throughout this chapter, optical mode can decays out from the waveguiding core, which highly depends on the physical structure of the waveguide. Examples of the causes are:

1) Waveguide dimensions are pushed towards the cut-off limit of diffraction
2) Waveguides have bent or angled interfaces
3) Roughness occurs on the interfaces.

When such a waveguide is placed in close proximity to another waveguide, optical coupling occurs. This section briefly describes the factors affecting the occurrence of optical coupling and discusses the mathematical parameters, using examples from a-Si:H waveguides.

Optical coupling from one waveguide to another waveguide occurs if both waveguides have the same n_{eff} value and β constant. However, under certain circumstances, it can also happen that optical coupling can occur even when the waveguides are not identical. For example, mode from waveguide 1 is subjected to scattering loss due to surface perturbation, such as a bend or interface roughness. The mode of waveguide 1 now propagates with field decaying into the cladding. If waveguide 1 is placed in close distance to another waveguide (waveguide 2), the decaying field of waveguide 1 can get coupled to waveguide 2. In this condition, full energy transfer would not be achieved due to the waveguides not being identical. But the coupling of the evanescent field from waveguide 1 to waveguide 2, is sufficient to slightly increase the optical power in the core of waveguide 2 [101].

Figure 3.11 shows the schematic of two waveguides placed next to each other, illustrating the amplitudes of the electric field distributions in the waveguiding core.

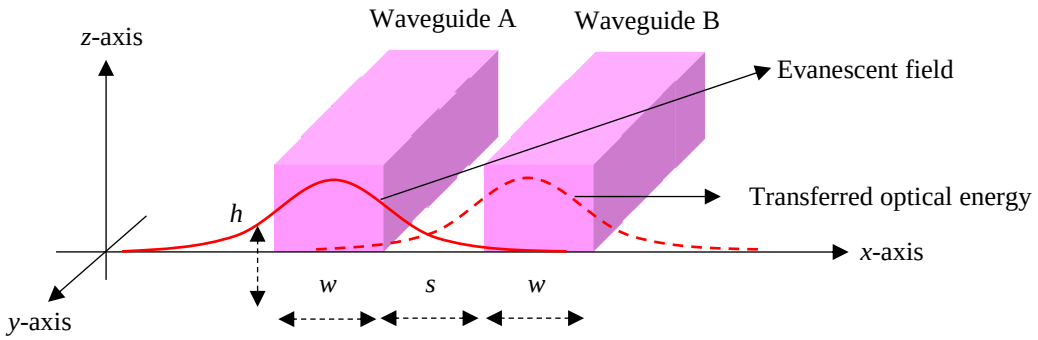


Figure 3.11 Schematic diagram of energy transfer from evanescent field (reproduced from [92]).

Given the propagating optical field in waveguide A, in the form [94, 100]:

$$(A) = (A_0(x,z)e^{j\beta z}e^{j\omega t}) \tag{3.26}$$

Similarly, the field in waveguide B propagates in the following form [94, 100]:

$$(B) = (B_0(x,z)e^{j\beta z}e^{j\omega t}) \tag{3.27}$$

The simplified form of the coupling equations that relate the amplitudes of each waveguide are written as follows [94]:

$$\frac{dA_0}{dy} = \kappa B_0 \tag{3.28}$$

$$\frac{dB_0}{dy} = -\kappa A_0 \tag{3.29}$$

With coupling coefficient (κ) equals to,

$$\kappa = \frac{2{k_{xg}}^2 k_{xc}\exp(-k_{xc}s)}{\beta w({k_{xg}}^2 + {k_{xc}}^2)} \tag{3.30}$$

Assuming that waveguide A is excited at $y = 0$, and waveguide B is not, the following equations apply [94, 100]:

$$A_0(y = 0) = 0 \tag{3.31}$$

$$B_0(y = 0) = C_0 \tag{3.32}$$

The solutions to these equations are [94, 100]:

$$A_0(y) = C_0\sin(\kappa y) \tag{3.33}$$

$$B_0(y) = C_0\cos(\kappa y) \tag{3.34}$$

From equations 3.31 and 3.32, it can be deduced that the electric field in the first waveguide can induce electric field in the neighbouring waveguide. This induction can occur across some distance in the *y*-direction, in a periodic manner.

The principle of optical coupling leading to the occurrence of crosstalk derives from the mode-coupling theory [92, 94, 100]. Optical power propagating along waveguide A (Figure 3.11) includes power travelling outside the waveguiding core. This part of the mode, which extends beyond the core and travels in the cladding, is referred to as the "evanescent field". When this evanescent field encounters another waveguide (waveguide B) with a matching β value, energy is transferred from one to the other over closed separation (s). The energy being transferred and which continues to travel over a significant length in waveguide B, propagates under maintained phase-coherence conditions. This means that light in each waveguide must propagate with the same phase velocity for optical coupling to occur. Full energy transfer from waveguide A to waveguide B occurs periodically along the *y*-direction, with a period given by coupling length, referred to as L_π [92, 94, 100]. The equation to determine the coupling length for achieving full energy transfer is as follows [94, 100]:

For full energy transfer $$L_\pi = \frac{m\pi}{2\kappa} \quad (3.35)$$

Mathematically, equation 3.30 shows that waveguides placed with very small separation (s) yield a high coupling coefficient (κ). Hence, waveguides placed in close proximity are likely to transfer their energy to the neighbouring waveguide. This attenuates the optical signal from the driving waveguide and increases the crosstalk signal in the other waveguide. When the separation of the two waveguides (s) is increased, the coupling coefficient (κ) decreases resulting in optical isolation between the two waveguides. Table 3-1 shows the list of parameters to the equations 3.30 and 3.35.

Table 3-1 List of variables for calculating the coupling coefficient (κ), and coupling length (L_π) for full energy transfer.

m	Integer values for periodic energy transfer	$m = 1, 2, 3, 4 \ldots \ldots$
k_{xg}	Propagation constant of the core in the x-direction	$k_{xg} = k_o\sqrt{{n_g}^2 - N^2}$
k_{xc}	Decay constant of the cladding in the x-direction	$k_{xc} = k_o\sqrt{N^2 - {n_c}^2}$
β	Effective propagation constant	$\beta = Nk_o$
s	Waveguide separation	*s (nm or μm)*
w	Waveguide width	*w (nm or μm)*
N	Effective index	*N (no unit)*

Using a-Si:H as the waveguiding material and considering equations 3.30 and 3.35, the effect of waveguide separation on κ and $L\pi$ was calculated: the results are shown and presented in Table 3-2. Figures 3.12 and 3.13 show the graphs of the coupling coefficient, κ, and coupling length, L_π, for the two waveguide dimensions, respectively. The graphs indicate that two waveguides placed very close to each other result in the waveguides having high coupling coefficients. This implies that the transfer of energy from one waveguide to another is possible.

In a waveguiding network system, this condition is undesirable, especially in multilayer photonics. It can attenuate the source signal propagating in the primary waveguide, increasing crosstalk to the neighbouring upper or lower level waveguide. Thus, separating the distance, s, between waveguides is necessary to reduce optical mode transfer to the neighbouring waveguide. In addition, κ in smaller waveguides is higher than in larger waveguides, as shown in Figure 3.12. This is due to the mode in the smaller waveguides being pushed out of the waveguiding core. As a result, waveguides with smaller dimensions are more susceptible than larger waveguides to transfer optical energy out, which leads to crosstalk.

Table 3-2 Calculations for effective propagation constant (β), coupling coefficient (κ) and coupling length (L_π) for full energy transfer, for two waveguide dimensions.

Parameters	**400 nm (w) by 400 nm (h)**		**1000 nm (w) by 400 nm (h)**	
Calculated effective index of fundamental mode, n_{eff}	2.67		3.16	
Calculated effective propagation constant, β (m^{-1})	1.08×10^7		1.28×10^7	
Separation, s (μm)	Coupling coefficient, κ (m^{-1})	L_π(μm)	Coupling coefficient, κ (m^{-1})	L_π(μm)
0.025	1.74×10^6	0.904	8.19×10^5	1.92
0.05	1.38×10^6	1.14	6.16×10^5	2.55
0.1	8.77×10^5	1.79	3.48×10^5	4.52
0.2	3.53×10^5	4.45	1.11×10^5	14.14
0.3	1.42×10^5	11.06	3.55×10^4	44.27
0.4	5.71×10^4	27.51	1.13×10^4	138.59
0.5	2.29×10^4	68.39	3.62×10^3	433.93
0.6	9.23×10^3	170.05	1.16×10^3	1358.59
0.7	3.72×10^3	422.77	3.69×10^2	4253.79
0.8	1.49×10^3	1051.1	1.18×10^2	13318.61
0.9	6.01×10^2	2613.20	3.77×10^1	41698.87
1.0	2.42×10^2	6496.80	1.20×10^1	130562.41

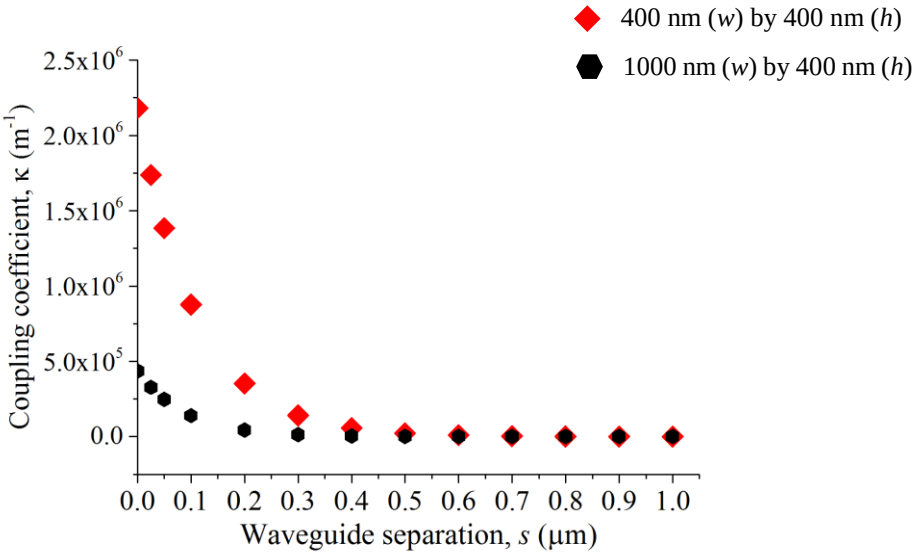


Figure 3.12 Coupling coefficient (κ) and waveguide separation (s) for two waveguide dimensions.

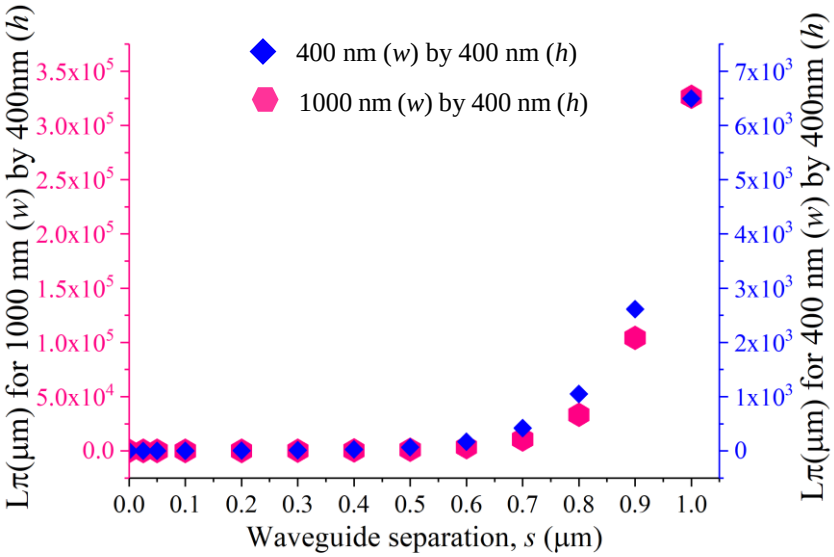


Figure 3.13 Coupling length for full energy transfer ($L\pi$) and waveguide separation (s) for two waveguide dimensions.

Theory regarding optical coupling occurring between two waveguides placed in parallel to each other as discussed in this section is intended to be used as a reference only. The crosstalk structure which was fabricated in this work was based on two waveguides placed in orthogonal on top of each other. Here, the treatment in optical coupling between two waveguides placed in parallel to each other and two waveguides placed in perpendicular on top of each other is different. This is because the evanescent field of the mode which managed to get coupled to the top (or bottom) orthogonal waveguide no longer maintains the same polarization as the input mode. And, it is improbable to achieve either half or full energy transfer, unlike those two waveguides which are placed in parallel to each other.

3.7 Summary

The fundamental operation of an optical waveguide is described in this chapter. The waveguide theory was extended to the way light propagates in a waveguide bend, which provided a tool to understand how light behaves in the interlayer slope waveguide. The characteristics and performance of an optical waveguide largely depend on waveguide parameters, such as dimensions of the waveguide, refractive index of the guiding and cladding materials, waveguide structures and fabrication processes. The theoretical background discussed in this chapter provides a reference for designing 3D interconnect devices for multilayer applications. To design the 3D interlayer coupler, knowledge of the behaviour of light coupling from one waveguide to another is necessary. Thus, in designing multilayer interconnect circuitry, it is critical to allow sufficient isolation between waveguides placed on two signal planes and side-by-side, to avoid unnecessary crosstalk. The theory discussed in this chapter is linked to the FDTD simulation work presented in Chapter 4.

Chapter 4 Modelling of the Interlayer Slope Waveguide Devices

4.1 Introduction

This chapter investigates the optical propagation characteristics of the interlayer slope waveguide in a multilayer platform. The method used was simulation with Lumerical finite-difference time-domain (FDTD) software. The chapter is divided into three main sections. The first section presents the design and simulation of the interlayer slope waveguide. The dimensions of the waveguide parameters and the slope platform structures are discussed in detail. This is followed by an investigation of the optical isolation required to prevent crosstalk between two waveguides placed orthogonally or in parallel to each other. This simulation was used to validate whether the cladding height modelled in the interlayer slope waveguide was sufficient to optically isolate the input and output waveguides – and other waveguides crossing the interlayer slope waveguide. The final section of this chapter presents an application of the interlayer slope waveguide model to function as a multilayer fly-over slope waveguide. The structure is discussed for varied parameters of the device.

4.2 The Interlayer Slope Waveguide Design

The interlayer slope waveguide comprised a lower level input waveguide and an upper level output waveguide, connected by a waveguide on the slope. The angle of the slope varied between 0^{o} and 85^{o}, with a cladding height sufficient to optically isolate the input and the output waveguides. The slope length was varied mathematically according to the slope angle. The waveguide parameters used in this work were as follows: 400 nm core height (h) with a waveguide width (w) ranging from 400 nm to 1000 nm. The waveguide dimensions of 400 nm core thickness (h) and 400 nm wide (w) waveguide provide maximal light confinement within the waveguide core while maintaining single-mode waveguide properties [105]. These two properties are generally desirable when designing a low-loss waveguiding network system.

The 220-nm core thickness is often used in SOI platforms. This dimension supports only the fundamental mode of transverse electric (TE_0). Because the effective index is much lower due to the corresponding smaller core height, the optical confinement in a 220-nm SOI platform is far less than with the 400-nm waveguide core thickness. As a result, a large fraction of the optical mode falls outside the waveguide core, occurring as evanescent field. Although evanescent field can be useful in certain waveguiding applications, such as directional couplers, it can be undesirable as it can create crosstalk in the waveguiding network system.

4.2.1 Determination of Dimensions for Single-Mode and Multi-Mode

The design of the interlayer slope waveguide coupler requires waveguide dimensions such that the waveguide supports the fundamental mode only, and has the highest confinement factor (Γ). Waveguide having a core thickness of 400 nm (*w*) and waveguide width of 400 nm (*h*) possess both these properties. FDTD simulation was performed to investigate and justify the range of dimensions for single-mode and multi-mode waveguides, to support fundamental and higher-order modes. Throughout the simulation in this chapter, refractive index (*n*) equals 3.55 for hydrogenated amorphous silicon (aSi:H) with fully-etched ridge waveguide structure, unless otherwise specified. The *n* value was obtained from Ellipsometer measurement at a working wavelength (λ) of1550 nm. The simulation parameters were such that *w* ranged from 0.2 μm to 1 μm, with a fixed *h* of 0.4 μm.

Figure 4.1 presents the simulation results, showing three supported modes for *w* of 0.2 μm to 1 μm, with fixed *h* of 0.4 μm. The waveguide is single-mode for waveguide *w* of 0.2 μm to 0.4 μm, for both TE_0 and TM_0. The waveguide becomes multi-mode when *w* is larger than 0.4 μm. However, the waveguide strongly supports and favours TE_0 and TM_0 modes at this width. It was observed that the difference in n_{eff} between TE_0 and TM_0 modes with TE_1 mode was greatest when *w* = 0.4 μm. The large difference reduced the likelihood of supporting the higher-order mode, TE_1. The TE_1 continued to be weakly supported until *w* was equal to 0.6 μm, and it began to be well-supported with further increase in *w*. Thus, *w* ranging from 0.4 μm to 0.6 μm was fabricated to investigate the optical characteristics of the HWCVD a-Si:H interlayer slope waveguide.

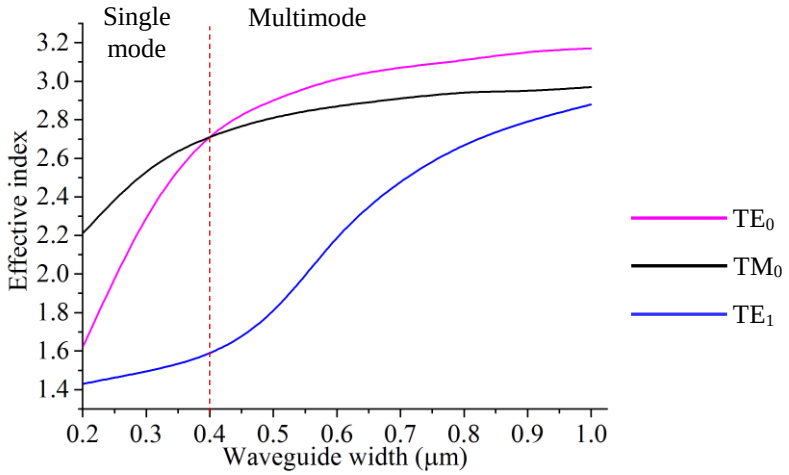


Figure 4.1 The effective index of the first three supported modes in a 0.4 μm thick a-Si:H ridge waveguide, as a function of waveguide width at a wavelength of 1550 nm.

Another parameter requirement in the design of the interlayer slope waveguide is that the waveguide should be able to contain substantial optical power. As discussed in Chapter 3, this

parameter, denoted as Γ, relies on the thickness of the core layer (*h*), the difference in the refractive index of the core (n_2) and the cladding (n_1), and the working wavelength (λ_o) [88, 91]. Effectively, Γ and n_{eff} are related and are used as a benchmark for choosing waveguide dimensions according to the waveguiding network system requirement.

4.2.1.1 **Discussion**

The number of modes that can be supported in a waveguide depends mainly on the width (*w*) and thickness of the core layer (*h*), the working wavelength (λ_o) and the refractive index difference (Δn) of the materials used in the waveguide. These point were discussed in Chapter 3 and the expression for calculating the number of supported modes is shown in equation 3.15. Based on the proportionality of the terms, decreasing the *h* and Δn parameters on the right-hand side of the equation results in a decrease in the number of supported modes (*m*). Likewise, increasing any of these parameters results in an increase in *m*.

The n_{eff} term plays a crucial role in designing an optical waveguide. Similar to the allowable number of modes, n_{eff} depends on the *h* and the *w* of the waveguide,as well as λ_o. In the simulation presented in Figure 4.1, the value of n_{eff} determined whether the waveguide was single-mode or multimode. Effectively, for a given wavelength and high refractive index difference, waveguides having large dimensions permit higher-order modes to propagate within the waveguide core. Decreasing the waveguide dimensions reduces the number of supported modes.

TE and TM mode polarizations behave differently according to waveguide dimensions. TE mode operates best with wider waveguides, whereas TM mode adapts well to high-aspect-ratio waveguide dimensions. This is due to the nature of the electric field component in TE mode propagating perpendicularly to the plane of incidence. By contrast, in TM mode the electric field component propagates in parallel to the plane of incidence.

The behaviour of TE and TM modes adapting to varied waveguide widths is shown in Figure 4.1. The TE_0 mode propagating in a waveguide with w = 0.2 μm has n_{eff} close to *n* of the cladding. At the same waveguide *w*, TM_0 has higher n_{eff}. At some point, TE_0 can still be guided but would only propagate with high loss. The high loss occurs because a large portion of the mode is extended out of the waveguide core and radiates into the cladding layer. This reduces the optical power carried by the waveguide.

The loss of TE_0 in a narrow waveguide can become pronounced with the presence of sidewall roughness. This is due to intense interaction of the TE mode with the sidewalls, which scatters the light and attenuates the optical power. As the *w* is increased to 0.3 μm, the n_{eff} of the mode increases, allowing TE_0 to be well guided. As the waveguide dimensions are enlarged, the n_{eff} increases further, permitting higher-order modes to be supported in the waveguide.

The main objective of this simulation exercise was to confirm that the waveguide dimensions of 400 nm (*w*) by 400 nm (*h*), used in this work would support only the fundamental mode. In addition, the exercise was intended to demonstrate that high optical power can be contained in the waveguide core. The simulation results, shown in Figure 4.1, proved that the square waveguide 400 nm (*w*) by 400 nm (*h*) strongly supported the fundamental mode both in TE and TM mode polarization, and weakly supported the higher-order mode. As *w* was increased to 0.6 μm, the waveguide still strongly supported TE_0 and provided less support for TM_0 and TE_1. The high n_{eff} of TE_0 indicated that it had the largest Γ and hence the smallest propagation loss, relative to TM_0 and TE_1.

Figures 4.2 and 4.3 illustrate the 2D optical-mode profiles of three waveguide dimensions: (a) 400 nm (*w*) by 220 nm (*h*); (b) 220 nm (*w*) by 400 nm (*h*); and (c) 400 nm (*w*) by 400 nm (*h*), for TE and TM mode, respectively. For TE mode polarization, a notable fraction of optical mode fell outside the waveguide core for the 400 nm (*w*) by 220 nm (*h*) dimension, as shown in Figure 4.2 (a). As the waveguide *w* was made narrower (as shown in Figure 4.2 (b)) the odds of TE_0 mode being supported diminished with a high portion of optical mode being pushed out of the waveguiding core and overlapping with the sidewalls. Optical mode in a 400 nm (*w*) by 400 nm (*h*) waveguide was better confined, as shown in Figure 4.2 (c).

For TM mode polarization, substantial optical mode fell outside the waveguide core, overlapping with the top and bottom interfaces, as shown in Figure 4.3 (a). As the core *h* was increased, TM_0 was well supported, with a smaller portion of optical energy being pushed out, as shown in Figure 4.3 (b). Optical mode was better supported when the waveguiding core was made into a square structure having 400 nm (*w*) by 400 nm (*h*) dimensions, as shown in Figure 4.3 (c).

Figure 3.7 (Chapter 3) plotted a graph of power confinement in relation to waveguide thickness (*h*) for a-Si:H waveguide cladded with SiO_2. The graph shows that light can be well confined within the guiding core by increasing the core height (*h*). Waveguide with *h* = 220 nm can contain 80.6% of optical signal, with the remaining signal occurring as evanescent field. Increasing the core *h* to 400 nm increased the power confinement to 93.2%.

The bending structure of the interlayer slope waveguide occurs in a vertical direction. Because the electric-field component of TM_0 propagates parallel to the plane of incidence, the preferred mode polarization for the interlayer slope waveguide is TE_0 rather than TM_0. This precaution avoids large amounts of light being lost through radiation because of significant mode-mismatch, when the mode (either TE_0 or TM_0) encounters the bend at the slope interface.

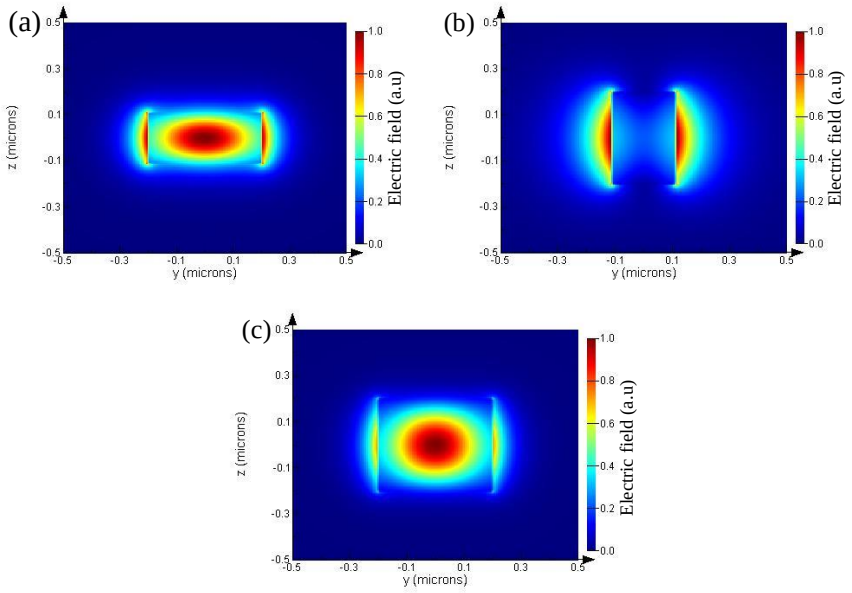


Figure 4.2 Simulation of 2D mode profiles for waveguide dimensions of, (a) 400 nm (*w*) by 220 nm (*h*), (b) 220 nm (*w*) by 400 nm (*h*), and (c) 400 nm (*w*) by 400 nm (*h*), at 1550 nm wavelength for TE mode polarization

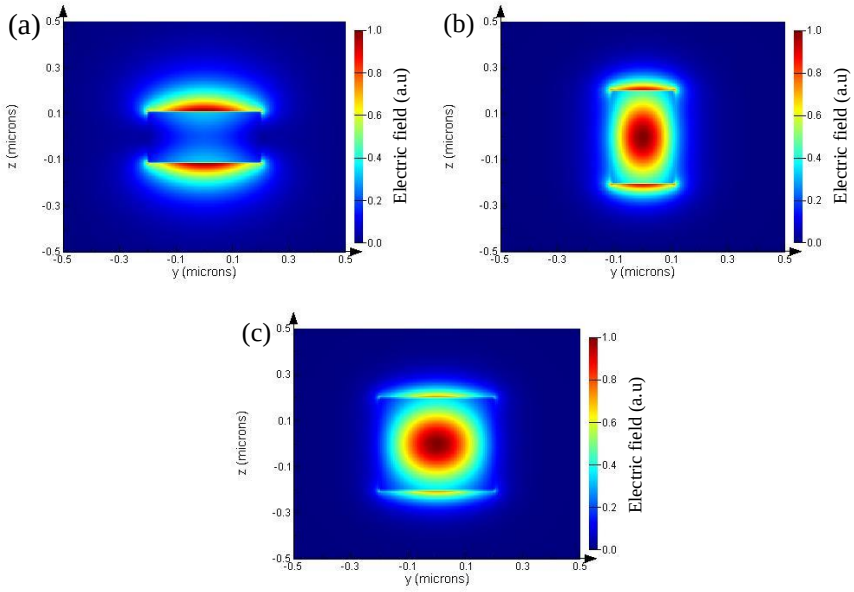


Figure 4.3 Simulation of 2D mode profiles for waveguide dimensions of, (a) 400 nm (*w*) by 220 nm (*h*), (b) 220 nm (*w*) by 400 nm (*h*), and (c) 400 nm (*w*) by 400 nm (*h*), at 1550 nm wavelength for TM mode polarization.

4.2.2 Design of the Slope Platform

The slope structure was designed so that the device was well adapted for practical use and integration into the multilayer silicon photonics platform. Two important criteria were considered:

1) The functionality of the waveguide to guide light from one layer to another with the highest transmission possible.
2) The compactness of the device to increase circuit density in terms of footprint.

In this work, a large slope height of 1.5 µm was designed to provide sufficient isolation between the lower level waveguide and the upper level waveguide and with other crossing waveguides. A preliminary study was conducted to assess the effect on transmission of varying slope height, with slope height set to 0.45 µm, 0.9 µm, 1 µm and 1.5 µm, with a fixed slope angle of 15°. The results showed insignificant change in the loss value and those results are not presented in this section.

In the design of the interlayer slope waveguide, the slope angle (inclination angle) plays a major role in obtaining high transmission. Based on the waveguide bend theory, the angle must be sufficiently small to avoid large changes in the n_{eff} propagating across the waveguide. Lumerical FDTD software was used to simulate the transmission characteristics of the interlayer slope waveguide with a varying slope angle from 5° to 85°. Here, the slope height was kept constant at 1.5 µm to allow sufficient isolation between the input and output waveguides, with the slope length varying according to the slope angle. The slope length was calculated based on Pythagoras' theorem, using a known slope height and angle. Table 4-1 shows the device structure parameters.

Table 4-1 Device parameters for the slope structure.

Slope height (µm)	Slope angle (°)	Slope length (µm)
1.5	5	17
	10	8.5
	15	5.6
	20	4.1
	25	3.2
	35	2.1
	45	1.5
	55	1.1
	65	0.7
	75	0.4
	85	0.1

The simulation was based on a a-Si:H film with waveguide dimensions of, first, a 400 nm (*w*) by 400 nm (*h*) and second, a 600 nm (*w*) and 400 nm (*h*). The 600 nm (*w*) by 400 nm (*h*) dimensions was used to investigate the effect of enlarging the waveguide *w* on the loss of the interlayer slope waveguide. The transmission characteristics for both waveguide dimensions are shown in Figure 4.4.

Figure 4.5 illustrates a 2D FDTD simulation of the interlayer slope waveguide at 10° slope angle, with waveguide dimensions of 400 nm (*w*) by 400 nm (*h*). The simulation profile shows that mode propagating the slope waveguide (after being perturbed at the first slope interface) appear to be multi-mode. The introduction of transition offset to the second slope interface suppresses the higher-order mode, reconstructing it back to fundamental mode [92, 98].

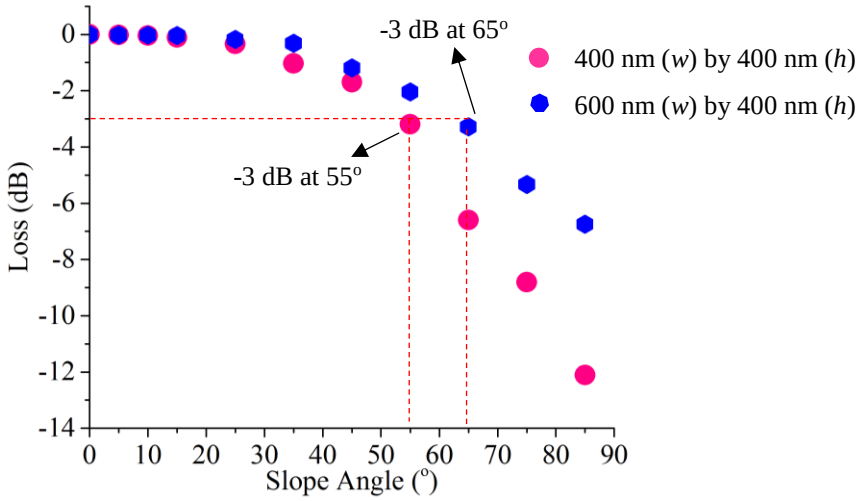


Figure 4.4 Transmission characteristics on varying the slope angle for two waveguide dimensions, at 1550 nm wavelength with TE polarized mode.

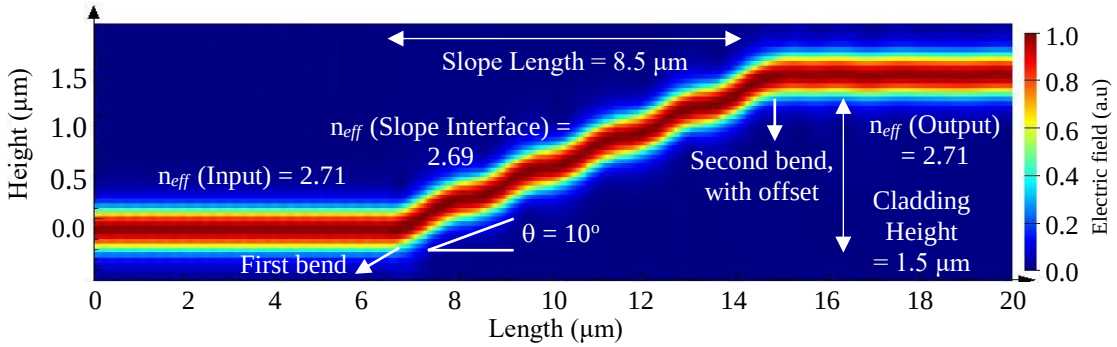


Figure 4.5 2D FDTD simulation profile for a-Si:H interlayer slope waveguide with 10° slope angle, at 1550 nm wavelength with TE polarized mode.

4.2.2.1 **Discussion**

The two graphs in Figure 4.4 show that smallest loss, below 0.1 dB, was achieved by a slope angle of 5° to 15° for the 400 nm (*w*) by 400 nm (*h*) dimensions. The smallest loss was achieved with a 5° to 20° angle for the 600 nm (*w*) by 400 nm (*h*) dimensions. The losses increased gradually with an increase in slope angle, and increased rapidly when the slope angle was made higher. Additionally, Figure 4.4 shows that the loss in the wider waveguide (600 nm (*w*) by 400 nm (*h*)) increased more slowly than in the narrower waveguide (400 nm (*w*) by 400 nm (*h*)). This suggests that the mode in the wider waveguide was largely confined within the waveguide core and was more susceptible to bend losses.

The simulation of the interlayer slope waveguide conformed to the theory of losses in waveguide bends (Chapter 3). In principle, losses in waveguide bend can be minimized by a gradual increase in the radius of the bend to allow small changes in the effective index of the mode propagating into the bend. Such a gradual increase means the mode propagating in the waveguide core can be tightly confined and will radiate less. Upon propagating along the bend, bend loss can further be minimized by a large bend radius. A large bend radius allows for a

gradual transition of rays to change direction along the bend section, preventing further radiation from the leaky mode. An abrupt change in the radius of the bend results in significant change in the direction of the ray, which induces much scattering and results in higher loss. The loss contributions are shown in Figure 4.4. The higher loss associated with the larger slope angle above 55^o is caused by the significant mode-mismatch through the bend at the slope interface.

As discussed in Chapter 3, mode propagating from a straight waveguide into the slope interface, which creates a surface perturbation, changes its direction of propagation regarding the interface curvature. This alteration changes the n_{eff} and thus the effective propagation constant (β) of the propagating mode. The change in n_{eff} induces mode-mismatch and causes the electric field of the propagated mode to become redistributed and distorted in shape. As a result, some of the field penetrates into the bottom cladding layer and is lost through radiation. The distorted mode, with evanescent field extended into the bottom cladding, continues to propagate along the waveguide on the slope, shedding its energy uniformly.

Figure 4.6 (a) to (d) shows the simulation of 2D electric field distribution of TE mode across the interlayer slope waveguide, for waveguide dimensions of 400 nm (*w*) by 400 nm (*h*). The *y*-axes represent to the *w* of the waveguide, and the z-axes show the waveguide *h*. Figure 4.6 (a) shows the 2D electric field distribution of TE mode at the input. Figure 4.6 (b), (c) and (d) show the 2D electric field distribution of TE mode at the slope interface, with a slope angle of 10^o, 25^o and 55^o, respectively. Mode distortion can be observed with the transition across Figure 4.6 (a) to (d), suggesting mode-mismatch due to phase shifting.

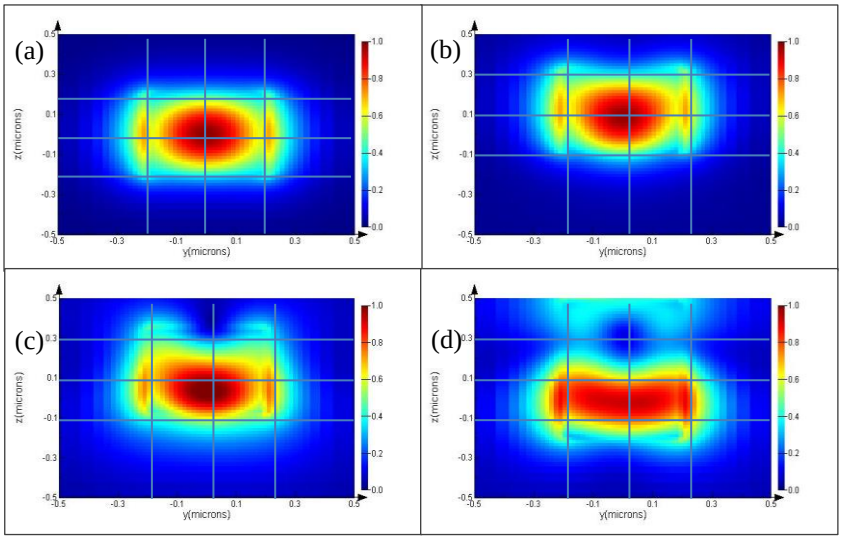


Figure 4.6 2D Electric field distribution of TE mode at: (a) Input, (b) 10^o slope interface, (c) 25^o slope interface, and (d) 55^o slope interface, at 1550 nm wavelength with TE polarized mode.

In addition, Figure 4.6 (c) and (d) show that the modes are pulled downwards to the bottom substrate. This indicates that the field of the mode travelling at the outer bend of the slope interface travels

faster, attempting to keep momentum with the field at the inner bend. But because that is not possible, part of the field of the mode decays into the bottom substrate, occurring as evanescent field. The mode continues to propagate along the waveguide on the slope by constantly shedding a fraction of optical energy. When the distorted mode encounters another bend on the upper level, it changes sign and induces further loss, as it does in an S-bend waveguide.

4.3 Modelling of Crosstalk and Isolation between Two Waveguides

This section presents the results for the investigation of the minimum cladding thickness required to isolate two waveguides placed orthogonally and in parallel on top of each other. The simulation results validated the design of the interlayer slope waveguide and verified a cladding thickness of 1.5 μm was ample to isolate the input and the output waveguides and other crossing waveguides. For all simulations reported in this section, hydrogenated amorphous silicon (a-Si:H) was used, with a refractive index (n) of 3.55 at a working wavelength of 1550 nm, with TE mode polarization.

4.3.1 Two waveguides placed orthogonally on top of each other

The schematic structure of two waveguides placed orthogonally on top of each other is shown in Figure 4.7. The device comprises bottom and top waveguides having the same dimensions, cladded with plasma-enhanced chemical vapour deposition (PECVD) silicon dioxide (SiO_2) for optical isolation. The height ($h_{cladding}$) varied from 0 nm to 1000 nm.

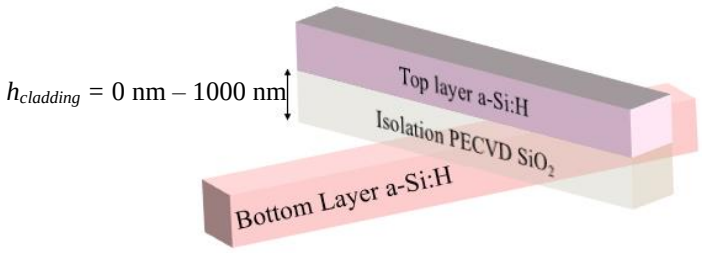


Figure 4.7 Schematic structure of an orthogonal waveguide placed on top of a straight waveguide.

The waveguide simulation was performed using Lumerical FDTD Solutions in 3D condition. Two waveguide dimensions, namely 400 nm (w) by 400 nm (h) and 1000 nm (w) by 400 nm (h) were used to investigate the minimum isolation thickness required to prevent crosstalk between two overlapping waveguides. To extract the coupled power at the output waveguide with reference to the source, three monitors were mainly used. Figure 4.8 shows the designed device in Lumerical FDTD software, indicating the positions of the three monitors.

Figure 4.9 presents the crosstalk graphs. The hypothesis of this simulation experiment was that 400 nm (w) by 400 nm (h) waveguides would require thicker cladding isolation than the 1000

nm (*w*) by 400 nm (*h*) waveguides. This is because light is less confined in the smaller waveguide than the larger waveguide. Thus, evanescent field from the smaller waveguide can easily be coupled to the neighbouring top waveguide.

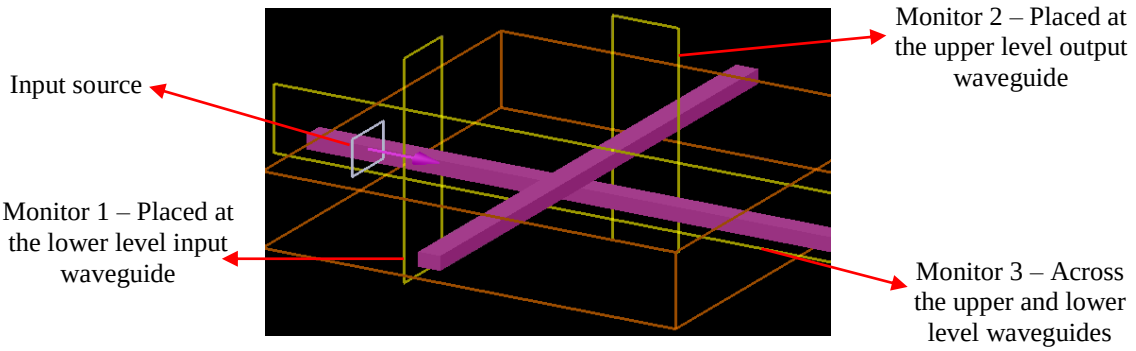


Figure 4.8 The 3D design of two waveguides placed orthogonally, visualised by Lumerical FDTD Solutions. Hydrogenated amorphous silicon (a-Si:H) was the waveguiding material.

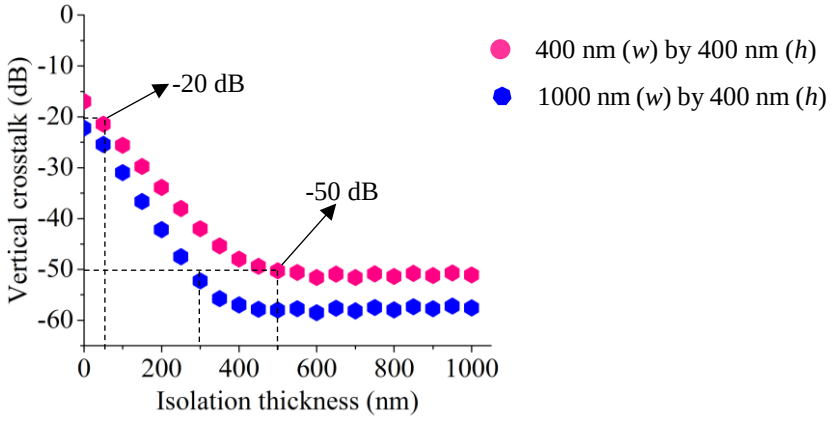


Figure 4.9 FDTD simulation of multilayer crosstalk (dB) with varying isolation thickness, for two waveguides placed orthogonally on top of each other.

4.3.1.1 **Discussion:**

The results of the simulation confirmed the hypothesis, in that the smaller waveguide (400 nm (*w*) by 400 nm (*h*)) could be more easily coupled than the larger waveguide. The two curves in Figure 4.9 show that the thickness required to isolate two waveguides placed orthogonally with -20 dB crosstalk, was 50 nm for the 400 nm (*w*) by 400 nm (*h*) dimension and 0 nm for the 1000 nm (*w*) by 400 nm (*h*) dimension. To isolate them with -50 dB crosstalk for the same waveguide dimensions would require 500 nm and 300 nm thick cladding, respectively. Table 4-2 summarizes the simulated data.

Figure 4.10 shows the 2D FDTD simulation profile for the 400 nm (*w*) by 400 nm (*h*) waveguide, illustrating the decrease in optical coupling for the orthogonal structure. Figure 4.11 shows the same behaviour for the 1000 nm (*w*) by 400 nm (*h*) waveguide. Figure 4.10 (a) to (c) and Figure 4.11 (a) to (c) present the simulation profiles across the bottom and top waveguides with varying cladding thickness (Monitor 3). Similarly, Figure 4.10 (d) to (f) and Figure 4.11

(d) to (f) present the simulation profiles of the coupled electric field at the output of the crossing waveguide, for varying cladding thicknesses (Monitor 2).

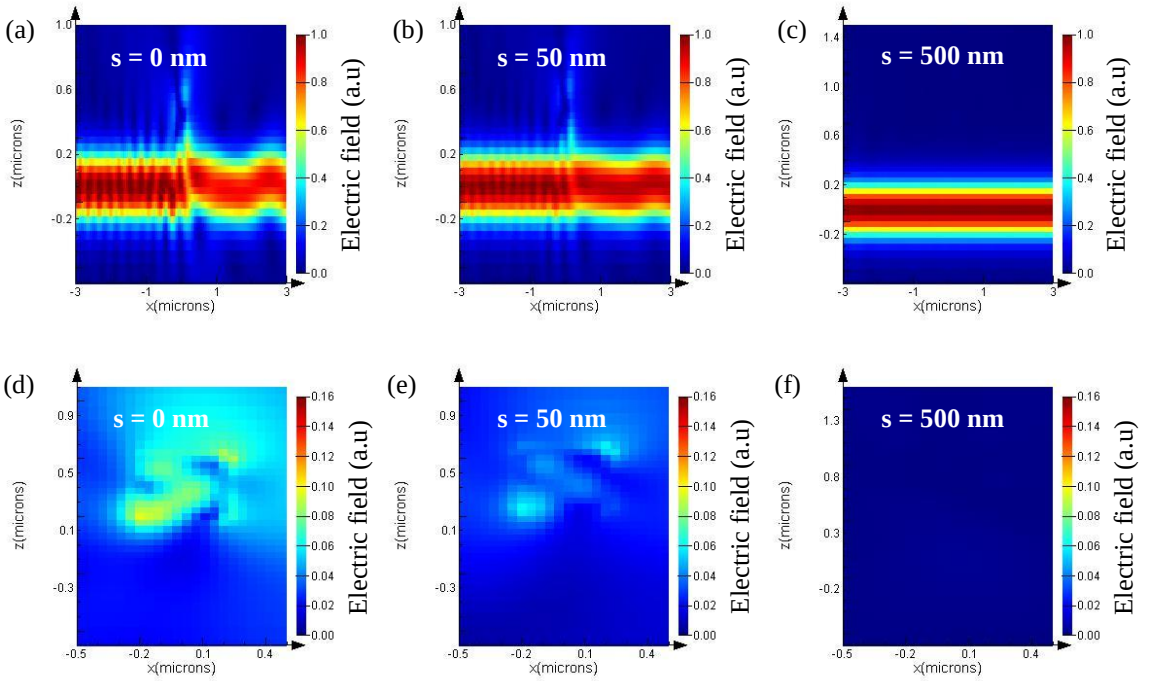


Figure 4.10 2D FDTD simulation profiles for two waveguides placed orthogonally on top of each other, for 400 nm (*w*) by 400 nm (*h*) waveguides, with varied separation (*s*), at 1550 nm wavelength with TE polarized mode. Panels (a) to (c) show the simulation profiles across the overlapping waveguides (Monitor 3), and panels (d) to (f) show the simulation profiles at the output arm of the crossing waveguide (Monitor 2).

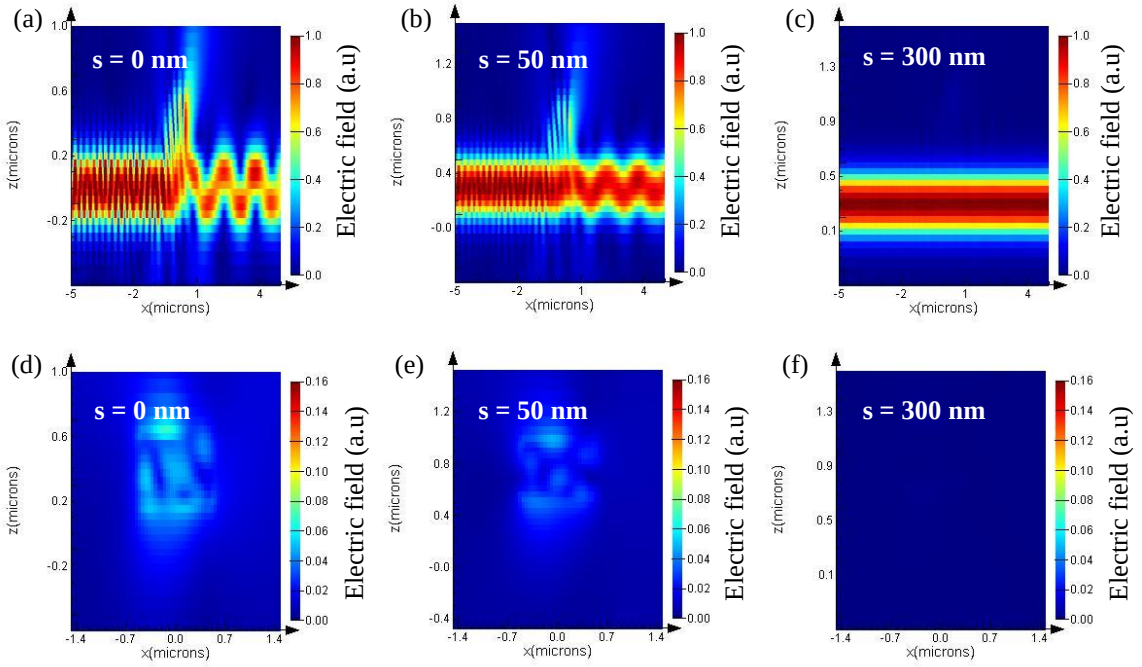


Figure 4.11 2D FDTD simulation profiles for two waveguides placed orthogonally on top of each other, for 1000 nm (*w*) by 400 nm (*h*) waveguides, with varied separation (*s*), at 1550 nm wavelength with TE polarized mode. Panels (a) to (c) show the simulation profiles across the overlapping waveguides (Monitor 3), and panels (d) to (f) show the simulation profiles at the output arm of the crossing waveguide (Monitor 2).

Table 4-2 Minimum cladding thickness (nm) required to isolate two waveguides placed in orthogonal on top of each other.

Waveguide dimensions	Cladding thickness (nm) for -20 dB crosstalk	Cladding thickness (nm) for -50 dB crosstalk
400 nm (*w*) by 400 nm (*h*)	50	500
1000 nm (*w*) by 400 nm (*h*)	0	300

As observed from the simulation profiles, the optical mode is easily coupled when two waveguides are placed in contact with each other. This is especially true for the 400 nm (*w*) by 400 nm (*h*) crossing waveguides with a separation of 0 nm, as shown in Figure 4.10 (a) and (d). This result was expected due to the physical dimensions of the waveguides, which easily allow the leaking of energy.

As the separation was enlarged to 50 nm, the intensity of the electric field of the coupled power faded, indicating that the two waveguides were isolated with approximately -21 dB, as shown in Figure 4.10 (b) and (e). Increasing the cladding thickness to 500 nm resulted in total isolation of the two crossing waveguides, as shown in Figure 4.10 (c) and (f). In a large waveguide, such as the 1000 nm (*w*) by 400 nm (*h*) dimension, optical mode confinement was increased relative to the 400 nm (*w*) by 400 nm (*h*) waveguide. Figure 4.12 shows the simulation of 2D FDTD mode profile for the 1000 nm (*w*) by 400 nm (*h*) waveguide dimensions, in TE mode polarization.

In a large waveguide, such as the 1000 nm (*w*) by 400 nm (*h*) dimension, optical mode confinement was increased relative to the 400 nm (*w*) by 400 nm (*h*) waveguide. Figure 4.12 shows the simulation of 2D FDTD mode profile for the 1000 nm (*w*) by 400 nm (*h*) waveguide dimensions, in TE mode polarization.

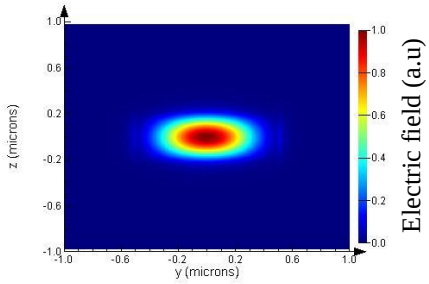


Figure 4.12 FDTD simulation of 2D mode profiles for waveguide dimensions of 1000 nm (*w*) by 400 nm (*h*), at 1550 nm wavelength for TE mode polarization.

Thus, it was expected that two waveguides of 1000 nm (*w*) by 400 nm (*h*) each, placed perpendicular to each other, would easily be isolated. These waveguides would require only thin cladding isolation compared to the 400 nm (*w*) by 400 nm (*h*) sized waveguides. This expectation was confirmed by the simulation and the results are shown in Figure 4.11 (a) to (f).

However, the mode observed in Figure 4.11 (a) shows an ambiguity. It seems the mode from the bottom waveguide was being coupled to the top waveguide, when in fact the two waveguides were isolated with approximately -22 dB crosstalk. The coupling of the optical mode was due to the bottom waveguide encountering a high refractive-index waveguide at the top, having the same effective propagation constants (β). The power coupled was insignificant because the width of the waveguides (1000nm) was insufficient to transfer or accept less than half of the optical mode energy. Hence, only a little light was coupled to the top waveguide, which later became coupled back down.

Differently to the 400 nm (w) by 400 nm (h) crossing waveguides with separation of 0 nm. Here, the waveguide width (400 nm) was sufficient to transfer at least half the optical mode energy, with sufficient electric field becoming coupled to the top waveguide, resulting in -16.9 dB crosstalk.

The trend in the simulation results are as expected. As discussed in Chapter 3, waveguides with smaller dimensions tend to radiate optical energy out of the waveguide core more easily than larger waveguides. Effectively, this increases the presence of evanescent field in the surrounding cladding layer, which results in higher potential for optical energy to be transferred to the neighbouring waveguide. This requires the two waveguides to be placed in close proximity to each other.

Referring to Figure 3.7, the graph indicates that waveguides with 400 nm core thickness can contain 93.2% optical power, with the remaining 6.8% of the optical power occurring as evanescent field. As the waveguide dimensions become larger to 1000 nm (w) by 400 nm (h), a higher fraction of optical power can be contained and carried inside the waveguide core, with only 1.1% of optical power leaking out into the cladding layer. Effectively, this reduces the possibility for the coupling of optical power to the next neighbouring waveguide.

Additionally, the coupling of optical power from one waveguide to the closest neighbouring waveguide is determined by the distance separating the two waveguides, as shown in Figure 4.10 and 4.11 (a) to (f). The parameter that defines the coupling capacity is referred to as the coupling coefficient, κ, (m^{-1}). As discussed in Chapter 3, two waveguides having the same n_{eff} and hence the same β placed a certain distance apart, would impose some value of κ. The value of κ gives an indication of the ability of a waveguide to transfer its optical energy to its neighbouring waveguide over a certain separation length. The relationship between κ with varying waveguide separation (s) is illustrated in Figure 3.12. The curves in Figure 3.12 show that the 400 nm (w) by 400 nm (h) waveguide has a higher κ than the 1000 nm (w) by 400 nm (h) waveguide.

This results implies that the smaller waveguides tend to couple more easily than bigger waveguides, and thus would need larger cladding separation to isolate the two waveguides and

preventing crosstalk. Table 4-3 summarizes the properties of the two waveguides, obtained by calculation.

Table 4-3 Calculated properties of two waveguide sizes.

Parameters	**400 nm (*w*) by 400 nm (*h*)**	**1000 nm (*w*) by 400 nm (*h*)**
Effective index, n_{eff}	2.67	3.16
Effective propagation constant, β (m^{-1})	1.08 x 10^7	1.28 x 10^7
Confinement factor, Γ (%)	93.2	98.9
Coupling coefficient, κ (m^{-1}) with s = 50 nm	1.38 x 10^6	6.16 x 10^5

4.3.2 Two waveguides in parallel on top of the each other

This section presents the crosstalk simulation for two waveguides placed parallel to each other, with fixed overlapping lengths of 15 μm, and with varying cladding thickness of 0 nm to 1000 nm. The schematic structure of the two waveguides in parallel is shown in Figure 4.13. Two waveguide dimensions, 400 nm (*w*) by 400 nm (*h*) and 1000 nm (*w*) by 400 nm (*h*), were simulated to investigate the minimum isolation thickness required to prevent crosstalk between the two overlapping waveguides. In this simulation experiment, three monitors were mainly used to extract the coupled power with reference to the input source. Figure 4.14 shows the designed device in Lumerical FDTD software, indicating the positions of the three monitors.

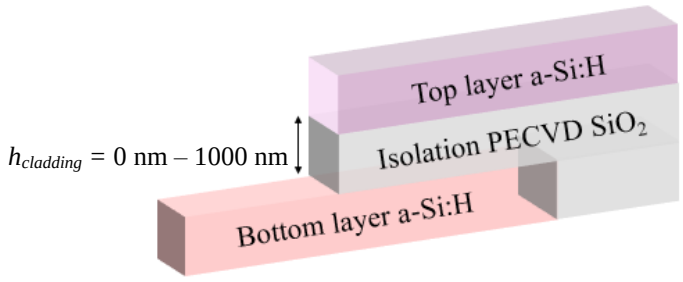


Figure 4.13 Schematic structure of a waveguide placed in parallel on top of a straight waveguide.

Similar to the previous simulation experiment, it was assumed that the 400 nm (*w*) by 400 nm (*h*) waveguides would require thicker isolation cladding than the 1000 nm (*w*) by 400 nm (*h*) waveguides. This was because mode propagating in the larger waveguide is tightly confined without radiating too much evanescent field, compared to the smaller waveguide.

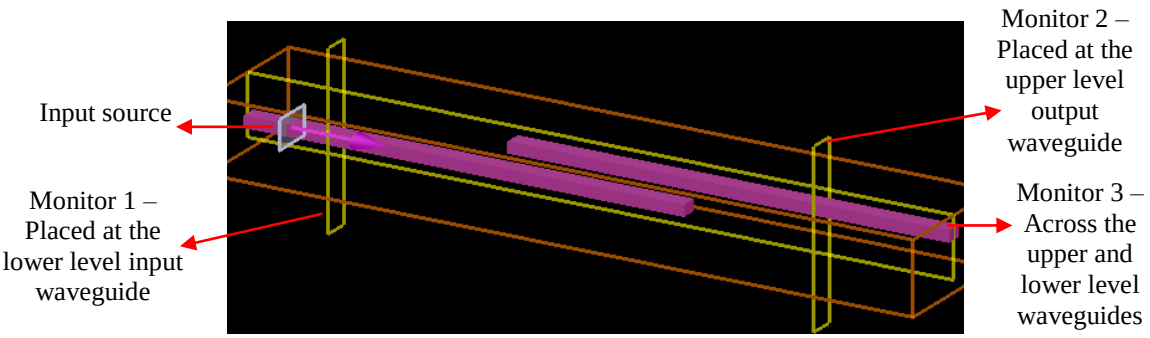


Figure 4.14 3D design of two waveguides placed in parallel to each other, visualised in Lumerical FDTD Solutions. Hydrogenated amorphous silicon (a-Si:H) was the waveguiding material.

Additionally, given how fields interact sinusoidally to transfer full optical energy to the neighbouring waveguide over a certain coupling length (L_π), it was expected that crosstalk values at the output arm would fluctuate against varied cladding separation. The crosstalk fluctuation was anticipated to occur continuously until the two overlapping waveguides were sufficiently isolated. It is important to note that the value of the L_π increases as the separation between the two waveguides increases, as presented in Table 3-2 (Chapter 3). With the designed overlapping length of 15 μm, the optical mode which was coupled up could continue to fully propagate at the output arm, yielding high crosstalk, or could be coupled back down and continue to propagate along the bottom waveguide to give 20 dB crosstalk isolation. In this simulation, the overlapping length was designed at a fixed length of 15 μm, hence the only variation investigated was the isolation thickness. Figure 4.15 presents the crosstalk graphs.

4.3.2.1 **Discussion**

The results of the simulation supported the theory, with larger waveguides requiring less cladding isolation than smaller waveguides. The two graphs in Figure 4.15 show that the 1000 nm (w) by 400 nm (h) waveguides were isolated more quickly than the 400 nm (w) by 400 nm (h) waveguides. This was as expected, because mode in the larger waveguides was more confined than in the smaller waveguides. The graphs show that the cladding thickness required to isolate the 400 nm (w) by 400 nm (h) waveguides is 550 nm, whereas for the 1000 nm (w) by 400 nm (h) waveguides it was 450 nm. Table 4-4 summarizes the simulated data.

Crosstalk values fluctuate with the increase in waveguide separation (s).It was anticipated that the fluctuations would occur for some values of cladding thicknesses, until the two overlapping waveguides were fully isolated. Figure 4.16 and Figure 4.17, (a) to (e), present the simulation profiles showing the coupling of the mode going in periodic with varying cladding thicknesses (Monitor 3). Figure 4.16 shows the simulation for the 400 nm (w) by 400 nm (h) waveguides, and Figure 4.17 shows the simulation for the 1000 nm (w) by 400 nm (h) waveguides.

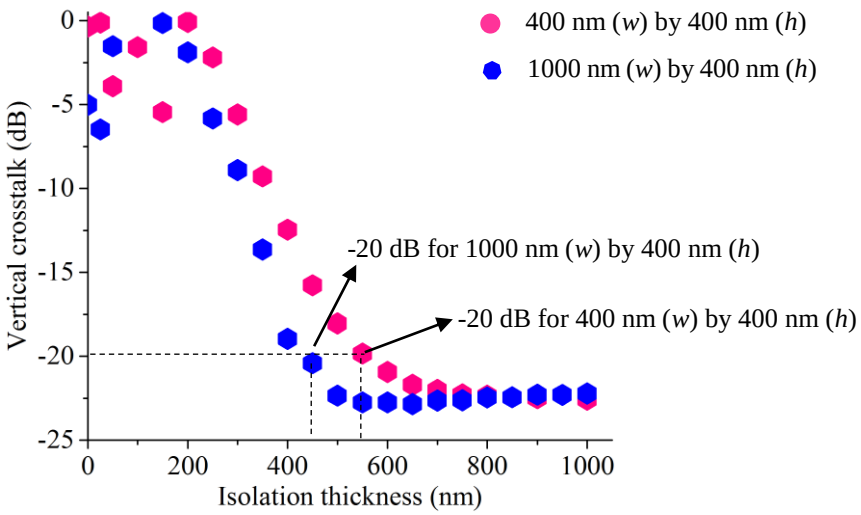


Figure 4.15 FDTD simulation of multilayer crosstalk (dB) with varying isolation thickness (nm), for two waveguides placed in parallel on top of each other, at 1550 nm wavelength with TE polarized mode.

Table 4-4 Minimum cladding thickness (nm) required to isolate two waveguides placed in parallel on top of each other.

Waveguide dimensions	Cladding thickness (nm) for -20 dB crosstalk
400 nm (*w*) by 400 nm (*h*)	550
1000 nm (*w*) by 400 nm (*h*)	450

As observed from the simulation profiles, the coupling of the optical mode occurred periodically over the 15-µm overlapping length. This was as expected and conformed to the theory (Section 3.6, Chapter 3). The length which the coupled mode continued to travel before it was coupled back down again depended strongly on the separation between the bottom and top waveguides and the dimensions of the waveguides. The L_π observed in the simulations closely correlated with the calculated L_π as shown in Table 3-2. For example, the L_π to transfer full energy of the mode was shorter for the 400 nm (*w*) by 400 nm (*h*) waveguides than for the 1000 nm (*w*) by 400 nm (*h*) waveguides. The isolation thickness was the same for both, at 50 nm, as shown in Figure 4.16 (b) and Figure 4.17 (a).

As discussed at the start of this section, depending on the overlapping length in the design of the crosstalk waveguides, the optical mode that coupled upward continued to fully propagate at the output arm, causing a strong crosstalk signal. Alternatively, it coupled back down and continued to propagate along the bottom waveguide to give sufficient -20 dB isolation.

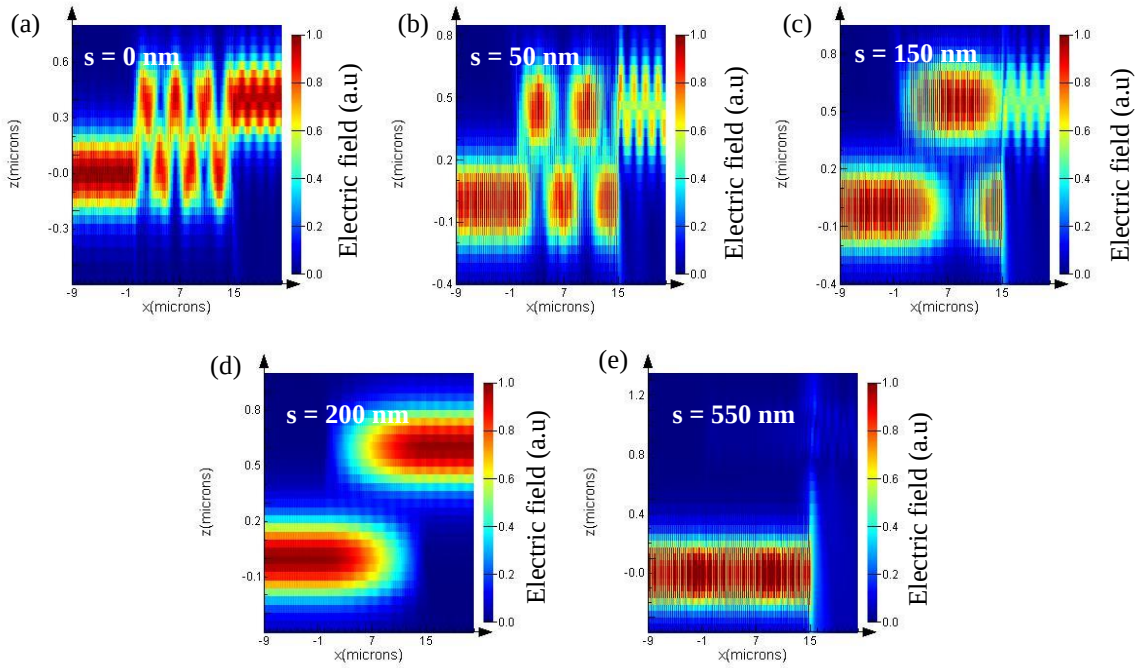


Figure 4.16 (a) to (e) shows the 2D FDTD simulation profiles for two waveguides placed in parallel on top of each other, for 400 nm (*w*) by 400 nm (*h*) sized waveguides with varied separation (*s*), at 1550 nm wavelength with TE polarized mode.

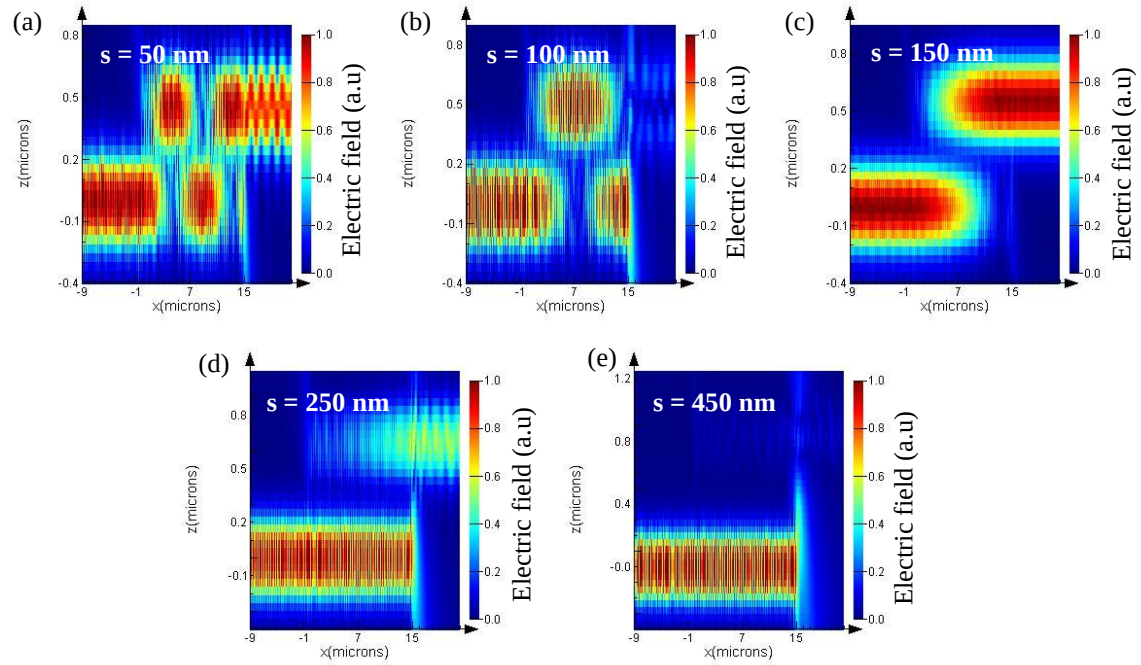


Figure 4.17 (a) to (e) shows the FDTD simulation profiles for two waveguides placed in parallel on top of each other, for 1000 nm (*w*) by 400 nm (*h*) sized waveguides with varied separation (*s*), at 1550 nm wavelength with TE polarized mode.

In this simulation, -50 dB crosstalk could not be achieved because the bottom waveguide was abruptly terminated. Light propagating towards the end of the bottom waveguide core was scattered out and radiated into the cladding layer, as shown in Figures 4.16 (e) and 4.17 (e). Because the output monitor (Monitor 2) was placed close to the overlapping structure, it easily collected the radiated light. This positioning increased the transmission at Monitor 2, thus increasing the value of the crosstalk. One way to solve this is by extending the output arm with

an S-bend structure to isolate the monitor. However, it is intended to standardise both crosstalk structures of Figure 4.7 and 4.13, thus the S-bend structure was not introduced in this simulation work, as it could lead to an additional cause of optical loss.

4.4 The Design of the Fly-Over Bridge Interconnect

With the interlayer slope waveguide and the crosstalk structures modelled and simulated, an extended structure based on the slope platform was designed and fabricated. The device was named the "fly-over slope waveguide". Figure 4.18 shows the schematic structure of the device. The aim of this simulation experiment was to investigate the interlayer slope waveguide structure to be applied in a real multilayer interconnect circuitry. In this simulation, a 10° slope angle was used, as the platform offers a balance between low loss and device compactness. Waveguide dimensions of 400 nm (w) by 400 nm (h) were used in this simulation with a-Si:H as the waveguiding material.

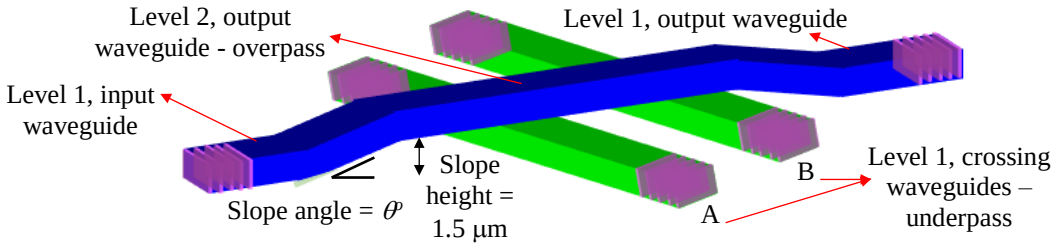


Figure 4.18 Schematic design of the fly-over waveguide coupler.

Similar to the previous simulation experiments, Lumerical FDTD Solutions in 3D condition was used in modelling the device. The slope platform had the following parameters: 10° inclination angle, 1.5 µm slope height, and corresponding calculated slope length of 8.5 µm. Two waveguides were placed below the overpass structure, lying on the same plane as the lower level input and output waveguides. These waveguides are referred to as "underpass waveguides". In this simulation experiment, the distance z of waveguide A and waveguide B to the waveguide on the slope were varied. The variations of the z-direction were made in accordance to the simulation experiment of Section 4.3.1, for consistency. Varying the vertical distance z would result in change of the horizontal distance in the x-direction. The corresponding calculated values of x were 2.5 µm, 2.8 µm, 3.4 µm, 5.1 µm and 7.9 µm. The variations of the x values (together with the z values) would then be used to investigate the susceptibility of the orthogonal waveguide either to couple or isolate itself with the waveguide on the slope. Figure 4.19 illustrates the schematic of the closed-up structure.

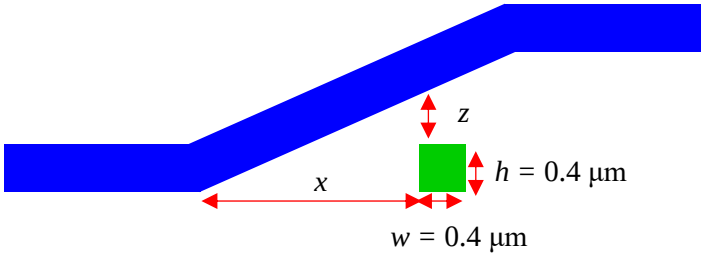


Figure 4.19 Schematic of the closed up structure.

Table 4-5 tabulates the calculated values of *x* with the corresponding values of *z*, for the 10° slope angle. Figure 4.20 (a) to (d) shows the 2D simulation profiles of the fly-over slope waveguide, with two waveguides placed below the device, for *x* of (a) 2.5 µm, (b) 2.8 µm, (c) 3.4 µm, and (d) 5.1 µm.

Table 4-5 Calculated values of distance *x* with the corresponding values of distance *z*, with a 10° slope angle.

Slope angle (°)	Distance *x* (µm)	Distance *z* (µm)
10	2.5	0.05
	2.8	0.1
	3.4	0.2
	5.1	0.5
	7.9	1.0

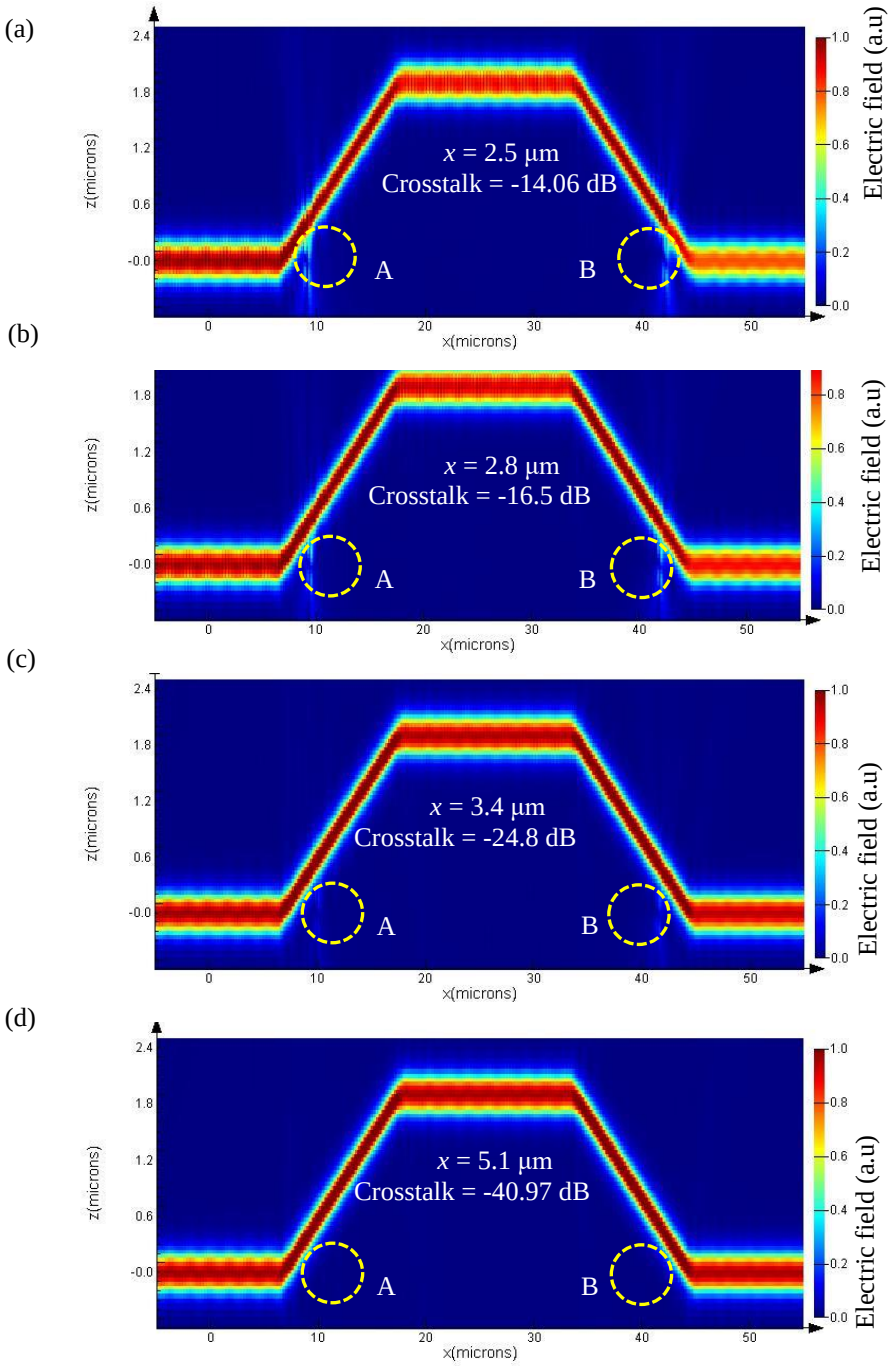


Figure 4.20 2D FDTD simulation profiles of the fly-over slope waveguide coupler, with two crossing waveguides placed below the 10° slope angle, for *x* of: (a) 2.5 µm, (b) 2.8 µm, (c) 3.4 µm and (d) 5.1 µm.

Also included in this section is a simulation experiment to investigate the effect of varying the slope angle to the crosstalk of the orthogonal waveguide placed next to the slope interface. In the modelling, slope angles equal to 5º and 25º were used. To be consistent with the 10º slope angle simulation experiment, the underpass waveguides were placed at the same *z* distance to the waveguide on the slope. The *z* values are 0.05 µm, 0.1 µm, 0.2 µm, 0.5 µm and 1 µm. The corresponding *x* values were then calculated using Pythagoras' theorem. Table 4-6 tabulates the calculated values of *x* with the corresponding values of *z*, for the two slope angles, 5º and 25º.

Table 4-6 Calculated values of distance *x* with the corresponding values of distance *z*, for a 5º and 25º slope angle.

Common distance *z* (µm)	**Slope angle (º)**	**Distance *x* (µm)**	**Slope angle (º)**	**Distance *x* (µm)**
0.05	5	5.1	25	0.96
0.1		5.7		1.1
0.2		6.8		1.3
0.5		10.2		1.9
1.0		16.0		3.0

Figure 4.21 (a) and (b) shows the 2D simulation profiles of the fly-over slope waveguide, with an orthogonal waveguides placed next to the transition region of the slope interface, for (a) 5º slope angle with *x* equals to 5.1 µm, and (b) 25º slope angle with *x* equals to 0.96 µm, for the same value of *z* distance of 0.05 µm.

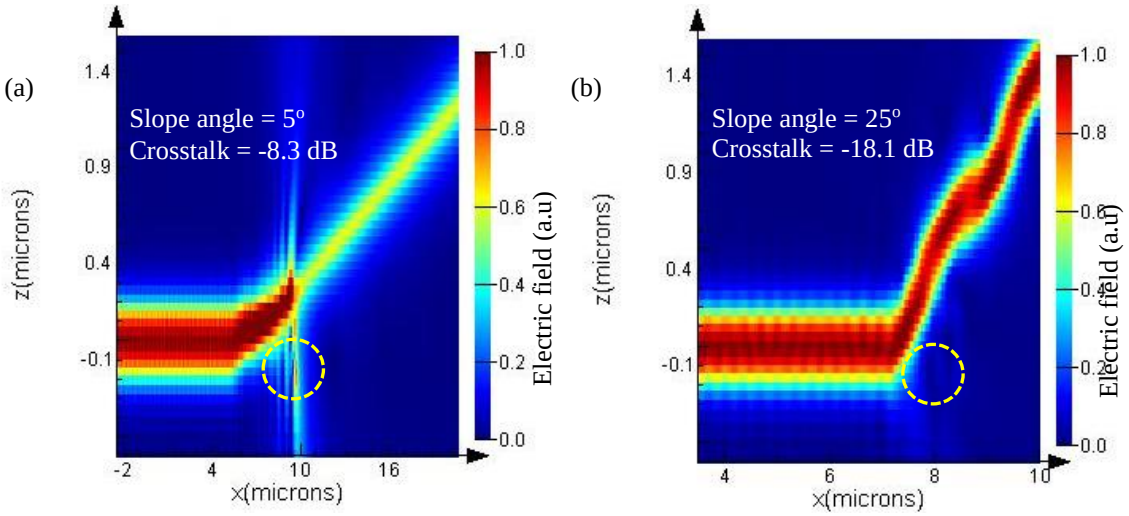


Figure 4.21 2D FDTD simulation profiles of the fly-over slope waveguide coupler, with a crossing waveguide placed below the (a) 5º slope angle, and (b) 25º slope angle, for *x* of 5.1 µm and 0.96 µm, respectively. The z distance for both (a) and (b) was kept constant at 0.05 µm.

From the simulation, it was observed that the values of crosstalk differs for both cases. The crosstalk for the 5º slope angle is 9.8 dB higher than the 25º slope angle. The trend in the simulation experiment also shows that the coupling decreases as the slope angle is made higher, such that in the 5º (-8.3 dB crosstalk), 10º (-14.06 dB crosstalk) and 25º (-18.1 dB crosstalk) slope angles, for the same value of *z* distance equal to 0.05 µm.

It is suggested that orthogonal waveguides which are placed next to the slope interface are less affected by the scattered mode due to the transition region of the different slope angles. This is because the scattered field is mainly occurring on the lower side of the bottom SiO_2 cladding. Thus, orthogonal waveguides placed next to the slope interface would mainly be affected by the evanescent field of the mode propagating along the waveguide on the slope. The crosstalk for the 5° slope angle is higher due to the evanescent interaction region between the orthogonal waveguide and the waveguide on the slope, in the *z*-direction, is closer than for the 25° slope angle. With the waveguide on the slope for the 25° slope angle being elevated, the extended field propagating on the slope is quite far from the bottom orthogonal waveguide.

4.4.1 Discussion

The aim of this simulation experiment was to investigate the capacity of the fly-over waveguide, an extended version of the interlayer slope waveguide, to function as a real 3D interconnect, with the presence of crossing waveguides placed beneath the slope structure. The crossing waveguides were placed on the same plane as the lower level input and output waveguides, with varied distance to the slope interface, labelled as *x*. This configuration enables the fly-over slope waveguide to be characterized in terms of its ability to isolate itself or to be susceptible to the occurrence of crosstalk, in the presence of any crossing waveguides placed below the slope structure.

As discussed in Section 3.6 (Chapter 3), the occurrence of crosstalk or optical coupling depends strongly on the proximity between two waveguides. It also requires that both waveguides have the same values of n_{eff} and β. Although, under certain conditions, this may not be necessary [101]. Two waveguides placed very close to each other would result in high crosstalk. This is observed in Figure 4.20 (a), where optical mode propagating on the slope becomes coupled to the underlying waveguides as it encounters the high-index materials. This creates crosstalk of approximately -14.06 dB at the output of both underlying waveguides, A and B. This results in the fly-over waveguide experiencing significant loss in the transmission of approximately 2.97 dB. As the underlying waveguides are placed further away from the slope interfaces and the waveguide on the slope, the coupling decreases, as shown in the transition of the simulation profiles. Table 4-7 presents the crosstalk values with varying distances for *x* (μm), at a fixed 10° slope angle.

Table 4-7 Crosstalk values at the output of the underlying waveguide, A, with varied separation in the *x*-direction, for 10° slope angle.

Slope angle (°)	Distance *x* (μm)	Distance *z* (μm)	Crosstalk (dB)
10	2.5	0.05	-14.06
	2.8	0.1	-16.5
	3.4	0.2	-24.8
	5.1	0.5	-40.97
	7.9	1.0	-40.83

The crosstalk values obtained in this simulation were slightly higher than the crosstalk values shown in Figure 4.9. In analysing the structures, it was expected that the coupling in the simulation would be higher. This is because the characteristics of the mode propagating along the slope interface differ from those of the mode propagating along a straight waveguide. As discussed in Sections 3.3 and 3.4 (Chapter 3), optical mode travelling along a bend structure contains substantial leaky mode at the cladding of the outer bend of the slope interface. Subsequently, the mode gets disturbed inducing to the occurrence of higher-order mode. Part of the field of the higher-order mode propagating along the waveguide on the slope decays into the cladding. The presence of vast evanescent field at the sides where the crossing waveguides are placed results in increased crosstalk at the output of the crossing waveguides, A and B. Figure 4.22 presents the graphs of crosstalk from structures in Figures 4.7 and 4.18, with varying distance *z* (μm), for comparison.

Further, simulations using 5° and 25° slope angles were performed to investigate the effect of varying the inclination angle of the slope structure on the crosstalk; the remaining parameters were kept the same.

Table 4-8 Crosstalk values at the output of the underlying waveguide, A, with varied separation in the *x*-direction, for 5° and 25° slope angle.

Distance *z* (μm)	**Slope angle (°)**	**Distance *x* (μm)**	**Crosstalk (dB)**	**Slope angle (°)**	**Distance *x* (μm)**	**Crosstalk (dB)**
0.05	5	5.1	-8.3	25	0.96	-18.1
0.1		5.7	-10.59		1.1	-29.82
0.2		6.8	-14.83		1.3	-32.15
0.5		10.2	-25.84		1.9	-40.08
1.0		16.0	-26.08		3.0	-41.32

Figure 4.4 shows an increase in the loss as the slope angles are increased. This suggests higher fraction of scattered field at the bottom cladding of the slope junction. Thus, it was expected for the crosstalk to be higher in higher slope angle, such as for the 25° compared to the 5°. However, the simulation results tabulated in Table 4-8 shows the opposite. The 5° slope angle incurred higher crosstalk compared to the 25° slope angle.

A possible explanation is that the evanescent field of the higher-order mode propagating along the waveguide on the slope, after it becomes distorted at the slope interface, travels in the direction of the *y*-axis. This is because the mode propagating is in TE mode polarization and the electric field of TE mode travels perpendicular to the plane of incidence (see Section 3.2.2 of Chapter 3). Increasing the slope angle increases the amount of scattered field due to the substantial change in the direction of propagation. But the evanescent field occurs mainly at the sidewalls of the waveguide travelling up the slope. Hence, with the angle being elevated, the extended field of the higher-order mode is quite far from the bottom crossing waveguide, with reference to the *z*-direction. Therefore, it does not couple with waveguides A or B easily. On the contrary, to the lower slope angle of 5°, the extended field of the higher-order mode travels

in close proximity to the underlying waveguide, with reference to the *z*-direction. Thus, coupling is highly likely to happen which results in the high crosstalk shown in Figure 4.23. Also, total isolation of approximately -50 dB can be achieved from the straight waveguide structure but not from the slope waveguide structures. This could be due to the radiated field in the cladding being coupled by the crossing waveguides, thus increasing the transmission or the crosstalk [101].

Figure 4.23 presents the crosstalk for the different slope angles with varying distance *z* (μm). Crosstalk from the straight waveguide structures, placed orthogonally to each other, is also shown in the graph for comparison. Note that the graphs are plotted with varying *z* instead *x*. This is to easily compare with the results from two straight waveguides placed orthogonally on top of each other, as shown in Figure 4.9.

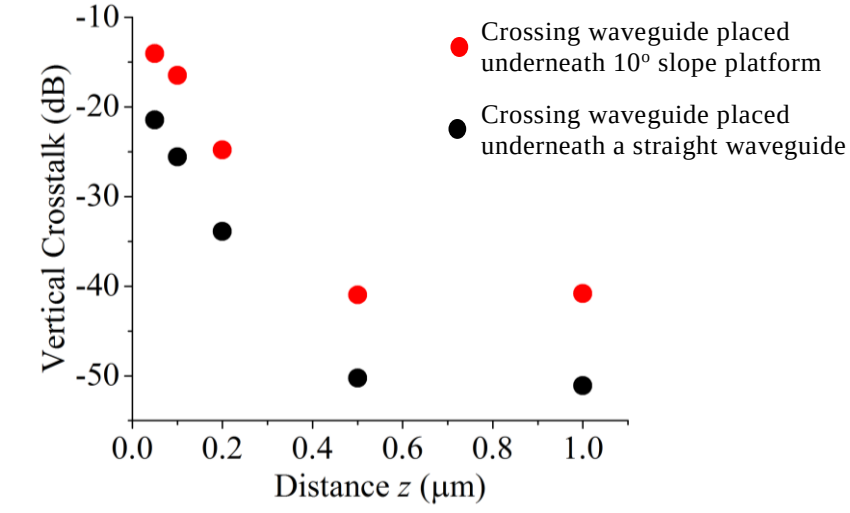


Figure 4.22 Figure 4.22 FDTD simulation of multilayer crosstalk (dB) for (a) a crossing waveguide placed underneath the 10° slope platform, and (b) crossing waveguide placed underneath a straight waveguide, with varying distance *z* (μm).

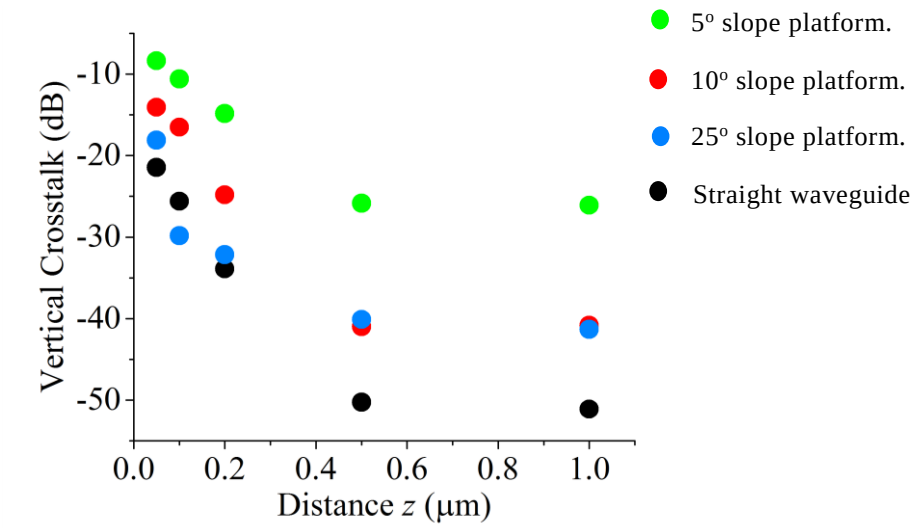


Figure 4.23 FDTD simulation of multilayer crosstalk (dB) for crossing waveguide placed underneath: (a) 5° slope platform, (b) 10° slope platform, (c) 25° slope platform and (d) a straight waveguide, with varying distance *z* (μm).

4.5 Summary

The simulation work in this chapter started with the determination of waveguide dimensions for single-mode and multi-mode waveguides. Core thickness (*h*) of 400 nm with waveguide widths (*w*) equal to 400 nm and 600 nm were chosen for the fabrication of the HWCVD a-Si:H interlayer slope waveguide. These parameters were preferred based on the simulation where waveguide dimensions of 400 nm (*w*) by 400 nm (*h*) strongly support fundamental TE_0 and TM_0 modes. At these dimensions, the higher-order mode TE_1 is present but weakly supported. The TE_1 continue to be weakly supported until *w* was made larger than 650 nm. Also, the simulation showed that TE_0 has higher n_{eff} than TM_0 and TE_1, indicating that the mode contained higher optical power than the other two modes.

Simulation to investigate the effect of varying the inclination angle of the interlayer slope waveguide was performed. The simulation showed that the lowest slope loss for angles between 5° and 15° yielded loss below 0.1 dB. The loss increased as the angle increased, due to significant mode-mismatch at the bend. A compromise in choosing a low-loss structure and device compactness is necessary. The 5° slope angle may give the lowest slope loss but requires a lengthy slope structure. The 45° slope angle is shorter but gives a loss of 3dB. Thus, slope angles between 10° and 15° were chosen for the fabrication of the 3D slope couplers.

Isolating at least 20 dB for two waveguides placed in perpendicular and in parallel on top of each other, required cladding separation of 50 nm and 550 nm, respectively for 400 nm (*w*) by 400 nm (*h*) waveguides. The cladding thickness required to isolate larger waveguides, having dimensions of 1000 nm (*w*) by 400 nm (*h*), decreased due to mode being well confined in the guiding core. The simulated crosstalk values corresponding to the varying cladding thicknesses were used as a guideline in fabricated the crosstalk 3D devices. In this work, crosstalk with two waveguides placed in perpendicular on top of each other was fabricated. This was because 3D SiP circuitry is concerned with crossing waveguide structure.

Furthermore, the modelling of the fly-over slope waveguide was performed. The slope angle was 10° with a slope height of 1.5 μm and corresponding slope length of 8.5 μm. Two crossing waveguides were placed below the slope structure. The simulation experiment was conducted to investigate the characteristics of the fly-over slope waveguide when used as a real 3D coupler. The simulation results conformed to the crosstalk simulation results, where 20 dB isolation crosstalk was achieved when the separation of the waveguides in the *z*-direction was larger than 1μm. Meanwhile, in isolating the orthogonal waveguide from the slope interface in the *x*-direction for crosstalk larger than -25 dB, require *x* values greater than 10 μm for the 5° slope angle, 3.4 μm for the 10° slope angle and 1 μm for the 25° slope angle. The device structure was replicated for the fabrication of the fly-over slope interconnect.

Chapter 5 Fabrication and Characterization of the Interlayer Slope Waveguide

5.1 Introduction

This chapter describes the sequential fabrication process to develop the interlayer slope waveguide. The description of the device development starts with a brief explanation about the mask design using L-Edit software, for both optical and electron-beam (e-beam) masks. This is followed by a description of the fabrication process flow including the tools and recipe used. Then, the characterisation and analysis of the device is thoroughly explained and discussed. The details of the fabrication recipe appear in Appendix A. Descriptions of the fabrication tools and characterisation techniques appear in Appendix B.

5.2 Mask Design

This section briefly explain the structural design of the optical and e-beam masks used to fabricate the slope platform and the waveguides. The mask designs were created using a two-dimensional (2D) vector drawing tool, L-Edit. The optical mask was mainly used to pattern large structures, whereas the e-beam mask was used to pattern sub-micron waveguide structures including the grating couplers.

The interlayer slope waveguide is characterized in terms of loss in dB per slope. Thus, in characterizing the interlayer slope waveguide, many slopes are required to be fabricated as a platform for the interlayer waveguide. The optical mask is designed with multiple bars that are used to define the slopes structure, shown in Figure 5.1. This designed structure comprised one cell (Cell 1), which was the first layer to be fabricated.

Figure 5.1 Schematic diagram of the optical mask design illustrating the multiple bars used to define the slope platform.

Positive photoresist, S1813, was used to transfer the pattern from the optical mask. In performing optical lithography, the exposed part of S1813 photoresist that is exposed to UV light becomes weakened on radiation and is dissolved during development. This produces structures shown in Figure 5.2, after the process of wet etching. Figure 5.2 illustrates the etched slope profiles for (a) a 1 slope platform, (b) 2 slopes platform, (c) 3 slopes platform, (d) 4 slopes platform, and (e) 5 slopes platform.

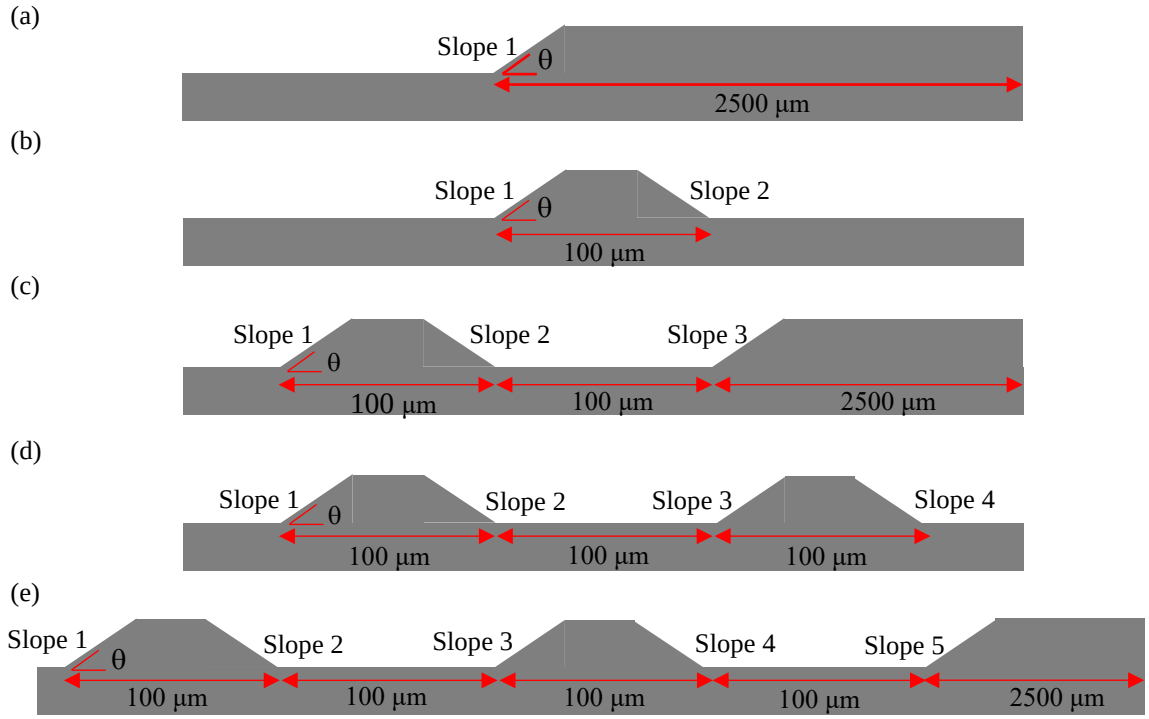


Figure 5.2 Schematic diagrams of cross-sectional views of the slope platform after wet etching, with pattern transferred using the optical mask.

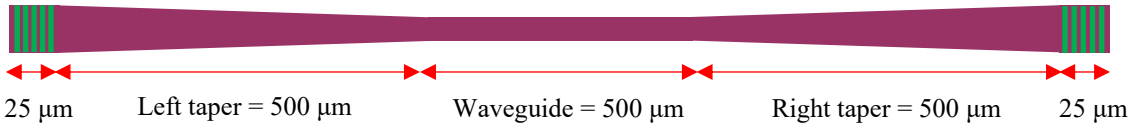


Figure 5.3 Schematic diagram of the waveguide structure.

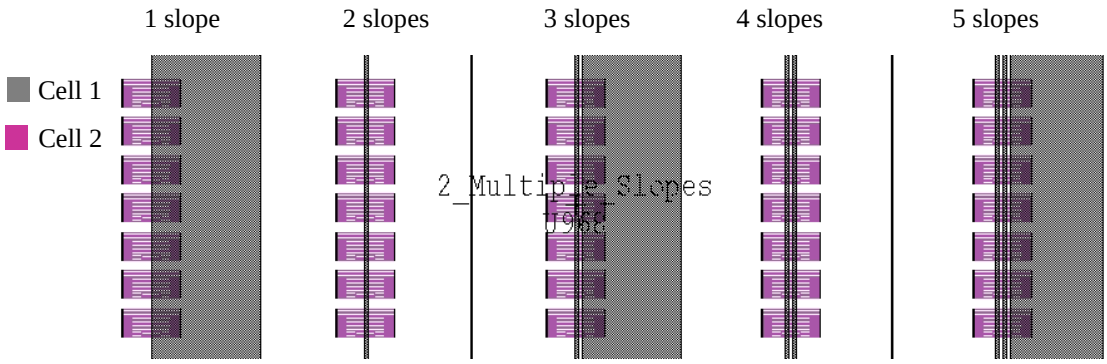


Figure 5.4 Mask design drawn in L-Edit software illustrating the design of the waveguide structures overlapping with the multiple bars.

Having used the optical mask to produce the slope platform, the e-beam mask was then used to generate the waveguide structures. Figure 5.3 illustrates the schematic drawing of the waveguide containing tapers and gratings attached at both ends of the waveguide. This made up the second cell (Cell 2). Here, the total length of the waveguide including the tapers and the gratings was 1550 μm. Then, the drawn waveguide structure, Cell 2, was placed overlapping with Cell 1, with the centred waveguide located in the middle of multiple bars, as shown in Figure 5.4.

5.3 Device Fabrication

This section described the details of the fabrication process for making the interlayer slope waveguide. The steps of the fabrication process are illustrated in Figure 5.5 (a) to (l).

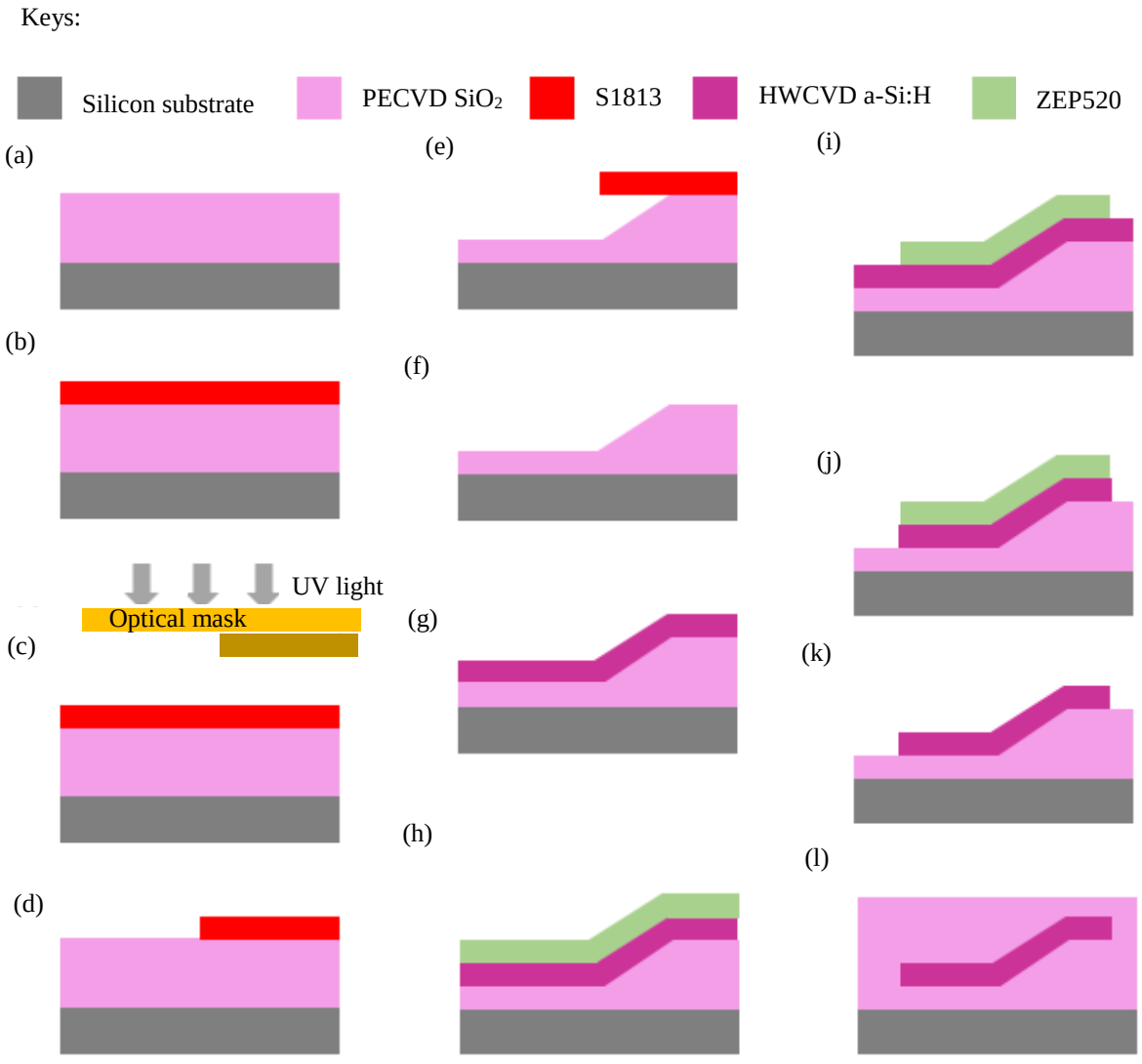


Figure 5.5 Fabrication steps for making the interlayer slope waveguide.

Device fabrication started with plasma-enhanced chemical vapour deposition (PECVD) deposition with 4.5 μm thick silicon dioxide (SiO_2) film at 350ºC on a 6" silicon wafer. The deposition parameters for depositing the SiO_2 film are shown in Table A.1 of Appendix A. The wafer was cut into four small samples measuring 4.2 cm by 2.5 cm. The samples were referred to as Sample A,

Sample B, Sample C and Sample D. The samples were cleaned in acetone and isopropyl alcohol (IPA) solutions for 5 minutes each. Then, a nitrogen gun was used to dry the samples. In general, samples must be cleaned in acetone and IPA solutions before carrying out any fabrication steps. This ensures that the samples are free from organic particles or general dust sticking to the surface.

5.3.1 Formation of Slope Platform

The next step was to pattern the four samples by optical lithography using S1813 as the photoresist to define the slope platform. In this project, the formation of the slope profile is the core step in fabricating the interlayer slope waveguide. In particular, the fabrication step by which the slope angle can be controlled through wet etching process, has become the novelty of this work. Throughout the course of carrying out the fabrication of the interlayer slope waveguide, there are a number of identified variants contributing to the controllable slope angle with the tapered-like structure etching profile. These include wet-etching parameters such as etchant concentration and temperature, porosity of the etching material (PECVD SiO_2) and most importantly the adhesion strength between the photoresist and the surface of the etching material (PECVD SiO_2).

By varying the properties of the photoresist through the addition of primer and subjecting the sample to thermal treatment, allow the adhesion strength between the photoresist and the etching material to be increased. This is caused by the physical linkages of bonding network between the atoms of the photoresist and SiO_2, which increases the intermolecular forces between the two interfaces. Increasing the adhesion strength would mean that the photoresist sticks very well to the surface of the etching material [6]. The stickiness allows the etching profile to be controlled.

The isotropic profile is the most commonly encountered etch profile for both wet and dry etching. This includes SiO_2 etched in aqueous hydrofluoric (HF) solutions where a curved sidewall is formed, as shown in Figure 5.6. This isotropic etching profile is created when the adhesion between the resist and the SiO_2 surface is high [6, 106].

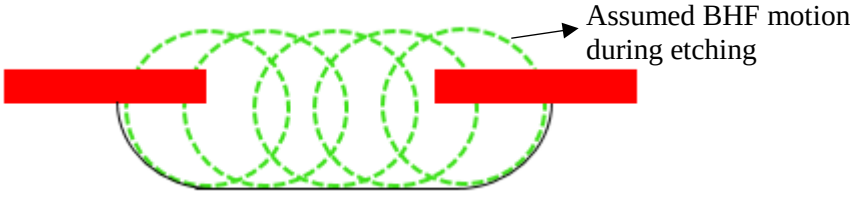


Figure 5.6 Cross-sectional view of the contour of the wall of wet etching silicon dioxide (SiO_2) in hydrofluoric (HF) acid solution, with strong adhesion of resist onto silicon dioxide (SiO_2) surface [6, 106].

In the case when the adhesion is poor, delamination of the resist occurs. The aqueous HF solutions easily attack the etching material underneath the resist due to the weak bonding network between the two interfaces. This results in the SiO_2 at the surface having higher etch rate and causing the top film to get etched faster. The film continued to be etched both in the horizontal and vertical directions

forming the tapered-like wall structure with sharp bends. The profile evolution and the resulting etch profile is shown in Figure 5.7 [106, 107].

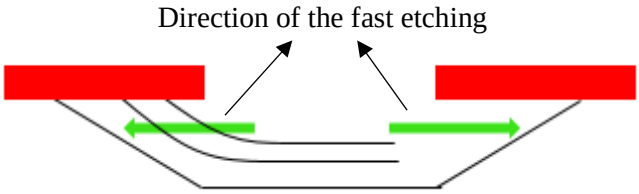


Figure 5.7 Profile evolution of the fast etching of the top surface of the silicon dioxide (SiO_2) in hydrofluoric (HF) acid solution, due to weak adhesion of resist onto silicon dioxide (SiO_2) surface [106, 107].

In this work, two types of S1813 were used in the optical lithography, S1813 G2, and S1813 G2 (SP15). The difference between these two types of S1813 photoresists is that S1813 G2 (SP15) contains adhesion primer. The addition of primer increases the adhesion strength between the photoresist and the SiO_2 film. As described in Section B.1.6 of Appendix B, the addition of adhesion promoter and further baking of the S1813 allows the slope etching profile to be controlled [106]. Sample A and Sample B were spun with S1813 G2. Sample C and Sample D were spun with S1813 G2 (SP15). The resulting resist thicknesses were approximately 1.2 μm. Then the four samples were exposed to UV light using an EVG620TB mask aligner system. After the photoresist was developed, Samples B and D were post-baked to increase the adhesion between the photoresist and the SiO_2 interface. Recipe details for using S1813 appear in Table A.4 of Appendix A. Figure 5.8 illustrates the photolithography steps for the four samples.

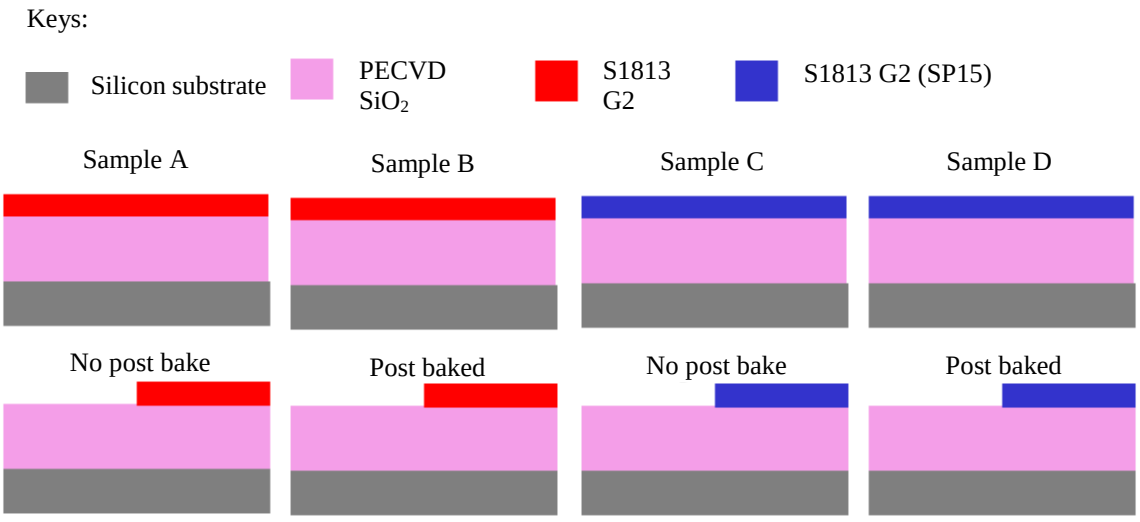


Figure 5.8 Illustration of photolithography steps for the four samples.

The fabrication process was followed by wet etching the four samples in buffered hydrofluoric acid, NH_4F:HF (7:1) for 5 minutes, at room temperature to define the slope profile [108]. Then the samples were placed in the plasma asher to strip off the remaining S1813 for 10 minutes. Recipe details for using the Tepla asher are given in Table A.11 of Appendix A. To clean the samples further, they

were immersed in N-Methyl-2-pyrrolidone (NMP) solvent, followed by cleaning them in acetone and IPA solutions for an equal duration of 10 minutes. Then the samples were dried using a nitrogen gun and were kept in an oven at 210^{o}C for 30 minutes to remove excess moisture. The above process was followed by the deposition of 400 nm thick a-Si:H film by an HWCVD system for the four samples. The recipe used for the deposition can be found in Table A.3 of Appendix A. The deposition parameters used to deposit the a-Si:H were optimized through a design of experiment (DOE) carried out separately lead by Dr Swe Zin Oo and Dr Antulio Tarazona [15]. The DOE was conducted to investigate the best deposition variables in terms of deposition temperature and flow rate of precursor gases to produce high-quality low-loss a-Si:H film. The four samples were then cleaned using acetone and IPA solutions for 5 minutes each before carrying out the next fabrication step. The samples were again dried using a nitrogen gun and kept in an oven at 201^{o}C for 30 minutes to remove any excess moisture and to increase surface adhesion. Then the samples were allowed to cool. This was followed by a coating of e-beam positive resist, ZEP520, which was used to pattern sub-micron waveguide structures by e-beam lithography. The resulting resist thicknesses were approximately 500 nm. The recipe used to spin and develop the 500 nm thick ZEP520 appears in Table A.5 of Appendix A. Sub-micron waveguide structures and grating couplers with varied periods from 500 nm to 1000 nm were then patterned onto the four samples using the JEOL JBX 9300FS e-beam tool. The beam conditions are shown in Table B.1 of Appendix B.

After developing the e-beam resist, the samples were dry-etched in the ICP tool using fluorine-based gas to form a strip waveguide structure. In fully etching the 400 nm thick a-Si:H film, approximately 290 nm thick ZEP520 was left. This gave and etching selectivity of almost 2:1, which meant that the a-Si:H was etched twice as fast as the ZEP520 resist. The details of the recipe for using ICP for etching the a-Si:H film are shown in Table A.10 of Appendix A. Next, the samples were placed in a beaker containing NMP solvents for at least 30 minutes to strip off the remaining ZEP520. The cleaning was followed by placing the samples into beakers containing acetone and IPA solutions, for 5 minutes each. The samples with the remaining ZEP520, with a-Si:H as the underlying material, were not cleaned in the plasma asher. This was a precautionary step to prevent exposing the a-Si:H film to high-energy oxide ions (O^{2-}) which were present in the plasma asher. The high-energy O^{2-} can bond itself to the dangling bonds of the a-Si:H film, which can alter the physical properties of the a-Si:H (for example, by increasing or decreasing the refractive index of the film). As a final step in the fabrication of the interlayer slope waveguide, the four samples were covered with 1 μm thick PECVD SiO_2 deposited at a temperature of 350^{o}C as the top cladding layer. Scanning electron microscopy (SEM) was used to image the cross-sectional topography of the fabricated interlayer slope waveguide. The samples were cleaved, and cleaned in acetone and IPA for 3 minutes. With the 5 minutes wet etch, Samples A, B, C and D produced slope angles of 11.8^{o}, 16.7^{o}, 20.8^{o} and 25.3^{o}, respectively. Figure 5.9 (a) to (d) shows the SEM images of the cross-sectional view of the four samples. Figure 5.10 shows the SEM image of the fabricated and un-cladded interlayer slope

waveguide with 400 nm width (*w*) and 400 core thickness (*h*); the inset picture shows the fully etched grating couplers used for measurement. Table 5-1 shows the slope profiles of the four samples.

Table 5-1 Slope profile with a 5 minutes wet-etching.

	S1813 G2		**S1813 G2 (SP15)**	
Slope parameters	Sample A	Sample B	Sample C	Sample D
Angle (°)	11.8	16.7	20.8	25.3
Height (μm)	1.44	1.51	1.44	1.45
Length (μm)	8.24	4.89	3.88	2.91
Calculated bend radius (μm)	17.6	10.9	5.9	4.1

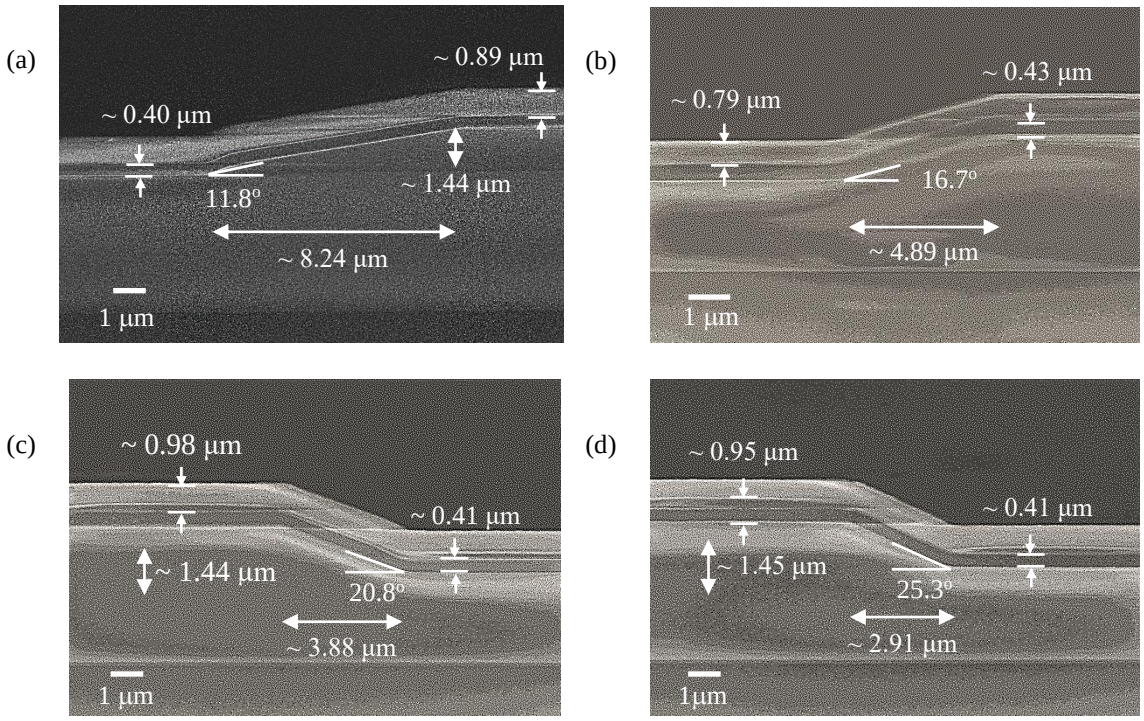


Figure 5.9 SEM images of cross-sectional view of the interlayer slope waveguide for, (a) Sample A, (b) Sample B, (c) Sample C, and (d) Sample D.

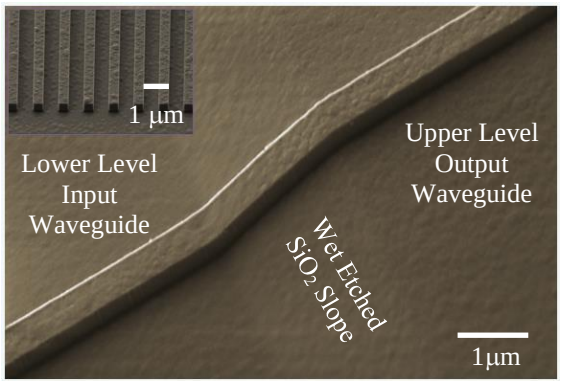


Figure 5.10 SEM image of top view of the interlayer slope waveguide for 400 nm core thickness (*h*) and 400 nm width (*w*). Inset: Fully-etched grating couplers connected at both ends of the interlayer slope waveguide.

5.4 Measurement Results

The transmission properties of the interlayer slope waveguides were measured in dB per slope (dB/slope) through averaging of up to five slopes. A tunable Agilent 81940A laser source and Agilent 81634B power sensor were used for the measurements at the wavelength of 1550 nm in transverse electric (TE) mode polarization. Single-mode SMF-28-J9 fibre was used to couple light at the input and output of the slope waveguides through fully etched grating couplers. The size of the grating couplers was 13 μm by 13 μm, sufficient to collect light from the single-mode core fibre with a mode field diameter of 10.4 μm. The design of the grating couplers allowed efficient coupling of TE mode polarization only. The fabricated waveguides had a varied width from 400 nm to 600 nm.

Figure 5.11 (a) to (d) shows the loss characteristics of Samples A, B, C and D with three repeated transmission measurements, for the 400 nm wide (*w*) by 400 nm thick (*h*) slope waveguide. Figure 5.12 (a) to (d) shows the loss characteristics of the four samples for 600 nm wide (*w*) by 400 nm thick (*h*) slope waveguide. In scanning the transmission across a range of wavelengths, it was observed that the output power fluctuated. Thus, each data point of the loss measurements was the results of averaging the transmission (dB) to up to a 20 nm wavelength interval, centred at 1550 nm in TE mode polarization. The graph of transmission against wavelength for Samples A, B, C and D for the 400 nm (*w*) by 400 nm (*h*) slope waveguides are attached in Appendix C. Figure 5.13 shows the measured losses from the four samples and a comparison with simulations, taken from Figure 4.4 (Chapter 4).

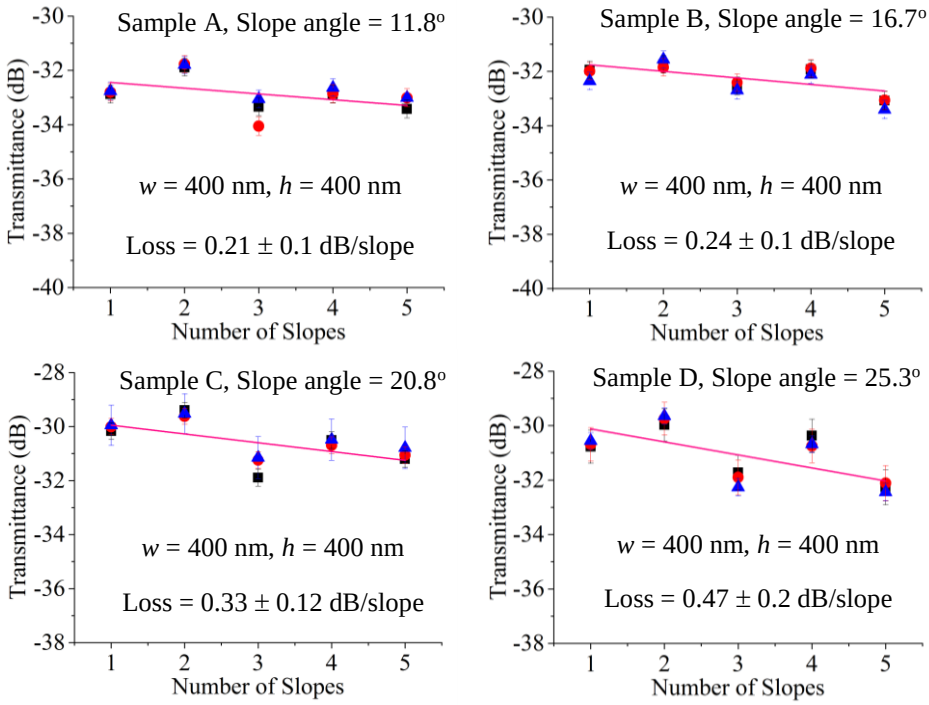


Figure 5.11 Transmission characteristics of the interlayer slope waveguide for 400 nm (*w*) by 400 (*h*) waveguide, at 1550 nm in TE mode polarization.

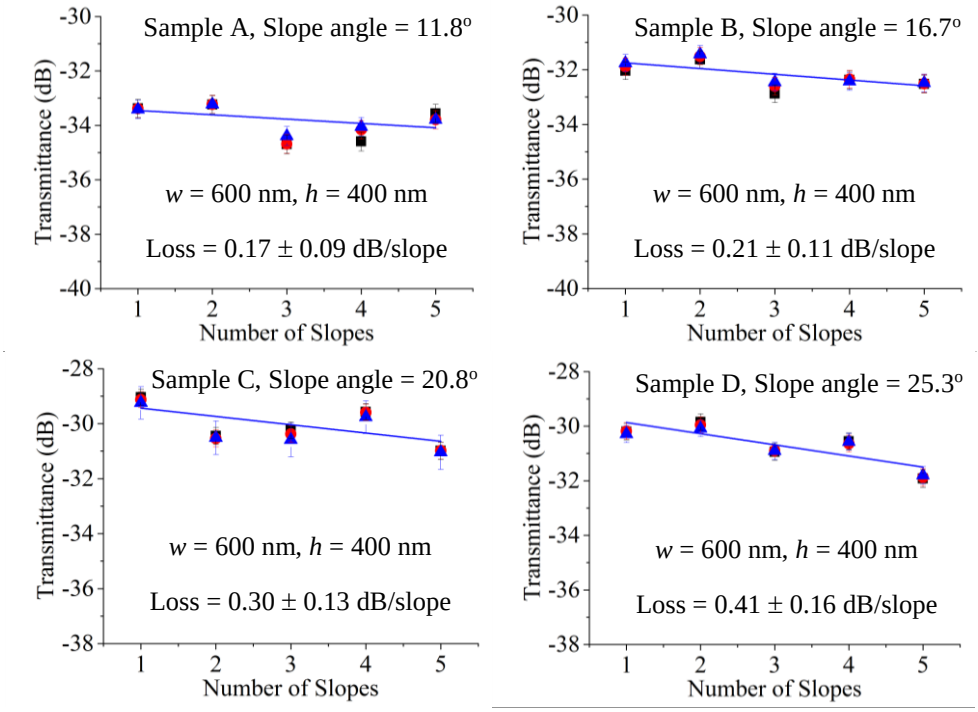


Figure 5.12 Transmission characteristics of the interlayer slope waveguide for 600 nm (*w*) by 400 (*h*) waveguide, at 1550 nm in TE mode polarization.

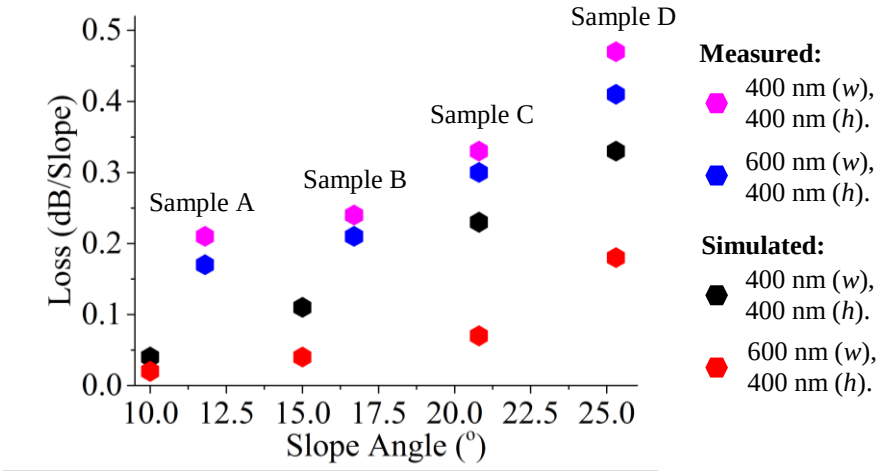


Figure 5.13 Measured and simulated losses for four slope angles and varied waveguide dimensions.

In examining the measurements, further analysis was conducted. Several factors could contribute to the high insertion loss to the devices. These include:

1. Un-optimized taper length and gratings structure. The 500 µm taper length may not be the optimal taper length for the 400 nm (*w*) by 400 nm (*h*) waveguide dimensions, for efficient adiabatic mode propagation. Mode propagating non-adiabatically will incur high scattering resulting to radiation losses.

   With regard to the gratings with fully etched structure used in project, it was anticipated that the coupling efficiency would be low due to the abrupt change in the refractive index discontinuity between each section of the grating, in comparison to shallow-etched

gratings. The high index change increases scattering causing mode-mismatch between the field from the uniform grating and the fibre mode.

2. Un-optimized bottom SiO_2 cladding. The gratings of the devices lie on different SiO_2 thicknesses, which are on 4.5 µm and 3µm. This would incur losses with power coupled towards the substrate and lost through radiation, resulting to low values of coupling efficiencies on the transmission.
3. Un-optimized thickness of the top SiO_2 cladding, resulting in high reflections at the fiber facet.
4. Radiation losses induced from the slope interfaces.

With regard to the gratings, the design of the one-dimensional (1-D) grating couplers allows coupling of TE mode only. However, the fabricated grating couplers structure were not fully optimized resulting to low coupling loss. The coupling loss of each grating coupler was estimated to be approximately 13.5 dB with equivalent coupling efficiency (C.E) equals to 4% only. In addition, the transmission properties of the single-mode HWCVD a-Si:H waveguides were characterized using the cut-back method at a wavelength of 1550 nm with TE mode polarization. The fabricated waveguides had lengths of 0.2, 0.3, 0.4, 0.5, 0.6 and 0.7 cm, widths (*w*) of 400 nm and core height (*h*) of 400 nm. These waveguides were fabricated on thermally grown SiO_2, with smoother surface – unlike the interlayers slope waveguides which were fabricated on a PECVD SiO_2 with rougher surface. Here, it was observed that the coupling loss of each grating coupler was 4.5 dB lower than the coupling loss from the interlayer slope waveguide samples. Figure 5.14 shows the linear fit of the extracted transmission losses of the TE mode of the 400 nm (*w*) by 400 nm (*h*) waveguides which were found to be 17.3 dB/cm.

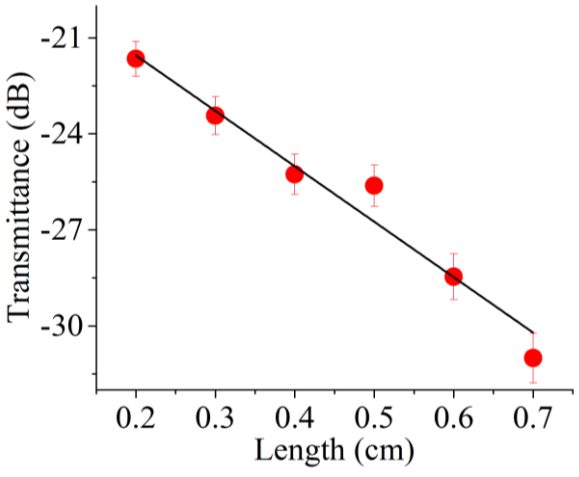


Figure 5.14 Measured transmission characteristics of the TE mode of the HWCVD a-Si:H waveguides with 400 nm (*w*) and 400 nm (*h*) at 1550 nm wavelength.

Here, it can be concluded that even with high insertion loss to the devices due to un-optimized variants such as the taper length, gratings structure, thickness of the bottom and top SiO_2 cladding,

slope interfaces, the aim in measuring the loss of the interlayer slope waveguide in terms of dB for 5 slopes was achieved, through the linear regression fit method.

5.5 Analysis and Discussion

Loss characteristics are presented here for the interlayer slope waveguide with four slope angles, namely 11.8^o, 16.7^o, 20.8^o and 25.3^o.Two waveguide dimensions, 400 nm (w) by 400 nm (h) and 600 nm (w) by 400 (h) were measured for the different slope angles. The loss measurements were compared with the simulation, as presented in Figure 5.13. The measured loss of the interlayer slope discussed in the sub-sections below.

5.5.1 Effect of Bending Structure

The losses of the four samples were observed to increase as the slope angle increased. This indicated that most of the losses in the interlayer slope waveguide were attributed to a higher slope angle. The trend in the loss characteristics conformed to the theory of losses in waveguide bend, as described in Section 3.3 of Chapter 3 and shown by simulation (Figure 4.4 of Chapter 4). That is, high loss was associated with higher slope angles.

When the optical mode travels from a straight waveguide into the slope interface, which it encounters as surface perturbation, it changes the direction of propagation with respect to the interface curvature. According to Kasap [99], as the mode enters a bend, the waveguide geometry is altered so that the zig-zagging ray now travels at an angle of incidence (θ_{ib}) that is narrower than the angle of incidence (θ_i) at the straight section ($\theta_{ib} < \theta_i$). The value of θ_{ib} becomes smaller with sharper bending. The change in direction of propagation also changes the effective index (n_{eff}) and thus the effective propagation constant (β) of the propagating mode. The varied n_{eff} values were noted as shown in Figure 4.5. In Figure 4.5, the value of n_{eff} on the straight section of the waveguide reduces from n_{eff1} = 2.71 to n_{eff2} = 2.69 at the slope interface. At the straight section of the waveguide, fundamental mode propagates with its respective propagation constant (β_1). The propagation changes of the fundamental mode from straight to the slope junction would excite bending mode that extend into the lower SiO_2 cladding, and a different propagation constant with respect to n_{eff2}. The difference in propagation constant between the straight waveguide (β_1) and mode at the slope interface (β_2), travelling at different phase velocities results in mode-mismatch. This reduces the overlap coupling between the two modes, which gives rise to transition losses occurring between the straight and the bent waveguides [88, 98].

In the measurement, the 25.3^o slope angle exhibited a loss of 0.47 dB/slope, and the 11.8^o slope angle had a loss of 0.21 dB/slope. This implies that mode propagating in the 25.3^o slope angle, experienced a sudden change in ray direction, which caused significant mode-mismatch, and

thus increasing the loss. In contrast, mode propagating in the 11.8° slope angle, underwent a smoother transition during the mode conversion [100].

5.5.2 Effect of Surface Roughness of the Film

Another loss contribution is the result of scattering due to roughness between the waveguide surface and cladding layers. The surface roughness of the HWCVD a-Si:H film and the underlying PECVD SiO_2were evaluated using the tapping mode of an atomic force microscope (AFM). The model and specifications of the equipment used for the AFM measurement are shown in Table 5-2.

Table 5-2 Model and specification of Atomic Force Microscopy (AFM) tool.

Equipment	Model / Specification
AFM	Bruker Nanoscope V
Scanner	J Scanner, 8280J
	Maximum scanning area = 120 µm
AFM Tip	PPP-NCHR
	Tip height = 10 -15 µm
	Tip radius = < 7 nm

As described in Sections 5.2 and 5.3, the structure of the interlayer slope waveguide consists of two-level platforms with two bottom-cladding SiO_2 thicknesses. The fabrication of the device involves wet etching the PECVD SiO_2 to produce the slope platform, resulting in two distinct surface profiles. Thus, it is necessary to characterize the surface roughness of both the upper and lower layer SiO_2, and the corresponding surface roughness of the upper and lower layer HWCVD a-Si:H film. The surface topography of the upper and lower layer PECVD SiO_2 and HWCVD a-Si:H extracted from the AFM measurements, are shown in Figure 5.15 (a) to (d).

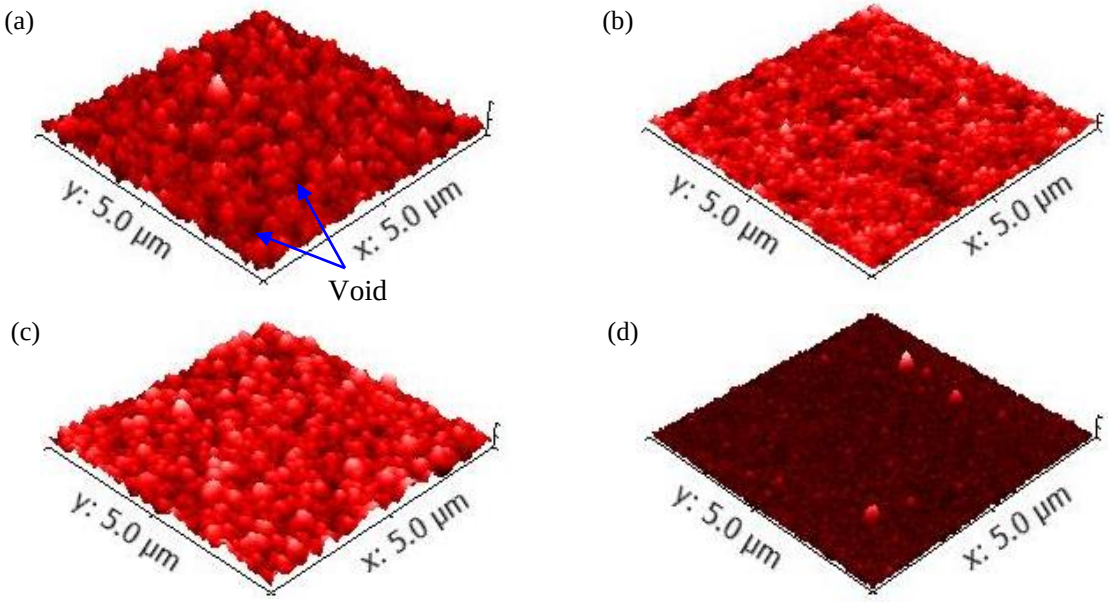


Figure 5.15 Topographical AFM image of (a) upper layer PECVD SiO_2, (b) lower layer PECVD SiO_2, (c) upper layer HWCVD a-Si:H and (d) lower layer HWCVD a-Si:H.

The AFM results are shown in Table 5-3.

Table 5-3 RMS surface roughness of upper and lower level PECVD SiO_2 and HWCVD a-Si:H waveguide.

Material	RMS surface roughness (nm)
Upper layer PECVD SiO_2	4.2
Lower layer PECVD SiO_2	2.1
Upper layer HWCVD a-Si;H	3.99
Lower layer HWCVD a-Si;H	1.35

The AFM measurements show distinct differences for the values of RMS surface roughness from the upper and lower level, for both PECVD SiO_2 and HWCVD a-Si:H films. Several conclusions can be drawn from the findings regarding the AFM measurements:

1) The surface roughness of the deposited PECVD SiO_2 was found to be 20 times higher than thermally grown SiO_2. This was because the PECVD process is rapid in comparison to wet thermal oxidation. In PECVD process, the presence of plasma – which is induced by high radio frequency (RF) power – has a role in dissociating precursor gases effectively. Large amounts of reactant gaseous species are produced, with high-energy ions. As these gaseous reactant species diffuse to the surface of the substrate, which is heated to 350^{o}C, the mobility of the gaseous reactant species increases [71]. This increases the deposition rate, resulting in random and rapid collision of the reacting gaseous SiO_2 species among themselves. Upon adhering to the heated substrate surface for the film growth, the reactant gaseous SiO_2 species forms SiO_2 clusters, resulting in inhomogeneous crystallite arrangement on the active substrate surface. As a result, the surface roughness of the SiO_2film increases [109-111]. The voids, which resemble a hollow feature, can be observed in Figure 5.15 (a). Amirzada *et al*. [110] analysed the surface roughness of PECVD SiO_2 films with varying substrate temperatures. SiO_2 film deposited at a substrate temperature of 300^{o}C had an RMS surface roughness of 5 nm, which was similar to the surface roughness measured in this work.

2) The AFM measurements showed that the surface roughness of the PECVD SiO_2 was smoothed out following the wet etching process using NH_4F:HF (7:1). The RMS surface roughness of the lower level SiO_2 film reduced by half with the 5 minutes wet etch. In the wet etching process, HF^{2-} molecules adsorbed onto the SiO_2 surface. By chemical reaction, the Si-O covalent bonds were efficiently broken through the high electronegativity of fluorine molecules [112]. As a result, the amorphous SiO_2 network structure became disjointed with the release of silicon atoms, as shown in equation B.6 in Appendix B [106, 113, 114]. The breaking off of the Si-O bonds also resulted in the efficient removal of the disordered sites of the random-sized SiO_2 clusters. This caused the contours of the SiO_2 clusters to be less

jagged revealing smoother surfaces; however, some pinholes remained on the film. The smoothened surface topography is evident in Figure 5.15 (b).

3) The RMS surface roughness of the upper and lower layer HWCVD a-Si:H closely follow the RMS surface roughness of the corresponding PECVD SiO_2. This is due to the surface roughness of the underlying PECVD SiO_2 film being transferred to the upper film layer. It is worth noting that the RMS surface roughness of HWCVD a-Si:H film deposited under the same deposition conditions, but using thermally grown SiO_2 as the bottom cladding, was measured as slightly lower than HWCVD a-Si:H film deposited on a PECVD SiO_2. The RMS surface roughness for thermally grown SiO_2 and the corresponding HWCVD a-Si:H film are shown in Table 5-4 for comparison.

Table 5-4 RMS surface roughness of thermally grown SiO_2 and HWCVD a-Si:H.

Material	RMS surface roughness (nm)
Thermally grown SiO_2	0.22
HWCVD a-Si:H at 230°C	0.91

As part of the analysis, Lumerical FDTD was used to simulate the effect of surface roughness on loss of the interlayer slope waveguide. The loss was estimated by introducing surface roughness to the top and bottom interfaces and the waveguide sidewalls. As an approximation, the roughness for the top interface was set to 3.99 nm, and the underlying bottom roughness was 4.4 nm. The exact roughness of the waveguide sidewalls could not be evaluated due to limitations of the AFM tool. However, for analysis purposes it is assumed that the sidewall roughness of the interlayer slope waveguide was the same as the roughness set to the top interface, which was 3.99 nm. The simulation was run at a wavelength of 1550 nm with TE mode polarization. The results showed an increase in the loss for all four slope angles with the added roughness. The results are shown in Table 5-5, with the simulation loss results tabulated with the measured loss results for comparison.

Table 5-5 Simulated and measured loss for different slope angles for 400 nm (*w*) by 400 nm (*h*) waveguide dimensions.

	Simulated loss		Measured loss
Slope angle (°)	Loss (dB/Slope) Without surface roughness	Loss (dB/Slope) With surface roughness	Loss (dB/Slope)
10	0.03	0.11	0.21
15	0.11	0.19	0.26
20	0.23	0.28	0.32
25	0.33	0.40	0.50

Similar simulations were performed to observe the effect of introducing surface roughness to the interlayer slope waveguide in 2D field distribution. Two monitors were placed across the coupler, one at the input and another 0.6 μm from the junction of the slope interface. The RMS surface roughness as described earlier was used.

Figure 5.16 (a) to (e) shows the 2D electric field distribution of TE mode across the interlayer slope waveguide. The *y*-axis shows the width of the waveguide, and the *z*-axis shows the height of the waveguide. Figure 5.16 (a) shows the 2D electric field distribution of TE mode at the input. Figure 5.16 (b) and (c) show the 2D electric field distribution at the slope interface with a 10^{o} slope angle, with no added surface roughness and with added surface roughness, respectively. Figure 5.16 (d) and (e) show the 2D electric field distribution at the slope interface with a 25^{o} slope angle, with no added surface roughness and with added surface roughness, respectively. The surface roughness induces loss as shown in Table 5-5 but the RMS roughness values are small enough to show an obvious effect on the mode solution.

To examine the shifting of the optical mode, graphs expressing the 1D electric field amplitude distribution of the three modes are shown in Figure 5.17. Figure 5.17 illustrates the electric field of the optical mode at 10^{o} and 25^{o} slope angles without surface roughness. The graphs show that the mode field was pulled towards the substrate, with a shift of approximately 30 nm and 100 nm respectively; this dispersed the field as it entered the slope interface, suggesting that part of the evanescent field decays into the bottom SiO_2 cladding.

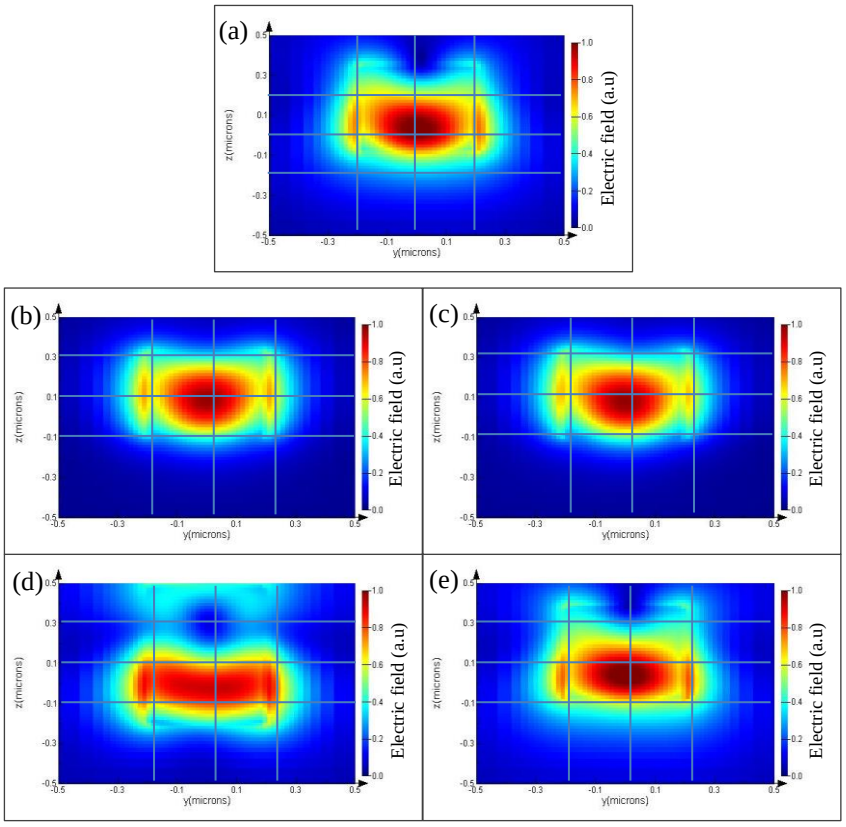


Figure 5.16 2D Electric field distribution of TE mode at (a) input, with no added surface roughness, (b) 10^{o} slope interface with no added surface roughness, (c) 10^{o} slope interface with added surface roughness, (d) 25^{o} slope interface with no added surface roughness, and (e) 25^{o} slope interface with added surface roughness. The results pertain to a 1550 nm wavelength with TE polarized mode.

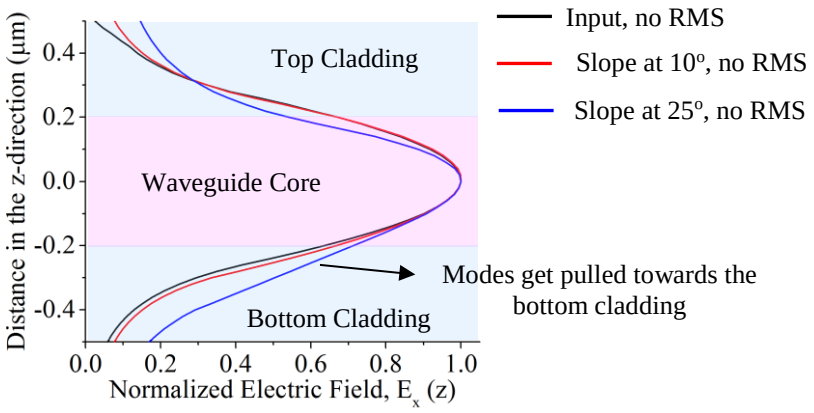


Figure 5.17 1D electric field amplitude distribution in the *z*-direction, at 1550 nm wavelength with TE polarized mode.

Because the interlayer slope waveguide was cascaded and fabricated on two level platforms, it was expected that the varying RMS surface roughness would affect the measurements. This would be due to the films on the upper and lower layers having different properties regarding surface roughness. The measurements of the interlayer slope waveguide are shown in Figure 5.11 (a) to (d) and Figure 5.12 (a) to (d). The transmission for each number of slopes decreased alternately. For example, the transmission for 1 slope was slightly lower than for 2 slopes. The transmission for 3 slopes was slightly lower than for 4 slopes, and so on.

This was the result of varied surface roughness of the two-level films on two-level platforms. Optical mode propagating at the output taper of the 1 slope, 3 slopes and 5 slopes devices interacted mainly with the upper level platform with RMS surface roughness of 4.4 nm. By contrast, optical mode propagating at the input and output tapers of the 2 slopes and 4 slopes devices interacted more with the lower level platform with RMS surface roughness equal to 2.2 nm. However, the varied surface roughness had minimal effect of the loss of the slope, since the mode interacting at the slope interfaces with respect to varied roughness was insignificant.

5.5.3 Effect of Enlarged Width of the Waveguide

Figure 5.13 illustrates that the losses in the 600 nm wide waveguides were slightly lower than the losses in the 400 nm wide waveguides. There are two possible reasons.

1) Optical mode propagating in the 600 nm wide waveguide is more confined within the waveguide core than mode propagating in the 400 nm wide waveguide. This reduces overlap of the optical mode with the roughness on the sidewalls and thus reduces the loss of the waveguide [115].

2) Optical mode propagating in a 600 nm (*w*) by 400 nm (*h*) waveguide was more susceptible to bend loss. Generally, this is because light propagating in the 600 nm (*w*) by 400 nm (*h*) waveguide travels at θ_i much larger than θ_c of the medium, compared with light propagating in the 400 nm (*w*) by 400 nm (*h*) waveguide of the same medium. To analyse this scenario quantitatively, it can be viewed in terms of the n_{eff} values of the two waveguide sizes. From the simulation in Figure 4.1, 400 nm (*w*) by 400 nm (*h*) waveguide has an n_{eff} value of 2.71, whereas 600 nm (*w*) by 400 nm (*h*) waveguide has an n_{eff} value of 3.01. Using equation 3.17 (Chapter 3) for estimation, these n_{eff} values give θ_i approximately equal to 49.4° and 58.2° for the 400 nm (*w*) by 400 nm (*h*) and 600 nm (*w*) by 400 nm (*h*) waveguides, respectively. Thus, it can be deduced that light travelling in a wider waveguide would have an θ_{ib} very much larger than the θ_{ib} in a narrower waveguide, for the same slope angle structure. Table 5-6 summarizes n_{eff} and θ_i for the two waveguides.

Table 5-6 Effective propagation constant of a mode (n_{eff}) and estimated incident angle (θ_i) for 400 nm (*w*) by 400 nm (*h*) and 600 nm (*w*) by 400 nm (*h*) sized waveguides.

Critical angle (θ_c) of the medium	**Waveguide dimensions**	**Effective index of a mode (n_{eff})**	**Estimated incident angle (θ_i)**
24.2	400 nm (*w*) by 400 nm (*h*)	2.71	4 9.9
	600 nm (*w*) by 400 nm (*h*)	3.01	58. 2

5.6 Summary

The interlayer slope waveguide was designed, fabricated and characterized. The characteristics of the HWCVD a-Si:H interlayer slope waveguide in terms of loss per slope with varying inclination slope angles were then used as a reference to extend its functionality as a 3D interconnect. The measurement results conformed to the theory of waveguide bend and simulation described in Chapter 4. Losses from four slope angles (11.8°, 16.7°, 20.8° and 25.3°) were measured. Loss of 0.21 dB/slope was obtained from the 11.8° slope angle with 400 nm (*w*) by 400 nm (*h*) waveguide dimensions. The loss increased to 0.47 dB/slope for a slope angle of 25.3°, indicating high mode-mismatch in the slope interface. Surface roughness also played a role in the loss of the device. In extending the interlayer slope waveguide as a real 3D interconnect, slope angles as low as 10° were chosen. This choice was a compromise between device compactness and low loss structure.

Chapter 6 Fabrication and Characterization of the Crosstalk Device and Fly-over Slope Waveguide

6.1 Introduction

In this chapter, the making of the crosstalk device is described, as well as the preliminary fabrication of the fly-over slope waveguide. Similar to Chapter 5, the mask design using L-Edit software for both optical and electron beam (e-beam) masks is explained first. This is followed by a description of the fabrication process. Then the characterization and analysis of the devices is presented and discussed. The details of the fabrication recipe appear in Appendix A and the descriptions of the fabrication tools and characterization techniques can be found in Appendix B.

6.2 Orthogonal Crosstalk Waveguide

The schematic structure of the orthogonal crosstalk waveguide placed on the interlayer slope waveguide is shown in Figure 6.1.

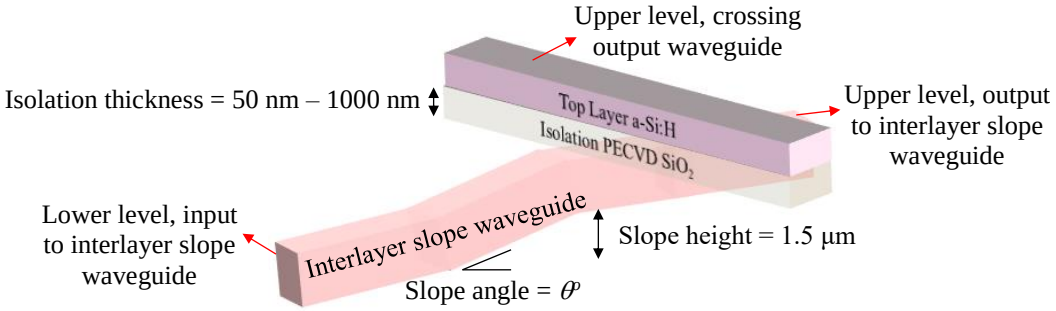


Figure 6.1 Schematic structure of an orthogonal waveguide placed on the interlayer slope waveguide.

The device comprises the interlayer slope waveguide described in Chapter 5, cladded with plasma enhanced chemical vapour deposition (PECVD) silicon dioxide (SiO_2) for optical isolation, with the height ranging from 50 nm to 1000 nm. In this work, the SiO_2 cladding layer was not planarized due to the unavailability of a chemical mechanical polishing (CMP) tool when the device was developed. Two waveguide dimensions were fabricated: 400 nm (w) by 400 nm (h) and 1000 nm (w) by 400 nm (h). A waveguide with the same dimensions as the interlayer slope waveguide was placed orthogonally on top of the upper level of the interlayer slope waveguide. One end of the orthogonal waveguide was bent with a curve radius of 35 μm, and tapered out to grating couplers, while the other end was terminated. The size of the gratings used to couple light into the waveguides had the same dimensions as the grating couplers used for the interlayer slope waveguide, as described in Section 5.3.

6.2.1 Mask Design

Similar to the interlayer slope waveguide, the fabrication of the orthogonal crosstalk waveguide required the use of both optical and e-beam masks. The main reason for using optical masks was to save writing time in patterning large rectangular structures. The e-beam mask was mainly used to pattern small structures, which included the sub-micron sized waveguides and grating couplers. Figure 6.2 shows the design of the optical mask used to form the slope platform in making the crosstalk device.

Figure 6.2 Schematic drawing of the optical mask design used to define the slope platform.

The structure of the optical mask made up the first cell (Cell 1), which was the first layer to be fabricated. Included in Cell 1 were alignment markers, used as a reference for aligning the two-level waveguides with the rectangular structures. The standard dimensions of the alignment markers were 20 μm by 1000 μm. The dimensions of the alignment markers, and the location of the alignment markers drawn by L-Edit on the sample size region, are shown in Figure 6.3 (a) and (b), respectively. These alignment markers were drawn on both the optical and e-beam masks.

Then e-beam masks were designed to pattern the first and second level waveguides. Two e-beam cells were required. The first, Cell 2, was used to pattern the first-level waveguides, including the grating couplers. The structure was the same as the structure shown in Figure 5.3. The second e-beam cell, Cell 3, was used to pattern the second-level waveguides, including the grating couplers. The schematic structure of the upper-level crosstalk waveguide is shown in Figure 6.4

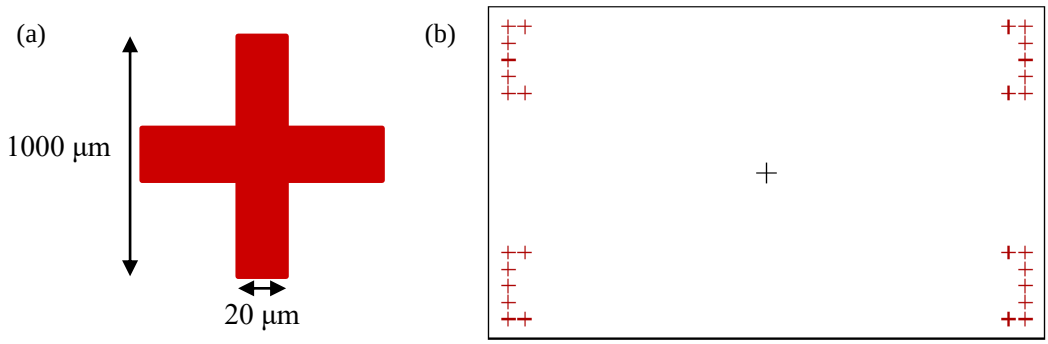


Figure 6.3 Schematic diagrams of the alignment markers showing (a) the dimensions of the structure, and (b) the location of the alignment markers on the sample region, drawn in L-Edit.

The second-level waveguides, Cell 3 were placed above the first-level waveguides (Cell 2), as shown in Figure 6.5. Then the superimposed structures which contained Cells 2 and 3, were placed onto

Cell 1, as shown in Figure 6.6. The distance between the edges of the rectangular structure and the orthogonal waveguide was 12.5 µm, as shown in Figure 6.7.

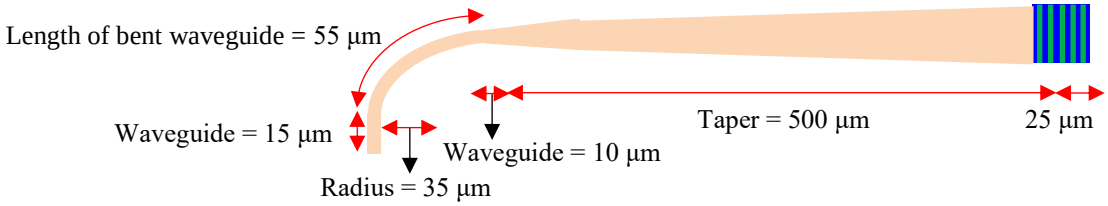


Figure 6.4 Schematic structure of the second-level waveguide.

Figure 6.5 Schematic structure of the second-level waveguide placed above the first level waveguide.

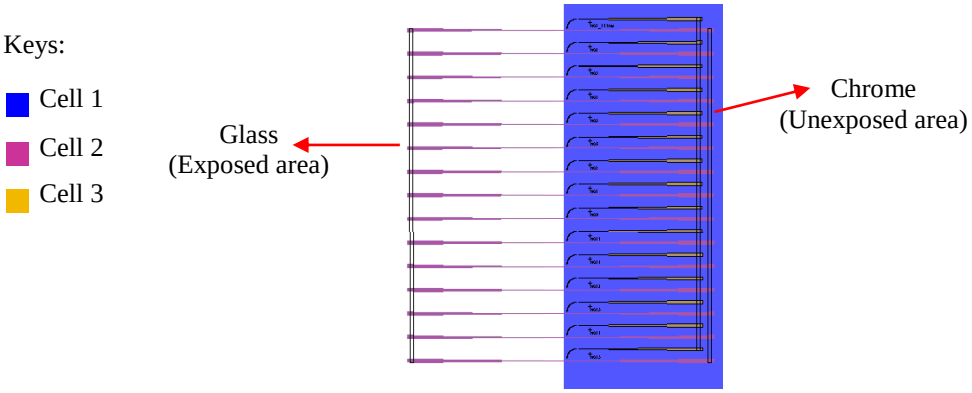


Figure 6.6 Mask design drawn in L-Edit software, illustrating the design of the crosstalk waveguide structure.

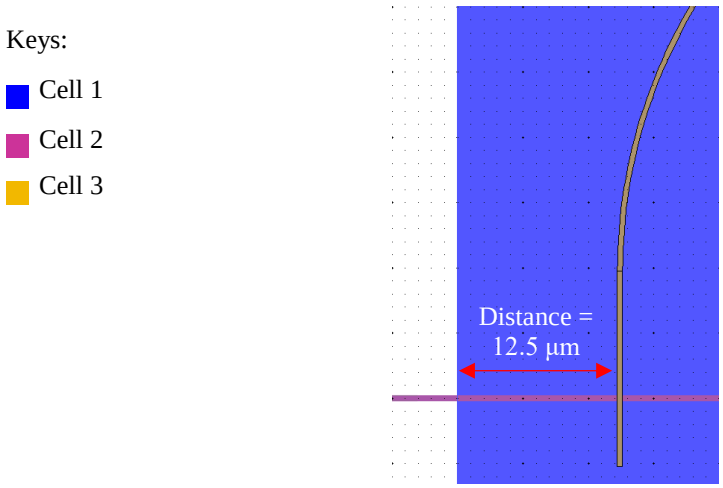


Figure 6.7 Close-up of the mask design drawn in L-Edit software showing the distance between the edges of the rectangular pattern (of the optical mask) to the crossing waveguide.

6.2.2 Device Fabrication

The device fabrication was similar to that of the interlayer slope waveguide, with additional steps to form the second-level orthogonal HWCVD a-Si:H waveguide. Waveguide dimensions of 400 nm (*w*) by 400 nm (*h*) and 1000 nm (*w*) by 400 nm (*h*) for the top and bottom waveguides were fabricated. In forming the slope platform, S1813 (G2) was used as the photoresist. Then the samples were post-baked, using the recipe described in Section 5.3. With a 5 minutes wet etching using NH_4:HF (7:1), a slope with a 15.8^o angle was formed.

PECVD SiO_2 was used as the cladding material to isolate the two crossing waveguides. Four samples were prepared containing crosstalk devices, with isolation cladding thicknesses equal to 50 nm, 200 nm, 500 nm and 1000 nm. Figure 6.8 shows the simplified fabrication steps in making the crosstalk device.

Figure 6.9 shows the SEM image of the cross-sectional view of a crosstalk device before the patterning of the second-level orthogonal waveguide. The layout of the fabricated crosstalk structure is shown in Figure 6.10. The blue area indicates the lower level platform after NH_4F:HF (7:1) wet etching, and the un-shaded area shows the upper level platform covered by photoresist during the wet etching. Figure 6.11 shows the optical microscopic images of the fabricated crosstalk device, focusing on the slope and the crosstalk structure.

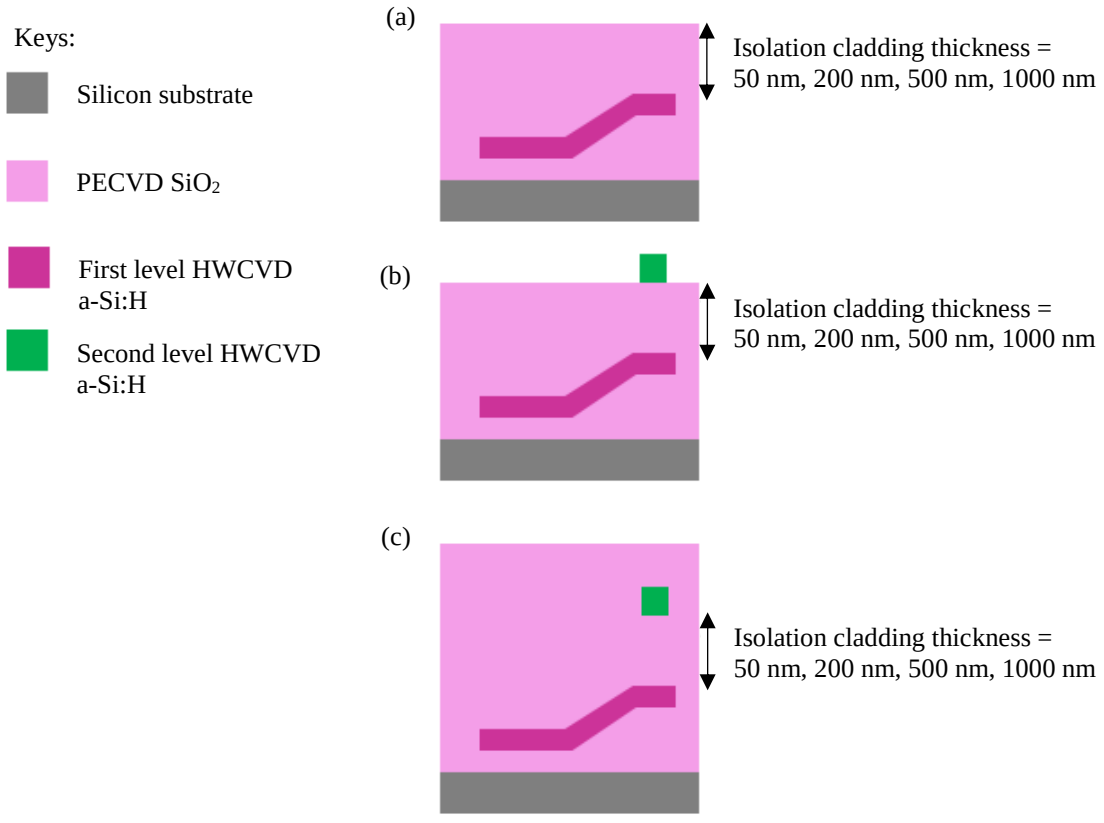


Figure 6.8 Simplified fabrication steps for making the crosstalk device.

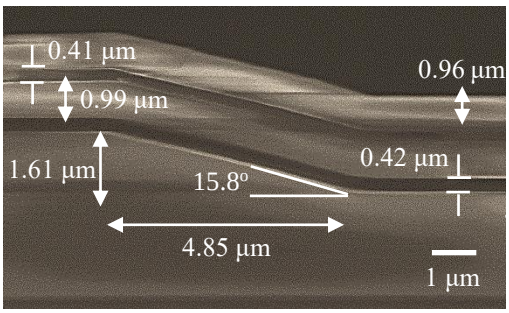


Figure 6.9 SEM image of cross-sectional view of a crosstalk device, showing HWCVD a-Si:H interlayer slope waveguide, cladded with 1000 nm PECVD SiO_2, and topped with a second-layer HWCVD a-Si:H film.

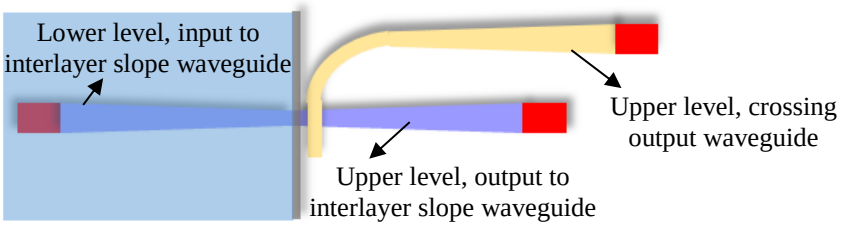


Figure 6.10 Schematic diagram of the fabricated crosstalk structure.

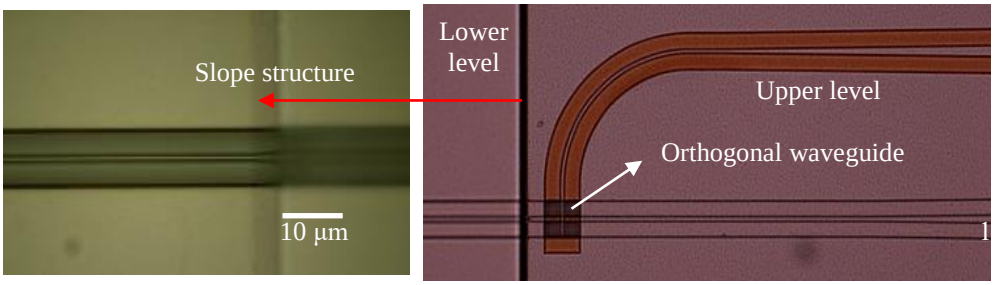


Figure 6.11 Optical microscopic image of the fabricated crosstalk device, comprising the orthogonal waveguide placed on the interlayer slope waveguide, with 15° slope angle.

6.2.3 Measurement Results

The transmission of the crosstalk waveguides was measured using the same set-up as that used to measure the transmission of the interlayer slope waveguide, as described in Section 5.4. Figure 6.12 illustrates the method for determining the coupling between the first- and second-level waveguides, which were placed vertically and orthogonal to each other.

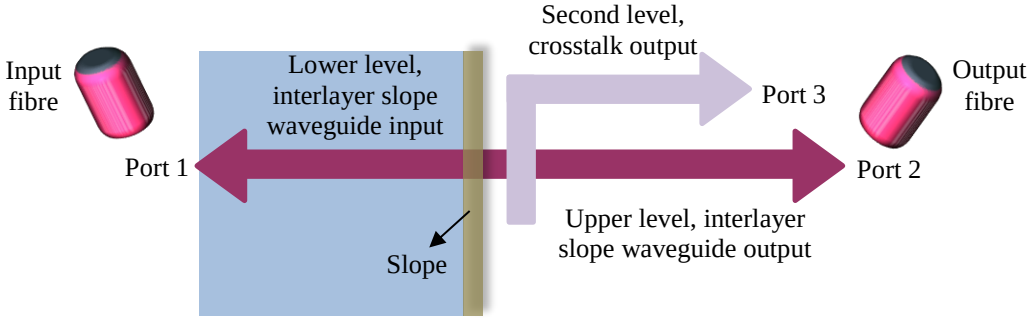


Figure 6.12 Illustrations of the crosstalk measurements.

The measurement method was as follows. First, the input fibre was aligned to the grating couplers of the input of the interlayer slope waveguide, Port 1. The output fibre was aligned to the output of the interlayer slope waveguide, Port 2. The transmission was recorded as Loss 1. Then the output fibre was moved and aligned to the grating couplers of the output of the second-level waveguide, Port 3. The transmission was recorded as Loss 2. Coupling loss was determined by subtracting Loss 2 from Loss 1, measured in dB.

Three measurements of three identical waveguide dimensions, for every isolation thickness (50 nm, 200 nm, 500 nm and 1000 nm) were recorded. Figure 6.13 shows the spectral transmission for the two output ports, Port 2 and Port 3, from the crosstalk device with 200 nm isolation thickness, for 400 nm (*w*) by 400 nm (*h*) waveguide dimensions. Figure 6.14 shows the coupling loss for each measurement of varying isolation thicknesses. The measured data for waveguide dimensions of 400 nm (*w*) by 400 nm (*h*) and 1000 nm (*w*) by 400 nm (*h*), for varying isolation thicknesses (50 nm, 200 nm, 500 nm and 1000 nm) appear in Table C1 of Appendix C.

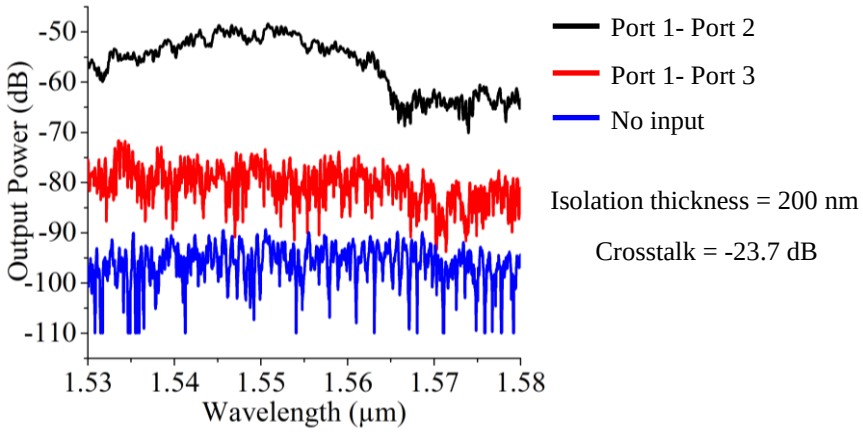


Figure 6.13 Transmission data of the two outputs, Port 2 and Port 3, for 200 nm isolation thickness, for 400 nm (*w*) by 400 nm (*h*) waveguide dimensions. The black curve shows transmission from the interlayer slope waveguide, Port 1 to Port 2; red curve shows crosstalk from the second-level waveguide, Port 1 to Port 3; and blue curve is dark noise of the detector.

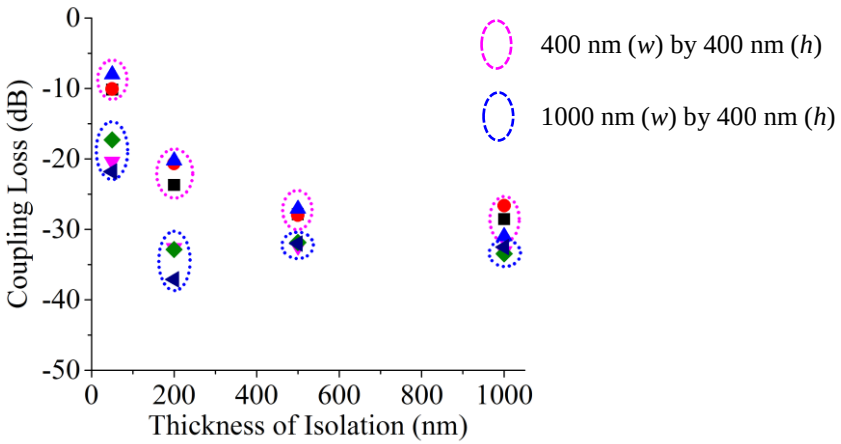


Figure 6.14 Measurement of coupling loss of a crossing waveguide placed on top of the interlayer slope waveguide, for 400 nm (*w*) by 400 nm (*h*) and 1000 nm (*w*) by 400 nm (*h*) waveguide dimensions, with varying isolation thicknesses.

6.2.4 Analysis and Discussion

Figure 6.14 illustrates that light was isolated by an average of -22 dB with 200 nm waveguide separation, for 400 nm (*w*) by 400 nm (*h*) waveguide dimensions. For larger waveguides (1000 nm (*w*) by 400 nm (*h*)), light was isolated with an average of -21 dB with isolation thickness as thin as 50 nm. The results of the measurements correlate with the simulated results, presented in Section 4.3.1 of Chapter 4.

The measured results showed that smaller waveguides (400 nm (*w*) by 400 nm (*h*)) were more susceptible to couple light than the larger waveguides. With isolation thickness of 50 nm, the 400 nm (*w*) by 400 nm (*h*) waveguides coupled approximately -10 dB optical power. As discussed in Section 4.3.1, this is due to the lower optical confinement in the 400 nm (*w*) by 400 nm (*h*) waveguides compared to the 1000 nm (*w*) by 400 nm (*h*) waveguides. In theory, small waveguides radiate optical energy out of the waveguide core more easily than larger waveguides. This results in the increase of evanescent field in the surrounding cladding layer. If another waveguide having the same effective propagation constant (β) is placed in close proximity to the first waveguide, optical coupling occurs.

It was also observed that evanescent coupling for both waveguide dimensions decreased with an increase in isolation thickness until it reached saturation value. The coupling of the smaller waveguides saturated at an average of -28 dB, whereas the larger waveguides saturated at an average of -33 dB. These values of saturation differ from the saturation values presented in Figure 4.9. According to the simulation results in Figure 4.9, crosstalk as low as -50 dB was achieved for 500 nm isolation thickness for the small waveguides, and for 300 nm isolation thickness for larger waveguides. This difference resulted from three main reasons.

1) The surface roughness attributed from the waveguides caused the optical mode to scatter out and collected by the deformed shape second-level waveguide. Gambling *et al.* [101] stated that under certain circumstances that satisfy the condition of optical mode coupling, optical power radiating into the cladding (because of surface perturbation such as bends or surface roughness) can be coupled by the optical mode of the waveguide core. This increases the optical power.
2) The bump formed by the unplanarized SiO_2 isolation layer resulted in the deformed shape of the second-level waveguide. This caused the optical mode from second-level waveguide to couple to the mode from the first-level, through the pointy deformed structure. The result was high coupling.
3) The fabricated structure based on Figure 6.1 is dissimilar to the simulated structure based on Figure 4.7. The addition of the slope platform with 15.8^o inclination angle affects the crosstalk profile. With the same reason to 1) and 2), the radiated power at the slope interfaces coupled to the nearby waveguide, thus increasing the transmission. In simulating the structure based on Figure 6.1, it was observed that the crosstalk saturated at an average of -33 dB for 400 nm (*w*)

by 400 nm (*h*) waveguides, and at -43 dB for 1000 nm (*w*) by 400 nm (*h*) waveguides. Figure 6.15 (a) and (b) show the measured and simulated crosstalk for 400 nm (*w*) by 400 nm (*h*) and 1000 nm (*w*) by 400 nm (*h*) waveguides, respectively, based on the fabricated structure of Figure 6.1.

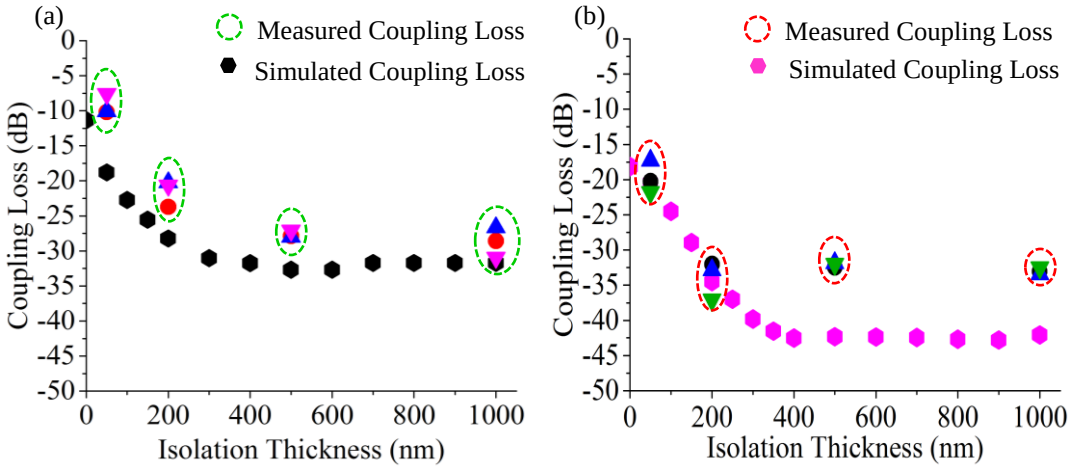


Figure 6.15 Measured and simulated coupling loss with varied isolation thickness based on structure of Figure 6.1, for (a) 400 nm (*w*) by 400 nm (*h*), and (b) 1000 nm (*w*) by 400 nm (*h*) at 1550 nm wavelength with TE polarized mode.

The difference in the coupling values for structures based on Figure 4.7 and Figure 6.1 are tabulated in Table 6.1 for comparison. The discrepancy in the saturated coupling values for the two crosstalk structures is important in understanding the characteristics of the designed interlayer slope waveguide. Optical mode propagating along the interlayer slope waveguide cannot be treated in the same way as mode propagating in straight waveguides. Optical mode propagating at the slope interface becomes scattered due to the change in the direction of propagation. The scattering causes the field of the mode that continue to propagate at the curved section to contain more components than a fundamental mode [116].

Table 6-1 Simulated optical coupling for crosstalk structure based on Figure 4.7 and Figure 6.1.

Crosstalk waveguides structure	**Waveguide dimensions**	**Cladding thickness (nm) for -20 dB crosstalk**	**Cladding thickness (nm) for -33 dB crosstalk**	**Cladding thickness (nm) for -50 dB crosstalk**
Structure based on Figure 4.7	400 nm (*w*) by 400 nm (*h*)	50	-	500
	1000 nm (*w*) by 400 nm (*h*)	0	-	300
Structure based on Figure 6.1	400 nm (*w*) by 400 nm (*h*)	50	500	-
	1000 nm (*w*) by 400 nm (*h*)	0	200	-

According to Melloni *et al*. [98], fundamental mode (φ_1) arriving at the curved interface junction A results in the excitation of bend mode (φ_b) as shown in Figure 6.16. This φ_b travels at a phase velocity that differs from that of the input φ_1. The difference in phase velocities results in the mode being

deformed in shape, which occurs as uncoupled mode, φ_2. Depending on the design of the device, the φ_2, or deformed mode may be reconstructed back to its original profile, φ_1. This is by way of introducing waveguide offset at the interface between the straight and bent waveguides [117]. In the absence of the offset structure, φ_2, continues to propagate along the remaining section of the waveguide, with field radiating into the cladding layer [98].

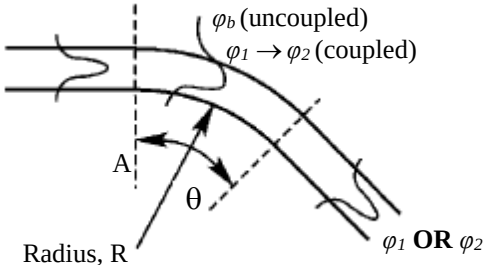


Figure 6.16 Schematic illustration of mode propagating in straight-bend-straight waveguide structure (reproduced from [113]).

The 2D FDTD simulation profile of the interlayer slope waveguide, shown in Figure 4.5, is designed with an offset introduced to the second slope interface. This allows the higher-order mode propagating after the second slope interface to be reconstructed. Similar simulation was performed for the interlayer slope waveguide with a 10° slope angle in the absence of waveguide offset. Figure 6.17 shows the 2D simulation profiles of the interlayer slope waveguide with a 10° slope angle, with (a) an offset, and (b) in the absence of offset. The removal of the offset from the second bend caused the loss to slightly increase from 0.03 dB to 0.04 dB, suggesting increased radiation [92, 98]. As explained earlier, the presence of radiated optical power in the cladding – which occurs due to surface perturbation can be coupled by the next neighbouring waveguide. This results in the increase of optical power. This finding suggests a lower saturated coupling loss of the fabricated crosstalk device with a structure based on Figure 6.1 than that of the crosstalk structure based on Figure 4.7.

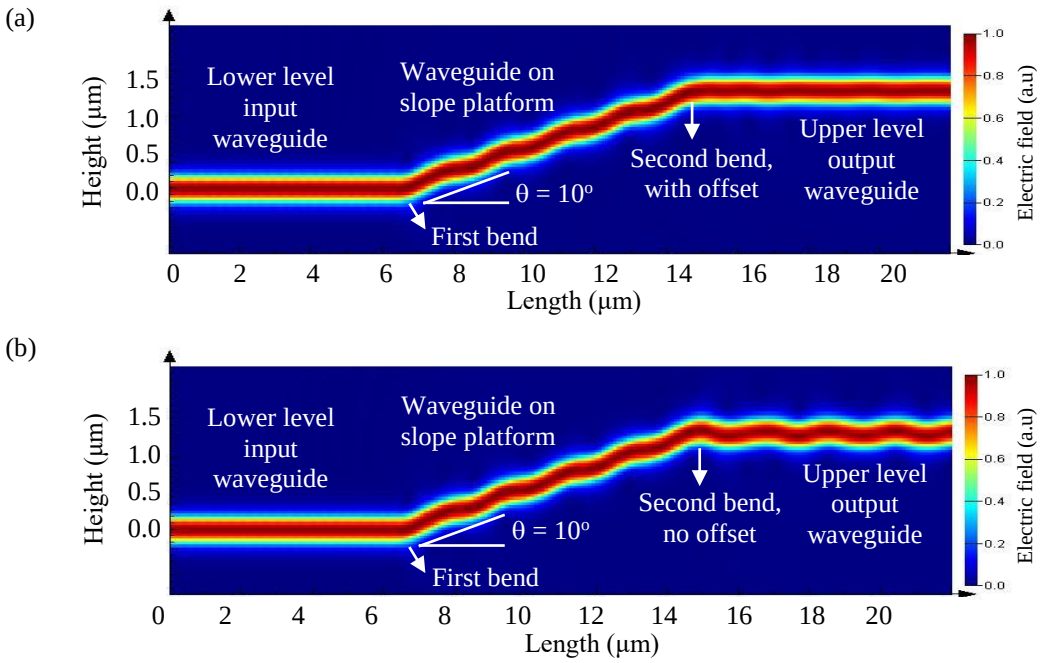


Figure 6.17 2D FDTD simulation profile of the interlayer slope waveguide with 10° slope angle, having (a) an offset, and (b) no offset.

By introducing surface roughness and a deformed waveguide to imitate the fabricated structure, a simulation based on the structure in Figure 4.7 was performed. Surface roughness as described in Section 5.5.2 was used. The structure shown in Figure 4.7, with modified structure for the upper level waveguide, was used. Depositing PECVD SiO_2 on an etched structure commonly results in non-conformal step coverage with voids surrounding the underlying structure [118]. If the surface of the PECVD SiO_2 film is not planarized, the uneven shape can be duplicated to the subsequent deposited layer, forming a bump on the waveguide. Figure 6.18 shows the SEM image of the cross-sectional view of a fabricated crosstalk device. A simulation was carried out to investigate the loss incurred from the bump structure. The waveguide dimensions are 400 nm (*w*) by 400 nm (*h*), with bump height estimated to be equal to 1.5 μm. The 2D FDTD simulation profile, as shown in Figure 6.19, shows that the mode gets scattered as it arrived at the bump interface and appearing as higher-order mode as it propagates along the bump section. Power monitors placed at the input (Monitor 1) and output (Monitor 2) of the waveguide shows loss of 7.2 dB. The high loss due to the bumpy waveguide must have contributed to the low transmission of the device, as shown in Figure 6.13.

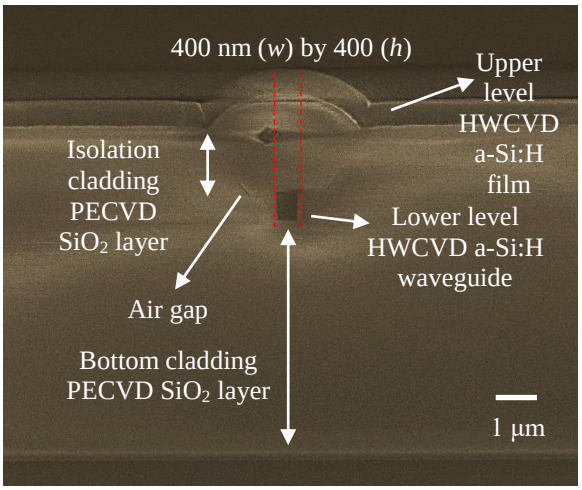


Figure 6.18 SEM of cross-sectional view of the crosstalk device, illustrating the un-even surface of PECVD SiO_2.

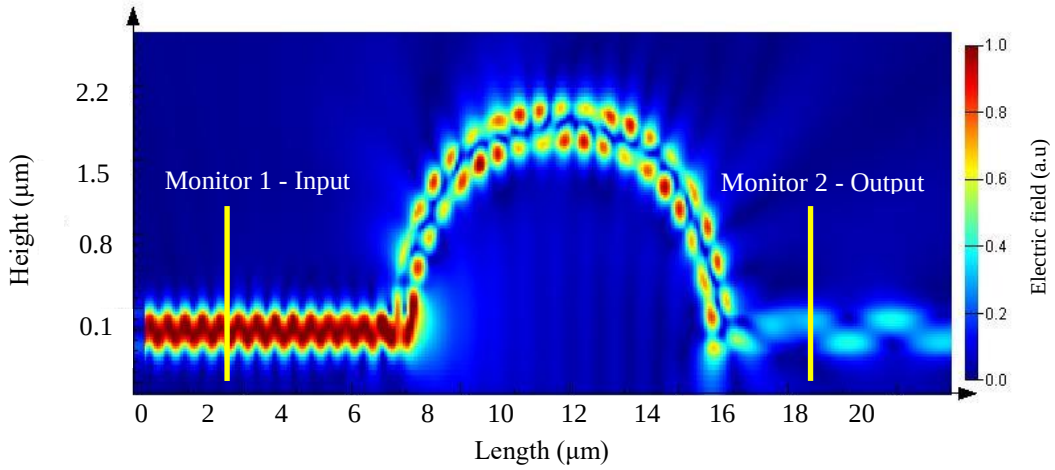


Figure 6.19 2D FDTD simulation profile of a bumpy waveguide to imitate the upper level waveguide structure due to unplanarized underlying surface.

The introduction of surface roughness and deformed shape in the upper level waveguide yielded, a closer correlation between the measured and the simulated results for the crosstalk structure based on Figure 6.1. Thus, it was concluded that any variation in core-guiding shape had various consequences for the propagating mode [119]. Light scattered into the cladding layer had the potential to be coupled to the next neighbouring waveguiding core. Table 6-2 shows the results of both the measurements and the simulations.

The measurement data validated the aim of the experiment, as they confirmed that the cladding height (designed for the interlayer slope waveguide) sufficiently isolated optical light from the input and output waveguides. Most importantly, the experiment demonstrated that the proposed interlayer slope waveguide could function as a real multi-layer interconnect.

Table 6-2 Results from measurement and simulation.

			400 nm (*w*) by 400 nm (*h*)		**1000 nm (*w*) by 400 nm (*h*)**	
Crosstalk waveguides structure	**Results obtained from:**		**Crosstalk (dB)**	**Isolation thickness (nm)**	**Crosstalk (dB)**	**Isolation thickness (nm)**
Structure based on Figure 7.1	Measurement	20 dB crosstalk isolation	-22	200	-21	50
	Simulation (no RMS)		-23	100	-20	50
Structure based on Figure 4.7	Simulation (RMS)		-22	100	-20	50
	Simulation (no RMS)		-20	50	-20	0
Structure based on Figure 7.1	Measurement	Maximum crosstalk isolation	-28	500	-33	500
	Simulation (no RMS)		-33	500	-43	400
Structure based on Figure 4.7	Simulation (RMS)		-35	500	-42	400
	Simulation (no RMS)		-50	500	-50	300

6.3 Fly-over Slope Waveguide

The schematic diagram of the fly-over slope waveguide is shown in Figure 4.18, and the modelling of the device is described in Section 4.4 of Chapter 4. This section presents the preliminary fabrication and the characterization of the device.

6.3.1 Mask Design

The fabrication of the fly-over slope waveguide required multiple steps in patterning. Similar to the previous device fabrication, the optical mask was used to pattern large rectangular structures to define the slope platforms, and the e-beam mask was used to pattern sub-micron waveguide structures with the grating couplers. In fabricating this device, the first layer to be fabricated was the alignment markers, referred to as Cell 1. The structures and dimensions of the alignment markers are shown in Figure 6.3.

Figure 6.20 shows the design of the optical mask with six sizes of rectangular structures used to form the slope platform for making the fly-over waveguide. This design is referred to as Cell 2.

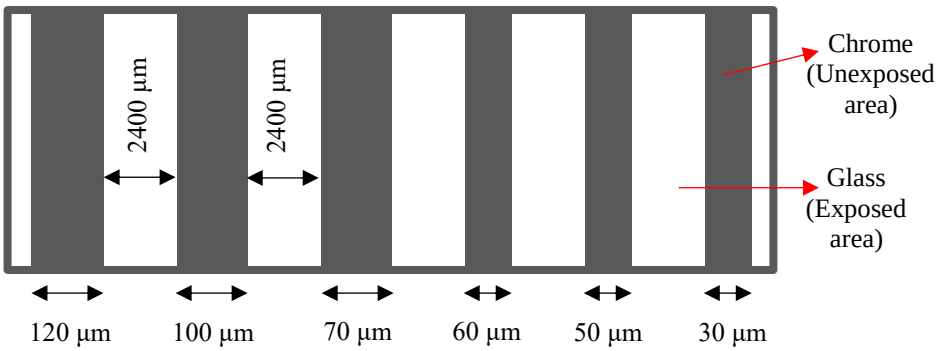


Figure 6.20 Schematic drawing of the optical mask used to define the slope platform for the fly-over waveguide.

The e-beam mask was designed to pattern the waveguide and grating coupler structures. Two e-beam cells were required. The first, Cell 3, was used to pattern the lower level crossing waveguides, including the grating couplers and opening box to clear up the HWCVD a-Si:H film for the top-level waveguides. The structure is illustrated in Figure 6.21.

The second e-beam cell, Cell 4, was used to pattern the upper level waveguide, including the grating couplers, and opening box to clear up the HWCVD a-Si:H film for the lower level crossing waveguides. Figure 6.22 is a schematic drawing of the upper level waveguide structure. Cell 3 and Cell 4 were then aligned and placed on Cell 2 of the optical mask, as shown in Figure 6.23.

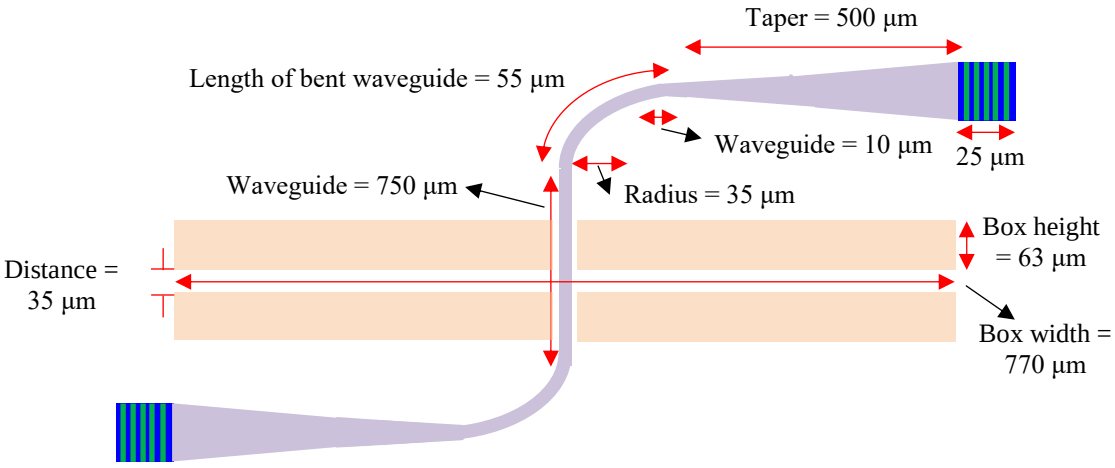


Figure 6.21 Schematic drawing of the lower level waveguide with opening box to clear up the HWCVD a-Si:H film.

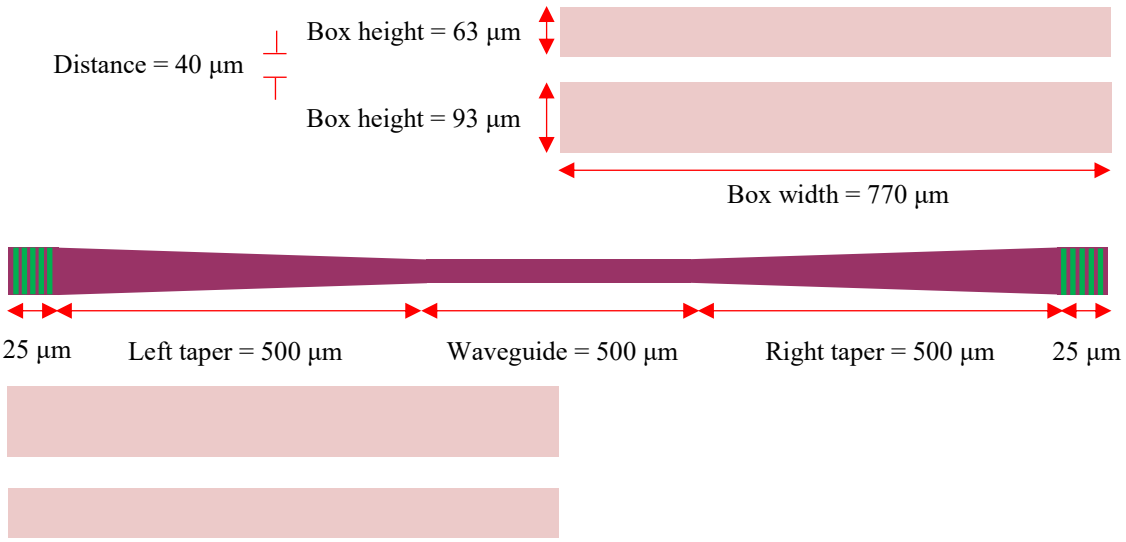


Figure 6.22 Schematic drawing of the upper level waveguide with opening box to clear up the HWCVD a-Si:H film.

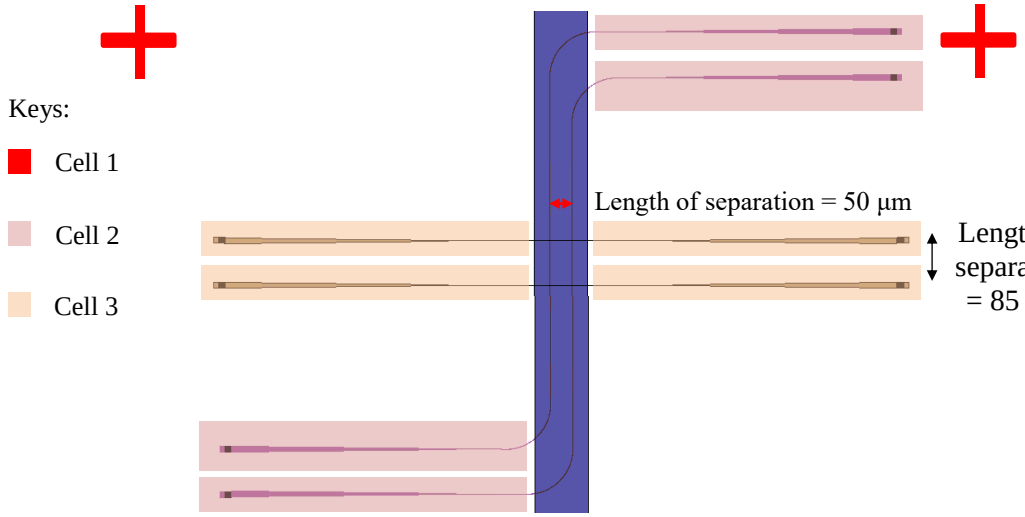


Figure 6.23 Schematic drawing of the fly-over slope waveguide, illustrating the e-beam masks of the upper level waveguide placed perpendicularly to the lower level waveguide, and aligned with the rectangular structure of the optical mask.

6.3.2 Device Fabrication

The details of fabricating the fly-over slope waveguide are described in this section. The steps of the fabrication process are illustrated in Figure 6.24 (a) to (o). The fabrication of the device started with the deposition of PECVD SiO_2 with a film thickness of 4.5 µm on a silicon substrate. The recipe used for the SiO_2 deposition is shown in Table A.1 of Appendix A. Then the wafer was cut into small samples of 4.2 cm by 2.5 cm each. This was followed by the coating of e-beam positive resist, ZEP520, which was used to pattern the alignment markers by e-beam lithography. The resulting resist thickness was approximately 900 nm. The recipe used to spin and develop the 900 nm thick ZEP520 appears in Table A.6 of Appendix A.

After developing the e-beam resist, the sample was dry etched in the RIE tool using fluorine-based gas to form deep etched trenches of alignment markers. It was important to achieve low flow rates for both precursor gases, trifluoromethane (CHF_3) and Argon (Ar), for the e-beam resist to withstand being etched. With a 30 minutes, approximately 750 nm of SiO_2 was etched and approximately 420 nm of ZEP remained. The recipe for the dry etching appears in Table A.9 of Appendix A. The fabrication process was followed by deposition of the first layer 400 nm thick HWCVD a-Si:H film. The recipe for depositing the HWCVD a-Si:H appears in Table A.3 of Appendix A.

Then, e-beam positive resist, ZEP520, was again used to coat the surface of the sample to pattern the lower level waveguides by e-beam lithography. The resulting resist thickness was approximately 500 nm. The recipe used to spin and develop the 500 nm thick ZEP520 can be found in Table A.5 of Appendix A. Then, sub-micron sized waveguide structures were patterned onto the sample using a JEOL JBX 9300FS e-beam tool. The beam conditions can be found in Table B.1 of Appendix B. Afterwards, the sample was dry-etched in the ICP tool using fluorine-based gas to form a fully-etched strip waveguide structure. The details of the recipe for using ICP to etch the HWCVD a-Si:H film appear in Table A.10 of Appendix A.

Following the patterning and etching of the first layer HWCVD a-Si:H waveguides, silicon nitride (Si_3N_4) was deposited as a sacrificial layer to protect the underlying HWCVD a-Si:H devices [120, 121]. This was an important step to prevent the HWCVD a-Si:H film from being attacked by the HF^{2-} molecules which were present in the NH_4F:HF (7:1) [122]. The Si_3N_4 with approximately 50 nm film thickness was deposited by the Helios tool. The recipe used to deposit Si_3N_4 using Helios tool is shown in Table 6-3. Because the Helios tool was not exclusively used in making any of the devices fabricated in this project, the full description of the tool is not included.

The Si_3N_4 film deposited by Helios was used after the unsuccessful fabrication using PECVD Si_3N_4 as a hard mask for the underlying HWCVD a-Si:H waveguides. In the first few attempts of fabricating the device, PECVD Si_3N_4 film with a thickness of roughly 30 nm was etched in NH_4F:HF (7:1). Si_3N_4 is resistant to chemical etching due to its strong covalent bonds [123], with etching rates of 1 nm/ minute in NH_4F:HF (7:1) [124]. However, the material was not compatible with the fabrication project.

Table 6-3 Recipe for the deposition of Si_3N_4 by Helios tool.

Si Target	
Ar (sccm)	40
N_2 (sccm)	30
Plasma power (W)	2000
D.C generator (W)	3000
Temperature (^oC)	38.2
Voltage (V)	774
Current (A)	4.2
Deposition rate (nm/sec)	0.17

There were three assumptions for the fast etching of PECVD Si_3N_4:

1) The deposited PECVD Si_3N_4 may contain high amount of N-H bonds [125] due to the incorporation of NH_3 gas as one of the precursor, in depositing the film. The standard recipe to deposit Si_3N_4 using the PECVD tool is shown in Table A.2 of Appendix A. In general, N-H bonds are weak [126] and thus can effectively be etched by HF^{2-} reactant etching species.
2) The film was deposited at a low temperature, 350°C. This resulted in high concentration of hydrogen, making the film porous which increased the etching rate in HF solutions [127].
3) The poor conformality of the PECVD deposition resulted in fast etching of the sidewalls of the Si_3N_4 film [118]. As a result, the HF solutions penetrated to the underlying HWCVD aSi:H film and attacked the grating couplers. Figure 6.25 shows the optical microscope images of the film delamination.

Following the deposition of Si_3N_4 using the Helios tool, the fabrication process was continued with the deposition of 1.5 μm thick PECVD SiO_2 (recipe in Table A.1 of Appendix A). After the 1.5 μm thick PECVD SiO_2 was deposited for the waveguide's isolation layer, S1813 G2 positive photoresist was spun on the sample to prepare it for optical lithography. Then the sample was exposed to UV light using EVG620TB, a mask aligner system to generate the multiple box structures. The recipe for the photolithography can be found in Table A.4, Appendix A. The fabrication process was followed by wet etching the sample in NH_4F:HF (7:1) for 4 minutes, at room temperature, to define the slope profile [108]. During this wet etching, approximately 1 μm of PECVD SiO_2 was removed, producing a slope angle of roughly 7°.

Then a second layer of 400 nm thick HWCVD a-Si:H film was deposited on the sample. This was followed by coating the surface of the sample with ZEP 520 e-beam resist to pattern the upper level waveguides.

After developing the e-beam resist, the sample was dry etched in ICP tool using fluorine-based gas to form a fully-etched waveguide structure. The details of the recipe for using the ICP to etch the a-Si:H film appear in Table A.10, Appendix A. As a final step, the sample was cladded with 1 μm thick PECVD SiO_2 to serve as the top cladding layer. Figure 6.26 shows the SEM image of the cross-sectional view of the fly-over slope waveguide. Figure 6.27 shows the top view of the fabricated fly-over waveguide cladded with 1 μm thick PECVD SiO_2. Figure 6.28 shows the optical microscope images of the fabricated and un-cladded fly-over waveguide. Bubble-like features are visible on the film surrounding the device. This was probably caused by the lattice mismatch between the many layers of films that occurred during the deposition process. These bubble-like features only appear after the deposition of the 1.5 μm PECVD SiO_2. It was suggested that the Si_3N_4 film, which serve as a sacrificial layer deposited at a temperature equal to 38.2°C using the Helios tool, could not tolerate the high temperature deposition (at 350°C) of the PECVD SiO_2 film. This results in stress of the lattice network of the Si_3N_4 film, which eventually breaks and appear as bubbling effect on the film.

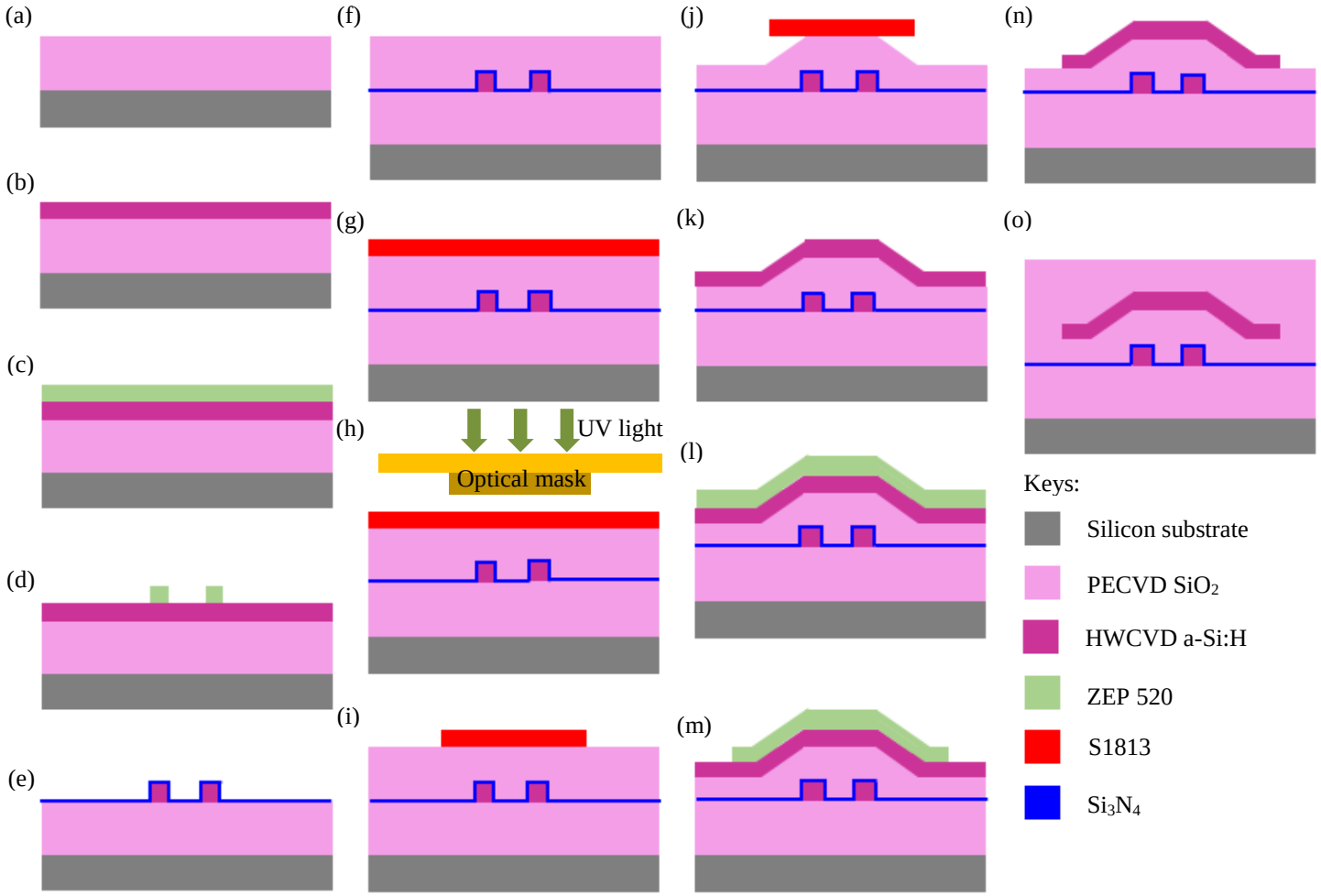


Figure 6.24 Fabrication steps for making the fly-over waveguide.

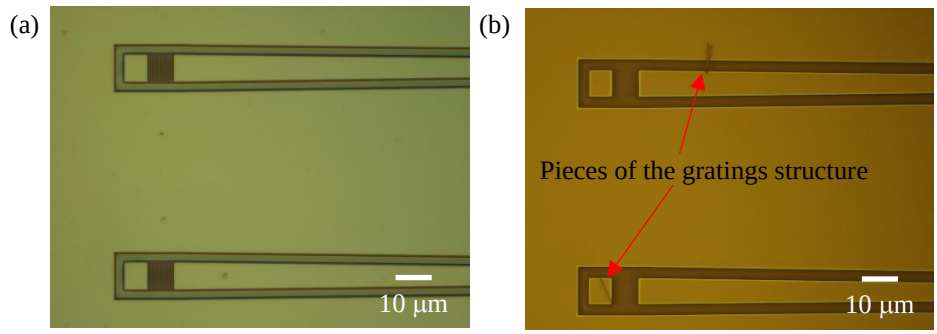


Figure 6.25 Optical microscopy images showing the delamination of the HWCVD a-Si:H gratings structure, using PECVD Si_3N_4 as the hard mask. (a) Before immersing the sample in HF solution, and (b) after immersing the sample in HF solution, to form the slope platform.

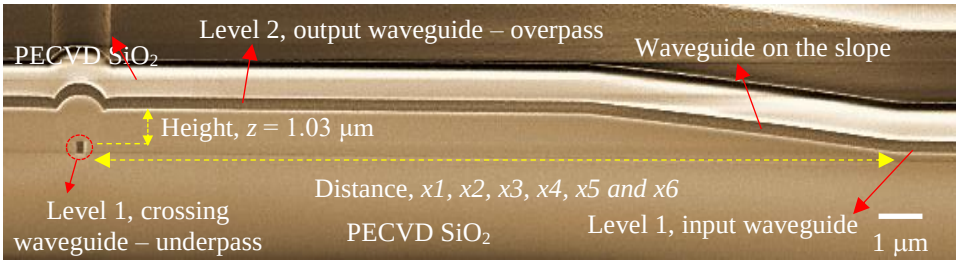


Figure 6.26 SEM image of cross-sectional view of the fly-over slope waveguide, showing lower level HWCVD a-Si:H waveguide, and upper level HWCVD a-Si:H waveguide, isolated with 1 µm PECVD SiO_2.

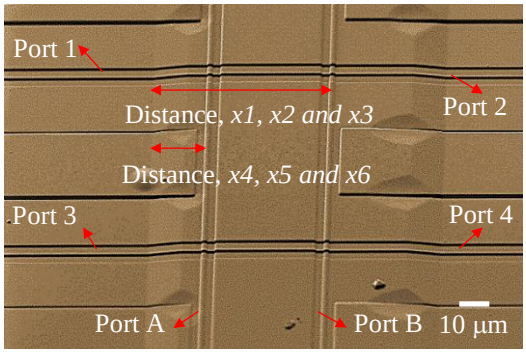


Figure 6.27 SEM image of top view of the cladded fly-over slope waveguide.

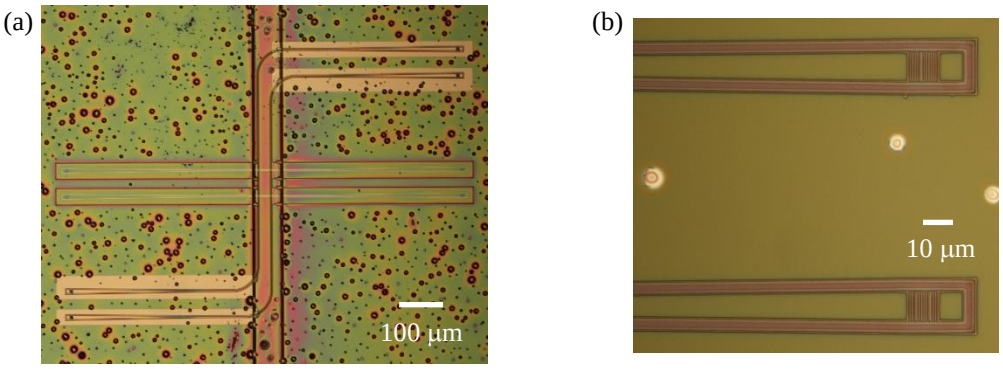


Figure 6.28 Optical microscope images of the un-cladded fabricated fly-over slope waveguide for, (a) the whole device, and (b) grating couplers from the lower level HWCVD a-Si:H waveguides.

6.3.3 Measurement Results

To characterize the device, the transmission of the four crossing waveguides was measured using the set-up described in Section 5.4. The coupling between the upper and lower waveguides was characterized with respect to the distance (x) between the two waveguides, in the x-direction, as indicated in Figure 6.29. Figure 6.29 is a schematic diagram showing the approach which was used to determine the coupling between the waveguides placed across the slope platform with the crossing waveguides placed beneath the slope structure.

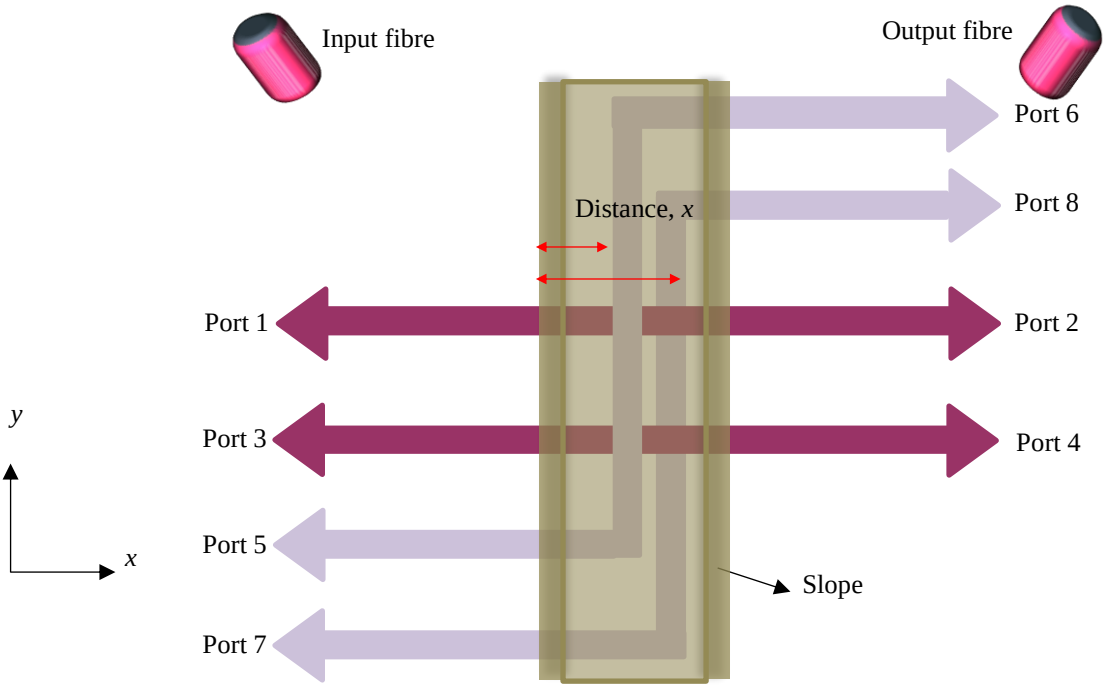


Figure 6.29 Schematic diagram of crosstalk measurements for the fly-over waveguides.

The methods of characterization were as follows. First, the input and output fibres were aligned to the grating couplers of Port 1 and Port 2, respectively. Then the transmission was recorded as Loss 1-2. The output fibre was then moved and aligned to the grating couplers of Port 6. The transmission was recorded as Loss 1-6. Loss 1-6 minus Loss 1-2, yields the crosstalk of the two waveguides. The method was repeated for all the ports of the waveguides. The waveguides were measured with six values of distance, x, as indicated in Figure 6.29 and Figure 6.30. Figure 6.30 (a) to (c) show the optical microscope images of the four crossing waveguides from three devices, with varying distance, x.

The values of the distance of separation between the two crossing waveguides in the x direction are shown in Table 6-4. Altogether, there were 12 possible paths as indicated in Figure 6.30. The path mapping is summarized in Table 6-5.

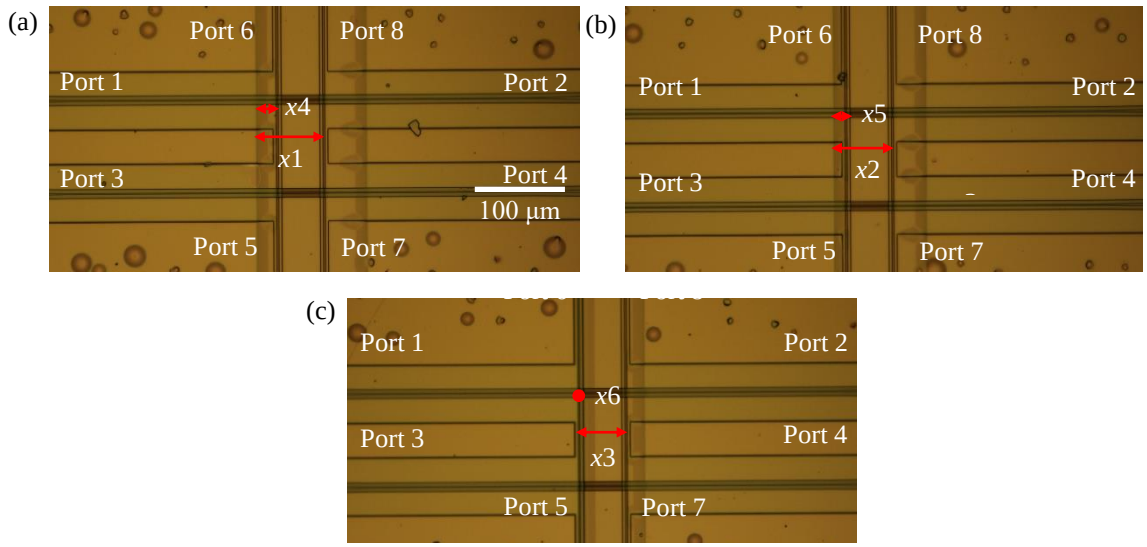


Figure 6.30 Optical microscope images of the un-cladded fabricated fly-over waveguide devices for varying distance *x*, for (a) Device 1, (b) Device 2, and (c) Device 3.

Table 6-4 Values of distance of separation of two crossing waveguides, *x*.

Position of *x*	**Distance (µm)**
*x*1	71
*x*2	61.9
*x*3	49.2
*x*4	21.9
*x*5	12.6
*x*6	0

Table 6-5 Possible crosstalk paths between the interlayer slope waveguide and the crossing waveguides placed beneath the overpass waveguide, in the *x*-direction.

		Position of *x*					
		*x*1	*x*2	*x*3	*x*4	*x*5	*x*6
Possible Paths	Crossing waveguides	Port 1 – 2	Port 1 – 2	Port 1 – 2	Port 1 – 2	Port 1 – 2	Port 1 – 2
		Port 1 – 8	Port 1 – 8	Port 1 – 8	Port 1 – 6	Port 1 – 6	Port 1 – 6
	Crossing waveguides	Port 3 – 4	Port 3 – 4	Port 3 – 4	Port 3 – 4	Port 3 – 4	Port 3 – 4
		Port 3 – 8	Port 3 – 8	Port 3 – 8	Port 3 – 6	Port 3 – 6	Port 3 – 6

The results of the loss measurements are presented in Figure 6.31. Figure 6.32 shows the spectral transmission of the two output ports of the fly-over device with a 21.9 µm separation (*x*4), in the *x*-direction.

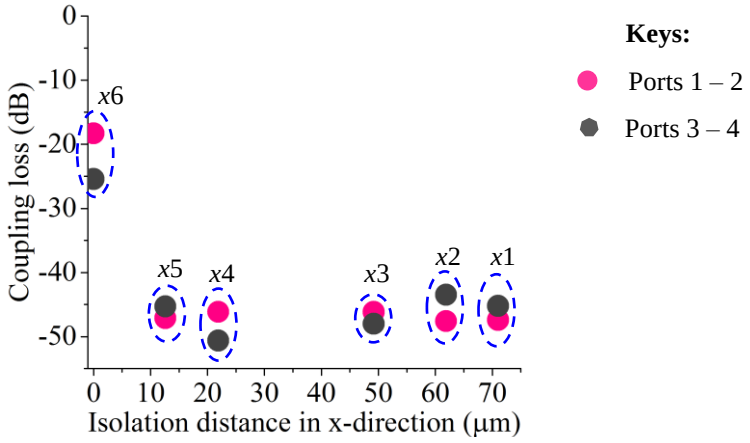


Figure 6.31 Measurement of the coupling loss for the possible 12 paths.

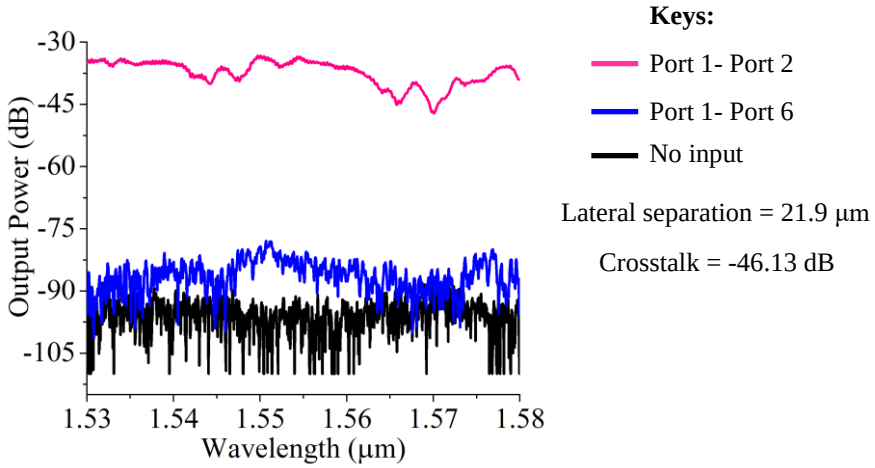


Figure 6.32 Transmission data of Ports 1 - 2 and 1 - 6, with lateral separation (*x*4) equal to 21.9 μm.

6.3.4 Analysis and Discussion

The design of the fly-over waveguide coupler demonstrated that waveguides placed across the slope platform referred to as “overpass”, did not couple with crossing waveguides placed below the slope platform referred to as “underpass”. According to the simulation discussed in Section 4.3.1 (Chapter 4), this principle should work for isolation thickness larger than 1 μm. In the design structure shown in Figure 4.18, two waveguides, A and B, lay on the same plane as the lower level input and output of the fly-over waveguide. In fabricating the proposed structure, high precision of alignment in joining the first and second deposited films was required. Figure 6.33 shows the schematic of the simplified proposed fabrication steps to obtain the structure shown in Figure 4.18. Because of time constraints while fabricating the device, a simpler step was used. As shown in the fabrication steps in Figure 6.24 (a) to (o), the underpass waveguides, A and B, lay on different planes from the input and output of the fly-over slope waveguide. However, the device was fabricated with a profile as close as possible to the proposed structure.

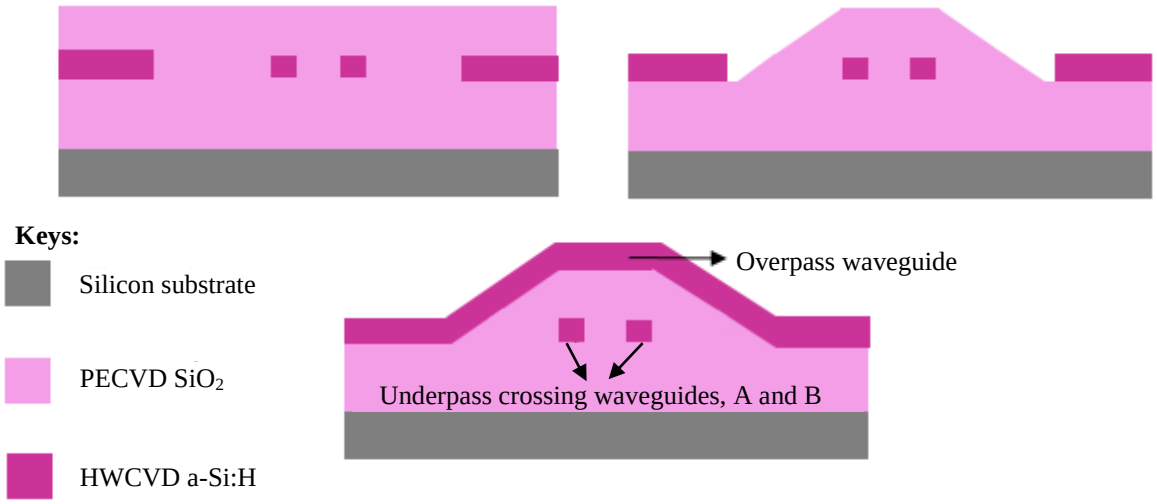


Figure 6.33 Proposed fabrication steps for the underpass crossing waveguides, A and B, to lie on the same plane with the input and output of the fly-over slope waveguide coupler.

By controlling the time during wet etching of the PECVD SiO_2 isolation cladding layer, approximately 290 nm of film thickness was left on the lower level slope platform. This meant that the underpass crossing waveguides were vertically isolated by 290 nm from the input and output of the fly-over slope waveguide.

Another fabrication feature which needs explanation is the unplanarized SiO_2 isolation cladding layer. As discussed in Section 6.2.4, this resulted in the formation of a bump on the upper level waveguide. Figure 6.34 shows an SEM image of the upper level waveguide resulting from duplication of the underlying film profile. In Section 6.2.4, a simulation was conducted to investigate the loss incurred by the bumpy structure, showing loss equal to 7.2 dB.

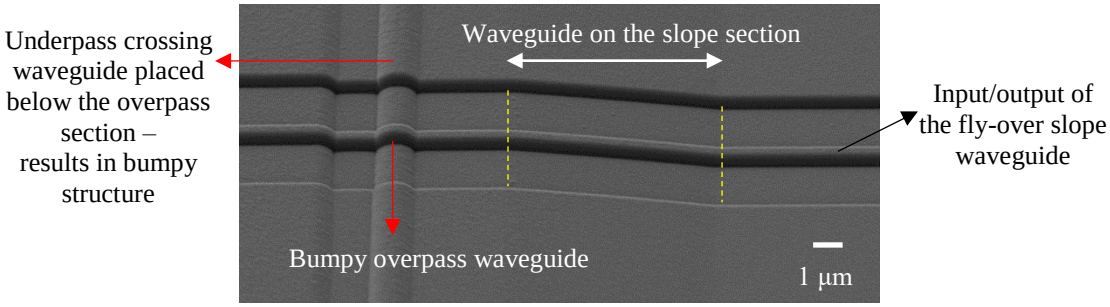


Figure 6.34 SEM image of the fly-over waveguide, focusing on the bumpy overpass waveguide.

The description of the fabricated structure is useful for understanding the analysis of the measurements. The device is characterized in terms of coupling loss with varying distance, *x*. The method of characterization was the same as that described in Section 4.4 of Chapter 4. With an exception, the underpass crossing waveguides were vertically isolated by 290 nm from the input and output of the fly-over waveguide. Figure 6.35 illustrates the schematic of the closed-up structure. In Figure 6.30, for $x1$, the underpass crossing waveguides were placed below the overpass structure. This meant that the waveguides were isolated by approximately 1.03 μm. By contrast, the underpass

waveguide for *x*6 was placed directly below the input of the fly-over waveguide. This meant that the waveguide A was vertically separated by approximately 290 nm in the *z*-direction, and by 0 nm in the *x*-direction, from the slope interface. This explains the -18 dB coupling.

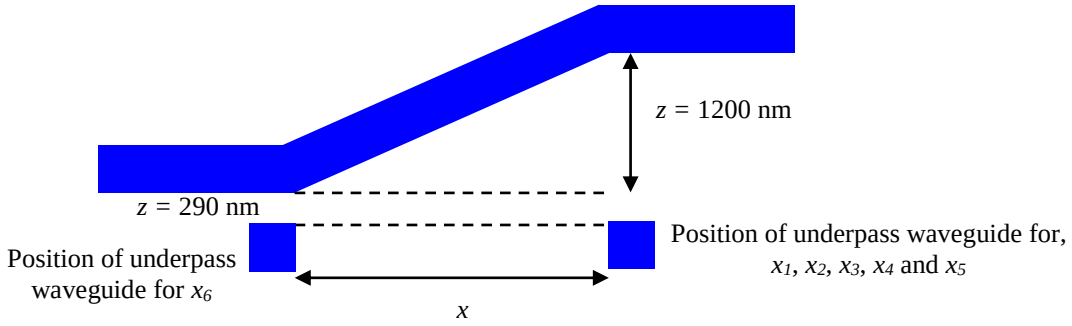


Figure 6.35 Schematic of the closed-up fabricated structure.

The measurement results shown in Figure 6.31 correlate with the simulation results in Figure 4.22. The measurements showed that crosstalk with an average value of -45 dB was achieved for waveguide separation larger than 1 μm in the *z*-direction and larger than 10 μm in the *x*-direction. As the waveguides were placed closer (*x*6) the crosstalk increased to approximately -18 dB. This result suggests that optical mode from the input of the fly-over slope waveguide coupled to the underpass waveguide due to the close vertical separation.

6.4 Summary

The measurements of the crosstalk experiment validated the simulation results, with smaller waveguides requiring thicker isolation than larger waveguides. It was figured that crosstalk between a crossing waveguide placed on top or below a slope waveguide, and two straight waveguides placed in perpendicular on top of each other, would have different characteristics. Crossing waveguide placed above or below a slope platform displayed higher crosstalk than straight crossing waveguides. This was due to the radiating mode at the slope interface and evanescent field from the higher-order mode propagating along the waveguide on the slope, being coupled to the nearby crossing waveguide, thus increasing the transmission.

The measurements of the fly-over slope waveguide confirmed that waveguide separation of larger than 10 μm in the *x*-direction and 1 μm in the *z*-direction, can sufficiently isolated crossing waveguides placed below the slope structure. The fabrication of the device was still at a preliminary stage and thus the device was not perfectly fabricated, with bumps resulting from unplanarized film. However, the proposed fly-over slope waveguide showed promising results and characteristics. The research demonstrated its potential for use as a multilayer interconnect in a multilayer silicon photonics platform.

Chapter 7 Summary and Future Work

This chapter summarizes the motivation and objectives of the project and briefly reviews the conclusions. Recommendations are proposed to improve certain aspects of the fabricated interlayer slope waveguide coupler and the crosstalk devices.

7.1 Summary

The last decade has seen the growth of silicon photonics (SiP) as a platform to potentially revolutionise various technological areas, including telecommunications, high-performance computing, security and sensing [1, 2]. This development stems from the following advantages that silicon-on-insulator (SOI) exhibits:

1) The fabrication of SOI photonics is compatible with CMOS fabrication processes, leading to a high-volume production at low cost [2].
2) The high index contrast between crystalline-silicon (c-Si) and silicon dioxide (SiO_2) (Δn, c-Si/SiO_2 = 3.47/1.45 = ~2.4) facilitates the convenience of building ultra-compact structures [8]. This property is the most fundamental in IC processing for large-scale, high-density integration on a chip [4].
3) c-Si has a large energy bandgap, allowing the material to be transparent in the 1550 nm wavelength window [8], which is an excellent property for building planar waveguide circuits [4].

Although c-Si is remarkable in terms of its optical properties, its development is restricted to two-dimensional (2D) circuit configuration. This is mainly due to the complexity of the growth process of c-Si, limiting further layers of optical components from being added to the integrated circuit. Turning the 2D circuit configuration into a 3D multilayer platform is beneficial as it offers highly dense components in a small footprint area [5, 75]. However, the challenge in realizing multilayer technology is to make 3D vertical optical vias to connect vertically stacked optical components through depositable material that is compatible with CMOS processes. Researchers have sought suitable materials for the multilayer technology, as discussed in Chapter 2. In parallel, researchers are exploring various ways of coupling light vertically using depositable materials and other suitable materials, as listed in Table 2.3.

The essential requirements for developing vertical interconnect are that the process of fabricating the 3D waveguiding structure must be CMOS compatible, and the process must be repeatable and simple in terms of fabrication. In this project, an interlayer slope waveguide coupler is proposed. The structure comprises an input waveguide placed at a lower plane and an output waveguide placed at an upper plane, connected by a waveguide on a slope. The structure has a slope angle (θ) and a large

slope height of 1.5 μm, with a slope length calculated from the two known parameters. The structure is analogous to an S-bend waveguide, which is designed to guide light up or down a multilayer platform, similar to electrical wiring in a CMOS infrastructure. Here, a large slope height (1.5 μm) is necessary to avoid mode coupling between the input and output waveguides, which are placed at the lower and upper planes. For real multi-level application, it is necessary to provide sufficient isolation so that any crossing waveguides placed on the same plane with the lower level input and output waveguides do not couple.

The characteristics of the proposed interlayer coupler are determined by the value of the slope angle. Knowing the values of the slope angle and the slope height allows the calculation of the bend radius of the slope structure. This information can then be used as a foundation to understand the loss characteristics of the interlayer slope waveguide, based on the theory of waveguide bend. The figure of merit of the device is assessed in terms of loss in dB per slope.

As an initial characterization, the 3D interlayer slope waveguide coupler was modelled using Lumerical FDTD Solutions software to investigate the effect of varying the slope angle on the transmission of the device. A detailed analysis was presented in Section 4.2.3 (Chapter 4). The simulation results showed that the lowest transmission, below 1 dB, was achieved for slope angles below 35^{o}. Higher loss occurred with larger slope angles of above 55^{o}, caused by a mode-mismatch through the bend, similar to any bend waveguides with a small radius curvature.

After the simulation study, the device was fabricated. Fabrication started with the deposition of 4.5 μm plasma-enhanced chemical vapour deposition (PECVD) SiO_2.The initially deposited PECVD SiO_2 film served two functions: (i) as a bottom cladding layer, and (ii) as a platform for the slope structure, which was defined by wet-etching using buffered hydrofluoric acid, NH_4:HF (7:1) through optical lithography. Two types of positive resist S1813 were used, S1813 G2 and S1813 G2 (SP15). The difference between the two was that surface adhesion promoter had been added to the S1813 G2 (SP15) to increase the stickiness of the surface of the etching material [106], PECVD SiO_2 film. In wet-etching the samples for 5 minutes, two slope angles were obtained, ~11.8^{o} and 20.8^{o}. Further, in post-baking the S1813 G2 and S1813 G2 (SP15) resulted in two slope angles, 16.7^{o} and 25.3^{o}. Through the 5 minutes etching, all devices were etched to a depth of approximately 1.45 μm. Then, hydrogenated amorphous silicon (a-Si:H) film was deposited at a low temperature using a hot-wire chemical vapour deposition (HWCVD) tool [15]. Sub-micron-sized waveguides with grating structures were then patterned using electron-beam (e-beam) lithography and dry-etched using fluorine-based chemistry. The dry-etching fully etched the gratings and the waveguides. Waveguides with dimensions of 400 nm (w) by 400 nm (h) and 600 nm (w) and 400 nm (w) were obtained. Then, all samples were cladded with 1 μm PECVD SiO_2.

In measuring the devices, slope losses of 0.21 dB/slope and 0.47 dB/slope were obtained from the lower and higher slope angles (11.8^{o} and 25.3^{o}, respectively) for 400 nm (*w*) by 400 nm (*h*)

waveguide dimensions. The measurement results conformed to the simulation results, with the loss increasing as the slope angle increased. As discussed in Section 5.5.1 of Chapter 5, increased loss was contributed from optical mode-mismatch. Optical mode-mismatch resulted from a sudden change in effective index as the mode propagated from the straight waveguide to the slope interface.

In further analysing the cause of the loss of the slope, atomic force microscopy (AFM) was used to measure the surface roughness of the PECVD SiO_2 and HWCVD a-Si:H films. The AFM measurements revealed root mean square (RMS) surface roughness values of 2.1 nm and 4.2 nm for lower and upper plane PECVD SiO_2, respectively. The corresponding values for lower and upper plane HWCVD a-Si:H films were 1.35 nm and 3.99 nm. These results are shown in Table 5-3. The cause of variation in the values of RMS surface roughness from one plane to another was the breaking of the S-O covalent bonds of the SiO_2 film by HF^{2-} molecules during the wet-etching process, which rendered the lower level plane smoother. Here, the surface roughness of the underlying PECVD SiO_2 was transferred to the deposited HWCVD a-Si:H film.

Lumerical FDTD simulations was used to characterize the effect of introducing surface roughness to the interlayer slope waveguide. As shown in Table 5-5, the loss of the slope increased by less than 0.1 dB. The simulation results correlated closely with the experimental results. Also, it was observed that losses for larger width waveguides were slightly lower than the narrower waveguide with the same slope angles. This suggests that mode in a waveguide with larger width, travelling through the slope interfaces, is relatively immune to bend losses due to the higher effective index of the mode.

An experiment on crosstalk was also performed. The aim was to investigate the minimum cladding thickness required to isolate two waveguides placed in perpendicular on top of each other. The device was designed, fabricated and characterized as described in Section 6.2 (Chapter 6). Two waveguide widths were fabricated, 400 nm (w) by 400 nm (h) and 1000 nm (w) by 400 nm (h). The fabricated structures are presented in Figure 6.1. The measurements shows that the 400 nm (w) by 400 nm (h) structure could be isolated by -22 dB with 200 nm waveguide separation. The 1000 nm (w) by 400 nm (h) could be isolated by -21 dB with 50 nm waveguide separation. The measured results conformed to the theory and simulated results, with smaller waveguides requiring higher isolation than larger waveguides. This is primarily due to the lower optical confinement in the 400 nm (w) by 400 nm (h) waveguides compared to the 1000 nm (w) by 400 nm (h) waveguides. The evanescent field of the smaller waveguides tended to radiate into the cladding. Furthermore, if there exist any waveguides placed in close proximity to the first waveguide and having the same effective propagation constant (β), light can be coupled and this increases the transmission.

In demonstrating how the interlayer slope waveguide functioned as an actual waveguide coupler in a multi-level platform, a device called fly-over waveguide was designed and fabricated. The structure is shown in Figure 4.18. The device comprises a bridge-like structure made from the slope platform with two crossing waveguides placed underneath. The fabrication and the experiment were at a

preliminary level due to limited time for finishing the work. The conclusion drawn from this experiment was that crosstalk with an average value of -45 dB can be achieved when the separation between the two crossing waveguides, in the *x* and *z* directions, is larger than 1 μm. In addition, coupling increases to -18 dB as the underlying waveguide is placed 290 nm closer to the slope interface. The measured results correlated with the simulated results, as shown in Table 4.7.

In conclusion, results from the three main experiments demonstrated that the proposed interlayer waveguide coupler has the potential for use as a 3D vertical optical coupler in multilayer SiP circuits. In this work, all fabrication processes were regulated below 400°C for FEOL and BEOL compatibility. The design of the interlayer coupler is compact, with high index material (n = 3.55), short slope length of 8.5 μm, and thick cladding height of 1.5 μm. In addition, isolation of -22 dB was demonstrated with a minimum cladding thickness of 200 nm for waveguide dimensions of 400 nm (w) by 400 nm (h). This value confirmed that the cladding height of 1.5 μm, modelled in the proposed interlayer slope waveguide coupler, was more than sufficient to avoid crosstalk between two orthogonal waveguides.

7.2 Recommendations for Future Work

Several recommendations are proposed here to improve the characteristics of the devices fabricated in this work.

1) The interlayer slope waveguide coupler.

i) The varying surface roughness of the lower and upper planes was observed to have an effect when measuring the transmission of different numbers of slopes. This was because the input and output tapers were placed on two different planes. For example, one side of the taper for waveguides having one, three and five slopes interacted more with the rough interfaces on the upper level. By contrast, tapers for two and four slopes interacted less with the rough interfaces. Thus, it is recommended that PECVD SiO_2 film be smoothed out before the waveguiding film is deposited. Smoothing can be done by the following methods:

   a. Performing chemical mechanical polishing (CMP) on the deposited PECVD SiO_2 film before performing optical lithography and wet-etching processes.
   b. In the absence of a CMP tool, the PECVD SiO_2 can be immersed in NH4:HF (7:1) before pattern generation and slope etching processes.
   c. Other materials, such as PECVD tetraethyl orthosilicate (TEOS) oxide, can be used; this material has a smoother surface than PECVD SiO_2 [128]. However, using it would mean that the wet-etching process to obtain the slope etching profile must be further investigated and optimised.

ii) The waveguiding material is not restricted to HWCVD a-Si:H film. It can be other CMOS-compatible depositable silicon-based materials, such as low-loss silicon nitride (Si_3N_4). Polycrystalline silicon (poly-Si) can potentially be used as the waveguiding material, provided that the inhomogeneous grain structures of the film can be tackled through low-temperature treatment processes.

iii) Because the high refractive index of HWCVD a-Si:H (n = 3.55) is so close to that of c-Si (n = 3.45), hybrid guiding material can be realized. This would mean that c-Si waveguide connected to a modulator placed on the lower level plane can be connected to the HWCVD a-Si:H interlayer slope waveguide bringing the optical signal up to the upper level plane.

iv) The number of layers of the interlayer slope waveguide structure is not restricted to two. The design can be increased to three layers, with a staircase structure, analogous to electrical interconnects. Preliminary simulation showed a 0.08 dB loss for a 10° slope angle. Figure 7.1 illustrates a 2D simulation of the proposed staircase interlayer slope waveguide structure at a 10° slope angle.

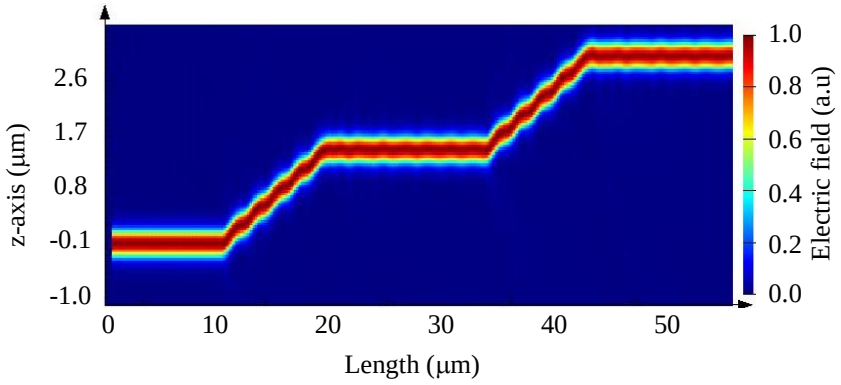


Figure 7.1 FDTD 2D simulation profile of staircase interlayer slope waveguide coupler at a 10° slope angle.

v) Other passive optical devices such as a directional coupler with a Y-junction structure and ring-resonator can be placed at the upper or lower level interlayer slope waveguide, to increase the number of levels of the multilayer platform.

vi) For the interlayer slope waveguide coupler to be more susceptible to mode transition loss between the straight and slope interface, increasing the waveguide dimensions through a taper structure at the slope junctions can reduce mode-mismatch for lower bending and insertion loss [129, 130]. This structure would make the fundamental mode have less effect on the change in direction of propagation because of the smaller effective index difference.

2) The orthogonal crosstalk waveguide.

i) The isolation cladding layers should be planarized before the deposition of the second-layer crossing waveguide. This can reduce the scattering from the bumps of the deformed second-layer waveguide.

ii) The opening box to clear out the top layer HWCVD a-Si:H was not large enough. This resulted in the coupling of mode from the first-layer waveguide to the top high-index HWCVD a-Si:H. As a consequence, the transmission was quite low. The structure of the opening box must be larger to prevent unnecessary coupling to the high-index film.

3) The fly-over waveguide.

i) The step coverage of PECVD SiO_2 deposition was not conformal, resulted in the sidewalls being etched faster than the planar areas. This became one of the biggest challenges in fabricating the device. When the sample was immersed in NH_4:HF (7:1), the acid penetrated to the bottom layer of HWCVD a-Si:H waveguides. Because the material was amorphous, the film was delaminated and etched the grating structure. Thus, other materials such as Si_3N_4 or c-Si should be used as the lower level waveguides, as they are less affected by NH_4:HF (7:1)

ii) Another option is to use less concentrated NH_4:HF (20:1) to avoid fast etching of the PECVD SiO_2 when forming the slope structure.

Appendix A Fabrication Recipes

A.1 Deposition

A.1.1 Plasma-Enhanced Chemical Vapour Deposition (PECVD)

Table A-1 shows the standard SiO_2 deposition recipe using PECVD.

Table A- 1 PECVD recipe for SiO_2 deposition.

SiH_4 (sccm)	4.2
N_2 (sccm)	80
N_2O (sccm)	350
Pressure (mTorr)	1000
RF power (W)	20
Temperature (°C)	350
Deposition rate (nm/sec)	1.17

Table A-2 shows the standard Si_3N_4 deposition recipe using PECVD.

Table A- 2 PECVD recipe for Si_3N_4 deposition.

SiH_4 (sccm)	12.5
NH_3 (sccm)	20
N_2 (sccm)	500
Pressure (mTorr)	750
RF power (W)	20
Temperature (°C)	350
Deposition rate (nm/sec)	0.27

A.1.2 Hot-Wire Chemical Vapour Deposition (PECVD)

Table A-3 shows the standard a-Si:H deposition recipe using HWCVD.

Table A- 3 HWCVD recipe for a-Si:H deposition.

Temperature of filament (°C)	1850
Temperature of substrate (°C)	230
Diameter size of filament (mm)	0.178
SiH_4 (sccm)	40
H_2 (sccm)	30
Pressure (mTorr)	7.5
Deposition rate (nm/sec)	0.58

A.2 Lithography

A.2.1 Optical lithography

Table A-4 shows the standard S1813 recipe used to generate pattern from optical mask.

Table A- 4 Positive photoresist, S1813, standard recipe.

Spin speed (rpm)	6000
Film thickness	1.2 μm
Pre-exposure bake temperature (°C)	115
Pre-exposure bake time (sec)	90
Exposure time (sec)	3.5
MF319 development time (sec)	35
Post-exposure bake temperature (°C)	130
Post-exposure bake time (sec)	60

A.2.2 E-beam lithography

Table A-5 shows the standard ZEP520 recipe for 450 nm resist thickness used to generate pattern from e-beam mask.

Table A- 5 Positive e-beam resist, ZEP520, for 450 nm resist thickness standard recipe.

Spin speed (rpm)	3370
Film thickness	500 nm
Pre-exposure bake temperature (°C)	180
Pre-exposure bake time (sec)	180
Exposure dose (μC/cm^2)	180
ZED-N50 development time (sec)	135

Table A-6 shows the standard ZEP520 recipe for 900 nm resist thickness used to generate pattern from e-beam mask.

Table A- 6 Positive e-beam resist, ZEP520, for 900 nm resist thickness standard recipe.

	Spin speed (rpm)	1000
	Film thickness	900 nm
Step 1	Pre-exposure bake temperature (°C)	70
	Pre-exposure bake time (sec)	60
Step 2	Pre-exposure bake temperature (°C)	180
	Pre-exposure bake time (sec)	180
	Exposure dose (μC/cm^2)	180
	ZED-N50 development time (sec)	207

A.3 Etching

A.3.1 Wet etching

Table A-7 shows the wet etch recipe using BHF based for different materials at room temperature.

Table A- 7 BHF based etch for different materials at room temperature (20°C).

Material	PECVD SiO_2	PECVD SiO_2	Thermal SiO_2	Si_3N_4
Volume ratio	7:1	20:1	7:1	7:1
Etching rate (nm/sec)	5	1.3	1.48	0.017

A.3.2 Dry etching

Table A-8 shows the standard dry etch recipe for SiO_2 with vertical profile.

Table A- 8 RIE recipe for SiO_2 with vertical profile.

CHF_3	50
Ar	25
RF power (W)	230
Pressure (mTorr)	40
Temperature (^oC)	20
Etching rate (nm/sec)	0.43

Table A-9 shows the dry etch recipe for slow etching SiO_2 with vertical profile.

Table A- 9 RIE recipe for slow etching SiO2 with vertical profile.

CHF_3	12
Ar	12
RF power (W)	200
Pressure (mTorr)	30
Temperature (^oC)	20
Etching rate (nm/sec)	0.42

Table A-10 shows the dry etch recipe for SiO_2 with vertical profile.

Table A- 10 ICP recipe for a-Si:H with vertical profile.

SF_6	25
C_4F_8	60
RF power (W)	50
ICP power (W)	750
Pressure (mTorr)	15
Temperature (^oC)	15
Etching rate (nm/sec)	3.81

Table A-11 shows the dry etch recipe used for stripping resists.

Table A- 11 Tepla Asher recipe for stripping photoresist/e-beam resists.

O_2 (sccm)	800
Power (W)	0.8
Pressure (mTorr)	71255
Photoresist etch rate (nm/sec)	≥ 25

Appendix A

Appendix B Fabrication Tools and Characterization Techniques

This appendix presents an overview of the fabrication tools and characterization techniques that are used in fabricating the interlayer waveguide devices throughout this project. The main elements of the fabrication process flow involved in this work are material deposition, pattern generation and structure etching. For materials deposition, the HWCVD and PECVD tools are mainly used. For pattern generation, both optical lithography and electron beam (e-beam) lithography techniques are used. For dry etching processes, both reactive ion etching (RIE) and inductively coupled plasma (ICP) etch tools are used. For wet etching, buffered hydrofluoric (BHF) containing ammonium fluoride (NH_4F) is used.

The first section of the appendix begins with a brief introduction to the deposition tools, with extra attention to the HWCVD method. Then, this will be followed by a brief explanation of the pattern generation method, both in optical lithography as well as electron beam (e-beam) lithography. Then, the mechanism of the dry etching tools will be briefly described, which will be followed by the description of the wet-etching method in a BHF solution to produce the slope platform. The details of the fabrication process flow, including the recipe used to fabricate the interlayer waveguide devices will not be included here but will be described in the chapters for each device. Also presented in this appendix, are brief overview on the characterisation tools and measurement set-up used in carrying out the work in this project.

B.1 Fabrication Tools

This section presents the tools primarily used for the fabrication work in this project. All the tools and equipment that are used are in-house and are available in the Southampton Nanofabrication Centre (SNC).

B.1.1 Chemical Vapour Deposition (CVD)

Chemical vapour deposition (CVD) is a process of producing thin film layers and depositing them on a substrate surface. The deposited thin film layers can be used for a variety of applications such as for optical isolation, optical waveguiding layer, top surface cladding layer and hard mask as sacrificial layer. Chemical vapour deposition (CVD) processes follow the seven main steps of film deposition. First, the dissociation of precursor gas into reacting gaseous species. Second, the diffusion of the gaseous reactant species occurring as radical ions towards the substrate surface. Third, the adsorption of the radical ions onto the heated substrate surface. Fourth, surface reactions due to the adsorbed radical ions on the active surface resulting in film growth. Fifth, the adsorbed radical ions desorb from the surface and return into the gas phase. Sixth, the diffusion of the desorbed

gas away from the surface. And finally, the removal of any by-product gases out of the chamber [6, 131]. Figure B.1 shows the illustration of the CVD process.

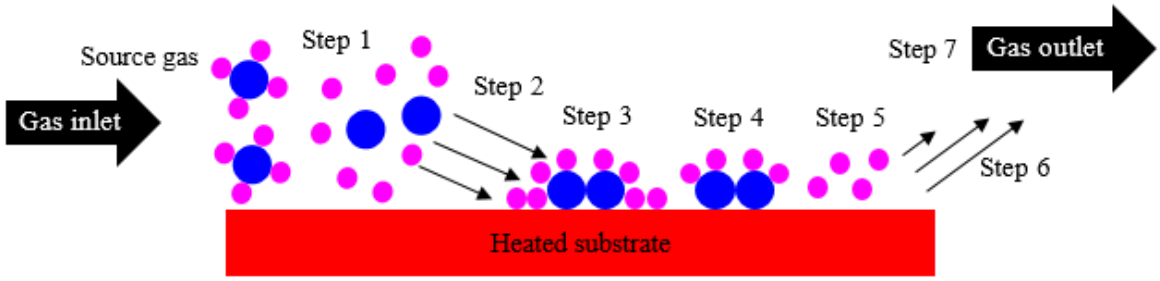


Figure B. 1 Illustration of chemical vapour deposition (CVD) process.

In principle, the dissociation of precursor gases can be induced by either temperature or plasma. Examples of a temperature-induced approach are hot wire CVD (HWCVD) and low pressure CVD (LPCVD), and an example of plasma-induced dissociation is plasma enhanced CVD (PECVD) [6]. Both approaches have advantages and disadvantages in terms of film quality and process requirements. In this project, a thermal budget below 450^{o}C has to be adhered to, for back-end of line (BEOL) process compatibility. This is because metal layers and dopants that have previously been deposited on an electronics chip may be affected by high temperature treatments, which can results in the deterioration of active devices. For example, aluminium (Al) starts to diffuse when subjected to temperatures as high as 450^{o}C for a duration over one hour, and, electro-migration in copper (Cu) becomes pronounced when the temperature is increased to 600^{o}C. Further, increasing the process temperature to up to 1000^{o}C will diffuse the dopant species which are readily present in active devices. Subsequently, this would result in the reduction of circuit performance [132-134]. Because of temperature limitations, HWCVD and PECVD both operating at temperatures below 450^{o}C are used in this project to deposit the waveguide materials. On this note, the low pressure CVD (LPCVD) tool is not an option in this work due to the high temperature operation of the system. The following section will give an overview of the operation for both HWCVD and PECVD systems.

B.1.1.1 Hot Wire Chemical Vapour Deposition (HWCVD) Tool

The hot wire chemical vapour deposition (HWCVD) is the main deposition tool used to deposit waveguide films in this project. As mentioned earlier, the gaseous dissociation process takes place at the surface of the heated filaments. Figure B.2 shows the schematic diagram of the HWCVD tool demonstrating the working fundamentals of the system [135, 136].

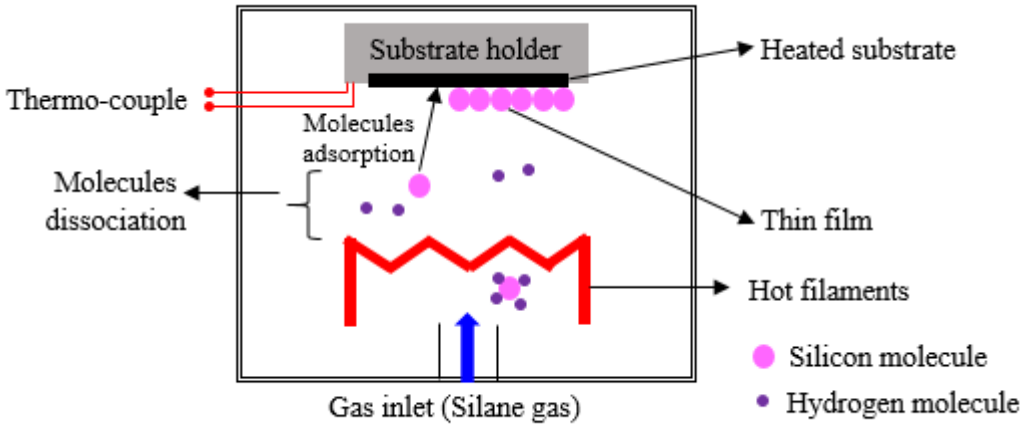


Figure B. 2 Schematic diagram of hot-wire chemical vapour deposition (HWCVD) chamber (Reproduced from[135, 136]).

In general, a HWCVD system comprises of a load-lock where samples can be mounted onto a sample holder and is used to load the sample in and out of the main process chamber. The process chamber, which is normally made of stainless steel, houses the filament wires which are electrically heated to a very high temperature [74]. Figure B.3 shows the Echerkon Nitor 301 HWCVD system available in the Southampton Nanofabrication Cleanroom, demonstrating the three fundamental parts: (a) the load-lock, (b) the chamber, and (c) the heated filament wires.

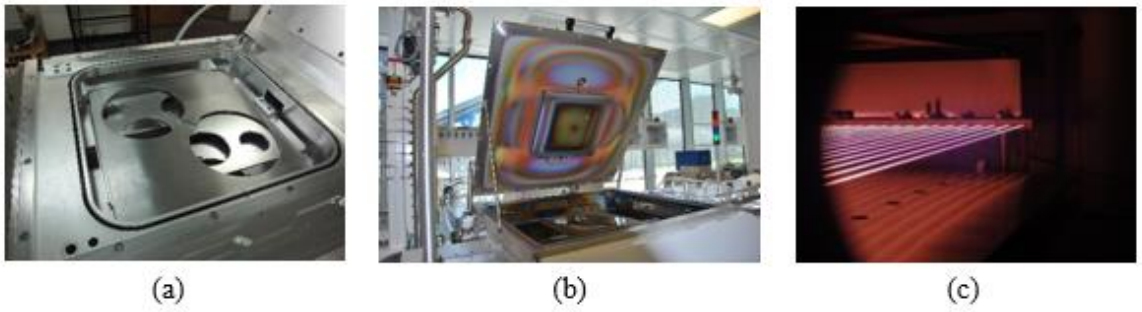


Figure B. 3 HWCVD system available in the Southampton Nanofabrication Cleanroom.

The typical HWCVD process begins with pumping down the process chamber to an operating pressure of ~1 x 10^{-6} Torr [136]. When the base pressure is reached, two gases are introduced consecutively into the process chamber. Firstly, hydrogen gas (H_2) is introduced into the chamber to precondition the filaments of the HWCVD tool. This preconditioning step is crucial as it prevents oxidation of the filament wires, especially when tantalum wire is used. By preconditioning the chamber, the efficiency and the lifetime of the tantalum wires can be preserved to produce better quality deposited films with high throughput. The preconditioning process normally takes about thirty minutes with H_2 gas flow rates depending on parameters such as the volume size of the chamber, the length, the diameter and the number of the filaments used. The H_2 gas usually requires between 10 sccm and 500 sccm to sufficiently blanket the filament wires.

Following the preconditioning process, the temperature of the filament wires is raised by flowing an electric current from a power source. Depending on the type of material to be deposited, the temperature of the filaments (T_f) ranges from 1300ºC to 2400ºC [70, 72, 74, 135-140]. As a result, the substrate, which typically placed few centimetres above the filaments, gets heated up by the radiative heat from the filament wires. In some HWCVD system, other researchers placed an additional heater attached to the substrate holder to heat up the substrate further [70, 139-141]. Here, the substrate temperature (T_s) accounted by the radiating filament wires as well as the additional heater is measured through a thermocouple placed on the surface holder just beside the substrate. Depending on the quality and film material, common substrate temperatures used range between 150ºC and 500ºC [70, 72, 135-137, 140, 142]. When the filament wires and substrate reach their desired temperature, precursor gases are injected in to the chamber through small nozzles beneath the heated filaments. Any gas molecules interacting with the high temperature filaments undergo a pyrolysis reaction. Using this project as an example, silane (SiH_4) is used and is pyrolised forming Si and H radicals. Depending on the filament temperature and the chamber pressure, the precursor gas can either be fully dissociated or partially dissociated forming Si radicals or Silyl (SiH_3) radicals. The chemical reactions are shown in the equations below [72, 139, 143],

$$SiH_4(g) \rightarrow Si\ (g) + 4H(g) \qquad \text{B.1}$$

$$SiH_4\ (g) \rightarrow SiH_3\ (g) + H(g) \qquad \text{B.2}$$

The reaction in equation B.1 is a result of having high filament temperature typically above 1600ºC [72, 143] and low applied pressure. The combination of these deposition parameters results in the complete dissociation of silane (SiH_4) into Si radicals and H radicals. Subsequently, the high energy Si radicals can be adsorbed onto the heated substrate and randomly arranged themselves forming an amorphous structure. On the other hand, at lower filament temperatures combined with a high reaction pressure, silane (SiH_4) cannot be decomposed fully. Instead, secondary gas-phase by-product radicals example Silyl (SiH_3) and hydrogen (H) are formed, as shown in equation B.2 [72, 139, 140, 143]. Nevertheless, the SiH_3 species also get adsorbed to the heated substrate contributing to the film growth of a microcrystalline structure [140]. It is also worth noting that the quality of deposited amorphous silicon films depend on the distance between the filaments and the substrate. Placing the substrate very close to the filament wires results in the film suffering a high rate of Si radicals depositing on the substrate surface. This leads to large void concentrations with a highly pronounce microcrystalline structure [70].

B.1.1.2 Plasma Enhanced Chemical Vapour Deposition (PECVD) Tool

Unlike HWCVD, the plasma enhanced chemical vapour deposition (PECVD) system utilizes high frequency electromagnetic energy to induce a plasma and thus dissociate source gases into reactive species. Using a plasma abstracts the dissociation of precursor gases from the substrate and allows the deposition process to take place at low temperatures. Temperatures in the range of 150ºC and

400°C are used when depositing thin films such as silicon dioxide (SiO_2), amorphous silicon (a-Si) and silicon nitride (Si_3N_4). Figure B.4 shows the schematic diagram of the PECVD system[6]. Similar to the HWCVD system, the PECVD process begins with the introduction of precursor gas through a metal showerhead. The showerhead plate distributes the reactant gas uniformly over the substrate surface. The gas is ionized into a plasma using a high frequency voltage applied to the showerhead. The voltage has a typical RF value equal to 13.56 MHz. The high energy electrons in the plasma bombard the precursor gases causing dissociation. As a result, gaseous radicals are generated, that get adsorbed and deposited onto the surface of the substrate forming a thin film layer [6, 137].

The focus of this thesis is on the HWCVD system as it is the tool used to deposit the waveguide material, however, PECVD also plays an important role. In this work PECVD is primarily used for the deposition of silicon dioxide (SiO_2) which is used as the waveguide's bottom and top cladding layers. It is also used for the deposition of silicon nitride (Si_3N_4) film which is used as a hard mask for hydrogenated amorphous silicon (a-Si:H) waveguide. The details of these processes recipe will be presented in their respective chapters of the device under the fabrication section.

Typical gases used for the growth of SiO_2 are silane (SiH_4) and nitrous oxide (N_2O). And, gases commonly used for the growth of silicon nitride (Si_3N_4) are silane (SiH_4) and ammonia (NH_3). The chemical reactions for both films deposition are shown in equation B.3 and B.4,

$$SiH_4(g) + 2N_2O\ (g) \rightarrow SiO_2(s) + 2H_2(g) + 2N_2(g) \qquad \text{B.3}$$

$$SiH_4\ (g) + 4NH_3(g) \rightarrow Si(NH_2)_4(s) + 4H_2(g) \qquad \text{B.4}$$

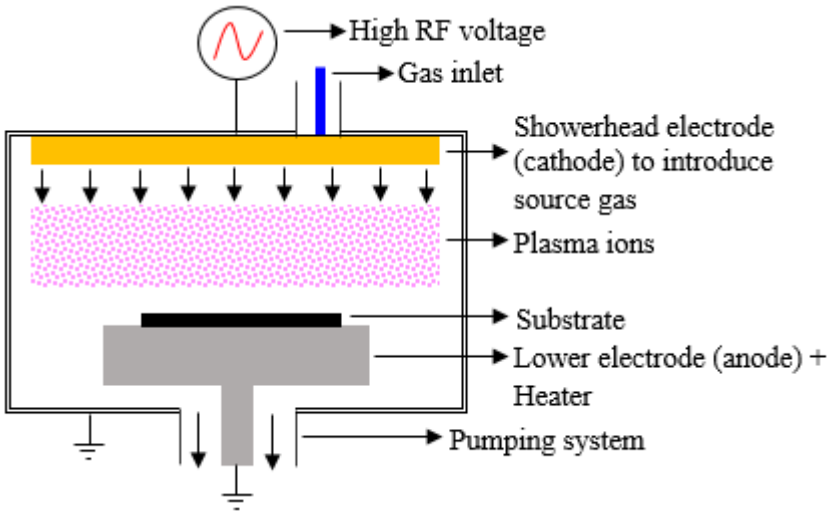


Figure B. 4 Schematic diagram of plasma enhanced chemical vapour deposition (PECVD) system (Reproduced from [6]).

In general, PECVD benefits from a low deposition temperature, which permits deposition over metal layers when the thermal budget below 450°C. The deposition rate in PECVD can be increased depending on the deposition parameters. This can be achieved by increasing the RF power, and by

reducing the spacing between the showerhead and the substrate. However, varying these two deposition parameters to increase the deposition rate, will compromise the quality of the deposited film [71]. Increasing the RF power will dissociate silane (SiH_4) effectively, thus, providing large amount of reactant species for surface reaction. However, a further increasing the RF power will result in a substantial increase in ion energies, leading to significant ion bombardment and as a result will damage the growing film [71]. Secondly, placing the substrate close to the showerhead helps to increase the deposition rate because the reactant radicals can reach the surface substrate efficiently. However, placing the showerhead electrode very close to the substrate causes the high energy ions to repeatedly bombard the film layers, which subsequently results in film stress and facilitates the formation of voids. In addition, hydrogen present in the precursor gases causes unwanted porosity in deposited films. This is exacerbated at lower deposition temperatures, and the film is more likely to develop pinholes when etching [6].

B.1.2 Optical Lithography

Optical lithography is a parallel lithography by which patterns are generated area by area, by exposing UV light through an optical mask. Thus, pattern generation in optical lithography is fast and relatively cheaper compared to other lithography techniques, for example electron beam lithography. Consequently, this allows high-throughput patterning at low cost. The work in this thesis uses optical lithography when large feature sizes are needed and where high resolution and precise alignment are not a major concern. A mask aligner, EVG620TB, is used for all the photolithography processes in this project. The mask aligner available at the SNC uses a mercury UV lamp, operating at a wavelength in the range between 350 nm and 450 nm. Hard contact, where the mask physically touches the sample us used and permits a pattern resolution as small as 1 μm. The contact between mask and substrate prevents divergence of the UV light under the mask and maintains optimum mask transfer.

In principle, optical lithography uses UV light to transfer a pattern, through an optical mask to a photon sensitive resist, or commonly called photoresist. The exposure of the UV light onto the photoresist causes a chemical reaction that allows a particular area of the photoresist to be weakened or hardened. In general, there are two types of photoresist, positive resist and negative resist. Upon radiation, for positive resist, the exposed part become soluble in the developer, while for a negative resist, the molecules of the exposed part cross-linked and becomes more stable in the developer [6]. Figure B.5 illustrates the optical lithography process.

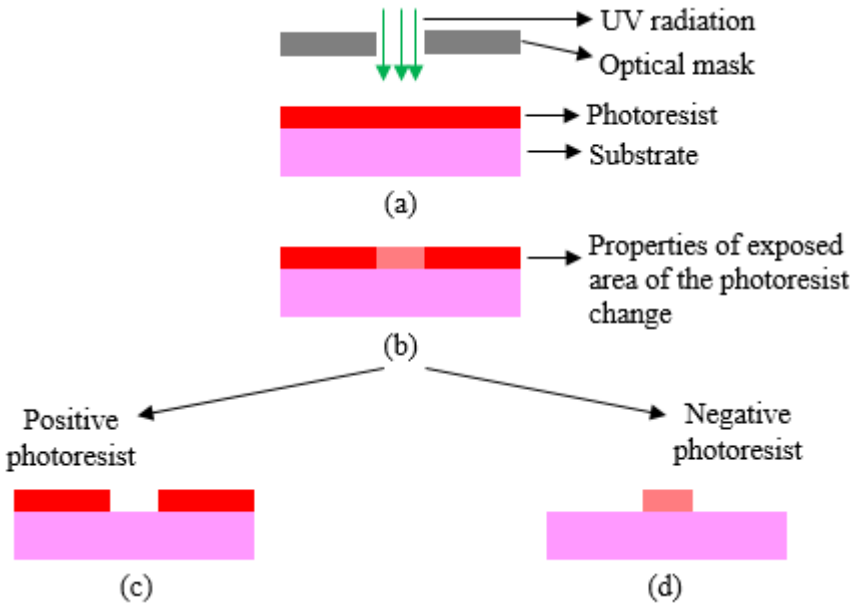


Figure B. 5 Photolithography process flow, (a) Sample which has been spun with photoresist is exposed under UV light through an optical mask, (b) After UV radiation, the properties of the exposed area of the photoresist change accordingly, (c) For positive photoresist, the exposed area becomes weakened and dissolved during development, and (d) For negative photoresist, the exposed area becomes hardened and remained after development. (Reproduced from [6]).

In optical lithography, exposure time determines the quality of the resist profile upon radiation. Underexposure and overexposure can severely distort the desired pattern. The exposure time can be determined by calculation using the formula shown below,

$$Exposure\ time\ (s) = \frac{Total\ exposure\ dose\ (mJ)}{Current\ intensity\ of\ machine\ (mW/cm^2)} \quad \text{B.5}$$

In this project, the positive photoresist, S1813, is exposed through the optical mask. The optical mask is made of soda lime (SL) glass substrate with one side covered with a chrome pattern. From the datasheet of S1813, the total exposure dose is equal to 150 mJ/cm^2. The current intensity of the machine can be measured in terms of mW/cm^2, therefore, it is possible to calculate the exposure time. Because the current intensity of the mask aligner available at the SNC changes over the course of completing this project, the exposure time has to be recalculated periodically. For example, at the start of the project, the time required to expose the S1813 was 3.5 seconds, for a current intensity equal to 42.9 mW/cm^2. The current intensity decreased over a period of three years, coming down to 13.7 mW/cm^2, requiring an exposure time equal to 11 seconds. In addition, resist adhesion also plays an important role in the fabrication of the interlayer slope waveguide. By using an adhesion promoter and a post thermal treatment to increase adhesion between the SiO_2 surface and the resist, the etching angle of the interlayer slope waveguide can be controlled.

B.1.3 Electron Beam Lithography

Electron beam lithography, which is commonly referred to as e-beam lithography, is a serial lithography by which patterns are created point by point by focusing a beam of electrons onto an

electron sensitive resist. Consequently, the pattern resolution can be improved. Resolution as high as 20 nm can be easily attained, permitting the fabrication of sub-micron device structures. Another advantage is the flexibility of changing the pattern design – as a physical mask is not required such as in optical lithography. The downside of using electron beam (e-beam) lithography is the slow speed of writing and the expense of the equipment. Nevertheless, the need to generate sub-micron sized waveguide containing sub-micron sized pitch grating couplers requires the need to use electron beam (e-beam) lithography in this project.

In this project, a high resolution positive electron beam (e-beam) resist, ZEP520A, is used to generate the waveguide patterns. On exposure, the molecular bonds of ZEP520A breaks which results to smaller molecules. These smaller molecules are less stable and become soluble when immersed in developer. In running the lithography, the following beam conditions as shown in Table B-1 shows the e-beam conditions used in this project.

Table B- 1 Beam conditions for running the e-beam lithography.

Dose (μC/cm^2)	Beam Aperture (μm)	Beam Diameter (nm)	Beam Current (nA)	Acceleration Voltage (kV)
180	200	20-24	10	100

B.1.4 Reactive Ion Etching (RIE) Tool

The mechanism of reactive ion etching (RIE) is very similar to the PECVD system described earlier. Figure B.6 shows the schematic of an RIE tool [6]. Firstly, etchant gases such as sulfur hexafluoride (SF_6) are introduced into the reaction chamber. Strong radio frequency (RF) power, with typical RF value equal to 13.56 MHz, is applied across the chamber creating a plasma. The high energy electrons in the plasma move around rapidly, some of them hit the chamber wall and get absorbed as the chamber is grounded, and some of them hit the bottom electrode resulting in an accumulation of negative charge. Consequently, this creates a bias causing the positively charged ions (SF_5^+) in the plasma to accelerate towards the bottom electrode. As a result, the positively ionised molecules collide with the material of the sample, breaking the bonds and eventually etches the etchable material. In general, etchant gas hits the surface of the sample at 90^o angle, thus, producing highly anisotropic etching profile. Additionally, process parameters which include applied RF power, operating temperature, chamber pressure and etchant gases composition and flow rate play significant role in determining the profile of the etch structure [6, 37]. In this work, the RIE tool is primarily used to etch alignment markers, with an etch depth of approximately 1 μm.

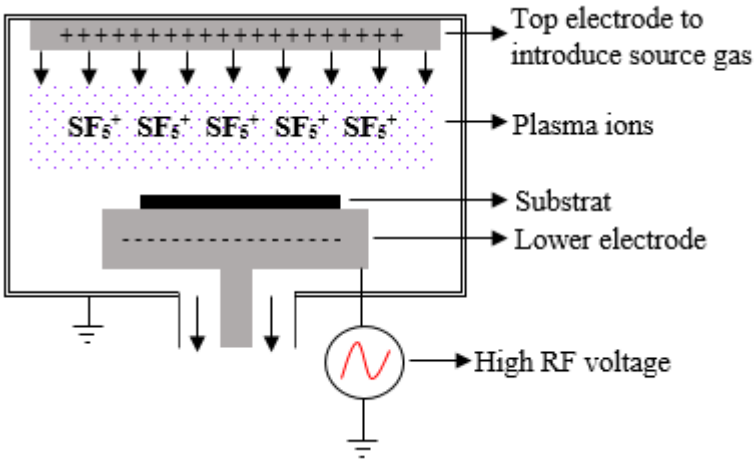


Figure B. 6 Schematic diagram illustrating a reactive ion etching (RIE) tool. (Reproduced from [6]).

B.1.5 Inductively Coupled Plasma Etching (ICP) Tool

An inductively coupled plasma (ICP) etching tool is similar to an RIE tool, with the addition of a second RF generator connected to the chamber. The schematic diagram of an ICP tool is shown in Figure B.7 [144]. In principle, the first RF generator which is connected to the bottom electrode is responsible in creating a plasma containing high density of etchant ions. The second RF generator controls the energy of the ions accelerating towards the surface of the substrate. This permits lower surface damage of the substrate due to the weakened field of the low energy ions bombarding the surface. In addition, high selectivity between the resist and the etched material can be achieved, enabling high aspect ratio trenches. In this project, the ICP tool is used to etch sub-micron sized waveguide structure with smooth sidewalls [6].

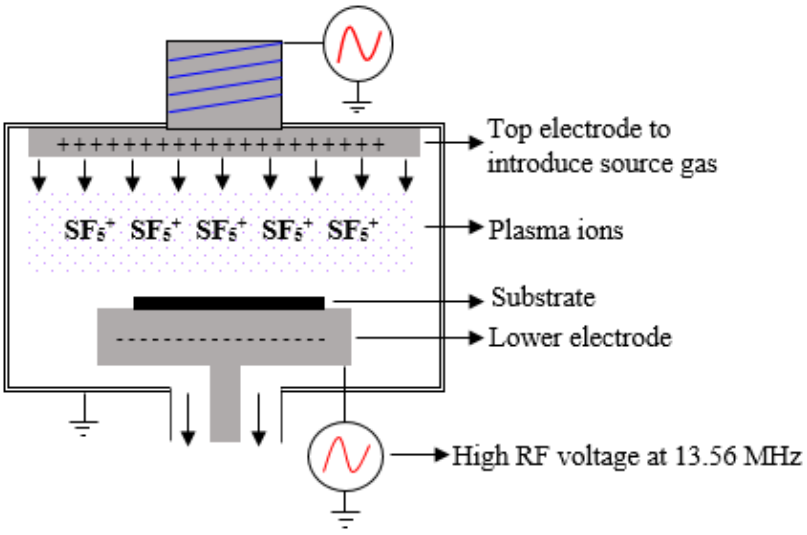


Figure B. 7 Schematic diagram illustrating an inductively coupled plasma etching (ICP) tool. (Reproduced from [144]).

B.1.6 Wet Etching in Buffered Hydrofluoric (BHF) Acid

In this project, PECVD silicon dioxide (SiO_2), which serves as dielectric isolation material, is etched in buffered hydrofluoric (BHF) acid, and is the most important step in the fabrication of the interlayer slope waveguide. The dissolution of silicon dioxide (SiO_2) in the BHF solution leads to the formation of the slope platform. In this section, the wet-etching method using BHF to produce the slope platform will be presented.

The fundamental reaction mechanism of wet-etching between SiO_2 and HF solution can be described by the chemical reaction as shown below [106, 113, 114],

$$SiO_2(s) + 6HF\,(aq) \rightarrow H_2SiF_6(aq) + 2H_2O(aq) \qquad \text{B.6}$$

In principle, SiO_2 is made of tetragonal silicate (SiO_4) compounds joined together forming a three-dimensional (3D) network structure connected by siloxane (≡Si–O–Si≡) covalent bonds [106]. In etching SiO_2, all of the four covalent bonds in the tetragonal silicate (SiO_4) compounds have to be broken down to break the amorphous network and release the silicon atom from the silicate structure. Wet chemical etching using aqueous HF solution containing H^+, F^-, and HF_2^- ions can break the covalent bonds efficiently. Depending on the wet etching parameters such as the HF concentration, temperature, oxide growth process and the quality of adhesion between the resist and the SiO_2, can determine the etch rate and the shape of the etch profile [106, 145]. Primarily, H^+ and HF_2^- ions are the two reactive etchant species which are responsible for breaking the covalent bonds and determine the etch rate. A high HF concentration results in severe delamination of the resist. Diluting HF solutions with either water (H_2O) or ammonium fluoride (NH_4F) decreases the acidity and allows the reaction rate to be controlled. The delamination of resist that occurs due to the attack of the reactive ion species at the SiO_2-resist interface can also be reduced with diluted HF solutions. Most wet etching processes result in an isotropic etch profile, include SiO_2 with aqueous HF solutions where a semi-circular sidewall is formed, as shown in Figure B.8 (a). This isotropic etching profile is formed when the adhesion between the resist and the SiO_2 surface is high. In the case when the adhesion is poor, delamination of the resist occurs. As a result, the top surface of the film etches quicker resulting to a tapered-like wall structure at the edge of the etching window, as shown in Figure B.8 (b). The fabrication of the interlayer slope waveguide, in this project, requires the adhesion between the SiO_2 surface and the resist layer to be relatively weak, to obtain the slope etching profile which is similar to the diagram as shown in Figure B.5 (b). Photoresist S1813 was used for the wet-etching processes, with the design structure had previously been transferred using the photolithography method.

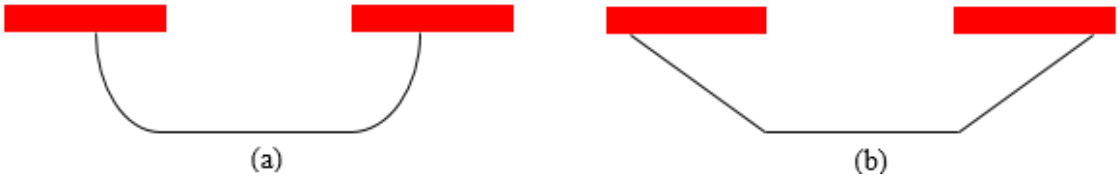


Figure B. 8 The contour of the wall of wet etching silicon dioxide (SiO2) in hydrofluoric (HF) acid solution, with (a) strong adhesion of resist onto silicon dioxide (SiO2) surface, and (b) weak adhesion between the resist-silicon dioxide (SiO2) interface which cause resist delamination and resulting to faster etching at the top surface. (Reproduced from [106]).

Initially, a slope angle of approximately 10^{o} with an etch depth of approximately 1.4 μm was achieved. Throughout the course of the project, experiments using an adhesion promoter and post-baking of the S1813, allowed control of the slope angle. These additional parameters permitted higher slope angles of approximately 15^{o}, 20^{o} and 25^{o}. The variations of the slope angle are useful in evaluating the loss characteristics of the interlayer waveguide coupler, and can accommodate different platform requirements.

B.2 Characterization Techniques

This section presents the measurement tools and set-up used to characterize and evaluate the performance of the HWCVD hydrogenated amorphous silicon (a-Si:H) interlayer slope waveguide devices. The characterization methods include thickness and refractive index measurements using an Ellipsometer, surface roughness measurements using atomic force microscopy (AFM) and optical coupling to grating couplers for transmission and loss characterization. Other than these characterization methods, microscopy tools such as optical microscope and scanning electron microscope (SEM) have also been primarily used for imaging the fabricated device throughout the course of completing this project.

B.2.1 Ellipsometry Measurement

The J. A. Woollam Ellipsometer is used in this work to determine film thickness and the refractive index value of the deposited film material. In general, the main components of an Ellipsometer comprises of a light source, polarizer, the sample to be measured, a polarization analyzer and detector. Polarized light with broad wavelength is projected onto the sample to characterize the film. In principal, as the injected polarized light interacts with the sample, a portion gets reflected and the rest is transmitted. As the polarized light interacts with the sample structure, light reflected at the interface experiences a change in amplitude and phase. This is then collected by the detector and converted into electronic signal. This information is compared with the known input polarization to determine the polarization change which is caused by the light's interaction with the sample. The changes are represented across the Ellipsometer wavelengths as Psi and Delta, which gives information on the physical thickness and other optical properties of the film material [146]. Figure B.9 illustrates the mechanism of principle of an ellipsometry [146].

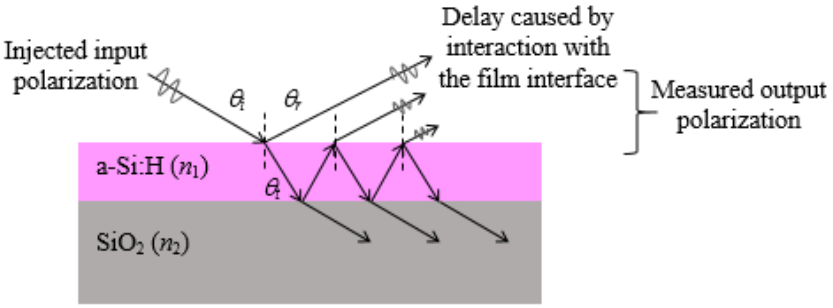


Figure B. 9 Illustration of the mechanism of operation of an ellipsometry. (Reproduced from [146]).

CompleteEASE software is used to analyse the raw data, and compare it to a known material model. The curve of the measured data has to match the model curve to characterise the film accurately. The fit of this curve can be adjusted automatically or manually by adjusting model parameters. The mean squared error (MSE) between the data and the model, is used to quantify the difference between the two curves where a lower MSE suggests a more accurate fit [146]. Figure B.10 shows an example of an Ellipsometry measurement carried out while fabricating the interlayer slope waveguides. As shown in the figure, three layers of material were deposited, starting from the PECVD SiO_2 isolation layer, followed by HWCVD a-Si:H for the waveguide layer and finally ZEP520 resist for electron beam lithography for the waveguide pattern generation.

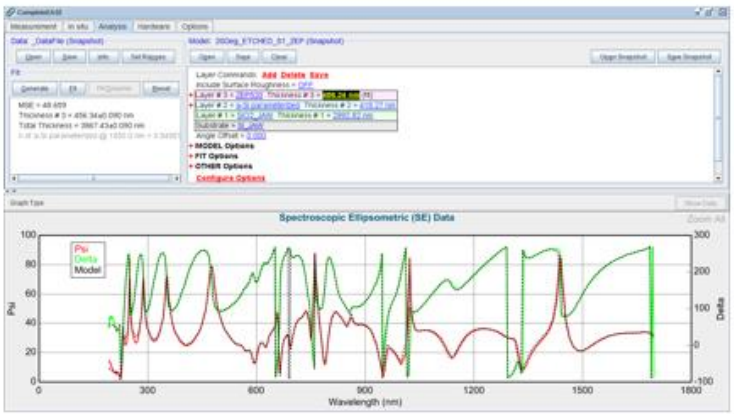


Figure B. 10 An example of ellipsometry measurement in fabricating the interlayer slope waveguide.

B.2.2 Atomic Force Microscopy (AFM) Measurement

Atomic force microscopy (AFM) is a technique used to characterize the surface morphology of a film. It provides a 3D surface profile of the film by measuring forces between a pointed probe tip and the film surface at a nanometre scale. Typical separations between the probe and a sample separation are in the range of 0.2 and 10 nm. The main components of an AFM are the probe tip, the cantilever to support the probe tip, the scanner to move the sample in the x, y and z direction, the laser, a data processor and a photodetector. Figure B.11 illustrates the schematic diagram of an AFM tool [147]. In the most fundamental configuration, a beam of light is directed at the cantilever from

the laser. As the tip interacts with the surface of the sample, it causes the cantilever to either bends towards or move away from the sample surface. The movement of the cantilever is supported by a piezoelectric element to allow the cantilever to oscillate. The height change is passed to the photodetector where the data signal gets recorded and processed in to a surface topology image. Typically, there are three types of imaging modes in AFM; contact mode, intermittent or tapping mode and non-contact mode. Depending on the surface characteristics, either one of these modes can be used. In this work, the tapping mode is used as it gives high resolution while preventing unnecessary damage to the surface of the sample.

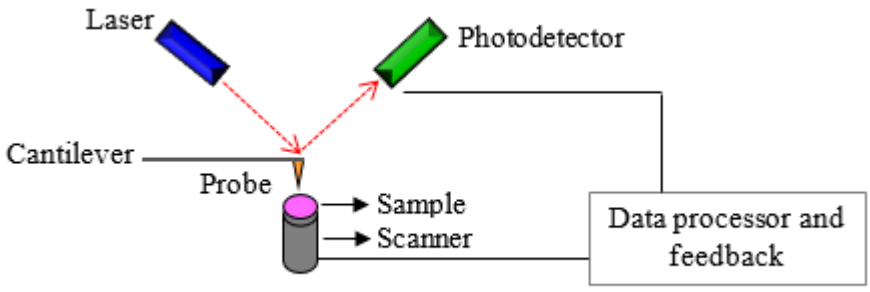


Figure B. 11 Schematic diagram of an AFM tool (Reproduced from [147]).

Gwyddion ver. 2.36 software is used to analyze the data measurements. Primarily, the quantities that are extracted from this software are the root mean square (RMS) surface roughness, symbolized as R_q, and the grains size of a deposited material. Upon scanning the sample surface, the RMS surface roughness (R_q) can be obtained directly from the 'Statistical Quantities' option. The RMS (S_q) function gives the true value of the film's surface roughness compared to average roughness (R_a) as it takes into account the square of the amplitudes of the peaks and valleys of the surface. While the R_a is just a mean absolute profile, with no distinct difference between peaks and valleys of the surface.

B.2.3 Loss Measurement via Grating Couplers

In measuring the transmission of the interlayer slope waveguides, light is coupled in and out of the structures via fully etched grating couplers. Figure B.12 illustrates the grating coupler set-up used to measure the optical transmission. The measurement setup uses a tunable Agilent 81940A laser source and Agilent 81634B power sensor, which are contained in an Agilent housing. The Agilent housing has a control panel for adjusting the input power and the wavelength. Both the laser source and the power sensor have an operating wavelength range between 1520 nm to 1630 nm at TE mode polarization.

In the set-up, two types of fibre were used to couple light in and out of the grating couplers, first is the polarization maintaining fibre, P5-1550PM-FC-2, and, second is the single mode SMF-28-J9 fibre. The polarization maintaining fibre and the standard single mode fibre, have mode field

diameter (MFD) of 10.1 µm and 10.4 µm, respectively, at 1550 nm wavelength. In the set-up as shown in Figure 5.12, the polarization maintaining fibre, coloured blue, runs from the laser source to a three-paddle polarization controller. A standard single mode fibre, coloured in yellow, is connected at one end to the output of the polarization controller. The other end is a cleaved facet that is mounted on a fibre holder. Another cleaved single mode fibre, coloured yellow, is mounted to an output fibre holder. This fibre is connected to the power detector via another polarization maintaining cable, coloured blue. The single mode optical fibres, coloured yellow are placed near vertically above the input and the output of the grating couplers. A slight tilt is necessary to avoid a large second order mode reflecting back into the fibre. This reflection is undesirable as it can cause the coupling efficiency of the grating couplers to get reduced, and thus deteriorating the optical performance of the waveguide [148, 149]. While aligning the optical fibres to the grating couplers, sub-micron accuracy is required to achieve maximum efficiency. Here, Nanomax-TS, translation stages are used to securely hold the input and the output fibre holders and to move the fibres in the x, y and z directions. The movement is highly accurate with travelling distance in the range of 4 mm for coarse tuning and 300 µm for fine tuning. The stage also has piezoelectric controllers, allowing nanometre precision with a resolution of 20 nm to align the fibres on the grating couplers.

In this work, an input power of 10 mW at a wavelength of 1550 nm is used. Upon maximizing the coupling transmission of the waveguide through optimized alignment at a wavelength of 1550 nm, the output power is scanned across a range of wavelengths using a piece of commercial software, called Photonic Application Suite (PAS). The software compares the output power collected from the detector with the input power from the laser. Consequently, a graph is produced displaying the loss of the waveguides in decibels (dB) on the y-axis against the scanned wavelengths (nm) on the x-axis. The plot of the graph is used to observe the transmission spectrum of the grating couplers, which can then be exported as an Excel file for waveguide loss analysis.

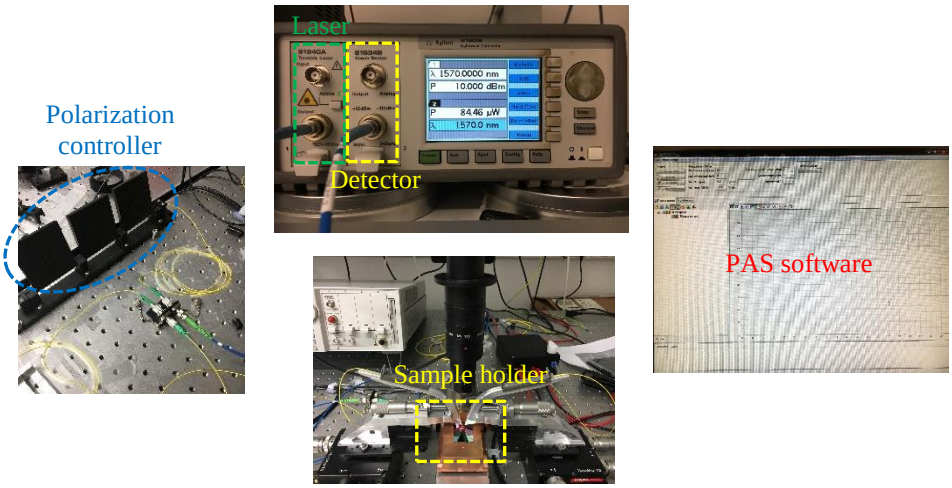


Figure B. 12 Grating couplers measurement set-up used to characterize the interlayer slope waveguide.

Appendix C Additional Results

Figure C.1 shows the transmission spectrum of the 400 nm (w) by 400 nm (h) interlayer slope waveguide, for Sample A with slope angle equal to 11.8°.

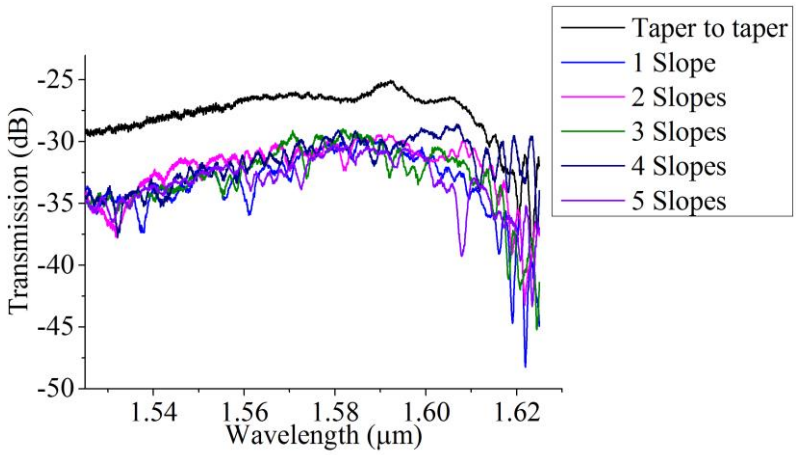


Figure C. 1 Measured transmission spectrum for Sample A with slope angle equal to 11.8°.

Figure C.2 shows the transmission spectrum of the 400 nm (w) by 400 nm (h) interlayer slope waveguide, for Sample B with slope angle equal to 16.7°.

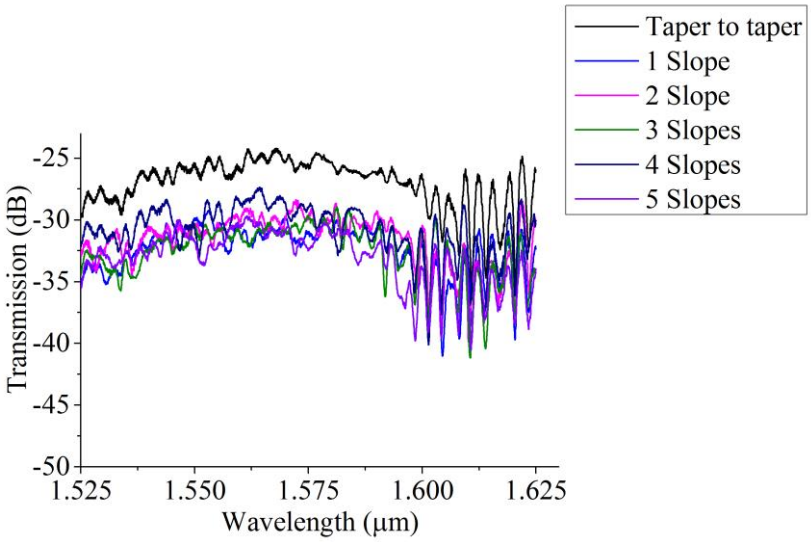


Figure C. 2 Measured transmission spectrum for Sample B with slope angle equal to 16.7°.

Appendix C

Figure C.3 shows the transmission spectrum of the 400 nm (w) by 400 nm (h) interlayer slope waveguide, for Sample C with slope angle equal to 20.8º.

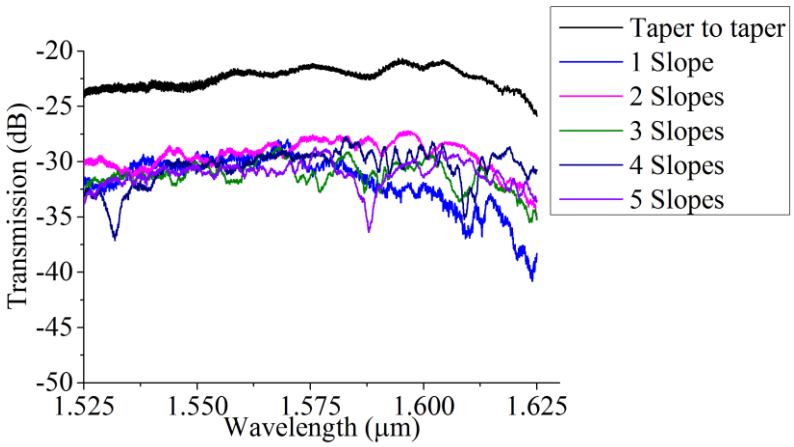


Figure C. 3 Measured transmission spectrum for Sample B with slope angle equal to 20.8º.

Figure C.4 shows the transmission spectrum of the 400 nm (w) by 400 nm (h) interlayer slope waveguide, for Sample C with slope angle equal to 25.3º.

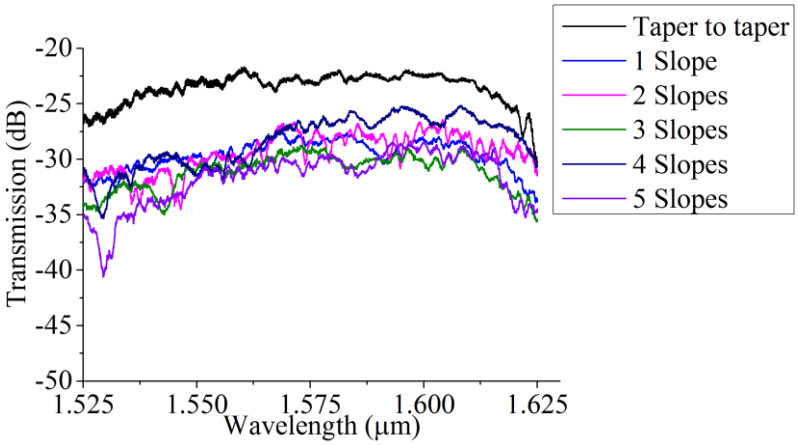


Figure C. 4 Measured transmission spectrum for Sample B with slope angle equal to 25.3º.

Table C- 1 Loss measurements of the crosstalk waveguides, for varying isolation thicknesses and waveguide dimensions.

Isolation Thickness = 50 nm												
Waveguide Width = 400 nm							**Waveguide Width = 1000 nm**					
	Measurement 1		Measurement 2		Measurement 3			Measurement 1		Measurement 2		Measurement 3	
	W	dB	W	dB	W	dB		W	dB	W	dB	W	dB
B-B	4.60E-09	-63.37	3.07E-09	-65.13	6.25E-09	-62.04	B-B	5.66E-08	-52.47	8.81E-08	-50.55	3.85E-08	-54.15
B-T	4.42E-10	-73.55	3.01E-10	-75.22	0.98E-9	-70.06	B-T	5.18E-10	-72.86	1.64E-09	-67.85	2.54E-10	-75.95
XTALK	-10.18		-10.09		-8.02		XTALK	-20.39		-17.3		-21.8	
Isolation Thickness = 200 nm													
Waveguide Width = 400 nm							**Waveguide Width = 1000 nm**						
	Measurement 1		Measurement 2		Measurement 3			Measurement 1		Measurement 2		Measurement 3	
	W	dB	W	dB	W	dB		W	dB	W	dB	W	dB
B-B	59.9E-09	-52.22	96.4E-09	-50.16	1.05E-07	-49.78	B-B	1.58E-06	-38.008	1.07E-06	-39.723	2.66E-06	-35.748
B-T	0.256E-6	-75.92	0.829E-09	-70.81	1.00E-9	-70.001	B-T	8.68E-10	-70.614	5.53E-10	-72.569	5.19E-10	-72.846
XTALK	-23.7		-20.65		-20.22		XTALK	-32.606		-32.846		-37.098	
Isolation Thickness = 500 nm													
Waveguide Width = 400 nm							**Waveguide Width = 1000 nm**						
	Measurement 1		Measurement 2		Measurement 3			Measurement 1		Measurement 2		Measurement 3	
	W	dB	W	dB	W	dB		W	dB	W	dB	W	dB
B-B	6.43E-08	-51.918	4.99E-08	-53.0221	4.10E-08	-53.875	B-B	1.12E-07	-49.5204	1.21E-07	-49.174	1.28E-07	-48.944
B-T	1.05E-10	-79.782	7.92E-11	-81.0127	8.01E-11	-80.962	B-T	6.40E-11	-81.939	7.90E-11	-81.0232	8.05E-11	-80.9429
XTALK	-27.864		-27.9906		-27.087		XTALK	-32.4186		-31.8492		-31.9989	
Isolation Thickness = 1000 nm													
Waveguide Width = 400 nm							**Waveguide Width = 1000 nm**						
	Measurement 1		Measurement 2		Measurement 3			Measurement 1		Measurement 2		Measurement 3	
	W	dB	W	dB	W	dB		W	dB	W	dB	W	dB
B-B	4.04E-08	-53.94	4.34E-08	-53.6228	4.63E-08	-53.343	B-B	1.50E-07	-48.236	1.51E-07	-48.2155	1.51E-07	-48.20329
B-T	5.63E-11	-82.494	9.39E-11	-80.2715	3.71E-11	-84.3049	B-T	7.41E-11	-81.304	6.81E-11	-81.6682	8.50E-11	-80.70552
XTALK	-28.554		-26.6487		-30.9619		XTALK	-33.068		-33.4527		-32.50223	

Table C- 2 Loss measurements of the fly-over waveguide, for different input and output ports with varying distance, *x*, between the two measured waveguides.

400 nm (*w*) by 400 nm (*h*)							
No	Distance, *x* (μm)	Loss 1-2 (dB)	Loss 1-8 (dB)	Crosstalk (dB)	Loss 3-4 (dB)	Loss 3-8 (dB)	Crosstalk (dB)
***x*1**	71	-33.46	-80.85	-47.39	-37.27	-82.47	-45.2
***x*2**	61.9	-34.59	-82.18	-47.59	-35.41	-78.88	-43.47
***x*3**	49.2	-35.77	-81.94	-46.17	-34.82	-82.81	-47.99
No	Distance, *x* (μm)	Loss 1-2 (dB)	Loss 1-6 (dB)	Crosstalk (dB)	Loss 3-4 (dB)	Loss 3-6 (dB)	Crosstalk (dB)
***x*4**	21.9	-33.46	-79.59	-46.13	-37.27	-87.87	-50.6
***x*5**	12.6	-34.59	-81.67	-47.1	-35.41	-80.73	-45.3
***x*6**	0	-46.77	-65.24	-18.43	-55.82	-81.24	-25.42

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