

Electronic–photonic convergence for silicon photonics transmitters beyond 100 Gbps on–off keying

KE LI,^{1,*} SHENGHAO LIU,¹ DAVID J. THOMSON,^{1,2} WEIWEI ZHANG,¹ XINGZHAO YAN,¹ FANFAN MENG,¹ CALLUM G. LITTLEJOHNS,¹ HAN DU,¹ MEHDI BANAKAR,¹ MARTIN EBERT,¹ WEI CAO,¹ DEHN TRAN,¹ BIGENG CHEN,¹ ABDUL SHAKOOR,¹ PERIKLIS PETROPOULOS,¹ AND GRAHAM T. REED^{1,3}

¹Optoelectronics Research Centre, University of Southampton, Southampton, SO17 1BJ, UK

²e-mail: D.Thomson@soton.ac.uk

³e-mail: G.Reed@soton.ac.uk

*Corresponding author: kl@ecs.soton.ac.uk

Received 28 September 2020; accepted 2 October 2020 (Doc. ID 411122); published 27 October 2020

We present design concepts for optical modulators without using any equalization or bespoke fabrication techniques. The demonstrated silicon photonics transmitter can operate at 100 Gbps OOK, while the power efficiency of the driver is 2.03 pJ/bit.

Published by The Optical Society under the terms of the [Creative Commons Attribution 4.0 License](#). Further distribution of this work must maintain attribution to the author(s) and the published article's title, journal citation, and DOI.

<https://doi.org/10.1364/OPTICA.411122>

The optical modulator is the critical component in systems serving modern information and communication technologies [1], not only in traditional data communication links, but also in microwave photonics or chip-scale computing networks. It is noticeable that several recent outstanding devices, which are based on thin-film lithium niobate [2,3] and electronic plasmonics [4], have demonstrated 100 Gbps on–off keying (OOK) transmission only, by incorporating equalization techniques. Furthermore, all of these devices suffer from concerns over fabrication complexity and productivity yield and are incompatible with standard CMOS processes. In contrast, silicon modulators based upon the plasma dispersion effect do not present these fabrication challenges and are favorable for chip-scale optoelectronic systems, where large numbers of photonic devices are fabricated on a single wafer. However, bandwidth limitation is the primary concern for this type of silicon modulator, and even by adopting additional dedicated fabrication process steps, such as substrate removal, the highest data rate demonstrated is 90 Gbps OOK [5] when fed by a driver amplifier requiring watts of power consumption.

Nonetheless, previously reported modulator designs, regardless of the device material or the device structure, look to optimize the trade-off among the different performance metrics: high bandwidth, low optical insertion loss, low-drive voltage, low fabrication

cost, small device footprint and device reliability, whereas few of the previous examples have ever deeply investigated the convergence of the photonics and electronics. In contrast to previous work in the field where photonics–electronics integration is mostly limited to the physical coupling approach between photonic and electronic devices such as monolithic [6], wire bonding [7] or flip-chip bonding [8], we have introduced a new design philosophy, where a synergistically designed electrical CMOS driver can solve the limited bandwidth dilemma of the silicon photonics modulator.

Inductive peaking is a standard technique that has been utilized for bandwidth enhancement for numerous high-speed electrical circuit designs. However, “T-coil” peaking provides an alternative means of increasing the bandwidth. Previous work [9] has demonstrated that an asymmetrical transformer can provide an additional 70% bandwidth enhancement over that provided by inductive peaking techniques when utilized in broadband amplifier designs. Therefore, an intuitive assumption is that an asymmetrical transformer may also find its utilization within the optical modulator driver design, where the concerns around bandwidth limitations could be alleviated to a large extent. Under this assumption, the PN doping levels of the silicon modulator can be purposely increased so that the modulation efficiency is enhanced, which in turn leads to optimization of the electrical power efficiency and photonic device footprint.

The preconditions for such great potential to be realized are that passive electrical elements, such as asymmetrical transformers, peaking inductors, and termination resistors, must provide a high-quality, low-loss profile over a broadband frequency range (>70 GHz), and within the typical CMOS process variations. We, therefore, designed all of these passive components (L_{M1} , L_{M2} , R_1 , R_2 , L_2 , L_3) in a standard commercial CMOS process (TSMC 28 nm High-K-Metal-Gate), allowing our linear driver amplifier to be designed and fabricated. As highlighted in Fig. 1, the asymmetrical transformer is realized with the top two thick metal layers of the CMOS process, with the gapped metal

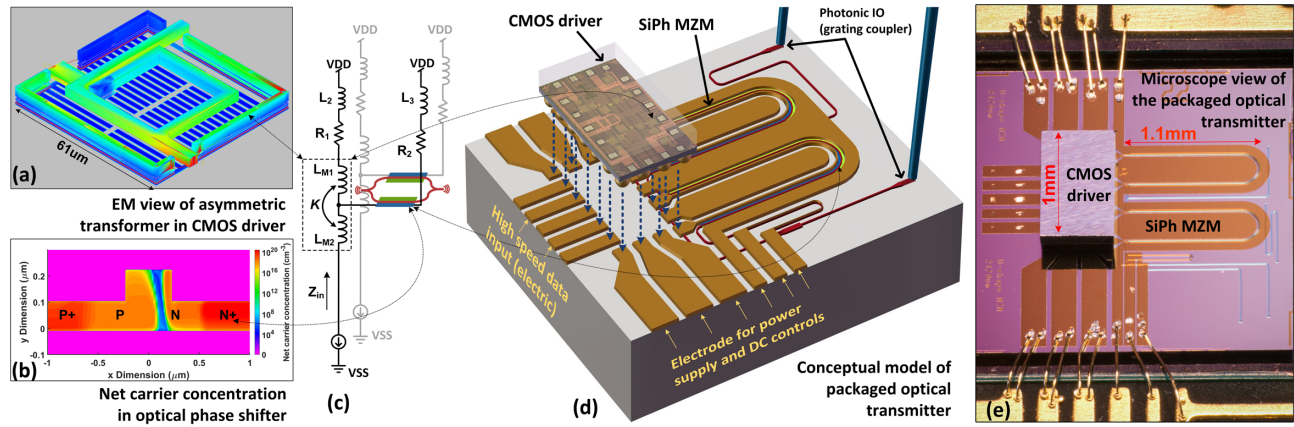


Fig. 1. Illustration of the convergence of CMOS driver and silicon photonics modulator. (a) EM view of asymmetric transformer; (b) net carrier concentration in silicon photonics carrier depletion phase shifter; (c) input impedance of asymmetric transformer with a traveling wave phase modulator as a load; (d) conceptual model of the packaged optical transmitter; (e) microscope view of the packaged optical transmitter.

tracks used for bottom shielding. The outer dimensions of the asymmetrical transformer are $61 \mu\text{m} \times 63 \mu\text{m}$, which is almost the same as a standard IO PAD. Furthermore, following the same concept of our previous work [7], a standard carrier depletion-based optical modulator is designed in a U-shapes MZM configuration, allowing access to both input and termination pads of the MZM on one side of the chip. This allows both ends of the modulator to be electrically connected to the CMOS driver by flip-bonding in this case. The U-shaped MZM was designed and modeled for operation at a wavelength of 1550 nm. The conceptual model and the microscope view of the packaged sample in Fig. 1 illustrates the integration process. The PN junction within the silicon MZM is fabricated with a higher doping concentration than is typically used, of $3 \times 10^{17} \text{cm}^{-3}$, $8.5 \times 10^{17} \text{cm}^{-3}$, $1 \times 10^{20} \text{cm}^{-3}$, $1 \times 10^{20} \text{cm}^{-3}$ for n, p, n+, and p+, respectively. The measurement results from a test structure show a modulation efficiency of 1.5 V·cm, and a phase-shifter loss of 2.7 dB/mm with a 1 V reverse bias voltage. The overall phase-shifter length in this design is chosen to be 2.47 mm, which gives a total optical loss of 6.9 dB including the losses from two MMIs, the passive waveguides, and the 2.47 mm phase shifters.

When conducting the optoelectronic testing, two independent electrical $2^7 - 1$ pseudo-random bit sequence (PRBS) test signals were provided by an SHF bit pattern generator (12104A) and fed into a MUX (SHF 603B) that can provide multiplexed signals up to 112 Gbps with a single-ended voltage swing of approximately 0.5 V. This signal was then fed into our driver amplifier. The optical output from the modulator was amplified by a low-loss EDFA and then fed into a Keysight Digital Communication Analyzer (DCA 86100D). The maximum power supply within the testing circuit was set at 2.8 V, under which the overall power consumption of the CMOS driver was measured to be 203 mW. Tuning the heating element to set the operating point on the silicon modulator consumed another 20–35 mW. When operating at the quadrature point, optical eye diagrams at 56 Gbps OOK, 80 Gbps OOK, and 100 Gbps OOK, shown in Figs. 2(a)–2(c), are detected, where no equalization techniques were used. It can be seen that the integrated silicon photonics transmitter can operate at 100 Gbps OOK, with ~ 3 dB extinction ratio and a power efficiency of 2.03 pJ/bit. To further investigate the performance limitation with a better power efficiency, the baud rate was increased, and the power supply

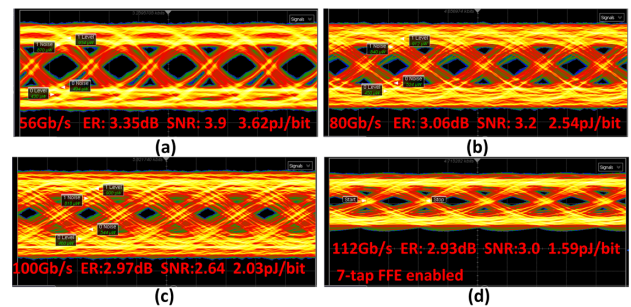


Fig. 2. Measured optical eye diagram at different baud rates. (a) 56 Gbps OOK; (b) 80 Gbps OOK; (c) 100 Gbps OOK; (d) 112 Gbps OOK with seven-tap feed-forward equalization enabled in the DCA.

of the driver was deliberately scaled down. Experimental results show that with a power efficiency of 1.59 pJ/bit, the proposed design can operate up to 112 Gbps OOK with signal-to-noise ratio (SNR) > 3 , although seven-tap feed-forward equalization was adopted within the DCA in this case.

These preliminary measurements results have already demonstrated comparable bandwidth performance to the reported lithium niobate modulators [2,3], which so far have not been realized with driver integration, which typically results in a significant bandwidth penalty. Furthermore, the power consumption of this work is 4 times lower compared to the electronic-plasmonic modulator [4] that has been integrated with electronics. In all comparative aspects, the proposed all-silicon optical transmitter solution is superior to all previous works in this field and illustrates great potential for next-generation optical communication links at 100 Gbaud and beyond.

Funding. Engineering and Physical Sciences Research Council (EP/L00044X/1, EP/L021129/1, EP/N013247/1, EP/T019697/1).

Acknowledgment. Dr. Ke Li acknowledges the funding support from the State Key Laboratory of Advanced Optical Communication System and Networks, Peking University, China. Dr. David J. Thomson acknowledges funding from the Royal Society for his University Research Fellowship.

Disclosures. The authors declare no conflicts of interest.

REFERENCES

1. G. T. Reed and G. Mashanovich, et al., *Nat. Photonics* **4**, 518 (2010).
2. M. He and M. Xu, et al., *Nat. Photonics* **13**, 359 (2019).
3. C. Wang and M. Zhang, et al., *Nature* **562**, 101 (2018).
4. U. Koch and C. Uhl, et al., *Nat. Electron.* **3**, 338 (2020).
5. M. Li and L. Wang, et al., *Photon. Res.* **6**, 109 (2018).
6. C. Xiong and D. M. Gill, et al., *Optica* **3**, 1060 (2016).
7. K. Li and D. Thomson, et al., in *European Conference on Optical Communication (ECOC)* (2018).
8. M. Raj and K. Chang, et al., *IEEE J. Solid-State Circuits* **55**, 1086 (2020).
9. J. Jun-De and H. Shawn, *IEEE Trans. Microw. Theor. Tech.* **56**, 3086 (2008).