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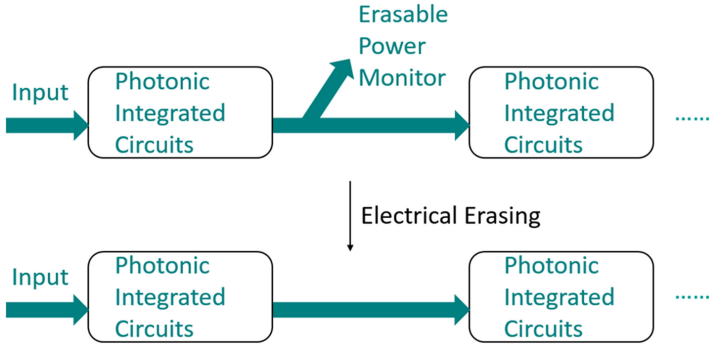
Xingshi Yu
Xia Chen
Milan M. Milosevic
Xingzhao Yan
Shinichi Saito
Graham T. Reed



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Electrically Erasable Optical I/O for Wafer Scale Testing of Silicon Photonic Integrated Circuits

Xingshi Yu,[1] **Xia Chen**,[1] **Milan M. Milosevic**,[1] **Xingzhao Yan**,[1] **Shinichi Saito**,[2] **and Graham T. Reed**[1]

[1]Zepler Institute for Photonics and Nanoelectronics, Optoelectronics Research Centre, University of Southampton, Southampton SO17 1BJ, U.K.
[2]Department of Electronics and Computer Science, Sustainable Electronic Technologies, University of Southampton, Southampton SO17 1BJ, U.K.

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Abstract: A technique for realizing electrically erasable photonics devices using micro-heaters for localized annealing of lattice defects in silicon is presented. The lattice defects have previously been introduced by ion implantation in order to cause a refractive index change. This technique can be used to fabricate electrically erasable on-chip directional couplers (DCs) and Mach-Zehnder Interferometer (MZI) switches. These devices can be used for wafer scale testing of photonics circuits, allowing testing of individual optical components in a complex photonic integrated circuit, or components for programmable optical circuits, whilst inducing negligible additional optical loss when erased electrically. In this paper, we report the designs and experimental results of fully, rapidly annealing of these devices.

Index Terms: Ion-implantation, Electrically erasable, Directional couplers, Mach-Zehnder Interferometer, Wafer scale testing.

1. Introduction

Silicon photonics is regarded as one of the most promising technologies for realizing on-chip integration of electronics and optics, and large-scale integration of optical circuits. Due to its promising potential for low fabrication costs and high integration capability, the industry has invested resources and effort to realize silicon photonics products for information interconnection, data transfer, LiDAR (light detection and ranging) and sensing technologies [1]–[6]. Various research groups in academia are also attracted by these promising prospects of silicon photonics and by potential applications for quantum technologies and computing [7]–[9].

To manufacture large scale photonic integrated circuits, maximizing wafer yield is essential to minimise costs, yet very limited methods are available to monitor the integrity and reliability of an optical device or components of a photonic circuit at wafer scale, until it is fully processed. Integrated optical devices, such as MZIs [10], ring resonators [11] and directional couplers, can be used to couple optical signals of a particular amplitude or a specific wavelength out of the circuit for

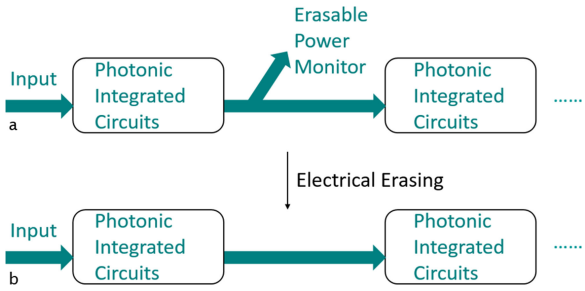

Fig. 1. A schematic of erasable optical monitor for wafer scale testing applications (a) before and (b) after electrical erasing.

monitoring purposes, which then can be used to test or adjust the function of the photonic circuit. However, after test, these optical devices will induce additional optical loss to the whole circuit, thus leading to increased power budget requirements and potential for additional optical reflections. In our recent work, we have used the germanium ion implantation technique in combination with rapid thermal annealing (RTA) or localized laser annealing to create erasable grating couplers in order to address this issue [12]. Furthermore, these technologies can also be used in trimming of ring resonators and MZIs [13]–[16].

RTA is a mature process in CMOS production and can control the temperature accurately. However, the entire wafer will be heated up and it is not suitable for local annealing which focuses on parts of devices. A continuous wavelength (CW) laser or an ultra-short pulse laser [17] can be used to realize the locally annealing. However, aligning and focusing the laser spot to the target position on chip is potentially a time-consuming process. Furthermore, laser annealing cannot be applied to test chips that are packaged. Therefore these annealing methods are not integration friendly and not ideal for commercial applications. Hence, electrical annealing is an attractive alternative.

In this paper, we demonstrate the electrical annealing of Ge ion implanted silicon photonic components using integrated TiN micro-heaters. Compared with conventional heaters of Pt and poly-Si, TiN has a higher melting point (2950 °C) and it is a CMOS compatible material [18]. A TiN micro-heater was fabricated on the top of each germanium ion implanted DC and MZI. The lattice damage in the optical devices can be partially or fully regrown when the implanted region is heated to the annealing temperature. As the TiN heater was integrated with the photonic circuits, the annealing process can be utilized both at wafer-scale as well as after final packaging. Furthermore, no additional time will be required for positioning and focusing, which is required for laser annealing.

TiN was used as the heater material in this work. As shown in Fig. 1, for wafer scale testing applications, DCs can be used in the form of erasable couplers. After annealing, test points are removed electrically resulting in no additional loss penalty for the photonic circuit. The proposed approach is relatively fast and highly compatible with large scale integration.

2. Device Design and Fabrication

The MZI is one the most widely used components in silicon photonic circuits for switching, modulation, filtering, sensing and building silicon photonics AI networks. By inducing a phase difference through ion implantation in the two arms of MZI, the transmission spectra of the MZI can be controlled. Fig. 2(a) and Fig. 2(b) show the structure of an ion implanted MZI with a TiN heater on the surface, between the waveguides, in both plan and cross sectional views.

The waveguides of the MZI arms are 500 nm wide and 220 nm thick. The 2 $\times$ 2 multimode interference (MMI) couplers act as the optical splitter and combiner in the MZI. The MMI is 6 μm wide and 44.8 μm long. Between the MMI coupler and the waveguides, the 20 μm long tapers are used to decrease optical loss.

The transmission of this MZI can be controlled by implanting different lengths of the implantation sections in each arm of MZI. A longer Ge ion implantation section (16 μm) was created in one arm

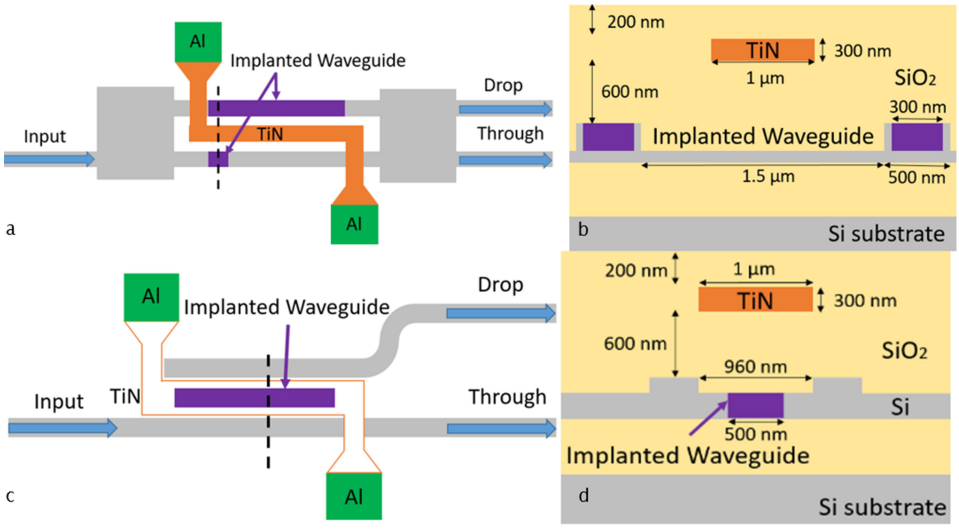

Fig. 2. A schematic of the ion implanted devices, (a) MZI top view, (b) MZI cross sectional view, (c) DC top view, and (d) DC cross sectional view.

of MZI, which was used to introduce a phase difference. A shorter implantation section (1 μm) in the other arm was used to balance any transition loss at the Si/amorphous Si interfaces. According to our previous study, over 80% of lattice disorder was created in silicon waveguides and there is an additional 1% optical loss at the interfaces [14].

Compared to the MZI, DCs can also achieve switching functions but the size of the device is much smaller. The design of two stage DCs is shown in Fig. 2(c) and Fig. 2(d). The refractive index change mainly originates from silicon lattice damage caused by Ge ion implantation [19]. The refractive index change will saturate when silicon is fully amorphized (the lattice is almost 100% damaged). In our previous work [20], [21], we found a dose of 10^{15} ions/cm^2 is sufficient to achieve full amorphization of silicon with Ge implantation, and a refractive index increase of 0.5 was measured. Higher implantation dose will mainly lead to more lattice damage, while higher implantation energy mainly will lead to deeper implantation depth. This implanted region can form an erasable waveguide as reported in our previous paper [22]. As illustrated in Fig. 2(c), the input optical signal can couple from input waveguide into the implanted waveguide in the middle, and then subsequently couple into the output waveguide at the top. A two-stage erasable DC is therefore formed.

The conventional waveguides are 500 nm wide with a 150 nm thick slab layer. A Ge-ion implanted waveguide was created in the silicon slab layer between the conventional waveguides, to couple light from the bottom waveguide to the top waveguide. The light (TE mode) was coupled from an optical fiber into the waveguides via grating couplers.

All the devices were fabricated in the Nano Fabrication Centre at the University of Southampton using a deep-ultraviolet lithography (DUV) scanner. SOI wafers with a 220 nm top silicon layer and 2 μm buried oxide have been used. The ion implantation process was carried out at the Ion Beam Centre at the University of Surrey. The energy and dose of the implanted Ge ions were 130 keV and 1×10^{15} ions/cm^2 respectively.

To prevent light absorption by the TiN, a silicon dioxide layer was deposited between the optical devices and TiN heaters. However, the thermal conductivity of silicon dioxide fabricated by the PECVD (plasma enhanced chemical vapour deposition) process is approximately 0.5–1 W/(m$*$K) [23], compared to silicon (130 W/(m$*$K)). Therefore, a thick silicon dioxide layer may lead to the reduced annealing efficiency of the implantation area. In this work, the optical response of silicon photonic devices was simulated using Lumerical Mode solution software, while the heat transfer through the structures was simulated using COMSOL. The simulation area for the DC and MZI was 300 μm $\times$ 300 μm. Simulation time was 10 seconds. The implanted region was set as amorphous

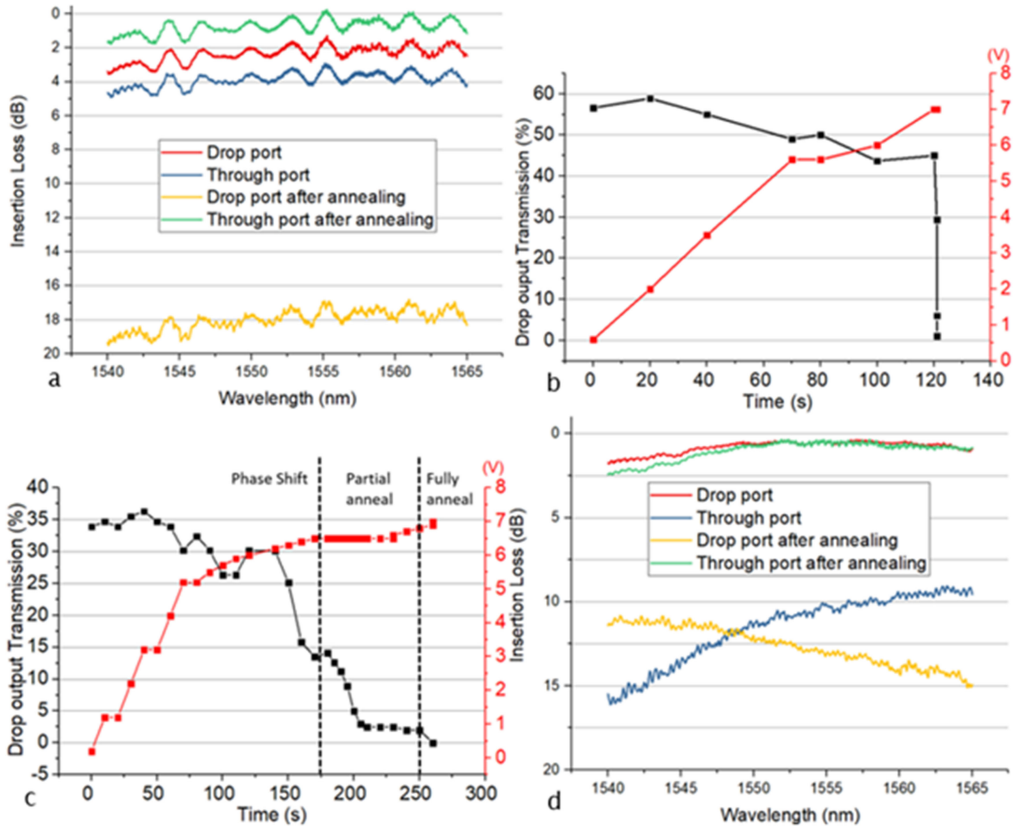

Fig. 3. (a) Optical transmission of DC before and after annealing by 19 μm TiN filament; (b) Experimental result showing the dynamics of the annealing process for a DC with 17 μm TiN filament; (c) Experimental results showing dynamics of the annealing process for a directional coupler with 16 μm TiN filament; and (d) Optical transmission spectrum of ion implanted MZI before and after annealing by 18 μm TiN filament.

silicon. Thus, the thermal conductivity of implanted silicon used in this simulation was 1.5 W/mK. The conductivity of the TiN heater was set to 10^5 S/m.

The oxidation temperature of TiN is between 400 and 800 °C [24], [25], however, based on our former study, using RTA [13], the temperature required for annealing of the ion implanted section is higher than 450 °C. Therefore, TiN may be oxidized before the implantation area reaches the required annealing temperature. To prevent this, a 200 nm thick SiO2 cladding layer was deposited on top of the TiN heaters to protect them.

3. Electrically Annealing for DC and MZI

For the directional couplers (DCs), the annealing process can regrow the lattice in the implanted waveguide between the two conventional waveguides, erasing the implanted waveguide. After the implanted waveguide is erased by the electrical heater, the light can no longer be coupled to the drop port of the waveguide, as the two conventional waveguides are too far apart to support evanescent coupling. Fig. 3(a) shows the optical transmission of a 2-stage directional coupler before and after annealing (the schematic of the structure is depicted in Fig. 2(c). The implantation length of this device is 17 μm while the length of the metal filament is 19 μm. The devices are not optimized for 100% coupling, and therefore, before the annealing, 65% of the signal power was coupled to the drop port while the remaining 35% was coupled to the through port. The annealing process lasted for approximately 30 seconds, and it was manually controlled.

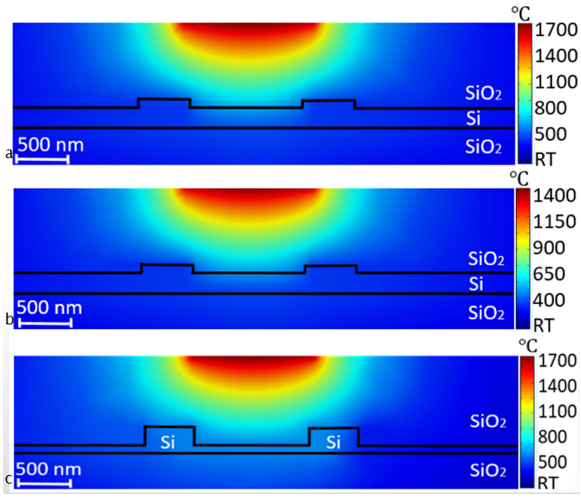

Fig. 4. Simulation result showing a temperature distribution across the vertical cross section of the devices at the different applied voltage. (a) DC with 17 μm filament at 7 V applied voltage; (b) DC with 17 μm filament at 6.5 V applied voltage; and (c) MZI with 18 μm filament at 6.5 V applied voltage.

In the first 25 seconds of the annealing process, the applied voltage was manually raised from 0 V to 8.7 V. As the applied voltage reached 8∼8.7 V, then the heater failed at approximately 8.7 V. The corresponding optical transmission detected from the drop port dropped from 65% to approximately 1.5%. This sudden drop of optical transmission at the drop port is consistent with a sharp refractive index change due to annealing process when the annealing temperature is reached. The signal collected from the through port was more than 95% of the original signal. The electrical annealing power was approximately 150 mW. Based on our previous study [22], the implanted waveguide is fully annealed in this case. The residual lattice damage left in the silicon waveguide after annealing caused an additional loss of 0.15 dB. According to our previously results [22], this two-stage DCs can achieve a maximum coupling efficiency of 95% to the drop port if appropriately designed. However, the fabricated DC devices under test in this paper were deliberately not designed to maximize the coupling efficiency, because wafer-scale testing typically does not require full coupling of light to the testing port. Therefore, we fabricated DCs with a wide range of coupling lengths, leading to varying coupling efficiencies. Nevertheless, the full annealing condition for the implanted waveguides of those DCs are the same, which very effectively demonstrates the electrical annealing process for this study.

The annealing experiments described above provided full annealing of the ion implanted directional couplers. A similar experiment was done by using DCs with 17 μm TiN filaments. According to Fig. 3(b), it can be seen that the annealing process was completed within a few seconds once the applied voltage reached 7 V. The electrical annealing power at this point was approximately 145 mW. The temperature distribution across the vertical cross section of the device is shown in Fig. 4(a). It shows that a temperature of the implanted section of directional coupler should be in the range 600 to 700 °C. This temperature is higher than our previous results using the RTA [13], and therefore electrical micro-heaters can locally achieve higher annealing speed and are therefore suitable for local electrical annealing. The index differences (both the real and imaginary parts) between crystalline silicon and the implanted silicon after recrystallization are negligible, as the peak germanium concentration in the silicon is less than 0.3% after implantation [13], [21], [22]. There is no discernable difference in performance between the fully annealed silicon and the original crystal silicon during our experimental characterization of the photonic devices.

In this paper, the thermal processes of electrical annealing are simulated in COMSOL. The dimensions set in COMSOL simulations are the same as those for fabricated devices. The key parameters for the materials used in these simulations are listed in Table 1. The electrical conductivity of the TiN filaments is calculated from our measured data. The parameters for Si and SiO2 come

TABLE 1
Key Parameters for Materials Used in COMSOL Simulations

Name of Parameters	Value
Electrical conductivity (TiN)	10^5 [S/m]
Thermal conductivity (Si)	130 [W/(m*K)]
Thermal conductivity (Buried SiO_2)	1.06 [W/(m*K)]
Thermal conductivity (Deposited SiO_2)	1.34 [W/(m*K)]

from references [26]–[28]. It can be seen that even at high annealing temperatures, the temperature drops to less than 100 °C within a few micrometres of the device under test, and so nearby devices remain unaffected.

To further explore the dynamics of the annealing process as a function of applied voltage and annealing time we have repeated the same experiments and more gradually raised the voltage of the TiN heater from 0 V to 7 V. The implantation area of the device experienced three different phases: an unannealed thermo optical tuning (temperature reversible change), a partially annealed phase, and a fully annealed phase. Fig. 3(c) shows the dynamics of this process from the start of the annealing process to the end when the heater failed due to the high applied voltage. During the first phase, the voltage was raised from 0 V to approximately 6.3 V, causing a steady decrease in the output signal of the drop port from 35% to about 20%. However, once the electrical power supply was removed, the transmission of the drop port returned to 35% of the input power. Therefore, we concluded that this phase is reversible and the change in the output power was caused by the thermo-optic phase shift of the directional coupler. The temperature increase causes a reversible change of the refractive index, and thus the coupling efficiency can be temporary controlled by the applied voltage. This principle is widely used to build programmable photonic circuits [29], or to tune the operating point of photonic devices such as MZIs. As the voltage was raised to 6.5 V, the transmission of the drop port was permanently changed, but slowly and controllably, and during this phase, ion-implanted sections were partially annealed. The simulated temperature distribution across the vertical cross section of the devices is shown in Fig. 4(b). In contrast to the former experiment, when the voltage is controlled in small steps around 6.5 V, the annealing speed of the implanted device was much more controllable and the corresponding simulated temperature of implanted section is about 500 °C. For the trimming application, this slow annealing control can give higher trimming accuracy. The electrical annealing power required for this partial annealing process was in the range of approximately 130 to 140 mW. Once the applied voltage reached 6.7 V, the output power had permanently dropped to zero, and the device was fully annealed.

For the MZI device shown in Fig. 2(a), a long implantation section (16 μm) was introduced to realize approximately 90% coupling efficiency to the drop port. Fig. 3(d) shows the optical transmission of the MZI before and after annealing. Based on our former experiments conducted for directional couplers, the heaters will fail in seconds when the applied voltage reaches 8 V. In this experiment, we applied an annealing voltage of 7 V. Within 10 seconds, approximately 90% of the input power was transferred from the drop port to the through port. The remaining 10% insertion loss is mainly caused by the phase error between the waveguide arms, not residual loss of the annealed MZI, which can be reduced by precise control over the annealing temperature or annealing length [14]. The electrical annealing power at this point was approximately 150 mW. To ensure a full annealing effect, the MZI was annealed for a further 10 seconds (at 7 V), however, this did not cause any change in optical transmission, indicating full annealing had been achieved. The simulated temperature distribution at the cross section of this device is shown in Fig. 4(c). It can be seen that a temperature of 600 to 700 °C was predicted in the middle of the silicon waveguides. The heater failed at an applied voltage of 7.5 V. In our experiment, the failure voltage varies, in the

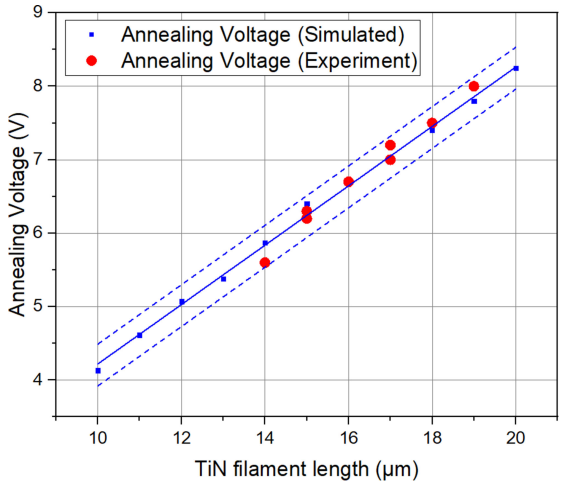

Fig. 5. Experimental and simulation voltages supplied to the filaments that achieved full annealing of the implanted devices.

range of 7 V to 8 V from chip to chip. We believe this difference is due to the fabrication variations and the non-uniformity of devices across the wafer.

A range of DCs with various TiN filament lengths were tested to the point at which full annealing was achieved. With an optimized design, the insertion loss of a two-stage erasable DC can be lower than 0.13 dB after annealing [22]. The experimental results are plotted in Fig. 5 together with the simulation results. The central solid blue line is the fitted curve for the simulated data. The two blue dotted lines represent the fitted curves for the maximum expected deviation of the experimental data from the simulation data, based upon simulations using the worst case variations in the fabrication process across the wafer. The experimental data falls well within these lines of maximum deviation, demonstrating the reliability of the process. The trend of experiment data agrees very well with simulation data, but the absolute annealing voltage varies slightly with the simulated values. Nevertheless, these results show the reliability and repeatability of the electrical annealing process for our fabricated devices. Furthermore, it gives a reference for the operational point of the electrical annealing process. It also shows that the power consumption for full annealing can be reduced with a shorter filament length for a shorter implanted waveguide. Therefore, we believe that the discrepancy between experimental data and simulation data is caused by fabrication variations across a wafer, which can lead to small variations of the heater dimensions, such as the thickness and width of TiN filament. These variations can also have a minor effect on the absolute heating efficiency of the annealing process.

4. Conclusions

In this paper, we have successfully demonstrated electrically erasable optical input and output (I/O) ports via both the DCs and the MZIs, which can be used for wafer scale testing of photonic integrated circuits, when integrated with grating couplers. Ge ion implantation of localized part of the silicon photonic devices in combination with electrical annealing was used to transfer light between output ports of these devices. The output signal can be efficiently switched to the through port using TiN micro-heaters. The temperature at which full annealing occurs was in the range 600 to 700 °C. The annealing process is very fast (a few seconds) and it is ideal for annealing in industrial mass production of photonic integrated circuits. By controlling the temperature in the phase shifting stage, the optical transmission of devices can also be controlled. As the temperature of the implanted area reaches approximately 500 °C, the implantation sections can be slowly annealed, thus achieving reversible or permanent refractive index changes, and reversible, partial or full annealing of the implanted silicon material. Therefore, this technique is very promising candidate for post-fabrication

trimming of silicon photonic circuits or programmable silicon photonic circuits, as well as facilitating wafer scale testing.

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