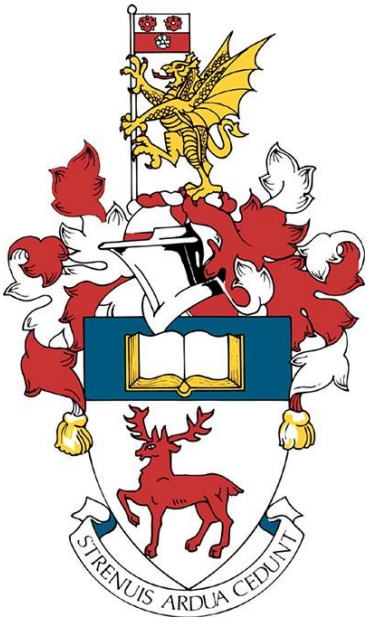
UNIVERSITY OF SOUTHAMPTON
Faculty of Engineering and Physical Sciences
School of Electronics and Computer Science



Narrow Slot Fully-Crystalline Accumulation Modulator for Low-Power Optoelectronic Interconnection

by

James Byers

A thesis submitted for the degree of
Doctor of Philosophy

July 2020

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

Narrow Slot Fully-Crystalline Accumulation Modulator for Low-Power Optoelectronic Interconnection

by James Byers

The information and telecommunication industry relies heavily on the opto-electronic (OE) modulator link between electronic computation and optical data transmission. As global data consumption has increased, the bandwidth, efficiency and cost demands placed upon OE modulators (in data centres for example) has also increased. OE modulators based on a silicon photonic platform have the potential to meet these bandwidth and efficiency demands, whilst remaining cost effective and industrially scalable due to their compatibility with conventional complemetary metal-oxide semiconductor (CMOS) fabrication processes.

The goal of this PhD project was to design and demonstrate a new type of energy efficiency, high-speed, fully-crystalline-Si (c-Si) modulator that could potentially answer the industry needs. To this end, in this thesis I present two new c-Si accumulation plasma dispersion effect (PDE) modulator designs. The critical OE component of these designs is, on the one hand, a bi-planar, horizontal-slot fin-waveguide on a double-silicon-on-insulator (SOI) platform, and on the other hand, a planar, partially recrystallised, vertical-slot rib-waveguide.

The key contributions I have made are (1) the development of a unique fabrication process involving anisotropic wet etching of mirrored Si crystal planes to realise the low-loss (0.85dB/mm) bi-planar, horizontal-slot fin-waveguide for use in an OE modulator, and (2) the fabrication of an efficient, fully-c-Si accumulation modulator with switching speed of 25Gb/s and modulation efficiency of 1.53V$\cdot\pi$. This modulator is the first demonstration of a uniquely designed modulator architecture which, with optimization, has the potential the genuinely address the industry demand for an energy-efficient, high-speed CMOS compatible OE modulator.

Contents

List of Figures

List of Tables

Acronyms

1D	1-dimensional
2D	2-dimensional
3D	3-dimensional
a-Si	amorphous-Si
AFM	atomic force microscope
ALD	atomic layer deposition
BOx	buried oxide
c-Si	crystalline-Si
CMOS	complemetary metal-oxide semiconductor
CMP	chemical mechanical polishing
CV	capacitance/voltage
CW	continuous-wave
DC	direct current
DCA	digital communication analyzer
DI	deionized
EDFA	erbium doped fibre amplifier
EM	electromagnetic
EO	electro-optic
EOT	equivalent oxide thickness
ER	extinction ratio
FCA	free carrier absorption
FDTD	finite difference time domain
FSR	free-spectral-range
GC	grating coupler

GSG ground-signal-ground

I/O input/output

IC integrated circuit

ICP inductively coupled plasma

LOCOS local oxidation of silicon

MMI multimode interferometer

MOScap metal-oxide-semiconductor capacitor

MSE mean squared error

MZI Mach-Zehnder interferometer

n-type negatively doped Si

OE opto-electronic

OEIC optoelectronic integrated circuit

p-type positively doped Si

PBG photonic bandgap

PDE plasma dispersion effect

PECVD plasma enhanced chemical vapour deposition

PhC photonic crystal

poly-Si polycrystalline-Si

PRBS pseudo-random bit sequence

Q-factor quality factor

RCA RCA clean

RF radio frequency

RIE reactive ion etching

rms root mean squared

RTA rapid temperature annealing

SEM scanning electron microscope

SISCap semiconductor-insulator-semiconductor capacitor

SMF single mode fibre

SOI silicon-on-insulator

TE transverse electric

TIR total internal reflection

TM transverse magnetic

WDDeM wavelength devision demultiplexer

WDM wavelength division multiplexer

WGM whispering gallery mode

Symbols and Nomenclature

C_m functional capacitance

C_p parasitic capacitance

$C_{junction}$ junction capacitance

E_{mod} modulus of elasticity

H_{wg} waveguide height

I_{loss} transmission loss

I_{max} maximum transmission intensity

I_{min} minimum transmission intensity

I_t transmission intensity

L wafer crack length

L_{shifter} phase shifter arm length

N_{eff} mode effective refractive index

R_{loss} loss coefficient

W_{fin} fin width

W_{trench} trench width

W_{wg} waveguide width

$\Delta\alpha$	apsorption coefficient change
$\Delta\boldsymbol{n}$	refractive index change
ΔL_{arm}	arm length difference
ΔN_e	change in free electron concentration
ΔN_h	change in free hole concentration
$\Delta\alpha_h$	$\Delta\alpha$ attributed to free hole concentration change
$\Delta\alpha_e$	$\Delta\alpha$ attributed to free electron concentration change
Δn_e	Δe attributed to free electron concentration change
Δn_h	Δe attributed to free hole concentration change
Λ_{fin}	fin period
α	absorption coefficient
β	propagation constant
δ	phase change
$\delta_{\Delta L}$	asymmetric section phase
δ_{active}	active arm phase
$\delta_{reference}$	reference arm phase
ϵ_0	electric permittivity of free space
ϵ_r	relative electric permittivity of dielectric
λ_{FSR}	free spectral range
$\mathrm{V}_\pi\mathrm{L}$	$\mathrm{V}\cdot\mathrm{cm}$ required to induce π phase shift
μ	magnetic permeability
μ_0	magnetic permeability of free space
ω	angular frequency
ρ	charge density
σ	conductivity
υ	specific surface energy
f_{3dB}	3dB bandwidth
k_0	wavevector
n	refractive index
r_3	Pockels electro-optic tensor

t_{carrier}	free carrier lifetime
t_{ox}	oxide thickness
t_{relax}	electrical circuit relaxation time
y	wafer crack separation distance/2
$\mathbf{B}$	magnetic induction
$\mathbf{D}$	electric displacement
$\mathbf{E}$	electric field
$\mathbf{H}$	magnetic field
$\boldsymbol{C}$	total capacitance
$\boldsymbol{N}$	doping concentration
$\boldsymbol{s}_3$	Kerr coefficient
$\boldsymbol{t}$	time
$\mathbf{A}$	area
$\mathbf{J}$	current density
$\mathbf{R}$	resistance
$\mathbf{t}_{\text{w}}$	wafer thickness
$\mathbf{V}_{\text{eff}}$	effective volume
$\mathbf{V}_{dc}$	direct current voltage

Chemicals and Reagents

ACE	acetone
Al	aluminium
Ar	argon
CHF_3	fluoroform
Espacer	thin-film conductive polymer

F fluoride

FOx16 flowable oxide from *Dow Corning*

GaAs gallium arsenide

H_2SO_4 sulfuric acid

HF hydrofluoric acid

HMDS hexamethyldisilazane

InP indium phosphide

IPA isopropanol

KOH potassium hydroxide

$LiNbO_3$ lithium niobate

MIBK Methyl isobutyl ketone

N_2 nitrogen

NH_2 amino group

NH_4OH ammonium hydroxide

NMP N-methyl-2-pyrrolidone

O_2 oxygen

PMMA poly(methyl methacrylate)

S1813 protective photo lithography resist

SF_6 sulfur hexafluoride

Si silicon

Si_3N_4 silicon nitride

$Si(OH)_4$ orthosicilic acid

SiO_2 silicon dioxide

Ti titanium

TiN titanium nitride

TMAH tetramethylammonium hydroxide

UVN-30 negative electron-beam lithography resist

ZED N50 n-Amyl Acetate

ZEP520A positive electron-beam lithography resist

Declaration of Authorship

I, James Joseph Byers, declare that the thesis entitled *Narrow Slot Fully-Crystalline Accumulation Modulator for Low-Power Optoelectronic Interconnection*, and the work presented in the thesis are both my own, and have been generated by me as a result of my own original research.

I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as: [1], [2], [3], [4], [5], and [6].

Signed: .....

Date: .....

Acknowledgements

I would like to thank my supervisor Professor Shinichi Saito for his guidance during my PhD, as well as my secondary supervisor Dr Kapil Debnath, both of whom have provided invaluable support technically, as well as in terms of my general understanding as a student. I would also like to thank Dr Khaled Husain for his invaluable support with fabrication, Moise Sotto for his help with some simulations, and Dr Hideo Arimoto for providing the initial horizontal-slot fin-waveguide designs. I would like to thank the rest of my research group generally, as well as the technical staff at the Southampton Nanofabrication Centre.

I want to thank my friends in Southampton for looking after me and keeping me on the (mostly) straight and narrow, particularly Daniel Burt, Rafa Gutierrez, Kevin Alabarta and Cesar Angeles. I would also like to thank my family for their support and encouragement throughout, particularly my parents Richard Byers and Ann Wilson. And lastly I would like to thank my girlfriend Iris, who believed in me even when I didn't believe in myself.

For Iris

Chapter 1

Introduction

For over 40 years optical interconnects have been developed to replace, first, long range electronic communication (erbium doped fibre amplifier (EDFA) enabled optical fibres[7] replacing copper coaxial cables for long-distance (1km-10,000km) telecommunication), then medium range electronic communication (fibre optics replacing copper cables for 1m-1km distances), and now they are set to replace electrical short-range (<1m) communication. Whenever shorter range interconnects have transitioned from electronic to optical communication, it has required the development not only of the new fibre optic cables themselves, but also the light source, amplifier, detector, wavelength division multiplexer (WDM) and wavelength devision demultiplexer (WDDeM) components, and importantly, the opto-electronic (OE) modulator to convert the electronic signal into an optical signal.

Silicon (Si) based devices have long been chosen for passive optical components due to the refractive index (n) difference (Δn)[8] of Si with its native oxide silicon dioxide (SiO_2), low optical loss[9], high mode confinement[10] (effective volume (V_{eff})), high bandwidth[11] (sustaining multiple wavelengths simultaneously for multi-channel operation), transparency at telecommunication wavelengths, and ease of production. However, owing to the fact that unstrained Si exhibits no 1^{st} order electro-optic (EO) effect[12] (due to its centrosymmetric crystal structure[13]), only a very weak 2^{nd} order EO effect, and lacks a direct energy bandgap, III-V semiconductor materials have traditionally dominated active optoelectronic components such as lasers[14,15], detectors[16] and modulators[17]. Despite these challenges, the desire for fully integrated on-chip optoelectronic integrated circuits (OEICs) with fully integrated optical emission, amplification, modulation and detection has driven active OE component innovation in the direction of Si photonics, which benefits from over 50 years of Si integrated circuit (IC) development and investment.

The rapid growth in the amount of data traffic in modern data centres from 4.7ZB per year in 2015 to a projected 15.3ZB per year for 2020 (27% annual compound growth

rate)[18] is pushing the electronic and OE performance metrics of device density, modulation speed, thermal output and energy consumption per bit etc. to the limit of what is possible with current technology. On-chip transistor density and computation speed continues to increase, but as parallel computation increases and bandwidth required for input/output (I/O) increases, the industry is now encountering the "bottleneck" interconnect problem, whereby increased computation is now limited by the speed at which information can be communicated between chips and servers[19,20]. Along with a Si laser/photodiode and small-scale photodetector, a critical technology required to solve this bottleneck problem of data transfer is an on-chip OE modulator. This device could in the long-run bridge the gap between separate components within a chip, and in the near term will allow better high-speed communication with off-chip systems. Traditionally, on-chip and off-chip interconnects have been metal (with IC being completely electronic), but industry is moving towards OE modulators to help solve the bottleneck problem of low power[21,22], high speed[23], cheap interconnects. Si photonics is also a logical approach to this problem because it is already compatible with complemetary metal-oxide semiconductor (CMOS) standard fabrication processes. Optical interconnects experience no crosstalk[24,25], have higher density with WDM fibres exhibiting 96 separate channels[26] commercially (more channels demonstrated academically) with a wavelength separation of 0.4nm (50GHz) etc.

OE modulators come in a variety of forms, using different modulation mechanisms, for example the 1st order nonlinear EO Pockel's effect (which lithium niobate crystal exhibits) or the 2nd order nonlinear EO Kerr effect which have traditionally been used in non-Si photonic devices. These effects can be used to change the n of the waveguide material as a function of input voltage (driven by an electronic signal), and therefore change the n of the propagating light. The electronic signal modulates at a certain speed, which modulates the input voltage of the device, which modulates the refractive index of the light. In an interference design device architecture, this very small refractive index change can be converted into a phase change between two beams of light, which results in either constructive or destructive interference, modulating the output light intensity. If the device architecture incorporates a resonant structure, this very small refractive index will cause the light to couple or decouple to the resonant structure, also modulating the output light intensity.

The main problem for Si based OE modulators is that due to its centrosymmetric crystal structure[27], it does not exhibit Pockel's effect[28], and it exhibits the the Kerr effect very weakly[28]. The bias V required to induce Δn in Si sufficient for phase change modulation using an Mach-Zehnder interferometer (MZI) or resonant structure exceeds the break down voltage of Si (Si becomes conductive at this point). The Franz-Keldysh effect is also very weak in Si at telecommunication wavelengths. Together, these three effects are the dominant operating mechanisms of III-V material semiconductor modulators. The solution to this problem is to use either the plasma dispersion effect (PDE) or the

thermo-optic effect. As the thermo-optic effect is limited to switching speeds on the order of MHz, it is too slow for GHz+ modulation speed required for telecommunication interconnects, which can only be produced in silicon based devices using PDE.

The PDE operates by changing the concentration of electrons and/or holes in a Si waveguide, which can change the n of the propagating light, which can then be converted into a change in output intensity (using an interference or resonance device). The concentration of free electrons and holes can be changed using one of three device architectures and corresponding mechanisms. One, carriers can be injected into the centre of a p-i-n diode structure. Two, carriers can be depleted from a depletion region at the centre of a p-n diode structure. Three, carriers can be accumulated either side of a narrow gate oxide slot in the middle of a metal-oxide-semiconductor capacitor (MOScap) structure.

The development of PDE Si OE modulators began with the development of very-low-speed(<MHz) carrier injection devices[29–31] due to the fact that fabrication of p-i-n diode structures within the waveguide was considerably less demanding than the fabrication of p-n diode structures or MOScap structures within the waveguide. Despite the fact that the first Si photonic OE switch was demonstrated in 1987[32] (which utilized carrier injection into the intrinsic region of a p-i-n diode waveguide as the mechanism to manipulate waveguide n), it took 13 years before the demonstration of a modulator with an operational speed >10MHz[33], and a further 4 years before the demonstration of the first a modulator with an operational speed >1GHz[34] (which was rapidly improved the following year when an operational speed of 10Gbit^{-1} was demonstrated[35]).

Despite the initial high-speed breakthrough occurring using a MOScap accumulation based device[34,35], due to fabrication concerns and a desire to increase operational speed, many high-speed, low-efficiency depletion based devices were subsequently demonstrated[36–42], with several exhibiting operational speed of 50Gbit^{-1}[43–46]. The current record for operational-speed in literature is 90Gbits^{-1}[47], which was achieved in a depletion device. High-speed depletion devices come at the cost of decreased energy efficiency compared to injection devices (which correspondingly suffer from lower speed limits, but with higher energy-efficiency). The important figure-of-merit used to determine modulation energy efficiency is $V_\pi L$, which is the required voltage applied of 1cm of the device to induce π phase-shift in the propagating light. The 50Gbits^{-1} devices demonstrated by Tu et al.[46] and Thomson et al[43] have $V_\pi L$ energy efficiencies of 26.7Vcm and 2.8Vcm, respectively, for example. The modulation speed is certainly one of the most important operating parameters, and there is niche industry demand for very-high-speed modulation at the cost of efficiency, however, because energy and cooling costs are such a large and growing concern for large data-centres, the primary industry demand is for medium-speed, high-energy-efficiency modulation.

Several medium-speed accumulation modulators have been demonstrated with high energy efficiency[48–52]. Fujikawa et al. demonstrated an operational speed of 25Gbits^{-1} with

a $V_\pi L$ of 0.28Vcm[50], Webster et al. demonstrated an operational speed of 28Gbits^{-1} with a $V_\pi L$ of 0.2Vcm[52]. These devices demonstrate the principle that accumulation based modulators can target the industry need for "middle-ground" OE interconnects between high-speed, low-efficiency depletion devices (which currently dominate the market, but present scaling problems due to high energy inefficiency), and low-speed, high-efficiency injection devices (which cannot support the high speeds necessary to satisfy most OE interconnect requirements). Because of the industry need for "middle-ground" OE interconnect devices, and the fact that fabrication methods have improved significantly over the last 20 years such that previously very challenging MOScap embedded waveguide designs can now be fabricated and tested in an academic environment, it is now a very promising time to pursue novel accumulation modulator designs to address this industry need.

Conventional accumulation OE modulators utilize a vertically stacked $Si/SiO_2/Si$ MOScap structure built into a rib-waveguide. This structure relies on either high-optical-loss, deposited, partially amorphous-Si (a-Si) or polycrystalline-Si (poly-Si)[34,48,49], or bonded double-crystalline horizontal-slot waveguide structures which introduces parasitic capacitance which increases energy consumption and limits switching speed[51]. Schematic representations of a conventional accumulation modulator utilizing poly-Si, and one using a bonded double-crystalline substrate are shown in 1.1 (a) and (b) respectively. A key challenge that must be solved is the design and fabrication of a fully-crystalline-Si (c-Si) slot-waveguide structure without any intrinsic parasitic capacitance. This thesis will explore two proposed solutions to this challenge.

The first possible solution that is explored is a design based on a horizontal-slot, fin-waveguide on bonded double-silicon-on-insulator (SOI)[1], which allows one to take advantage of the inherent $c\text{-}Si/SiO_2/c\text{-}Si$ structure easily[53]. A schematic of this design is presented in 1.1 (d). Fabrication of high quality OE devices on double-SOI is also a prerequisite to the further development of multi-layer optoelectronic devices or multi-layer integrated optoelectronic and microelectronic devices on the same double-SOI substrate. A challenge associated with using a horizontal-slot double-SOI is how to pattern the bottom SOI layer using lithography of the top SOI layer, since the double-SOI wafers must be bonded prior to patterning so as to ensure excellent interface quality. I will demonstrate the use of anisotropic wet-etching of mirror-aligned top and bottom SOI layers to solve this challenge, and and thereby establishing a unique fabrication process to fabricate horizontal-slot strip/fin-waveguides consisting of two c-Si SOI layers separated by a 10nm gate oxide SiO_2 layer, with multiple fin-gratings for use as electrode connections. In the future this design will also enable optical communication to be overlaid directly above microelectronic computation, which will lead to a whole new architecture of fully integrated (as well as vertically integrated) optoelectronic integrated circuits (OEIC). This structure also has the secondary benefit that it allows for easy ion implantation/-doping of the SiO_2 slot (for example in the case of an erbium doped slot-waveguide

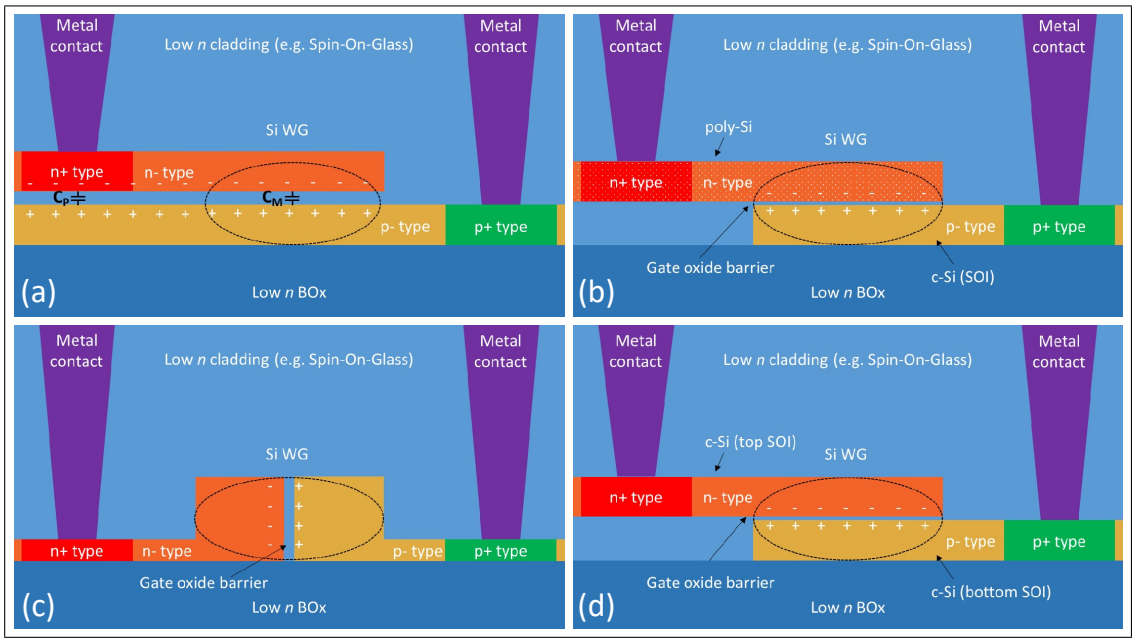


FIGURE 1.1: Schematic representations of conventional accumulation modulator designs ((a) and (b)), demonstrating their inherent weaknesses, and two proposed solutions to these weaknesses ((c) and (d)). Cross-section through active region of waveguide. Black dotted oval represent approximate region of propagating mode. (a) Double-c-Si design formed by bonding two (100) orientation SOI wafers. Total capacitance across the gate oxide is made up of two components, C_m and C_p, only the C_m. Utilizing this platform there is currently no way to remove the bottom-left SOI, thus removing C_p. The propagating mode is maintained in the position that it is (at the edge of the top SOI) as a WGM at the edge of a microdisk resonator. (b) Deposited a-Si can only be partially recrystallized to high-optical loss poly-Si. (c) Proposed solution design #1: Vertical-slot oxide grown on the side of exposed Si wall using LOCOS process, then a-Si is deposited and recrystallized, before patterning waveguide with vertical slot in the centre. (d) Proposed solution design #2: Double-c-Si design formed by bonding two (110) orientation SOI wafers. Anisotropic tetramethylammonium hydroxide (TMAH) wet etching can be used to suspend the top SOI, thus removing C_p.

optical amplifier), a process that is difficult to achieve for high aspect ratio vertical-slot designs.

The second possible solution that is explored is the use of a fully-c-Si vertical-slot rib-waveguide[3,54] accumulation modulator. A schematic of this design is presented in 1.1 (c). This device is fabricated using a process involving sidewall local oxidation of silicon (LOCOS) to grow the vertical gate-oxide layer, deposition of a-Si which is then fully recrystallised using the SOI layer as a crystallization seed, chemical mechanical polishing (CMP) planarization, waveguide patterning and etching. Subsequently, electrically active components (doping, metal contacts etc.) are fabricated to complete the electrically active design. This design is planar, and is therefore compatible with established Si photonics devices on the same chip, which has advantages in terms of on-chip integration. This solution will be shown to satisfy the key aim of the PhD which is to fabricate

and characterise a low-power-consumption fully-c-Si OE modulator that overcomes the challenges listed above.

The key aims of this thesis are:

1. Propose two new possible fully-c-Si slot-waveguide design architectures that do not include intrinsic parasitic capacitance, for use in an energy-efficient, high-speed accumulation modulator.

2. Demonstrate the feasibility of fabricating these two fully-c-Si slot-waveguide designs.

3. Utilize one of the new designs to fabricate an optoelectronically active, high-efficiency, high-speed accumulation modulator, and demonstrate such performance.

The thesis is organized as follows:
Chapter 2 will give an overview of the theory and relevant literature relating to three areas. Firstly electromagnetic (EM) wave propagation (for strip and slot waveguides, grating couplers (GCs), multimode interferometers (MMIs), Mach-Zehnder interferometers (MZI) and photonic crystal (PhC) bandgap guided propagation (relevant for one of the fin-waveguide designs)) will be discussed. Secondly, the active use of OE modulators, focussing on accumulation modulators, will be presented. And thirdly, some key Si photonics fabrication techniques (wafer bonding and thinning, and anisotropic wet etching using tetramethylammonium hydroxide (TMAH) etc.) will be discussed.
Chapter 3 will present the two distinct designs (horizontal-slot fin-waveguide accumulation modulator and vertical-slot rib-waveguide accumulation modulator) that make up the two proposed solutions in this thesis. These will be presented with relevant computational simulations. The fabrication process flow for each of these designs will also be presented in detail here.
Chapter 4 will present the fabrication characterisation and the post-fabrication characterisation and analysis of the passive horizontal-slot strip-waveguides. This chapter will also present the characterisation of MOScap devices fabricated on the bonded double-SOI demonstrating the quality of the bonding-oxide and its suitability for use in an active modulator.
Chapter 5 will present the analysis of the fin-waveguides themselves, and the their use in passive MZI devices.
Chapter 6 will present the fabrication characterisation and the post-fabrication characterisation and analysis of the passive vertical-slot rib-waveguides, and will then go on to present the analysis and operational characteristics of the active accumulation modulator based on the vertical-slot rib-waveguide.
Finally, Chapter 7 will provide a summary of the thesis, highlighting the key conclusions (two new silicon photonics architectures proposed and developed, and a new architecture accumulation modulator demonstrated), and propose some possible future work.

Chapter 2

Theory And Literature Review

2.1 Waveguides

EM waves with λ smaller than the cross-section of the waveguide through which they are guided can often be described using total internal reflection (TIR) and Snell's law. However, when the cross-sectional dimensions of the waveguide approach or are smaller than the λ of the propagating EM wave, the wave nature of light needs to be taken into consideration and Maxwell's equations need to be utilized.

2.1.1 Electromagnetic Propagation in 2-Dimensional Waveguides: Maxwell's equations

The wave equation can be derived from Maxwell's equations. Maxwell's four differential equations relate the electric field ($\mathbf{E}$) and electric displacement ($\mathbf{D}$) to the magnetic field ($\mathbf{H}$) and magnetic induction ($\mathbf{B}$), as well as the charge density (ρ) and the current density (J) as follows (for the specific case of a charge free ($\rho = 0$, J $= 0$), nonmagnetic (magnetic permeability (μ) = magnetic permeability of free space (μ_0)) dielectric (conductivity (σ)$= 0$) medium) :

$$\nabla \cdot \mathbf{E} = 0 \tag{2.1}$$

$$\nabla \cdot \mathbf{H} = 0 \tag{2.2}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{H}}{\partial t} \tag{2.3}$$

$$\nabla \times \mathbf{H} = \mu_0 \epsilon_0 \frac{\partial \mathbf{E}}{\partial t} \tag{2.4}$$

μ_0 = magnetic permeability of free space (H/m) = $4\pi \times 10^{-7}$ H/m
ϵ_0 = electric permittivity of free space (F/m)
t = time (s)

These four equations can be used to derive the wave equations for magnetic (2.5) and electric fields (2.6) in an inhomogeneous medium ($n(\mathbf{r}) = \mathbf{r}$).

$$\nabla^2\mathbf{H} = \mu_0\epsilon_0 n^2 \frac{\partial^2\mathbf{H}}{\partial t^2} \tag{2.5}$$

$$\nabla^2\mathbf{E} = \mu_0\epsilon_0 n^2 \frac{\partial^2\mathbf{E}}{\partial t^2} \tag{2.6}$$

A propagating EM wave can be split into x, y and z component parts, E_x, E_y, E_z, H_x, H_y, H_z. For an EM wave propagating in the z-direction, it can be polarized in two ways that must be considered for waveguide design. These are transverse electric (TE) polarization or transverse magnetic (TM) polarization, which are defined as follows:

$$\text{TE polarization: } \mathbf{E} = \mathrm{E}_x;\ \ \mathrm{E}_y{=}\mathrm{E}_z{=}0;\ \ \mathrm{H}_x{=}0$$

$$\text{TM polarization: } \mathbf{H} = \mathrm{H}_x;\ \ \mathrm{H_y}{=}\mathrm{H}_z{=}0;\ \ \mathrm{E}_x{=}0$$

The TM wave equation (2.7) and TE wave equation (2.8) describe a polarized EM wave propagating in the z-direction in a homogeneous medium, and incorporate the mode defining parameter, the propagation constant (β).

$$\frac{\partial \mathrm{H}_x(y)}{\partial t^2} = [k_0^2 n^2(y) - \beta^2]\mathrm{H}_x \tag{2.7}$$

$$\frac{\partial \mathrm{E}_x(y)}{\partial t^2} = [k_0^2 n^2(y) - \beta^2]\mathrm{E}_x \tag{2.8}$$

$\mathrm{H}_x(y)$ indicates that the magnetic field in the x-direction is a function of y.
k_0 = wavevector = $(\frac{2\pi}{\lambda_0})^2 = \mu_0\epsilon_0\omega^2$
λ_0 = wavelength in vacuum (nm)
ω = angular frequency (rad/s)
n = refractive index (constant in this case)
$\beta = k_0 N_{eff}$
N_{eff} = mode effective refractive index

β defines a unique EM field distribution, which is a unique mode of propagation. β can be determined from the transcendental equations (which are specific to the waveguide geometry) for TE and TM polarization separately. If a single solution to either of these equations exist, a single propagating mode exists; the waveguide is single-mode. If multiple solutions exist, multiple propagation modes exist; the waveguide is multi-mode, however, the first "fundamental" mode carries most of the energy. Only a finite number of discrete propagation modes can exist. If no solution exists, no propagation mode exists and only unguided radiation modes exist, which will leak out into the surrounding material. The horizontal-slot, strip and fin-waveguides, as well as the vertical-slot rib waveguide, on which the accumulation modulators proposed in this thesis are based, are designed to contain one fundamental propagating TE mode for the energy spectrum of

interest (λ ~1500-1600nm). A schematic and finite difference eigenmode simulation of a TE mode, conventional Si on buried oxide (BOx) strip-waveguide with SiO_2 cladding (performed using *Lumerical Solutions* MODE: Waveguide Simulator, version 2017a[55]) is presented in Figure 2.1.

The conventional TE mode presented in Figure 2.1 is the fundamental spacial profile solution to discretized Maxwell's equations, across a 2-dimensional (2D) cross-sectional area, for this particular geometry. The electric field intensity, $|\mathrm{E}(r)|$ (Figure 2.1(a)), and magnetic field intensity, $|\mathrm{H}(r)|$ (Figure 2.1(b)), at each point, r, are functions of their x, y, z components, and are defined in 2.9 and 2.10 respectively:

$$|\mathrm{E}(r)| = |E_x(r)|^2 + |E_y(r)|^2 + |E_z(r)|^2 \tag{2.9}$$

$$|\mathrm{H}(r)| = |H_x(r)|^2 + |H_y(r)|^2 + |H_z(r)|^2 \tag{2.10}$$

The energy density, $\eta(r)$, at each point, r, is a function of $|\mathrm{E}(r)|$, $|\mathrm{H}(r)|$ and $\epsilon(r)$, and is defined in 2.11:

$$\eta(r) = \frac{1}{2}(\epsilon(r)|\mathrm{E}(r)| + \mu_0|\mathrm{H}(r)|) \tag{2.11}$$

where $\epsilon(r) = \epsilon_0 n(r)^2$. $\epsilon(r)$ is not dependent on changeable $\mu(r)$ as neither Si nor SiO_2 are magnetic, and therefore $\mu(r) = \mu_0$ for all values of r. Despite the fact that there is an obvious $|\mathrm{E}(r)|$ peak either side of the waveguide, within the low n cladding, as evidenced in Figure 2.1(b), this only has a minor effect on the $\eta(r)$ in this region (Figure 2.1(c)). Each peak accounts for 9% of the total $\int |\mathrm{E}(r)|dxdy$ across the entire simulation region (56% of total $\int |\mathrm{E}(r)|dxdy$ is within the Si waveguide), but <1% of the total $\int \eta(r)dxdy$ across the entire simulation region (73% of total $\int \eta(r)dxdy$ is within the Si waveguide). This is for two reasons: (1) $|\mathrm{H}(r)|$ contributes negligibly to $\eta(r)$ in this region, and (2), $\frac{\epsilon(\mathrm{Si})}{\epsilon(\mathrm{SiO_2})} = 5.5$, and therefore the same $|\mathrm{E}(r)|$ contributes to higher $\eta(r)$ in the Si waveguide region.

2.1.2 Optical Loss Mechanisms

In an ideal single mode waveguide, the propagating mode is perfectly confined in two dimensions and is subject to 0% optical transmission loss. However, in reality, there are several important loss mechanisms that must be taken into account, and are outlined herein (in order of increasing importance for nm scale strip and slot-waveguide designs):

- Inter-band absorption
  A photon excites a valance band electron across the bandgap into the conduction band, which then relaxes in Si's case usually with the emission of a phonon. This effect is negligible at $\lambda = 1.55$ μm, as the incident photons do not have the required energy to excite electrons across the bandgap.

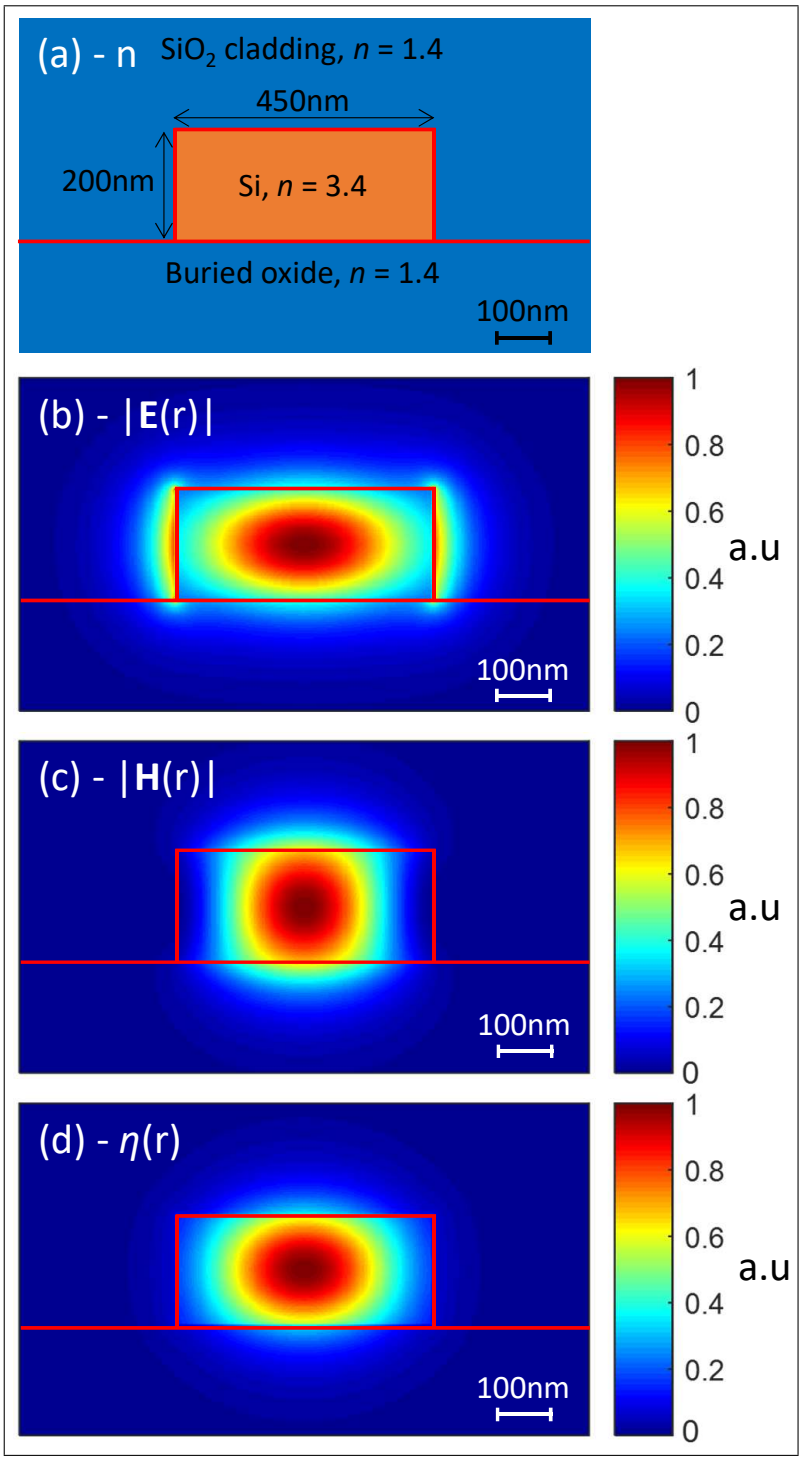


FIGURE 2.1: (a) Cross-section schematic of simple Si strip-waveguide on BOx with typical design parameters; waveguide width = 450nm and waveguide height= 200nm. n_{Si}=3.4; n_{BOx}=1.4; n_{clad} = 1.4. Normalized electric field intensity ($|\mathbf{E}(\mathrm{r})|$), normalized magnetic field intensity ($|\mathbf{E}(\mathrm{r})|$), and normalized energy density ($\eta(\mathrm{r})$), for the fundamental TE mode of structure (a) is shown in (b), (c) and (d) respectively. The majority of dominating components are strongly confined to the high n Si strip-waveguide. Normalized profile and arbitrary units used as absolute values depend on arbitrary input power.

- Volumetric inhomogeneity scattering
  Any internal discontinuity in $n_{x,y}(z)$ (for a 2D waveguide propagating in the z-direction) causes a change in the mode profile. This mode-mismatch causes scattering of the electromagnetic wave into the cladding. It is for this reason that it is crucial to maintain a uniform oxide layer through excellent bonding quality (no voids) when fabricating strip-waveguides with on bonded double-SOI with nm scale bonding oxide.

- Free Carrier Absorption (FCA)
  Photons are absorbed by free electrons or holes present in the material. This is particularly important when considering positively doped Si (p-type) and negatively doped Si (n-type) regions for active devices such as OE modulators. It is also a necessary side effect of increasing the free carrier density to manipulate the material n. This effect is described by the Drude-Lorenz equation, and is explained in more detail in Section 2.2.2. As a rough estimate, a free carrier concentration of $10^{18}/\text{cm}^3$ is responsible for an additional FCA propagation loss of approximately 10dB/cm.

- Surface roughness scattering
  Waveguide surface roughness can be modelled as a random variation in waveguide width, with changes in local n along the sidewall surface. This random change of refractive index is a "pseudo-grating" (as opposed to a normal grating which has a periodic change in refractive index), which can couple light into the surrounding cladding[56]. As waveguide width decreases, the sidewall/interface region makes up a larger proportion of the waveguide area, and therefore (in a conventional device) there is a greater mode concentration at the sidewall and the pseudo-grating has a larger effect on the mode. Surface roughness scattering is proportional to Δn^3 [57]. This is the dominant loss mechanism for passive single-mode waveguides (dry etching incurs significant roughness) with widths $< 1\mu$m, and must therefore be minimised if possible by wet etching techniques.

2.2 Modulators

2.2.1 Si and Non-Si Optoelectronic Modulators

Si was initially not an obvious material on which to build active OE components. It exhibits no 1$^{\text{st}}$ order EO effect (Pockels effect) due to its centrosymmetric crystal structure, and only a very weak 2$^{\text{nd}}$ order EO effect (Kerr effect) with which to directly modulate a change in the real refractive index change (Δn) or the imaginary refractive index (absorption coefficient change ($\Delta\alpha$)) in the material. Traditionally, non-centrosymmetric materials that demonstrate one of these effects, such as lithium niobate ($LiNbO_3$), which

possesses ferroelectric properties (local internal electric polarization which can be manipulated by an applied electric field) or III-V material gallium arsenide (GaAs) (which has the added benefit of having a direct energy bandgap and can be used to make near-infrared laser diodes[58]) have been used to modulate light directly.

Optical modulation requires the change of output optical intensity, either by directly modulating changes in absorption or by modulating changes in the refractive index (which can be used in a device such as an interferometer to shift the phase of a propagating wave, or in a resonator to couple light from the main (access) waveguide into a secondary resonant structure, which then indirectly effects the output intensity). The refractive index of a material is made up of a real and an imaginary component, the refractive index (n) and the absorption coefficient (α) respectively.

Δn - refractive index change

$\Delta \alpha$ - apsorption coefficient change

An electrical signal can induce a change in $\mathbf{E}$ in the material which then causes a Δn and $\Delta \alpha$ in the material, which modulates the light propagating through that material, thus converting the electrical signal into an optical signal. The primary mechanisms traditionally used by non-Si modulators to effect material Δn and $\Delta \alpha$ are the following:

Pockels effect (not present in Si)

The 1st order (linear) electro-optic effect changes n proportional to the applied electric field, $\mathbf{E}$, by changing the materials birefringence (a material property whereby the refractive index of the material is dependent on the light polarization and propagation direction) according to the following equation 2.12[59] (when the direction of the applied $\mathbf{E}$ field is aligned with the direction of the principle crystal axis):

$$\Delta n = r_3 n_3 \frac{\mathbf{E}_3}{2} \tag{2.12}$$

Where:
r_3 = Pockels electro-optic tensor (material and crystallographic orientation dependent, hence the subscript "3" denoting the alignment in the three relevant crystal planes)
n_3 = refractive index in the direction of the applied field, $\mathbf{E}$.
$\mathbf{E}$ = applied electric field

Kerr effect (weakly present in Si)

The 2nd order (quadratic) EO effect. Δn is proportional to $\mathbf{E}^2$ according to the following equation 2.13:

$$\Delta n = s_3 n_0 \frac{\mathbf{E}^2}{2} \tag{2.13}$$

Where:
s_3 = Kerr coefficient
n_0 = refractive index whe n $\mathbf{E} = 0$

Δn is independent of $\mathbf{E}$ direction relative to crystal axis. Applied $\mathbf{E}$ required for Δn sufficient for phase change modulation in Si occurs at an applied $\mathbf{E}\sim 100\text{V}/\mu\text{m}$ at $\lambda = 1.33\mu$m (theoretically calculated by Soref and Bennet[12]) which is above the breakdown voltage of Si. The change in Δn as a function of applied electric field for $\lambda = 1.3$-1.6μm is plotted in Figure 2.2 (a) (from Soref and Bennet[12]). Figure 2.2 (b) (from Soref and Bennet[12], original data from Wendland and Chester[60], and also reproduced in Reed, Chapter 4, Figure 4.4[59]) shows the change in the $\Delta\alpha$ of Si as a function of photon energy at various applied electric fields. At photon energy < 1.02eV (i.e. at $\lambda > 1033$nm) the Franz-Keldysh effect contributes negligibly to total absorption coefficient (α) compared to other loss mechanisms such as volumetric scattering, free carrier absorption (FCA) or surface roughness scattering[59].

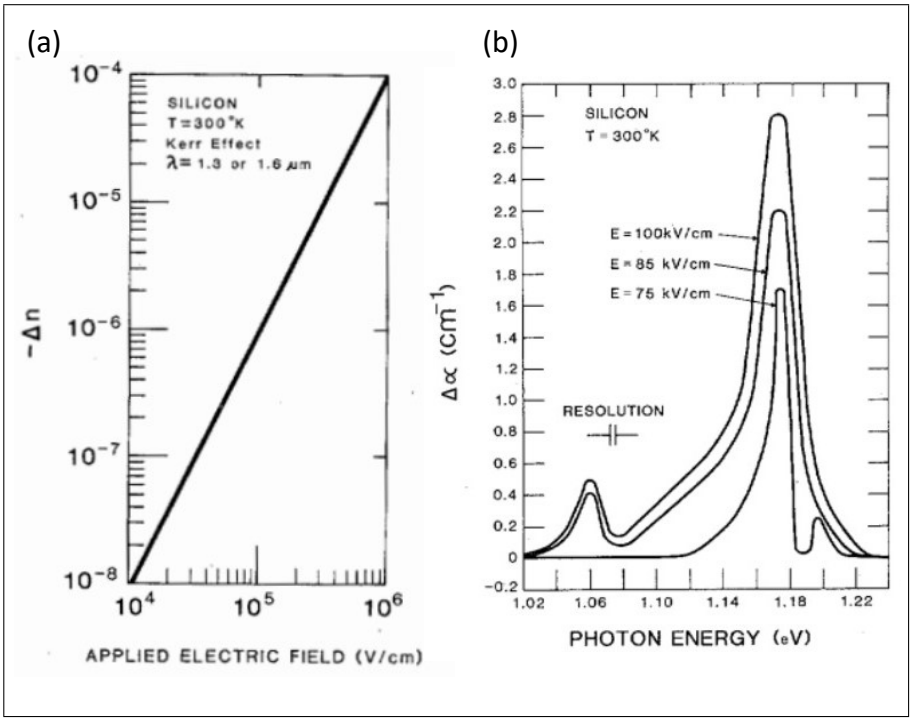


FIGURE 2.2: (a) Δn as a function of applied electric field (V/cm) due to Kerr effect. Reproduced from Soref and Bennet[12]. (b) $\Delta\alpha$ as a function of photon energy at applied $\mathbf{E}$ fields 75 kV/cm, 85 kV/cm, and 100 kV/cm, due to the Franz-Keldysh effect. Reproduced from Wendland and Chester[60].

2.2.2 Plasma Dispersion Effect

The only available mechanism to modulate light at high speed in Si is the PDE. This is the phenomenon whereby the n and α change independently as a function of concentration of free carriers (either electrons or holes), according to the following analytic equations

produced by Soref and Bennet[9] (at wavelength 1.55μm):

$$\Delta n = \Delta n_e + \Delta n_h = -[8.8 \times 10^{-22} \times \Delta N_e + 8.5 \times 10^{-18} \times (\Delta N_h)^{0.8}] \tag{2.14}$$

$$\Delta \alpha = \Delta \alpha_e + \Delta \alpha_h = [8.5 \times 10^{-18} \times \Delta N_e + 6.0 \times 10^{-18} \times (\Delta N_h)^{0.8}] \tag{2.15}$$

Where:
Δn_e = refractive index change attributed to change in free electron concentration
Δn_h = refractive index change attributed to change in free hole concentration
$\Delta \alpha_e$ = absorption coefficient change attributed to change in free electron concentration
$\Delta \alpha_h$ = absorption coefficient change attributed to change in free hole concentration
ΔN_e = change in free electron concentration
ΔN_h = change in free hole concentration

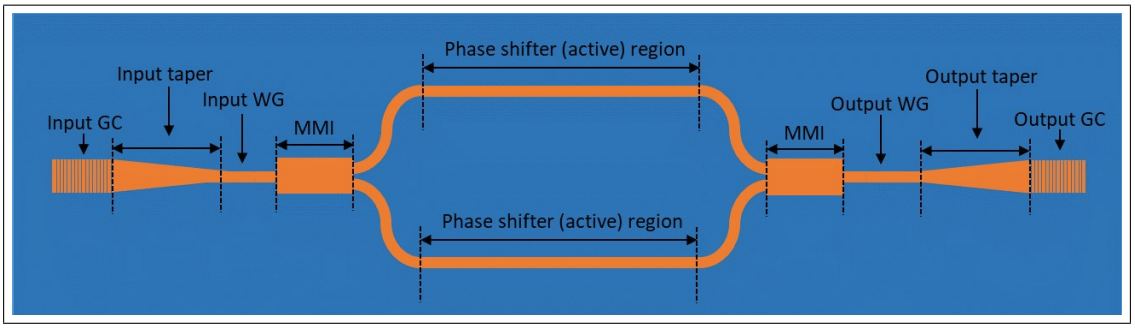


FIGURE 2.3: Typical MZI modulator design

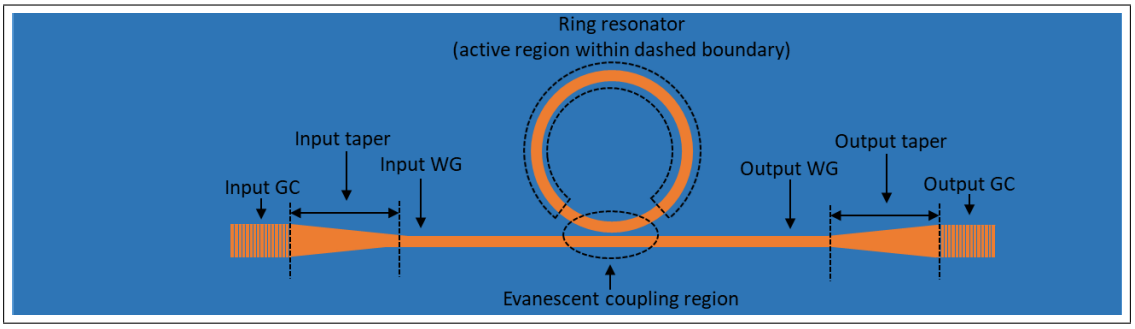


FIGURE 2.4: Typical ring resonator modulator design

Using equation 2.14 we can determine that carrier density change of 5×10^{17} cm^{-3} results in a $\Delta n = 1.66 \times 10^{-3}$. This can be used in certain architectures to realise a significant output intensity change. In a typical MZI design (Figure 2.3), light is coupled from the input fibre into a waveguide and split into two parallel waveguides that make up the phase shifter section of the device. If Δn is induced in one waveguide and not the other, the group velocity of the light propagating in that waveguide is decreased. If Δn and phase shifter arm length (L_{shifter}) are sufficient, when the two waves are recombined they will destructively interfere and the output intensity will be 0 (in an ideal case). The V $\cdot$ cm required to induce π phase shift ($V_\pi L$) (V·cm) of a device is a critical figure of

merit for MZI devices that defines the V·cm required to achieve one full π phase shift, for maximum destructive interference. In typical resonant ring/disk modulators (2.4) a Δn induced in the waveguide making up the ring/disk changes the resonant frequency of the ring/disk and light from the adjacent waveguide couples evanescently into the resonating ring/disk structure. At requisiteΔn caused by biased induced **E** in the active region, all light couples into the ring/disk and output light intensity at the end of the waveguide decreases to 0.

2.2.3 Injection, Depletion and Accumulation Plasma Dispersion Effect Modulation

Three different PDE operating mechanisms can be used to modulate free carrier dispersion in the waveguide section of a device. These are carrier accumulation, depletion or carrier injection (Figure 2.5). In a carrier accumulation semiconductor-insulator-semiconductor capacitor (SISCap) device[34], a gate dielectric layer (usually SiO_2) is sandwiched between lightly doped Si strips that make up the waveguide. When a bias V is applied across the capacitor, free carriers of opposite charge accumulate on either side of the dielectric layer, changing their concentration where the mode concentration is highest, inducing Δn. This approach has the potential to achieve the highest switching speed (i.e. high-speed, high data throughput) because it is not limited by high free carrier lifetime (t_{carrier}), before recombination, associated with the other mechanisms. However, there are a few fabrication challenges associated with this design such as dielectric-semiconductor interface quality, and the reliance on a-Si or poly-Si for one-half of the waveguide.

Carrier depletion modulators have a waveguide made up of a p-type and n-type regions so that they form a p-n diode, and operate in reverse-bias. When V is applied across the diode, carriers are attracted away from the centre p-n interface region, forming a depletion layer at the centre of the waveguide. In carrier injection modulators the waveguide is formed of three separately doped regions, p-type, intrinsic and n-type, forming a p-i-n diode. When V is applied across the p-i-n diode in forward bias, free carriers are injected from the doped regions into the intrinsic central region. Injection type modulators have lower switching speeds compared to depletion type modulators due to high free carrier lifetime, t_{carrier}, before recombination.

The "figures of merit" that define the performance quality of optoelectronic modulators are the following:

- Modulation 3dB bandwidth (f_{3dB})
  The frequency over which transmission is at least 50% of maximum transmission value. Resonant structure modulators (ring/disk) are “narrowband” devices with much lower bandwidths available for modulation (on the order of 100s pm[61]).

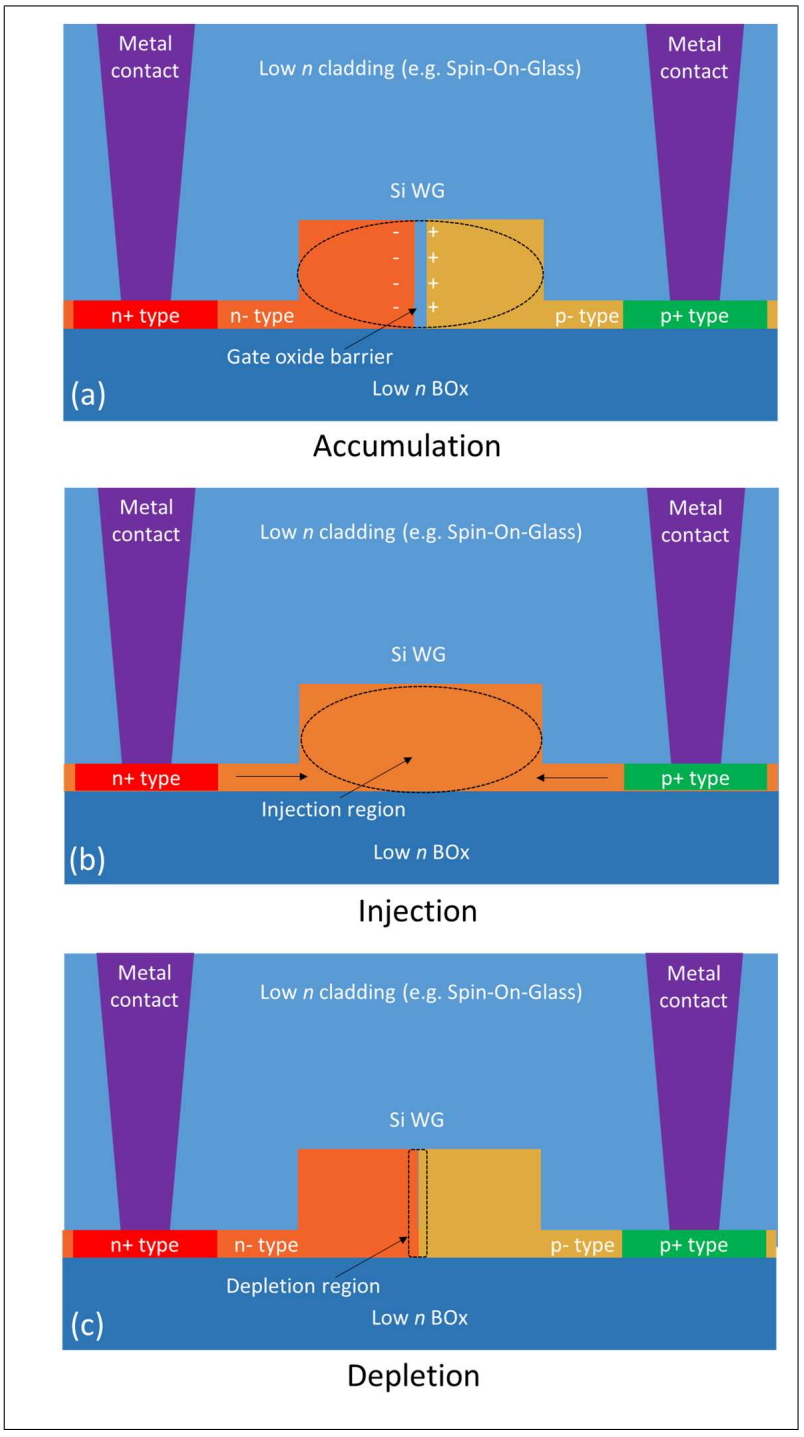


FIGURE 2.5: Schematic of (a) accumulation based PDE Si strip modulator with horizontal gate oxide barrier, (b) injection based PDE Si strip modulator and (c) depletion based PDE Si strip modulator.

Narrowband devices also suffer from very low fabrication tolerance (e.g. resonant wavelength of a ring/disk can change by as much as 0.25nm, double modulation bandwidth, for a 1nm increase in ring width[62]), and have higher temperature sensitivity than MZI devices[63,64]. MZI devices have much larger available bandwidths (10s of nm's) and are said to be "wideband" devices.

- Modulation depth
  Ratio of maximum transmission intensity (I_{max}) to modulated minimum transmission intensity (I_{min}) in dB. The required modulation depth depends on the intended application, 4-5dB is often sufficient[11], however, if minimizing device footprint and power consumption are a priority, a lower modulation depth may be tolerable.

- Modulation speed
  Speed at which light can be reliably modulated. Under high-speed operation the output "eye diagram" must remain open for reliable modulation.

- Optical loss
  "Passive" and "active" loss as explained in 2.1.2. As waveguide cross-sections have been decreased to reduce device footprint and increase light-matter interaction[65], increase speed and decrease power consumption, passive optical loss has increased.

- Device footprint
  Reducing device footprint increases device density and decreases cost per device, however, this is often at the expense of other performance metrics, such as a significantly reduced bandwidth and high thermal sensitivity (with incumbent additional power required to maintain device temperature) when comparing small device footprint resonator devices to large device footprint MZI devices.

- Power consumption (or power consumption per bit)
  Energy required per modulated bit. Lightwire's accumulation modulator operating at 10Gbit s-1 has an energy consumption of 5pJ bit[7,11].

2.2.4 Review of Injection, Depletion and Accumulation Modulator Devices in Literature

The three modulation mechanisms (injection, depletion and accumulation) and the two device architectures (MZI and ring resonator) each have pros and cons. This subsection will review the development of these three mechanisms in the literature, highlighting which mechanisms/architectures are suitable for which applications. Injection mechanism modulators are the easiest to fabricate, as the p-type and n-type doped regions are separated by the intrinsic region, so doping layer alignment and controlling the dopant diffusion pattern is less critical than with depletion devices, and the waveguide doesn't need to be built around a precise oxide capacitor layer, as with accumulation devices. The ease of fabrication is exemplified by the fact that injection mechanism switches were the first to be developed from 1987[29] which utilized "x-switch" splitter architecture[29,66], MZI freespace architecture[31], and MZI on-chip architecture[33,67], prior to achieving high-speed modulation in 2004[68] which utilized a microdisk resonator architecture. Since then many medium-speed, high efficiency injection devices have been demonstrated[45,69–75]. Exceptionally low energy consumption per bit has been achieved with injection devices.

Preston, K. et al. demonstrated 86fJ/bit energy consumption at 3Gbit/s operation[73] using a micro-ring resonator architecture, and Debnath, K. et al. demonstrated 1.6fJ/bit energy consumption at 0.5Gbit/s operation[74] using a a cascaded WDM PhC resonator architecture. The majority of injection mechanism modulators demonstrate operational speed $<$ 20Gbit/s, and because of the long minority carrier lifetime (t_{carrier}) in Si they will be restricted to lower operational speeds at $<$2V drive voltage (IC compatible drive voltage). This speed limitation can be circumvented to an extent by utilizing resonant structures[45] but these devices are narrow-bandwidth compared to MZI architecture devices, and require thermal heaters to tune the devices, which increases energy/bit massively, generally offsetting the efficiency of injection mechanism devices.

Depletion mechanism modulators are more challenging to fabricate due to the need to carefully control the placement of the p-type and n-type doped regions and dopant diffusion pattern. The first deletion mechanism modulator was proposed in 2005[76], and realised in 2007[36,37]. Since then many medium/high-speed depletion devices with various designs have been realised[19,39,44,77–83], with some demonstrating operational speeds up to 90Gbit/s[47]. Despite the plethora of medium/high-speed depletion devices demonstrated, they all have corresponding high energy consumption, with most reported devices (and most cited in this paragraph) having $V_\pi L$ $>$2 V·cm, with Zeilbell, M. et al. reporting 3.5V·cm for 40Gbit/s operational speed[84], and Thomson, D. J. et al. reporting 2.8V·cm for 50Gbit/s operational speed[43] as representative examples.

As previously mentioned, the accumulation mechanism modulator was the first to demonstrate $>$ 1Gbit/s[34] and then $>$10Gbit/s[35] performance. It was understood that accumulation mechanism modulators could outperform injection mechanism modulators as they are not limited by long minority carrier lifetimes, but instead are limited by device resistance and capacitance[11], which can be optimized with appropriate fabrication methods. However, despite the recognised potential, accumulation modulator development was slow due to inherent fabrication challenges. As fabrication methods improved, several MZI accumulation modulators with operational speed $>$ 20Gbit/s and $V_\pi L$ $<$ 0.3V·cm have been demonstrated[48–50,52], as well as low energy-per-bit operation micro-disk resonator structures[51]. Accumulation modulator operational speeds are slightly (20Gbit/s) lower than that demonstrated by depletion modulators, but their $V_\pi L$ efficiency is almost an entire order of magnitude that that demonstrated by depletion modulators.

As can be seen, different modulation mechanisms are suitable for different purposes, with injection mechanism modulators suitable for applications where ultra-high speed is not necessary but that require ultra-high efficiency, depletion mechanism modulators suitable for ultra-high-speed applications at lower efficiency, and accumulation mechanism modulators suitable for middle-ground applications that require both high-speed and high-efficiency. The goal of this project is to realise an efficiency (low$V_\pi L$), low optical loss, high bandwidth, high speed modulator for short range OE interconnects. This application area is particularly important because of the growing energy concerns

within the telecommunications/OE of data-centres industry. The most promising mechanism to achieve this middle-ground of high-speed and high-efficiency is the accumulation mechanism.

2.2.5 Plasma Dispersion Effect Accumulation Mach-Zehnder Interferometer Modulators

The first GHz Si OE modulator was based on carrier injection into a p-i-n diode waveguide, demonstrated in 2004 with a speed of 5GHz[85]. The switching speed of this type of device was limited by the long t_{carrier}. In 2004 Intel demonstrated a Si accumulation modulator with an operating speed exceeding 1GHz[34] (1Gbit/s pseudo-random bit sequence (PRBS) successfully modulated). This was improved in 2009 when Lightwire demonstrated an accumulation modulator with 10Gbits^{-}1 operation, with a modulation depth of 9dB[11]. In 2013 Cisco demonstrated another MOScap accumulation Si modulator with 28Gbits^{-}1 and 9dB modulation depth (40Gbits^{-}1 for 8dB modulation depth)[48]. The goal of this thesis is to modify and improve upon this design.

The electrical circuit electrical circuit relaxation time (t_{relax}=RC) is the switching speed limiting factor in depletion/accumulation devices[76], as opposed to the t_{carrier} limiting factor for carrier injection devices[86]. Reverse-bias, p-n diode, depletion modulators with $t \ll t_{\text{carrier}}$ were easier to fabricate than accumulation modulators in the past and therefore Si modulator research initially focussed on these devices[87]. However, the junction capacitance ($C_{junction}$) (the capacitance arising from the charge variation in the depletion region) and the resistance (R) of depletion modulators are both functions of doping concentration (N) of the p- and n- doped regions according to the following relationships:

$$R \propto N^{-1} \tag{2.16}$$

$$C_{junction} \propto N^{\frac{1}{2}} \tag{2.17}$$

In accumulation modulators total capacitance (C) is independent of N and is determined exclusively by relative electric permittivity of dielectric (ϵ_r) of the dielectric material, and the oxide thickness (t_{ox}) of the capacitor (equation2.18). As C is independent of doping, it allows for the design of either low-voltage (high-C) or high speed (low C) modulators depending on the application.

$$C = \epsilon_r \epsilon_0 \frac{A}{t_{ox}} \tag{2.18}$$

Si accumulation modulators with embedded horizontal gate oxides separating a doped poly-Si layer (top) and doped c-Si layer (bottom), have previously been shown to operate with data transmission speed of 10Gb^{-}1[35]. However, light propagating through poly-Si is subject to high scattering loss from the many poly-Si grain boundaries as previously described. This design of poly-Si/dielectric/c-Si accumulation modulator is shown in Figure 2.6.

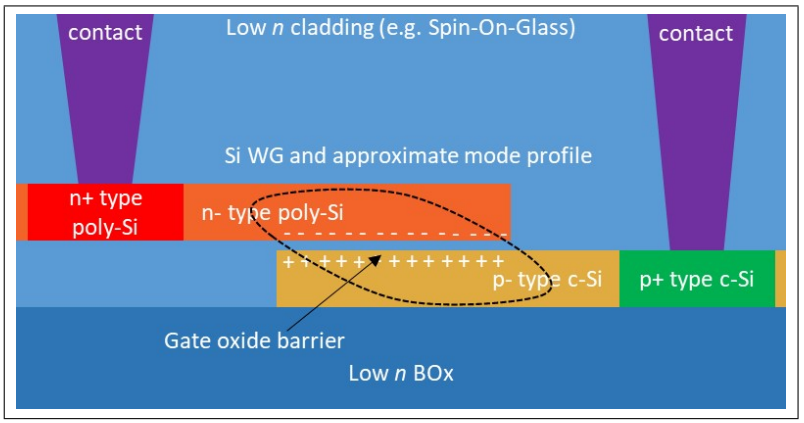


FIGURE 2.6: Schematic of horizontal poly-Si/dielectric/c-Si SISCap accumulation modulator.

Sodagar, M. et al[51] demonstrated a c-Si/SiO_2/c-Si high-quality factor (Q-factor) microdisk resonator modulator on a bonded double-SOI (2.7) with a 10GHz bandwidth and 15 $Gbit^{-1}$ operating speed. The Sodagar, M. et al.[51] device is comprised of a microdisk optical resonator (radius=3um), placed 150nm away from the waveguide width (W_{wg})= 450nm wide access waveguide (for evanescent coupling with the access waveguide). Both top and bottom Si layers were connected to metallic contacts (1.5μm from the WGM located in the microdisk to minimize propagation loss from metallization). The SiO_2 capacitor extends across the microdisk, and upon the application of positive bias, V, causes an accumulation of oppositely charged carriers ($\Delta N_{h,e}$) on the top and bottom Si layer. Accumulated charge at the centre of the capacitor has negligible effect on the fundamental TE mode confined mostly to the edge of the microdisk. The C is made up of the C_m, where the mode is confined, and the C_p, at the centre of the microdisk where there is virtually no mode present.

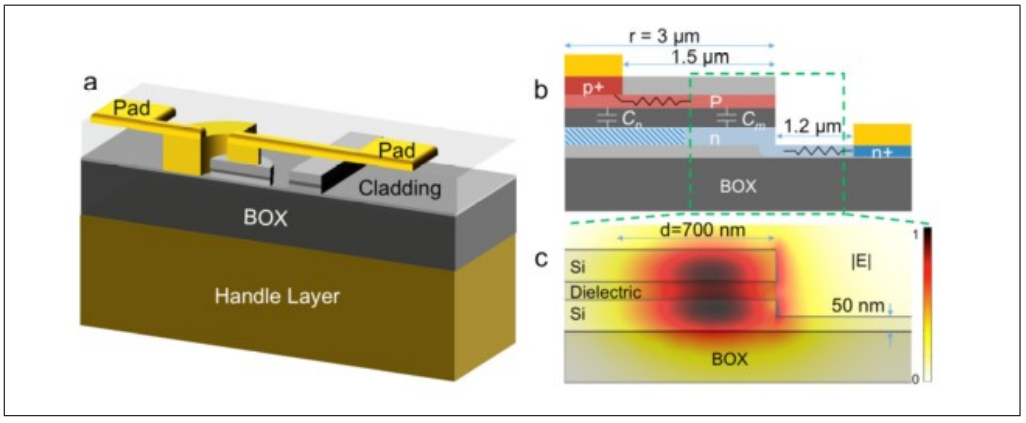


FIGURE 2.7: (a) Schematic of c-Si/70nm SiO_2/c-Si accumulation-based microdisk resonator modulator. (b) Cross section of microdisk resonator section of the device, indicating C_m, where the optical mode is designed to propagate, as well as C_p, in the central region of the disk. (c) Mode profile of the ring resonator. (a), (b) and (c) taken from Sodagar, M. et al.[51]

change in free electron concentration (ΔN_e) and change in free hole concentration (ΔN_h)

in the region of mode confinement induces Δn in accordance with the PDE, which changes the optical path length in the microdisk and therefore changes the evanescent coupling efficiency between the input waveguide and the microdisk.

The Sodagar, M et al. device was fabricate on a directly bonded[88,89] double-SOI. The double-SOI fabrication process (outlined in Moradinejad. H et al.[90]) is as follows (schematically presented in Figure 2.8):

1. 35nm thermal oxide grown on thinned down undoped SOI (3μm BOx)
2. SOIs cleaned using acetone (ACE), methanol, isopropanol (IPA) and an industry standard cleaning process to remove organic contaminants, remove the native oxide, and remove ionic contamination (developed by the Radio Corporation of America and commonly known as an RCA clean). This cleaning was performed to minimize surface contaminations as any particles of any size can reduce bonding quality through void formation or weak adhesion.
3. Activation step of application of O_2 plasma from reactive ion etching (RIE) followed by submersion in ammonium hydroxide (NH_4OH) (to increase the surface hydrophilicity).
4. Following bonding, the handle layer and BOx of the top wafer was thinned down using a combination of dry and wet etching.

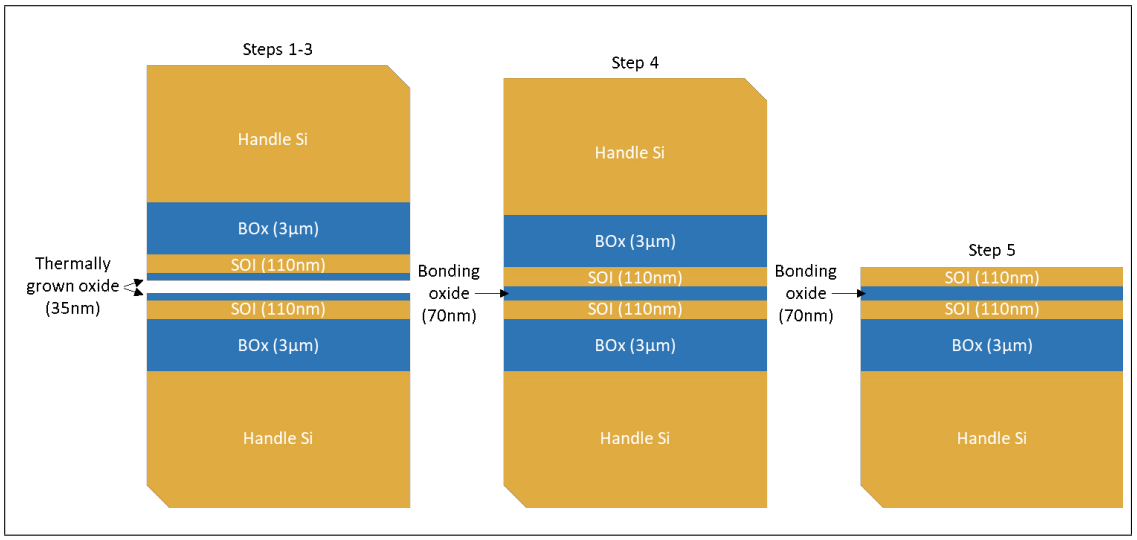


FIGURE 2.8: Direct wafer bonding and thinning down process. Steps 1-3 — Thermal oxidation, SOI cleaning and pre-bonding activation. Step 4 — Direct bonding and annealing. Step 5 — Top handle and BOx removal to realise double-SOI structure

The optical devices were patterned on double-SOI using e-beam and dry etching using inductively coupled plasma (ICP) and RIE. An oxide layer was then deposited on the sample via atomic layer deposition (ALD) to prevent ion tail channelling. Several ion

implantation steps were implemented to realise the p-/p+/n-/n+ doped areas required for the active device. The sample was then annealed using rapid temperature annealing (RTA) to electrically activate the implanted ion dopants, then coated with oxide using plasma enhanced chemical vapour deposition (PECVD). Vertical channels were ICP etched through the deposited oxide above highly doped regions, allowing subsequently deposited Ti/Cu metal to contact the substrate. These vertical channels which allow vertical electrical connection through insulating oxide are referred to, by convention, as "via's".

A continuous-wave (CW) laser source was coupled into the input waveguide using cleaved single mode fibres (SMFs). The coupling and access waveguide total loss was measured to be 20dB at wavelength 1560nm. The light source was then polarization controlled and the wavelength swept from 1550nm to 1570nm. Figure 2.9 (a) (taken from Sodagar. M.[51]) shows the normalized transmission spectrum for various applied direct current voltage (V_{dc})). At V_{dc}) = 0, the resonance feature (f_{3dB}) ∼0.45nm (Q-factor ∼ 3500). As V_{dc} is swept from 0V – +20V the resonance wavelength is blue shifted ∼340pm due to Δn in Si[12] caused by the accumulated free carriers in the area where the mode is concentrated. At the same time, FCA increases microdisk loss, decreasing the Q-factor.

Figure 2.9 (b) (taken from Sodagar. M. et al.) shows the measured resonance wavelength shift for positive and negative polarizations as function of the absolute value of V_{dc}, both of which follow the same trend of increased blue shift with increased V_{dc}. However, the blue shift associated with the negative polarization is smaller because in this case the Si layers must first be depleted of oppositely charged carriers because of their initial doping. This phenomenon is common in the inversion condition of a regular MOScap[91]. When $V_{dc} > 12$V, resonance wavelength shifts at a rate of ∼25 pm/V, in accordance with theoretical predictions. At $V_{dc} < 12$V, resonance wavelength shift rate is lower than predicted, due to non-zero flat band voltage caused by fabrication errors such as charge traps.

A data transfer rate of 15 Gb/s was achieved by studying the response to PRBS at 15 Gb/s at peak V = 4V. The authors claim that the "eye-diagram" produced implies a data transfer rate of up to 30 Gb/s is achievable with this device and that with proper optimization (of doping profile, microdisk Q-factor etc.), the authors predict a data-switching rate of 60 Gb/s is achievable. This is a very high switching speed considering the compactness of the device. However, compactness comes at the cost of increased fabrication intolerances and massively reduced bandwidth. The fabrication process for realising this double-SOI horizontal-slot accumulation modulator can be taken in part and adapted to fabricate an MZI on a double-SOI structure.

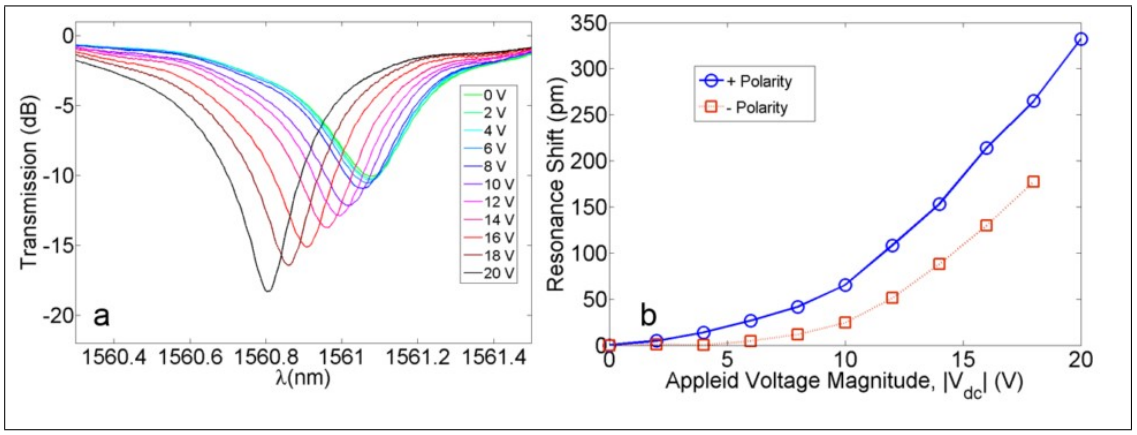


FIGURE 2.9: (a) Normalized transmission spectrum of microdisk resonator modulator at various applied V_{dc}. (b) Resonance shift as a function of applied V_{dc} for positive and negative polarities. Both figures from Sodagar. M.

2.3 Fabrication

2.3.1 Direct Bonding

Liang, D. et al[92] outlined a process for low-temperature SiO_2/SiO_2 covenant bonding to bond III-V semiconductors to SOI, a process that can easily be modified to bond SOI-SOI to create double-SOI. A bonding oxide layer of 60nm was achieved, although there is no reason to expect a <10nm bonding oxide cannot be achieved. After SiO_2 is thermally grown, the process involves O_2 plasma treatment by RIE and application of dilute hydrofluoric acid (HF) activation steps to form a "porous fluorinated network"[93], enhancing low-temperature bonding. After this step, the wafers are baked on a hotplate (whilst simultaneously applying NH_4OH vapour), then bonded under 1.5MPa pressure, and annealed at 300C for 2-12 hours. This step could be followed by a high temperature annealing step (i.e. over 800C for high-temperature bonding, where the inter-facial oxide becomes viscous, increasing the contact area enhancing diffusion of hydrogen trapped at the interface, reducing inter-facial voids[88]), but that was not the purpose of this particular study.

The bonding quality was tested via the "crack-opening method"[89]. Equation 2.19[89,94] shows the relationship between the geometry of a crack propagating through a cleaved bonded wafer and the specific surface energy (υ) at the interface between the two bonded wafers:

$$\upsilon = \frac{3E{t_w}^3 y^2}{8L^4} \tag{2.19}$$

Where:

υ = specific surface energy(ergs/cm^2)

y = wafer crack separation distance/2 (thickness of inserted blade (cm))

L = wafer crack length (length between blade edge and first interference fringe from

blade (cm))
t_w = wafer thickness (cm)
E_{mod} = electric field (material specific, $E = 1.66 \times 10^{12} dyn/cm^{cm}$ for <100> Si)

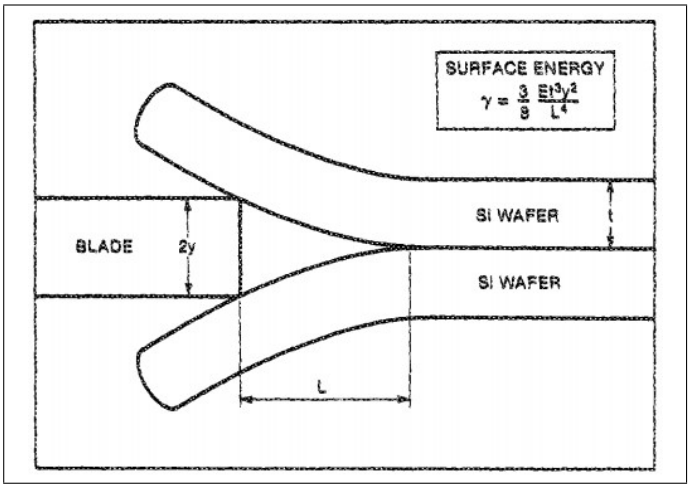


FIGURE 2.10: Schematic of crack opening method[89]

A crack is made with a blade at the edge of the wafer and interference fringes parallel to the blade edge can be observed using transmission IR radiation. This technique can also be used to observe individual voids larger than $\sim 1\mu$m, as they cause breaks in the regular pattern of the interference fringes.

This technique was used by Liang. D et al.[92] to determine a surface energy of 2.63 J/m^2 (averaged from several samples of 1cm^2 chips cleaved from the same double bonded wafer), for wafers bonded at 300C for 2 hours, falling to between 2.23 J/m^2 – 2.44 J/m^2 following 12 hours annealing. 2.11[92] shows the relationship between annealing time and υ (after saturating at ~2.5-3 hours υ fluctuates but shows no correlation with increased annealing time) as well as an infra-red transmission image of a 1cm^2 chip cleaved from a bonded double-bulk Si wafer (with combined 60nm PECVD deposited oxide bonding layer), showing 0 visible voids.

Voids can form for a few primary reasons. Firstly, any pre-bonding contamination particles are points where the two wafers will not contact, therefore pristine conditions must be maintained pre-bonding. Despite this, voids are inevitable around the edges of the wafer where it has been handled with tweezers. Secondly, trapped inter-facial gas or gasses produced as by-products of the bonding reaction that cannot diffuse away from the interface during annealing can cause voids[88,95].These particularly lead to high internal pressure, which can lead to the bonded wafer cracking when annealed at high temperature, or lead to micro-scale voids in less extreme cases. O_2 plasma treatment via RIE was shown to reduce such voids. Figure 2.11 (from Liang, D. et al.[92]) shows two bonded samples, (a) underwent no O_2 treatment and has a void density of 138 cm^{-2}, (b) underwent O_2 plasma treatment and has a void density of 2 cm^{-2}. This void density reduction is thought to be due to a reduction in surface defects (not reduction in

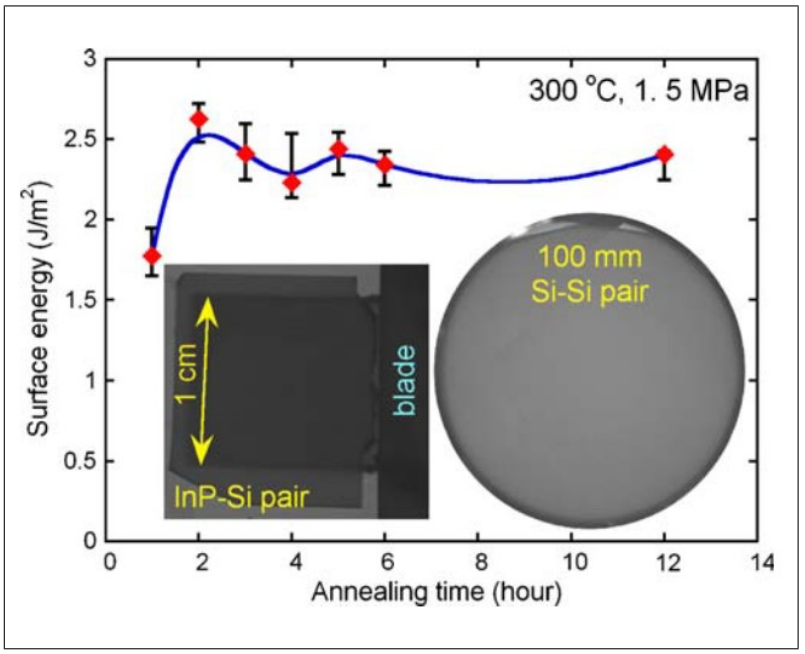


FIGURE 2.11: Surface energy of bonded Si/Si wafer as function of annealing time at 300C. Left inset: InP/SOI bonded chips. Right inset: Si/Si bonded wafer annealed for 2 hours, imaged using infrared transmission, showing 0 voids. Taken from Liang. D et al.[92]

contaminations). O_2 plasma grows a <5nm layer of SiO_2 with a higher strain compared to thermally grown SiO_2[96], and deforms the structure of the thermally grown SiO_2. This surface is also more hydrophilic, which leads to a higher density of Si-OH bonds after contact with dilute HF. O_2 plasma also breaks Si-O bonds, decreasing the surface stability[97] increasing Si-O to Si-fluoride (F) and Si-amino group (NH_2) reactions in the subsequent HF activation step. It also reduces the amount of bonding by-product H_2O, which vaporizes upon annealing and can lead to trapped gas causing cracks as well as voids. These processes and problems must be taken into account when developing a bonding process.

Ljungber K. et al.[98] were the first to develop the method of dilute buffered HF (sulfuric acid (H_2SO_4):H_2O_2:HF) cleaning and H_2O rinsing prior to bonding, which improves initial van der Waals low-temperature bonding. Buffered HF increases surface hydrophobicity and passivates the surface with Si-F dangling bands, which are then replaced with Si-OH bonds when rinsed in H_2O. The Si-OH bonds are unstable and bond easily to other Si-OH bonds. This method can be used to bond SiO_2-SiO_2 surfaces, as well as Si-Si surfaces. The authors also showed that surface energy (i.e. bonding strength) increases with annealing temperature from 350C (where the low-temperature bonding regime ends) to at least 600C for wafers treated with buffered HF prior to bonding.

A patent for an "Optical modulator utilizing wafer bonding technology"[99] was published in 2011 (Figure 2.12), which describes the fabrication of a bonded double-SOI and subsequent splitting step (instead of top handle Si dry/wet etching) using an injected implant

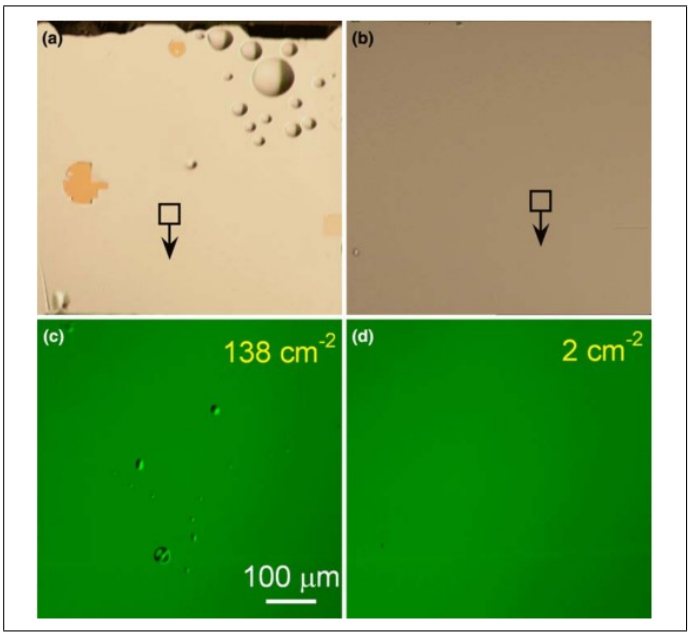


FIGURE 2.12: Two separate, bonded samples. (a) without O_2 plasma treatment ((c) 100x magnification showing 138 cm^{-2} void density), (b) with O_2 plasma treatment ((d) 100x magnification showing 2cm^{-2} void density). From Liang, D. et al.[92]

layer to weaken the bonded wafer in the appropriate place, and subsequent modulator fabrication.

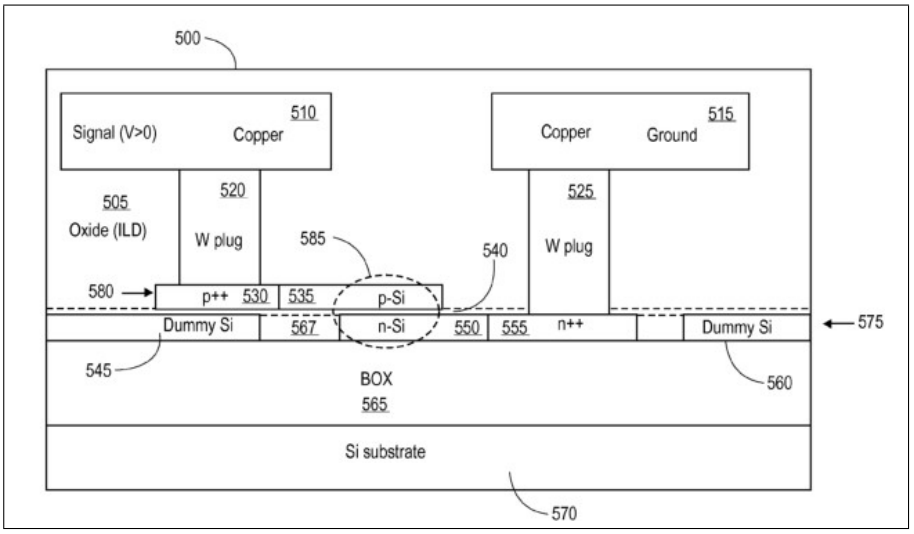


FIGURE 2.13: Schematic of patented optical modulator. Light propagates though the central waveguide highlighted by the dashed oval in the middle. Reproduced from patent[99]

The optical loss in undoped poly-Si waveguides is approximately 9dB/cm[100,101], which increases when doped. For high-speed EO modulator operation (i.e. >25 Gb/s) high doping is required, which in poly-Si would lead to unacceptable optical loss. Therefore, the only way to achieve high-speed EO modulation in a MOScap device is to us double-c-Si, which can be most feasibly achieved using the bonding methods described.

2.3.2 Tetramethylammonium Hydroxide Etching

The high refractive index difference ($\Delta n = 2.0$) at the Si/SiO_2 interface allows high optical confinement but is also a major source of loss, as scattering loss from the sidewall's of the waveguide is proportional to Δn^2 [57]. As such, it is important to smoothen the sidewall's as much as possible. Strip and slot waveguides are conventionally etched after e-beam lithography by dry etching (i.e. RIE or ICP etc.), but this causes significant sidewall roughness. This sidewall roughness after dry etching can be reduced by two wet etching steps. Firstly, the structure can be oxidised to grow a thin oxide layer on the surface of the Si waveguide, and subsequently removed by wet etching with HF. Secondly, the structure can be anisotropically etched using tetramethylammonium hydroxide (TMAH) (which etches the Si <111> crystal plane at ∼2% the speed at which it etches the <100> crystal plane).

The anisotropic etching of Si by TMAH (chemical formula: $(CH_3)_4NOH$) is a result of the fact that different Si atoms in the crystal structure are subject to different removal rates, and etching is determined by site-dependent chemical reaction kinetics. The "etching event" is a complex process involving either a chemical or electrochemical oxidation of surface Si atoms [102], and subsequent etching step, resulting in a free orthosicilic acid ($Si(OH)_4$) product. The surface Si atoms on the <100> plane are bonded to only two additional Si atoms, whereas Si atoms on the <111> plane are bonded to three additional Si atoms [103]. The activation energy barrier required for the sequence of "etching event" chemical reactions to take place is higher in the case of the strongly bound <111> plane atoms than the weakly bound <100> plane atoms [104,105], and is consequently less likely to take place. When a Si atom is etched from the <111> plane, a pit forms surrounded by three less strongly bound Si atoms. These Si atoms have a higher etch probability than <111> plane surface atoms and are therefore etched faster. As they are removed, more weakly bound Si atoms are exposed, and rapid etching propagates parallel to the <111> plane. This etching can sweep over the entire <111> plane, creating an atomically smooth layer. <111> plane etching is therefore a combination of rare/slow removal of strongly bound Si atoms (nucleation), and subsequent rapid lateral etch propagation. From a macroscopic perspective, the <111> plane can be modelled as slow-etch rate stopping layer, that creates perfectly atomically smooth planes. The site-dependent reaction-controlled etching of TMAH (and other anisotropic wet etchants) is opposed to diffusion-controlled etching, in which all surface atoms are etched at the same or similar rates, and etching rate is determined by reactant supply and product dispersion.

In 2001, Lee. K et al. [106] demonstrated 0.8 dB/cm optical loss for a TMAH etched 0.5μm wide Si strip-waveguide. Figure 2.14 (taken from Lee. K et al. [106]) shows AFM images for (a) a conventionally dry etched waveguide, (b) a waveguide fabricated using dry etching and oxidation smoothening, and (c) a waveguide using dry etching, oxidation smoothening and TMAH etching. The sidewall's roughness visibly decreases for the oxidation

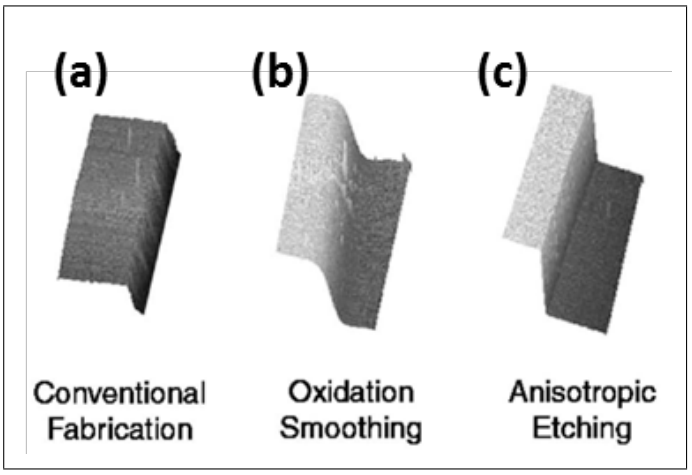


FIGURE 2.14: AFM images of waveguides having undergone different levels of sidewall smoothening. (a) Conventional RIE dry etching only, rms roughness (σ) = 10nm. (b) After dry oxidation and HF wet etching smoothing, σ = 2nm. (c) After TMAH anisotropic etching, <111> plane clearly defined. σ = 2nm.

smoothening sample, and smoothens further after TMAH etching. The transmission loss associated with these three types of devices are >10dB/cm, 1-10dB/cm and <1dB/cm respectively. This is a promising technique for reducing sidewall scattering induced loss, as well as patterning lower layers of a device from above using <111> plane selective etching.

Debnath. K. et al.[54] used a similar method using <110> wafers (crystallographic plane <110> perpendicular to the surface), to fabricate ideally atomically flat sidewall waveguides with sidewalls perpendicular to the BOx substrate, as opposed to trapezoid (54.7deg angle between sidewall and BOx surface due to crystalline structure) waveguides fabricated by Lee. K. et al.[106] which are polarization sensitive and therefore not suitable for use in polarization independent OE modulators. Debnath. K. et al.[54] was able to demonstrate strip-waveguides with 0.85dB/cm loss for TE polarization, and 1.08dB/cm loss for TM polarization at λ = 1550nm, demonstrating polarization insensitivity.

Chapter 3

Design and Methodology

As outlined in 1 and 2.2.4, there is a growing industry need for compact, high efficiency, OE modulators as a solution to the short-medium range telecommunication bottleneck problem. Si photonics PDE modulators are a promising technology to address this need due to their CMOS compatibility and scalability. 2.2.4 presents the historical development of Si PDE OE modulators and demonstrates that although injection and depletion mechanism modulators have advantages in terms of either absolute efficiency (injection) or absolute speed (depletion), accumulation modulators offer the best middle-ground solution of medium-speed, high-efficiency that industry requires. As outlined in 2.2.5, despite the progress in accumulation modulator design and fabrication, there is still no demonstration of a fully-crystalline-Si modulator that does not exhibit intrinsic parasitic capacitance. Sodagar, M. et al[51] demonstrated a fully-crystalline-Si horizontal-slot accumulation modulator on a bonded double-SOI structure, but there was no way to remove the bottom SOI layer independently from the top SOI layer, and the device therefore suffered from parasitic capacitance (decreasing energy efficiency) and limited the modulator to a microdisk design. Wu, X. et al.[48] demonstrated a horizontal-slot accumulation modulator using partially recrystallized poly-Si. This device demonstrated 20Gbit/s and 4.5pJ/bit operation, but this design will always be limited by the fact that the deposited a-Si can not be fully recrystallized, leading to high poly-Si optical loss, higher input power, and therefore higher energy consumption. The two designs presented in this chapter both solve the problem of how to fabricate a fully-crystalline-Si accumulation modulator without intrinsic parasitic capacitance, in two different ways.

The horizontal-slot fin-waveguide accumulation modulator design (3.1) is a unique design that utilizes a bonded double-SOI platform with mirrored top-SOI/bottom-SOI crystal alignment, allowing for the bottom SOI layer to be anisotropically under-etched from above, removing parasitic loss and introducing a new biplanar (vertical-MOScap structure) waveguide design. The vertical-slot rib-waveguide accumulation modulator (3.2) presents a unique planar, vertical-slot (horizontal-MOScap structure) modulator, in which the SiO_2 thickness is defined using LOCOS, and one half of the rib-waveguide

is comprised of fully recrystallized deposited a-Si, using innovative c-Si "seed" windows. This chapter will detail the simulated device performance demonstrating that as well as conceptually innovative designs, these designs have the potential to compete with established accumulation modulator devices. This chapter will also detail the fabrication process flows for both devices, and 3.3 will outline key fabrication techniques used.

3.1 Horizontal-Slot Fin-Waveguide Accumulation Modulator

3.1.1 Design

Figure 3.1 shows the new proposed design for the horizontal-slot, low $V_\pi L$, low-loss, high-speed accumulation OE modulator. The fully c-Si horizontal-slot strip/fin-waveguide is fabricated on bonded double-SOI. A major problem associated with using the double-SOI platform is patterning of the bottom layer separately from the top layer, seeing as the double-SOI wafer should be bonded before any patterning processes take place to ensure excellent Si/SiO_2 interface and SiO_2/SiO_2 bonding interface quality. The solution to this problem is to use anisotropic wet-etching to selectively under and over etch the top and bottom SOIs independently in a single step. This will form a fin-waveguide structure with the multiple-fin grating being used as electrode connections.

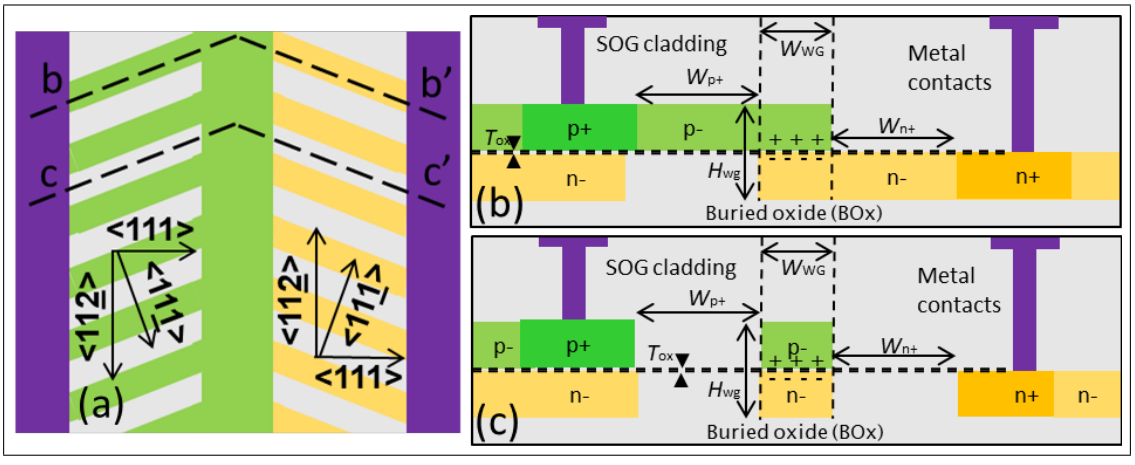


FIGURE 3.1: Design schematics of (a) the top down view of phase-shifter fin-waveguide region. The relevant <111> stable planes are superimposed over the fins of the top SOI and bottom SOI on the left (green) and right (yellow) respectively. (b) Cross-section b-b'. W_{wg} = 350-500nm, H_{wg} = 210nm, t_{ox} = 5-10nm, W_{n-}= W_{p-}=1000nm. (c) Cross-section b-b'.

The bonded double-SOI consists of two <110> 100nm Si SOI wafers, bonded with a 10nm thermally grown gate oxide slot. The orientations of the stable <111> crystallographic planes of the top and bottom wafers are mirrored (Figure 3.1). The sidewalls of the upper fins align perpendicular to the upper SOI <111> direction. The sidewalls of the

lower fins align perpendicular to the lower SOI <111> direction. The fins are therefore at a 20° angle perpendicular to the waveguide. Perpendicular to the substrate, the fin width (W_{fin}) is between 100-200nm and the fin period (Λ_{fin}) is between 250-400nm. Figure 3.1 (b) and (c) shows a schematic of the active phase-shifter section of the MZI device.

3.1.2 Simulation

Finite difference eigenmode simulations were performed[55] to establish the characteristics of the expected TE mode profile in both the horizontal-slot strip and fin-waveguides (Figure 3.2). $|\mathbf{E}|^2$ is concentrated around the central oxide region, the region where free carrier change is expected to be highest in an active MOScap based modulator device utilizing this design. The concentration of $|\mathbf{E}|^2$ around the oxide for this fundamental mode increases the potential Δn in an active device. Also, despite the fact that the mode profile is slightly "tilted" in the fin section as opposed the the strip waveguide section, the $|\mathbf{E}|^2$ concentration is negligible at over 100nm into the fins.

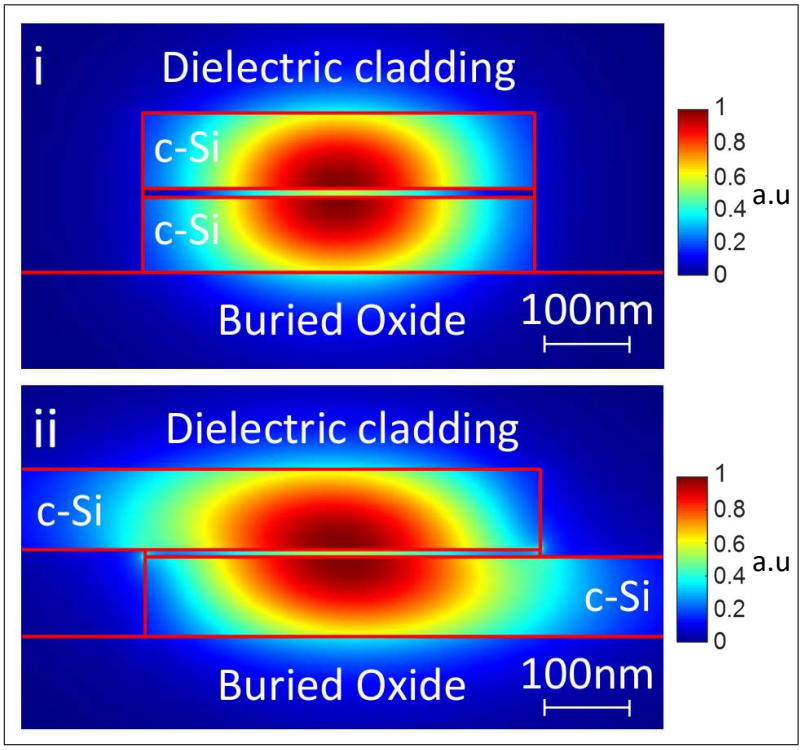


FIGURE 3.2: Simulated normalized energy density (η(r)) of TE optical mode profile of (a) and (b) strip-waveguide at W_{wg} = 500nm in linear scale.

The fins serve the primary function of acting as electrical contacts either side of the oxide barrier, however, due to the fact that their placement is periodic, they can serve the secondary function of acting as a pseudo-1-dimensional (1D) PhC. Four fin-waveguide designs (Table 3.1.2) (varying W_{fin} and Λ_{fin} were studied. According to 3D finite difference time domain (FDTD) simulations (performed using *Lumerical Solutions* FDTD:

3D Electromagnetic Simulator, version 2017a[107]) (Figure 3.4) fin-waveguide design #4 exhibits a clear 42nm wide bandgap between wavelengths 1576nm-1618nm. If desired, this device could be operated at the band-edge in the "slow-light" region (the exponential increase of group index, n_g, at the band edge is indicative of slow light), however, for the purpose of this study, maximizing bandwidth and lower propagation loss are of a higher priority.

3D charge transport simulations (*Lumerical Solutions* CHARGE: 3D Charge Transport Simulator, version 2017a[108]) were performed to estimate $V_\pi L$, f_{3dB} and optical loss as a function of W_{wg} (Figure 3.3) for fin-waveguide MZI modulators with W_{fin} = 160nm, Λ_{fin} = 214nm, as well as non-fin horizontal-slot SISCap MZI modulators for reference. $V_\pi L$ is improved 10% at W_{wg} = 500nm, where optical confinement is strongest. Optical loss is improved by 0.4dB at W_{wg} = 350nm. Figure 3.3 shows that f_{3dB} is decreased by the fin structure. This is due to the increased resistance caused by the fins.

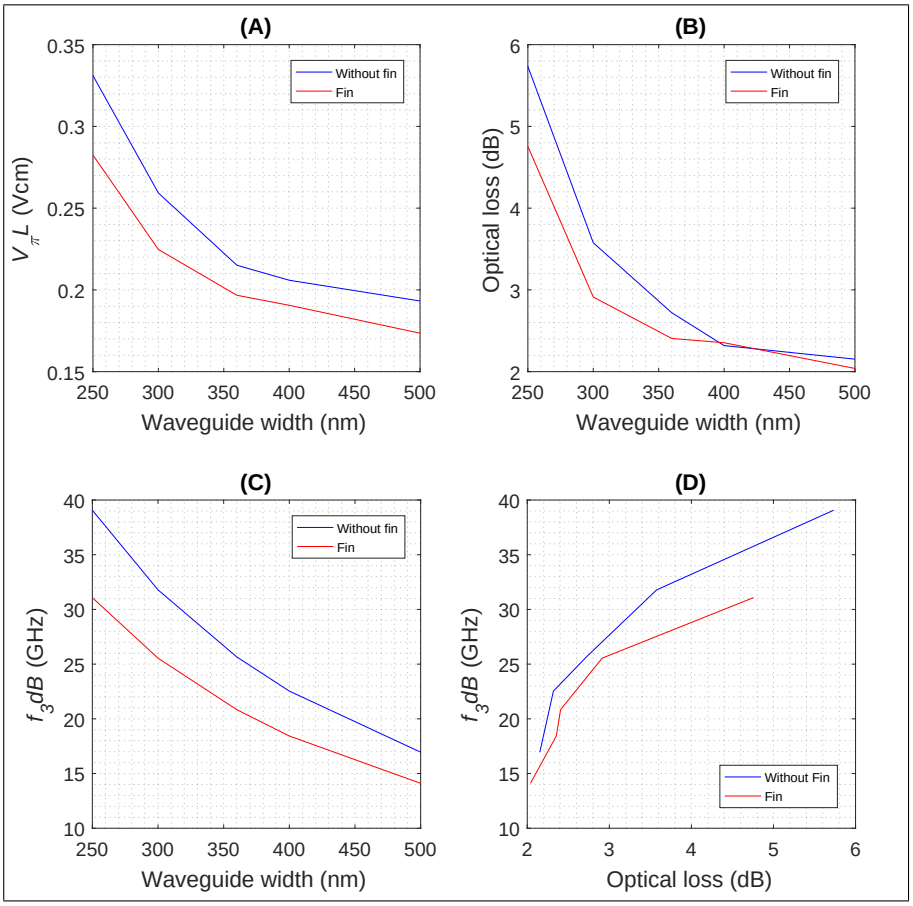


FIGURE 3.3: Simulated performance characteristics of horizontal-slot fin-waveguide accumulation modulator, compared to non-fin waveguide. (A) $V_\pi L$ as a function of W_{wg}. The fin-waveguide device shows a 17.4% improvement in efficiency over the non-fin-waveguide structure at W_{wg} 250nm, and a 11.4% improvement in efficiency at waveguide width 500nm. (B) Optical loss as a function of W_{wg}. (C) f_{3dB} as a function of waveguide width. (D) f_{3dB} as a function of optical loss (dB). Simulations carried out in *Lumerical Solutions* CHARGE[108].

TABLE 3.1: Four different fin designs (with different W_{fin} and Λ_{fin})

Design #	Fin width (nm)	Fin period (nm)
1	100	300
2	125	250
3	150	300
4	200	400

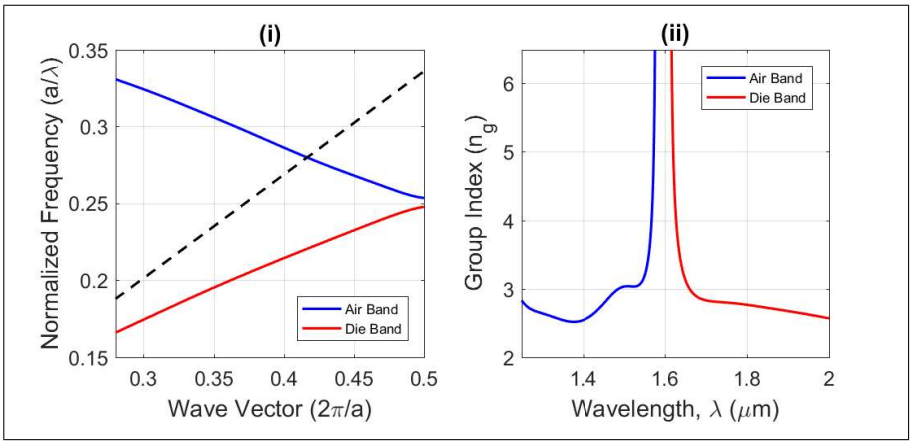


FIGURE 3.4: Dispersion relation (a) and group index of fundamental TE mode for fin-waveguide design#4 (W_{fin} = 200nm, Λ_{fin} = 400nm). The dispersion relation clearly shows a photonic bandgap. 3D simulations carried out in *Lumerical Solutions* FDTD[107].

3.1.3 Fabrication Process Flow

The primary fabrication challenge involved for the realisation of the horizontal-slot fin-waveguide accumulation modulator described above is the problem of how to selectively under-etch one side of the fins and over-etch the other side of the fins. The solution proposed and demonstrated in this thesis is to bond two <110> wafers together, such that that the crystal orientation of the top layer mirrors the crystal orientation of the bottom layer. TMAH anisotropic wet etching therefore effects each layer differently. By patterning the fins such that their sidewalls are aligned normal to the the <111> crystal plane of one layer (and are therefore out of alignment with the normal to the <111> crystal plane of the other layer), the top fins can be under-etched and the bottom fins over-etched simultaneously in a single step, in a "self-aligned" process. This is demonstrated clearly in Figure 3.5 which shows the fabrication process for fin-waveguides from the starting point of a bonded double-SOI substrate.

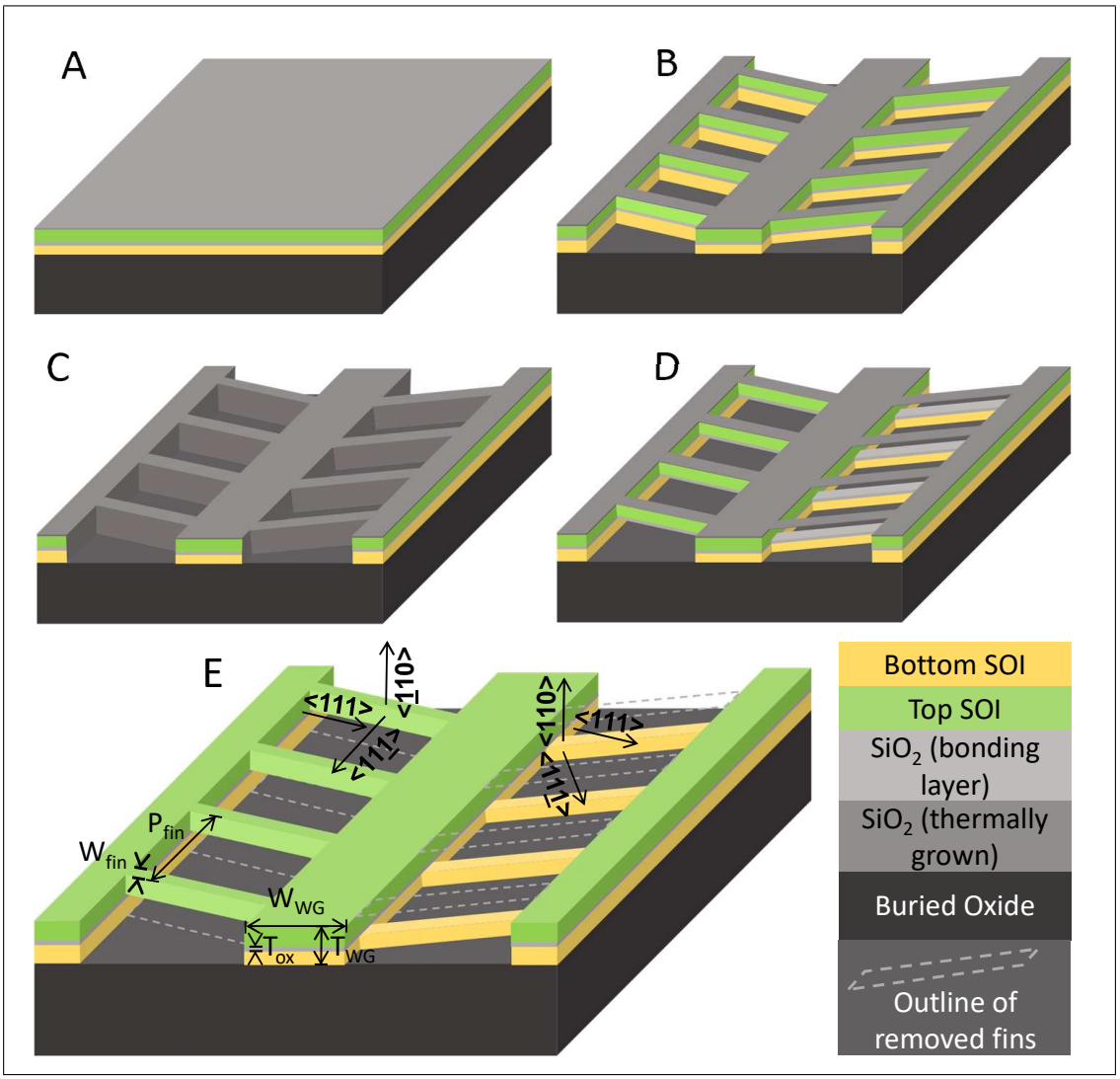


FIGURE 3.5: Fin-waveguide fabrication process flow. (A) Bonded double-SOI platform with 10nm bonding "gate" oxide. 22nm thermal oxide protective layer grown on top. The top and bottom (110) SOI layer have mirrored crystal orientation (shown in (E)). Fin-waveguide patterned using electron beam lithography and dry etched using SF_6 and CHF_3 chemistry ICP. (C) Local oxidation of silicon (LOCOS) process. ~10nm thermal oxide grown on (111) sidewalls to reduce sidewall roughness to an acceptable limit pre-TMAH etching. (D) Sidewall oxide removed using HF and TMAH applied for 105 minutes etching non-stopping Si planes (i.e. non-(111) Si planes). Left-lower fins etched whilst top fins protected by (111) sidewall. Right-upper fins etched whilst bottom fins protected by (111) sidewall. (E) Remaining exposed oxide removed using HF. Dielectric protective layer (PMMA, $n = 1.44$) applied.

3.2 Vertical-Slot Rib-Waveguide Accumulation Modulator

3.2.1 Design

The cross-section of the vertical-slot rib-waveguide and the MZI phase-shifter design are presented schematically in Figure 3.6 and Figure 3.7 respectively.

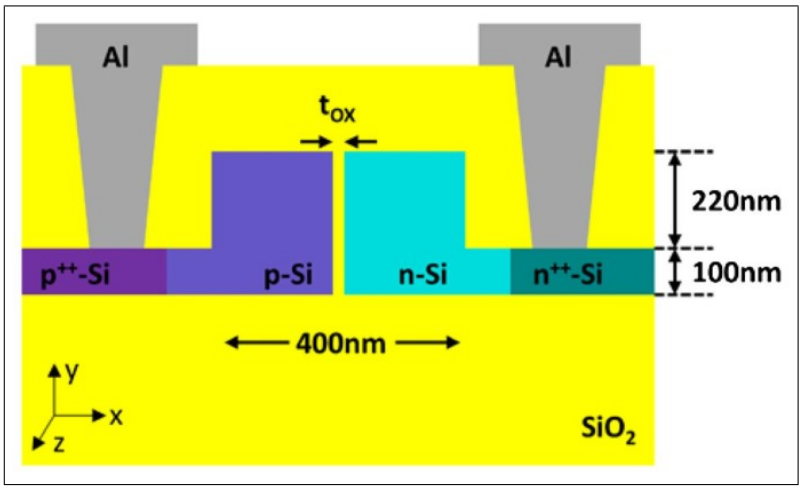


FIGURE 3.6: Vertical-slot waveguide cross-section.

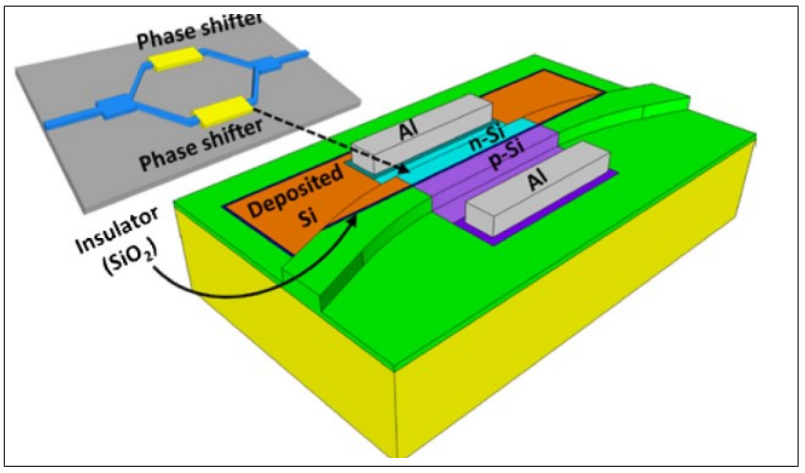


FIGURE 3.7: Active MZI section of vertical-slot rib-waveguide accumulation modulator, 3D schematic.

The vertical-slot rib-waveguide is designed to have a total waveguide thickness of 320nm, with 100nm thick Si contacts either side of the waveguide which act as electrical contacts. These electrical contacts are thin enough such that the fundamental TE mode is confined almost entirely within the central rib section of the waveguide, whilst also being thick enough to provide adequate low-resistance contacts. Both sides of the rib-waveguide are lightly doped (target doping concentration = $1x10^{18}$) with n- or p-, allowing for high-bandwidth performance without inducing intolerable FCA optical loss. The heavily doped (target doping concentration = $1x10^{20}$) n+ and p+ regions, which are required for ohmic contacts to the metal layer, are each 900nm away from the centre of the rib-waveguide. The mode field is negligibly present 900nm from the centre of the rib-waveguide, therefore these highly doped regions do not contribute to significant FCA optical loss. When a bias is applied across the MOScap device, electrons accumulate either side of the oxide barrier.

The MZI utilizes conventional partially-etched input/output grating couplers and MMI

splitters. The waveguide bends (at the end of which the slot is introduced adiabatically from the side) have a radius of 50μm. The length of the phase shifter section of the device is 500μm.

3.2.2 Simulation

Simulations (FDTD[107] and CHARGE[108]) were performed to establish estimates for device C, phase change (δ), propagation loss, device operating speed and operating efficiency. Figure 3.8 (a) shows the simulated distribution of charge carrier concentration under 4V applied bias. This charge carrier concentration change is most significant on the Si side of the SiO_2 interface as expected, which is the location of the highest $|\mathbf{E}|$ concentration (Figure 3.8 (b)). This causes the n of this mode to change in accordance with equation 2.14. The 3D FDTD simulation of the section of the waveguide transitioning from rib-waveguide to rib-slot-waveguide (Figure 3.8 (c)) suggests a coupling loss of ~1dB, which is tolerable considering that the GC loss is expected to be ~4dB per GC.

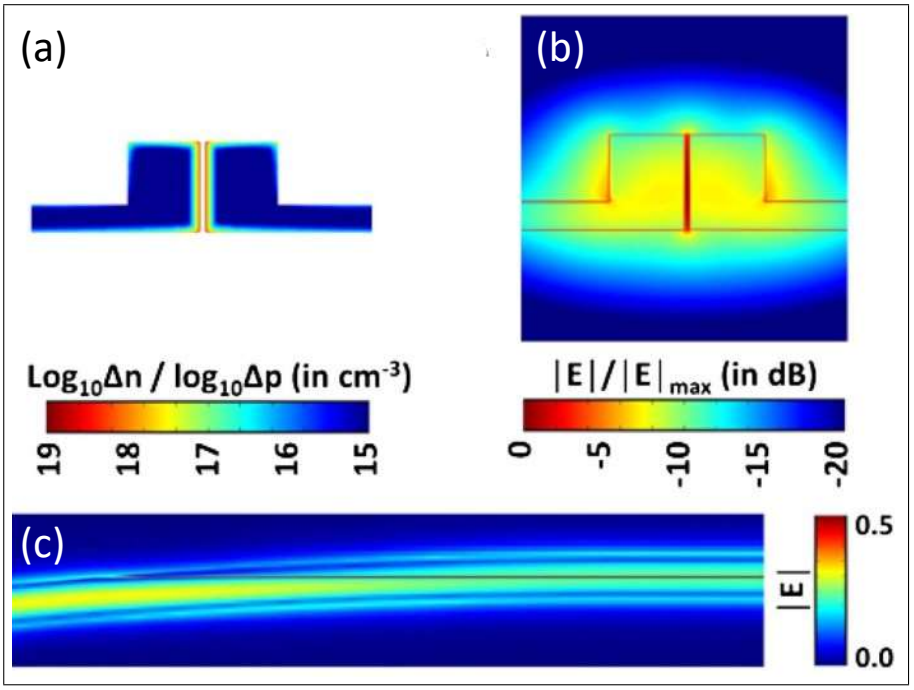


FIGURE 3.8: (a) Cross-section of log carrier concentration (cm^{03}) as a result of 4V applied bias across MOScap device structure. (b) Cross-section showing normalized $|\mathbf{E}|$ of fundamental TE mode. (c) Top-down view showing simulated $|\mathbf{E}|$ in section of the waveguide transitioning from rib-waveguide (left) to rib-slot-waveguide (right).

Given the stated parameters of waveguide width, height, doping concentration and high-concentration doping positioning etc. the most important parameter that effects the performance characteristics of the modulator is the t_{ox}. The device is designed to operate with a positive bias applied to the positively doped side of the waveguide in accumulation mode. As shown in Figure 3.9 (a), as positive bias is applied, capacitance increases

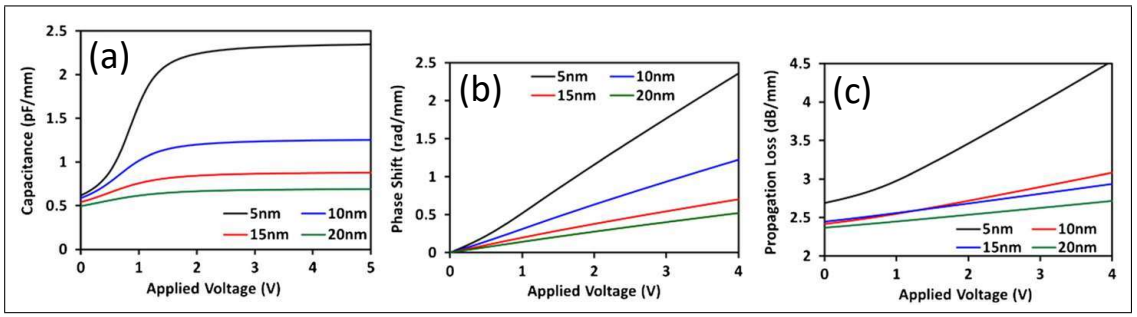


FIGURE 3.9: Vertical-slot rib-waveguide accumulation modulator: (a) capacitance (pF/mm), (b) phase shift (rad/mm) and (c) propagation loss (dB/mm) as a function of applied voltage for gate SiO_2 thickness = 5nm-20nm.

until it reaches a saturation point at the "flat-band voltage". Maximum achievable capacitance increases exponentially as t_{ox} decreases. Increased capacitance for the same applied voltage increases device efficiency, but it also comes at the cost of an increased electrical relaxation time constant, which decreases maximum modulation bandwidth. If operating the device with a voltage swing from 0V—4V, with t_{ox}=5nm, modulation efficiency=0.53Vcm and modulation bandwidth=20GHz. If t_{ox}=20nm, modulation efficiency=2.4Vcm but modulation bandwidth=52GHz. t_{ox}=5nm and t_{ox}=20nm are either end of the high-efficiency/low speed to low-efficiency/high speed spectrum, and a design decision has to be made as to whether to target high-efficiency/low-speed or low-efficiency/high-speed, or to target medium-efficiency/medium-speed. For the purposes of this study it was decided to target medium-efficiency/medium-speed, and therefore a t_{ox}=10nm. With t_{ox}=10nm, simulations indicate that the performance metrics that can be expected are as follows: capacitance=1.25pF/mm, modulation efficiency=1Vcm, maximum modulation bandwidth=32GHz (Figure 3.9).

3.2.3 Fabrication Process Flow

The process flow for the fabrication of the passive vertical-slot rib-waveguides is presented schematically in Figure 3.11 (2D cross-section) and Figure 3.10 (3D model). The most important feature of this device and this fabrication is the vertical-slot oxide. The realisation of this non-planar feature (in the phase-shifter region of the device only) required a slightly non-conventional fabrication technique, which is outlined here (details in 6.1.1). Dry etching a vertical-slot and depositing SiO_2 is possible and practical for slot widths $\gtrsim$ 100nm, but at shorter widths the height/width aspect ratio prevents adequate SiO_2 deposition, resulting in unacceptably large void regions within the slot. High height/width ratio vertical slots are also difficult to etch, and their sidewalls cannot be easily smoothed using LOCOS or TMAH wet etch techniques. Instead the vertical-slot oxide layer must be grown on an exposed Si sidewall. Using this technique, an arbitrary wide "trench" is etched exposing the sidewall that will define the vertical oxide layer

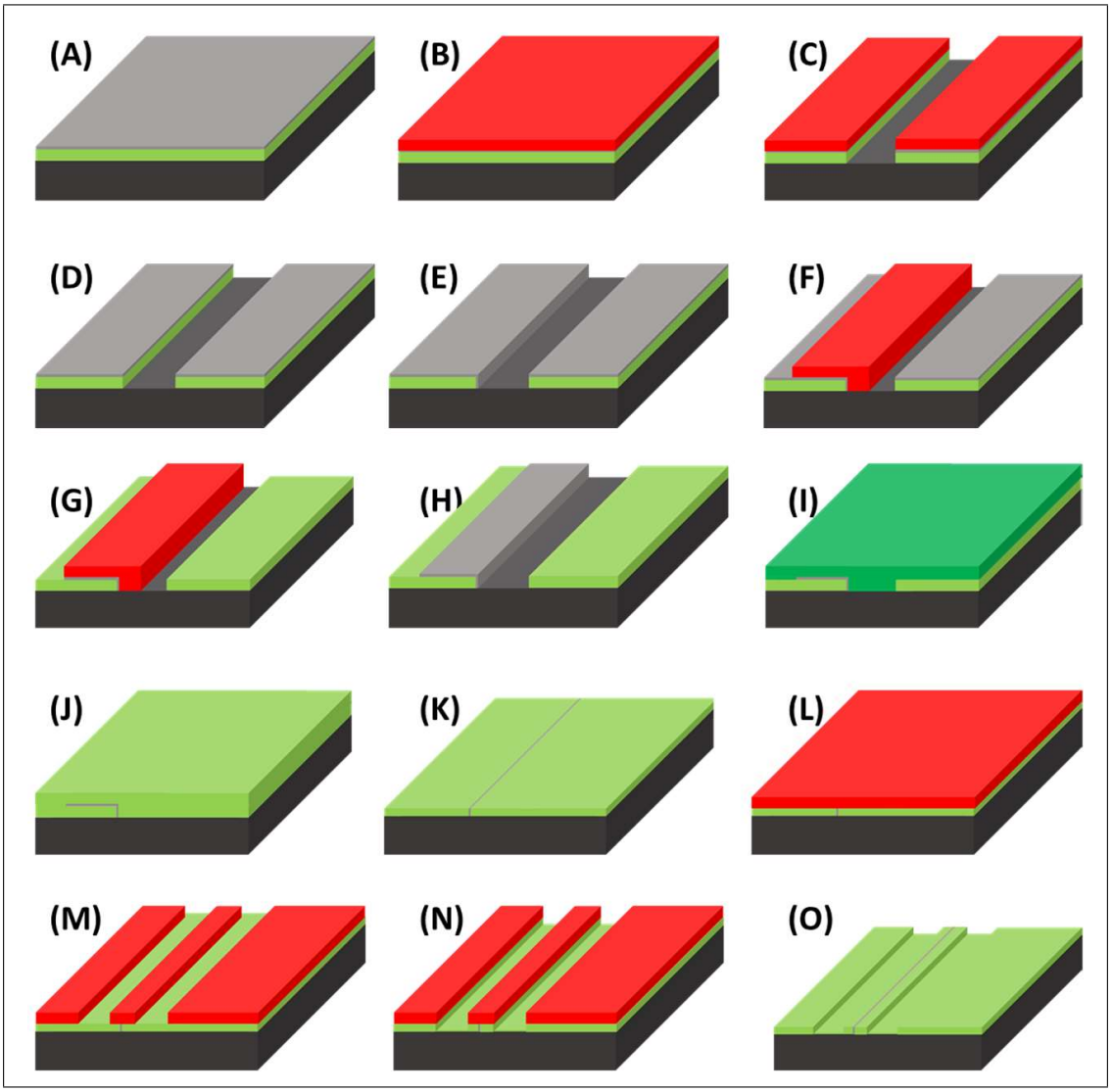


FIGURE 3.10: Fabrication of passive vertical-slot fin-waveguide process flow schematic (3D). Active (doping) steps omitted here but explained in the text for the sake of clarity. (A) (110) 320nm SOI layer with 20nm thermal oxide. (B) Positive electron-beam resist (ZEP520A) applied. (C) Rectangular trenches patterned and dry etched, using the bottom BOx as a stopping layer. (D) Resist removed and TMAH applied to reduce sidewall roughness. (E) Substrate oxidized to grow 10nm on exposed (111) sidewall. (F) Negative electron-beam resist (UVN-30) applied and patterned such that everything except the region around the vertical-slot are exposed. (G) Exposed top-surface and sidewall SiO_2 layer removed using HF. (H) Negative resist removed. (I) a-Si applied using PECVD. (J) Recrystallization of a-Si to c-Si using the a-Si/c-Si contact windows as recrystallization "seed" points. (K) Substrate underwent CMP to recover smooth, planar surface. Top Si layer 320nm thick. (L) Positive electron-beam resist applied. (M) Waveguide and MZI structure patterned. (N) Waveguide and MZI structure defined by ICP dry etching, leaving 100nm thick Si layer connecting outer regions to waveguide for use as electrical contacts.

and centre of the rib-waveguide (Figure 3.10 (D)). The sample is then oxidized, growing the vertical SiO_2 layer (Figure 3.10 (E)). An a-Si layer is then deposited using PECVD

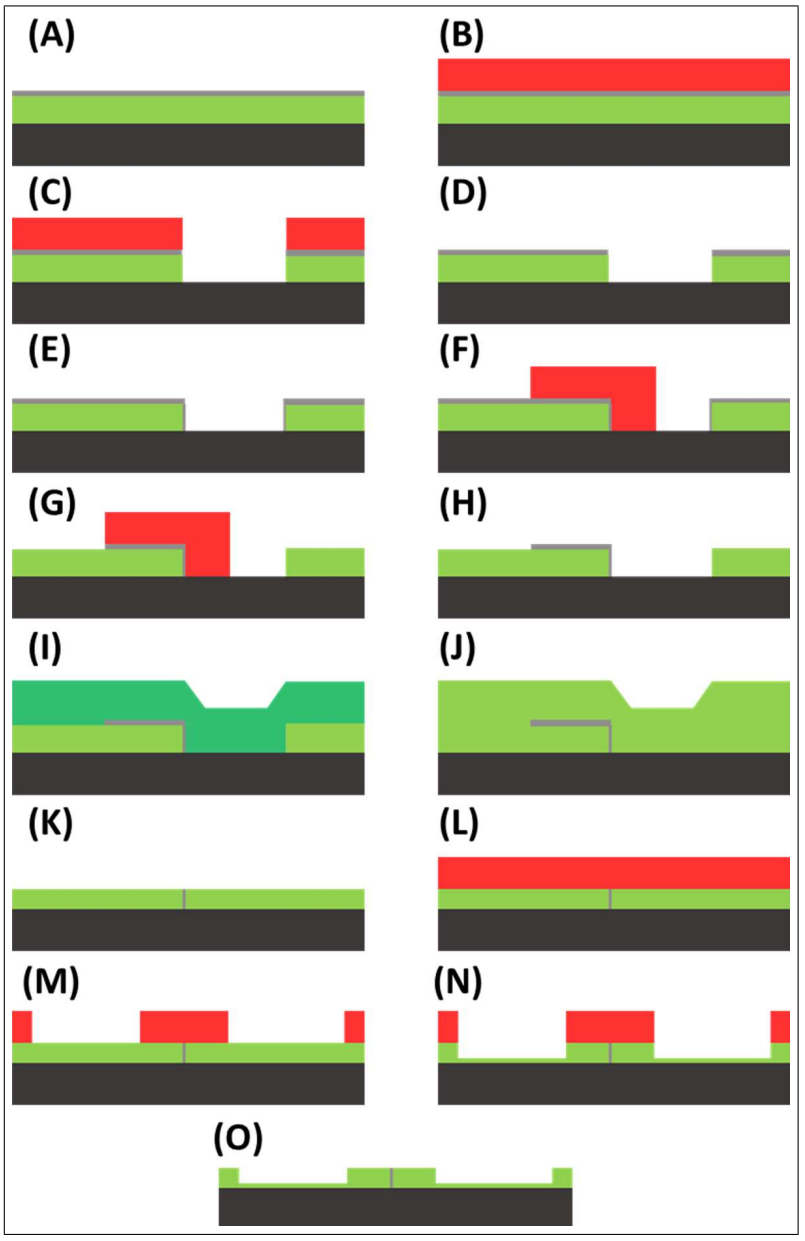


FIGURE 3.11: Fabrication of vertical-slot fin-waveguide process flow schematic (2D cross-section).

(Figure 3.10 (I)), which is then recrystallized at high temperature (using exposed c-Si/a-Si contact points to "seed" crystal growth, Figure 3.10 (J)). The non-planar substrate is than planarized using CMP (Figure 3.10 (K)). The rib-waveguide and total MZI can then be defined using conventional dry etching, doping, metal contact deposition etc.

3.3 Fabrication Techniques

This section will give an overview of the fabrication techniques utilized to realise the above mentioned devices. Some device features (∼100nm GC gratings and ∼100nm wide

fins) were too small to realize using photolithography. For this reason and to increase speed of design iteration, electron-beam lithography was used exclusively for both design. The techniques covered are 3.3.1 electron-beam lithography patterning and development, 3.3.2 inductively coupled plasma dry etching, 3.3.3 plasma enhanced chemical vapour deposition, 3.3.4 chemical mechanical polishing, 3.3.5 SiO_2/SiO_2 bonding and 3.3.6, local oxidation of silicon. TMAH wet etching has been covered extensively in 2.3.2.

3.3.1 Electron-beam Lithography: Pattering and Development

Electron-beam lithography is a process by which a focussed beam of electrons expose an electron sensitive resist, and either increase (negative resist) or decrease (positive resist) the solubility of the resist to the resist developer. The electron beam is focussed and steered using a system of magnetic lenses, and linearly swept across the substrate according to a preset design. This is a time consuming process compared to photolithography, where the entire design can be exposed simultaneously. However, it is required to achieve feature sizes as low as 10nm. The design can also be easily changed programmatically, whereas a photolithography mask must be ordered, custom manufactured and delivered physically for each iteration of the design before it can be used. For these reasons, electron-beam lithography was used in this work.

A 100kV Joel JBX 9300FS Electron Beam Lithography System was used. The electron-beam generation, acceleration and direction system consists of a ZrO/W electron emitter gun, an acceleration electrode, a beam "blanker" (which blocks the electron beam, effectively acting as a beam on/off switch), an aperture and a series of condenser lenses,and finally an aperture and an objective lens. At the focus point, the substrate is placed on a movable stage, the position of which is carefully monitored with an interferometer.Figure 3.12[109] presents a schematic of the electron optics system and electron beam deflection system (B), a representation of the electron beam field (A), and schematic of the entire e-beam system, showing how the substrate is positioned in a wafer holder on a movable stage below the deflection system (C). Figure 3.12(C) includes a flow diagram detailing how the design inputted into the "COMPUTER CONTROL SYSTEM" interacts with the electron-beam lithography system hardware, and is included for completeness.

The beam current and aperture size define the Gaussian width of the beam at the surface of the substrate, and the objective lens directs the beam to write the pattern across the surface. Complex geometrical patterns are broken up into rectangles. The beam is swept as a series of circular spots across each rectangular area to be exposed in a form of a vector scan. The beam is then blanked, redirected, and the next rectangular area is exposed. The required exposure dose ($\mu A{\cdot}s{\cdot}cm^{-2}$) is achieved by varying the time the beam spends at each spot position, and proximity error control (PEC) is used calculate the time required at each spot (as spots at the centre of an exposed area will be subject to additional exposure from scattered electrons from surrounding spots, than from edge

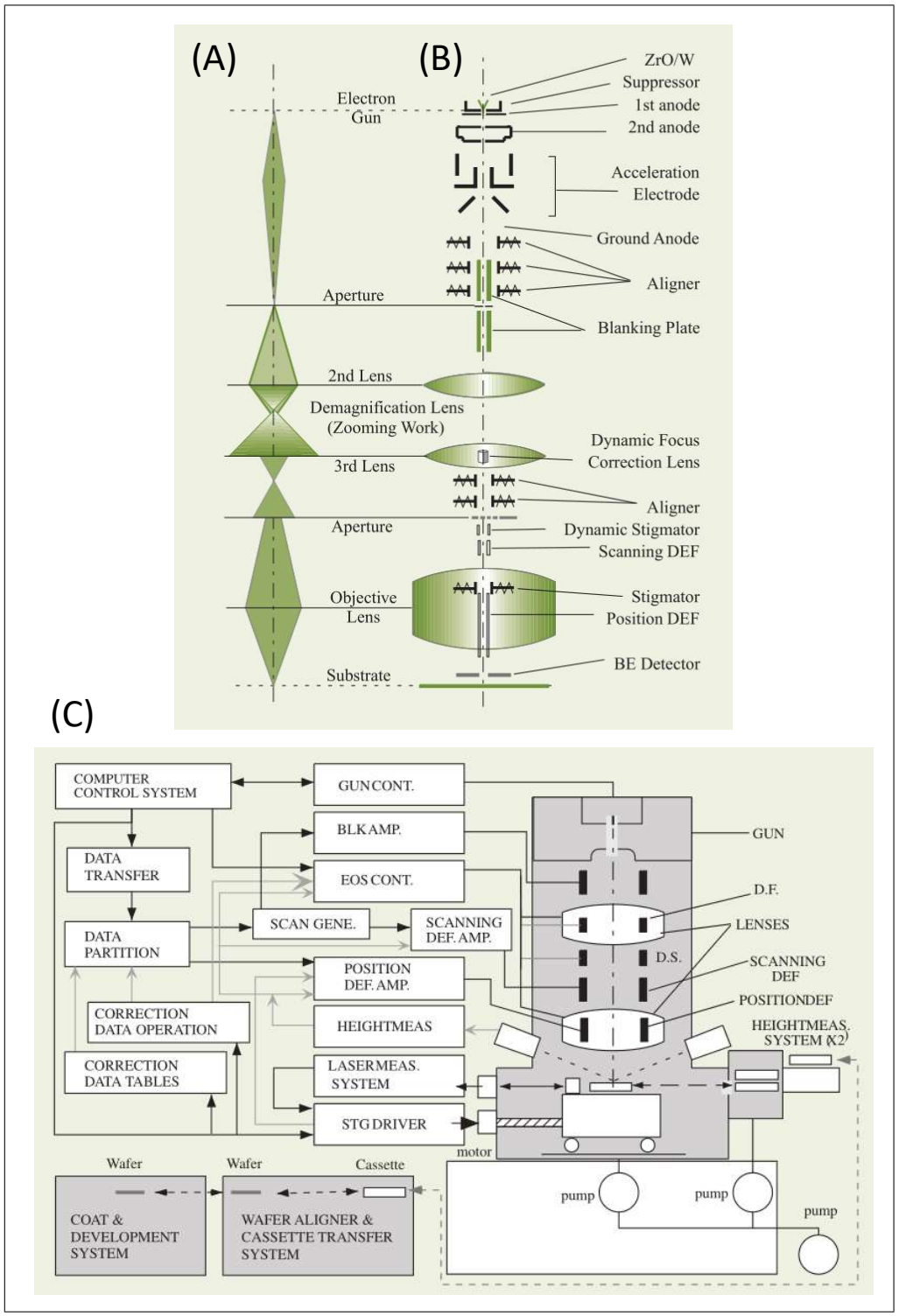


FIGURE 3.12: Electron-beam lithography schematic

spots which are exposed to fewer scattered electrons). The beam can pattern a 500μm x 500μm field area, before the beam is blanked, and the sample automatically, physically repositioned by the stage, before another 500μm x 500μm field area can be written. In this manner, an entire 150mm diameter wafer can be written as a series of 500μm x 500μm fields.

Two positive resists were used, high-resolution ZEP520A, and medium-resolution polymethyl methacrylate (PMMA). Before exposure, ZEP520A is spun onto the sample at 3370rpm (revolutions per minute) and subsequently baked on a hotplate at 180°C for 3 minutes. This achieves a resist thickness of 400nm. In the case of PMMA9504A resist, the sample is first exposed to hexamethyldisilazane (HMDS) vapour for 3 minutes to increase surface adhesion. PMMA9504A it is spun onto the sample at 1500rpm, baked at 180°C for 3 minutes to achieve a resist thickness of 350nm. The recipe for developing ZEP post-electron-beam lithography exposure is as follows: the sample is submerged (and agitated physically) in n-Amyl Acetate (ZED N50) for 2 minutes, 15 seconds, followed by agitated submersion in IPA for 30 seconds, followed by deionized (DI) rinse and N_2 drying. At this point the substrate of the exposed regions of the design will be exposed for any subsequent dry or wet etching. The recipe for developing PMMA post-electron-beam lithography exposure is as follows: the sample is submerged in a 1:1 solution of Methyl isobutyl ketone (MIBK):IPA for 1 minute 30 seconds, followed by submersion in IPA for 30 seconds, followed by DI rinse and N_2 drying. The sample then undergoes a post-development bake at 110C for 2 minutes.

3.3.2 Inductictively Coupled Plasma Etching

Inductively coupled plasma (ICP) etching is a common fabrication technique used to isotropically or anisotropically etch a developed pattern into the substrate. The substrate is placed into an loadlock chamber which is pumped down to low pressure (X) before the sample is transferred to the process chamber. Once the sample is in the process chamber, the etch recipe is initiated. This recipe usually consists of 5 steps: 1) pre-process gas purge, 2) plasma strike step, 3) plasma etch step, 4) cooling step, 5) post-process gas purge. During the plasma strike and plasma etch step, a high-power radio frequency (RF) through a coil generates a magnetic field, which induces a current in the gas, causing the gas to ionize and form a plasma. A separate RF bias is applied to the sample which creates a directional electric field above the substrate, which causes the ions to be drawn to the substrate, increasing the anisotropic nature of the etch.

Table 3.2: ICP Si and SiO_2 etch recipes

Target etch material	Ar flow rate (sccm)	CHF_3 flow rate (sccm)	SF_6 flow rate (sccm)	ICP power (W)	Platen bias power (W)	Si etch rate (nm/s)	SiO_2 etch rate (nm/s)	ZEP etch rate (nm/s)
Silicon	0	45	25	800	50	5	1	1
Silicon dioxide	38	12	0	1000	40	3	1	1

Substrate etching is achieved by a combination of chemical etching, and physical etching (sputtering) caused by the accelerated high-mass ions colliding with the substrate. The

target material (e.g. Si) etch speed, the ratio between the target material and mask or stopping layer material (e.g. ZEP or SiO2) (selectivity), the anisotropy and the uniformity are all dependent on the chemical composition of the plasma and chemical flow rates, the ICP RF and RF power, the platen generator RF and RF power to apply the directional DC bias, the chamber pressure and the substrate temperature. For Si etching, a plasma consisting of SF_6 and CHF_3 was used, and for SiO_2 etching, a plasma consisting of Ar and CHF3 was used. During Si etching, fluorine (which is broken off from the SF_6 in the plasma) is responsible for the chemical etching of Si, whilst the CHF_3 coats the vertical sidewalls as they are etched, creating vertical etch walls/trenches. During SiO_2 etching, CHF_3 provides chemical etching, and Ar, being chemically inert, provides physical etching. The recipes optimized in this work for vertical Si and SiO_2 etching are shown in Table 3.3.2.

3.3.3 Plasma Enhanced Chemical Vapour Deposition

Plasma enhanced chemical vapour deposition (PECVD) is a process in which a RF electromagnetic energy source is used to ionize a gas, forming a plasma (similar to how ICP plasma is formed), which then bombards and deposits material onto the substrate. The use of RF energy source allows for the formation of a plasma which would otherwise only form at very high temperatures. This allows materials such as Si, SiO_2, silicon nitride (Si_3N_4) to be deposited at low temperatures (the substrate only has to be heated to 300C). a-Si can be deposited using a combination of SiH_4, H_2 and Ar plasma, with SiH_4 obviously being the active agent, and H_2 and Ar included to optimize the characteristics of the deposited layer. SiO_2 can be deposited using a combination of SiH_4, N_2 and N_2O. The standard recipes used in this work for Si and SiO_2 deposition are shown in Table 3.3.3.

Table 3.3: PECVD recipes for Si and SiO_2 deposition

Deposition material	SiH_4 flow rate (sccm)	H_2 flow rate (sccm)	Ar flow rate (sccm)	N_2 flow rate (sccm)	N_2O flow rate (sccm)	RF power (W)	Chamber pressure (mT)	Deposition rate (nm/s)
Silicon	100	100	300	0	0	10	400	0.3
Silicon dioxide	4	0	0	80	350	20	1000	1

3.3.4 Chemical Mechanical Polishing

Chemical mechanical polishing is a fabrication technique that uses a combination of chemical and mechanical milling to smoothen the surface of a substrate. A chemically

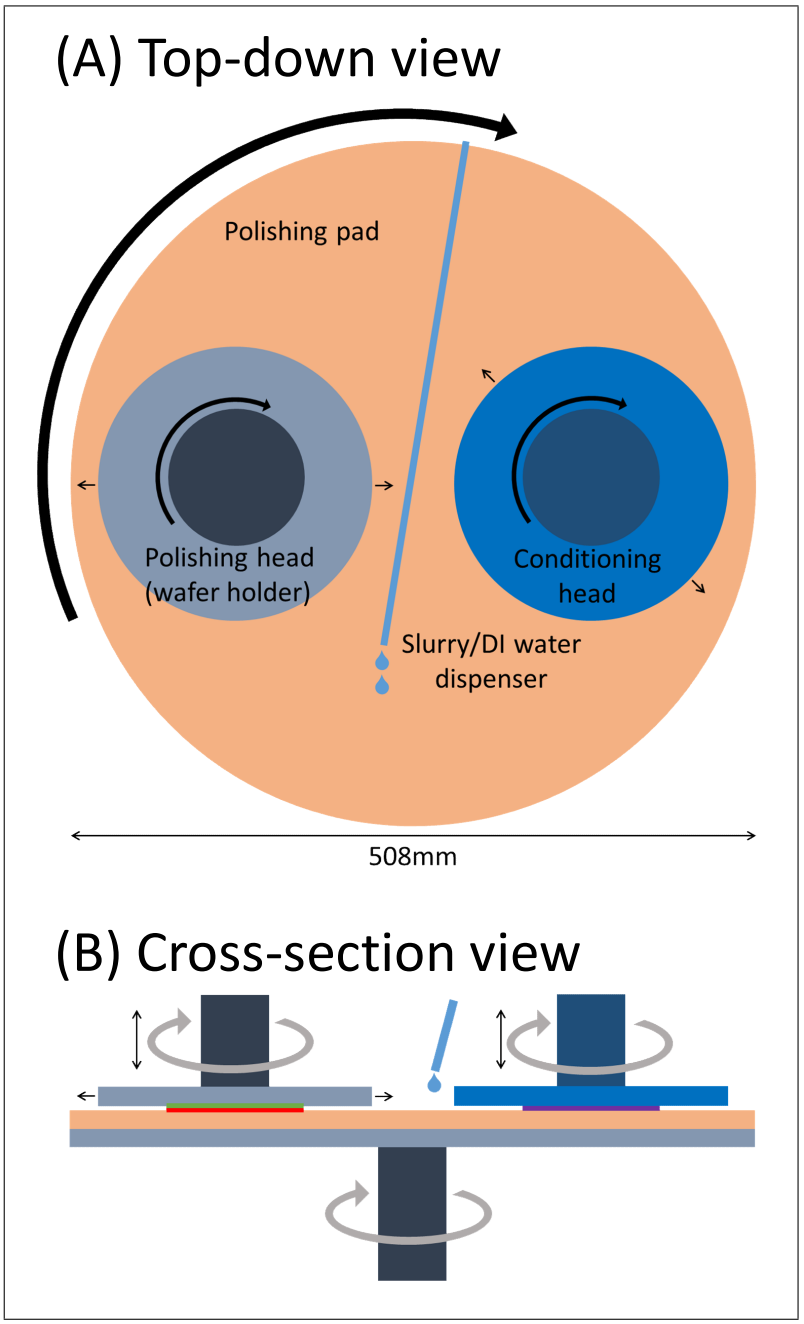


FIGURE 3.13: Top-down and cro-secctional view schematic of CMP tool. Top-view shows the orange polishing pad which rotates clockwise, the polishing head which holds the wafer underneath itself, the conditioning head which holds a conditioning head underneath and the flexible slurry/DI water dispenser. During operation the polishing head and the conditioning head can both be oscillated side to side whilst rotating. Slurry/DI water is dispensed near the centre of the polishing pad, and spreads towards the edge as a result of centrifugal force. The cross-sectional view shows how both heads can be moved up and down, bringing the wafer and conditioning pad out of or into contact with the polishing pad. A thin rubber membrane (green) is used to hold the back of the wafer (red) whilst dynamic force is applied to the wafer.

corrosive slurry (a mixture of microscopic particles (e.g. spherical SiO_2 particles) suspended in liquid) is applied to the surface of the rotating wafer as the rotating wafer is

simultaneously pressed against a rotating polishing platen. A schematic of a CMP tool, highlighting the key operational components, is presented in Figure 3.13 and an image of the CMP tool used in this work (POLY 500 CMP SYSTEM from G&P Technology) is shown in Figure 3.14.

FIGURE 3.14: CMP tool showing the polishing table/platen with the white polishing pad, the conditioning head on the left, the polishing head/wafer holder on the right, and the central tubes for dispensing slurry and DI water to the rotating pad.

The wafer is held in place under the polishing head by placing the wafer in contact with a thin plastic membrane, and applying a vacuum to the other side of the membrane. In addition to the type of slurry used, there are several variable parameters that effect the polishing rate of different materials on the substrate and the polishing uniformity, including wafer pressure, rotational speed of the platen/polishing head/conditioning head, slurry wetting time and pre-polishing conditioning, flow rate of the slurry and DI water and the polishing time. If a device has a complicated 2D structure, the relative polishing rates of different materials at different heights can be hard to establish, and can change significantly as polishing continues. For this reason a single CMP step is often broken

into several smaller steps, with the polishing status/progress being measured using an ellipsometer and a stylus-profiler (which measures structure height along a cross-section). The following is a sequence of typical steps for conducting a chemical mechanical polishing: (1) the polishing pad is "wetted" using DI water, (2) the pad is conditioned with slurry, the oscillating, rotating conditioning head is in contact with the rotating polishing pad, (3) the polishing pad is lowered such that the wafer is in contact with the polishing pad, under slight applied pressure. The polishing head is rotated, (4) The polishing head is raised from the polishing pad, the wafer is cleaned with DI water and can be measured/further processed.

3.3.5 SiO_2/SiO_2 Bonding

Direct SiO_2/SiO_2 bonding is described in 2.3.1. This subsection will therefore simply introduce the wafer bonding equipment used, the "EVG520 HE Semi-Automatic Wafer Bonding System" from EVG. The 150mm diameter wafers to be bonded are preprocessed before being manually brought into surface-surface contact. Depending on the surface material, the top wafer may slide over the bottom wafer. If alignment between the top and bottom wafer is required, this much be done visually and manually, before introducing the weakly bonded wafer pair into the bonding machine. During operation, a 150mm diameter top plate applies force uniformly to the backside of the top wafer. The top and bottom contact plates that hold the wafer during bonding can be heated independently up to 500C. The recipe can be set programmatically, the plates are ramped to the desired temperature, top-down force is applied for a preset duration of time, and then the plates are ramped back to room temperature. Once the recipe is complete, the bonded wafers can be annealed at high-temperature in a high-temperature furnace is necessary.

3.3.6 Local Oxidation of Silicon

Local oxidation of silicon (LOCOS) is a process whereby a thicker SiO_2 layer is grown in a particular exposed area of Si than in nearby protected areas, when the substrate undergoes thermal oxidation. The protective layer used is usually a combination of SiO_2 and/or Si_3N_4. When utilized on a horizontal Si layer, this method can be used to selectively lower the Si/SiO_2 interface to define rib-waveguides, or insulate CMOS transistors in the case of IC fabrication. When utilized on a vertical Si layer or sidewall, with thick ($\sim$20nm) protective SiO_2 layer on the top horizontal layer, this method can be used to grow $\sim$5nm SiO_2 (consuming $\sim$2nm Si), whilst only $\sim$1nm SiO_2 is grown on the protected top horizontal layer (consuming $\sim$0.5nm Si). Because the oxidation rate of Si is very dependent on the surface SiO_2 thickness[110], particularly at low SiO_2 thickness, and on rough Si sidewalls oxidation can occur from slightly different directions (e.g. a small triangular Si protrusion is etched from two sides simultaneously), this causes the exposed jagged, rough Si surface to quickly smoothen after only a few nm SiO_2 growth.

Chapter 4

Bonded Double-SOI and Horizontal-Slot Strip-Waveguide

This chapter will present the SiO_2/SiO_2 bonding process that was developed to realise the SiO_2 horizontal-slot layer, and the characterisation of MOScap devices using the SiO_2 horizontal slot as the gate oxide to demonstrate the bonding quality. The initial trial fabrication of a horizontal-slot strip-waveguide utilizing this bonding technique will also be presented.

4.1 Bonded MOScap

4.1.1 Fabrication

MOScap devices were fabricated on directly bonded bulk <100> Si wafers with a 10nm bonding SiO_2 to establish bonding quality. Application of medium power O_2 plasma using RIE prior to SiO_2/SiO_2 bonding has been shown in some circumstances to reduce interfacial void density[92]. However, any processing steps prior to bonding have the potential to introduce particle contaminations to the surface which increase void density. To establish whether RIE O_2 plasma should be applied prior to SOI/SOI bonding for the fabrication of optical devices, several different pre-bonding recipes were tested. Three pairs of wafers were bonded. Two of the pairs underwent pre-bonding RIE O_2 plasma and one did not. The wafer details and pre-bonding recipe details are presented in Table 4.1.

The three pairs of wafers were bonded and MOScap chips were fabricated using the following process (which is presented schematically in Figure 4.1):

1. Both top and bottom wafers were thermally oxidized in a high-temperature dry-O_2 environment furnace at 950C for 5 minutes. Reference wafers measured indicated SiO_2 thickness between 7.7-9.1nm.

TABLE 4.1: Summary of SiO_2/SiO_2 pre-bonding recipe parameters

	Top Wafer			Bottom Wafer		
	Target SiO_2 Thickness (nm)	Doping Type	RIE Forward Power (W)	Target SiO_2 Thickness (nm)	Doping Type	RIE Forward Power (W)
W1	5	p-	300	5	p-	300
W2	5	p-	250	5	p-	250
W3	5	p-	n/a	5	n+	n/a

2. W1 and W2 underwent O_2 plasma RIE surface conditioning at forward power 300W and 250W respectively. DC bias = 0V, RF power = 0W.

3. All wafers were individually immersed in dilute (1:200 HF:DI water) HF for time=50-80s to thin the surface SiO_2 to the target 5nm, and to increase the surface hydrophobicity (saturating the surface with dangling –OH bonds) immediately prior to bonding.

4. Wafers surfaces were placed in direct contact and aligned manually, aligning wafer-flat to wafer-flat visually. Once suitable alignment was achieved (estimated <1mm horizontal misalignment, <0.1mm vertical misalignment, <2° rotational misalignment), very slight pressure was allied on the backside of the top wafer with a tweezer, and the two SiO_2 layers bonded, with an audible *click* caused by the bonding "wave" spreading from the "nucleation point". At this point the wafers were weakly bonded.

5. Wafers were annealed at 450C for 7 hours under uniformly distributed top-down applied force of 5kN (68.5×10^3 Pa) in a EVG520HE Semi-Automatic Wafer Bonding System.

6. Wafers were annealed at 100C for 3 hours in an N_2 atmospheric-pressure environment.

7. Wafers were immersed in 1:20 HF for 15 minutes to remove the SiO_2 from the back of the wafer and ensure good Al contact.

8. 100nm Al was sputtered onto both sides of the wafer.

9. The wafers were spin coated and baked on both sides with protective S1813 photoresist.

10. Wafers were cleaved using a diamond pen inscriber into chips with surface area 100-300mm^2.

11. Wafers were cleaned using N-methyl-2-pyrrolidone (NMP) for 5 minutes, rinsed in DI water and dried using N_2 to fully remove the photoresist.

12. MOScap chips were them removed for measurement.

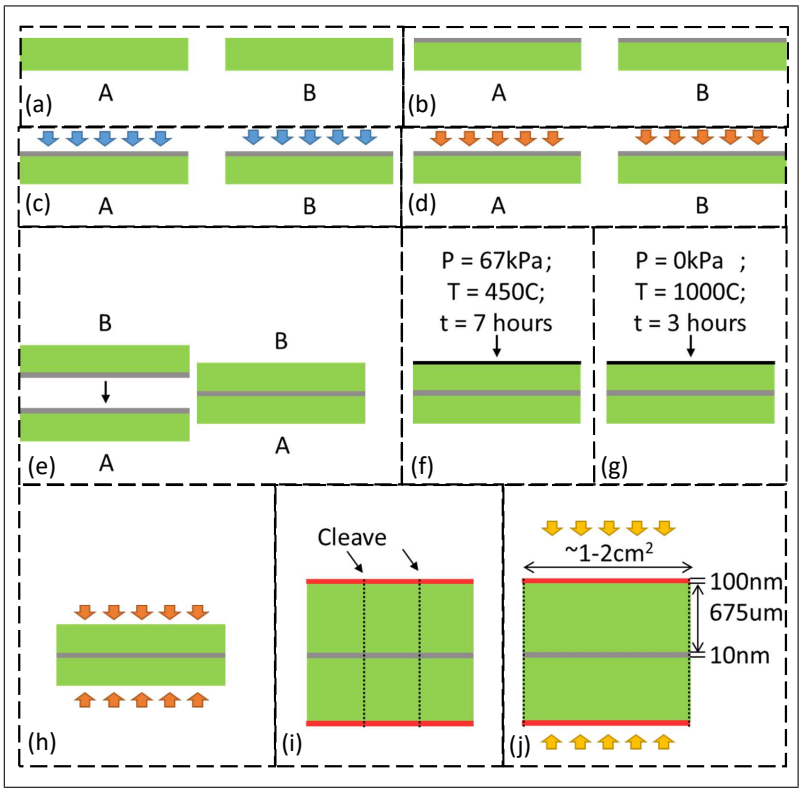


FIGURE 4.1: Process flow for SiO_2/SiO_2 bonding (a) Top and bottom wafers labelled "A" and "B". (b) 7.5nm SiO_2 layer grown by thermal oxidation at 950C (5 minutes). (c) W1 and W2 undergo RIE 0_2 plasma treatment for 30 seconds at RIE power 300W and 250W respectively. W3 did not undergo pre-bonding RIE treatment. (d) Wafers immersed in dilute HF (1:200 HF:DI water) to increase surface hydrophobicity and thin top SiO_2 layer to 5nm. (e) Wafers placed in direct contact manually, aligning wafer-flat to wafer-flat visually. Estimated rotational misalignment $<2°$. (f) High-pressure was applied at medium-temperature for 7 hours. (g) High-temperature was applied at atmospheric-pressure for 3 hours. (h) Wafers were immersed in HF (1:7) for 15 minutes to remove back SiO_2 layer. (i) Immediately following SiO_2 removal, 100nm Al was deposited on both sides of the wafer using sputtering. A protective photoresist layer (S1813) was spun and baked onto the top and bottom of the wafer, which was then cleaved with a diamond pen into chips of various sizes ranging from 100-300mm^2. (j) The chips were cleaned using NMP for 5 minutes, rinsed with DI water, dried with N_2 and measured.

The bonded c-Si/SiO_2/c-Si interface from W1 (RIE 300W) was imaged using scanning electron microscope (SEM) (Figure 4.2), and a the thin SiO_2 layer can be clearly seen. Figure 4.2 (a) shows the SiO_2 most clearly, where it appears to be ∼50nm. However, this appears to be an artefact of the SEM (SiO_2 charges during SEM operation, and therefore appears very bright, overshadowing adjacent Si areas at this magnification and SEM operational energy). Figure 4.2 (a) does show the c-Si/SiO_2/c-Si interface to be slightly bent, indicating that the wafer might be slightly bowed. This bowing is caused by non-uniform distribution of tension between the two wafers, but this is expected to relax upon removal of the handle layer of one of the wafers, and is therefore not expected to effect the quality of devices fabricated on double-SOI substrates that have been bonded using this technique. Figure 4.2 (b) and (c) at higher magnification show the SiO_2 layer

thickness to be ∼20nm, which is closer to the expected value of 10nm (which is based on accurately grown and thinned thermal oxide).

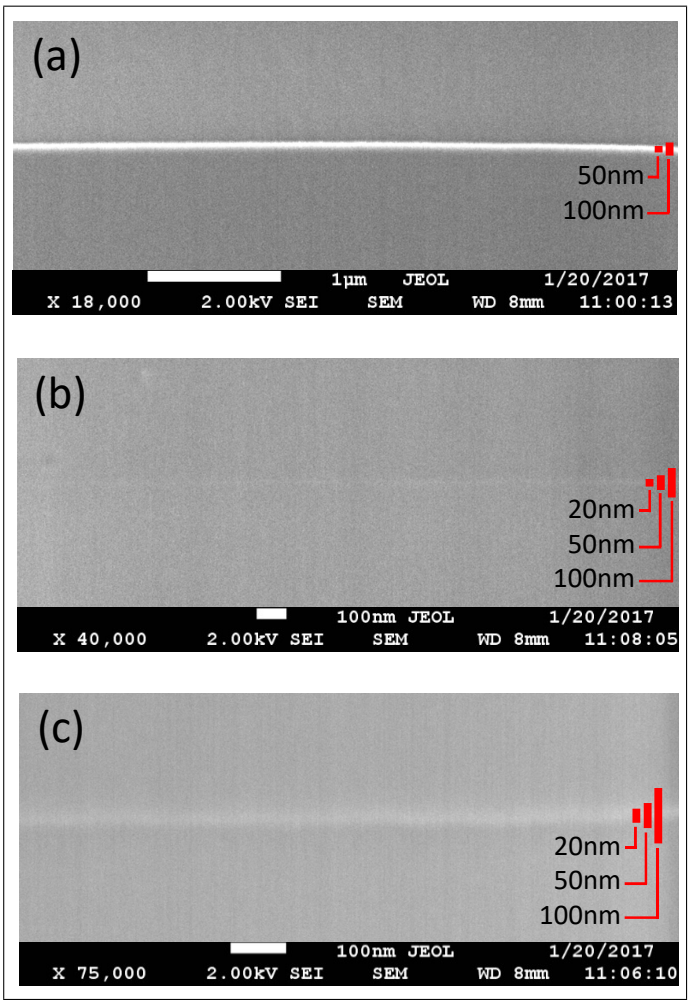


FIGURE 4.2: SEM images at the c-Si/SiO_2(10nm)/c-Si interface. (a) x18,000 magnification, (b) x40,000 magnification, (c) x75,000 magnification.

4.1.2 Interface Quality Characterisation

8 x W1 (p-/i/p-) chips, 4 x W2 (p-/i/p-) chips and 11 x W3 (n+/i/p-) chips were characterized using high-frequency capacitance/voltage measurements, to establish the electrical quality of the thin SiO_2 bonding layer and the c-Si/SiO_2/c-Si interface. A high quality SiO_2 bonding layer will have low leakage current, and uniform ϵ_r throughout its volume. A high quality oxide layer will therefore demonstrate equivalent oxide thickness (EOT) close to the physical oxide thickness ∼ 12nm, and high uniformity across different devices. The measurements were taken with 30mV AC at 10kHz operating frequency. In the case of devices from W1 and W2, gate bias was swept from -2V to +2V. In the case of devices from W3, gate bias was swept from -2V to +2V to -2V. The area (A) of each device was also measured. Using C and A it was possible to estimate the EOT of the

SiO_2 layer using the following equation:

$$\text{EOT} = \frac{A\epsilon_0\epsilon_r}{C} \tag{4.1}$$

Where:
C = capacitance (F)
α = area of parallel plates comprising capacitor (i.e. chip area (m))
ϵ_0 = electric permittivity of free space (F/m)
ϵ_r = relative electric permittivity of dielectric. This value is a function of material, material thickness and measurement frequency, as well growth/deposition parameters etc. Accurate determination of ϵ_r is necessary for applications involving ultra-thin films ($t_{ox} \sim$ 1nm), but at $t_{ox} \gtrapprox$ 10nm, for high temperature grown thermal oxide, we can assume that $\epsilon_{SiO_2} = 3.9$[111]. If, using this assumption, EOT is significantly larger than the physical value, the electrical quality of the oxide is poor.
EOT = separation between parallel plates (m)

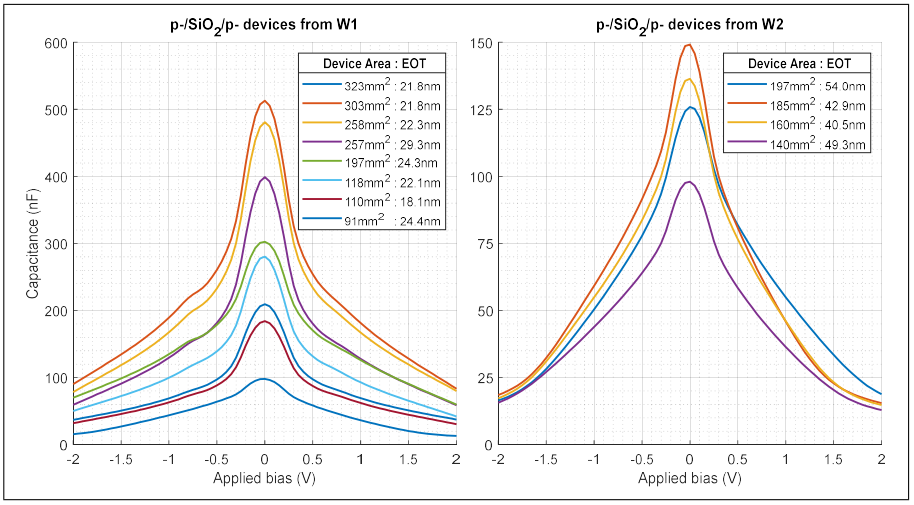


FIGURE 4.3: CV measurements for bonded p-/SiO_2/p- devices with various surface area. EOT for each device indicated in legend. Bias V swept from -2V to +2V

Figure 4.3 shows the experimental CV measurements for the p-/SiO_2/p- devices from wafers W1 and W2. These wafers went through a pre-bonding fabrication recipe that involved O_2 plasma RIE surface treatment with RIE power of 300W and 250W respectively. The peak capacitance (at direct current (DC) bias = 0V) was extracted and used to calculate EOT for each device. This is shown in the figure legend next to the respective device. W1 EOT = 18.1-29.3nm (EOT_{avg} = 23.0nm). W2 EOT = 40.5-54.0nm (EOT_{avg} = 46.7nm). Figure 4.4 shows the experimental CV measurements for the n+/SiO_2/p- devices from wafer W3. This wafer did not go through a pre-bonding fabrication recipe that involved O_2. Each device was measured twice, initially bias was applied in the n-i-p direction, and subsequently bias was applied in the p-i-n direction. All devices demonstrated CV curves characteristic of accumulation/inversion/depletion operation with bias applied in n-i-p direction, and depletion/inversion/accumulation in

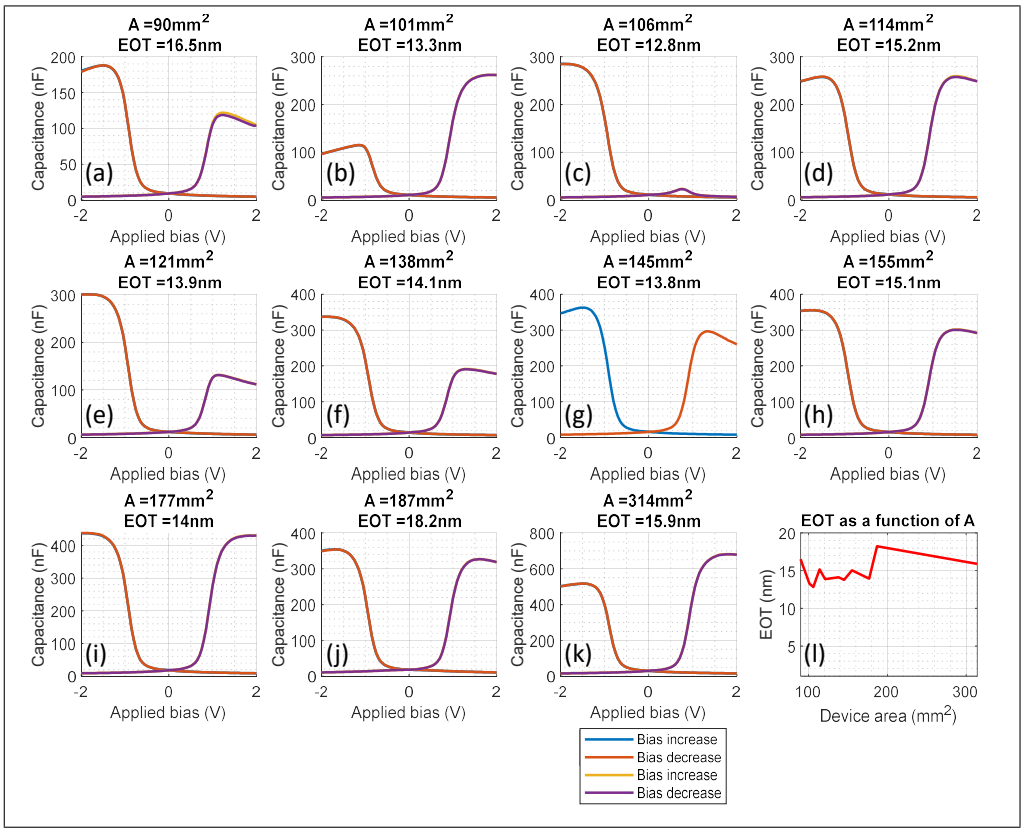


FIGURE 4.4: (a-k) CVmeasurements for bonded p-/SiO_2/n- devices with various surface area. Bias V swept from -2V to +2V to -1V (except for device (g) due to a tool error). Each device was measured once with bias initially applied in n-i-p direction and then flipped, and then measured again with bias applied in the p-i-n direction. (L) shows the EOT as a function of device area for chips (a-k), showing that EOT is independent of device area

the case of bias applied in the p-i-n direction, except for Figure 4.4 (c) which exhibited a breakdown voltage ∼0.75V when operated in p-i-n direction. Several devices exhibited significant asymmetry when measured the opposite directions, which is a consequence of the imperfect Al contact, but no device exhibited hysteresis. Device (i) resembles most closely the ideal case, with symmetrical CV curves when measured in each direction, and an EOT = 14.0nm. Device (c) operated in n-i-p direction is also an ideal case, with maximum capacitance indicated EOT = 12.8nm. Across the measured devices EOT = 12.8-18.2nm (EOT_{avg} = 14.8nm).

Figure 4.5 shows the measured EOT as a function of device area for each wafer. The devices from W3 (no RIE surface activation pre-bonding) consistently demonstrate a EOT closest to the actual SiO_2 thickness (which was carefully controlled prior to bonding). Figure 4.5 also shows that EOT is independent of device area, which implies that there are no device edge effects such as leakage current that effect the performance of these devices. The increase in EOT from the expected value can be explained by the presence of minor nm size inter-facial voids, which increases the effective separation of the two Si “plates”. The presence of such voids may lead to increased optical transmission loss

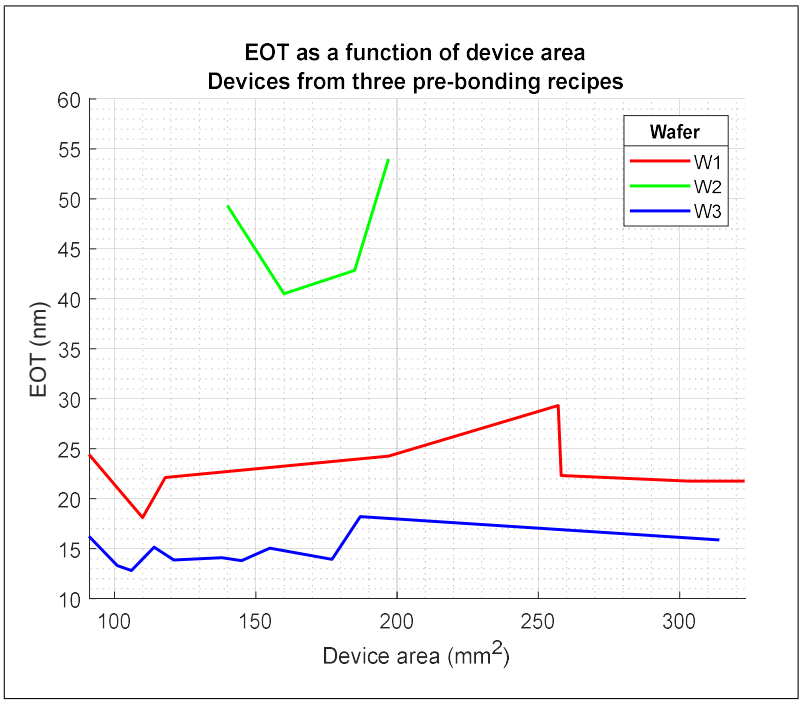


FIGURE 4.5: Measured EOT as a function of device area from bonded wafer utilizing different pre-bonding recipes.

in waveguides fabricated on bonded double-EOT, as well as decreasing actual C from designed C in the active horizontal-slot fin-waveguide accumulation modulator (resulting in higher $V_\pi L$ or lower modulation speeds) fabricated on such a platform. However, despite minor voids, there was no evidence of major voids and working MOScap devices could be successfully fabricated. Based on these results it was decided to forego RIE in future SiO_2/SiO_2 bonding, as it was deemed to introduce unnecessary surface particles/contaminations.

4.2 Horizontal-Slot Strip-Waveguide

4.2.1 Fabrication

Having established SiO_2/SiO_2 bonding and c-Si/SiO_2/SiO_2 interface sufficient to realise active active MOScap devices with $EOT_{avg} = 14.8$nm, double-SOI substrates were fabricated using the same pre-bonding recipe. The process flow of the fabrication up until the realisation of the double-SOI is shown in Figure 4.6, and the major processing steps are listed below:

1. Two pairs of 220nm SOI wafers with (110) crystallographic orientation in the direction of the surface normal were thinned by a process of dry O_2 furnace oxidation

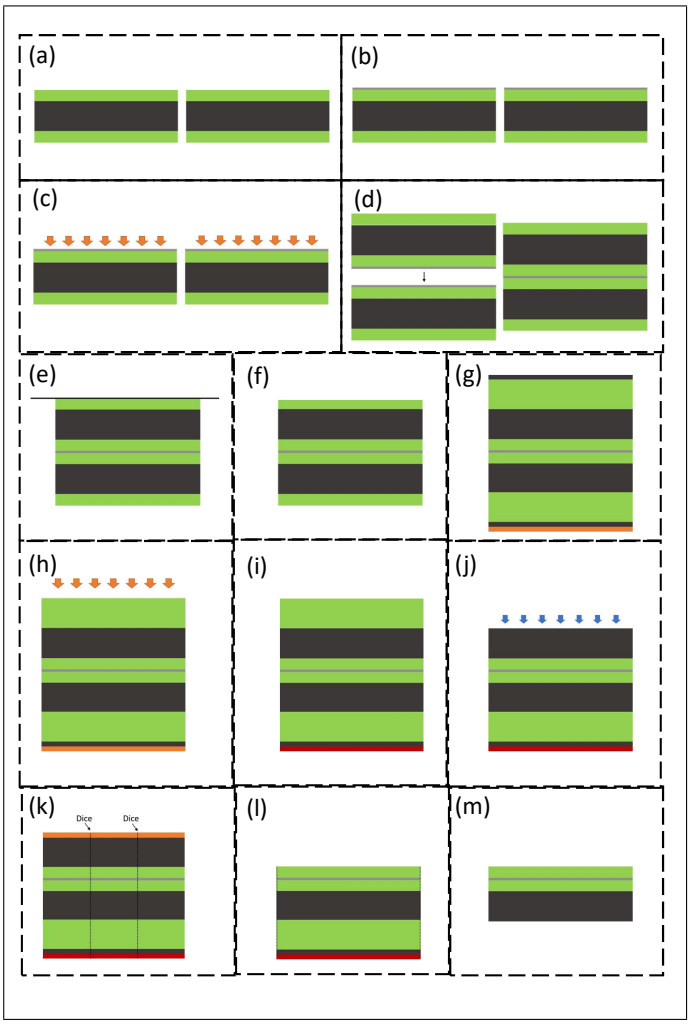


FIGURE 4.6: Process flow showing double-SOI substrate fabrication. (a) Two (110) orientation SOI wafers thinned to 103nm. (b) Thermal annealing, grew 8.8nm SiO_2. (c) 1:200 HF pre-bonding surface conditioning and thinning to target thickness = 5nm per wafer. (d) Wafers placed in direct contact. (e) Double-wafers annealed at pressure = 67kPa, temperature = 450C, time = 7 hours. (f) Double-wafer annealed at pressure = 0kPa, temperature = 1000C, time = 3 hours. (g) S1813 was deposited on the top wafer. Si_3N_4 was deposited using PECVD on the bottom wafer. Then S1813 was removed. (h) Exposed 2μm SiO_2 layer on the bottom of the top wafer was removed using 1:7 HF. (i) ~675μm Si handle layer removed using potassium hydroxide (KOH). (k) S1813 was spun and baked. The wafer was diced into 4cm x 3cm chips. S1813 was then removed. (l) The exposed 2μm SiO_2 BOx layer was removed using 1:7 HF. (m) Double-SOI substrate realised.

and HF oxide removal to an SOI thickness = 102.6nm, 104.3nm (pair #1), and SOI thickness =105.0nnm, 104.9nm (pair #2).

2. 8.8nm SiO_2 was grown on the surface of the wafers.

3. 1:200 HF was used to thin the top SiO_2 layers of all wafers to 5nm.

4. The wafer pairs were immediately placed in direct surface/surface contact and slight pressure was applied to the back of the top wafer using a tweezer.

5. The bonded wafers were annealed at temperature 1000C for 3 hours.
6. Photoresist S1813 was spun onto the top of each bonded wafer pair and baked.
7. Si_3N_4 was deposited onto the bottom of each wafer pair using PECVD.
8. S1813 was removed from the top of each wafer pair using NMP, ACE, IPA and DI water.
9. The exposed 2μm SiO_2 layer on the bottom of the top wafer of each wafer pair was removed using 1:7 HF.
10. The exposed ~675μm Si handle layer of the top wafer of each wafer pair was removed using an elevated temperature potassium hydroxide (KOH) etch over several days. Total etch time for pair #1 = 906 minutes (equivalent to ~34% over-etch) and pair #2 = 825 minutes (equivalent to ~22% over-etch).

Potassium hydroxide (KOH) is a strong base chemical that is a strong anisotropic etchant of crystalline Si. Due to the rounded edges of the wafers, the KOH etched the wafer edges and underneath the top wafer at the wafer edge (Figure 4.7).This caused the wafer edges to become incredible fragile and breakable; this was potentially a major source of contaminations. KOH also selectively etches different Si planes at different etch rates. This, along with the fact that the backside of an SOI wafer has high nanoscale roughness and can have +-25μm variation in thickness across the wafer, leads to certain areas being etched faster than others. In Figure 4.8 (A) "nucleation" sites (maybe initially scratches or small areas where particularly high roughness causes a major indentation in the substrate), where KOH etches along the <111> crystal plane, can be seen. These appear as distinctive squares, sometimes in patters along a line which could come from scratches acquired when the wafer was placed in the PECVD machine for Si_3N_4 deposition.

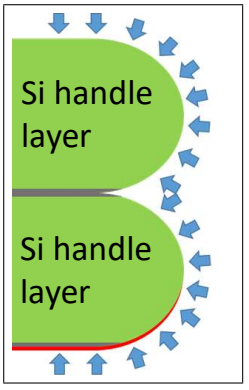


FIGURE 4.7: Schematic showing KOH wafer edge etching

In Figure 4.8 (B) the areas which etched faster can be seen to have etched down to the 2μm BOx before the rest of the surface. In Figure 4.8 (C) some of these nucleation sites have etched all the way through the BOx to bottom SOI. At other points patterns can

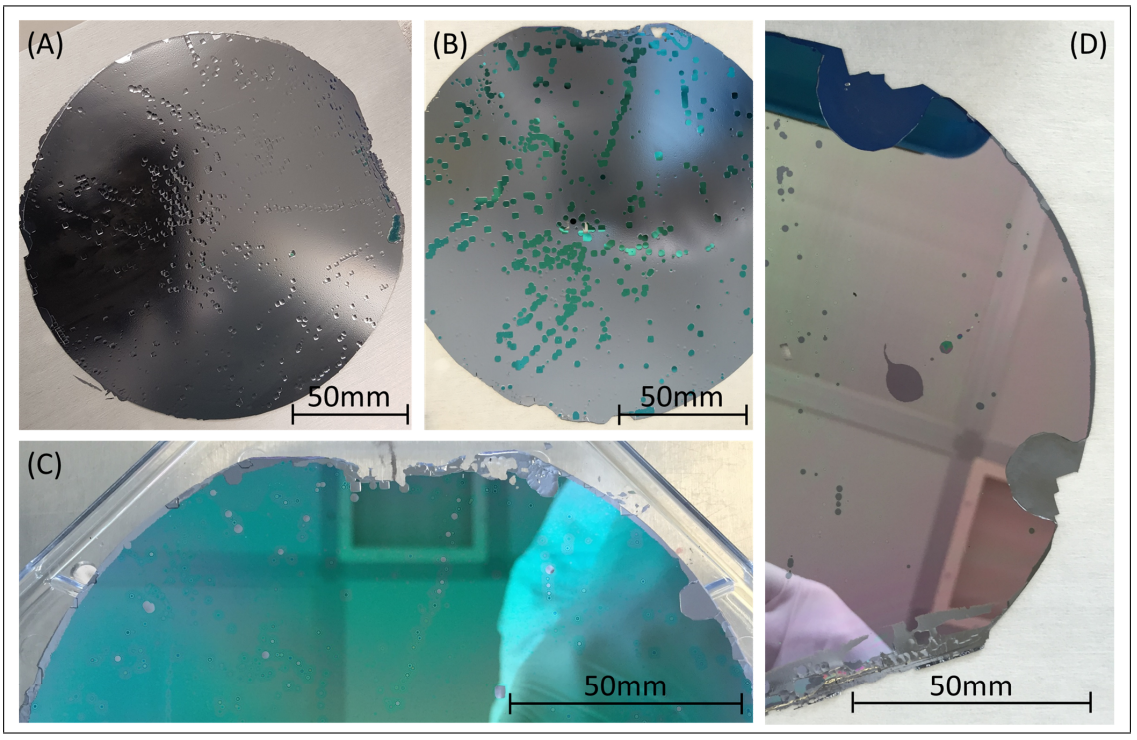


FIGURE 4.8: Images of the wafer pair #1 (A, B, C), and wafer pair #2 (D), having undergone KOH thinning. Wafer pair #1 after 690 minutes (A), 840 minutes (B), and 906 minutes KOH etching (completely etched) (C). Turquoise/green surface is BOx oxide. Grey blemishes in (C) are KOH over-etched regions of bottom wafer handle layer Si. Wafer pair #2 after 825 minutes KOH etching (completely etched).

still be observed where the square nucleation sites were, suggesting that at these points the BOx has been etched significantly further than the general area. Full-wafer scan ellipsometry measurements were taken of wafer pair #1 (906 minute etch) (Figure 4.9) and wafer pair #2 (840 minute etch) (Figure 4.10). Wafer pair #1 data mostly fit a stack model of Si substrate/SiO_2 layer, suggesting that KOH had over-etched through the top BOx, both SOI layers and the SiO_2 bonding layer. Wafer pair #2 data mostly fit a stack model of Si substrate/2μm SiO_2/100nm Si/12nm SiO_2/100nm SiO_2/ 1000nm SiO_2, suggesting that in this case, KOH etching reached half-way through the 2μm top BOx stopping layer as intended. Despite the fact that most measured data points fit a physical stack model with sufficiently low mean squared error (MSE), there were many measured points on both wafer pairs with a very poor experimental data/stack model fit. Measured data at these "broken" points was either very noisy or in some other way could not be fit to a physical substrate stack model, potentially due to high local non-uniformity. Broken points are identified as points with MSE $\gtrapprox$ 200. 9 "broken" points were identified for wafer pair #1 and 18 "broken" points were identified for wafer pair #2. This can be interpreted as 83% wafer yield and 67% wafer yield respectively. These meaningless data points have been removed in Figure 4.9 (A) and (B), and Figure 4.10 (C), (D), (E) and (F). Removed points have been blanked out with black rectangles so

as not to give the misleading impression that the etching uniformity is greater than it actually is.

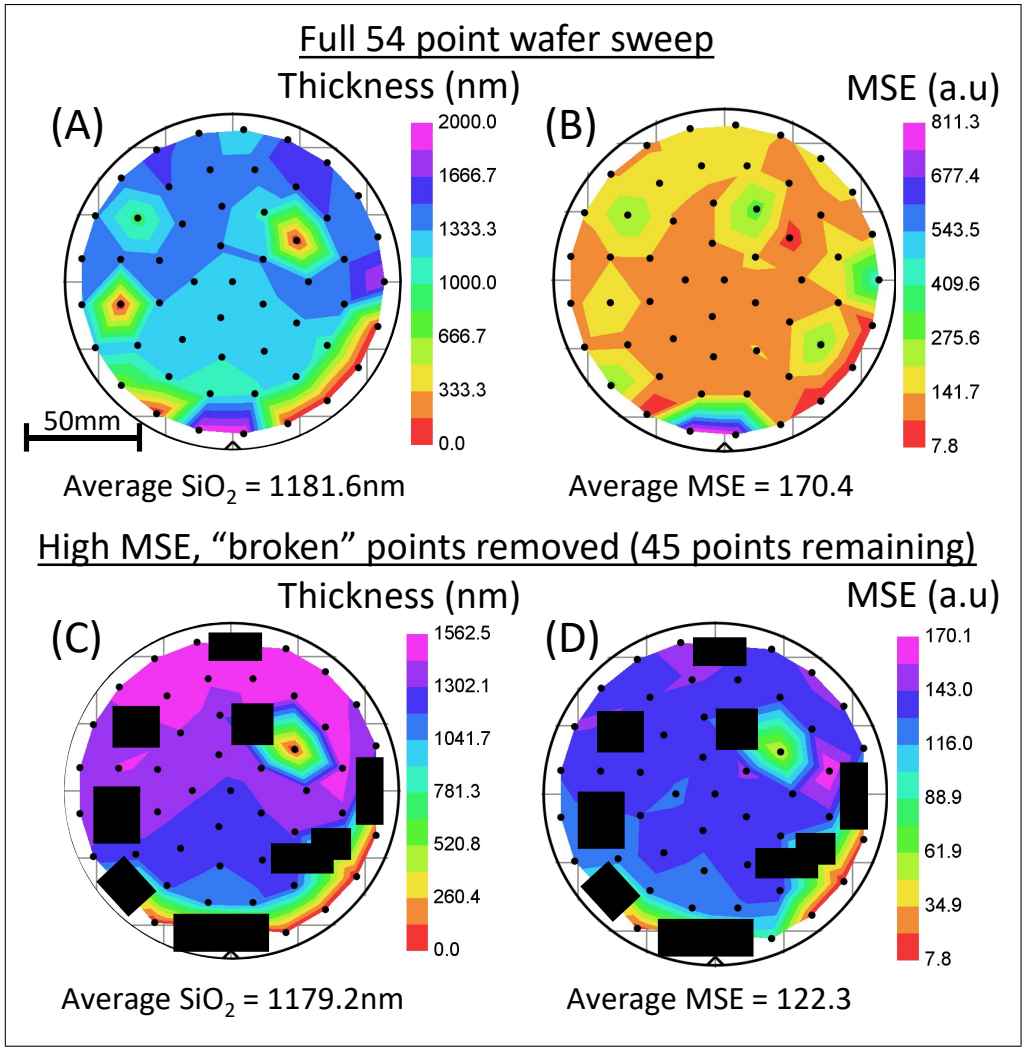


FIGURE 4.9: Ellipsometry data map of KOH etched bonded wafer (906 minute etch time). (A) shows the fitted value for SiO_2 thickness across the wafer, with corresponding MSE at each point in (B). (C) shows the fitted value for SiO_2 thickness across the wafer with high MSE "broken" points removed, with corresponding and MSE at each point in (D). KOH etch rate was fastest near the flat (bottom) of the wafer, etching through to the bottom Si substrate at some points, as well as at one anomalous point near the centre of the wafer.

Figure 4.9 (C) shows that KOH etch rate was slowest at the top of the wafer, and fastest near the flat (indicated on the figure by the small arrow at the bottom of the black circle representing the circumference of the wafer). At several points (near the flat and at the anomalous red point top-right of the centre) the bottom SiO_2 layer is completely removed ($SiO_2 = 0$nm). Average remaining SiO_2 thickness = 1181.6nm, range = 1562.5nm, standard deviation = 479.8nm.

Figure 4.10 (C) shows that wafer pair #2 KOH etching was more uniform than wafer pair #1 KOH etching. Average remaining top SiO_2 thickness = 888.9nm, range = 155.3nm,

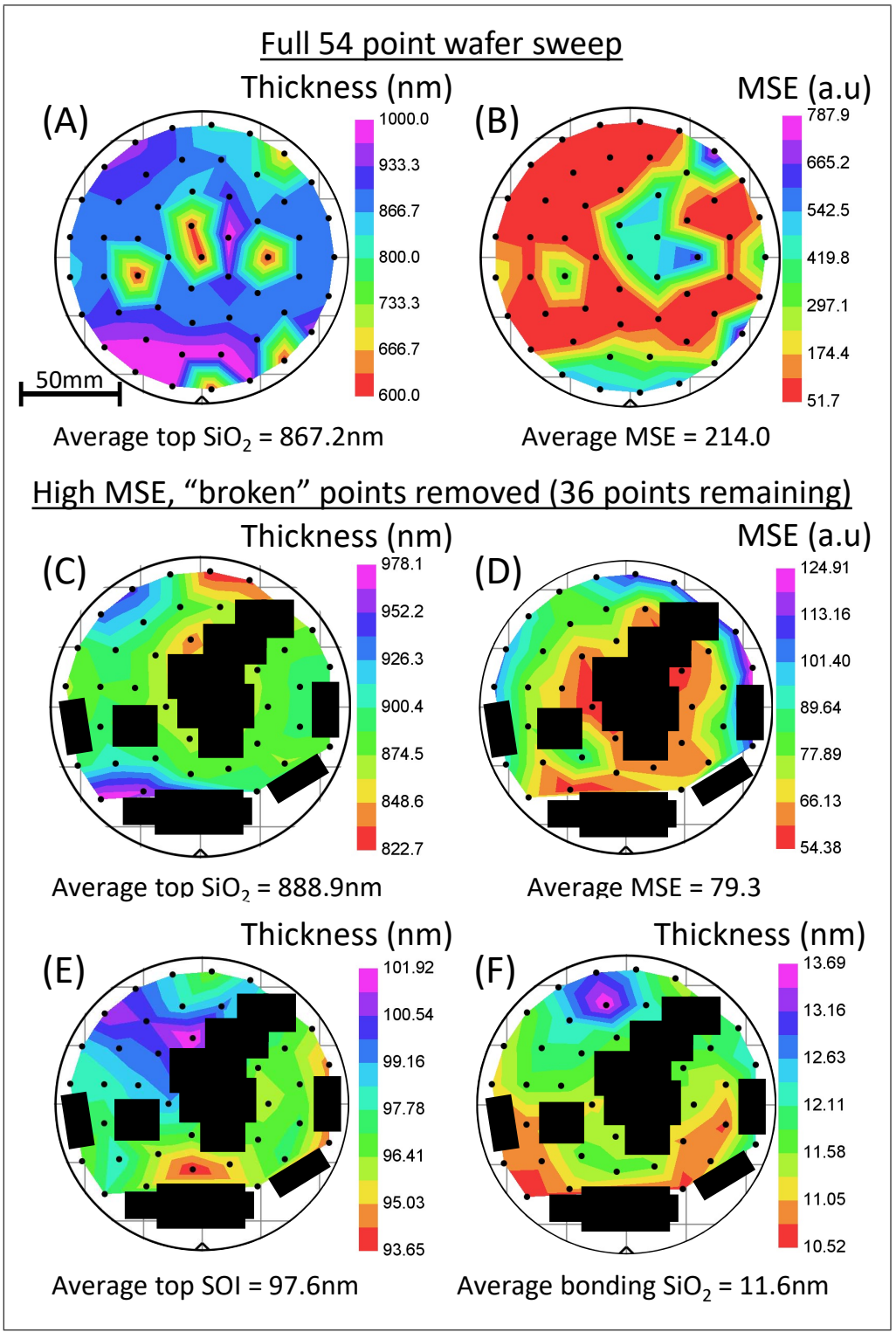


FIGURE 4.10: Ellipsometry data map of KOH etched bonded wafer (840 minute etch time). (A) shows the fitted value for top SiO_2 thickness across the wafer, with corresponding MSE at each point in (B). The high MSE "broken" points are removed and wafer maps for the top SiO_2, top SOI and bonding SiO_2 layer thicknesses are shown in (C), (E) and (F) respectively.

standard deviation = 31.0nm (Figure 4.10 (C)). Average top SOI thickness = 97.6nm, range = 8.3nm, standard deviation = 1.9nm (Figure 4.10 (E)). Average bonding SiO_2 thickness = 11.6nm, range = 3.2nm, standard deviation = 0.7nm (Figure 4.10 (F)). Average bottom SOI thickness = 99.7nm, range = 5.9nm, standard deviation = 1.2nm.

After KOH etching, the wafer pair #2 was diced and the top SOI BOx was removed using HF to produce a true double-SOI substrate on which horizontal-slot strip-waveguides and fin-waveguides could be fabricated. The fabrication process is detailed below:

1. Alignment marks were patterned using e-beam lithography and etched using ICP.
2. 12nm thermal oxide was grown in the furnace to protect the top surface.
3. The tapers, waveguides, multi mode interferometers (MMI) and MZI devices were patterned using e-beam lithography and etched using ICP. The bottom BOx was used as a stopping layer during this step.
4. The resist was then cleaned and the chips were thermally oxidised for 15s at 850C to grow ∼1-2nm thermal oxide on the sidewalls of the etched regions.
5. The chips were immersed in 1:200 HF for 1 min to remove 1-2nm sidewall oxide in an attempt to reduce sidewall roughness acquired during ICP etching.
6. The chips were then immediately placed in TMAH for 30 minutes to smoothen the sidewalls further as well as under and over-etch the dry etched top and bottom fins respectively to realise the unique 3D fin structure. After this step SEM images of the TMAH devices were taken. Figure 4.11 (a) shows the fin-waveguide structure. If the TMAH etching had worked as intended, the right top fins would have been etched away and this would have been apparent in the image. Figure 4.11 (b) shows an MMI from the same chip. The TMAH should have etched the curved waveguide exiting the MMI.
7. ZEP520A was then spun on the chips and baked at 180C for 3 minutes. This was followed by covering the chips with a thin-film conductive polymer (Espacer).
8. Grating couplers (GC) were patterned using e-beam lithography
9. The GCs were etched using ICP (using the 10nm bonding SiO_2 layer as a stopping layer).
10. The chips were stripped of resist and cleaned.

Before discussing the transmission loss results of these fin and strip waveguide devices, it is worth understanding the fabrication problems that led to less than optimal device performance. The first problem, already discussed, is that of TMAH wet etching not working. This meant the novel 3D fin design was not fully realised as designed, but it also

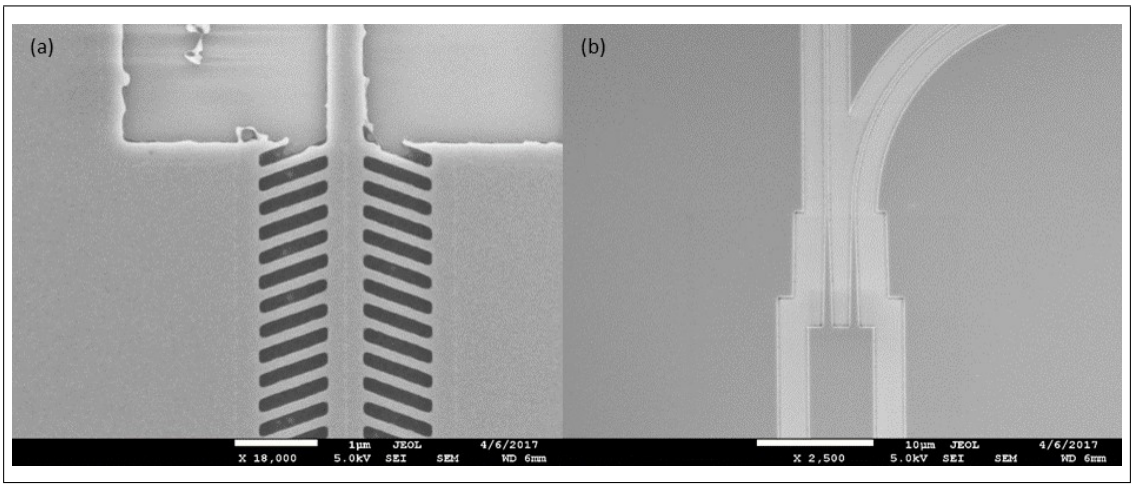


FIGURE 4.11: SEM images of (a) fin waveguide and (b) MMI on bonded double-SOI

meant that the sidewall roughness of the strip-waveguides was not completely removed to achieve atomically flat <111> crystalline plane sidewalls as designed. This remaining surface roughness (thermal oxidation and HF removal of SiO_2 does not completely remove surface roughness) will be a source of optical loss. A second cause of loss is the presence of nm scale voids in the bonding SiO_2. The O_2 or H_2 voids will have similar refractive index, n, to that of SiO_2 but they will deform the shape of the oxide layer and thus the $n(x, y)$ across the cross-section of the waveguide will change as a function of z. This will cause mode mismatch induced loss. The final and most significant contributing factor to increased optical loss is the imperfections in the double-SOI is caused by non-uniform KOH etching.

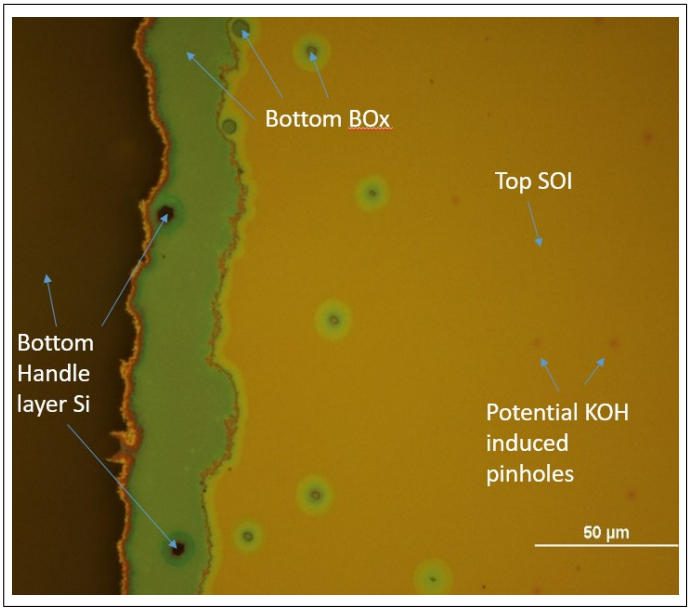


FIGURE 4.12: Surface of bonded double-SOI with large KOH blemish on the left, bordered by the bottom BOx. The small KOH "pin-holes" are present across the entire surface.

Figure 4.12 shows an optical image of the bonded double-SOI taken after top BOx removal. Obviously, any large blemishes where KOH has etched through to the bottom handle layer break any device passing through these regions, these devices can be discounted. However, small dot blemishes in Figure 4.12 labelled "Potential KOH induced pinholes" are present consistently across the entire surface, meaning there will be hundreds present on each device. If these pinholes are indeed etched through to the lower bottom SOI, they will cause parasitic optical loss in any waveguide devices fabricated through them, which explains the unexpectedly high transmission loss of strip-waveguides and multi mode interferometers (MMI) fabricated on this wafer, as will be shown in the next section.

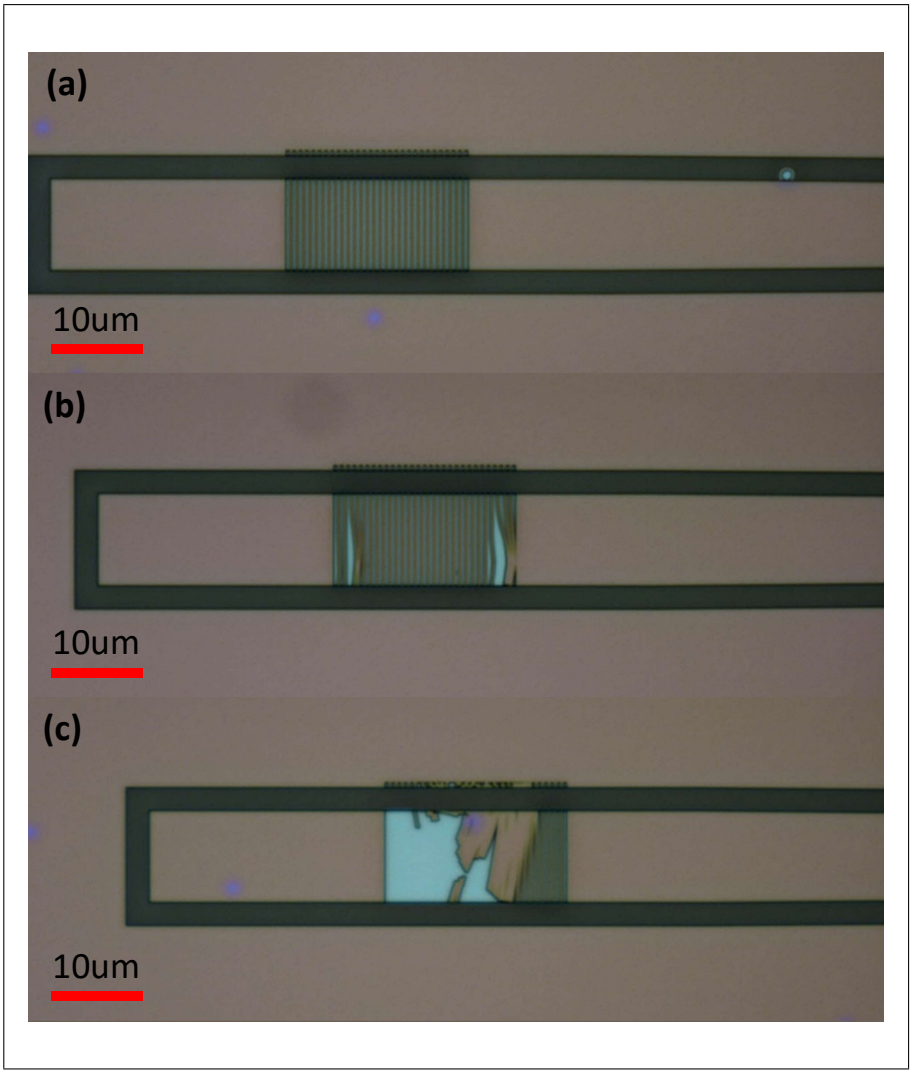


FIGURE 4.13: Optical images of grating couplers (GC) fabricated on bonded double SOI. (a) ideal GC, (b) and (c) "Peeling" grating couplers (GC).

Figure 4.13 shows optical images of three separate grating couplers (GC) in a range of conditions from ideal to completely broken, taken immediately before the final FOx16 (flowable oxide from *Dow Corning*) spinning on step. Figure 4.13 (a) is an ideally fabricated GC (the $>1\mu$m lateral misalignment is irrelevant, the design accounts for

this). ∼ 30% of measurable grating couplers (GC) appeared to be "peeling" (Figure 4.13 (b)). This could be caused by weak bonding adhesion (or voids) causing the thin GC fins to peel off the top oxide. This induces massive coupling losses for these devices. Many devices were completely unmeasurable (0% transmission) because the grating couplers (GC) had "peeled" off so much they could not couple any light from the fibre into the tapered waveguide. Figure 4.13 (c) shows this phenomenon.

4.2.2 Optical Characterisation

The transmission spectrum's of horizontal-slot strip-waveguides fabricated on the KOH thinned double-SOI substrate were measured using a TE polarized CW light source, to establish fabrication quality. A tunable (1530-1620) non-polarized laser source (output power 10mW (10dBm)) was TE polarized using a fibre polarization controller. Input and output partially-etched grating couplers were used to couple light from the flat-cleaved SMF into and out of the waveguide. Output power was measured using a photodetector connected to the output SMF. The design parameters and calculated 1st order Bragg condition λ (target peak coupling efficiency λ) are presented in Figure 4.2. The raw transmission spectrum's, as well as the minimum loss for each device and the extrapolated loss (dB/mm) and total coupling loss (dB), are presented in Figure 4.14.

Table 4.2: GC designs and target peak coupling efficiency λ

GC Design #	Fill-Factor	Λ (nm)	Calculated 1st Order Bragg Condition λ			Measured Peak Coupling λ
			14.5°	16.0°	17.5°	
1	0.5	690	1554	1536	1519	1541.7
2	0.5	740	1666	1648	1629	1612.4
3	0.5	790	1779	1759	1739	1619.2
4	0.7	660	1568	1552	1535	1536.0

The transmission losses of horizontal-slot strip-waveguides of lengths 250μm, 500μm, 1000μm and 2000μm were measured. Transmission loss per mm (dB/mm) and total coupling loss was extracted using minimum loss measured for each device. Transmission loss of 3.36dB/mm was extracted for GC4 devices, with a total coupling loss of 16.8dB (8.4dB per grating coupler). The minimum loss graphs show a weak correlation between measured loss and the linear fit, demonstrating that the quality varies considerably between waveguides which were fabricated on the same chip. These inconsistencies can be explained by the presence of ∼1μm scale KOH induced pinholes scattered across the substrate. Any waveguides that are aligned directly over a pin-hole exhibit very large scattering at that point, whereas waveguides that avoid pinholes do not. If, for example, the anomalously high loss 2mm GC1 waveguide is excluded from the loss/mm fit, the extracted loss/mm becomes 3.1dB/mm (from 6.5dB/mm), and if both 2mm waveguides are excluded, the extracted loss becomes 0.7dB/mm. It is unproductive however to speculate on the validity of loss/mm results from these measured waveguide, as it is difficult

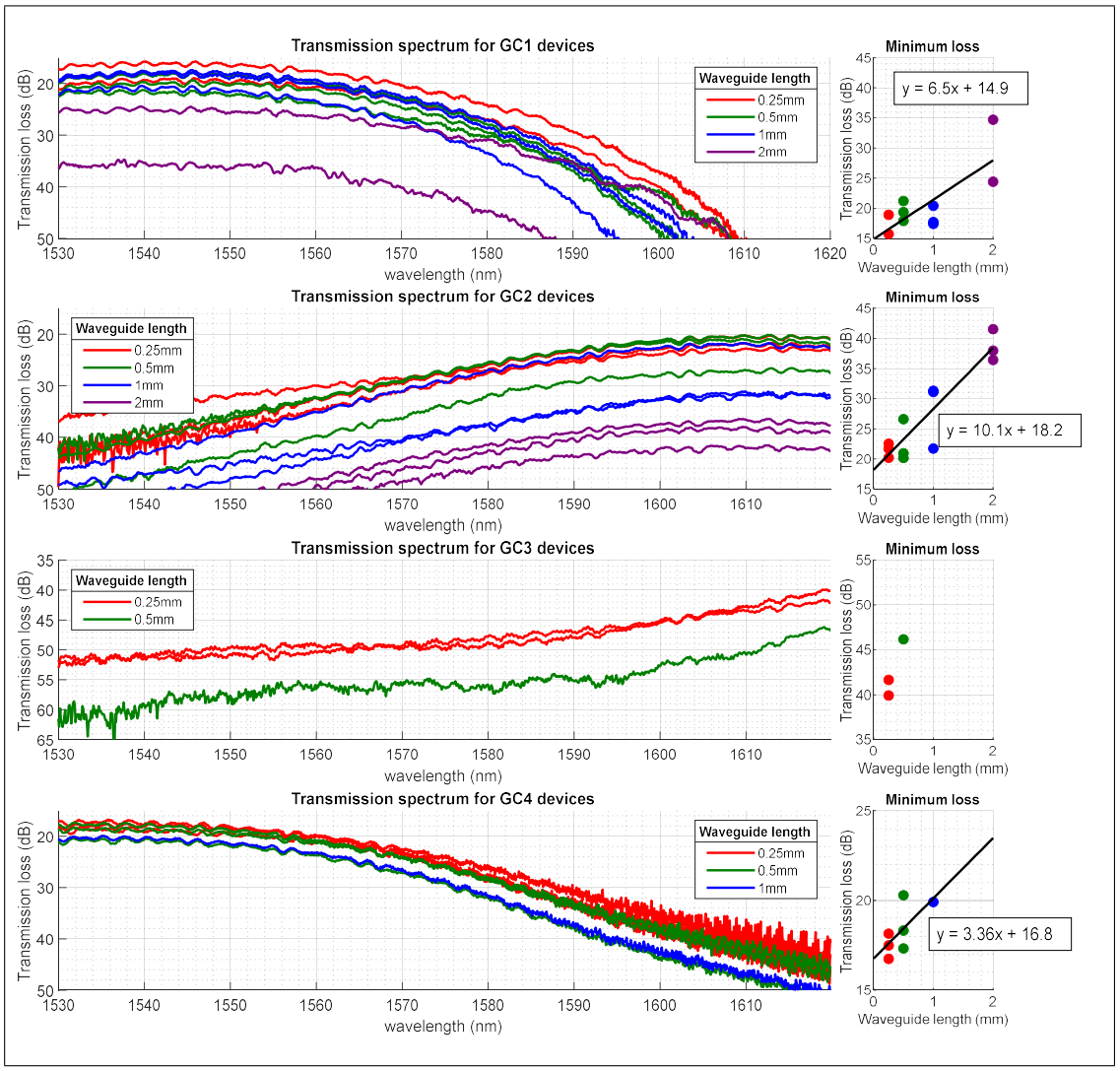


FIGURE 4.14: Horizontal-slot strip-waveguide fabricated on KOH thinned double-SOI transmission spectrum. Raw transmission spectrum for each measured device on the left and corresponding extracted minimum loss on the right. The overlaid black line on the minimum loss plots is the linear best fit for all points. The overlaid equation corresponds to the linear best fit. GC3 coupling efficiency was too low in this spectrum, therefore no linear fit for GC3 measured devices.

to establish whether the primary loss mechanism for particular waveguide is the intrinsic loss/mm, or the anomalous pin-hole induced loss point/points. This fabrication can be considered a provisional success, and reveals a key area where fabrication optimization must be employed to remove KOH induced pin-holes.

4.3 Conclusion

Direct SiO_2/SiO_2 bonding has been established and MOScap devices have been fabricated which exhibit expected CV characteristics and a gate oxide thickness between

13-14nm. This 30-40% increase in effective gate oxide thickness can be explained by the presence of nm scale gas voids in the oxide. However, measured thickness of the bonded double-SOI wafer (using ellipsometry post handle layer removal) shows an oxide thickness of 12nm, only a 20% increase in expected thickness. In conjunction with the good C-V characteristics, this 30-40% increase in effective gate oxide thickness is acceptable, and proves the bonding quality is sufficient to pursue active devices.

A double-SOI was fabricated using bonding and KOH wet etching handle layer thinning down, on which horizontal-slot strip-waveguides were fabricated. A range of strip-waveguides were measured with variable transmission loss, which can be attributed to KOH induced pinholes and potentially voids or points of low adhesion which caused grating couplers (GC) to "peel". The lowest, most reliable optical transmission loss for the horizontal-slot strip-waveguide was 3.3dB/mm. As discussed previously, there are several contributing factors to this high transmission loss result. Addressing these factors to reduce horizontal-slot strip-waveguide loss and realise the up/down 3D fin-waveguide will be the focus of the next chapter.

Chapter 5

Fin Waveguides and Passive Mach-Zehnder Interferometer

After the relative success of the initial bonding tests, gate oxide quality/thickness characterisation, and horizontal-slot strip-waveguide fabrication and characterisation on bonded double-SOI, the next step was to optimize that process and realise the fully 3D horizontal-slot fin-waveguide using wet etching. In 4.1.2 it was established that a pre-bonding recipe involving wet etching only (i.e no RIE etching due to increased surface contamination risk), and a bonding step involving applied pressure under moderate temperature followed by high temperature annealing, provided the best electrical quality bonding SiO_2 layer (Figure 4.4 and Figure 4.5 showing expected CV operation for devices having undergone these bonding processes). It was also established that although KOH etching is an effective method for removing the top Si handle layer from a SOI/SOI bonded wafer pair, this introduces unacceptable optical-loss inducing "pin-hole" defects across the substrate (shown in surface image in Figure 4.12). It is for this reason that ICP dry etching was chosen as the method for removing the top Si handle layer in the fabrication laid out in this chapter. This chapter will detail the unique fabrication process developed to realise the horizontal-slot fin-waveguide, and then present the optical transmission characterisation results of these devices.

5.1 Fabrication

The process flow to realise the double-SOI on which the waveguides were fabricated was similar to the one outlined in 4.2.1 and Figure 4.6. However, there were some key important differences which are highlighted in the process flow below:

1. Two undoped (110) SOI (330n SOI, 2μm BOx) wafers were thinned down using thermal oxidation and HF wet etching to SOI = 114.6nm, 98.6nm (the top SOI

layer would be thinned down through several thermal oxidation steps to ∼100nm during horizontal-slot fin/strip-waveguide fabrication).

2. The wafers were bonded using a similar process to that used for the MOScap devices outlined in 4.1, with a targeted bonding oxide thickness of 10nm.

3. The bonded wafer was annealed at low temperature (450°C) under an applied pressure of 67kPa in vacuum for 2 hours in an EVG520 wafer-bonding machine, followed by a high temperature anneal (1000°C) in atmospheric conditions for 3 hours.

4. The back 2μm oxide was removed in 7:1 HF.

5. The 675μm handle layer was thinned down using ICP (as opposed to pin-hole inducing KOH). ICP recipe: SF_6 = 200; Ar = 35sccm; ICP forward power = 2500W; RF Forward power = 10W; DC bias = 40V.

6. The top handle layer was thinned down to 115μm over 120 minutes etch time (4.6μm/min Si etch rate). At this point, the sample had to be cleaved into 3cm x 4cm chips for the sake of the ICP tool.

7. The wafer was diced (protective resist was applied, wafer diced, resist was stripped) and a further 25 minutes of ICP etching was applied until the entire Si handle layer was removed.

8. The chips were cleaned using ACE and IPA and the top BOx was removed using HF 7:1, revealing the double-SOI structure with stack handle Si/BOx/Si (100nm)/SiO_2 (11nm)/Si (110nm).

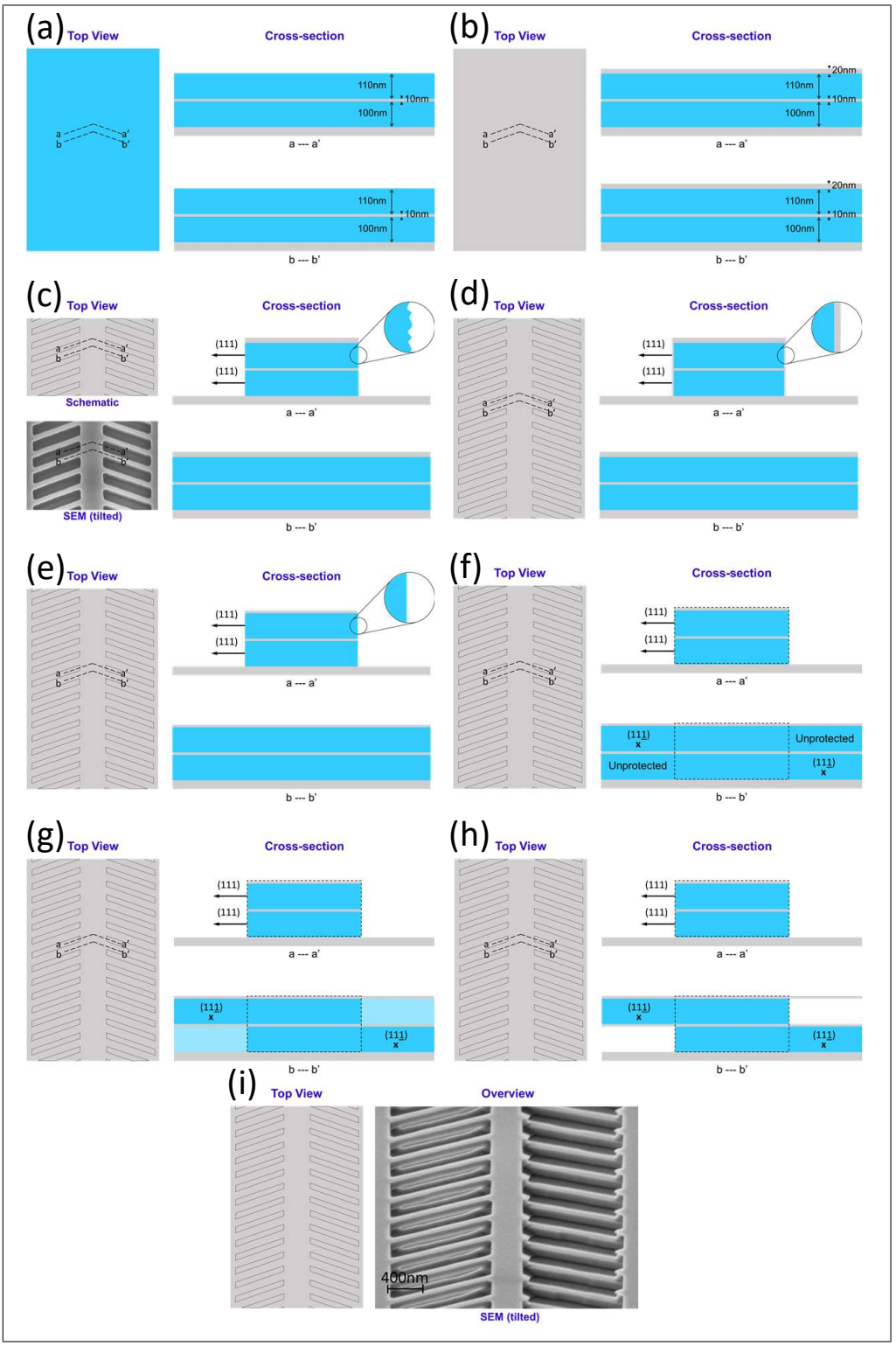


FIGURE 5.1: Top-view and cross-sectional view of process flow showing fabrication of horizontal-slot fin-waveguide from bonded double-SOI. (a) Double-SOI. (b) Grow thermal oxide. (c) Conventionally dry-etch strip and fin-waveguides (SEM of ICP etched fin-waveguide shown). (d) Thermally oxidizer growing 5nm SiO_2 on the <111> crystal orientation sidewalls. (e) Sidewall SiO_2 removed using HF. (f) shows the protected (111) sidewalls (marked x) and the unprotected sidewalls. (g) TMAH applied. (h) Unprotected sidewalls etched whilst protected fins remain intact. (i) Tilted SEM overview image of fin-waveguide.

From this double-SOI, horizontal-slot fin-waveguides were fabricated using the process detailed below, and presented schematically in Figure 5.1:

1. E-beam lithography and ICP etching was used to conventionally pattern and ICP dry-etch horizontal-slot strip and fin-waveguides, MZI passive devices.
2. After waveguide sidewalls were dry etched, the samples were thermally oxidised (5nm SiO_2 on the (110) surface, expected 7.5nm on (111) sidewall).
3. PMMA resist was applied and etch windows were opened around the horizontal-slot fin-waveguides. The samples were immersed in HF to remove the oxide; this was immediately followed by immersion in room temperature TMAH (25% concentration) for 20 minutes, to etch fins. This serves the dual purpose of smoothening the waveguide sidewalls (LOCOS, outlined in 3.3.6) and over/under-etching non-<111> crystal plane protected fin sidewalls (outlined in 3.1.3 with TMAH etching outlined in 2.3.2).
4. SEM images were taken of the fin-waveguide structure after 20min TMAH etch time (Figure 5.2 (a) and (b)). TMAH etching is clearly visible, but further etching was required to fully etch the fins.
5. The HF and TMAH steps were repeated. HF etching targeting 3nm oxide removal was applied, followed by 85minutes room temperature TMAH (25% concentration) etching (100nm just etch in of <100> crystal plane + 500% over-etch. 30nm <111> crystal plane etching is expected, thinning fins and the waveguide slightly)). This TMAH step was fully successful, as SEM images show (Figure 5.2). The <111> crystal plane etch rate$\sim$0.3nm/min. The <100> crystal plane etch rate$\sim$5.5nm/min. The etch rate is assumed to be uniform, as it is a wet etch, and the total etched sample area is small (all devices within 20mm x 30mm rectangular area).
6. HF was applied to remove free standing SiO_2 (seen in Figure 5.2 (c-f)). The results of this are shown in Figure 5.3.
7. Grating couplers were patterned using electron-beam lithography and partially etched using the horizontal-slot SiO_2 as a hard stopping layer) (Figure 5.4.
8. The final step was to coat the device in a protective dielectric cladding. PMMA was chosen (n = 1.48), which had a baked thickness $\sim$1.8μm.

5.2 Optical Characterisation

Three different types of devices were measured; horizontal-slot strip-waveguides, horizontal-slot fin-waveguides, and passive Mach-Zehnder interferometers (MZI) with fin "phase

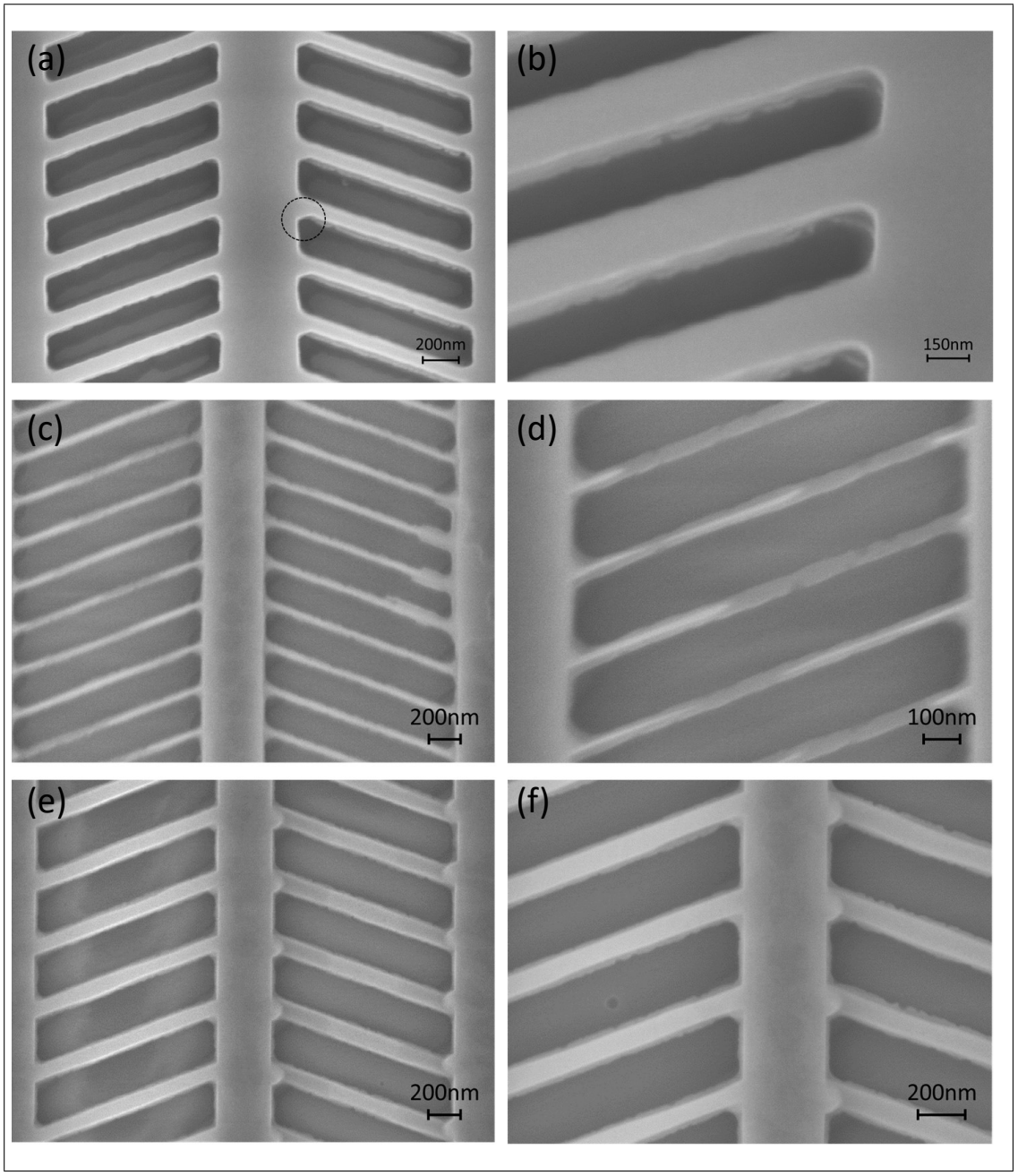


FIGURE 5.2: (a) and (b) SEM images of double-SOI fin-waveguide after 20min total TMAH etching. Defined (111) surface has been highlighted in (a). TMAH etching has occurred but 20 minutes was not enough time to fully etch fins. (c-f) SEM images of double-SOI fin-waveguide after 105min total TMAH etching. (c) and (d) show fin design #1 (W_{fin}=100nm). It is apparent from (d) that sections of the fins that were meant to be un-etched (defined by (111) sidewalls) have etched away completely, and only either the 10nm bonding oxide or the top oxide (light grey) remains. (e) and (f) show fin design #4. These fins were under and over-etched correctly, and a ∼20nm oxide remains free-standing either side of the fins.

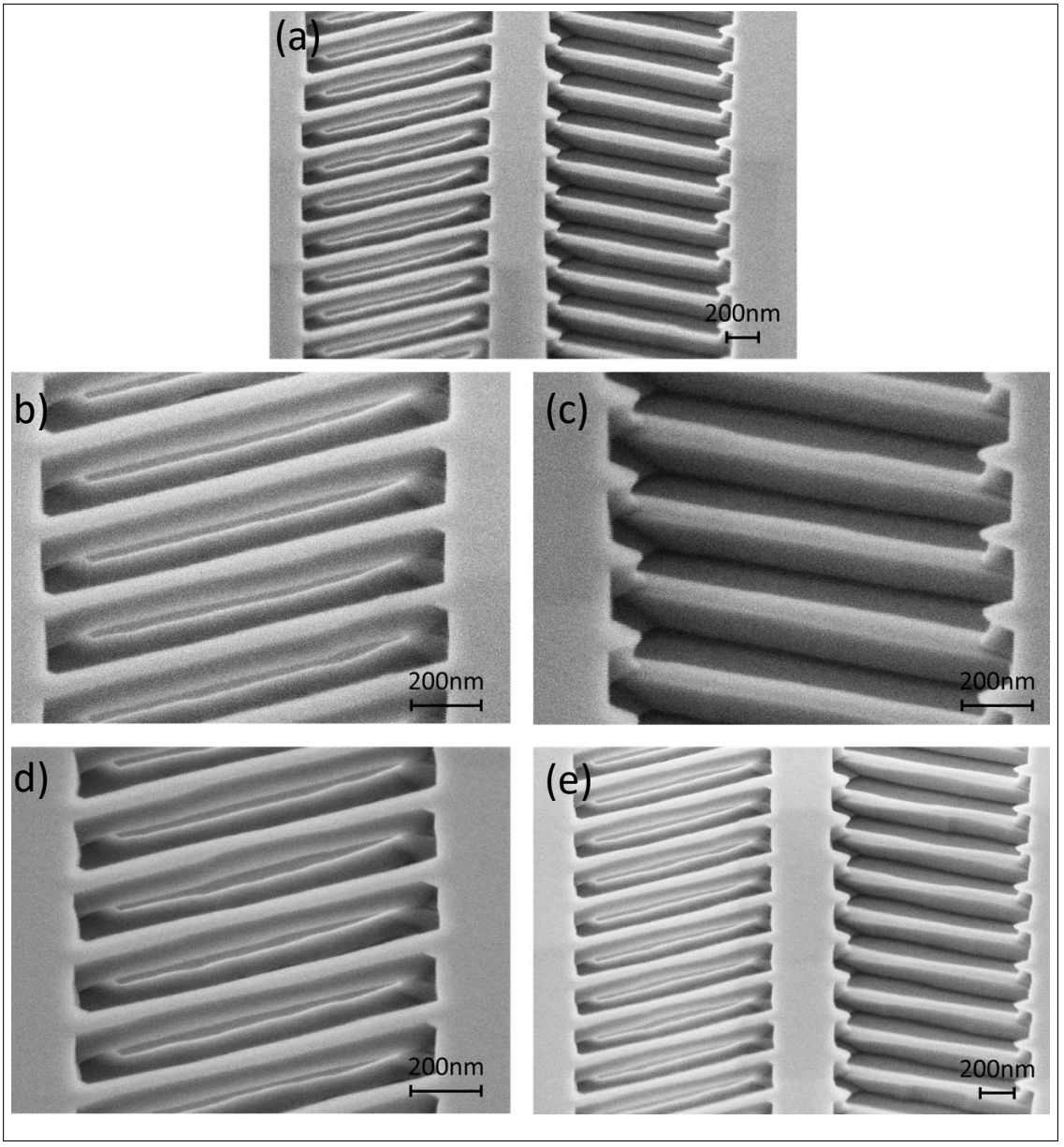


FIGURE 5.3: SEM images of fin-waveguides after full TMAH etch and subsequent oxide removed fin-waveguide. (b) and (c) close up of left fins (under-etched) and right fins (over-etched) respectively. (d) and (e) were taken using "line average stabilization". This gives the misleading impression that the waveguide and fins are curved, however, it does provide higher resolution and confirms more clearly how the top fins have indeed been fully under-etched.

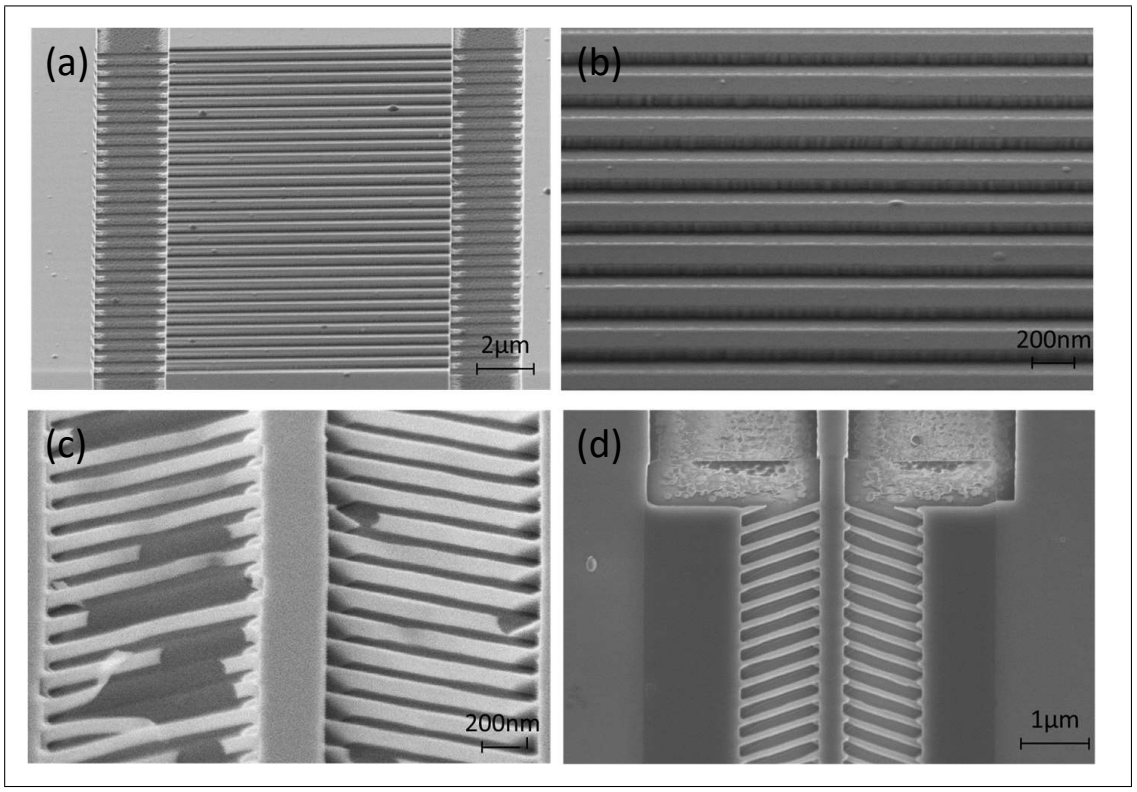


FIGURE 5.4: (a) and (b) SEM of dry etched GC (etch depth=100nm, stopping on bonding oxide layer). No "peeling" or significant defects observed in any grating couplers (GC). (c) broken narrow width fins (taken at ∼54°tilt) and (d) point where the tapered input strip-waveguide ends and the fin-waveguide begins. The abrupt introduction of fins as well as the PMMA window misalignment leads to several problems. For example, because the PMMA window extends ∼700nm along the input strip-waveguide taper, there is an abrupt defect/discontinuity which will be a source of scattering induced loss. However, these problems can be easily solved in the next design.

shifter" sections. For characterization of device transmission loss, CW TE polarized light was coupled through the grating couplers (GC) from SMFs into the device. The wavelength of the CW light source was swept from 1525nm-1625nm and transmission power was measured using a photodetector connected to the output SMF.

Strip-Waveguides and Fin-Waveguides

Three devices of each waveguide length (250μm, 500μm, 1000μm and 2000μm) were measured. The lowest transmission loss value for each measured device was plotted as a function of waveguide length. Figure 5.5, Figure 5.6 and Figure 5.7 show the transmission loss results for strip-waveguide devices and fin-waveguide devices, using GC#1, GC#2 and GC#4 respectively. The measurement results are shown before (left) and after (right) fibre input angle optimization to maximize coupling efficiency. The black line indicates the best linear fit, and the loss (dB/mm) and coupling loss (dB) values overlaid on the graph are refer to the gradient and intercept values of this line respectively. Because

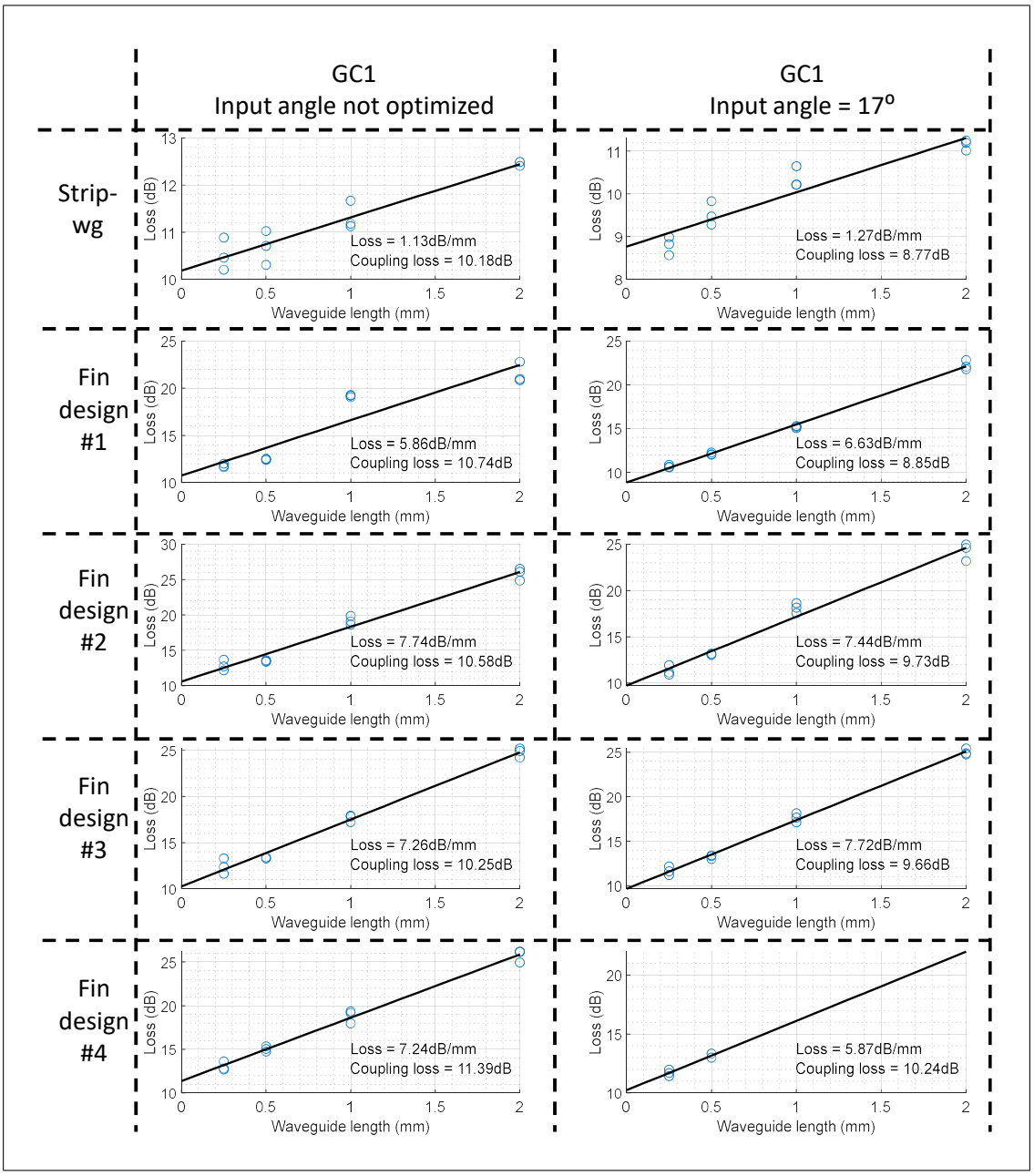


FIGURE 5.5: Optical transmission loss of strip and fin-waveguide devices with GC#1

GC#3 was designed for peak efficiency at λ>1739nm, coupling loss was very high in the measurement range available, and these results have therefore been omitted.

The minimum transmission loss of three GC#4 devices with 0μm waveguide (i.e. entire device consists of a 500μm taper in and a 500μm out) are shown as a function of fibre input angle in Figure 5.8 (c). The black line represents the best polynomial fit to the data. The minimum coupling loss of 7.85dB occurs for input angle=19°, which equates to a coupling loss of 3.9dB/GC. The raw transmission loss spectrum for this device, as

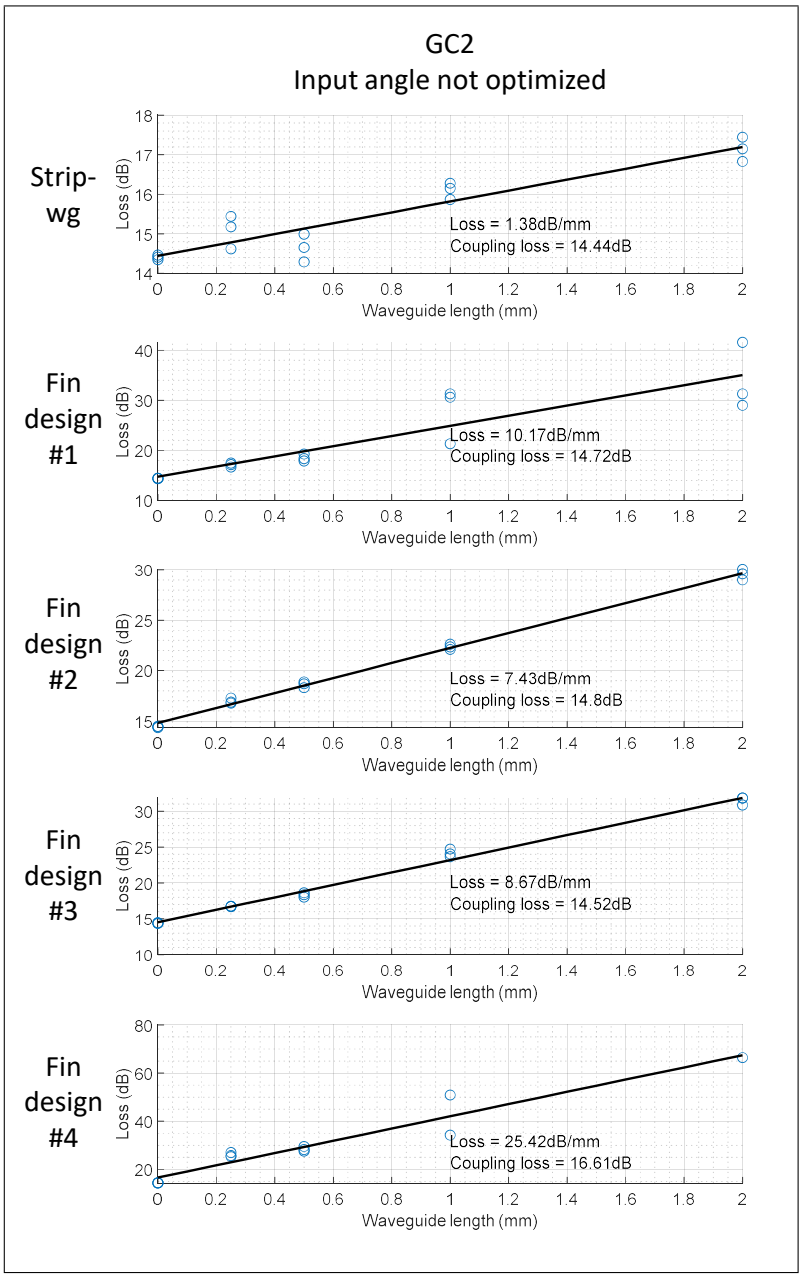


FIGURE 5.6: Optical transmission loss of strip and fin-waveguide devices with GC#2

well as the same device at input angle 15°, 17° and 21° is shown in Figure 5.8 (a), with a close-up showing the coupling loss between 7.85dB-10dB for λ=1535nm-1570nm (b).

MZI Devices Transmission Loss

Two designs of MZI devices were fabricated and characterised. One with a phase-shifter arm length difference (ΔL_{arm})=200μm, the other with ΔL_{arm}= 400μm. A schematic of both devices is shown in Figure 5.9. The design for the 1x2 MMI coupler is presented in Figure 5.10 The fin design#2 was used for the 500μm phase-shifter fin-waveguide section.

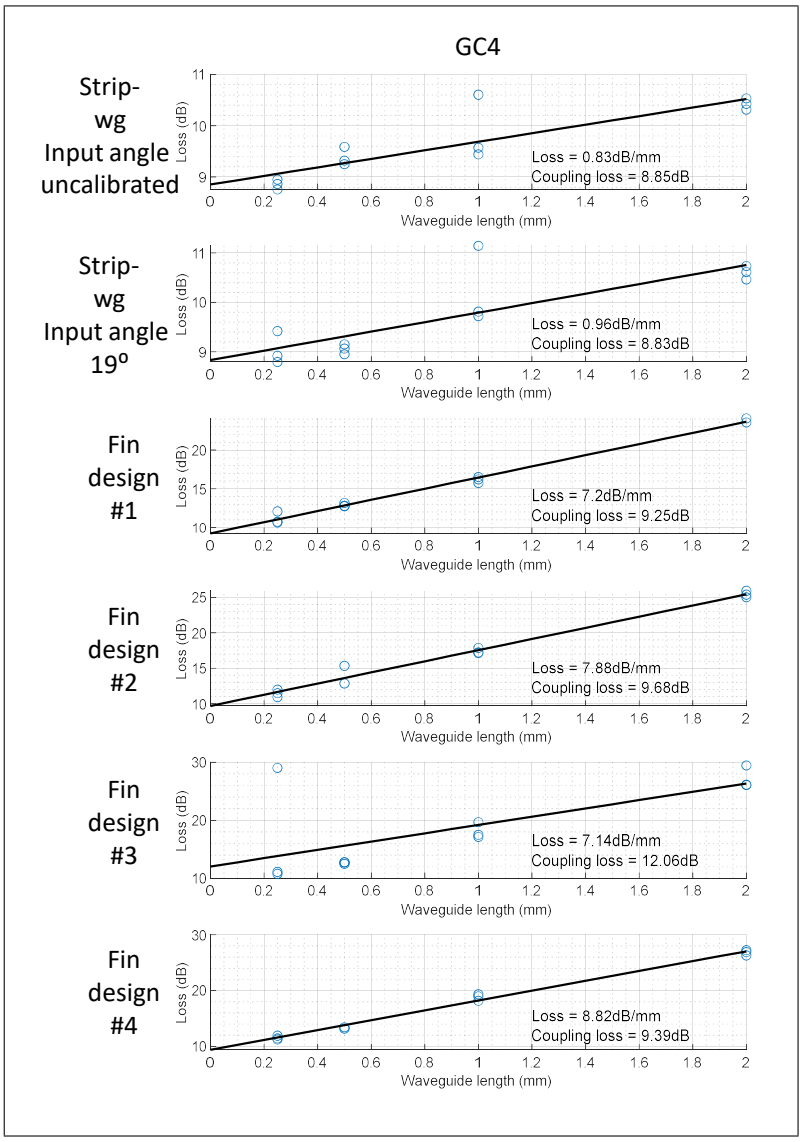


FIGURE 5.7: Optical transmission loss of strip and fin-waveguide devices with GC#4

Transmission loss measurements were taken for the MZI devices, using the same set up as that used for the strip and fin-waveguides. As can be seen in Figure 5.11, the free spectral range (λ_{FSR}) between transmission loss "peaks" (caused by π shift destructive interference when EM waves from both arms recombine in the output MMI) is significantly lower in the ΔL_{arm}=400μm device, although the extinction coefficient is the same, implying perfect destructive interference. The devices with GC#4 show similar results to those with GC#1, except overall transmission decreases at Λ>1570nm. This is due to the design of GC#4 being optimized for operation between Λ=1530-1570nm, and exhibiting low coupling efficiency above this λ.

Simulation results predict a photonic bandgap to be present with fin waveguide, design #4 (W_{fin} = 200nm, Λ_{fin} = 400nm), with the stop band starting at λ ~1579nm. This is clearly observed for the 250μm long fin-waveguide devices using GC#4, as can be seen for all 3 devices in Figure 5.12. Thephotonic bandgap (PBG) has shifted for GC#1

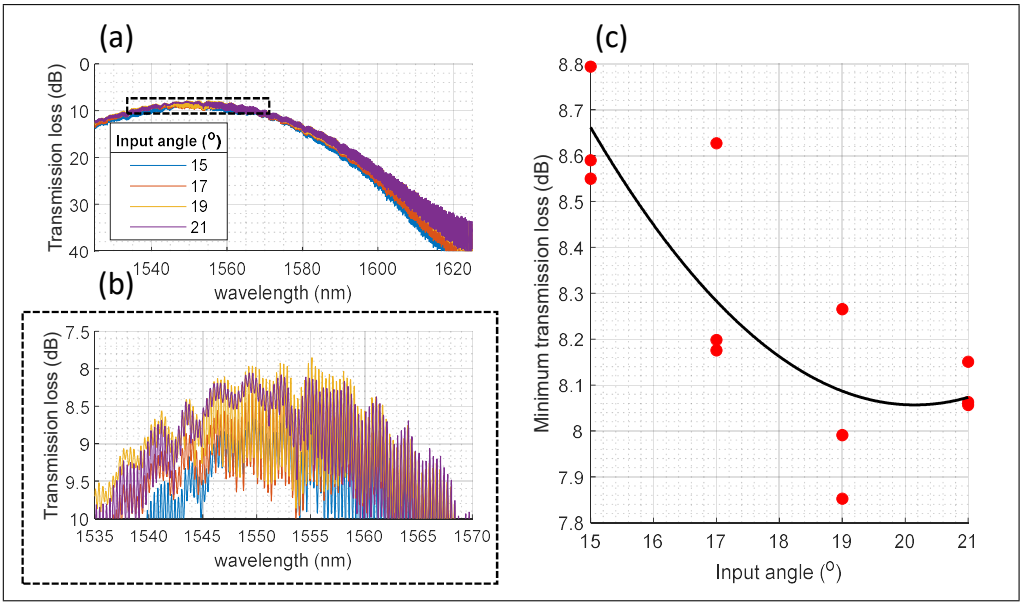


FIGURE 5.8: Coupling loss for GC#4 as a function of fibre input angle.

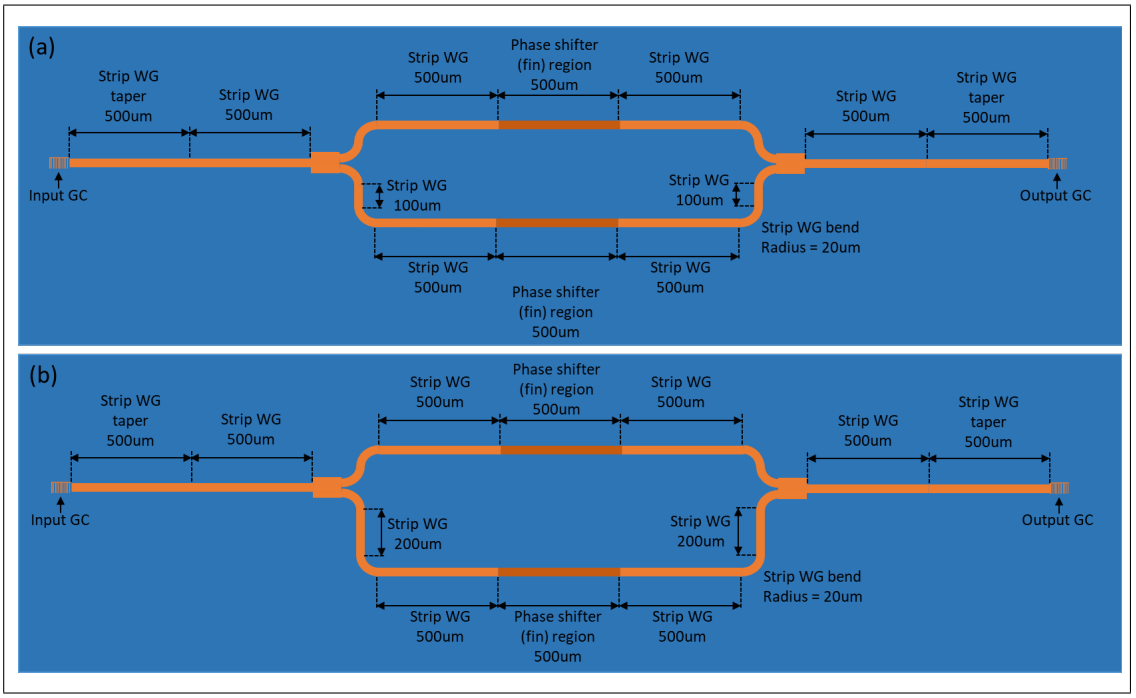


FIGURE 5.9: Design of (a) ΔL_{arm}=200μm and (b) ΔL_{arm}=400μm passive Mach-Zehnder interferometers (MZI) fabricated on bonded double-SOI with TMAH wet etched phase shifter fin region. Fin design #2 (fin width = 150nm, period = 300nm) used in shifter region.

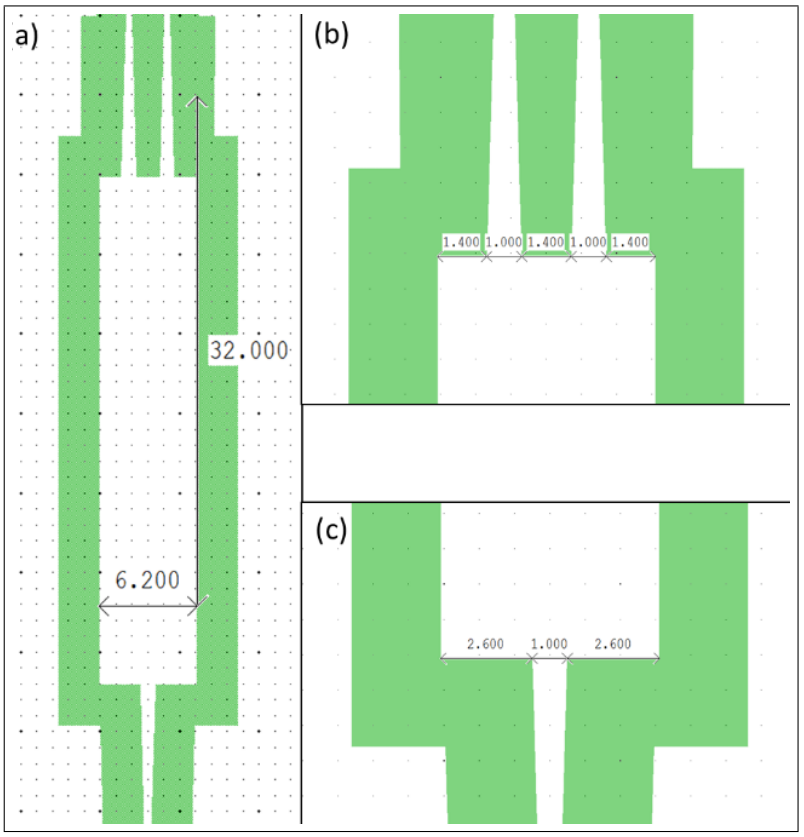


FIGURE 5.10: Design of MMI used in MZI devices. (a), (b) and (c), overall MMI, output and input respectively

devices and GC#2 to λ ~1602nm and λ ~1584-1586nm respectively. This is explained by fabrication errors and fabrication non-uniformity across the chip.

5.3 Conclusion

Strip-waveguides and fin-waveguides (with and without pseudo-PhC fins and associated PBG), as well as passive MZI devices have been fabricated on bonded double-SOI. The fins were successfully under and over-etched simultaneously using a unique combination of mirrored (111) Si crystallographic plane alignment of the top and bottom SOI layers, and selective TMAH etching. SEM images confirming this have been presented. This is the first demonstration of under-etching a lower SOI layer independently of the top SOI layer, to achieve a horizontal-slot fully-c-Si waveguide with independent up/down contact arms. The lowest extracted transmission loss for each of the fin-waveguides is presented in Figure 5.2. The lowest measured coupling loss (per GC) is presented in Figure 5.2.

A shown in Figure 5.11, passive MZI devices also exhibit low enough loss to pursue active devices, with the minimum passive loss ~20-22dB. The introduction by ion implantation of low concentration ($1x10^{18}cm^{-3}$) charge carriers phase-shifter section of the

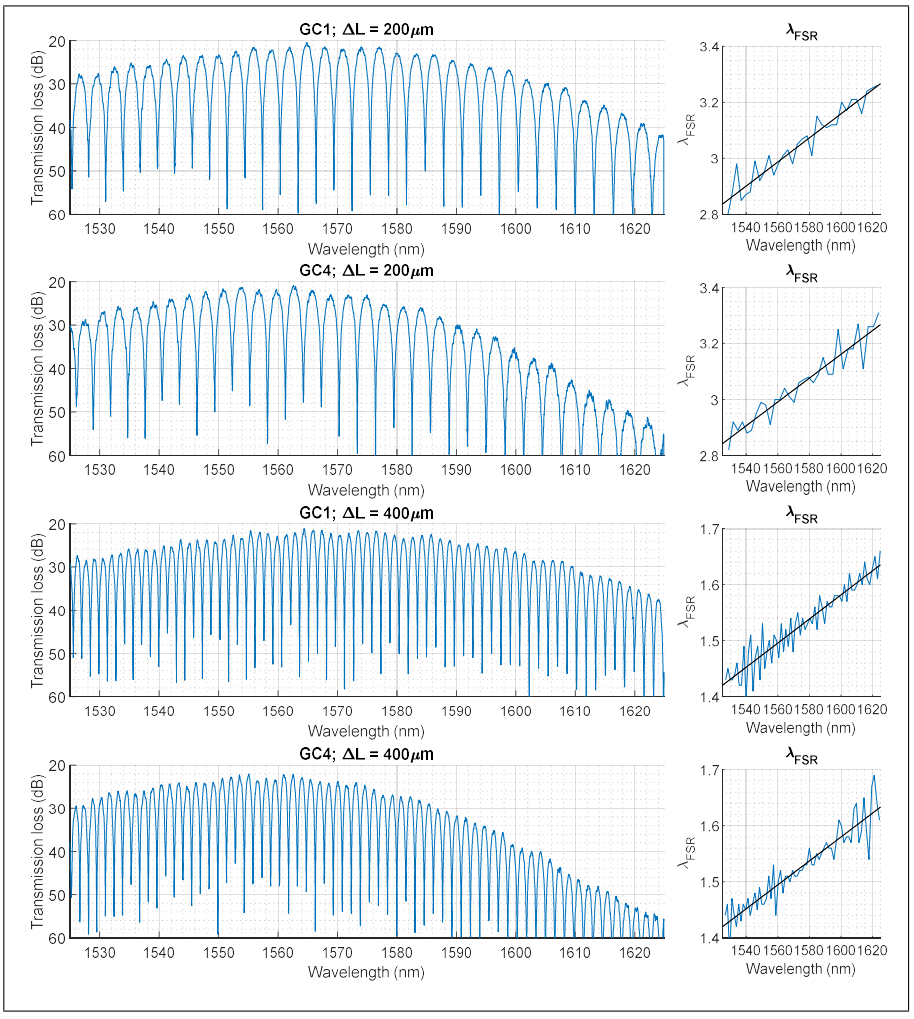


FIGURE 5.11: Passive MZI transmission spectrum. Four devices shown, GC#1 and GC#4 with ΔL_{arm}=200μm, and GC#1 and GC#4 with ΔL_{arm}=400μm (top to bottom). To the right of each transmission spectrum is the corresponding free-spectral-range wavelength λ_{FSR} as a function of λ (blue line) with the black line representing to best linear fit.

TABLE 5.1: Summary of coupling efficiency for different waveguide designs

Grating coupler design	Coupling loss (dB/GC)	Max coupling efficiency \lambda (nm)
#1 (fill-factor = 0.5, Δ = 690nm)	4.39	1564
#2 (fill-factor = 0.5, Δ = 740nm)	7.22	1624
#4 (fill-factor = 0.7, Δ = 660nm)	3.93	1555

device is expected to increase the loss by only ∼1dB/mm, acceptable considering the L_{shifter} is only 500μm long. The demonstrated loss is satisfactory, however, there are several major sources of loss which could be addressed in future. For example, a sharp discontinuity caused by TMAH etching is observed at the interface between the tapered strip-waveguide and the fin-waveguide (Figure 5.3 (d)). This could be overcome by changing the design slightly without changing the established fabrication process. One area of fabrication optimization which could be pursued is the optimization of TMAH

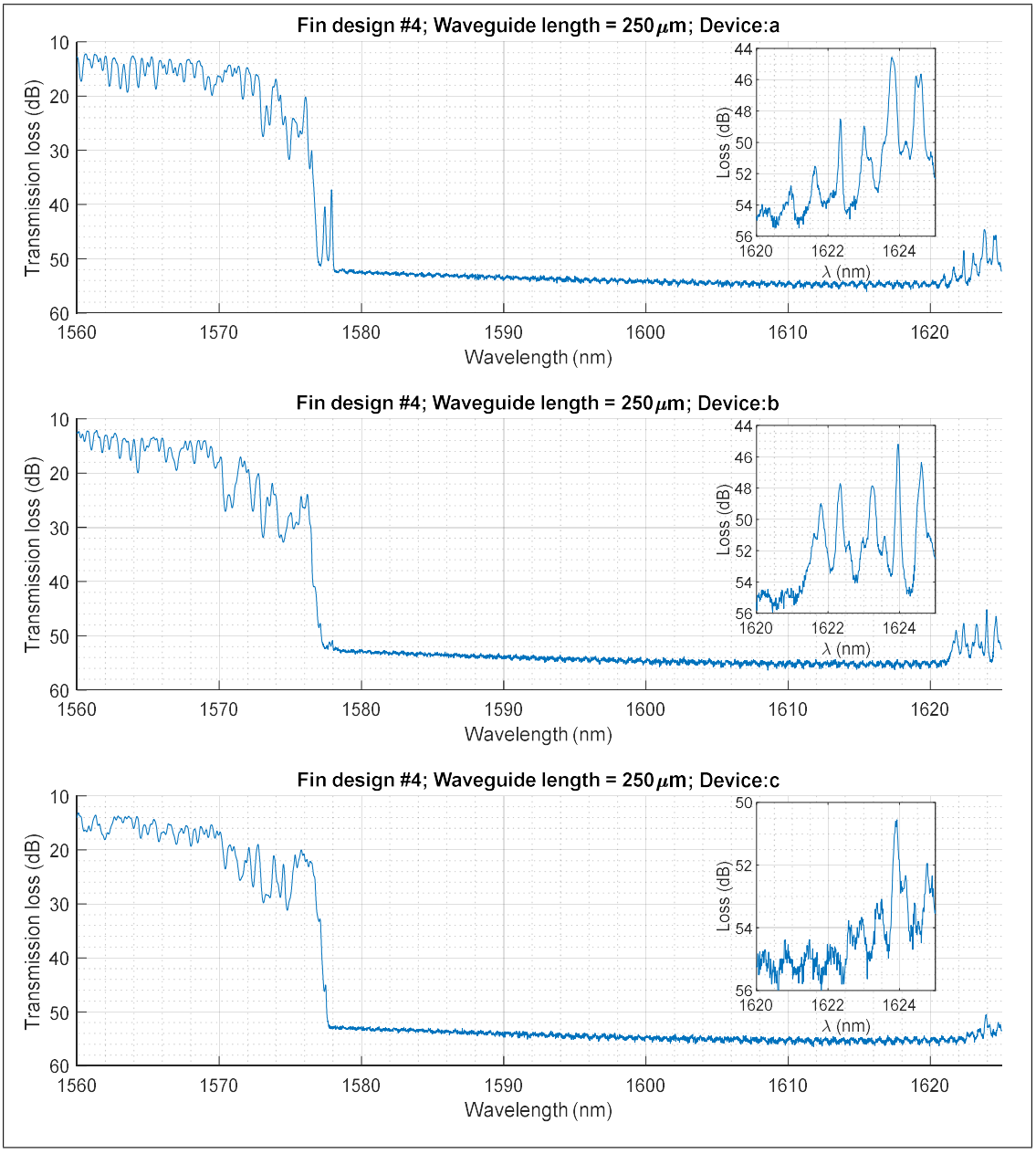


FIGURE 5.12: Transmission spectrum results for fin-waveguide (design #4, GC#4) fabricated on bonded double-SOI, clearly showing a PBG at the correct wavelengths predicted by simulation (λ ~1579nm-1620). The inserts show a close-up of the upper end of the stop band of their respective device.

TABLE 5.2: Summary of transmission loss for strip and fin-waveguides

Waveguide design	Coupling loss (dB/mm)	Passive loss expected in 500μm long phase-shifter arms (dB)
Strip-waveguide	0.83	
Fin-waveguide#1 (fin width = 100nm, Δ = 300nm)	6.63	3.32
Fin-waveguide#2 (fin width = 125nm, Δ = 250nm)	7.43	3.72
Fin-waveguide#3 (fin width = 150nm, Δ = 300nm)	7.14	3.57
Fin-waveguide#4 (fin width = 200nm, Δ = 400nm)	7.24	3.62

etch-time. In this case ∼500% over-etch was applied. This was done to guarantee full fin suspension and over-under etching, however, it does cause the strip-waveguide section of the fin-waveguide to shrink, causing periodic bumps where the fins are positioned. Iterative design/fabrication improvements can certainly be made in this area.

Chapter 6

Vertical-slot Waveguide and Accumulation Modulator

This chapter will present the fabrication of the passive vertical-slot rib-waveguide. This will include the various fabrication problems which needed to be solved, the most significant of which was how to adequately deposit and recrystallize a-Si which was necessary to realise the vertical-slot needed to fabricate the rib-waveguide. The chapter will then go on to the present the characterisation results of the passive vertical-slot rib-waveguide in the form of transmission loss results. Finally the characterisation of the active vertical-slot rib-waveguide accumulation modulator will be presented, in the form of the transmission spectrum change under applied DC bias (steady state), the phase modulation and modulation efficiency, and the high-speed analysis, where the device was modulated up to 25Gbit/s exhibiting a 3.5dB extinction ratio and a modulation efficiency of 1.53Vcm.

6.1 Vertical-Slot Rib-Waveguide Characterisation

Before pursuing an active accumulation modulator based on a new vertical-slot rib-waveguide design, it was first necessary to characterise the waveguide design passively, to establish its suitability. If the passive vertical-slot rib-waveguide was unrealisable due to fabrication problems or demonstrated unreasonably high transmission loss, the design/fabrication would have to be reconsidered before it could be included in the active modulator. This section will be split into a discussion of the vertical-slot and vertical-slot rib-waveguide fabrication challenges (6.1.1), and a discussion of the transmission results 6.1.2.

6.1.1 Fabrication

The fabrication process for the vertical-slot rib-waveguide is broadly outlined in section 3.2.3 (particularly Figure 3.11 and Figure 3.10). What will be discussed here is a detailed description of the a-Si deposition and recrystallization required for the fabrication of the vertical slot, followed by a detailed description of the total fabrication process. As shown clearly in Figure 3.11, a wide trench must be etched into the SOI layer into which a-Si can be deposited. A variable parameter of interest was the trench width (W_{trench}). Two values for W_{trench} were chosen for investigation, W_{trench}=500nm and W_{trench}=2μm. The positioning of this trench as well as the design of the entire passive device used for passive characterization devices is shown in Figure 6.1.

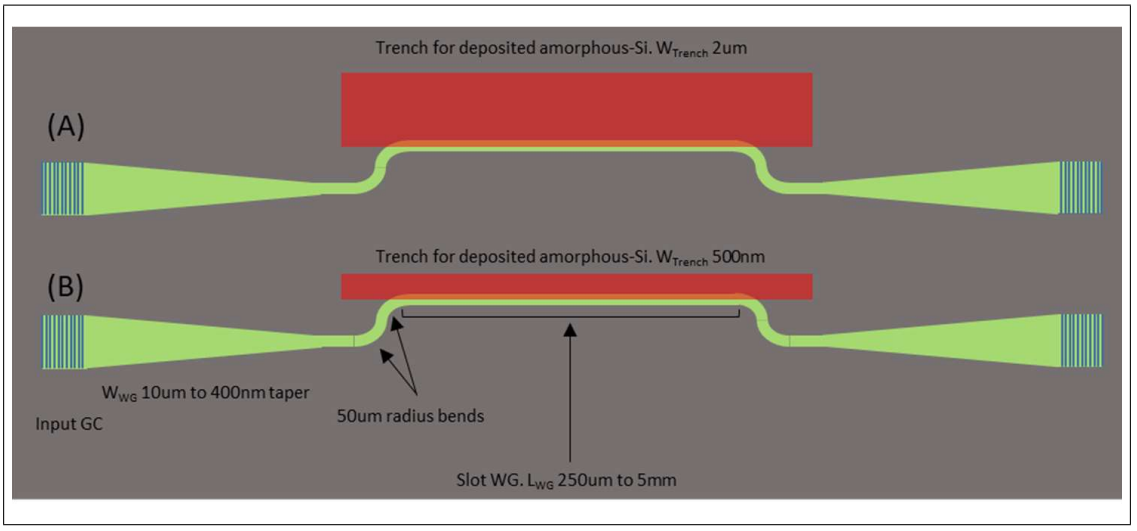


FIGURE 6.1: Passive vertical-slot rib-waveguide device schematic showing trench position for a-Si deposition. Showing two devices with (A) W_{trench}= 2μm and (B) W_{trench}=500nm.

The trench was etched using ICP, a-Si was deposited using PECVD, and the wafer was annealed for 10 hours at 100C in an N_2 environment. Following this (before CMP planarisation), cross-section and top-down SEM images were taken of the trench region. The top-down images were taken after the removal of the top SiO_2 layer also, which was unintentionally grown during the 10 hour 1000C N_2 environment anneal due presumably to the very slight presence of O_2 in the annealing chamber. Figure 6.2 (a) and (c) show a 2μm wide trench cross-section and top-down view respectively, whereas (b) and (d) show a 500nm wide trench cross-section and top-down view respectively. Poly-Si grains are clearly visible within the 2μm trench from the top-down image, and can also be observed (albeit slightly less clearly) from the cross-sectional image. Poly-Si grains are not present in the 500nm wide trench from the top-down image, and the cross-sectional image shows a much smoother profile. These images confirm that the a-Si could be fully recrystallised for a W_{trench}=500nm.

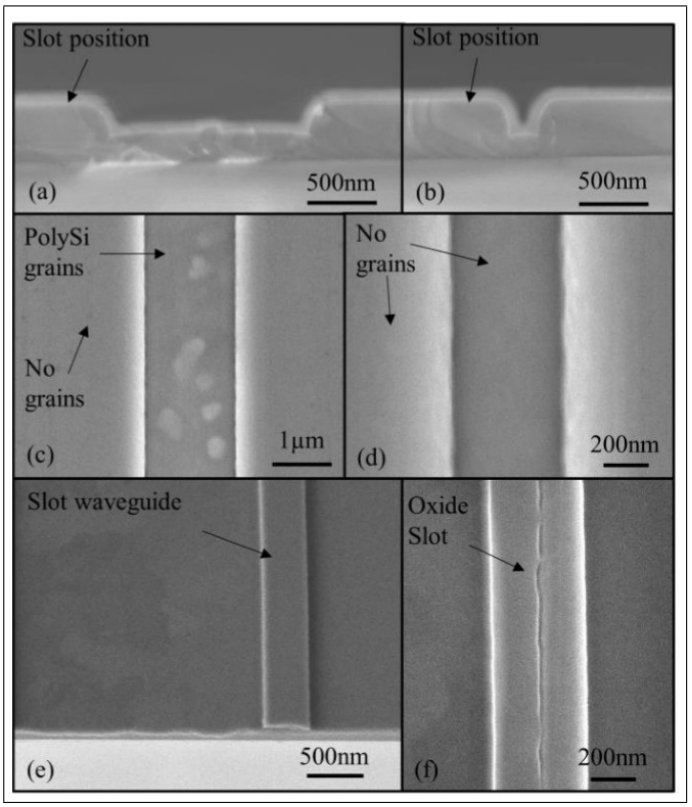


FIGURE 6.2: SEM images of recrystallized PECVD Si covering vertical-slot feature, and partially-etched vertical-slot rib-waveguide. (a) and (c) W_{trench}=2μm cross-section and top-down view respectively, (b) and (d) W_{trench}=2μm cross-section and top-down view respectively. Top-down view of fabricated vertical-slot rib-waveguide is shown before (a) and after (b) 10 minute HF etch to accentuate the position of the exposed SiO_2.

During annealing, the a-Si can recrystallize from two distinct and designed seed "windows" where the a-Si/c-Si contact. A model for how this occurs is presented schematically in Figure 6.3. If the trench width is too long, recrystallization occurs from both directions and meets in the middle of the trench or near to the vertical-slot. A wider trench also increases the likelihood of poly-Si grains growing from nucleation sites along the BOx/a-Si interface. With the current parameters for deposition and annealing conditions, as well as the trench design, a W_{trench} of 500nm appeared to be the optimum width for avoiding in-trench poly-Si grains (as can be seen in the disparity between the fully-c-Si trench in Figure 6.2 (b) and (d) vs. the poly-Si grains apparent in Figure 6.2 (a) and (c)).

However, despite the fact that poly-Si grains are unlikely to form in the 500nm wide trench, it is important to consider how the W_{trench} effects the deposition rate and deposition characteristics, as well as the eventual recrystallization quality. The a-Si deposition rate for the narrower trench is slower and less consistent than the a-Si deposition rate for the wider trench, and there is a chance of creating voids at the crucial SiO_2/BOx/a-Si corner region (indicated by a red circle in Figure 6.3 (B)). Also, although poly-Si grains appear with W_{trench}=2μm, these appear over 200nm from the vertical-SiO_2 slot.

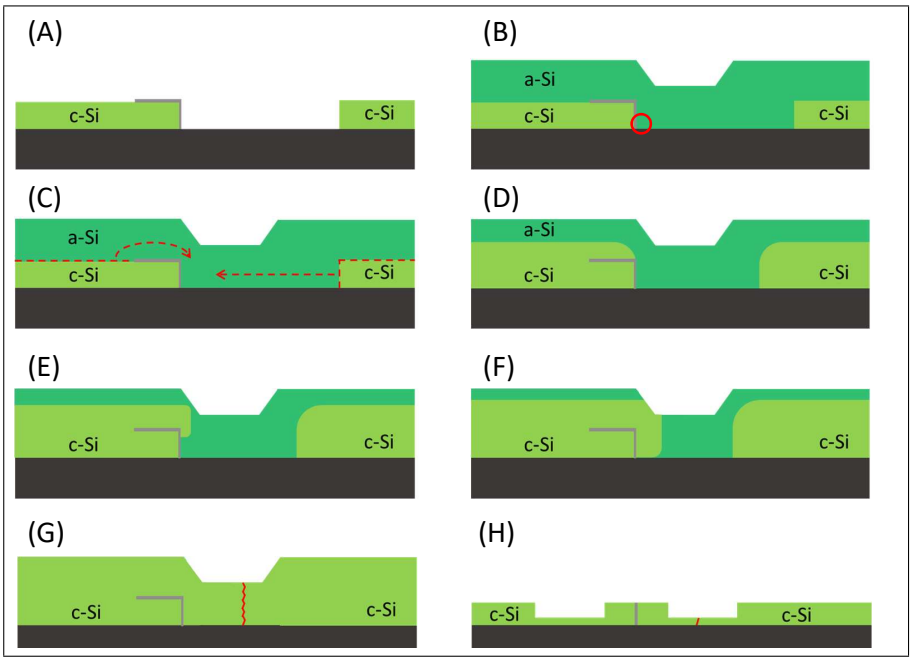


FIGURE 6.3: Schematic showing model of recrystallization from two recrystallization "seed" windows for vertical-SiO_2 slot. (A) Trench etched, oxidized and "seed" windows selectively opened using HF. (B) ~350nm thick a-Si applied using PECVD. (C) Recrystallization "seed" windows designated by dotted red lines at a-Si/c-Si boundary, with red dotted arrows indicating recrystallization directions. (D) to (F) show recrystallization propagation direction from both "seed" windows. (F) shows the point at which the trench is not fully recrystallized, but all of the Si that will make up the eventual rib-waveguide has recrystallized. (G) shows an ideal case where recrystallization from both "seed" windows has met at a point far removed from the vertical-slot where the waveguide will be patterned. The crooked red line in (G) indicates the recrystallization meeting point where a c-Si/c-Si boundary is expected to materialize. Ideally both sides will be fully recrystallized but this boundary will appear as a poly-Si boundary.

They will therefore not be present in the waveguide section of the device (which will be fully-crystalline), and not negatively effect the optical performance of the device. These poly-Si grains will be present in the 100nm thick connecting electronic connecting layer, but this will not negatively effect the electrical performance. For these reasons it was decided to use a 2μm wide trench for the modulator device.

Figure 6.2 (e) and (f) show top-down SEM images of the partially-etched vertical-slot (using 2μm trench) rib-waveguide before and after 10 minutes HF etch. It is clear from Figure 6.2 (e) (pre-HF etch) that the waveguide and region closest to the waveguide is all uniform, indicating that it is fully-crystalline. Figure 6.2 (f) (post-HF) exposes the 10nm SiO_2 slot from above, which appears to be bent. However, this appearance can be attributed to non-uniform HF etching of this very narrow exposed SiO_2. HF etches such narrow high aspect-ratio features non-uniformly.

The following is a detailed description of the entire fabrication process: The 340nm (100) SOI (2μm BOx) substrate is initially annealed at 950C in a dry (i.e. no H_20) O_2 environment to grow 20nm protective thermal oxide. Positive electron-beam lithography

resist ZEP520A is then spun onto the substrate and a 5μm rectangular trench is patterned and etched using vertical-sidewall ICP dry etching. Dry etching causes significant sidewall roughness, which increase propagation loss. To combat this, TMAH is applied for several minutes to reduce the sidewall roughness. The resist is then removed using a combination of dry and wet processes and the substrate is again annealed in a 950C O_2 environment to grow 10nm SiO_2 on the sidewalls of the trench. This also causes the top SiO_2 protective layer to grow by ∼3nm-5nm. Negative electron-beam resist UVN-30 is then applied, and areas either side of the trench sidewall that are to constitute the central slot-oxide are patterned and removed(Figure 3.11 and Figure 3.10 (G)). The top and sidewall oxide is removed using dilute buffered HF. The resist is removed and the wafer is cleaned. Then a 350nm thick layer of a-Si is deposited using PECVD. This a-Si layer covers the entire surface, and is therefore in direct contact with the un-etched fully-c-Si on the SOI layer. For this reason it is possible to employ the technique of epitaxial recrystallization using the points of a-Si/c-Si contact as "seed" regrowth regions. The epitaxial recrystallization occurs when the sample is placed in a 1000C N_2 environment for ten hours.

Following this crystallization, the surface will be incredibly non-uniform. To re-establish a smooth top-surface, planar substrate , CMP must be used. The substrate is polished until the top SOI thickness is 320nm, the target waveguide thickness. Before the waveguide itself and corresponding MZI architecture and grating couplers (GC) etc. is patterned and etched, boron (p-type) and phosphorus (n-type) dopants are implanted using ion beam implantation. The design ensures that each dopant is applied no closer than 100nm from the central slot-oxide, to avoid cross-contamination. The dopants are then thermally defused such that they reach the vertical-slot oxide diffusion stopping layer, and have a target dopant concentration of 1x10^{18} cm^{-3}. The waveguide/MZI/grating couplers (GC) structures is then patterned and dry etched using positive electron-beam resist (ZEP520A) and ICP etching. The asymmetrical MZI L_{shifter} is 500μm per arm, with an ΔL_{arm} of 200μm. Highly doped (doping concentration = 1x10^{20}cm^{-3}) p++ and n++ regions are implanted 900nm away from the central slot for use as ohmic contacts. A 1μm PECVD SiO_2 layer is applied which served as a dielectric protective layer. Vias are patterned, etched, and metal contacts consisting of a Ti/TiN/Al/TiN/Ti stack are sputtered.

6.1.2 Transmission Characterisation

The transmission characteristics were measured using the same optical set-up described in Figure 4.2.2. Vertical-slot rib-waveguides of lengths 200μm, 500μm, 1mm, 2mm, and 5mm were measured, as well as no-slot rib-waveguides of lengths 500μm, 1mm, 2mm, 5mm and 10mm as reference. The normalized transmission loss for these devices is shown in Figure 6.4, which shows the linear transmission loss of the vertical-slot rib-waveguide

to be 1.38dB/mm, and the linear transmission loss of the no-slot rib-waveguide fabricated on the same wafer to be 0.85dB/mm.

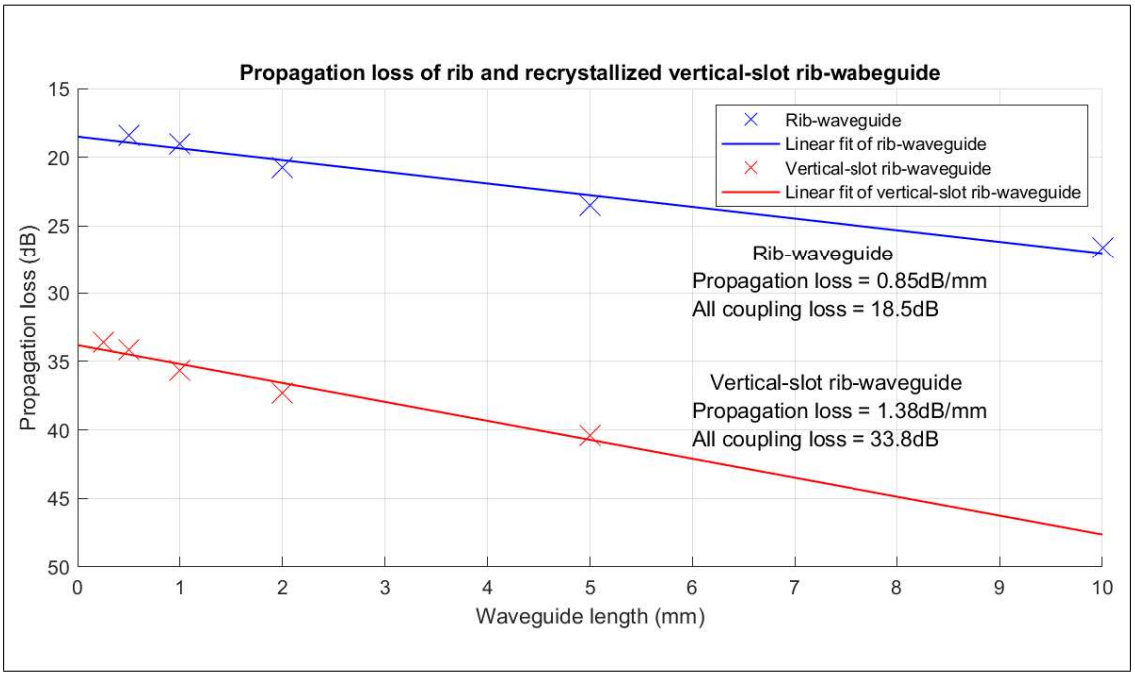


FIGURE 6.4: Absolute transmission loss (x markers) and linear fit (solid line) for no-slot rib-waveguide (blue) and vertical-slot rib-waveguide (red)

The vertical-slot rib-waveguide demonstrates almost double the propagation loss (1.38dB/mm) of that demonstrated by the horizontal-slot strip-waveguide (0.74dB/mm) fabricated by bonding, thinning down and dry etching (discussed in 4.2). This increased loss is attributed to the top-surface roughness which cannot be completely removed using CMP (the rms roughness of the wafer post-CMP was 8nm, compared to 1nm for pristine SOI wafers. The roughness of the top of the vertical-slot waveguide was not measured, but it can be assumed to be closer to that of pristine SOI wafers because it was defined by the BOx which was removed), and the non-uniform deposition of a-Si on the trench-etched side of the waveguide. However, the horizontal-slot fin-waveguides have significantly higher loss (5.8dB/mm) than the vertical-slot rib-waveguides (1.38dB/mm) which can be used for an electrically active device. Therefore, despite the horizontal-slot strip-waveguide having a lower loss (and the lowest demonstrated loss for any ultra-narrow slot waveguide), because of the complicated alternating fin design required to utilize this horizontal-slot waveguide, until the fabrication issues can be overcome such that the introduction of fins does not significantly increase loss, it is preferable to choose the vertical-slot rib-waveguide structure for the active modulator device. The fin-waveguide structure does still have some advantages over the vertical-slot which have been discussed, but for the purposes of this project, it makes sense at this time to continue forward with the vertical-slot rib-waveguide.

6.2 Vertical-Slot Accumulation Modulator Characterisation

The vertical-slot rib-waveguide accumulation modulator was fabricated as described in 6.1.1, and its characterisation is described here. Due to fabrication concerns, cross-chip performance variability was very high and therefore a systematic study of multiple devices with varying design parameters could not be done. Here is presented the results from a single device (unless otherwise stated), which can be considered as an example of a "worst case" device, which can be significantly improved upon by optimizing the fabrication design.

The vertical-slot accumulation modulator was characterised using the following method: A tunable CW laser source was used to send light through a polarization rotator to convert the input light to TE mode, which was then coupled into the device using grating-couplers. A positive DC bias of 0V, 6V and 10V was applied to the p-terminal of the device whilst the tunable input laser was swept from λ = 1555nm-1565nm, and the transmission loss was recorded. The MZI L_{shifter}=500μm and the ΔL_{arm}=200μm. The transmission loss as a function of λ at these applied biases is shown in Figure 6.5 and Figure 6.7 (a) (normalized to the transmission loss of a non-slot rib-waveguide to remove intrinsic system loss).

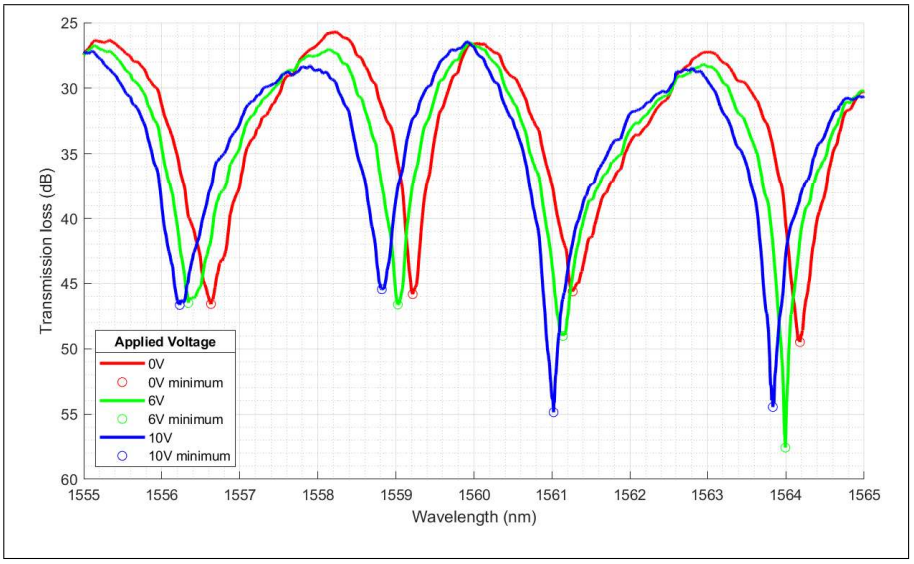


FIGURE 6.5: Transmission loss results for active modulator device at λ=1555nm-1565nm at applied DC bias of 0V, 6V and 10V. MZI L_{shifter}=500μm and the ΔL_{arm}=200μm

The extinction ratio (ER) for this device in the bandwidth of interest (λ=1555nm-1565nm) is between 17dB-29dB, and the average free-spectral-range (FSR) is 2.5nm. The insertion loss at peak intensity varies because of device non-uniformity and because of the intrinsic Gaussian distribution of the coupling efficiency but at this spectrum of interest the insertion loss is 26dB (at λ = 1558.2nm). It is useful to analyze the level to

which each section of the device contributes to this insertion loss. From reference waveguides on the chip it was found that the doped waveguides exhibited transmission loss of 5.1dB/mm, whereas the undoped waveguide exhibited transmission loss of 1.7dB/mm. Transmission loss of 5.1dB/mm in the 500μm long doped phase-shifter arms of the MZI device indicate that the loss through this active region of the device was only 2.5dB, and the majority (90%) of the transmission loss is accounted for in the passive regions of the device. Reference passive waveguides were included on the chip to measure the transmission loss which occurred at the no-slot rib-waveguide/vertical-slot rib-waveguide transition. This loss was found to be $\sim$ 5.5dB/transition, which is higher than expected from simulation. This increased transition loss can be accounted for by acknowledging that the fabrication process was not optimized and not perfect. No-slot/vertical-slot transition is an area that requires additional design/process optimization and research, but lowering transmission loss of the passive components was not the focus of the project, and despite the increased transition loss the device still operated well enough to test it actively, which was the focus of the project.

As can be seen clearly in Figure 6.5, as a positive DC bias was applied to the positive terminal of the device, the MZI transmission spectrum was blue-shifted by $\sim$0.2nm (0V to 6V) or $\sim$0.35nm (0V to 10V). This is caused by the increased free carries which accumulate either side of the vertical-slot oxide barrier in accumulation operation, which very slightly decreases the the effective index of the mode propagating through that 500μm long phase-change arm of the MZI device. n is a function of applied voltage, and λ_{FSR} is a function of n according to the following equation :

$$\lambda_{\mathrm{FSR}} = \frac{\lambda^2}{n_V L} \tag{6.1}$$

Where:
λ_{FSR}= λ free spectral range (peak-to-peak or minima-to-minima (easier to determine))
n_V = refractive index of propagating mode within the "cavity" under applied DC bias V
L = 2 x "cavity" length. In the case of an MZI device L = 2 x ΔL_{arm}.

Alternatively, the minima-to-minima FSR can be extracted from the transmission data and this can be used to calculate the refractive index change induced by the change in free carriers. The FSR varies from 2.05nm to 2.915nm over the spectrum presented but the average FSR is 2.5nm. This equates to an n_{0V} = 2.417. This value for n_{0V} can be used to roughly model the transmission spectrum for a MZI device, and this model can be used to estimate the refractive index change which occurs at bias 6V and 10V. The transmission intensity (I_t) is a function of the δ between the two MZI arms:

$$I_{\mathrm{t}} = \frac{(1 - R_{loss})^2}{(1 - R_{loss})^2 + 4R_{loss}\sin^2\frac{\delta}{2}} \tag{6.2}$$

$$I_{\mathrm{loss}} = 1 - I_{\mathrm{t}} \tag{6.3}$$

Where:
I_t = transmission intensity (a.u)
I_{loss} = transmission loss (a.u)
δ = phase change between the two arms (a.u)
R_{loss} = loss coefficient (a.u)

δ is a function of the phase change along the reference arm ($\delta_{reference}$), the phase change along the active arm (δ_{active}) and the phase change along the additional length of waveguide which makes up the asymmetric section of the device ($\delta_{\Delta L}$).

$$\delta = |\delta_{\mathrm{ref}} - (\delta_{\mathrm{active}} + \delta_{\Delta \mathrm{L_{arm}}})| \tag{6.4}$$

Where:

$$\delta_{\mathrm{ref}} = \frac{4\pi n_{0V} L_{\mathrm{ref}}}{\lambda} \tag{6.5}$$

$$\delta_{\mathrm{active}} = \frac{4\pi n_{V} L_{\mathrm{active}}}{\lambda} \tag{6.6}$$

$$\delta_{\Delta \mathrm{L_{arm}}} = \frac{4\pi n_{0V} L_{\Delta \mathrm{L_{arm}}}}{\lambda} \tag{6.7}$$

Where:
n_{0V} = refractive index in the vertical-slot rib-waveguide under applied DC bias of 0V
n_V = refractive index in the vertical-slot rib-waveguide under applied DC bias
L_{ref} = length of reference waveguide arm (500μm)
L_{active} = length of active waveguide arm (500μm)
$L_{\Delta \mathrm{L_{arm}}}$ = length of waveguide which makes up the asymmetric section of the device

Figure 6.6 (a) shows the normalized experimental transmission results for applied bias of 0V, 6V, 10V as well as the calculated model of the transmission using Figure 6.3. The calculated transmission loss (I_{loss}) was multiplied by an arbitrary coefficient and added to an arbitrary background loss coefficient (otherwise I_{loss} in this formulation is normalized between 0-1). loss coefficient (R_{loss}) was chosen such that the shape of the curve roughly matches that of the experimental results. This does not change the

minimum point of the curve and therefore does not change subsequent calculation of Δn, but the more accurate curve helps the figure to provide a more intuitive understanding of how the MZI system works.

The n_{0V} value closest to 2.417 that places the calculated minima at the correct point for 0V applied bias is $n_{0V} = 2.41679$. The n values which placed the calculated minima with the experimental minima for applied DC bias of 6V and 10V were 2.41656 and 2.41630 respectively. These equates to a n reduction of 2.3×10^{-4} and 4.9×10^{-4} respectively. These refractive index changes are in keeping with expected values, and over a 500μm long phase-shifter are sufficient to adequately shift the MZI transmission spectrum minima such that a significant change in I_t (or in this case I_{loss}) is observable.)

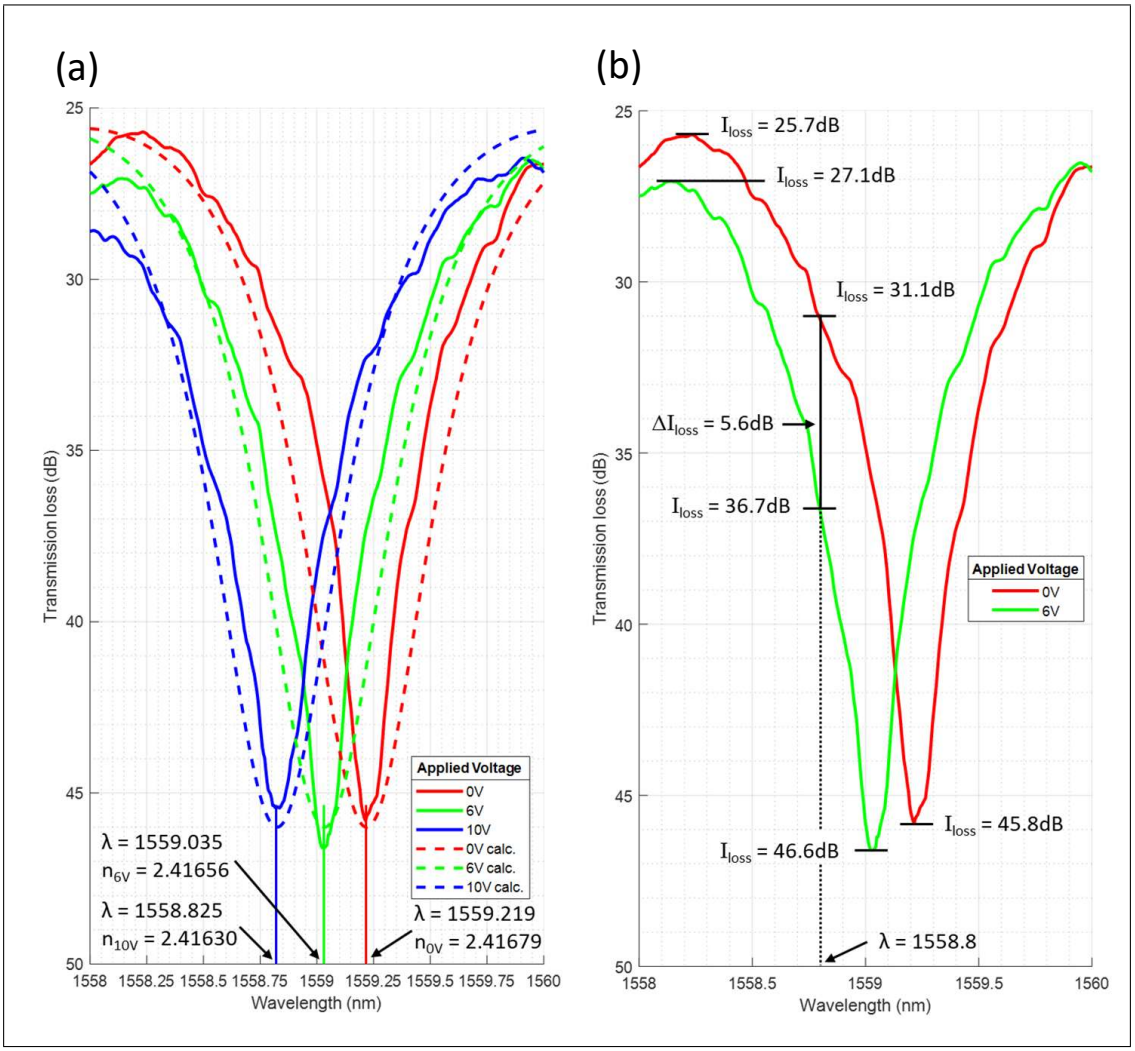


FIGURE 6.6: (a) Transmission spectrum of vertical-slot rib-waveguide modulator at applied DC bias 0V, 6V, 10V, with overlaid calculated spectrum at varied n. The minima point is a function of n_V and by aligning the calculated spectrum to the experimental spectrum, the Δn_V can be accurately established (even if the n_V is incorrect). (b) Transmission spectrum at 0V and high-speed operational bias 6V, showing clearly the quadrature point on the 0V spectra and the $\Delta I_{loss} = 5.6$dB at operational $\lambda = 1558.8$nm.

The blue-shift observed in the transmission spectrum can be converted to the phase modulation (phase change) which occurs along the 500μm long phase-shifter arm of the device, and this in turn can be used to calculate the modulation efficiency ($V_\pi L$). Increased $V_\pi L$ equates to lower device energy consumption and/or a smaller device footprint. $V_\pi L$ is the voltage-length product required to realise a π radian phase change:

$$V_\pi L_\pi = \frac{\pi}{\delta} \times \frac{V}{(\frac{1cm}{L})} \tag{6.8}$$

Where:
δ = phase change induced by applied DC bias
V = applied DC bias
L = phase-shifter arm length (m)

The phase modulation and corresponding modulation efficiency is plotted in Figure 6.7 (b). As applied DC voltage is increased, the modulation efficiency decreases. This is in accordance with simulation and theory, as charge carriers do not accumulate linearly with applied glsbdc bias, and therefore phase-shifter arm waveguide refractive index does not decrease linearly. glsbdc bias of 6V will be used to conduct the high-speed analysis of the device. Experimentally, for applied glsbdc bias 6V, the measured $\delta = 0.61599$ (for 500μm) and modulation efficiency 1.53Vcm. According to *Lumerical Solutions* CHARGE simulations discussed in 3.2.2, the results of which are shown in Figure 3.9, δ of 0.61599 implies a vertical-slot gate oxide thickness of $\sim$ 14nm.

During high-operation-speed analysis of the device, a PRBS was used to provide an input signal for a drive amplifier which boosted the signal to the required 6V. The signal was applied to the device using a high-speed ground-signal-ground (GSG) probe. The GSG probe contacted the metal pad which connected the electrical signal through the via and metal layer to the metal/p++ doped SOI contact at the input side of the phase-shifter waveguide. The p++ doped region was connected to the p- doped side of the waveguide which made up the active phase-shifter waveguide arm of the MZI device. The output side of the phase-shifter waveguide was connected in reverse order to a metal output pad, to which a second GSG probe was connected. The second GSG probe was connected to a 50Ω termination point to act as DC block.

The operating wavelength chosen to carry out the high-speed analysis was 1558.8nm. This corresponds to the quadrature point for this device. For 0V bias, transmission is 5.4dB lower than at the nearest peak transmission, which is 27% of the local ER of 20.1dB. For 6V bias, transmission is 9.9dB lower than at the nearest peak transmission, which is 49% of the local ER of 19.5dB. The difference in transmission intensity at 1558.8nm between 0V and 6V under steady-state conditions is 5.6dB. This is shown in Figure 6.6 (b). In high-speed operation the device will obviously experience a smaller ER in the eye-diagram.

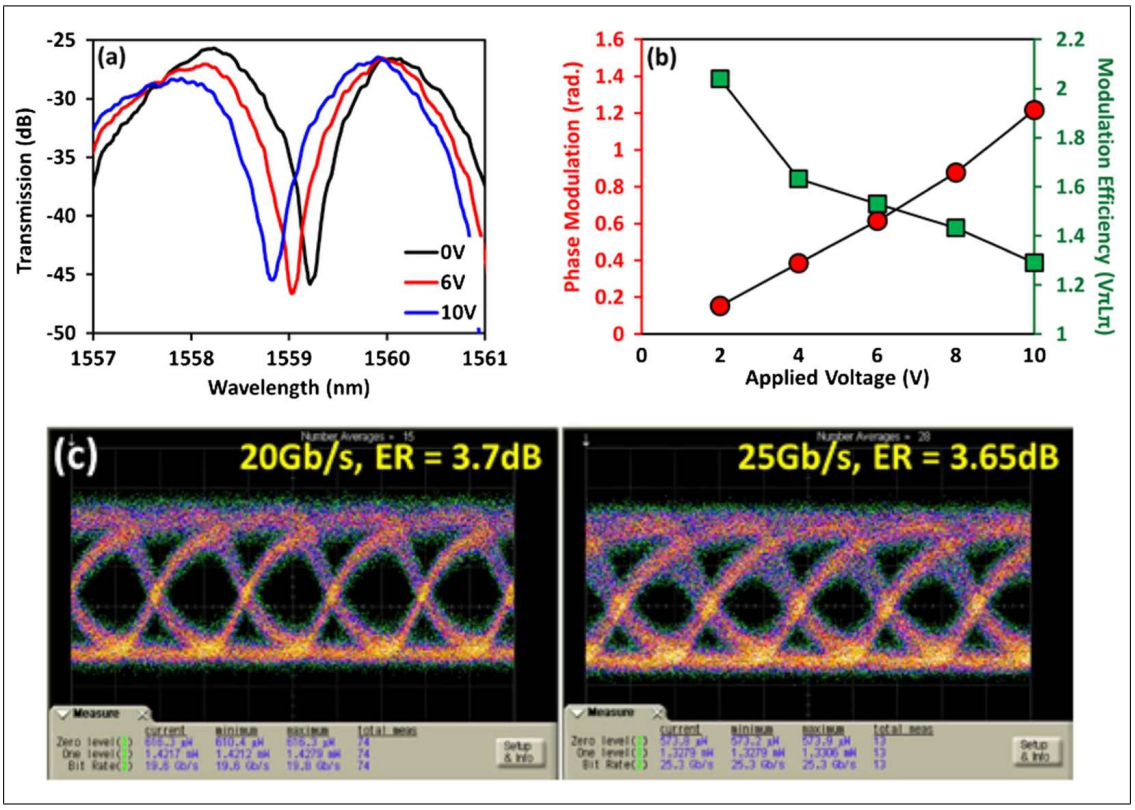


FIGURE 6.7: Characterisation results for active vertical-slot rib-waveguide accumulation modulator. (a) Transmission spectrum for λ=1557-1561nm for 500μm phase-shifter length MZI as a function of applied voltage. (B) Phase change and extracted modulation efficiency as a function of applied voltage. (C) Eye diagrams for device measured at 6V driving voltage (3V DC bias) showing clear "eye opening" when modulating a PRBS at 20Gb/s (left) and 25Gb/s (right)

In high-speed operation, the output light is coupled into a fibre and from there into an EDFA and then an optical filter. This amplifies the optical signal and then removes some of the noise that this amplification generates. The optical signal was then passed to the digital communication analyzer (DCA), with which the characteristic "eye-diagram" was observed. The eye-diagrams for operation at 20 Gbit/s and 25 Gbit/s are shown clearly in Figure 6.7 (c) left and right respectively. These eye-diagrams demonstrate ERs of 3.7dB and 3.6dB respectively, which, whilst lower than the steady state ER of 5.6dB, is still sufficient for the purpose of high-speed EO modulation.

The operating speed of 25Gbit/s is lower than the operating speed predicted from simulation, which was 42GHz. One of the primary causes contributing to this reduction in operating speed is the contact resistance of 11Ω, which was not accounted for in the simulation (ohmic contacts were assumed). Another primary cause contributing top to this reduction is the connecting rib doping concentration, which was designed to be uniformly 1×10^{18}cm^{-3}, but when measured using a PN diode test structure from the same wafer it was found to be 6×10^{17}cm^{-3}. This reduction in doping concentration will mean an increased contact rib resistance, which also was not accounted for in the simulation.

6.3 Conclusion

Fully-crystalline vertical-slot rib-waveguides were developed using a unique fabrication process involving the full recrystallization of deposited a-Si using exposed "seed" windows of Si and CMP planarisation to realize a vertical-slot SiO_2 layer seamlessly integrated into the planar SOI layer. This vertical-slot SiO_2 layer was used as the vertical gate oxide at the centre of the vertical-slot rib-waveguide which would become the active MOScap component of the accumulation modulator. The propagation loss of the passive vertical-slot rib waveguide fabricated in this was was shown to be 1.38dB/mm, which, although higher than the minimum propagation loss exhibited by the horizontal-slot strip-waveguide (0.85dB/mm), it was significantly lower than the lowest propagation loss exhibited by the horizontal-slot fin-waveguide (6.6dB).

Having confirmed that the passive transmission loss was acceptable, the active accumulation modulator was fabricated and characterised. The transmission spectrum at 0V DC applied bias showed total device insertion loss = 26dB, ER = 17-29dB, FSR = 2.5nm (average). The propagation loss through the active region of the device was measured to be 2.5dB. This low propagation loss was enabled by the recrystallization process. When comparing the experimental spectrum with the calculated spectrum it was found that the $\Delta n_V = 2.3 \times 10^{-4}$ and 4.9×10^{-4} for applied DC bias of 6V and 10V respectively. At the quadrature point the steady-state ER between 0-6V was 5.6dB. The phase change observed over the 500μm phase-shifter arm waveguide between 0-6V was 0.62, which suggests a modulation efficiency of 1.53Vcm and a gate oxide thickness of $\sim$14nm. During high-speed analysis conducted at λ=1558.8nm, a PRBS produced a characteristic "eye-diagram" on the DCA for operating speeds up to 25Gbit/s, where the "eye-diagram" demonstrated ER=3.6dB.

The modulation speed of 25Gbit/s and modulation efficiency of 1.53Vcm can be considered high-speed and high-efficiency when acknowledging the fact that this is a based on a new vertical-slot in-plane design architecture and a new fabrication process. The simulations suggest that the current design can be competitive with horizontal-slot accumulation modulator designs[3] and the design/fabrication process can still be optimized in several ways (e.g. fabricated doping profile aligning with designed doping profile, reducing 11Ω contact resistance, improving fabrication for no-slot rib-waveguide to vertical-slot rib-waveguide transition, lowering passive transmission loss caused by CMP induced top-surface roughness etc.). Also, whilst the horizontal-slot fin-waveguide devices can be designed as pseudo-1D PhCs (and may in some configurations be able to be used as a TE-TM converted), the vertical-slot rib-waveguide design can more easily accommodate the inclusion of a standard 2D photonic crystal structure. This can easily be achieved by changing the pattern used to define and etch the rib-waveguide, which is a trivial step which occurs after the realization of the in-plane vertical-slot, and does not effect the vertical-slot. The vertical-slot rib-waveguide can also be included in a ring resonator

whereas the horizontal-slot fin-waveguide cannot. The vertical-slot rib-waveguide accumulation modulator demonstrated here can therefore be more easily integrated into already established silicon photonics platforms.

Chapter 7

Conclusions

7.1 Thesis Summary

OE modulators are a key enabling technology when it comes to medium and short range interconnects, as well as an enabling technology for further electronic and optical integration. There are many potential platforms and designs on which OE modulators can be based. The purpose of this PhD was to develop a fully-crystalline narrow-slot high-speed/high-efficiency accumulation modulator that could be easily integrated into existing silicon photonics technologies (both in terms of design and compatibility with existing fabrication processes), and would be competitive with current industry standard Si accumulation modulators. To this end, two competing designs were proposed: (1) a bi-layer horizontal-slot fin-waveguide fabricated by mirrored orientation (111) orientation SOI bonding, thinning and subsequent self-aligned TMAH wet etching to simultaneously realise under-etching of the top fins and over-etching of the bottom fins, and (2) an in-planar vertical-slot rib-waveguide fabricated by a-Si deposition and recrystallization and CMP.

Simulations for both designs have been presented and the advantages/disadvantages of each design have been discussed at length. The horizontal-slot fin-waveguide has several advantages over the vertical-slot rib-waveguide. These include the ability more accurately control the SiO_2 slot thickness, as well as grow a thinner SiO_2 slot if required. Both horizontal-slot c-Si/SiO_2 interfaces will also be perfect as they were both grown using thermal oxidation of c-Si, whereas one of the vertical-slot c-Si/SiO_2 interfaces will be of lower quality because it will rely on the extent/quality of a-Si coverage on that side of the slot, and then the quality of the recrystallization. The horizontal-slot fin-waveguide top surface will also be smoother than the vertical-slot fin-waveguide top surface because it will be defined by the perfect c-Si/BOx interface instead of CMP. For these two reasons, the horizontal-slot strip-waveguide has lower transmission loss (0.85dB/mm)

than that exhibited by the vertical-slot rib-waveguide (1.38dB/mm) (and lower transmission loss than any comparable fully-crystalline slot waveguide). The horizontal-slot fin-waveguide is the first demonstration of a simultaneously over-etched/under-etched bi-layer silicon photonics device, and this technique could be used to realise new previously impossible bi-layer architectures. All relevant passive devices have been fabricated using the horizontal-slot fin/strip-waveguide platform, including grating couplers (GC), Mach-Zehnder interferometers (MZI) and multi mode interferometers (MMI), and pseudo-1D PhCs exhibiting a PBG. The characterisation and analysis of these devices has been presented at length in this thesis in 4 and 5.

However, despite these advantages, once the proof-of-concept passive horizontal-slot fin-waveguides were successfully demonstrated, it became apparent that the complexity of the 3D fin structure would make the fabrication of a satisfactory horizontal-slot fin-waveguide based accumulator incredibly challenging. The transmission loss of the horizontal-slot fin-waveguide was also x5 higher than that of the vertical-slot rib-waveguide. For these reasons, it was decided that for the active modulator the vertical-slot rib-waveguide design was to be pursued.

The vertical-slot rib-waveguide was fabricated by growing a thin (14nm) SiO_2 layer on the vertical Si sidewall, depositing a-Si via PECVD and then recrystallizing the a-Si. This was then planarized using CMP to realise the in-plane vertical-slot which would act as the gate oxide in the MOScap component of the device. SEM images demonstrate that recrystallization was complete in the region that would make up the waveguide (200nm either side of the vertical-slot). The rib-waveguide was then patterned and etched, ion implantation was used to lightly dope the waveguide and connecting ribs (1×10^{18} was targeted, but 6×10^{17} was measured using PN junction test devices), and heavily dope contact regions (1×10^{20}). A SiO_2 cladding layer was applied by PECVD, vias were etched and metal contacts deposited.

The transmission loss of the doped and undoped vertical-slot rib-waveguides was found to be 1.38dB/mm and 5.1dB/mm respectively. The insertion loss of the active modulator was 26dB, with only 2.5dB being attributed to loss in the 500μm long active phase-shifter section of the device. The no-slot/vertical-slot rib-waveguide transition exhibited a transition loss of 5.5dB/transition. The MZI exhibited an average FSR of 2.5nm and an ER of 17-29dB. Under the influence of an applied DC bias in steady-state operation, the transmission spectrum was found to blue-shift by 0.2nm (6V) and 0.35nm (10V), which equates to $\Delta n_{6V} = 2.3 \times 10^{-4}$ and $\Delta n_{10V} = 4.9 \times 10^{-4}$ respectively. The ER from 0V to 6V at the quatrature point was found to be 5.6dB in steady state operation. The experimentally observed blue-shift was converted into phase change to find the modulation efficiency, $V_\pi L = 1.53V{\cdot}cm$. Under high-speed operation, an "eye-diagram" with an ER of 3.6dB was observed for a modulation speed of 25Gbit/s. These characterisation details demonstrate that the vertical-slot rib-waveguide operates as expected, and although the

experimentally observed modulation speed was not as high as that predicted by simulation (42GHz), they demonstrate the potential of this platform to be competitive with appropriate design/fabrication optimization.

7.2 Future Work

There are many opportunities for improvement/optimization of the designs and fabrication processes mentioned in this thesis. There are also several new research areas and directions which became apparent during the work but which could not be pursued due to time and resource constraints. In this section the possible future design/fabrication optimizations will be discussed, as well as new research areas.

7.2.1 Horizontal-Slot Fin-Waveguide Accumulation Modulator

The horizontal-slot strip-waveguides demonstrated promising transmission loss values, and it is expected that these can be reduced significantly simply by applying short TMAH etch (10 minutes). However, the more pressing issue that should be addressed is the issue of reducing the horizontal-slot fin-waveguide loss. This could be done by a systematic study of many different fin designs and various sidewall thermal oxide thickness's (for LOCOS) and various TMAH etching times. Because of the limited number of chips available, such a systematic study of TMAH etch times could not be carried out in this case. There are also several design optimizations that could be explored. For example, one of the benefits of using a fully-crystalline silicon photonics platform with a centrally placed SiO_2 horizontal-slot is that the horizontal-slot acts as an inbuilt hard stopping layer when applying dry or wet Si etching. Stopping Si etching in the middle of the SiO_2 horizontal-slot layer (which exhibits high selectivity against Si when etching for many etching types) is beneficial as it avoids creating a rough Si top-surface where the etching stops. This SiO_2 horizontal-slot stopping layer could be used to improve the quality of apodized partially etched grating couplers. Another example of a potential design improvement would be the removal of the sharp discontinuity between the horizontal-slot strip-waveguide and the fin-waveguide, perhaps introducing the fins in a tapered fashion instead of beginning fins and TMAH etch window abruptly. Obviously once the fabrication has been sufficiently optimized such that the horizontal-slot fin-waveguide transmission loss is comparable with the vertical-slot rib-waveguide transmission loss, it will be very exciting to fabricate the active accumulation modulator, as the design is still promising.

Another research direction that would be interesting to pursue would be the exploration of novel applications of the up/down offset pseudo-1D PhC structure created by the periodic fins. FDTD simulations suggest for example that by introducing a mismatch in

alignment between left and right fins, a PBG appears for the TE mode only, whilst the TM mode is unaffected. This PBG could be used to couple TE mode to TM mode. Also, the inherent left-right asymmetry and ability to under-etch the bottom-layer distinctly from the top-layer could be used to design new PhC waveguide architectures generally, which have until now been restricted to one layer in-plane with the waveguide. The horizontal-slot fin-waveguide is the first demonstration of a bi-layer PhC waveguide. A design for the horizontal-slot fin-waveguide is presented schematically in 7.1.

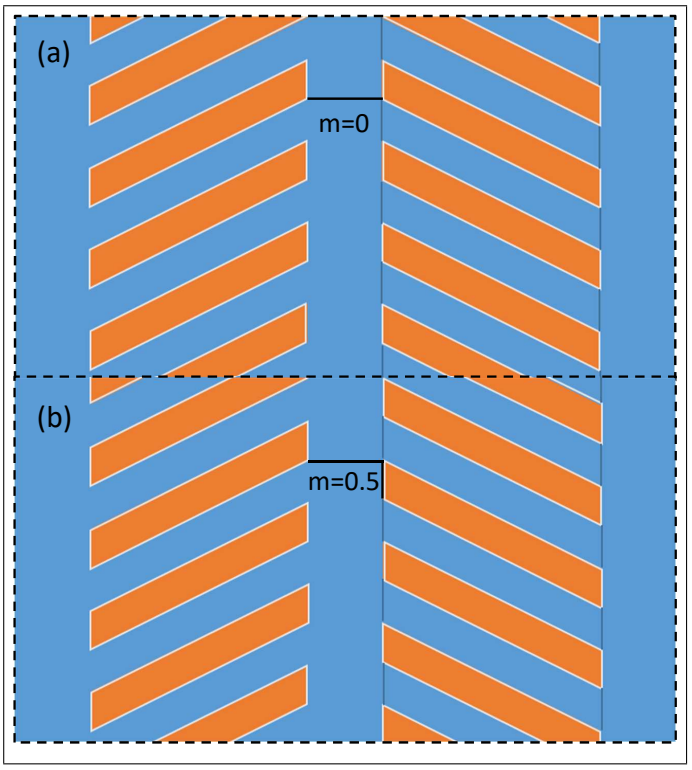


FIGURE 7.1: Top-down schematic of horizontal-slot fin-waveguide with (b) and without (a) period alignment mismatch

7.2.2 Vertical-Slot Rib-Waveguide Accumulation Modulator

The future work to be pursued in regards to the vertical-slot rib-waveguide accumulation modulator follows two trajectories. Firstly, design and fabrication optimization must be carried out to demonstrate that the current design can operate at the simulated speed of 32GHz with efficiency of 1V·cm (with gate oxide thickness=10nm instead of the realised 14nm), or 42GHz with lower efficiency. Secondly, the current design could be easily amended to include a standard PhC-waveguide instead of a rib-waveguide, or a ring-resonator modulator structure instead of an MZI modulator structure.

In terms of increasing the performance metrics of the current vertical-slot rib-waveguide accumulation modulator design, several areas of improvement have already been mentioned. The most critical being the optimization of the doping concentration profile and

the accurate realisation of this optimized profile, the reduction of top-surface roughness induced by CMP (potentially using LOCOS), and the reduction of the contact resistance. Two other areas that would benefit from optimization are the control of the vertical-slot SiO_2 thickness (10nm was targeted but the experimental thickness was estimated to be 14nm) and an improvement of the design and/or the fabrication of the no-slot/vertical-slot rib-waveguide transition, which exhibited a x5 expected loss from simulation per transition. With these improvements the device will be able to perform more in line with simulation results.

In terms of amending the design and integrating it on-chip with other established silicon photonics devices/components, the two most obvious next steps for integration are demonstrating a vertical-slot PhC-waveguide and a vertical-slot rib-waveguide ring-resonator modulator. Depending on how the PhC was designed and tunes, the vertical-slot PhC-waveguide accumulation modulator could be operated in the slow-light regime at the edge of the PBG, or it could be part of an electronically controllable optical filter.

It is clear that having now successfully demonstrated two new unique approaches to the problem of how to fabricate fully-crystalline MOScap waveguides, these two approaches can be developed to exploit their respective advantages.

Appendix A

Publications and Conferences

Publications

Primary Author

Byers, James, et al. "Silicon slot fin waveguide on bonded double-SOI for a low-power accumulation modulator fabricated by an anisotropic wet etching technique." Optics express 26.25 (2018): 33180-33191.[1]

Contributing Author

Saito, Shinichi, et al. "Si photonic waveguides with broken symmetries: applications from modulators to quantum simulations." Japanese Journal of Applied Physics 59.SO (2020): SO0801.[112]

Debnath, Kapil, et al. "All-silicon carrier accumulation modulator based on a lateral metal-oxide-semiconductor capacitor." Photonics Research 6.5 (2018): 373-379.[3]

Conferences

Presented

Byers, James, et al. "3D Fin Waveguide on 10nm Gate Oxide Bonded Double-SOI for Low $V_\pi L$ Accumulation Modulator." 2018 IEEE 15th International Conference on Group IV Photonics (GFP). IEEE, 2018.[2]

Contributing Author

Saito, Shinichi, et al. "Novel Si Photonic Waveguides and Applications to Optical Modulators (Invited)", Twenty-Forth Microoptics Conference (MOC2019), page 2. JSAP, 2019,[113]

Zhang, Weiwei, et al. "High speed silicon capacitor modulators for TM polarisation." 2019 IEEE 16th International Conference on Group IV Photonics (GFP). IEEE, 2019.[5]

Debnath, Kapil, et al. "20Gbps silicon lateral MOS-Capacitor electro-optic modulator." CLEO: Science and Innovations. Optical Society of America, 2018.[4]

Tomita, Isao, et al. "$LiNbO_3$/Si-Hybrid Slot-Waveguide Electro-Optic Modulators." 2018 IEEE 15th International Conference on Group IV Photonics (GFP). IEEE, 2018.[114]

Thomson, David J., et al. "Towards High Speed and Low Power Silicon Photonic Data Links." 2018 20th International Conference on Transparent Optical Networks (ICTON). IEEE, 2018.[6]

Bibliography

[1] James Byers, Kapil Debnath, Hideo Arimoto, M. Khaled Husain, Moise Sotto, Zuo Li, Fayong Liu, Kouta Ibukuro, Ali Khokhar, Kian Kiang, Stuart A. Boden, David J. Thomson, Graham T. Reed, and Shinichi Saito. Silicon slot fin waveguide on bonded double-soi for a low-power accumulation modulator fabricated by an anisotropic wet etching technique. *Opt. Express*, 26(25):33180–33191, Dec 2018.

[2] J. Byers, K. Debnath, H. Arimoto, M. K. Husain, M. Sotto, Z. Li, F. Liu, A. Khokhar, K. Kiang, S. A. Boden, et al. 3D fin waveguide on 10nm gate oxide bonded double-SOI for low $V_\pi L$ accumulation modulator. In *2018 IEEE 15th International Conference on Group IV Photonics (GFP)*, pages 1–2. IEEE, 2018.

[3] Kapil Debnath, David J. Thomson, Weiwei Zhang, Ali Z. Khokhar, Callum Littlejohns, James Byers, Lorenzo Mastronardi, Muhammad K. Husain, Kouta Ibukuro, Frederic Y. Gardes, et al. All-silicon carrier accumulation modulator based on a lateral metal-oxide-semiconductor capacitor. *Photonics Research*, 6(5):373–379, 2018.

[4] Kapil Debnath, David J. Thomson, Weiwei Zhang, Ali Z. Khokhar, Callum Littlejohns, James Byers, Lorenzo Mastronardi, Muhammad K. Husain, Frederic Y. Gardes, Graham T. Reed, et al. 20Gbps silicon lateral MOS-Capacitor electro-optic modulator. In *CLEO: Science and Innovations*, pages SM3B–5. Optical Society of America, 2018.

[5] Weiwei Zhang, Kapil Debnath, Bigeng Chen, Muhammad K. Husain, Ali Z. Khokhar, Shenghao Liu, James Byers, Wei Cao, Martin Ebert, Jamie Dean Reynolds, et al. High speed silicon capacitor modulators for TM polarisation. In *2019 IEEE 16th International Conference on Group IV Photonics (GFP)*, pages 1–2. IEEE, 2019.

[6] David J. Thomson, Kapil Debnath, Weiwei Zhang, Ke Li, Shenghao Liu, Fanfan Meng, Ali Z. Khokhar, Callum Littlejohns, James Byers, Lorenzo Mastronardi, et al. Towards high speed and low power silicon photonic data links. In *2018 20th International Conference on Transparent Optical Networks (ICTON)*, pages 1–4. IEEE, 2018.

[7] R. J. Mears, L. Reekie, I. M. Jauncey, and D. N. Payne. Low-noise erbium-doped fibre amplifier operating at 1.54μm. *Electronics Letters*, 23(19):1026–1028, Sep. 1987.

[8] James S. Foresi, Desmond R. Lim, Ling Liao, Anuradha Agarwal, Lionel C. Kimerling, M. Tavassoli, M. Cox, Min Cao, and Wayne M. Greene. Small radius bends and large angle splitters in SOI waveguides. In *Silicon-Based Monolithic and Hybrid Optoelectronic Devices*, volume 3007, pages 112–119. International Society for Optics and Photonics, 1997.

[9] R. A. Soref and J. P. Lorenzo. Single-crystal silicon: a new material for 1.3 and 1.6μm integrated-optical components. *Electronics Letters*, 21(21):953–954, 1985.

[10] P. Andrew Anderson, Bradley S. Schmidt, and Michal Lipson. High confinement in silicon slot waveguides with sharp bends. *Optics Express*, 14(20):9197–9202, 2006.

[11] Graham T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson. Silicon optical modulators. *Nature Photonics*, 4(8):518, 2010.

[12] R. A. Soref and B. R. Bennett. Electrooptical effects in silicon. *IEEE journal of quantum electronics*, 23(1):123–129, 1987.

[13] R. A. Soref. Silicon-based optoelectronics. *Proceedings of the IEEE*, 81(12):1687–1706, 1993.

[14] H. Ennen, Jörg Schneider, G. Pomrenke, and A. Axmann. 1.54-μm luminescence of erbium-implanted III-V semiconductors and silicon. *Applied Physics Letters*, 43(10):943–945, 1983.

[15] Shahram Keyvaninia, Gunther Roelkens, Dries Van Thourhout, Christophe Jany, Marco Lamponi, Alban Le Liepvre, Francois Lelarge, Dalila Make, Guang-Hua Duan, Damien Bordel, et al. Demonstration of a heterogeneously integrated III-V/SOI single wavelength tunable laser. *Optics express*, 21(3):3784–3792, 2013.

[16] D. G. Parker, P. G. Say, A. M. Hansom, and W. Sibbett. 110 GHz high-efficiency photodiodes fabricated from indium tin oxide/GaAs. *Electronics Letters*, 23(10):527–528, May 1987.

[17] Ed L. Wooten, Karl M. Kissa, Alfredo Yi-Yan, Edmond J. Murphy, Donald A. Lafaw, Peter F. Hallemeier, David Maack, Daniel V. Attanasio, Daniel J. Fritz, Gregory J. McBrien, et al. A review of lithium niobate modulators for fiber-optic communications systems. *IEEE Journal of selected topics in Quantum Electronics*, 6(1):69–82, 2000.

[18] Cisco Visual Networking. Cisco global cloud index: Forecast and methodology 2014-2019 (white paper). 2015.

[19] Po Dong, Shirong Liao, Dazeng Feng, Hong Liang, Dawei Zheng, Roshanak Shafiiha, Cheng-Chih Kung, Wei Qian, Guoliang Li, Xuezhe Zheng, et al. Low V_{pp}, ultralow-energy, compact, high-speed silicon electro-optic modulator. *Optics express*, 17(25):22484–22490, 2009.

[20] Richard Soref. The past, present, and future of silicon photonics. *IEEE Journal of selected topics in quantum electronics*, 12(6):1678–1687, 2006.

[21] Yongqiang Shi, Cheng Zhang, Hua Zhang, James H. Bechtel, Larry R. Dalton, Bruce H. Robinson, and William H. Steier. Low (sub-1-volt) halfwave voltage polymeric electro-optic modulators achieved by controlling chromophore shape. *Science*, 288(5463):119–122, 2000.

[22] David AB Miller. Attojoule optoelectronics for low-energy information processing and communications. *Journal of Lightwave Technology*, 35(3):346–396, 2017.

[23] Fuad E Doany, Clint L Schow, Benjamin G Lee, Russell Budd, Christian Baks, Roger Dangel, Richard John, Frank Libsch, Jeffrey A Kash, Benson Chan, et al. Terabit/sec-class board-level optical interconnects through polymer waveguides using 24-channel bidirectional transceiver modules. In *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, pages 790–797. IEEE, 2011.

[24] Ian A. Young, Edris Mohammed, Jason T. S. Liao, Alexandra M. Kern, Samuel Palermo, Bruce A. Block, Miriam R. Reshotko, and Peter L. D. Chang. Optical I/O technology for tera-scale computing. *IEEE Journal of Solid-State Circuits*, 45(1):235–248, 2010.

[25] Sudeep Pasricha and Nikil Dutt. *On-chip communication architectures: system on chip interconnect*. Morgan Kaufmann, 2010.

[26] Michael L. Davenport, Jared F. Bauters, Molly Piels, Martijn J. R. Heck, Arnold Chen, Alexander W. Fang, and John E. Bowers. A 400 Gb/s WDM receiver using a low loss silicon nitride AWG integrated with hybrid silicon photodetectors. In *National Fiber Optic Engineers Conference*, pages PDP5C–5. Optical Society of America, 2013.

[27] Li Chen and Ronald M. Reano. Compact electric field sensors based on indirect bonding of lithium niobate to silicon microrings. *Optics Express*, 20(4):4032–4038, 2012.

[28] R. Soref. Silicon photonics: A review of recent literature. *Silicon*, 2(1):1–6, 2010.

[29] JP Lorenzo and RA Soref. 1.3 μm electro-optic silicon switch. *Applied physics letters*, 51(1):6–8, 1987.

[30] GV Treyz, PG May, and Jean-Marc Halbout. Silicon mach–zehnder waveguide interferometers based on the plasma dispersion effect. *Applied physics letters*, 59(7):771–773, 1991.

[31] CK Tang and GT Reed. Highly efficient optical phase modulator in soi waveguides. *Electronics letters*, 31(6):451–452, 1995.

[32] Richard A Soref and Brian R Bennett. Kramers-kronig analysis of electro-optical switching in silicon. In *Integrated Optical Circuit Engineering IV*, volume 704, pages 32–38. International Society for Optics and Photonics, 1987.

[33] P Dainesi, A Kung, M Chabloz, A Lagos, Ph Fluckiger, A Ionescu, P Fazan, M Declerq, Philippe Renaud, and Ph Robert. Cmos compatible fully integrated mach-zehnder interferometer in soi technology. *IEEE Photonics Technology Letters*, 12(6):660–662, 2000.

[34] Ansheng Liu, Richard Jones, Ling Liao, Dean Samara-Rubio, Doron Rubin, Oded Cohen, Remus Nicolaescu, and Mario Paniccia. A high-speed silicon optical modulator based on a metal–oxide–semiconductor capacitor. *Nature*, 427(6975):615, 2004.

[35] Ling Liao, Dean Samara-Rubio, Michael Morse, Ansheng Liu, Dexter Hodge, Doron Rubin, Ulrich D Keil, and Thorkild Franck. High speed silicon mach-zehnder modulator. *Optics Express*, 13(8):3129–3135, 2005.

[36] Ansheng Liu, Ling Liao, Doron Rubin, Hat Nguyen, Berkehan Ciftcioglu, Yoel Chetrit, Nahum Izhaky, and Mario Paniccia. High-speed optical modulation based on carrier depletion in a silicon waveguide. *Optics express*, 15(2):660–668, 2007.

[37] Liu Liao, A Liu, D Rubin, JABJ Basak, YACY Chetrit, HANH Nguyen, RACR Cohen, NAIN Izhaky, and MAPM Paniccia. 40 Gbit/s silicon optical modulator for high-speed applications. *Electronics Letters*, 43(22):1196–1197, 2007.

[38] Michael R Watts, William A Zortman, Douglas C Trotter, Ralph W Young, and Anthony L Lentine. Low-voltage, compact, depletion-mode, silicon mach–zehnder modulator. *IEEE Journal of Selected Topics in Quantum Electronics*, 16(1):159–164, 2010.

[39] Ning-Ning Feng, Shirong Liao, Dazeng Feng, Po Dong, Dawei Zheng, Hong Liang, Roshanak Shafiiha, Guoliang Li, John E Cunningham, Ashok V Krishnamoorthy, et al. High speed carrier-depletion modulators with 1.4 v-cm v π l integrated on 0.25 μm silicon-on-insulator waveguides. *Optics express*, 18(8):7994–7999, 2010.

[40] DJ Thomson, FY Gardes, Y Hu, G Mashanovich, M Fournier, P Grosse, JM Fedeli, and GT Reed. High contrast 40gbit/s optical modulation in silicon. *Optics express*, 19(12):11507–11516, 2011.

[41] JC Rosenberg, WMJ Green, S Assefa, T Barwicz, M Yang, SM Shank, and Yurii A Vlasov. Low-power 30 gbps silicon microring modulator. In *Quantum Electronics and Laser Science Conference*, page PDPB9. Optical Society of America, 2011.

[42] Xi Xiao, Xianyao Li, Hao Xu, Yingtao Hu, Kang Xiong, Zhiyong Li, Tao Chu, Jinzhong Yu, and Yude Yu. 44-gb/s silicon microring modulators based on zigzag pn junctions. *IEEE Photonics Technology Letters*, 24(19):1712–1714, 2012.

[43] David J Thomson, Frederic Y Gardes, Jean-Marc Fedeli, Sanja Zlatanovic, Youfang Hu, Bill Ping Piu Kuo, Evgeny Myslivets, Nikola Alic, Stojan Radic, Goran Z Mashanovich, et al. 50-gb/s silicon optical modulator. *IEEE Photonics Technology Letters*, 24(4):234–236, 2012.

[44] Matthew Streshinsky, Ran Ding, Yang Liu, Ari Novack, Yisu Yang, Yangjin Ma, Xiaoguang Tu, Edward Koh Sing Chee, Andy Eu-Jin Lim, Patrick Guo-Qiang Lo, et al. Low power 50 gb/s silicon traveling wave mach-zehnder modulator near 1300 nm. *Optics express*, 21(25):30350–30357, 2013.

[45] Takeshi Baba, Suguru Akiyama, Masahiko Imai, Naoki Hirayama, Hiroyuki Takahashi, Yoshiji Noguchi, Tsuyoshi Horikawa, and Tatsuya Usuki. 50-Gb/s ring-resonator-based silicon modulator. *Optics Express*, 21(10):11869–11876, 2013.

[46] Xiaoguang Tu, Tsung-Yang Liow, Junfeng Song, Xianshu Luo, Qing Fang, Mingbin Yu, and Guo-Qiang Lo. 50-gb/s silicon optical modulator with traveling-wave electrodes. *Optics express*, 21(10):12776–12782, 2013.

[47] Xi Xiao, Miaofeng Li, Lei Wang, Daigao Chen, Qi Yang, and Shaohua Yu. High speed silicon photonic modulators. In *2017 Optical Fiber Communications Conference and Exhibition (OFC)*, pages 1–3. IEEE, 2017.

[48] Xiaotie Wu, Bipin Dama, Prakash Gothoskar, Peter Metz, Kal Shastri, Sanjay Sunder, Jan Van der Spiegel, Yifan Wang, Mark Webster, and Will Wilson. A 20Gb/s NRZ/PAM-4 1V transmitter in 40nm CMOS driving a Si-photonic modulator in 0.13μm CMOS. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 128–129. IEEE, 2013.

[49] Junichi Fujikata, Shigeki Takahashi, Masashi Takahashi, and Tsuyoshi Horikawa. High speed and highly efficient Si optical modulator with MOS junction for 1.55μm and 1.3μm wavelengths. In *2013 IEEE 10th International Conference on Group IV Photonics (GFP)*, pages 65–66. IEEE, 2013.

[50] Junichi Fujikata, Shigeki Takahashi, Masashi Takahashi, Masataka Noguchi, Takahiro Nakamura, and Yasuhiko Arakawa. High-performance mos-capacitor-type si optical modulator and surface-illumination-type ge photodetector for optical interconnection. *Japanese Journal of Applied Physics*, 55(4S):04EC01, 2016.

[51] Majid Sodagar, Amir H. Hosseinnia, Pierre Isautier, Hesam Moradinejad, Stephen Ralph, Ali A. Eftekhar, and Ali Adibi. Compact, 15 Gb/s electro-optic modulator through carrier accumulation in a hybrid Si/SiO_2/Si microdisk. *Optics Express*, 23(22):28306–28315, 2015.

[52] M Webster, P Gothoskar, V Patel, D Piede, S Anderson, R Tummidi, D Adams, C Appel, P Metz, S Sunder, et al. An efficient MOS-capacitor based silicon modulator and cmos drivers for optical transmitters. In *2014 IEEE 11th International Conference on Group IV Photonics (GFP)*, pages 1–2. IEEE, 2014.

[53] Ryan M. Briggs, Michael Shearn, Axel Scherer, and Harry A. Atwater. Wafer-bonded single-crystal silicon slot waveguides and ring resonators. *Applied Physics Letters*, 94(2):021106, 2009.

[54] Kapil Debnath, Hideo Arimoto, Muhammad K. Husain, Alyssa Prasmusinto, Abdelrahman Al-Attili, Rafidah Petra, Harold M. H. Chong, Graham T. Reed, and Shinichi Saito. Low-loss silicon waveguides and grating couplers fabricated using anisotropic wet etching technique. *Frontiers in Materials*, 3:10, 2016.

[55] Lumerical MODE. Lumerical Solutions, Inc. Version: 2017a. https://www.lumerical.com/products/mode/.

[56] Christopher G. Poulton, Christian Koos, Masafumi Fujii, Andreas Pfrang, Thomas Schimmel, Jrg Leuthold, and Wolfgang Freude. Radiation modes and roughness loss in high index-contrast waveguides. *IEEE Journal of Selected Topics in Quantum Electronics*, 12(6):1306–1321, 2006.

[57] Senichi Suzuki, Masahiro Yanagisawa, Yoshinori Hibino, and Kazuhiro Oda. High-density integrated planar lightwave circuits using SiO_2-GeO_2 waveguides with a high refractive index difference. *Journal of Lightwave Technology*, 12(5):790–796, 1994.

[58] Gary Shambat, Bryan Ellis, Jan Petykiewicz, Marie A. Mayer, Tomas Sarmiento, James Harris, Eugene E. Haller, and Jelena Vučković. Nanobeam photonic crystal cavity light-emitting diodes. *Applied Physics Letters*, 99(7):071105, 2011.

[59] Graham T Reed. *Silicon photonics: the state of the art*. John Wiley & Sons, 2008.

[60] P. H. Wendland and Marvin Chester. Electric field effects on indirect optical transitions in silicon. *Physical Review*, 140(4A):A1384, 1965.

[61] Guoping Dong, Guobo Wu, Shaohua Fan, Fangteng Zhang, Yuanhao Zhang, Botao Wu, Zhijun Ma, Mingying Peng, and Jianrong Qiu. Formation, near-infrared luminescence and multi-wavelength optical amplification of PbS quantum dot-embedded silicate glasses. *Journal of Non-Crystalline Solids*, 383:192–195, 2014.

[62] T. Barwicz, H. Byun, F. Gan, C. W. Holzwarth, M. A. Popovic, P. T. Rakich, M. R. Watts, E. P. Ippen, F. X. Kärtner, H. I. Smith, et al. Silicon photonics for compact, energy-efficient interconnects. *Journal of Optical Networking*, 6(1):63–73, 2007.

[63] Jie Teng, Pieter Dumon, Wim Bogaerts, Hongbo Zhang, Xigao Jian, Xiuyou Han, Mingshan Zhao, Geert Morthier, and Roel Baets. Athermal silicon-on-insulator ring resonators by overlaying a polymer cladding on narrowed waveguides. *Optics express*, 17(17):14627–14633, 2009.

[64] N. Ye Winnie, Jurgen Michel, and Lionel C. Kimerling. Athermal high-index-contrast waveguide design. *IEEE Photonics Technology Letters*, 20(11):885–887, 2008.

[65] Nathalie P. De Leon, Brendan J. Shields, L. Yu Chun, Dirk E. Englund, Alexey V. Akimov, Mikhail D. Lukin, and Hongkun Park. Tailoring light-matter interaction with a nanoscale plasmon resonator. *Physical review letters*, 108(22):226803, 2012.

[66] Lionel Friedman, Richard A Soref, and Joseph P Lorenzo. Silicon double-injection electro-optic modulator with junction gate control. *Journal of applied physics*, 63(6):1831–1839, 1988.

[67] CZ Zhao, GZ Li, EK Liu, Y Gao, and XD Liu. Silicon on insulator mach–zehnder waveguide interferometers operating at 1.3 μm. *Applied physics letters*, 67(17):2448–2449, 1995.

[68] Vilson R Almeida, Qianfan Xu, Carlos A Barrios, and Michal Lipson. Guiding and confining light in void nanostructure. *Optics Letters*, 29(11):1209–1211, 2004.

[69] Qianfan Xu, Bradley Schmidt, Sameer Pradhan, and Michal Lipson. Micrometre-scale silicon electro-optic modulator. *Nature*, 435(7040):325, 2005.

[70] William MJ Green, Michael J Rooks, Lidija Sekaric, and Yurii A Vlasov. Ultra-compact, low rf power, 10 gb/s silicon mach-zehnder modulator. *Optics express*, 15(25):17106–17113, 2007.

[71]

[72] Xiaonan Chen, Yun-Sheng Chen, Yang Zhao, Wei Jiang, and Ray T Chen. Capacitor-embedded 0.54 pj/bit silicon-slot photonic crystal waveguide modulator. *Optics Letters*, 34(5):602–604, 2009.

[73] Kyle Preston, Sasikanth Manipatruni, Alexander Gondarenko, Carl B Poitras, and Michal Lipson. Deposited silicon high-speed integrated electro-optic modulator. *Optics express*, 17(7):5118–5124, 2009.

[74] Kapil Debnath, Liam O'Faolain, Frederic Y Gardes, Andreas G Steffan, Graham T Reed, and Thomas F Krauss. Cascaded modulator architecture for wdm applications. *Optics Express*, 20(25):27420–27428, 2012.

[75] Takeshi Baba, Suguru Akiyama, Masahiko Imai, Takeshi Akagawa, Masashi Takahashi, Naoki Hirayama, Hiroyuki Takahashi, Yoshiji Noguchi, Hideaki Okayama,

Tsuyoshi Horikawa, et al. 25-Gbps operation of silicon pin mach-zehnder optical modulator with 100-μm-long phase shifter. In *CLEO: Science and Innovations*, pages CF2L–3. Optical Society of America, 2012.

[76] F. Y. Gardes, G. T. Reed, N. G. Emerson, and C. E. Png. A sub-micron depletion-type photonic modulator in silicon on insulator. *Optics Express*, 13(22):8845–8854, 2005.

[77] FY Gardes, A Brimont, P Sanchis, G Rasigade, D Marris-Morini, L O'Faolain, F Dong, JM Fedeli, Pieter Dumon, L Vivien, et al. High-speed modulation of a compact silicon ring resonator based on a reverse-biased pn diode. *Optics express*, 17(24):21986–21991, 2009.

[78] Jong-Bum You, Miran Park, Jeong-Woo Park, and Gyungock Kim. 12.5 gbps optical modulation of silicon racetrack resonator based on carrier-depletion in asymmetric pn diode. *Optics express*, 16(22):18340–18344, 2008.

[79] Jeong Woo Park, Jong-Bum You, In Gyoo Kim, and Gyungock Kim. High-modulation efficiency silicon mach-zehnder optical modulator based on carrier depletion in a pn diode. *Optics express*, 17(18):15520–15524, 2009.

[80] Tsung-Yang Liow, Kah-Wee Ang, Qing Fang, Jun-Feng Song, Yong-Zhong Xiong, Ming-Bin Yu, Guo-Qiang Lo, and Dim-Lee Kwong. Silicon modulators and germanium photodetectors on soi: monolithic integration, compatibility, and performance optimization. *IEEE Journal of Selected Topics in Quantum Electronics*, 16(1):307–315, 2009.

[81] Douglas M Gill, Mahmoud Rasras, Kun-Yii Tu, Young-Kai Chen, Alice E White, Sanjay S Patel, Daniel Carothers, Andrew Pomerene, Robert Kamocsai, Craig Hill, et al. Internal bandwidth equalization in a cmos-compatible si-ring modulator. *IEEE Photonics Technology Letters*, 21(4):200–202, 2009.

[82] SJ Spector, MW Geis, ME Grein, RT Schulein, JU Yoon, DM Lennon, F Gan, G-R Zhou, FX Kaertner, and TM Lyszczarz. High-speed silicon electro-optical modulator that can be operated in carrier depletion or carrier injection mode. In *Conference on Lasers and Electro-Optics*, page CFH4. Optical Society of America, 2008.

[83] Philip Sibson, Jake E Kennard, Stasja Stanisic, Chris Erven, Jeremy L O'Brien, and Mark G Thompson. Integrated silicon photonics for high-speed quantum key distribution. *Optica*, 4(2):172–177, 2017.

[84] Melissa Ziebell, Delphine Marris-Morini, Gilles Rasigade, Jean-Marc Fédéli, Paul Crozat, Eric Cassan, David Bouville, and Laurent Vivien. 40 gbit/s low-loss silicon optical modulator based on a pipin diode. *Optics express*, 20(10):10591–10596, 2012.

[85] Ching Eng Png, Seong Phun Chan, Soon Thor Lim, and Graham T. Reed. Optical phase modulators for MHz and GHz modulation in silicon-on-insulator (SOI). *Journal of lightwave technology*, 22(6):1573, 2004.

[86] C. Angulo Barrios, V. R. Almeida, R. Panepucci, and M. Lipson. Electrooptic modulation of silicon-on-insulator submicrometer-size waveguide devices. *Journal of Lightwave Technology*, 21(10):2332–2339, 2003.

[87] Erman Timurdogan, Cheryl M. Sorace-Agaskar, Jie Sun, Ehsan Shah Hosseini, Aleksandr Biberman, and Michael R. Watts. An ultralow power athermal silicon modulator. *Nature communications*, 5:4008, 2014.

[88] U Gösele and Q-Y Tong. Semiconductor wafer bonding. *Annual Review of Materials Science*, 28(1):215–241, 1998.

[89] W. P. Maszara, Goetz Goetz, A. Caviglia, and J. B. McKitterick. Bonding of silicon wafers for silicon-on-insulator. *Journal of Applied Physics*, 64(10):4943–4950, 1988.

[90] Hesam Moradinejad, Amir H. Atabaki, Amir H. Hosseinia, Ali A. Eftekhar, and Ali Adibi. High-Q resonators on double-layer SOI platform. In *2013 Photonics Conference (IPC)*, pages 430–431. IEEE, 2013.

[91] S. B. Ben Streetman. *Solid State Electronic devices*. Pearson, 2005.

[92] Di Liang, Alexander W. Fang, Hyundai Park, Tom E. Reynolds, Keith Warner, Douglas C. Oakley, and John E. Bowers. Low-temperature, strong SiO_2-SiO_2 covalent wafer bonding for III–V compound semiconductors-to-silicon photonic integrated circuits. *Journal of Electronic Materials*, 37(10):1552–1559, 2008.

[93] Q.-Y. Tong, G. Fountain, and P. Enquist. Room temperature SiO_2/SiO_2 covalent bonding. *Applied Physics Letters*, 89(4):042110, 2006.

[94] Peter P. Gillis and J. J. Gilman. Double-cantilever cleavage mode of crack propagation. *Journal of Applied Physics*, 35(3):647–658, 1964.

[95] S. Mack, H. Baumann, and U. Gösele. Gas development at the interface of directly bonded silicon wafers: investigation on silicon-based pressure sensors. *Sensors and Actuators A: Physical*, 56(3):273–277, 1996.

[96] Donato Pasquariello and Klas Hjort. Plasma-assisted InP-to-Si low temperature wafer bonding. *IEEE Journal of Selected Topics in Quantum Electronics*, 8(1):118–131, 2002.

[97] LI Popova, E. D. Atanassova, S. K. Peneva, and E. A Tcukeva. On the structure of thin plasma-treated thermal SiO_2 films. *Crystal Research and Technology*, 23(8):979–988, 1988.

[98] Karin Ljungberg, Anders Söderbärg, and Ulf Jansson. Improved direct bonding of Si and SiO_2 surfaces by cleaning in H_2SO_4:H_2O_2:HF. *Applied Physics Letters*, 67(5):650–652, 1995.

[99] Haisheng Rong and Ansheng Liu. Optical modulator utilizing wafer bonding technology, May 28 2011. US Patent 8,450,186.

[100] Ling Liao, Desmond R. Lim, Anuradha M. Agarwal, Xiaoman Duan, Kevin K. Lee, and Lionel C. Kimerling. Optical transmission losses in polycrystalline silicon strip waveguides: effects of waveguide dimensions, thermal treatment, hydrogen passivation, and wavelength. *Journal of electronic materials*, 29(12):1380–1386, 2000.

[101] Ling Liao. *Low loss polysilicon waveguides for silicon photonics*. PhD thesis, Massachusetts Institute of Technology, 1997.

[102] P Allongue. Molecular imaging and local density of states characterization at the si (111)/naoh interface. *Physical review letters*, 77(10):1986, 1996.

[103] MA Gosálvez, K Sato, AS Foster, RM Nieminen, and H Tanaka. An atomistic introduction to anisotropic etching. *Journal of Micromechanics and Microengineering*, 17(4):S1, 2007.

[104] MA Gosálvez, D Cheng, Risto M Nieminen, and K Sato. Apparent activation energy during surface evolution by step formation and flow. *New Journal of Physics*, 8(11):269, 2006.

[105] Miguel A Gosálvez, I Zubel, and Eeva Viinikka. Wet etching of silicon. In *Handbook of silicon based MEMS materials and technologies*, pages 447–480. Elsevier, 2010.

[106] Kevin K. Lee, Desmond R. Lim, Lionel C. Kimerling, Jangho Shin, and Franco Cerrina. Fabrication of ultralow-loss Si/SiO_2 waveguides by roughness reduction. *Optics Letters*, 26(23):1888–1890, 2001.

[107] Lumerical FDTD. Lumerical Solutions, Inc. Version: 2017a. https://www.lumerical.com/products/fdtd/.

[108] Lumerical CHARGE. Lumerical Solutions, Inc. Version: 2017a. https://www.lumerical.com/products/charge/.

[109] Hirofumi Ohki and Hitoshi Takemura. 100 kv electron beam lithography system: Jbx-9300fs. *JEOL News E*, 35, 2000.

[110] Richard C Jaeger. *Introduction to microelectronic fabrication*, volume 2. Prentice Hall Upper Saddle River, NJ, 2002.

[111] Paul R Gray, Paul J Hurst, Stephen H Lewis, and Robert G Meyer. *Analysis and design of analog integrated circuits*. John Wiley & Sons, 2009.

[112] Shinichi Saito, Isao Tomita, Moïse Sotto, Kapil Debnath, James Byers, Abdelrahman Z. Al-Attili, Daniel Burt, Muhammad K. Husain, Hideo Arimoto, Kouta Ibukuro, et al. Si photonic waveguides with broken symmetries: applications from modulators to quantum simulations. *Japanese Journal of Applied Physics*, 59(SO):SO0801, 2020.

[113] Shinichi Saito, Moise Sotto, Kapil Debnath, James Byers, Abdelraham Al-Attili, Tomita Isoa, Burt Daniel, Mohammed K. Husain, Kouta Ibukuro, David J. Thomson, Weiwei Zhang, Bigeng Chen, Frederic G. Gardes, Graham T. Reed, and Harvey N. Rutt. Novel Si photonic waveguides and applications to optical modulators (invited). In *The Twenty-Forth Microoptics Conference (MOC2019)*, page 2. JSAP, 2019.

[114] Isao Tomita, Kapil Debnath, Kouta Ibukuro, M. K. Husain, James Byers, Zhiming Zhang, and Shinichi Saito. $LiNbO_3$/Si-hybrid slot-waveguide electro-optic modulators. In *2018 IEEE 15th International Conference on Group IV Photonics (GFP)*, pages 1–2. IEEE, 2018.