

UNIVERSITY OF SOUTHAMPTON

**High Performance CMOS modulator  
drivers for Silicon Photonics  
Mach-Zehnder Modulator**

by

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ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING  
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The modulator driver is a crucial electrical module within the optical transceiver. All the data to be conveyed optically must pass through this device, which typically requires it to operate at the highest operation speed of any electrical modules among the whole communication system. In addition, due to the weakness of the electro-optical effects of these high-speed modulators, the driver must produce relatively large voltage swing, which not only exceeds the nominal breakdown voltage of these ultra-deep-submicron CMOS technologies, but also leads to the concerns about the power efficiency and thermal reliability.

To address all these challenges, this work commenced from the design and implementation of a new driver circuit at 40nm CMOS technology. Silicon proven results demonstrated this new circuit could operate properly up to 40Gb/s. Thanks to the experience and knowledge base of the Silicon Photonics team that author is embedded into, a holistic solution has been proposed as a synergistic design approach between the CMOS driver and the depletion type Si MZM. The proposed solution has been illustrated from circuit-level design to real chip tape-out at 28nm process node, which not only features with the outstanding power efficiency (1.6 pJ/bit) and operation speed(40Gb/s), but also enabled the compact integration among optical and electrical component. In addition, target on the thermal reliability issue, a CMOS driver circuit has been proposed and demonstrated with relatively stable performance over the temperature range 27°C to 110°C.

The endless effort has been made and will continuously be devoted to speed enhancement and the optimization of power efficiency on each generation of the optoelectrical transceiver. It is hoped some of the research outcome recorded in this work will become as a step-stone for future research, where the driver and modulator will be co-designed as a complex function for the future communication system.



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# Nomenclature

<i>NTRS</i>	National Road-map for Semiconductors
<i>CMOS</i>	Complementary metal-oxide-semiconductor
<i>Txline</i>	transmission line
<i>InP</i>	Indium phosphide
<i>GaAs</i>	Gallium arsenide
<i>LiNbO<sub>3</sub></i>	Lithium niobate
<i>MZM</i>	Mach-Zehnder modulator
<i>Si</i> or <i>si</i>	Silicon
<i>RRM</i>	Ring resonator modulator
<i>RF</i>	Radio frequency
<i>UKSP</i>	UK Silicon Photonics
<i>SPFS</i>	Silicon Photonics for Future Systems
<i>EPSRC</i>	Engineering and Physical Sciences Research Council
<i>NRZ</i>	None return zero
<i>PLL</i>	Phase lock loop
<i>PD</i>	Photo detector
<i>LA</i>	Limiting amplifier
<i>TIA</i>	Trans-impedance amplifier
<i>CDR</i>	Clock and data recovery
<i>SerDes</i>	Serializer and de-serializer
<i>S2D</i>	Single to differential converter
<i>EAM</i>	Electrodeposition modulator
<i>MZI</i>	Mach-Zehnder interferometer
<i>MSM</i>	Metal-semiconductor-metal
<i>SOI</i>	Silicon on insulator
<i>CML</i>	Current mode logic
<i>DA</i>	Distribute amplifier
<i>WDM</i>	Wavelength-division multiplexing
<i>PAM</i>	Pulse amplitude modulation
<i>OMA</i>	Optical modulating amplitude
<i>ER</i>	Extinction ratio
<i>MSB</i>	Most significant bit

<i>LSB</i>	Least significant bit
<i>QPSK</i>	Quadrature Phase-Shift Keying
<i>PDM</i>	Polarization-division-multiplex
<i>QAM</i>	Indium phosphide
<i>TM</i>	Transverse electric
<i>TE</i>	Transverse magnetic
<i>DMT</i>	Discrete multi-tone
<i>FFT</i>	Fast Fourier transform
<i>IFFT</i>	Inverse fast Fourier transform
<i>DML</i>	Directly modulated laser
<i>AWG</i>	Arbitrary waveform generator
<i>DSO</i>	Digital storage oscilloscope
<i>OFDM</i>	Orthogonal frequency-division multiplex
<i>PRBS</i>	Pseudo random binary sequence
<i>FOM</i>	Figure of merit
<i>EDFA</i>	Erbium-Doped Fiber Amplifier
<i>BER</i>	Bit error ratio
<i>DUT</i>	Design under test
<i>BGR</i>	Band gap reference
<i>ADS</i>	Advanced Design System
<i>DRC</i>	Design Rule Check
<i>LVS</i>	Layout VS Schematic

# Chapter 1

## Introduction

### 1.1 Interconnect bottleneck and silicon photonics

It is an understatement to remark that the modern world is becoming reliant on a computing technology that depends on silicon technology. Almost all industries are now driven by advanced technology based on integrated electronic circuits which are fabricated on silicon wafers. Along with the demand for large quantities of high performance and powerful computing components in all industries, the development of silicon-based manufacturing has evolved rapidly. In 1965, the famous Gordon Moore's law, which states that development progress is similar to an economic project plan,

- The complexity for minimum component costs has increased at a rate of approximately a factor of two per year.[78]

The complexity may be understood as either the number of transistors or the computing performance of the smallest component. Depending on the development of the manufacturing process, the transistor size is both gradually reduced and its speed becomes faster. Therefore, in the past few decades, the electronics manufacturing industry though has been recently slowed down, has been following Moore's Law.

However, a serious problem challenging Moore's Law has been noticed and summarized in a report by the National Road-map for Semiconductors (NTRS), which states that, along with the progress of semiconductor manufacturing technology, although the transistor size and speed have been optimized, the interconnection has become a bottleneck. Fig.1.1 is extracted from the NTRS 1997 reports and it clearly describes the problem that is after the 200nm gate feature size, the interconnection delay is dominating the overall delay. No matter on which conductor and dielectric metrical, the interconnection metal is thinner and narrower while the process development. The RC capacitive charging and discharging delay dominates the overall performance of integrated circuits. A modern

electronic chip contains over  $1\text{km}$  length of metal wires on  $1\text{cm}^2$  chip area, therefore the interconnection delay is the inhibition of chip performance.[\[45\]](#) The exposure problem is often referred to as the interconnect bottleneck.

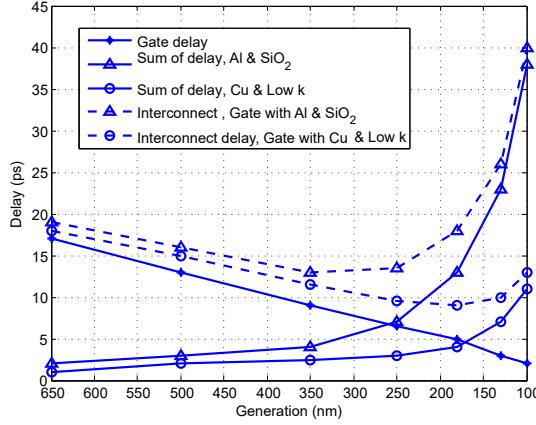


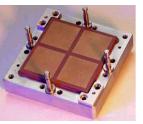
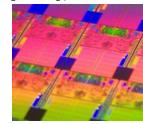
FIGURE 1.1: Gate and Interconnection Delay feature versed Technology Generation [\[81\]](#)

An interconnect bottleneck not only directly affects the continuity of Moore's Law, but it is also an indicator that the limits of electrical transmission progress are approaching. Not only the on-chip interconnections, but all the electrical connections between chips, and between chips and devices, will also be affected, because, as transmission rates increase, the attenuation of the high frequency signal in the transmission line (Tx line) also increases significantly. Current solutions for interconnect bottlenecks could be summarized as increasing the pin counts of chips (more parallel signals), optimizing the low-k dielectrics or limiting the distance of interconnections. However, according to updates of the ITRS report relating to interconnects and packaging[\[46\]](#), these traditional electrical interconnect optimizations may difficult to satisfy future performance requirements.

The interconnect bottleneck, which is difficult to solve by traditional electrical methods may be resolved by optical technology. Many expect photonics to provide a solution that relieves the interconnect bottleneck in the long term.[\[28; 36; 75; 78\]](#) The potential benefits of optical interconnections include delay reductions, crosstalk removal, and power consumption reduction. Traditional optical devices made from III-V-based compounds such as indium phosphide (*InP*), gallium arsenide (*GaAs*) or the electro-optic crystal lithium niobate (*LiNbO<sub>3</sub>*) could be used to replace traditional electrical connections between chips or modules. But these solutions come at either higher manufacturing and materials costs, or they will require a large layout area. In addition, they are often custom-made and are assembled from discrete components which are hand-assembled and require very little automation.[\[36\]](#) More importantly, they are too difficult to be integrated into the CMOS computing chips and replaces the on-chip interconnections. Aside of these traditional optical devices, another obvious solution is the silicon photonics.

Firstly, silicon gains the manufacturing experience which has been the mainstay of the

TABLE 1.1: Evolution of optical interconnects (Courtesy of M. Taubenblatt [112])

					
	<b>LAN</b> Rack level	<b>System</b> Card level	<b>Board</b> On Card	<b>Module</b> Chip level	<b>Sub module</b> On-chip
Distance	30+m	Less 1m	0.1-0.3m	5-100mm	0.1-10mm
Number of lines	~ 100	~ 100 – 1000	~ 1000	~ 10'000	~ 100'000

electronics industry for more than 40 years. The feature sizes needed for processing these silicon waveguides are on the order of  $0.5 - 1\mu m$ . Therefore, even with 90-nm CMOS lithography, it is still sufficient to fabricate the optical device on the silicon wafer.[36] Silicon is also used for fabricating electrons and holes that are also required in silicon active optic devices to modulate the optical signals.

Secondly, silicon photonics provides an important compatible possibility with existing CMOS fabrications. Only if implementing the optical device and the state of the art CMOS computing device in the same silicon die (monolithic photonics platform), the on-chip interconnection could be replaced as an optical connection.[109]

Thirdly, unlike the traditional optical devices, the size and scale of silicon photonics devices could be closer to the state of the art CMOS devices, since these minimal sized silicon photonics modulators and detectors only occupy tens of square microns layout areas.[28; 109] These small size designs are similar to the nanometer scale CMOS devices.

Finally, the advantages of silicon-based manufacturing in terms of materials and lower costs are significant, since clearly, in interconnection, which has an extremely wide range of application, high-cost technology is unlikely to be widely implemented.

Table 1.1 demonstrates the evolution of optical interconnects, it covers the rack level communication which mainly serves the data centers to on-chip communications. As research has progressed, the transmission distance has gradually decreased, while the number of lines has rapidly increased dramatically. Especially in the module and sub module stages, based on existing computing components in silicon-based manufacturing, almost only silicon photonics can be an effective solution.

## 1.2 Motivation and objectives

Although silicon photonics have their advantages, the modulation (or generation) and detection of optical signals is highly challenging. Especially in the si modulators, limited by the properties of silicon-based materials, both the reliability and efficiency of the device need to be concerned. The depletion-type si Mach-Zehnder modulator (MZM)

is well researched in the silicon photonics. Though the MZM is always devalued for its relatively inferior power efficiency and large footprint, the fact is that depletion-type si MZM is almost always preferred because of its practical benefits. In comparison to carrier injection modulators and the Ring Resonator Modulators (RRM), depletion-type si Mach-Zehnder modulator has its advantages in the speed modulation reliability and environmental tolerance.[37]

According to a recent publications, the si MZM has already attained over 90Gb/s NRZ optical modulation.[128] However this result, like most other MZM transmission experiments, is based on the testing setup using all commercial modulator drivers. In the testing and research phase, testing using commercial equipment is faultless, however, a reality reveals is that a significant gap has already appeared between these commercial devices and future applications of silicon photonics. Commercial modulator drivers are usually a broadband radio frequency (RF) amplifier, which is quite difficult to integrate to the MZMs due to its huge volume. Simultaneously, the power consumption of these amplifiers is now more than 1W, which suggests that optical transmitter efficiency of the optical transmitter has now moved beyond the practical stage. Additionally, most commercial devices are not built on the CMOS technology. In future, silicon photonics, no matter how monolithic their photonics platform level integration or other integrations with CMOS based computing units are, such commercial devices are almost impossible integrate efficiently into the systems.

The optical transmitter should not only be an electric-optical transforming device, but a combinational circuit or system, which, most importantly, should include the electrical devices available to directly integrate with the state of the art CMOS computing units. Therefore, it is essential to build modulator drivers that rely only on CMOS technology. A proper modulator driver needs to demonstrate not only enough bandwidth performance but that it is also sufficiently efficient for it to be integrated into the MZM.

In 2011, the state of the art silicon photonics research shows the si depletion MZM [116] is functional up to 40Gb/s. But this result is based on commercial driver devices in the testing lab. For future silicon photonics circuit and related applications, it is difficult to broadly use commercial driver due to the size (at least several  $mm^2$  per driver) and power consumption (could be over Watt). To optimize the opto-electronic circuit from the discrete devices level to the compacted packaged level, and to provide a driver that has a low area cost and low power consumption, CMOS based optical modulator driver design is one of several options. The cost of the CMOS process is much lower than III/V material ones and even lower than a BiCMOS process. A further advantage of the CMOS process creates a possibility to build drivers as IO of the processing unit including computing elements, DSP units and/or SerDes systems, which is also using standard CMOS process. Although the BiCMOS process is compatible with both Bipolar and CMOS transistors, the CMOS used in the BiCMOS process is much slower than the current method which is not appropriate for processing units.

In order to provide a proper CMOS modulator driver, this PhD project aims to establish optical transmitter, based on si MZM with a CMOS circuit at, or over, 40Gb/s data transmission that meets the si MZM, which has been presented in 2012. Even in latter phase of this project, the current Si photonics modulator has reached 90Gb/s[128], while most industrial optical interconnect level applications is still at or lower than 40Gbaud/s per electric IO[21; 22]. Therefore, the 40Gb/s opto-electronic transmitter which includes a CMOS modulator driver, is an alternative in terms of this project's research target. The reliability, efficiency and integration methods of CMOS modulator driver should be researched in this project. The MZM samples which integrates with the modulator driver should be provided by the co-operative optical designer in the same research project.

Between 2012 and 2018, while the author has been working on this PhD, silicon photonics technology has undergone six years of rapid development. During the period, most state of the art CMOS based modulator drivers for MZM amounted only to approximately 10Gb/s and it required a high power consumption. Today's MZM, however, is functional upto 90Gb/s with the commercial testing devices, and the CMOS circuit which integrates with MZM, operates to a level higher than 40Gb/s.

At the beginning of the PhD project, MZM temperature reliability was well understood, however, the modulator driver, which provides performance independent of temperature was too expensive. In addition, the author lacked high-speed CMOS circuit design experience; therefore, it was the first time the author has been involved with the opto-electronic design. The topic then become high speed low power design as it relates to temperature reliability, whereas the first CMOS design, which was the project's original subject, related to circuit research and design.

Following the first design, during the second year of this project, I proposed a novel structure which optimized the conventional push pull modulator driver to enable it to attain a higher operating speed alongside a lower power consumption. During the next two years, the modulator driver was modified and optimized in two tape outs within two different CMOS processes. The final result enables the modulator driver to operate at 40Gb/s transmission with relatively low power consumption.

In late 2015, together with colleagues, author devised a novel plan that consisted of a U-shape MZM and an efficient modulator driver. The electric chip design I was working on for the optical device unfortunately had to be abandoned, for 20 months as I contracted lymphoma. Although the author contributed to the research, the electronic circuit design was completed by a colleague. In late 2017, after the lymphoma was in complete remission, I continued with integrating and testing for the optical transmitter, in late 2018, the project came to an end.

The author's PhD is a sub-topics of two continued research projects in University of Southampton. These two research projects are on the order of UK Silicon Photonics

(UKSP) and Silicon Photonics for Future Systems (SPFS) which are both funded by Engineering and Physical Sciences Research Council (EPSRC).

### 1.3 Thesis Organization and Contributions

This thesis is structured as follow:

The state of the art is reviewed in the Chapter 2. The chapter is divided into six sections which review the general optical transceivers, optical devices and related electronic circuits, integration methods of silicon photonics, high speed amplifier design methodologies, the output stage structures and the complex modulation on silicon photonics.

Chapter 3 provides a novel N-over-N cascode amplifier structure to optimize the state of the art CMOS modulator drivers. The chapter theoretical analysis the proposed amplifier structure, compared the circuit with conventional circuit topologies, and provide two parts of optimizations on the proposed circuit.

Chapter 4 includes three implementations bases on the proposed circuit in Chapter 3. These three implementations on the order to demonstrate the functionality of N-over-N cascode amplifier and two optimizations. Each implementation is independent designed and analyzed. Both the simulation and experimental testing result are also included in the chapter.

Chapter 5 provides a efficient optical transmitter design which includes the CMOS driver. This design is a synergistic design which contributes by both of the optical and electric designers in the research projects. Rely on the synergistic design technology, the MZM is embedded into the electronic circuit design. Apart of the theoretical analysis which focuses on the electronic circuit design and the top-level topologies and integration is presented in the chapter. In addition, to use the optical transmitter to demonstrate an efficiency PAM4 optical transmitting, an analysis PAM4 modulating on si MZM is followed in the chapter.

Chapter 6 includes the implementations result of the synergistic designed optical transmitter which is analyzed in Chapter 5. The experimental result demonstrates the NRZ transmission, bit error ratio test and the PAM4 transmission of the design.

Chapter 7 provides a optimized temperature variation tolerance modulator driver design methodology. The proposed circuit demonstrates high reliability in unstable thermal environment. The modulator driver could be used for MZM which avoids the electric signal integrity loss in high temperature.

Chapter 8 demonstrates the implemented circuit which bases on the analysis in chapter 7. With a on-chip control loop, the modulator driver provides almost no damaged signal up to 12.5Gb/s in a wide temperature range.

Chapter 9 concludes this thesis with a summary of the research outcome in this project. Several potential research ideas have been discussed as continuously work for this PhD project.

Finally, it is necessary to point out that this thesis has covered a wide range of technical topics, include the design and fabrication of optical devices, the packaging and integration of photonics and electronic devices, the design and simulation of high-speed CMOS circuit, the functional verification and performance characterization of the optical transmitter. Apparently, all these works require team-work among many research colleagues. It is therefore necessary to clarify the contribution made by the author.

- Firstly, the author mainly focuses on the design and characterization of CMOS circuit whereas the design and fabrication of these optical devices are finished by the colleagues in the Silicon Photonics Group.
- Secondly, the beginning of this PhD project commenced from the design and modelling of the temperature behavior of high-speed CMOS amplifier. A self-sustained temperature tolerant CMOS amplifier is proposed by the author with its functionality verified by a series testing results.
- Thirdly, the idea of N-over-N cascode amplifier is proposed by the author and the concept is demonstrated and characterized by the electrical tape-out at TSMC 40nm CMOS process node.
- Finally, the last contribution of this PhD project is the synergistic designed optical transmitter which consists of a U-shaped MZM and 28nm CMOS driver. It is an honor that the author has deeply involved with the invention and discussion of this idea at the beginning of it. It is a regret that author missed the circuit design and fabrication stage due the severe illness. It is so lucky that after 20 months of medical treatment, the author recovered from the illness and caught up with the integration and testing stage of this work.

8 publications have arisen from this work in the author's PhD period. The published articles are 2 journal papers and 6 conference papers. The publishes are listed below:

- Liu Shenghao, Li Ke and Wilson Peter R. (2015) **A temperature independent driver for Mach-Zehnder modulators.** ISCAS 2015: IEEE International Symposium on Circuits and Systems, Portugal. 24 - 27 May 2015.
- Li Ke, Thomson D., Wilson Peter R., Liu Shenghao and Reed Graham T. (2015) **A 30 Gb/s CMOS driver integrated with silicon photonics MZM.** RFIC 2015: 2015 IEEE Radio Frequency Integrated Circuits Symposium, RFIC2015/Microwave Week 2015, United States. 17 - 19 May 2015.

- Reed G.T., Li K., Thomson D.J., Liu S., Wilson P.R., Hu Y., Gardes F.Y., and Mashanovich G.Z., **Devices for an integrated Silicon Photonics platform**, International Photonics and Optoelectronics Meetings (POEM), Wuhan, China, 13-20 Jun. 2015 (Invited)
- Liu Shenghao, Thomson D., Li K., Wilson Peter and Reed Graham T. (2015) **N-over-N cascode push-pull modulator driver in 130nm CMOS enabling 20Gb/s optical interconnection with Mach-Zehnder modulator.** Electronics Letters, 51 (23), 1900-1902.
- Cao Wei, Hagan David, Thomson David J., Nedeljkovic Milos, Littlejohns Callum G., Knights Andy, Alam Shaif Ul, Wang Junjia, Gardes Frederic, Zhang Weiwei, Liu Shenghao, Li Ke, Rouifed Mohamed Said, Xin Guo, Wang Wanjun, Wang Hong, Reed Graham T. and Mashanovich Goran Z. (2018) **High-speed silicon modulators for the 2 m wavelength band.** Optica, 5 (9), 1055-1062.
- Thomson David, Gardes Frederic, Debnath Kapil, Zhang Weiwei, Li Ke, Liu Shenghao, Meng Fanfan, Khokhar Ali, Littlejohns Callum, Byers James, Mastronardi Lorenzo, Husain Muhammad, Saito Shinichi, Chen Xia, Miloevic Milan, Franz Yohann, Runge Antoine F.J., Mailis Sakellaris, Peacock Anna, Wilson Peter and Reed Graham (2018) **Towards high speed and low power silicon photonic data links.** ICTON 2018 - International Conference on Transparent Optical Networks, Bucharest. 01 - 05 Jul 2018.
- Liu Shenghao , Thomson Dave J., Li Ke, Wilson Peter and Reed Graham T. (2018) **A 40Gb/s low power CMOS driver for MZM.** European Optical Society Biennial Meeting (EOSAM) Delft, Netherlands, Oct. 2018
- Li Ke, Thomson David, Liu Shenghao, Meng Fanfan, Shakoor Abdul, Khokhar Ali, Cao Wei, Zhang Weiwei, Wilson P. and Reed G.T. (2018) **Co-design of electronics and photonics components for Silicon Photonics transmitters.** In 44th European Conference on Optical Communication. OSA.

# Chapter 2

## States of the Art

In the past years, the research on Silicon Photonics gains a significant amount of momentum. In both interconnection and long-haul communication applications, some of the commercial transceivers on silicon photonics has been produced. A growing number of silicon photonics research is not limited to the devices, but to the silicon photonics circuit and system. Silicon photonics has the integration advantages with CMOS chips; therefore the electronic chip technology associated with silicon photons is also evolved. Many electrical chip studies have been continuously improved from traditional circuits to specifically serve silicon photonics circuits and achieving better integration and overall performance results.

This chapter is a literature review covers from a conventional optical transceiver's architecture to a optical transmitter with complex modulating. Since the PhD project is aiming to develop the CMOS circuit for silicon photonics modulators, the states of the art have been focused on the electronic circuits in related area, not just silicon photonics.

### 2.1 Introduction

Hereinafter in this chapter, six sections gradually review the silicon photonics and its related electronic circuit.

Firstly, a conventional optical transceiver has been reviewed and the importance of a modulator drive which acts as the electric-optical interface has been pointing out. Secondly, in order to relate the silicon photonics device to electronic circuits, an introduction covers types of optical devices. After that, a review illustrates three integration method for electronic and optical devices. Then, there are two sections on the order reviewing the high speed amplifier and output stage circuit for optical modulators. Lastly, as the most common silicon photonics circuit, the complex modulating optical transmitter is also reviewed.

Due to the target of the author's project, the states of the art chapter has focused on the modulator driver and its related content as the electrical circuit that directly serves the silicon photonics device.

## 2.2 The top Level circuit of optical transceivers

The primary function of the general optical link is to transfer data between the transmitter and receiver via fiber or other optical channels. In Fig.2.1, there is a system level transceiver of the optical data link. In order to focus on the full structure of transceiver, it is not intended for a particular type of modulator or laser as an electro-optic modulator. In this transceiver, the transmission data is assumed as none return zero (NRZ) data with the single wavelength of optical carry wave, and more complex optical modulations are presented in Sec.2.7.

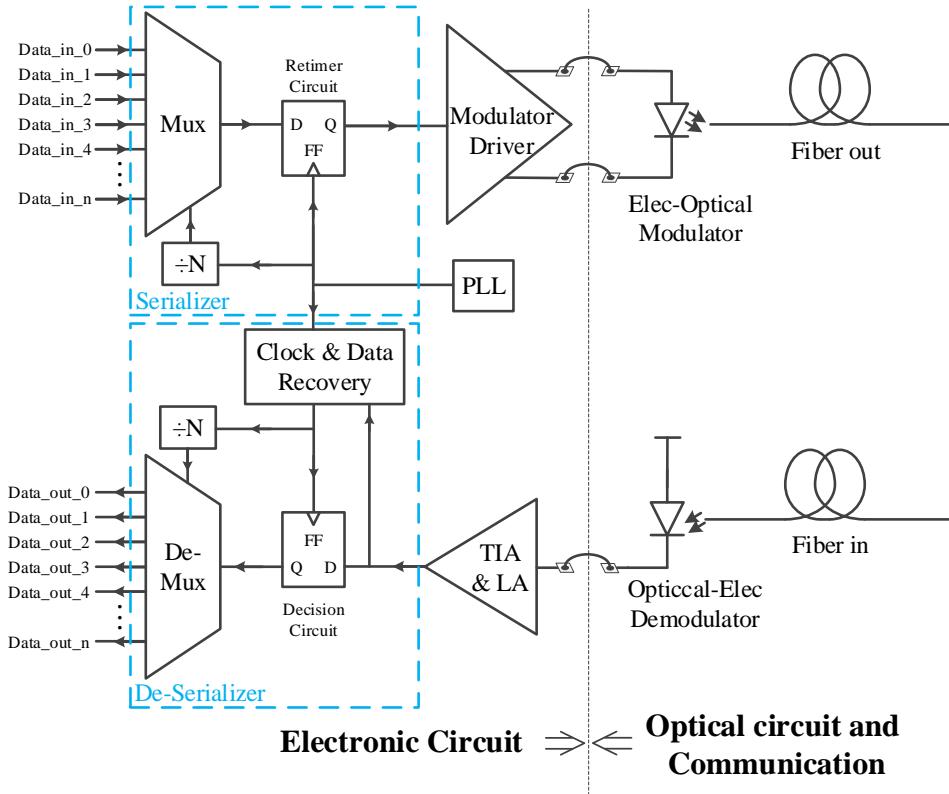


FIGURE 2.1: Abstract view of an example optical data link (edited from [12])

The top half circuit in Fig.2.1 is the optical transmitter. In this transmitter, a serializer circuit consists of the multiplexer, phase lock loop (PLL), re-time Flip Flops and clock frequency divider. With the serializer, parallel channels of low-speed electronic input data can be sped as high-speed serial data. The high speed re-timed electronic data feeds into the modulator driver (in some approach, i.e. VCSEL, it is a laser driver).

Amplified data signal from modulator driver transfers as optical signal in the electro-optical modulator and be transmitted into fiber.

The optical receiver (bottom half) in Fig.2.1) reverses the process of the transmitter. A photo detector (PD) functions as a demodulator, detects the optical signal and converts it to a current signal. A trans-impedance amplifier (TIA) and limiting amplifier (LA) converts the current to a stable voltage mode electric signal. A clock and data recovery (CDR) circuit, decision Flip Flop, de-multiplexer and frequency divider compose the de-serializer circuit. CDR rebuilds a clock which bases on the receiving data and local PLL. Via the de-serializer circuit, the data signal is parallel back to multiple channels, which meets the input signal module.

The transceiver system in Fig.2.1 is a full version for the commercial approach. In this transceiver, serializer and de-serializer (SerDes) circuit with timing system is well-understood and widely used in conventional electronic data links. Therefore, in the silicon photonics research area, the most significant design challenges are focusing on electric-optical modulating and optical-electric demodulating. Instead of presenting a full version, a brief version is presented regarding the optical transceiver in Fig.2.2. This brief version transceiver starts from the modulator driver and ends at TIA and LA.

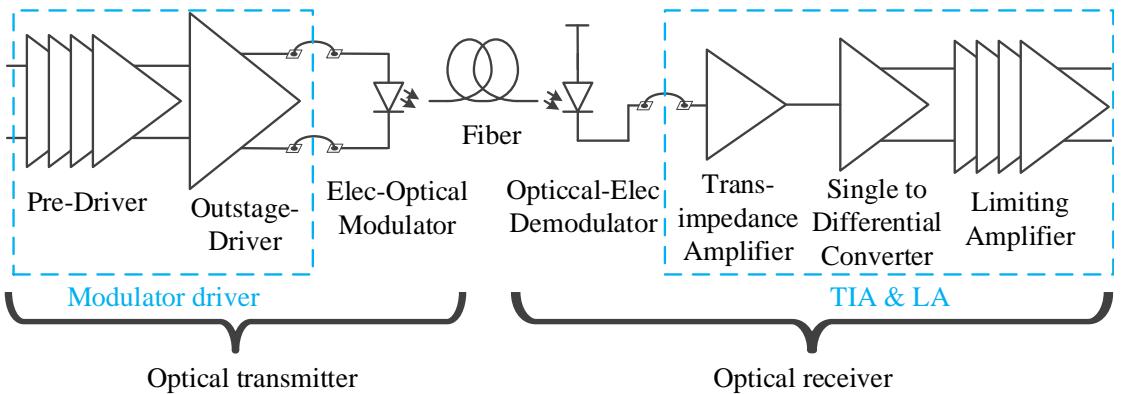


FIGURE 2.2: Abstract view of an example brief optical data link

Fig.2.2 also presents the inner structure of modulator drivers and TIA, LA circuits. Most modulator drivers include two pars, the pre-driver and output stage driver. Pre-driver amplifies the input signal and fed into the output stage. The output stage is always specifically designed for modulators. In most approach, the output stage in the modulator driver is not only an amplifier but also including the integration design. In the optical receiver, some PD and TIA are single end devices. In this approach, to convert the received high speed signal to differential signals, a single to differential converter (S2D) is generally added between the TIA and LA. LA amplifies the TIA output signal (generally TIA output signal is only tens of mV [33]) onto a detectable level for later testing device or latter receiver circuits.

The target of the author's PhD is to design a modulator driver for the silicon-based

Mach-Zehnder modulator (MZM) which reduce power consumption and other costs at the highest possible transfer rate. The design of the modulator driver not only includes knowledge of high-speed circuit design but also provides integration in specific practice. The following sections introduce common optoelectronic devices and the electric circuits that match them, the integration methods of optoelectronic circuits and review the broadband high-speed circuit design for pre-driver and output stages. These knowledge are directly related to the design and integration techniques of the modulator driver.

### 2.3 Common optical devices and circuits

Though author's target is modulator driver design for MZM, a wider range of optical devices and their electric circuits are investigated. Four types of modulators (or laser), VCSEL, EAM, RRM and MZM, are commonly applied as optical transmitting devices. In silicon photonics, these modulators or lasers are also This section reviewed these modulators and demodulator PD with the electronic circuit.

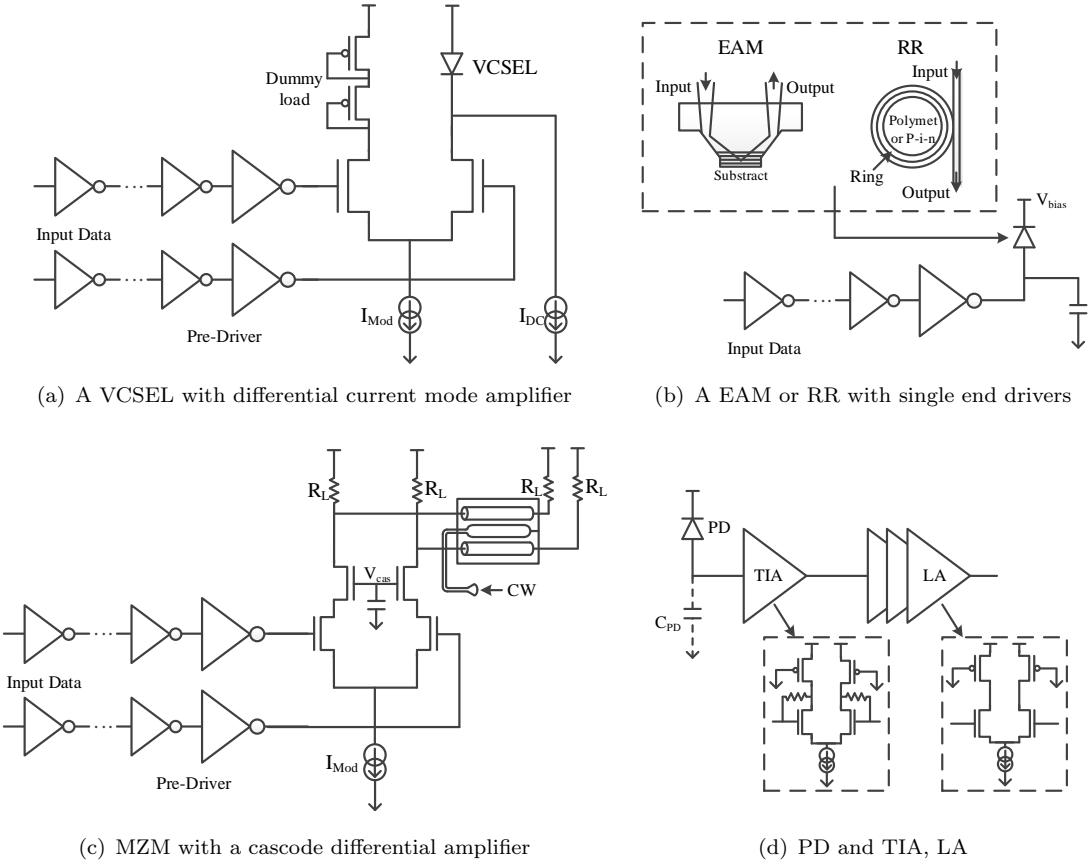


FIGURE 2.3: Schematic of (a) VCSEL (b) EAM and RR (c) MZM with common driving circuit (d)PD & TIA, LA receiving system

- VCSEL

The full name of VCSEL is (Junction) Vertical-Cavity Surface-Emitting Lasers. Since it is a laser, this modulator generates the optical signal by itself. It is a current mode device. Optical power is related to the current going through the device. Due to its linear optical power and driving current relationship being beyond a threshold current region, to drive up this kind of device, an external current bias is necessary. The bandwidth of VCSEL is  $BW_{VCSEL} \propto \sqrt{I_{avg} - I_{th}}$ .<sup>[6; 39]</sup> This kind of device also has fairly good stability at a high temperature.<sup>[39]</sup> A major problem of VCSEL is speed limitation due to both electrical parasitics and carrier-photon interactions. To increase the speed of VCSEL, an electric FFE (feed forward equalizer) is necessary. In <sup>[72]</sup> and <sup>[54]</sup>, while the transmission speed is over 40Gb/s even 56Gb/s, the signal jitter is increasing due to the limitation of FFE. A example of a VCSEL with output stage driver (differential current mode) is shown in Fig.2.3(a)<sup>[6]</sup>.

Currently, IBM and Intel both focus on this type of modulator on the rack to rack and the card to card level optical interconnection. Most VCSEL based optical communication is on a wavelength 850nm <sup>[29; 44]</sup>. However, in recent years, some longer wavelength (i.e. 1300nm, 1530nm) VCSEL is also produced with very good performance<sup>[54; 72]</sup>. VCSELs consume less power than most other modulators in a wide speed range. To boost VCSEL into higher speed, it requires not only increase power on the driver but also a feed forward equalizer to maintain the signal quality.<sup>[29]</sup>

- EAM

An electrodeposition modulator (EAM) is a device based on the Franz-Keldysh effect. To produce a modulated optical signal, EAM needs bias voltage on the device. While an optical carry wave goes through the channel on EAM (Fig.2.3(b), EAM module), the electric field is applied by the voltage signal on EAM. The more overlap there is between the wave functions of free electrons and holes, the higher optical absorption will be. Thus the carry wave power will be modulated while it goes through the device.<sup>[6; 93]</sup>

Due to the carry wave of EAM being generated from external of EAM, this kind of device does not display any speed limitation on carrier-photon interactions. On circuit implementation, EAM is generally regard as a lumped capacitor. Vbias is usually a high Vdd which is not the same as the driver system.<sup>[6]</sup>

A classic electronic and optical integrated design is demonstrated in <sup>[93]</sup>. The electric driver uses the structure in <sup>[125]</sup> and provides 2V output swing for a EAM in 90nm CMOS process. The total transceiver power is 23.6mW at 1.8Gb/s.<sup>[93]</sup> In recent years, EAM has also produced outstanding speed performance in silicon photonics. <sup>[38]</sup> from IMEC presents an EAM and PD array based on a germanium silicon process and is functional at 56Gb/s per channel for a short reach connection. Moreover, EAM in <sup>[84]</sup> also works at 50Gb/s with 2Vpp signal which is suitable to integrate with CMOS drivers.

- RRM

Ring resonator modulators (RRM) are on either p-i-n diode material (silicon based) or polymer material (carbon polymer based). Electro-optic polymer based RR[7] could avoid the bandwidth limitations of p-i-n diode based RR[3]. However, the p-i-n diode is closer to silicon integration. As Fig.2.3(b) presents, RRM is located on the side of an optical waveguide. While the optical carry wave goes through this waveguide, RR could modulate the optical signal by the voltage level on the p-i-n junction. The modulated optical signal could directly transmit from the waveguide.[6]

Since each RRM can be effective at a very narrow wavelength, RR is exceptionally easy to use for WDM[63; 70]. Also, the size of RRM could be smaller than other types of modulators. Consider about the silicon based RRM, it is closer to integration the optical device with traditional silicon computing systems on the same silicon die[64; 109].

The model of RRM is similar to EAM (Fig.2.3(b)). The RRM can be consider as a lump capacitor for modulator driver design. A significant problem of RRM is temperature variation. RR is very sensitive to process and temperature, while with temperature variations, the modulation wavelength will be shifted. Therefore on a useful RRM system, an additional (not be shown in Fig.2.3(b)) tuning heater with control loop to maintain the temperature environment around RR is necessary.[6; 108].

- MZM

[37] presents the carrier accumulation, carrier injection and carrier depletion of silicon Mach-Zehnder modulator (MZM). In the reason of carrier depletion silicon MZM provides the best bandwidth performance and author's job is around this type of modulators, the MZM hereinafter is the carrier depletion silicon MZM.

MZM is an optical modulator which works on free carrier plasma dispersion effect. The input waveguide is split up into two waveguide interferometer arms. Each arm is a Mach-Zehnder interferometer (MZI), and the optical signal will be phase shifted in each arm. While two optical signals are merged back together, the phase difference between two arms generates the different power loss, and it is the modulated carry wave. MZM shows voltage mode characteristic. Generally, the phase shifter on waveguide is a capacitive loads under the transmission line.  $V_\pi$  usually describes the performance of phase shifting efficient by . To compromise the optical insertion loss, the length of MZM is limited. Therefore, a disadvantage of MZM is that it requires high voltage.[4] In fact, MZM generates excellent bandwidth performance since the speed of MZM is only limited by the transmission line. However, a driver provides both high bandwidth and high voltage swing is difficult.

The depletion type Silicon MZM is often devalued for its relatively worse power efficiency and large footprint, although the fact is that depletion-type Silicon MZM

is almost always preferred for practical use due to its higher modulation speed compared to the carrier injection type, its better tolerance to fabrication errors as well as environment stability compared to resonant modulators[37].

As shown in Fig.2.3(c), a classic differential cascode driver is used for the MZM. At the end of MZM, there is another pair of termination load resistances. Double termination is the most common method to complete a modulator driver for MZM.[5; 6]

In [4] and [5], the driver works over 20Gb/s, and output swing is 5V. Though the power consumption regards to modulator driver is not clearly stating in the publish, the modulator driver should account for a large part of the full transceiver power consumption which is 2.5W. MZM request much higher power than other methods.

[13; 119] provide MZM with lower voltage swing requirement as low as 1.5Vpp. In addition, to implement further efficient MZM and remove the bandwidth limitation of Tx lines, [8; 24] replaces the conventional Tx lines on MZM as slow-wave ones and complete over 40Gb/s operation with 1.6Vpp voltage swing. Another bandwidth boost method on MZM is demonstrated in [25]. Tx lines with phase shifters are segmented and inductors are added between the segments. The Tx line and inductor combined MZM boosts the bandwidth from 9GHz to 17GHz.

- PD

A photo detector (PD) is a standard optical receiving (demodulating) device. In silicon photonics, most of the state of the art PDs are not made from all silicon but germanium or other materials based on Si wafers.[23; 28; 85; 122] No matter which material, PDs work with a DC current with voltage bias. They can be treated as current source with parasitic capacitance on electric design.[6] As Fig.2.3(d) shows, it is a classic optical receiver with a typical differential common source CMOS TIA and common source CMOS LA.

Another issue with PD is, with different materials, the parasitic capacitance and efficient of PD is different. For instance, with Intel, a metal-semiconductor-metal (MSM) is used to generate  $200\mu\text{A}$  at responsively is  $0.9 \text{ A/W}$  with less than  $250\text{fF}$  capacitance.[44] Also, another p-i-n diode works responsively at  $0.9 \text{ A/W}$ , but capacitance is around  $150 \text{ fF}$  [4]. The parasitic capacitance and efficient of PD is directly affecting the TIA design and overall performance of receiving circuit.

According to the IMEC's report[Rakowski], a summarized comparison result is presented in Table2.1.

Though RRM provides the very compact layout area of the modulator device and very low power consumption, the thermally robust and narrow optical band increased the difficulty of application of RRM. The advantage and disadvantage of MZM are opposite of RRM. MZM gains the best thermally robust and almost broadband optical band, but

TABLE 2.1: Modulator comparison[Rakowski]

	Optical Band	Thermally robust	Compact	Power consumption
MZM	Broadband	High robust	Large device ( $\geq 1\text{mm}$ )	Large dynamic power
RRM	Narrow ( $< 1\text{nm}$ )	Sensitive ( $< 1\text{K}$ )	Very compact ( $\mu\text{m}$ level)	Low dynamic power (1Vpp)
EAM	Wide ( $< 30\text{nm}$ )	Sensitive ( $< 30\text{K}$ )	Compact (less $100\mu\text{m}$ )	Low dynamic power (2Vpp)

it consists of the largest device area and power consumption. EAM seems a compromise solution between RRM and the MZM.

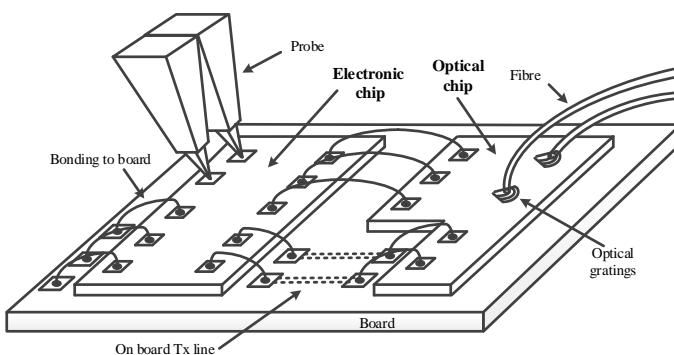
In this thesis, regard to the modulators are the Si MZM, a major target is focusing on optimize the modulator driver with CMOS process reliable with as lower the power consumption.

## 2.4 Integration

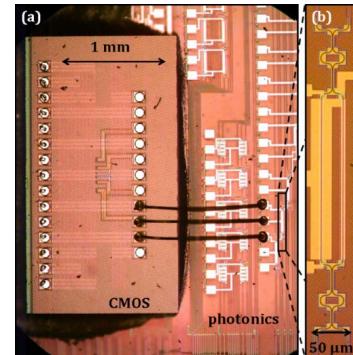
Fig. 2.1 shows dotted line boundaries in relation to the optical and electrical devices at system level. Integrate optical and electrical devices is a part of the optoelectronic design. The most direct approach is integrated the electric devices with optical devices on the same die which calls as monolithic photonics platform. For the reason of material, fabrication process, cost issue and performance limitations, most optoelectronic design are not implant on monolithic photonics platform. Below, the integration methods have been classified as three approaches.

- Bonding wire

This is a most classic approach to integrate optoelectronic devices. As Fig.2.4(a)



(a) Abstract view of Bonding wire/airbridge integration



(b) An example of wire bonding integration [9]

FIGURE 2.4: Wire bonding integration

shows, a wire bonding based method integration is used. Between the optical chip and electronic chip, all pads are connected via bonding wires. Depending on the specific situation, on board Tx line can also be used. On optical chip, the optical

gratings connected to fibers describes the optical IOs.

The advantages of the bonding wire are low cost and being easy to achieve. This approach is widely used for integrating different types of optical device. [96] connects the electronic devices to a RRM via bonding wires. The bonding wire exhibits excellent performance on optical device is modelling as a lumped capacitor. In an appropriate bandwidth range, the bonding wire could be seen as a inductor which enhances the bandwidth of electric output. On the optical devices which are modelling as Tx lines, the bonding wire integration restricts the performance due to impedance discontinuing on bonding wires. [95] and [117] both demonstrate that the bandwidth limitation of bonding wire is around 20GHz.

Fig.2.4(b) shows an example of bonding wire integration from [9; 96]. Because it's simple to implement, bond wires are almost the most common way to integrate the optical and electric devices.

- Flip chip bonding

One of the disadvantages of bonding wire method is the state of being higher

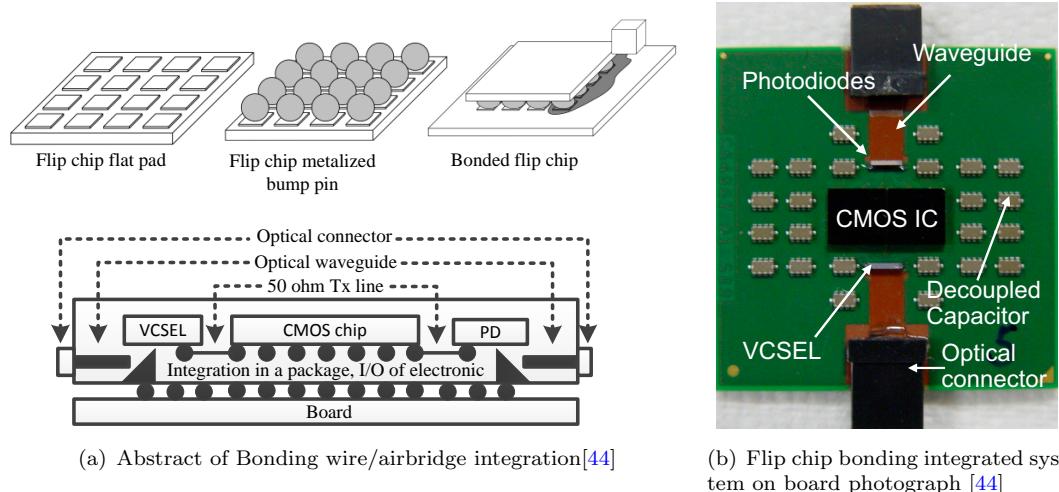


FIGURE 2.5: Flip chip bonding integration

than 20GHz.[95] This is mainly caused by the length of the bonding wire. In order to minimize the bonding length, flip-chip bonding is developed. As Fig.2.5(a) shows, this is the flip-chip bonding method. There are metalized bumps mounted on the flat pads of the flipped chips. Bumped chip pads directly face to the flat pin pads on board or another chip. With suitable bonding environment (pressure, heating and/or ultrasonic power), the bumps connects to the flat pads and chips are connected via the bumps [31; 73]. Lastly, some developers melt underfill and fill into gaps between chips then solidify it[135]. Flip chip integration generates high quality S parameter on wide-band and reaches high frequencies which are hard to achieve by wire bonding.[102; 117].

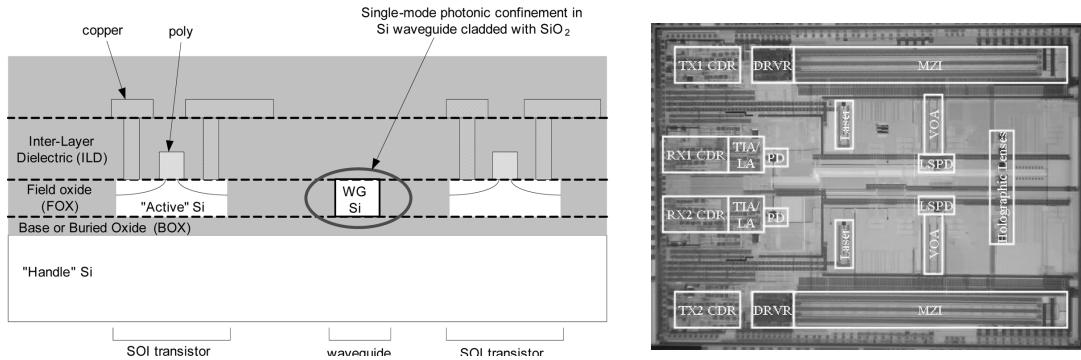
Fig.2.4(a) bottom shows the abstract view of a flip chip integrated optoelectronic transceiver from [44]. Optical devices and electronic devices are individually flip

chip bonded onto board and communicating via bumps and on board Tx lines. An overview photograph of the integrated device is shown in Fig.2.5(b).

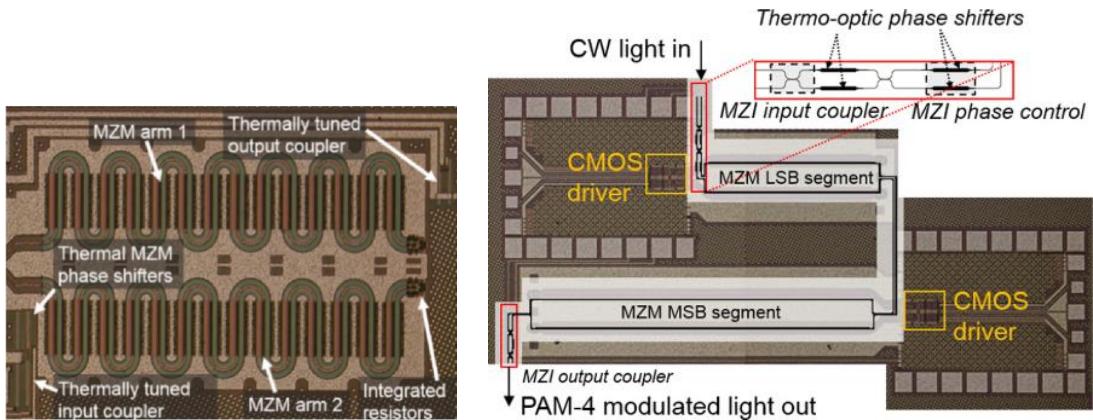
Furthermore, flip chip bonding is particularly suitable for placing the devices as an array. [91] demonstrates a flip-chip packaged transceiver which supports a CMOS chip flipped connected to 4 modulators and 4 photo-detectors. In this approach, optical and electric devices are placed in two individual flats (two chips) and sharing the area in a 3D space while it integrates.

- Monolithic photonics platform

A monolithic photonics platform uses a fabrication process which supports the build up of both optical and electric devices on the same wafer. With on chip metal tracks, the electronic circuit and optical device are interconnected in the same chip. Monolithic photonics platform avoid the off-chip integration between optical and electronic devices.



(a) Cross section of monolithic silicon photonics platform (not to scale)[4; 5] (b) A transceiver on monolithic photonics platform in [4]



(c) A transmitter on monolithic photonics platform in [34] (d) A PAM4 modulator with monolithic photonics platform in [131]

FIGURE 2.6: Monolithic photonics platform

[4] and [5] have a monolithic photonics platform design on  $0.13\mu\text{m}$  silicon on insulator (SOI) CMOS process. Fig.2.6(a) shows the cross section of this design platform. The optical waveguide together with the active layer of CMOS SOI de-

vice (including optical module and electric transistors) are of the same design and fabrication process. As can be seen from the illustration, optical and electronic devices coexist in the same layer of active silicon. For this design platform, an optical transceiver is presented in Fig.2.6(b). The optical transmitter includes the modulator driver and the on-chip MZM. The optical front-end receiver consists of an external high-speed PD and on-chip TIA+LA circuit. Before the modulator driver and after the TIA+LA, data recovery circuits are also placed in this design as an electronic interface. The carry wave of this design allows either a commercially available external laser, or a semiconductor laser mounted directly on the die. The advantages of this design includes reduced size, power consumption, and package integration complexity. Without integration between chips, the electronic device and optical device on the same die can be seen as that they are integrated into one joint circuit.

Another advantage of a monolithic photonics platform is unique optical and electric design. Though on the previous integration level, unique optical and electric design is not impossible, being without parasitic on integration and precise optoelectronic modeling makes the unique optoelectronic design easier. Fig.2.6(c) presents a monolithic photonics optical transmitter with a unique MZM in [34]. Unlike the conventional MZM with Tx line, this MZM consists of unloaded RF segments and loaded PN junctions as phase shifter segments. The unloaded RF segments are electrode regions that are not connected to PN junctions, and so have relatively high ( $\sim 75\Omega$ ) characteristic impedance whereas the PN junction loaded electrode sections have a  $\sim 30\Omega$  impedance.[34] The unloaded and loaded segments are combined as a transmission line with a target impedance between  $45\Omega$  to  $50\Omega$ . A CMOS modulator driver on the same chip consists of a three stage preamplifier followed by a nominal  $50\Omega$  driver, which is driving the MZM up to  $32\text{Gb/s}$ . This approach relies on accurate optoelectronic modelling, successfully raising the low-impedance phase shifter to  $50\Omega$ . In [131] and [130], a conventional MZM is segmented as longer and shorter phase shifters to be the most and least significant bits in an optical PAM4 transmitter. In this monolithic photonics design (Fig.2.6(d)), this MZM is designed as a  $30\Omega$  Tx line. Modulator drivers are open driver amplifiers with  $30\Omega$  termination resistance at the far end of MZM. [109] is another monolithic photonics platform example which achieves communication between an on-chip microprocessor and a memory circuit with on-chip RRM and SiGe PD. Though the optical connection consists of off-chip fiber with optical amplifier, to the best of the author's knowledge, this is the first fully integrated electronic processing system integrated with optical interconnections.

The monolithic photonics platform benefits from significant advantages in process performance, but manufacturing cost is a major concern. Both active and passive optical devices integrated with the electronic circuit can dramatically increase

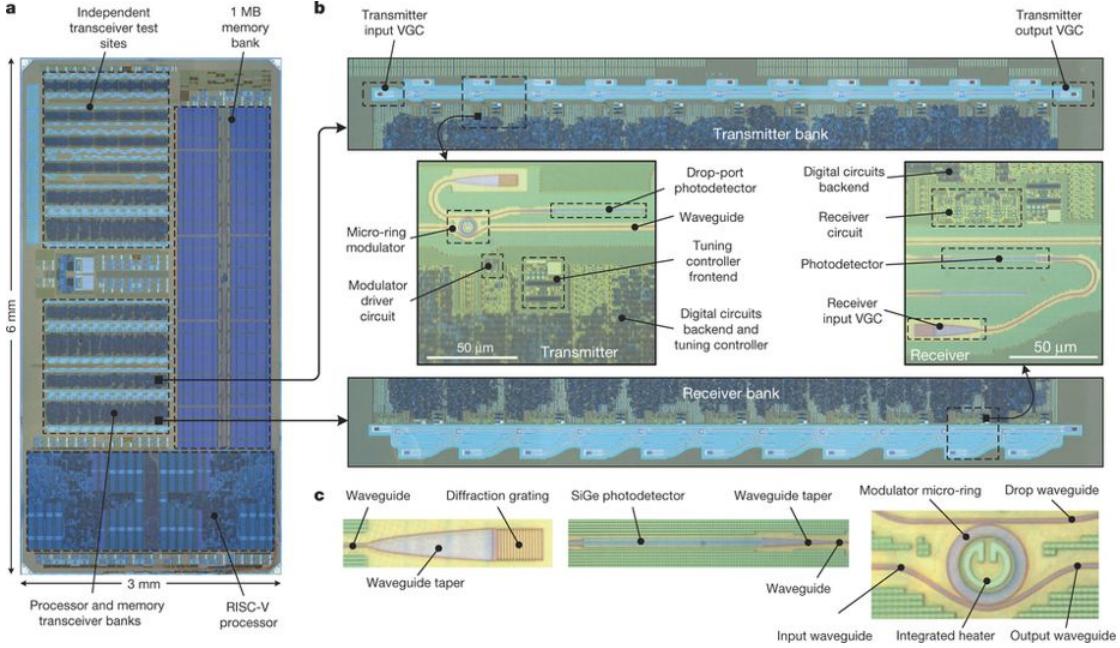


FIGURE 2.7: Single-chip microprocessor that communicates directly using light (a, Die photo of the  $3\text{mm} \times 6\text{mm}$  chip showing the locations and relative sizes of the processor, memory, and transceiver banks, imaged from the backside of the chip. b, The processor transmitter and receiver banks (the memory transmitter and receiver banks are identical) with close-ups of individual transmitters and receivers sites. c, Micrographs of the grating coupler, photodetector, and resonant micro-ring modulators.)[109]

manufacturing complexity in fabrication process. In addition, the dimensions of optics and CMOS electrical devices are not on the same scale, which leads to the optical device taking up a large layout area, in comparison to the on-chip CMOS circuit. Therefore, this approach requires compromise between performance and cost.

In these three integration approaches, the advantage of wire bonding is low cost, but there is a performance limitation due to additional inductance from the bonding wire. Though an appropriate inductance also could boost the device bandwidth, while the operating speed increases, the length of wire bonding is challenging to be shorted, then the drawback is unavoidable. Due to the modelling of the solid ball or pillar in flip chip bonding can be treat as a lower 100pH inductor with minor resistance, compared to wire bonding, the bandwidth limitation of flip-chip bonding can be neglected. But the complexity, as well as the cost of flip-chip bonding, is much higher than the wire bonding. Furthermore, the monolithic photonics platform provides the possibility to design optoelectronic devices in the same platform and could avoid the external integration drawback. But the cost of these platforms is much more expensive than the other integration methods due to the difficulty of fabrication.

## 2.5 High speed limiting amplifiers

The implementation of modulator drivers relies on the broadband amplifier design technologies. In order to complete an efficient modulator driver design with excellent bandwidth performance, the high speed limiting amplifier design for pre-driver is investigated in this section. Some of the bandwidth boost methods are also available to use in output stage design.

The signal produced by the end of the electronic transmitter or TIA usually suffers from a small amplitude. Thus, high gain on broadband is required, which is challenging to complete on one stage of an amplifier. The typical pre-driver and limiting amplifier, form multiple stages of the amplifier in a serial cascade.

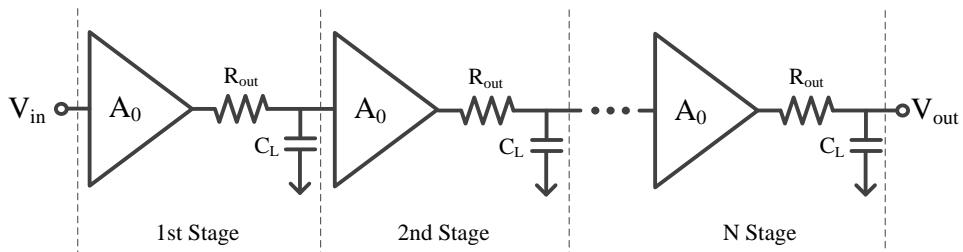


FIGURE 2.8: Cascade gain multiple stage amplifier

In the common limiting amplifier design, all stages are the same amplifier. Fig.2.8 presents  $N$  stages of amplifiers generate the same gain,  $A_0$  with the same output resistance ( $R_{out}$ ) and load capacitance ( $C_L$ ). With stages of amplifiers, the bandwidth reduces. Overall, the transfer function of  $N$  stages amplifier is given by[12],

$$H(s) = \left( \frac{A_0}{1 + \frac{s}{\omega_0}} \right)^N \quad (2.1)$$

where  $\omega_0 = (R_{out} \cdot C_L)^{-1}$ . Assuming  $s$  as  $\omega_{-3dB}$ ,

$$\left( \frac{A_0}{\sqrt{1 + (\frac{\omega_{-3dB}}{\omega_0})^N}} \right)^N = \left( \frac{A_0}{\sqrt[N]{2}} \right)^N \quad (2.2)$$

While  $N \geq 2$  similarly,

$$\omega_{-3dB} = \omega_0 \sqrt{\sqrt[N]{2} - 1} \approx \omega_0 \frac{0.9}{\sqrt{N}} \quad (2.3)$$

Thus, the bandwidth of the cascode gain amplifier reduces along with the numbers of stages. If we arrive at a gain-bandwidth product  $B = A_0 \cdot \omega_0$ , the transfer function of

N stages will be given by,

$$H_{(s)} = \left( \frac{\frac{B}{\omega_0}}{1 + \frac{s}{\omega_0}} \right)^N \quad (2.4)$$

For N stages,  $A_{tot} = A_0^N = (B/\omega_0)^N$ ,

$$\omega_{-3dB} = B \frac{\sqrt[N]{\sqrt{2} - 1}}{\sqrt[N]{A_{tot}}} \approx B \frac{0.9}{\sqrt{N} \sqrt[N]{A_{tot}}} \quad (2.5)$$

With forward calculating, achieving 40dB gain, the  $\omega_{-3dB}/B$  product is  $5 \leq N \leq 10$  (between 5 to 10, bandwidth increase less than 15%)[12]. Furthermore, more stages with less gain will increase noise on each stage and generate more power. Therefore, a 40dB cascode gain multiple stages amplifier is typically 5 stages. For higher gain than 100, increased numbers of stage could also follow this stage gain and bandwidth product experience.

Overall, bandwidth reduction is inevitable on a cascade gain multiple stage amplifier. A single stage of an amplifier is limited by gain and bandwidth production, to maintain the same gain but expand the high bandwidth area, is called broadband technique. Below, different broadband techniques are given, to increase the high-speed performance of the amplifier.

### 2.5.1 Inductive peaking amplifier

Adding inductors is the most common method to increase bandwidth on amplifiers. Increasing numbers of inductors can (to a certain extent) remove the pole due to load capacitor. A consort inductor could add zeros to loading impedance and create peaking on a higher band, to increase bandwidth. Unlike inductive peaking in a low noise amplifier or other narrow band amplifier system, a broadband amplifier is across several exponents on Hertz. Inductive peaking continues with a wide pass band of transistors. Thus, the bandwidth enhancement of inductive peaking in a broadband amplifier is limited.

In the example of a shunt inductor on the load, assuming the transistor is ideal, the bandwidth is controlled by R,C and L. Fig.2.9 presents a classic shunt inductive loading amplifier. The loading impedance of the RCL network is given by[114],

$$Z(s) = (sL + R) \parallel \frac{1}{sC_L} = \frac{R[s(L/R) + 1]}{s^2LC_L + sRC_L + 1} \quad (2.6)$$

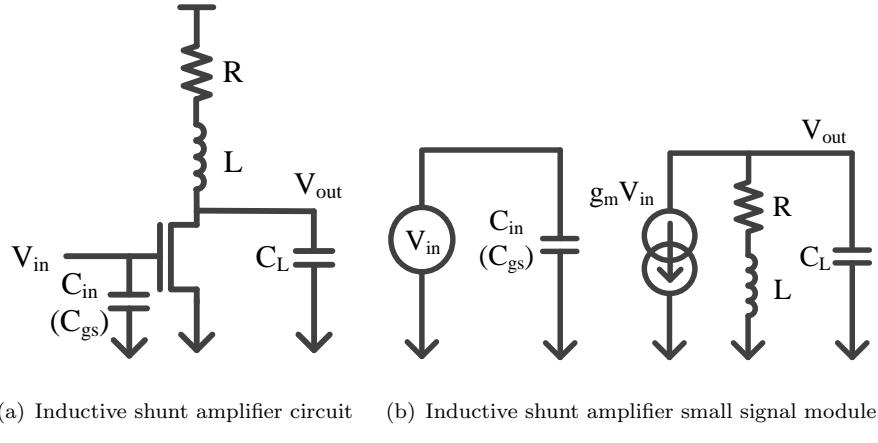


FIGURE 2.9: Broadband amplifier with a shunt inductive peaking[114]

Put this load into amplifier, gain is given,

$$Av = gm \cdot |Z(j\omega)| = gm \cdot R \sqrt{\frac{(\omega L/R)^2 + 1}{(1 - \omega^2 LC_L)^2 + (\omega RC_L)^2}} \quad (2.7)$$

In contrast with a simple RC load case, one more numerator (one more zero) is added to the transfer function to move the cut off frequency into a higher bandwidth. Furthermore,  $1 - \omega^2 LC$  term in the denominator contributes to an increased  $Z$ . Both these two points are the enhanced bandwidth of the amplifier.

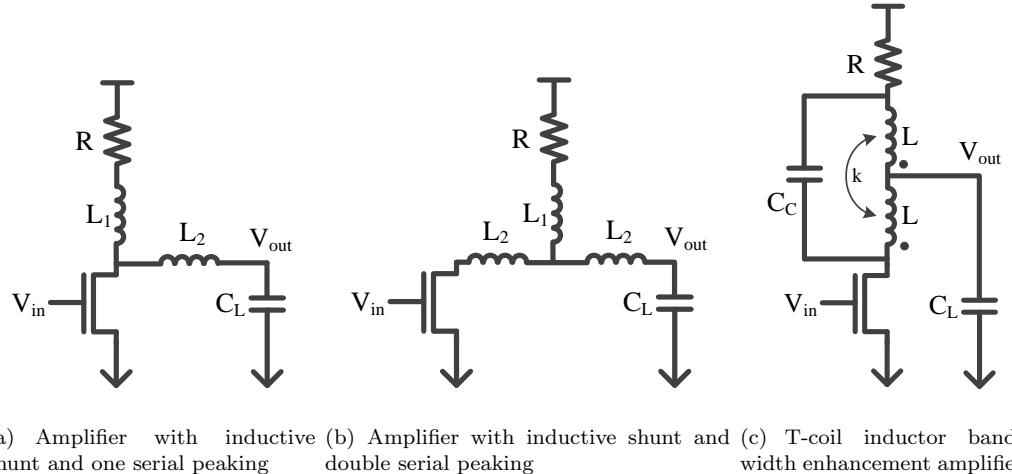


FIGURE 2.10: Three optimized topology with more inductive peaking[114]

Fig. 2.10 shows three optimized topologies with more inductive peaking (serial peaking and coil inductive peaking). The additional inductors could optimize the amplifier transfer function by creating more zero elements.

Overall, inductive peaking is the most common method to increase bandwidth. In theory, proper inductor peaking creates nearly no negative effect. A major problem is inductor has a high layout area cost component in the on-chip design. An inductor with

good quality (Q factor) always requires a large layout area. With the CMOS design, an unrestricted using inductor will cancel out the low-cost advantage of CMOS processes. But, with CMOS technology improvements, the  $f_T$  of the transistor is increased in advanced processes. Inductor value should be reduced for higher frequency peaking. The layout area cost of the inductive peaking circuit is declining with advanced CMOS processes.

[77] and [127] are respectively using shunt and serial inductors to enhance the bandwidth on the cascode amplifier and push-pull cascade limiting amplifier. In order to limit the area cost of inductors, a custom 3D inductor is commonly used in [118] and [79]. Furthermore, for a differential limiting amplifier with multiple stages, a shared inductor could cut half of the inductor cost. In continues the two cascade stages, first stage and second stage in differential arms (they are semi same phase) are sharing the shunt inductor. [42] saves 56% chip area by using shared inductors.

### 2.5.2 Cherry Hooper amplifier

The Cherry Hooper amplifier topology was created by [27] in 1963. After that, these kinds of amplifiers featured local feedback in the drain(of CMOS, or collector in BJT) network to improve speed, named after their creators.

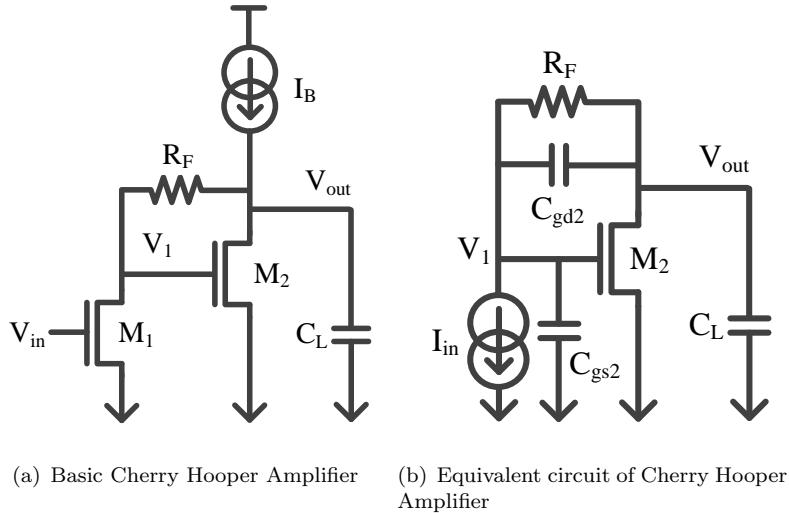


FIGURE 2.11: Cherry Hooper Amplifier topology analysis[12]

The Cherry Hopper amplifier is built on two stages of common source amplifier with a feedback resistance or another improved feedback network. As shown by the simplified circuit in Fig.2.11(a), assuming the CMOS is ideal, the current product is  $g_m \cdot v_{gate}$ , [12] analysis the low frequency small signal model, and given by,

$$V_1 = V_{out} - I_{M1ds} \cdot R_F = V_{out} - g_{m1} \cdot V_{in} \cdot R_F \quad (2.8)$$

The small signal current of  $M2$  must flow through  $R_F$ ,

$$g_{m2}(V_{out} - g_{m1} \cdot V_{in} \cdot R_F) = -g_{m1} \cdot V_{in} \quad (2.9)$$

The overall gain is given by,

$$A_v = \frac{V_{out}}{V_{in}} = g_{m1} \cdot R_F - \frac{g_{m1}}{g_{m2}} \quad (2.10)$$

If  $R_F \gg g_{m2}^{-1}$ , the gain is equal to a common source amplifier with load of  $R_F$ .

Considering high frequency bandwidth, poles on band are given by, on order of  $\omega_{pole,V_1} \approx g_{m2}/C_{gs2}$  and  $\omega_{pole,V_{out}} \approx g_{m2}/C_L$ . Compared with the general frequency pole on the common source amplifier ( $\omega_{pole} = (R_L \cdot C_L)^{-1}$ ), it is an improvement.

For a more accurate pole result, the circuit needs to be transferred to the equivalent circuit in Fig.2.11(b). Summing the output current[12],

$$-V_{out}C_Ls - g_{m2}V_1 = I_{in} + V_1C_{gs2}s \quad (2.11)$$

and hence,

$$V_1 = \frac{-V_{out}C_Ls - I_{in}}{g_{m2} + C_{gs2}s} \quad (2.12)$$

Therefore,

$$\frac{V_{out}}{I_{in}} = \frac{R_F^2 C_{gd2}s^2 + g_{m2}R_F C_{gd2} + C_{gs2} - C_{gd2})R_Fs + g_{m2}R_F - 1}{R_F(C_{gs2}C_L + C_{gd2}C_L + C_{gd2}C_{gs2})s^2 + (C_L + g_{m2}R_F C_{gd2}C_{gs2})s + g_{m2}} \quad (2.13)$$

For the best bandwidth product, suppose the two poles are the same,

$$\omega_{pole1} = \omega_{pole2} = \frac{2g_{m2}}{C_{gs2} + C_L + g_{m2}R_F C_{gd2}} \quad (2.14)$$

If the third term of denominator is negligible, the poles are given by the average value of  $C_{gd2}$  and  $C_L$  and  $g_{m2}$ . Overall, it is much higher than that of the general common source amplifiers.

A challenge for the CMOS Cherry Hooper Amplifier is the requirement for a relative DC power supply. When output voltage bias is closer to the power supply voltage, there will be no headroom for the signal. The gain-headroom trade off is a common discussion regarding this kind of amplifier. The most general method is to increase DC power supply which as shown with  $I_B$  in Fig.2.11(a).

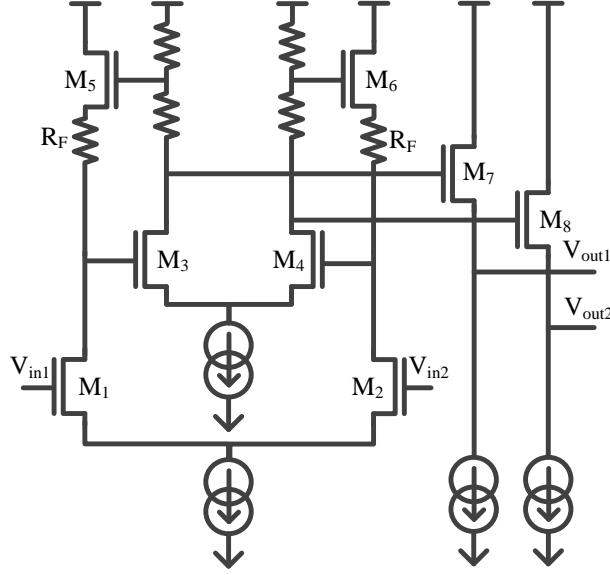


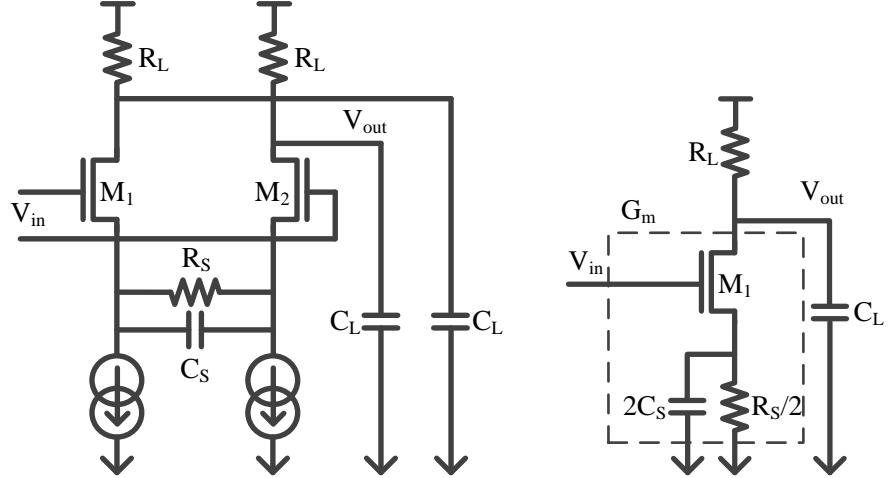
FIGURE 2.12: Modified CMOS Cherry Hooper differential amplifier with DC bias reset for limiting amplifier application[15]

In the implementation, an optimized method is to use Cherry Hooper Amplifier as shown in Fig.2.12. A classic Cherry Hooper amplifier input and output DC bias is different. In [14] and [15], a modified Cherry Hooper amplifier is presented. In this circuit,  $M_1, M_2, M_3$  and  $M_4$  are acting as a classic Cherry Hooper amplifier. The difference is feedback is built with a source follower ( $M_5$  and  $M_6$ ) and feedback resistance ( $R_F$ ). Ideally, the source follower generates 0dB gain from gate input in the same phase but with the feedback DC bias reset. This structure could reset the DC bias of drain of  $M_3$  and  $M_4$ , and save some headroom for the signal. However the source follower is not performing very well on a very high speed signal. More designers prefer to use this structure with a BJT process (emitter follower with resistor feedback).

The last problem of the Cherry Hooper amplifier is that input and output DC bias are different. Some designers have added a DC bias reset circuit. As in [1; 14; 15], they add source followers (or emitter follower) on  $M_7$  and  $M_8$  for bias reset. This means a Cherry Hooper have to use more power and complexity on circuit to support the cascade stage application.

### 2.5.3 Capacitive Degeneration amplifier

Capacitive degeneration is a broadband technique commonly used in a differential pair amplifier. It is low cost source degeneration in a differential pair. As Fig.2.13(a) shows, capacitive degeneration is adding a RC network between sources of two CMOS amplifiers. This network could increase effective CMOS transconductance in the high frequency region.[12]



(a) Differential pair amplifier with capacitance degeneration (b) Equivalent half circuit of the amplifier with capacitance degeneration

FIGURE 2.13: Capacitance degeneration analysis[12]

Firstly, the circuit could be equalized to a small signal circuit, as shown in Fig.2.13(b), on each side of a differential pair. Since the other part is differential,  $R_C$  and  $C_C$  could be transferred to  $R_C/2$  and  $2C_C$  to AC ground.

Considering the frequency effects, amplifier transconductance  $G_m$  is given by[12],

$$G_m = \frac{g_m}{1 + g_m(\frac{R_S}{2} \parallel \frac{1}{2C_S s})} \quad (2.15)$$

$$= \frac{g_m(R_S C_S s + 1)}{R_S C_S s + 1 + \frac{g_m R_S}{2}} \quad (2.16)$$

Hence transconductance contains an additional zero at  $1/(R_S C_S)$  and pole at  $(1 + g_m R_S/2)/(R_S C_S)$ . This means new transconductance is constant before zero, and increasing between zero and pole, then turning back to a constant after pole. We can use the zero to cancel the original common source amplifier pole which is  $(R_L C_L)^{-1}$ . Assuming  $R_S C_S = R_L C_L$ , the voltage gain pole will be removed from  $(R_L C_L)^{-1}$  to  $(1 + g_m R_S/2)/(R_S C_S)$ . Thus, the bandwidth of the amplifier is increasing.

[126] and [138] use capacitive degeneration, or an optimized structure. This raises the on chip parasitic problem of capacitive degeneration. The capacitive degeneration boosting bandwidth is less than the mathematical result, especially in the process with improved less minimal length of CMOS. This is because, with these processes, the transistors generate less  $C_L$ . Meanwhile,  $R_L$  is gently lower; hence,  $R_S$  and  $C_S$  in capacitive degeneration are located at a low value. In on chip design, to achieve resistance and capacitor at low value always comes with the parasitics which means the low Q factor. The performance of capacitive degeneration which consists of low Q factor devices is significantly damaged.

Overall, capacitive degeneration could enhance the bandwidth by increasing new pole if an  $RC$  network is appropriate. But in high speed design with optimized CMOS processes, the performance can be damaged by parasitics. The specific design requirements decide if this method is appropriate to the current design.

#### 2.5.4 Active feedback amplifier

Active feedback in limiting amplifier or pre-driver is a very low cost method. As the name of this method, it means feedback is un-passive transform, but active function. In CMOS design, it is generally negative feedback with transistors.

This method support very good bandwidth enhancement. With butterworth response feedback from orders later, gain cascade amplifier bandwidth is different from Eq.2.3. With butterworth response feedback order value  $m$ , the new bandwidth is given by,

$$\omega_{-3dB} = \omega_0 \sqrt[2m]{\sqrt[2m]{2} - 1} \quad (2.17)$$

Clearly, with butterworth feedback,  $\omega_{-3dB}$  will be enhanced. With theorematic, the  $m$  larger,  $\omega_{-3dB}$  is closer to  $\omega_0$ .

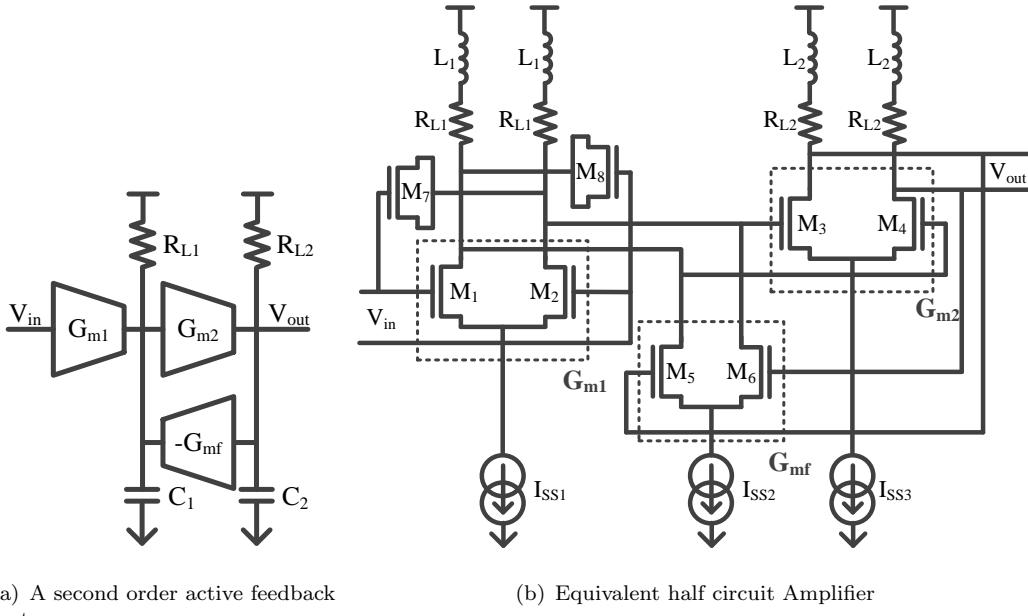


FIGURE 2.14: Active feedback amplifier topology analysis[12; 32]

Fig.2.14(a) is a second order active feedback topology and Fig.2.14(b) presents the implement circuit in differential amplifiers. In the circuit, each part is in correspondence.  $M7$  and  $M8$  is a Miller capacitor castellation,  $C_{M7,8} \cong C_{Mgd1}(g_{m1}R_{L1}+1)/(g_{m1}R_{L1}+1)$ .  $G_{mf}$  are built with NMOS gate connected from the differential side of the second order output. It is equal to the  $-G_{mf}$  in topology.

Assuming the two stage amplifier is of the same condition. Set  $g_m$  is transconductance of  $M1, M2, M3$  and  $M4$ ,  $g_f$  is transconductance of  $M5$  and  $M6$ [12],

$$G_{m1} = G_{m2} = \frac{g_m \cdot R}{1 + RCs} \quad (2.18)$$

$$G_{mf} = \frac{g_f \cdot R}{1 + RCs} \quad (2.19)$$

This second order system transfer function could be characterized as,

$$H_{(s)} = \frac{G_{m1} \cdot G_{m2}}{1 + G_{m2} \cdot G_{mf}} \quad (2.20)$$

$$= \frac{g_m^2 R^2}{(1 + RCs)^2 + g_m g_f R^2} \quad (2.21)$$

$$= \frac{A_0^2}{(1 + \frac{s}{\omega_0})^2 + A_0 \beta} \quad (2.22)$$

where  $\omega_0 = 1/RC$ ,  $A_0 = g_m \cdot R$  and  $\beta = g_f R$ .

In low frequency,

$$A_{tot} = \frac{A_0^2}{1 + A_0 \beta} \quad (2.23)$$

Compared with Eq.2.1 at  $N = 2$ , the new denominator ( $A_0 \beta$ ) created another zero in transfer function. Thus, the bandwidth will be enhanced. But,  $A_{tot}$  is damaged while feedback acts as a denominator.

Indeed, active feedback is a most classic gain-bandwidth trade off on size of  $\beta$ . While increase the feedback, it sacrifices the overall gain and creates extra high frequency peaking close to  $\omega_0$ . Therefore, active feedback have to locate the  $\beta$  at an appropriate scale of  $G_m$ . With some implementations, the  $\beta$  is 1/15 or less to achieve reasonable gain loss with appropriate peaking on  $\omega_0$  band.[12]

Base on the Eq.2.3 and Eq.2.17, as an example, to achieve a cascade gain multiple stage amplifier which total bandwidth ( $\omega_{-3dB}$ ) is 10GHz. Assume this amplifier was achieved with 6 stages ( $N = 6$ ),  $\omega_0 = 28.5\text{GHz}$ ,  $17\text{GHz}$ ,  $14\text{GHz}$  and  $13\text{GHz}$  for  $m = 1, 2, 3$  and  $4$ . With 6 stages, response order generates different  $\omega_0$  needs. From no feedback to 2nd order feedback and 3rd order feedback, the  $\omega_0$  reducing is very obvious (on 4th order, it nearly no more less). So, most designs are selected between 2nd order or 3rd order active feedback.

To achieve maximum bandwidth performance, in a long chain of amplifiers, active feedback support adds more interleaving feedbacks. This could increase boost the bandwidth performance. In [41], an amplifier with third order interleaving active feedback achieves a 10Gb/s inductor-less driver on  $0.18\mu\text{m}$  CMOS technology. The circuit topology is shown in Fig.2.15. In this example, a 12 stage main stage with 7 active feedbacks is

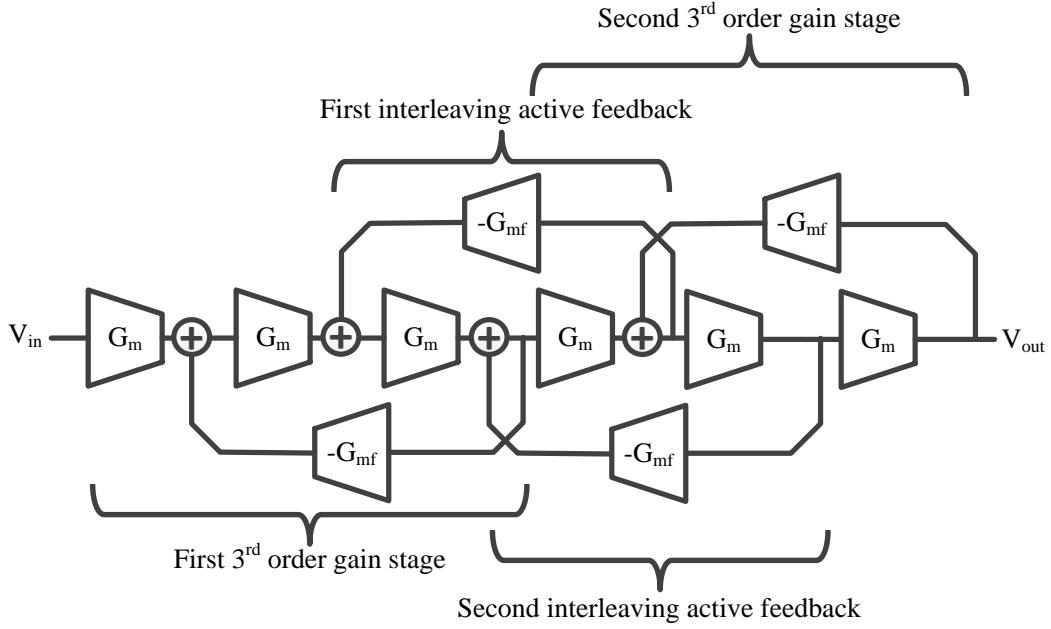


FIGURE 2.15: Third order interleaving active feedback cascade gain amplifier topology  
[\[41\]](#)

used and it provides around 30dB overall gain.

Overall, though the gain of the amplifier is reduced, active feedback is indeed enhancing bandwidth. Nonetheless, to achieve the required gain with an active feedback, the number of amplifier stage must increase due to gain loss. Increasing stage leads to more power consumption. Therefore active feedback implementation has to find an appropriate compromise between power and performance.

## 2.6 Output Stage of Modulator Driver

According to Sec.2.2, the main driver of modulator driver is the output stage. This section investigates the most common circuit topologies for modulator driver output stages.

No matter on current or voltage mode devices, transmission lines is commonly used for either connecting to the device or acting as the electro-optical device itself. Fig.2.16 presents a current mode laser driver works with a VCSEL and a voltage mode modulator driver drives up a MZM with terminations.

In most transmission line based design, the impedance is nominal of  $50\Omega$ . In the laser driver (current mode) example, the VCSEL acts as a  $50\Omega$  impedance load, and be driven by the driver via the Tx line. The modulator driver for MZM is a voltage mode amplifier with output impedance  $Z_O = 50\Omega$ . The output signal travels through the Tx lines based MZM and terminated with far end termination impedances.

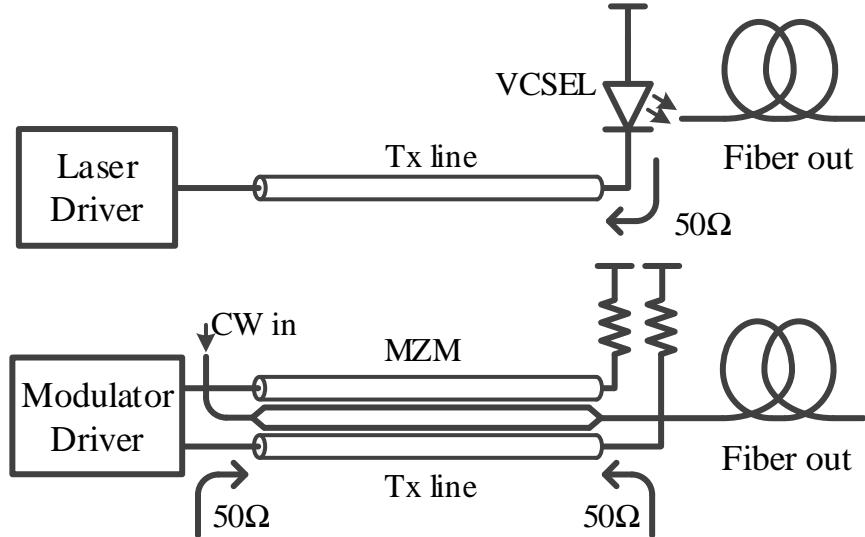


FIGURE 2.16: Laser driver output impedance matching with a optical modulator

The  $50\Omega$  is the most commonly used value, which also is provided by most of the commercial testing devices. Increase the impedance on the Tx line is a benefit to saving power of the output stage amplifier while bandwidth performance on the Tx line is neglect, therefore narrow width of the electrode on MZM (the Tx line) could increase the inductance, where raising the impedance of Tx line. Another reality is the velocity of the electric signal on the Tx line which has to be matched to the group velocity of the optical signal of the waveguide phase shifter. To compensate the capacitive load on the phase shifter and match the group index on the optical signal, the selected value of the impedance of Si MZM is generally  $50\Omega$  or lower.

Within the designs, some of the previous design examples tried to change and adjust the  $50\Omega$  impedance. This is more common in design with monolithic photonics platform. In general, increase the nominal impedance and termination, will enhance the output power but compensate with bandwidth performance. [131] uses open drain structure for MZM with the transmission impedance is located at  $30\Omega$  but  $50\Omega$ . The lower load and nominal impedance enhances the bandwidth performance of the MZM but the power consumption is obviously higher. In addition,  $50\Omega$  impedance (or other appropriate value) also could be provide by flexible combining the element on different nominal impedances. The other MZM in [25] provides an overall  $50\Omega$  transmission line which is consists of nominal  $75\Omega$  and  $30\Omega$  segments.

In the reason of most MZM are Tx line based device, the following investigated output stage circuit can be adapted to use in transmission line applications.

In the later subsections, five standard output stage structure has been demonstrated. In Chapter4 , Table4.5 lists several state of the art examples of the modulator driver regarding to push pull, current mode logic and distribute amplifier designs. With a simple summarize, push pull is easier to used for the designs requires compact integration

but the output impedance is more difficult to accurate rather than the current mode logic structure.  $f_T$  doubler significantly reduces the input load pressure but it turns onto the output load, so this is a very effective approach though it does not meet the extreme bandwidth requirements. Open drain approach is similar to the standard current mode logic structure but with out inner loads. It saves half of the power with more risk on the test and variations. Distribute amplifier is a advanced selection when there is a high bandwidth requirement. But area cost and power consumption of distribute amplifier is higher than the other approaches.

### 2.6.1 Push pull on output stage

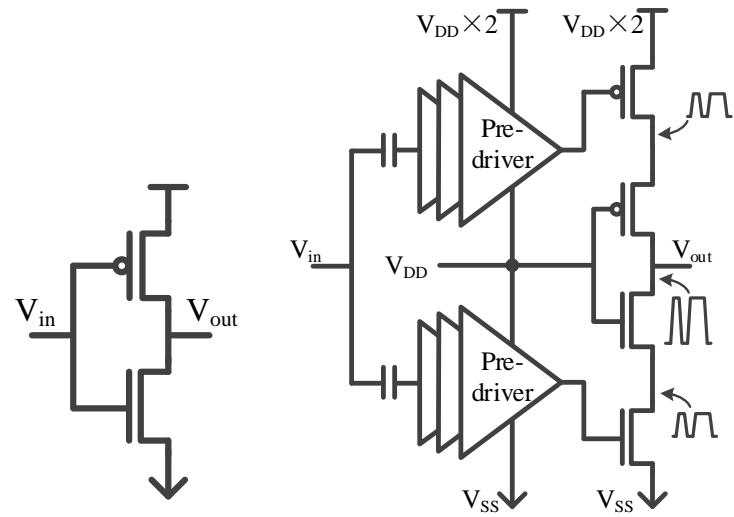
Push pull structure is the most common CMOS amplifier solution. Fig.2.17(a) presents a typical digital inverter, which is a push pull structure. This amplifier could directly drive up the modulators if the output impedance is modified as an appropriate value. For the reason of both PMOS and NMOS are amplifying device, the linearity of push pull amplifier is more difficult than current mode logic amplifiers but higher gain. In order to optimize the output voltage swing for silicon photonics MZM, a common improvement is cascode the push pull amplifier. Fig.2.17(b) presents a cascode push pull modulator driver with pre-drivers. The power supply of modulator driver is  $2 \times Vdd$  and the output swing is almost doubled of the one in Fig.2.17(a).

Compare with the current mode logic amplifier as the output stage, push pull as a output stage usually generates better output swings with lower power consumption. Hence this structure is widely used for efficient modulator driver designs. A major problem of push pull structure is the speed limitation. Due to  $f_T$  of PMOS being much less than NMOS, the overall speed of push pull amplifier is limited by PMOS[65].

[9] shows a classic 2 times fan out push pull digital inverter based driver which based on a 90nm CMOS process. The output stage is a  $1328\mu\text{m}$  PMOS and a  $512\mu\text{m}$  NMOS. Output swing is programable on a different  $Vdd$  supply from 0.8V to 5V. This modulator driver is integrated with a forward biasing p-i-n diode via bonding wire and the averaged power in 4ns is 2mW at 2Gb/s. In addition, [65] is an improved push pull structure which supports a double  $Vdd$  output swing. With doubled  $Vdd$ , the output swing of this driver is 4Vpp differential (2Vpp on single side) at 10Gb/s. Another outstanding push pull modulator driver with two layers of cascode is demonstrated in a 28nm FD-SOI CMOS process[106]. This modulator integrates to a MZM and operates 44Gb/s data transmitting in [132].

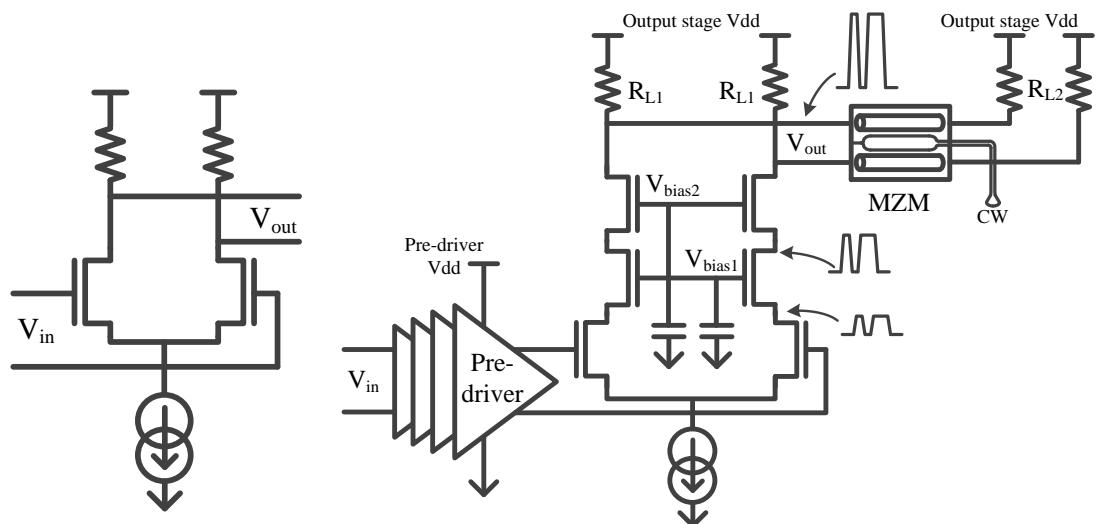
### 2.6.2 Current mode logic on output stage

For reason of limitation of bandwidth of PMOS, the CMOS based output stage design achieves better bandwidth performance with current mode logic (CML) design.



(a) A standard push pull digital inverter  
 (b) An improved high output voltage swing (double  $V_{dd}$ ) push pull based laser driver

FIGURE 2.17: Push pull output stage



(a) A standard current mode logic analogue inverter  
 (b) An improved high output voltage swing cascode current mode based laser driver

FIGURE 2.18: Current mode logic output stage

Fig.2.18(a) a classic current mode logic differential inverter. Unlike a push pull amplifier, only NMOS amplifies the input signal. The linearity of CML amplifier is only related to the  $g_m$  of NMOS and the loads, hence it is easier to achieve than a push pull. Simultaneously, due to there is no PMOS in amplifier, the bandwidth of CML is enhanced from a push pull.

To achieve higher output voltage swing, the cascode amplifier is commonly used in a CML driver. In Fig.2.18(b), there is a two stage cascode output stage for MZM. The output stage amplifies the signal from the pre-driver, then drives the MZM with double termination in the example circuit. With the cascode stages, the  $G_M$  and output voltage swing of amplifier increases.  $V_{bias1}$  and  $V_{bias2}$  are generated from the bias circuit.[61] Assuming this is a nominal  $50\Omega$  MZM,  $R_{L1}$  and  $R_{L2}$  are doublers terminated as the same  $50\Omega$  (overall DC load on  $V_{out}$  is indeed  $25\Omega$ ).  $R_{L1}$  is the near end termination which usually consists of on chip resistance, and  $R_{L2}$  is a pair of far end termination after the MZM.

In [5] and [4], a modulator driver with current mode output stage is demonstrated in  $0.13\mu m$  CMOS SOI technology. With a 5V power supply, the driver is functional up to 20Gb/s with 5V differential output swing. MZM is double terminated by  $50\Omega$ . In [48; 49], a CML modulator driver has achieved 2V output swing, 33GHz bandwidth with 45nm SOI CMOS technology.

### 2.6.3 $f_T$ doubler on output stage

On the output stage of the modulator driver, the width of transistor could be  $100\mu m$  or even higher. Input capacitance becomes a serious problem in terms of damaging the bandwidth and increasing the difficultly of pre-driver design.  $f_T$  doubler is a method of reducing input capacitance in a differential amplifier while maintaining the same gain.

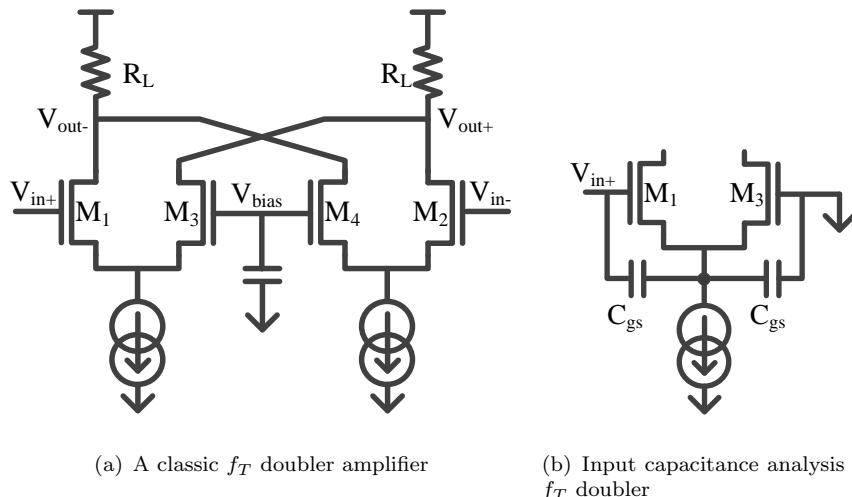


FIGURE 2.19:  $f_T$  doubler output stage

On a differential pair amplifier, also with the current mode logic inverter in Fig.2.18(a), the gain of this amplifier is given by,

$$A_v = \frac{V_{out}}{V_{in}} = g_m \cdot R_{load} \quad (2.24)$$

where the  $g_m$  denotes the transconductance of transistor and input capacitance is  $C_{gs}$  of input MOS.

In Fig.2.19(a), there is a  $f_T$  doubler amplifier.  $M_1$ ,  $M_2$  and  $R_{load}$  are the same as the classic CML amplifier. But additional  $M_3$  and  $M_4$  which are the same size as  $M_1$  and  $M_2$  reduces input capacitance on this amplifier. In this circuit,  $V_{bias}$  is given as the same common mode level of  $V_{in}$  on  $M_1$  and  $M_2$ . Fig.2.19(b) presents the input capacitance equivalent circuit of  $M_1$  and  $M_3$ . In fact, if parasitic capacitance is negligible, input capacitance will be exactly  $C_{gs}/2$ . Since this circuit halves input capacitance while overall transconductance is the same as it is before, it is named as  $f_T$  doubler.

The  $f_T$  doubler suffers from several backwards. First, With  $f_T$  doubler, the power consumption of the amplifier is doubled. Second, the doubled current through the load resistance is possible driving transistors back into the triode due to bias voltage of output reduction. In addition, though input capacitance is halves, the output capacitance by transistors of this stage is doubled. Furthermore, considering parasitic capacitance on source bulk junction and tail current source is in-negligible, input capacitance is higher than  $C_{gs}/2$ . Lastly,  $f_T$  doubler doubled the transistor size and complicated the circuit which means more parasitics and layout area cost.[12]

Despite all these backwards,  $f_T$  doubler is still a very useful topology on output stage of a broadband driver. [41] and [33] both both select  $f_T$  doubler as the output stage buffer. The design reduces the input loading capacitance to almost half and maintains the output power as the same as without  $f_T$  doubler.

#### 2.6.4 Open drain on output stage

No matter for the current or voltage mode optical modulators, in previous sections, the CML output drivers are all double terminated. Many designs prefer double termination due to convenient to measurement and better tolerance. Assume an optical modulator is a double terminated nominal  $50\Omega$  device, the DC load impedance is indeed of two  $R_L$  which is  $25\Omega$ . The power consumption of double termination is also doubled due to load impedance being half.

In this condition, some designs with a fixed loading condition will replace the output stage as an open drain design.[82] In Fig.2.20(a), the last stage is unloaded as an open connection on drains of transistors. As the same condition of loading optical device is a nominal  $50\Omega$  impedance matching device, this device could directly connect on to

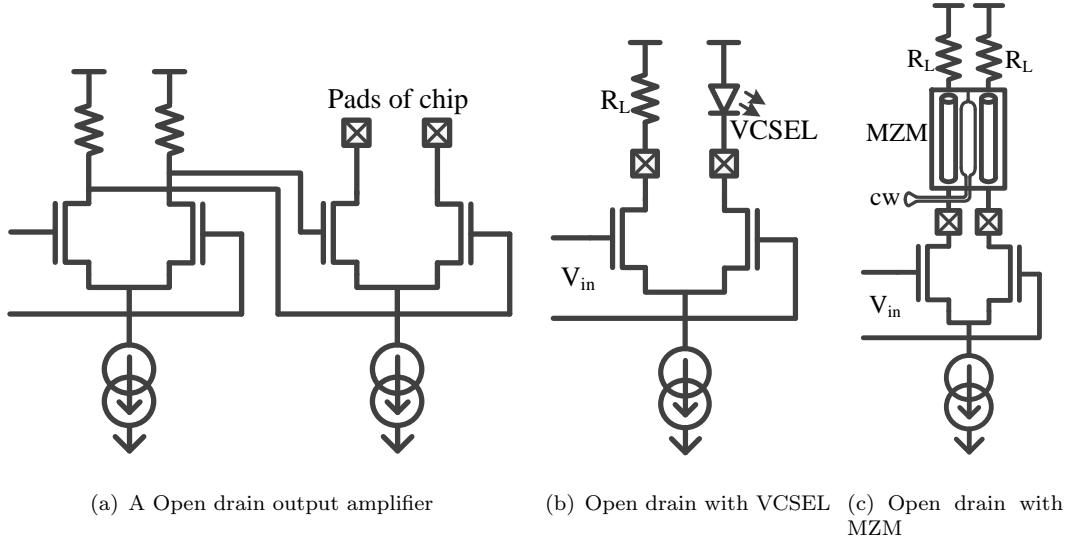


FIGURE 2.20: Open drain topology analysis

drain of NMOS with DC load (if necessary) from Vdd. In Fig.2.20(b) and 2.20(c), there are examples of open drain circuits working with a VSCEL and a MZM. With open drain design, the DC load of output stage is increased back to one time of transmission impedance. It leads to half of the power consumption in comparison to doubled termination.

In the open drain, any minor modelling error will change the load of the amplifier which affects performance. Therefore, the open drain is more stable in the monolithic photonics platform. [131] demonstrated two open drain output stage modulator drivers which transmits optical PAM4 with 2 segments of MZM. In this design, the load impedance is located at  $30\Omega$  but  $50\Omega$ .

### 2.6.5 Distribute amplifier

Due to most of the MZM is designed within traveling wave electrodes which is a Tx line, the distribute amplifier (DA) is an excellent choice for MZM.

Fig.2.21(a) is a conventional common source amplifier. The input and output poles are given by,

$$|\omega_{in}| \approx \frac{1}{R_S[C_{GS} + (1 + g_m R_D)C_{GD}]} \quad (2.25)$$

$$|\omega_{out}| \approx \frac{1}{R_D C_L} \quad (2.26)$$

Where the  $C_L$  includes the drain junction and gate drain overlap capacitance of transistor. Obviously, the bandwidth performance of the amplifier is limited by the transistor and load capacitance. In the output stage, with the width of the transistor increasing,

the cut off frequency is limited by the amplifier itself.

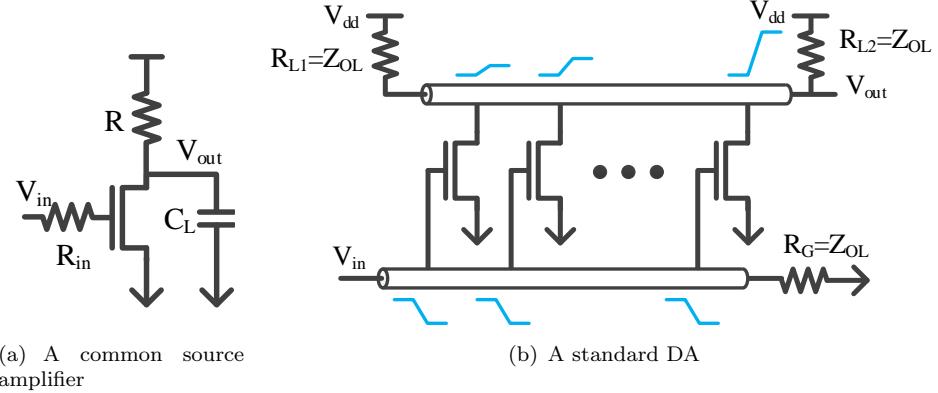


FIGURE 2.21: DA analysis

A DA splits the transistor to become multiple transistors and connects them with multiple segmented Tx lines as Fig.2.21(b) shows. The input signal travels through the Tx line and drive up all gates of transistors. The output (drain) of all segments connect to the output Tx line. The distance between transistors is properly designed so that the output power from each transistor is summed in phase. In a DA, the input and output Tx lines are specially designed which is higher than the  $Z_{OL}$ . When it is loaded periodically with multiple segments of transistors, the characteristic impedance is lowered to  $Z_{OL}$  and presents the matching on time constants.

The key observation here is that, in a DA, the transistor capacitances do not translate to a time constant. Rather, they simply lower the characteristic impedance of input and output Tx line. In other words, with lossless lines, the DA can in principle provide infinite gain with infinite bandwidth.[12]

Infinite gain with infinite bandwidth is extremely attractive but only exists on a theory level. In reality, the major problem is the attenuation on Tx line. The integrity of input signal on input Tx line is the same on all gates of transistors in Fig.2.21(b). But the amplitude of signal is decreasing gradually in reality. To maintain the signal quality on Tx line, the segment number has to be limited. Most designs select 3 or 4 stages. [12] compares a DA example with 5 and 6 stages and a relatively low overall gain increasing is observed.

Furthermore, the area cost of DA is another backwards. On chip Tx lines for input and outputs costs a relatively large layout area.

In any case, the bandwidth and gain performance of the DA is far superior to other amplifier structures. Therefore, DA has a decisive position in experimental tests and demonstrates extreme performance, but the efficiency of DA is an obvious limitation.

In order to cancel the Miller effect on transistors and optimize the gain and output voltage swing, DA based on CMOS process usually uses a cascode structure as Fig.2.22(a)

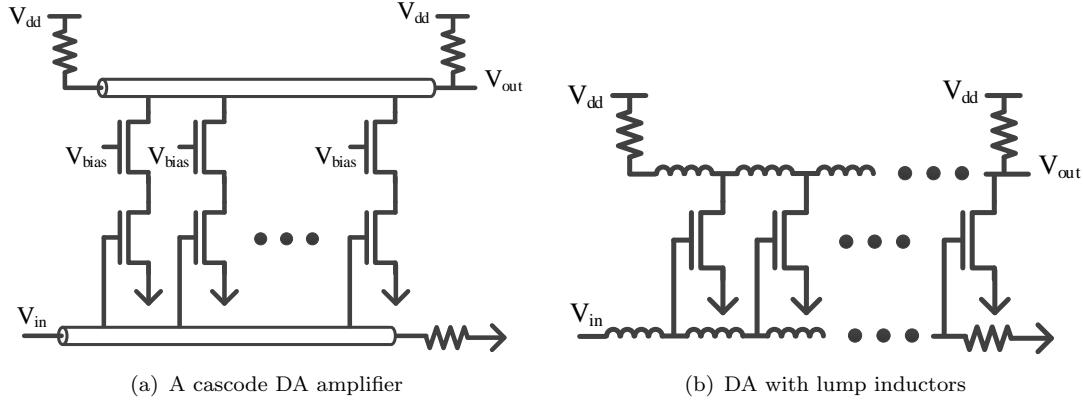


FIGURE 2.22: Two optimization on conventional DA

shows. [52] demonstrates a cascode three segments DA design is functional up to 92GHz. In additional, the conventional Tx lines can be replaced with other module which follows the transmission theory. The most common way is to replace the Tx line with lumped inductors as shown in Fig.2.22(b). [18] and [17] both demonstrate the use of lumped inductors to complete a broadband DA which is saving the area cost. Due to there being numbers of segments in the amplifier, some designs [134] even can make minor adjustments to each segment to compose special pre-emphasis on the amplifying signal.

TABLE 2.2: Output stage amplifier comparison

	Push-pull	CML	$f_t$ doubler	Open drain	DA
Out Vpp	High	Low	Low	Low	High
Power cons.	Low	High	High	Low	Very high
Bandwidth	Low	High	Ok	High	Very high
Out imp.	Difficult	Easy	Easy	Difficult	Easy
Input load	Very high	High	Low	Low	Very low
Area cons.	Low	Low	Low	Very low	Very high

In the last, the previous reviewed output stage amplifier structures are listed and compared in the Table2.2. Push-pull and CML are the most commonly used structures.  $f_t$  doubler lower the input load capacitance with a compromise of the overall bandwidth. The difficulty of the open drain is the control of output impedance, as well as the MZM, has to be designed as a part of the amplifier circuit. In the order of the DA transfers the input load of the amplifier as on the transmission line, the input capacitance could be neglected in theory. Realistically it could be treated as the loss of the input transmission line, however it still much lower than the other structures. Regard to the power consumption and area consumption performance, the DA are both lacks of these two performances.

## 2.7 Optical transmitter with complex modulations

Silicon photonics also support complex modulation transmission. The efficiency of optical communication transmission is incarnated in the high transmission capability. In Fig.2.23, the general development methods of increasing transmission capability in optical communication are presented.

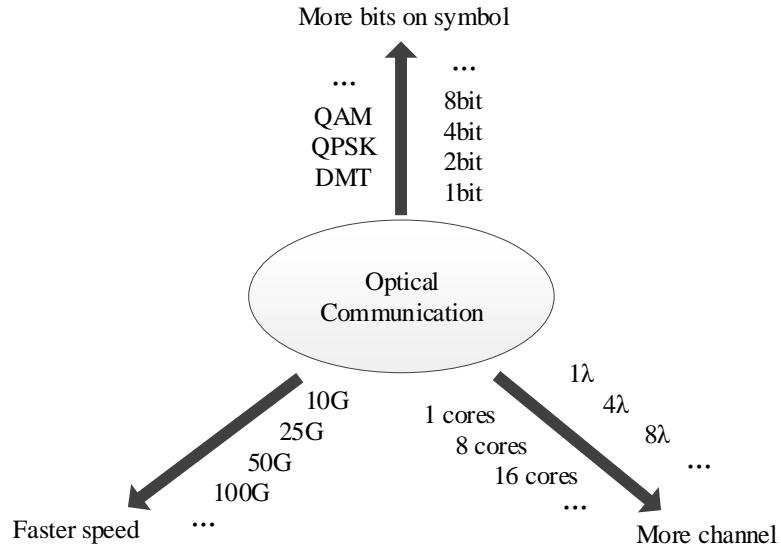


FIGURE 2.23: Transmission capability development of optical communication

With three dimensions of developments, faster channels, more channels and more bits per symbol, all can increase the data capability on fiber. The faster channel is the most conventional optimization. Increasing numbers of core in fiber relates to multi-core fiber technology. Aside of these two, the other methods in Fig.2.23 are all related to complex modulated optical communication.

This section introduces several general modulation methods. In the implementations of these modulations, electronic and photonics integration and electronic-optical cooperative design are significant.

### 2.7.1 Wavelength-division multiplexing

As Fig.2.24 shows, wavelength-division multiplexing (WDM) is realized by optical carry waves carrying signals independently at different wavelengths. In this example, optical carry waves are on different 4 wavelength ( $\lambda$ ). Modulated optical signals are multiplexed and transmitted on fiber. De-multiplexer on receiver transforms signal back onto 4 optical channel and demodulated by independent PDs.[56; 68; 69]

In silicon photonics, the WDM is generally realized by MZM or RRM. The implementation of WDM on MZM is relatively simpler to realize because MZM is a wide band

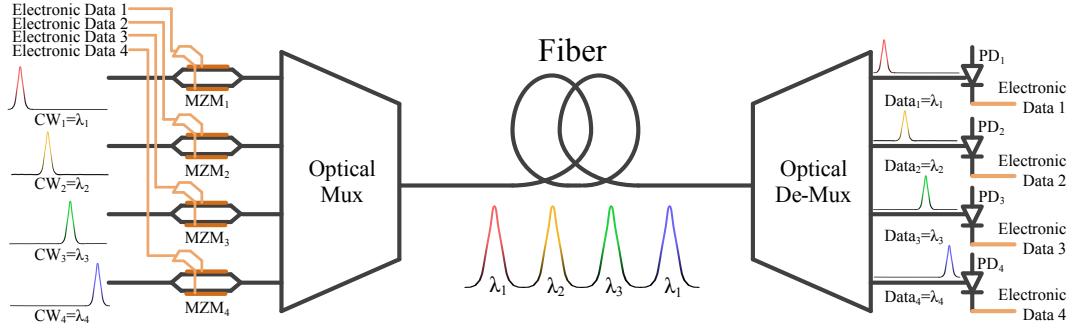


FIGURE 2.24: Optical connection with multiple channel

optical modulator. The carrier of each channel should be generated individually or be de-multiplexed from laser source.[56; 68] RRM is a narrow band optical device, hence the optical multiplexer is not necessary.[76] But the temperature sensitivity and process variation problem of RRM can generate mismatch between RRM and targeting wavelength. To increase the tolerance, [136] demonstrates a active wavelength control for RRM and turns the RRM to the targeting carrier wavelengths.

Regardless of the types of the modulator, WDM integrates multiple modulators in a small chip area. To realize a WDM with electric circuits, the modulator drivers and transmitter circuit before the drivers have to compact integrate to modulators. Furthermore, realizing multiple numbers of drivers in one electronic chip is also necessary.

### 2.7.2 Optical pulse amplitude modulation

It is challenging to increase the transmission data rate due to the limited electro-optic bandwidth on optoelectronic device. An alternative solution is multilevel signaling. Fig.2.25 presents a NRZ and a pulse amplitude modulation (PAM) 4 signal. In PAM4, 2 digital bits per symbol are encoded into four signal levels. Therefore data rate of PAM4 is doubled of conventional NRZ in the same symbol rate.

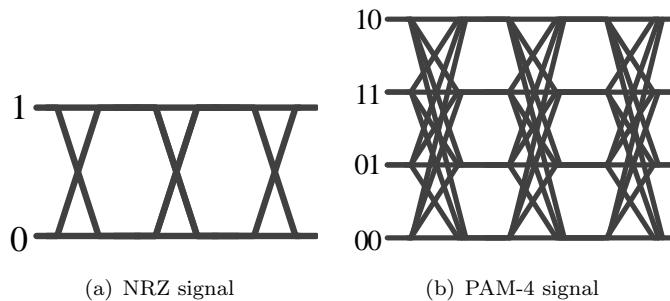


FIGURE 2.25: A NRZ data and a PAM4 data

Though the PAM4 requires only half of the symbol rate to complete the same data rate on NRZ which leads to lower the bandwidth performance requirement on the optoelectronic device, the PAM4 has a higher obligation on optical modulating amplitude (OMA). [131]

presents a comparison of a 25Gb/s NRZ and a 50Gb/s PAM4 (25Gbaud) transmission. To achieve the same BER, compare to NRZ, PAM4 needs around 6db higher on the OMA, as well as the extinction ratio (ER). Therefore, the increased ER of PAM4 is a compromise for low bandwidth requirements. Further than PAM4, PAM8 (3 bits per symbol), PAM16 (3 bits per symbol) or more signal levels could further increase the data rates. But because of Compared to PAM4, they are more difficult to implement and require a larger ER to maintain BER, in this section the pulse amplitude modulation is more focus on PAM4.

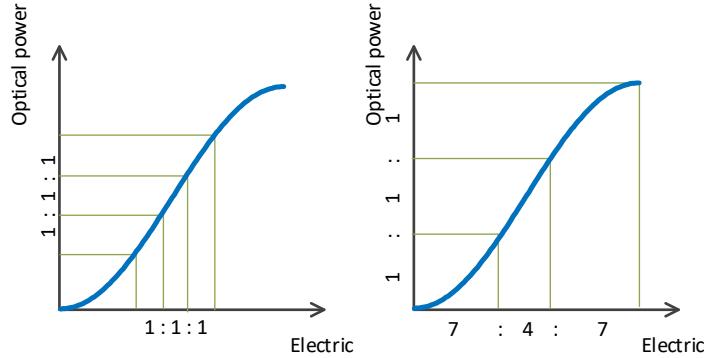


FIGURE 2.26: Optical PAM linearity problem example

Another noteworthy performance on PAM is the linearity of signal. Take PAM4 as an example, the four signal levels separate three eyes vertically placed on one data symbol. Linear amplitude response is desired to achieve equally in PAM because of the BER is limited by the least-open eye. Different types of modulators have their own methods of maintaining linearity. A VCSEL requires the modulating current signal that higher than the threshold current of VCSEL.[88; 121] MZM modulates signal depends the phase difference between two arms, hence the optical power transfer function is a  $\pi$  curve.[104] Assuming a PAM4 modulating is on a normalized ideal MZM and the modulated signal is on quadrature point the electric to optical power transfer function is presented in Fig.2.26. Inherent nonlinear phase limits the MZM either use the linear region around the quadrature point or optimize the electric modulating signal to maintain the optical amplitudes equalled. [103; 104; 137]

Fig.2.27 presents three architectures of PAM4 optical transmitter which consists of MZM.[99].

Fig.2.27(a) is PAM4 optical transmitter consists of a normalized MZM and an electric PAM4 to be its inputs. A electronic DAC combines two NRZ signal to be a electric PAM4 and amplified signal is fed into MZM to produce optical PAM4. This structure has high requirements on electrical devices. To achieve a DAC and modulator driver with fine linearity is increasing challenge at high speed.

[131] and [100] both demonstrate the PAM4 modulating with segmented MZM. Two individual NRZ modulates two pairs segmented phase shifters and forms the PAM4 signal

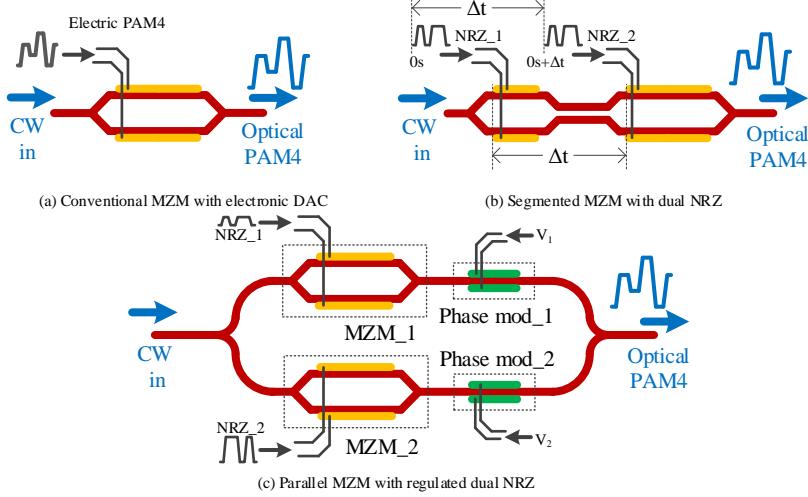


FIGURE 2.27: Optical PAM example with PAM4 on MZM[99]

on optical output. This configuration avoids electrical DAC to simplify the transmitter. However, this structure requires an electrical delay between two NRZ inputs to compensate for the first segment group delay.[100; 107] In addition, [131] observed the electrode bandwidth on short and long segment are un balanced and the PAM4 symbol rate is limited by the lower one (longer segment).

[101] demonstrates a parallel MZM PAM4 transmitter. NRZ2 is amplified by 6 dB in respect to the other NRZ1, such that NRZ1 and NRZ2 represent the most significant bit (MSB) and the least significant bit (LSB), respectively. Two NRZ signals individually modulate the optical carry wave on their arm and optical PAM4 is a result of merged modulated signals. Before the signals are combined, a phase shifter is necessary to modify the two arms' signal are in the same optical phase. This phase shifter is generally consists of heater on waveguide. In Fig.2.27, there are two of thermal phase shifters but usually, only one of them should be used.

Compare to segmented MZM architecture, insertion loss of parallel MZM is lower in the fair comparison, however the segmented MZM architecture would require a slightly lower drive voltage to achieve a similar ER.[101] The optimum drive voltage/optical insertion loss trades off between these two architectures. Compares with the conventional MZM with electric DAC configuration, the other two architectures both advantage on uses only NRZ as electric inputs, but the system level complexity is compromised.

### 2.7.3 Coherent optical transmitters

Coherent optical transmission in silicon photonics can double the transmitting data rates.

[74] presents a Quadrature Phase-Shift Keying (QPSK) optical transmitter bases on silicon MZM. The architecture of this optical transmitter is presented in Fig.2.28. In Fig.2.28, an optical carry wave is separated into two independent MZM and modulated the NRZ data. The thermal phase shifter on each arm has concealed into the independent MZM. The modulated two arms of signal are correct the phase on to quadrature via phase shifters (two phase shifters in the figure is generally only active one of them). The receiving of QPSK (or other coherent signal) relies coherent receiving system (direct-conversion receiver is the most comment system) but single PD. Received optical signal is mixed with quadrature carry waves from local oscillator laser, then detected by multiple PDs and fed into the DSP system to demodulate it.[51]

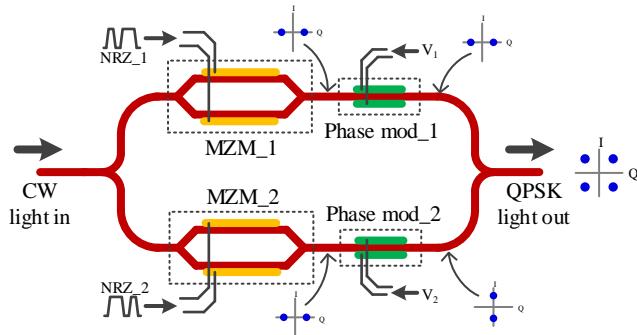


FIGURE 2.28: Optical QPSK with two MZM, edited from[74]

[26] demonstrates an polarization-division-multiplexed (PDM) QPSK optical transmitter which is available 112Gb/s transmission. PDM supports doubled the transmission data capability by using Transverse electric (TE) mode and Transverse magnetic (TM) mode via polarizer. In this review, it will not be deeper discussed. In either TE or TM mode, it is a QPSK modulating. Meanwhile each QPSK is 56Gb/s (dual 28Gb/s NRZ inputs).

In a QPSK optical transmitter, at least three thermal heaters (phase shifter) need to be adjusted. Two of them are in the two balanced MZM and the last one is used for adjusting I and Q on quadrature.[74] In addition, multiple RF amplifiers or modulator drivers have to integrate with the optical device in a limited area. An efficient heater control electronic circuit and modulator drivers which support compact integration are important for these coherent optical transmitters. [74] [123] also discusses (on an InP QPSK optical transmitter, but the similar scenario of silicon-based ones) the importance to optimize the efficiency of modulator drivers in these applications.

Optimize the NRZ to PAM signals could enhance the data transmission in limited bandwidth, hence it is QAM. In Fig.2.29, base on three different optical PAM4 methods in Sec.2.7.2, there are three general QAM16 optical transmitter architectures. The QAM16 optical transmitter in Fig.2.29(a) consists of conventional MZM with PAM electronic signal as inputs.[67; 124] And Fig.2.29(b) presents a QAM optical transmitter bases on multiple QPSK. The electronic inputs are multiple numbers of NRZ signals, and mod-

ulated QPSK on different amplitudes combines the QAM as a output.[30; 86; 97; 98] [2] demonstrates a Dual-Polarization 64-QAM optical transmitter. Through this design bases on a InP process, the QAM device on each polarization is a segmented MZM device. An abstract view which is transformed to a QAM16 is presented in Fig.2.29(c).

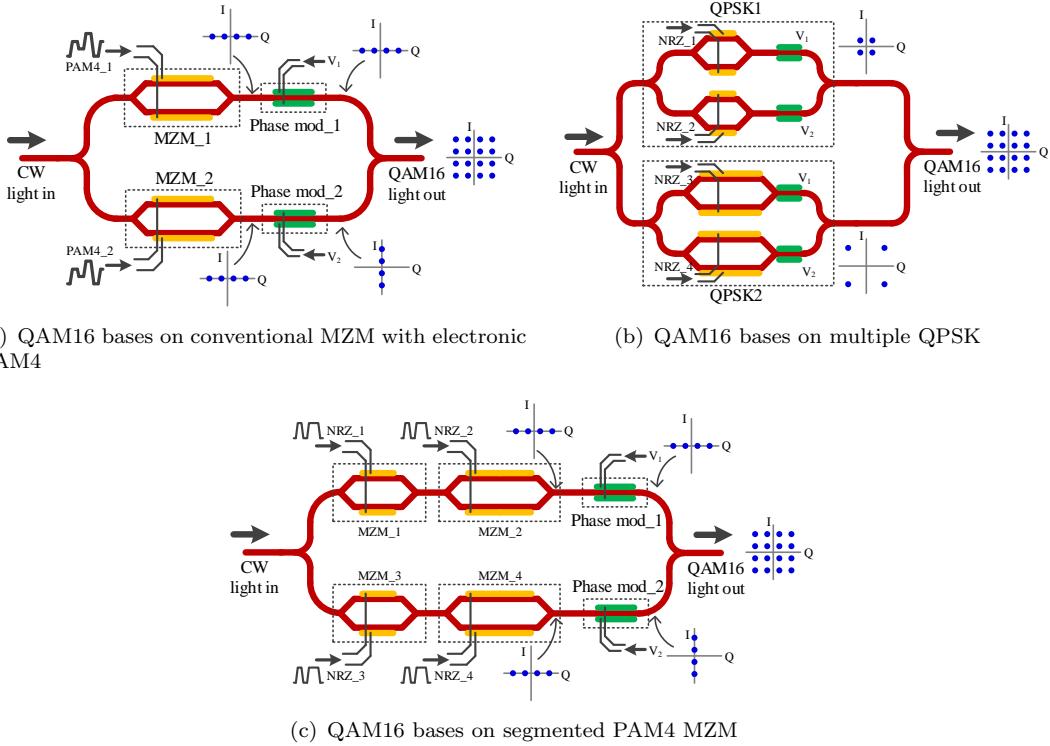


FIGURE 2.29: Three architectures of QAM16 optical transmitter

No matter which optical QAM transmitter architecture, it either requires higher performance on modulator drivers or further increases the number of modulator drivers in the system. In addition, the thermal phase shifters controller also should be considered to be embedded into the electronic circuit to optimize the optical calibrations. The electronic circuit for coherent optical transmitter increases the design difficulty onto the system level. More integration problem and system level control need to be considered and designed while maintaining design performance.

#### 2.7.4 Optical Discrete multi-tone modulation

Discrete multi-tone (DMT) modulation is an advanced modulation which has been used in general long distance optical communication. In short, it is frequency-division multiplexing applied on optical.

An abstract view of DMT link is shown in Fig.2.30. The DMT signal is generated through bit encoding, inverse fast Fourier transform (IFFT), cyclic prefix insertion processes. The receiver reverses the modulating process and a equalization is always

used.[16; 47; 110]

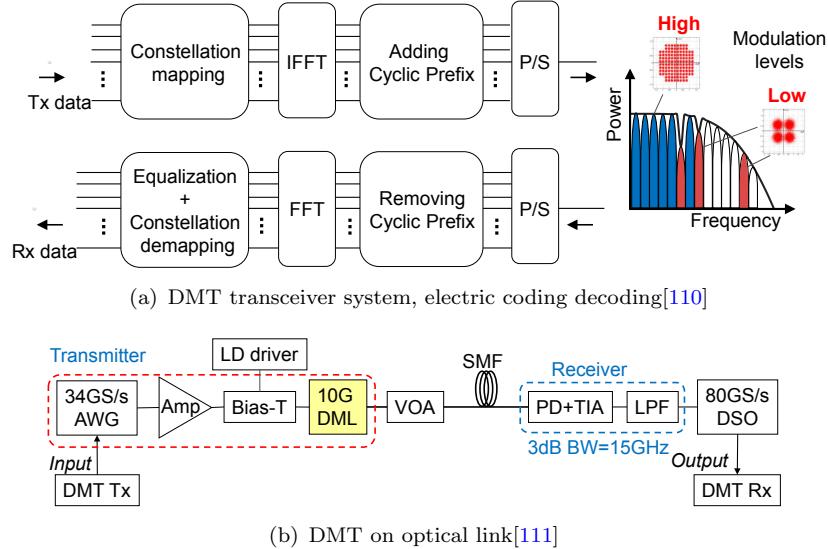


FIGURE 2.30: Optical DMT full link system

In a limited bandwidth, data capability of DMT could be higher than PAM4. A comparison in [10] presents a 8 bit DMT and a PAM4 on 100Gb/s transmission. PAM4 requires 32GHz bandwidth and it is only 20GHz on the 8 bit DMT.

Backward of DMT is the complexity. DMT requires complex constellation mapping (demapping in receiver) and IFFT (FFT in receiver) system to modulate the signal. [111] demonstrates a 50Gb/s DMT transceiver on a directly modulated laser (DML). But the electric transmitter and receiver are consists of arbitrary waveform generator (AWG) and digital storage oscilloscope (DSO). The electronic modulating and demodulating functions in this demonstration is still off-line DSP. To transform these off-line DSP to a real time processing system is challenging. In addition, the complexity of DMT increases power of the CMOS circuit. [10] estimates the power consumption of CMOS circuit for DMT is 2.5 times of PAM4.

To further improve the transmission data capability of DMT, orthogonal frequency-division multiplexing (OFMD) is the coherent DMT. The structure of OFMD is similar to the QPSK modulator, but input signals are two rail independent DMT signals. OFMD doubles the DMT transmission data rate, and it also doubled increases the transmitter circuit. The receiving of OFMD relies on the coherent optical receiver.

In order to reduce the backwards caused by complex DSP in DMT and OFDM, [129] and [71] demonstrate a all-optical OFMD transmitter system. The IFFT (and FFT in the receiver) implements as silicon photonics circuits, not general electronic DSP system. The inputs of this OFDM transmitter are independent 8 groups of NRZ digital signals.

## 2.8 Summary

In this chapter, the literature review covers a conventional optical transceiver's structure, the silicon photonics device are common related to the electric circuits, the integration of optoelectronic devices, conventional broadband technology for amplifier designs, the state of the art output stage structures for optical modulators and the complex modulating implementation on the silicon photonics.

In the silicon photonics transceiver, the modulator driver amplifies the highest operating speed signal and drives the optical modulators. Unlike the well researched electronic circuits, with the development of optical modulators, the research on the specially designed modulator driver is still very promising.

The electronic and optical chip integration is also essential in silicon photonics. Multiple integration methods are investigated regard to cost and performance of packaged devices. In the reviewed three integration method, though monolithic photonics platform enables to integrate the optical devices into the CMOS fabrication, lot of designers are still prefer wire bonding and flip chip approaches due to the cost and complexity of fabrication.

On the modulator driver, the general broadband technology for high-speed amplifiers and the typical output stage structures have been reviewed. In recent years, especially in the output stage design, more and more modified structures was presented in the literature.

The complex modulated optical transmitter could be seen as a silicon photonics circuit. The modulator drivers used on these circuits require to enhance the linearity, power efficiency, and compact integration while maintain the bandwidth performance.

From the reviewed literature, it can be seen that the CMOS based modulator driver for si MZM is promising. The silicon photonics circuit in future research and applications is seeking CMOS based circuits which is more efficient and compact to replace the commercial amplifier and related discrete devices. Therefore, while the bandwidth performance is maintained, the power efficiency and the integration method of CMOS modulator driver should be optimized to fit the future applications. In addition, some of the optical devices are sensitive to the environmental factors like temperature. The reliability of electronic circuit should be also researched due to it is a part of the compact integrated optical transmitter.

## Chapter 3

# Theoretical Analysis of N Over N Cascode Push Pull Modulator Driver

In the field of Silicon Photonics, an optical interconnection link using a Mach-Zehnder modulator (MZM) is common and well researched. Previous designs [48; 50; 61] use a current-mode logic circuit with resistive loads which can generate a high voltage swing at the output with good impedance matching performance, however, the problem is that most of these designs require an external biasing system (such as a biasing tee) to be integrated with an optical modulator.

For interconnection applications, the modulator driver design is expected to be low-cost and compact-provide. In this chapter, a novel output stage of modulator driver is created for MZM at low cost and low power. Most importantly, the modulator driver is available to compact integrated with MZM.

### 3.1 Introduction

A novel N-over-N cascode output stage for modulator driver is demonstrated and analyzed in this chapter.

After illustrating the function of the proposed circuit, mid-band performance and high frequency performance are calculated. This structure also supports compact integration for the si MZM and possesses advantages relating to a wide application range when compared with other conventional output stage structures. Lastly, two sections describe a bandwidth enhancement method with inductor peaking and an enhancement circuit with a pre-driver stage is developed base on the proposed topology.

### 3.2 Functionality of proposed circuit

Fig.3.1 presents the circuit of the N over N cascode push pull amplifier. The proposed circuit improves upon the conventional P over N cascode amplifier in Fig.3.1(a). An NMOS based source follower ( $M_4$ ) in the proposed N over N cascode amplifier replaces the PMOS based common source amplifier ( $M_4$ ) in the conventional P over N cascode amplifier.

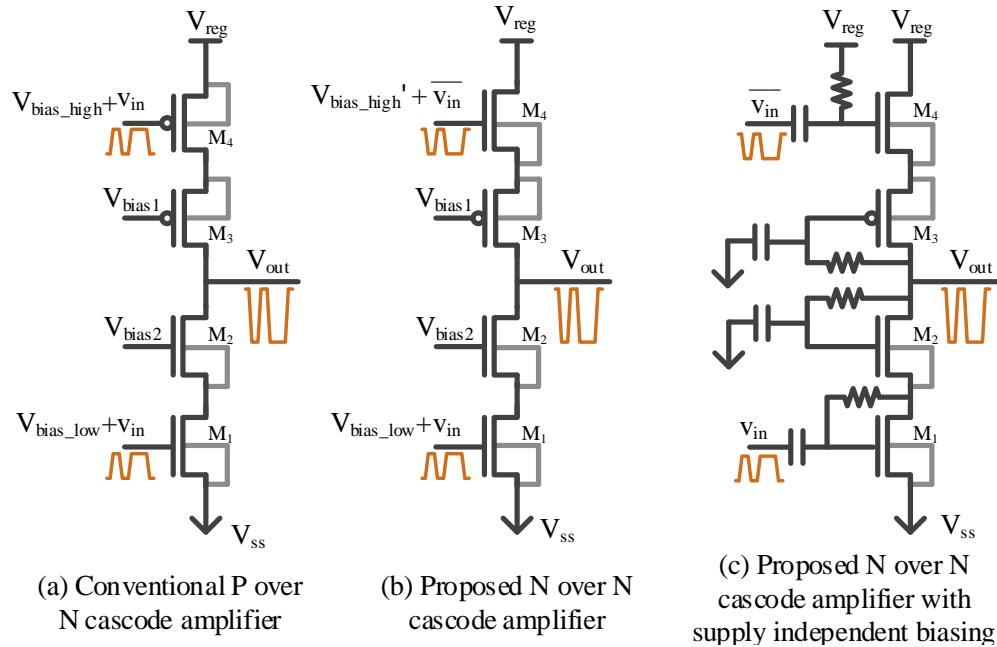


FIGURE 3.1: Circuit topology of N over N cascode push pull amplifier

In the conventional push-pull structure, the width of the PMOS is generally around three times that of the NMOS. With the top transistor replaced as an NMOS source follower, the input capacitance of the circuit could be decreased. In addition, another advantage is the bandwidth of the proposed circuit is enhanced. It is because of the bandwidth performance of a PMOS based common source amplifier is much lower than an NMOS based source follower.

Fig.3.1(b) presents the basic circuit of the N over N cascode push-pull amplifier, moreover Fig.3.1(c) presents a self-biased circuit topology for integrated circuit implementation. In the self biased topology, the  $V_{bias\_high}$  is placed onto  $V_{Reg}$ . Input signals are going through DC block capacitance and  $M_1$  and  $M_4$  are re-biased within the inner circuit. Cascode transistors are also re-biased by a local RC feedback network.

Fig.3.2 shows an actual signal example of the proposed circuit while a group of NRZ data signals are applied to it. This example signal is based on a 130nm process. The example transistor width ratio is  $W_{M1} : W_{M2} : W_{M3} : W_{M4} = 3 : 5 : 5 : 5$  and while simulation occurs, there is an AC  $50\Omega$  load applied onto the Out.

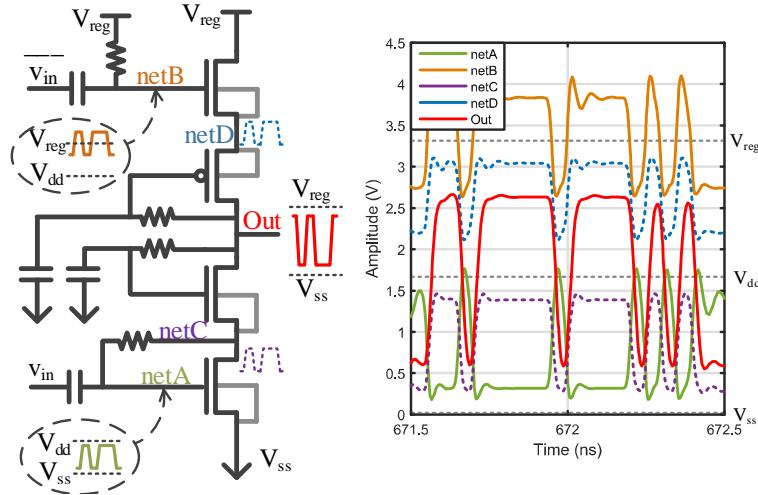


FIGURE 3.2: Functionality of N over N cascode amplifier

The resulting behavior of voltage signals on five nets are also presented in the figure. The two inputs (*netA* & *B*) are differential signals and re-biased on DC operating points at *netC* and  $V_{reg}$ . The regulated supply ( $V_{reg}$ ) is 3.3V. *NetC* and *netA* are inverted phase due to the NMOS common source amplifier  $M_1$ . The voltage  $V_{gd}$  of  $M_4$  varies in the range  $\pm 0.8V$ . The signal on the gate (*netB*) and source (*netD*) of  $M_4$  are in the same phase.  $V_{gs}$  and  $V_{ds}$  of  $M_4$  are also less than 1.6V in data transmission. Therefore, the voltage differences between the nodes on  $M_4$  are always less than the break-down voltage ( $V_{break\_down} = 1.6V$  in this 130nm CMOS process).

### 3.3 Mid-band performance analysis

In this section and the next section, the proposed circuit is analysed by small-signal analysis. Though the amplifier is practice in a large swing signal, the small-signal performance analysis still provides us with the amplifier performance around the bias point, therefore it presents a significant direction to adjust the circuit.

The analysis of the proposed circuit starts with the mid-band gain analysis. This section describes the gain of the amplifier and the output impedance of the proposed circuit.

Fig.3.3 is the mid-band small signal model of the N over N cascode push pull amplifier.

In this small signal model (Fig.3.3),  $v_x$  ( $v_y$ ) is patellar loading  $g_{m2} \times v_{gs2}$  ( $g_{m3} \times v_{gs3}$ ) and  $r_{ds2}$  ( $r_{ds3}$ ) to  $v_{out}$ . To simplify this small signal model to an equivalent model which is easier to modify regarding nodal equations, transform trans-conductance model in cascode transistors to  $g_{m2} \times v_{gs2} = -g_{m2} \times v_x$  ( $g_{m3} \times v_{gs3} = -g_{m3} \times v_y$ ) with a load impedance  $1/g_{m2}$  ( $1/g_{m3}$ ) on  $v_x$  ( $v_y$ ). The simplified equivalent mid-band small signal model is presented in Fig.3.4.

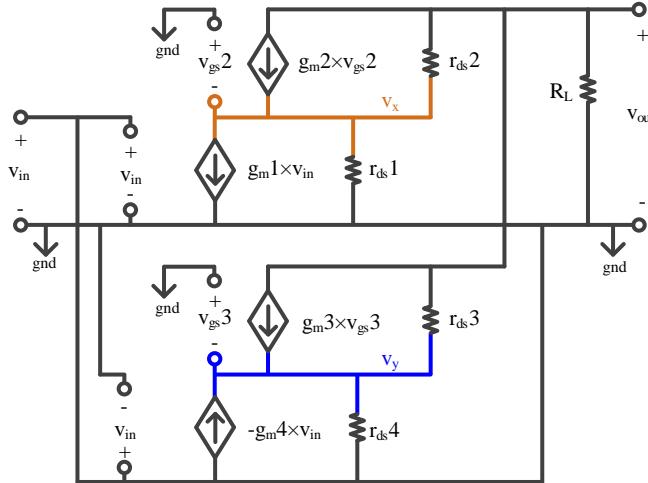


FIGURE 3.3: Mid-band small signal model of N over N cascode amplifier

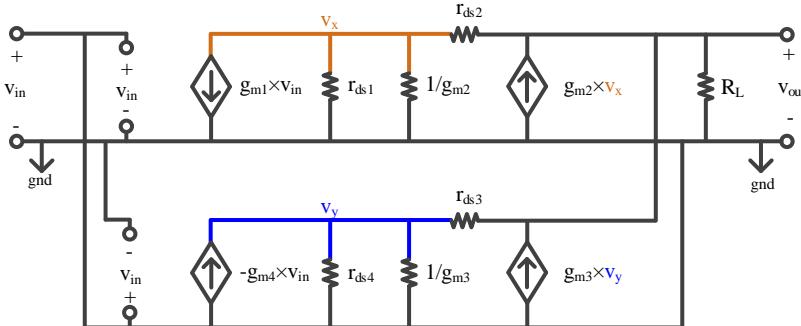


FIGURE 3.4: Simplified equivalent mid-band small signal model of N over N cascode amplifier

Based on the simplified small signal model in Fig.3.4, the nodal equations becomes,

$$\begin{cases} v_{out}(g_L + g_{ds2} + g_{ds3}) = v_x(g_{ds2} + g_{m2}) + v_y(g_{ds3} + g_{m3}) \\ -g_{m1}v_{in} = (g_{ds1} + g_{ds2} + g_{m2})v_x - g_{ds2}v_{out} \\ -g_{m4}v_{in} = (g_{ds4} + g_{ds3} + g_{m3})v_y - g_{ds3}v_{out} \end{cases} \quad (3.1)$$

Solving for transfer function  $v_{out}/v_{in}$ , it yields as below,

$$\frac{v_{out}}{v_{in}} = -\frac{\frac{(g_{ds2}+g_{m2})g_{m1}}{g_{ds1}+g_{ds2}+g_{m2}} + \frac{(g_{ds3}+g_{m3})g_{m4}}{g_{ds1}+g_{ds2}+g_{m2}}}{g_L + g_{ds2} + g_{ds3} - \frac{(g_{ds2}+g_{m2})g_{ds2}}{g_{ds1}+g_{ds2}+g_{m2}} - \frac{(g_{ds3}+g_{m3})g_{ds3}}{g_{ds1}+g_{ds2}+g_{m2}}} \quad (3.2)$$

In Eq.3.2, the mid-band transfer function is complex due to the pull up network and pull down network being entirely parallel with each other. To simplify the mid-band transfer function, it can be assumed that all the parameters in the pull up network are the same value as the matching factors in the pull down network. Assume  $g_{m1} = g_{m4}$ ,

$g_{m2} = g_{m3}$ ,  $g_{ds1} = g_{ds4}$  and  $g_{ds2} = g_{ds3}$ , the transfer function yields as below,

$$\frac{v_{out}}{v_{in}} = -\frac{-2 \times g_{m1}(g_{ds2} + g_{m2})}{2 \times g_{ds1}g_{ds2} + g_L(g_{ds1} + g_{ds2} + g_{m2})} \approx \frac{-2 \times g_{m1}}{g_L} \quad (3.3)$$

Based on the previous assumption, the simplified transfer function can be approximated as,

$$\frac{v_{out}}{v_{in}} \sim -\frac{g_{m1}(g_{ds2} + g_{m2}) + g_{m4}(g_{ds3} + g_{m3})}{g_{ds1}g_{ds2} + g_{ds4}g_{ds3} + g_L \frac{g_{ds1} + g_{ds2} + g_{m2} + g_{ds4} + g_{ds3} + g_{m3}}{2}} \sim \frac{-g_{m1} - g_{m4}}{g_L} \quad (3.4)$$

The mid-band output impedance is,

$$\begin{aligned} r_{out} &= (r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2})\|(r_{ds4} + r_{ds3} + g_{m3}r_{ds4}r_{ds3})\|R_L \\ &\approx R_L \end{aligned} \quad (3.5)$$

Therefore, to provide a  $50\Omega$  output impedance in the mid-band frequency range, the solution is to create a load resistance at the output of the amplifier with  $R_L = 50\Omega$  or higher than  $50\Omega$  depending on the value of the patellar part  $(r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2})\|(r_{ds4} + r_{ds3} + g_{m3}r_{ds4}r_{ds3})$ . Note this  $R_L$  should be an AC effective only load resistance. Otherwise, this load resistance on the output will affect the DC bias of all transistors. Due to most implementations of proposed circuits are fully differential amplifiers, creating a load resistance  $R_L = 100\Omega$  or higher than  $100\Omega$  between the differential outputs is a simple solution to turn the output impedance to  $50\Omega$  on each single end without affecting DC biasing.

While the proposed circuit connects to MZM, and the MZM could be traded as a  $50\Omega$  transmission line, there should be an AC  $50\Omega$  termination after the MZM. Therefore, the overall  $R_L$  on mid-band in design implementation is close to  $25\Omega$  in the mid-band.

### 3.4 Frequency response analysis

The previous section illustrates the mid-band performance of the N over N push pull cascode amplifier. In this section, the frequency response of the proposed circuit will be analyzed. Extraction of poles and zeros in the circuit is the basic of further improvement related to bandwidth enhancement.

Fig.3.5 presents a small signal model of proposed circuit topology with parasitic capacitance.

Note there is input resistance (source impedance,  $R_i$ ) also added (to avoid confusion with factor  $s = j \times \omega$ , it has been named  $R_i$  but the common name is  $R_s$ ) into the circuit. In the proposed circuit, due to deep N-well NMOS will be used on  $M2$  and  $M4$  (bulk is going to share the voltage on source of this transistor) and bulk of PMOS

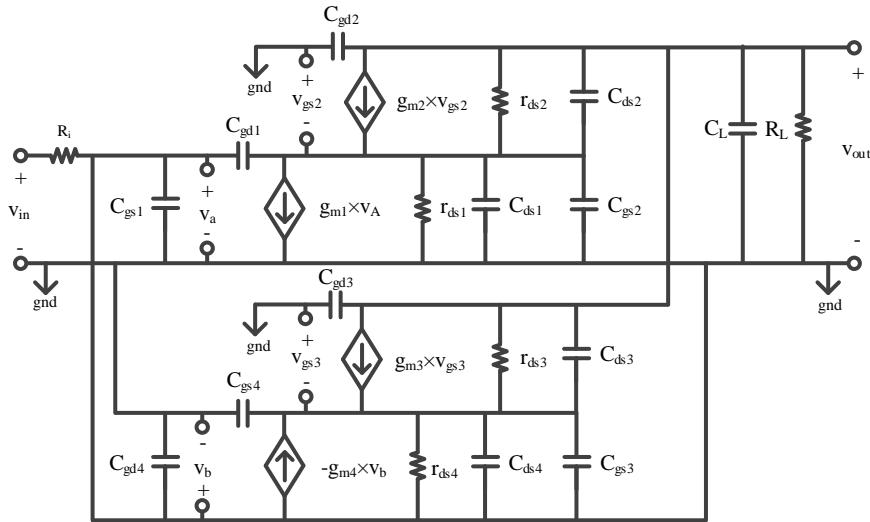


FIGURE 3.5: Small signal model of N over N cascode amplifier

$M3$  will directly connect to the source of this transistor. There will be no significant body effect,  $C_{db2}$  ( $C_{db3}$ ) and  $C_{sb2}$  ( $C_{sb3}$ ), and in general the cascode system, it has been replaced by  $C_{ds2}$  ( $C_{ds3}$ ).

This small signal model needs to be simplified for further analysis. Hence, all cascode stages have been simplified regarding transfer to ground base stage with all capacitance combined. The small signal has been simplified as shown in Fig.3.6.

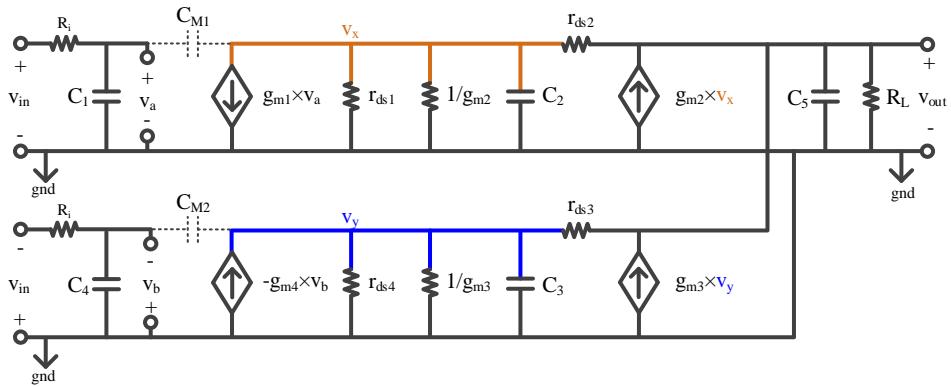


FIGURE 3.6: Simplified equivalent small signal model of N over N cascode amplifier

In the simplified small signal model, combined capacitors  $C_1$ ,  $C_2$ ,  $C_3$ ,  $C_4$  and  $C_5$  are

listed as below,

$$\left\{ \begin{array}{l} C_1 = C_{gs1} + C_{gd1} \\ C_2 = C_{gd1} \cdot (1 + \frac{v_x}{v_a}) + C_{ds1} + C_{gs2} \\ \quad \cong 2 \times C_{gd1} + C_{ds1} + C_{gs2} \\ C_3 = C_{gd4} \cdot (1 - \frac{v_x}{v_a}) + C_{ds4} + C_{gs3} \\ \quad \cong C_{ds4} + C_{gs3} \\ C_4 = C_{gs4} \\ C_5 = C_{gd2} + C_{gd3} + C_{ds2} \cdot (\frac{v_{out}}{v_x} - 1) + C_{ds3} \cdot (\frac{v_{out}}{v_y} - 1) + C_L \\ \quad \cong C_{gd2} + C_{gd3} + C_{ds2} + C_{ds3} + C_L \end{array} \right. \quad (3.6)$$

The additional information which must be mentioned here is all are split Miller capacitors.

In Fig.3.6, Miller capacitor  $C_{M1} = C_{gd1}$  in  $M1$  is split into  $C_1$  and  $C_2$ . With I/O phase inverting and Miller effect analysis,  $C_1$  (on gate of  $M1$ ) receives one instance of Miller capacitor  $C_{gd1}$ , and the output (drain of  $M1$ ) receives the split Miller capacitor as

$$C_{Mo1} = (1 + Av)C_{gd1} \cong C_{gd1} \cdot (1 + \frac{v_x}{v_a})$$

. Assume output (drain) of  $M1$  amplifies the input signal with the gain approximately to 1 or even less than 1 to match the source follower  $M4$ ,  $C_{Mo} \approx C_{gd1} \cdot (1 + 1) = 2 \times C_{gd1}$ . Therefore, the  $C_{Mo}$  in  $C_2$  is presented as shown in Eq.3.6.

Simultaneously, the I/O of the Miller capacitor  $C_{M2}$  on  $M4$  shares the same phase on gate and source, and it will not split any capacitance on  $C_4$ . On output (source) of  $M4$ , the split Miller capacitance on  $C_3$  is given by,

$$C_{Mo2} = (Av - 1)C_{gd4} \cong C_{gd4} \cdot (\frac{v_y}{v_b} - 1)$$

Since the gain of the source follower is close to 1 but less than 1,  $C_{Mo2} = (1 - 1)C_{gd4} = 0$ ,  $C_3$  also receives no capacitance from  $C_{M2}$ .

The other two Miller capacitors on the two cascode transistors  $M2$  and  $M3$  are  $C_{ds2}$  and  $C_{ds3}$ . The I/O of the cascode transistors are also the same signal phase. Thus, there is no split Miller capacitance on  $C_2$  and  $C_3$ . Assuming the gain of the cascode transistor is 2 times gain, on  $C_5$ , Miller capacitance split into output capacitance is approximately one time  $C_{ds2}$  and  $C_{ds3}$ .

Though splitting the Miller capacitor is kind of rough, it literally simplifies the circuit for further analysis. However, there is a risk, which is a potential zero is removed while the Miller capacitor is split into I/O capacitance. Based on the simulation mentioned later, luckily in implementation, this zero being located somewhere will not significantly

affect  $\omega_{-3dB}$ . Therefore, splitting Miller capacitor is acceptable in this analysis.

Based on the simplified small signal model in Fig.3.6, the nodal equations now become,

$$\begin{cases} v_{out}(g_L + g_{ds2} + g_{ds3} + sC_5) = v_x(g_{ds2} + g_{m2}) + v_y(g_{ds3} + g_{m3}) \\ -g_{m1}v_a = (g_{ds1} + g_{ds2} + g_{m2} + sC_2)v_x - g_{ds2}v_{out} \\ -g_{m4}v_b = (g_{ds4} + g_{ds3} + g_{m3} + sC_3)v_y - g_{ds3}v_{out} \\ v_a = \frac{g_i}{g_i + sC_1}v_{in} = \frac{1}{1 + sC_1 R_i}v_{in} \\ v_b = \frac{g_i}{g_i + sC_4}v_{in} = \frac{1}{1 + sC_1 R_i}v_{in} \end{cases} \quad (3.7)$$

Since the full transfer function is complex, and from  $v_{in}$  to  $v_{out}$ , there are at least three poles, the full transfer function is very difficult to analyze and with the three poles in the single transfer function it is almost impossible to split every pole. In this case, since Miller capacitors  $C_{M1}$  (and  $C_{M2}$ ) have been split into  $C_1$  ( $C_4$ ) and  $C_2$  ( $C_3$ ),  $v_{in}$  to  $v_a$  (or  $v_b$ ), and from  $v_a$  (or  $v_b$ ) to  $v_{out}$  can be regulated as two independent transfer function modules. From  $v_a$  (or  $v_b$ ) to  $v_{out}$ , there are two poles, and the extra pole will be generated by circuit from  $v_{in}$  to  $v_a$  (or  $v_b$ ).

The circuit from  $v_a$  (or  $v_b$ ) to  $v_{out}$  is composed of the pull up and pull down networks which are entirely parallel with each other. To simplify the complexity of the transfer function, the parameters in these two networks are assumed matching. With assumption of  $g_{m1} = g_{m4}$ ,  $g_{m2} = g_{m3}$ ,  $g_{ds1} = g_{ds4}$ ,  $g_{ds2} = g_{ds3}$  and  $C_2 = C_3$ , the transfer function is represented as below,

$$\frac{v_{out}(s)}{v_a(s)} = \left( \frac{1}{1 + as + bs^2} \right) \left( \frac{-2 \times g_{m1}(g_{ds2} + g_{m2})}{2 \times g_{ds1}g_{ds2} + g_L(g_{ds1} + g_{ds2} + g_{m2})} \right) \quad (3.8)$$

where

$$a = \frac{C_2(g_L + 2 \times g_{ds2}) + C_5(g_{ds1} + g_{ds2} + g_{m2})}{2 \times g_{ds1}g_{ds2} + g_L(g_{ds1} + g_{ds2} + g_{m2})} \quad (3.9)$$

and

$$b = \frac{C_2 C_5}{2 \times g_{ds1}g_{ds2} + g_L(g_{ds1} + g_{ds2} + g_{m2})} \quad (3.10)$$

Assume that the general second-order polynomial can be written as below,

$$P(s) = 1 + as + bs^2 = \left(1 - \frac{s}{p1}\right) \left(1 - \frac{s}{p2}\right) = 1 - s\left(\frac{1}{p1} + \frac{1}{p2}\right) + \frac{s^2}{p1p2} \quad (3.11)$$

Now, assume  $|p2| \gg |p1|$ , then  $P(s)$  can be simplified as below,

$$P(s) \approx 1 - \frac{s}{p1} + \frac{s^2}{p1p2} \quad (3.12)$$

Therefore, the two poles can be written in terms of  $a$  and  $b$  as below,

$$\begin{cases} p1 = \frac{-1}{a} \\ p2 = \frac{-a}{b} \end{cases} \quad (3.13)$$

Applying this to the previous Eq.3.9, the first pole is given by,

$$\begin{aligned} p1 &= \frac{-(2 \times g_{ds1}g_{ds2} + g_L(g_{ds1} + g_{ds2} + g_{m2}))}{C_2(g_L + 2 \times g_{ds2}) + C_5(g_{ds1} + g_{ds2} + g_{m2})} \\ &\approx \frac{-g_L}{C_5} \end{aligned} \quad (3.14)$$

And applying this to the previous Eq.3.9 and Eq.3.10, the second pole is given by,

$$\begin{aligned} p2 &= \frac{C_2(g_L + 2 \times g_{ds2}) + C_5(g_{ds1} + g_{ds2} + g_{m2})}{C_2C_5} \\ &\approx \frac{-g_{m2}}{C_2} \end{aligned} \quad (3.15)$$

Assume  $C_2$  and  $C_5$  are in the same order of magnitude (in real application,  $C_5$  is much bigger than  $C_2$  due to load capacitance  $C_L$ ), and  $g_{m2}$  is greater than  $g_L$ , then  $|p1|$  is smaller than  $|p2|$ . Thus, the previous approximation  $|p2| \gg |p1|$  is valid.

In addition, there is an extra pole at the input of the circuit,

$$v_a = \frac{g_i}{g_i + sC_1} v_{in} = \frac{1}{1 + sC_1R_i} v_{in} \quad (3.16)$$

the pole is given by,

$$pole = -\frac{g_i}{C_1} \quad (3.17)$$

To simplify the previous calculation of frequency response, the circuit has been assumed to be a pull down network and pull up network mirroring each other. With implementation, it is generally  $C_1 > C_4$  due to Miller effect capacitance. In this topology, the pull down network and pull up network are fully parallel with each other. Therefore  $p2$  and  $p3$  will generate by major effective capacitance but not the smaller one. However, all of these capacitances are still in the same order of magnitude, and the other halfs lower effect arm should not be ignored.

To summarize all the above, there are three poles in the N over N cascode amplifier stage. In order they are given as,

$$p1 \approx -\frac{g_L}{C_5} \quad (3.18)$$

$$p2 \approx -\frac{g_{m2}}{C_3} \quad or \quad p2' \approx -\frac{g_{m2}}{C_2} \quad (3.19)$$

$$p3 = -\frac{g_i}{C_1} \quad or \quad p3' = -\frac{g_i}{C_4} \quad (3.20)$$

In fact, if the Miller capacitor is not split into  $C_1$  ( $C_4$ ) and  $C_2$  ( $C_3$ ), there should be a zero approximate  $g_{m1}/C_{M1}$  ( $g_{m4}/C_{M2}$ ). This is a disadvantage of simply splitting the Miller capacitors in the analysis. The author has compared these two modules (split Miller capacitor and not) with factors from an example circuit, and the result shows this zero will not significantly affect the  $-3dB$  frequency. This missing zero can be classified as a minor error due simplifying the calculation.

Base on previous frequency response analysis, hereinafter provides an example circuit on a 40nm CMOS process. Assume  $M1 = 100\mu m/40nm$ ,  $M2 = 100\mu m/40nm$ ,  $M3 = 300\mu m/40nm$  and  $M4 = 100\mu m/40nm$ . The small signal model frequency response and Spectre simulation based on circuit are plotted in Fig.3.7. The DC operating parameters for small signal model frequency response analysis are carried from the transistors via the Spectre simulator.

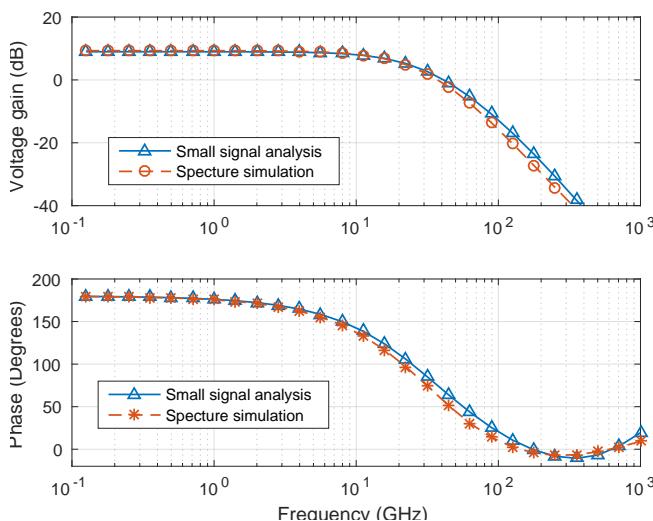


FIGURE 3.7: A comparison of small signal model analysis and Spectre simulation on example N over N cascode amplifier

The results show Spectre simulation and small signal model analysis basically match with each other. The pass-band gain readings are  $9.305dB$  and  $8.963dB$  with  $-3dB$  bandwidth located at  $19.5GHz$  and  $17.37GHz$  of small signal model simulation and Spectre analysis. The minor mismatch is may because of inaccurate extraction parasitic parameters or missing parameters while the module is simplifying. Therefore, the small signal model could effectively describe the frequency response of the proposed circuit. Meanwhile, the small signal model also helps designer to analyze the proposed circuit and calculate the overall performance. Furthermore, in later sections, the improve about bandwidth enhancement is also based on the analysis in this section.

The mid-band performance analysis in previous section and the frequency response analysis are both basing on the small signal model of the circuit. Though the driver itself is a large signal circuit, in high speed operating scenario, the small signal model still provides the gain, bandwidth performance at the DC biasing point. In addition, the

small signal model analysis links the load impedance, parasitics onto the transistor level circuit which guides the method of circuit design.

While large signal applies on the driver, another significant performance of the modulator driver is the headroom (output voltage swing) of it. Assume the transistor width of modulator drivers are large enough to load the output impedance, in the mid-band, the headroom of the circuit is approximate from  $V_{TH,M3} + V_{TH,M4}$  (on output logic '0' DC biasing) to  $Vdd - V_{TH,M1} - V_{TH,M2}$  (on output logic '1' DC biasing). Due to the  $V_{TH}$  of transistor is devices by the CMOS processes, it is difficult to optimize. In order to provide a more specific performance analysis about the large signal performance (output signal voltage swing), the proposed circuit is compared with several other circuit topologies within a example process in next section.

### 3.5 Comparison of multiple circuit topologies

Small signal analysis in previous sections only provides a overall performance of amplifier around the bias point. In order to present performance of the proposed circuit which operates in large signal environment, four conventional output amplifier topologies for modulator driver and the proposed circuit are compared with using simulation in this section. In Fig.3.8, these five different topologies of output stage are presented in a 40nm CMOS process. For the reason of assuming the specification of the drivers designed for the MZM, these five drivers are always loading up a pair of termination  $50\Omega$  in different methods.

In order, these five topologies are,

**(a) Current mode logic (CML) amplifier with biasing tee network**

Hereinafter referred to as biasing tee network, this is a CML based modulator circuit topology. There is a modulator driver operating a 10Gb/s data rate with a biasing tee network in [61] with a  $0.18\mu m$  CMOS process. With the biasing tee network, the DC operating point of the modulator driver output is biased. The current density of transistors is increased to peak  $f_T$  with minimal power consumption. In this simulation comparison, a modified circuit with a 3V power supply is built into a 40nm CMOS process with an ideal biasing tee network ( $L_{BT} = 10\mu H$ ,  $C_{BT} = 10\mu F$ ) with 2V biasing power supply. The disadvantage of this topology is a biasing tee network is an off-chip device which has a very large area and is very difficult to compact integrate into a circuit.

**(b) Current mode logic amplifier with double DC termination**

Hereinafter referred to as double DC termination, this is a CML based modulator circuit topology. [5] demonstrated a 20Gb/s data rate modulator driver with double DC termination in a  $0.13\mu m$  SOI CMOS process. The termination of this

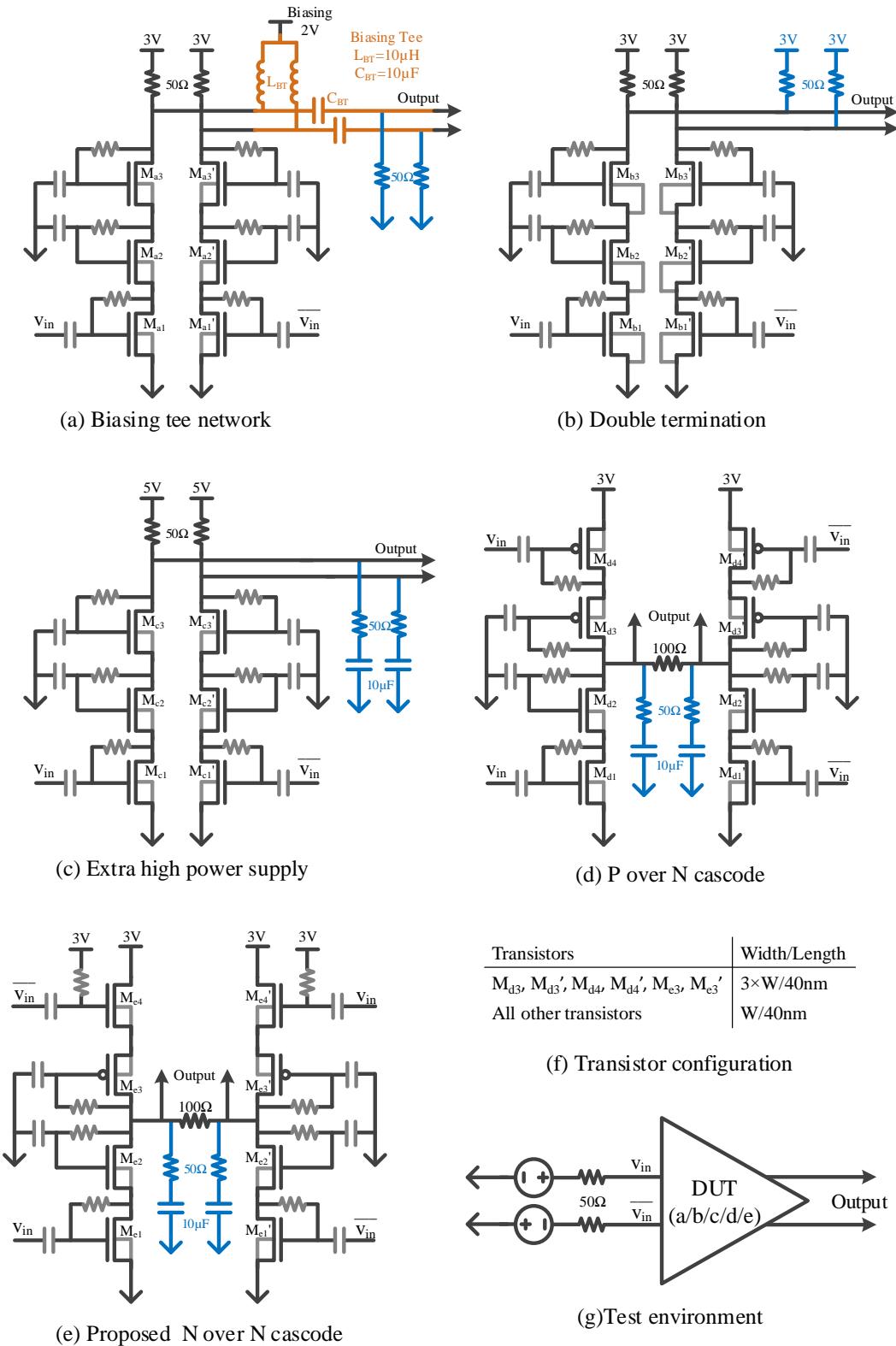


FIGURE 3.8: Five different output stage of modulator driver circuit topologies and the testing environment

topology is not an AC termination but a DC termination on power supply (3V in this simulation comparison). Unlike a biasing tee network topology, this circuit requires only termination resistance but also the power supply on the termination. Therefore, double DC termination could be compact integrated to MZM but an extra power supply connected to termination resistances is required.

**(c) Current mode logic amplifier with extra high power supply**

Hereinafter referred to as extra high power supply, this is a CML based modulator circuit topology. In [48], a modulator driver based on extra high power supply topology achieved 40Gb/s data rate without an extra biasing network in a 45nm SOI CMOS process (NMOS  $f_T > 400GHz$ ). The power supply in this design is 5V but 3V which could lead to the aforementioned voltage breakdown problem. This topology needs no external biasing network but only termination at the end of transmission, thus it could be easily compact integrated to MZM. In this simulation comparison, it has been modified as a supply independent self bias model and all transistors are standard CMOS but SOI versions.

**(d) P over N cascode amplifier (push pull mode)**

Hereinafter referred to as P over N cascode, it is a push pull based modulator circuit topology. [58] presents a P over N cascode amplifier as a modulator output driver for a micro-ring resonator. In this simulation comparison, it has been modified as a  $50\Omega$  output AC impedance driver which is suitable for integrating with MZM without extremal biasing network but only terminations. This circuit topology requires only AC termination after transmission, so compact integration of this circuit and MZM is available.

**(e) N over N cascode amplifier (push pull mode)**

Hereinafter referred to as N over N cascode or proposed circuit/topology, this is a push pull based modulator circuit topology. This circuit also has advantage of compact integration like a P over N cascode modulator driver.

To simplify the comparison, all circuit topologies have been modified as a without inductor version. All topologies are input resource independent (with DC blocks) and cascode transistors are also self biased. All AC coupling capacitors and bypass capacitors are  $5pF$  and resistance is  $40k\Omega$ . There are  $50\Omega$  as loading in the current mode logic topologies and  $100\Omega$  as termination resistance between differential outputs in the push pull topologies to evaluate the AC output impedance close to  $50\Omega$  on each end of the output, which is also independent by width of transistors. All width of PMOS in the circuits is three times of width the NMOS as presented in Fig.3.8(f). The assumed MZM can be placed between the driver output and termination  $50\Omega$  (blue in figure). As Fig.3.8(g) shows, the input is a pair of differential signal with  $50\Omega$  source resistance (push-pull amplifiers requires two pairs of inputs).

The result of the simulation is compared in Fig.3.9.

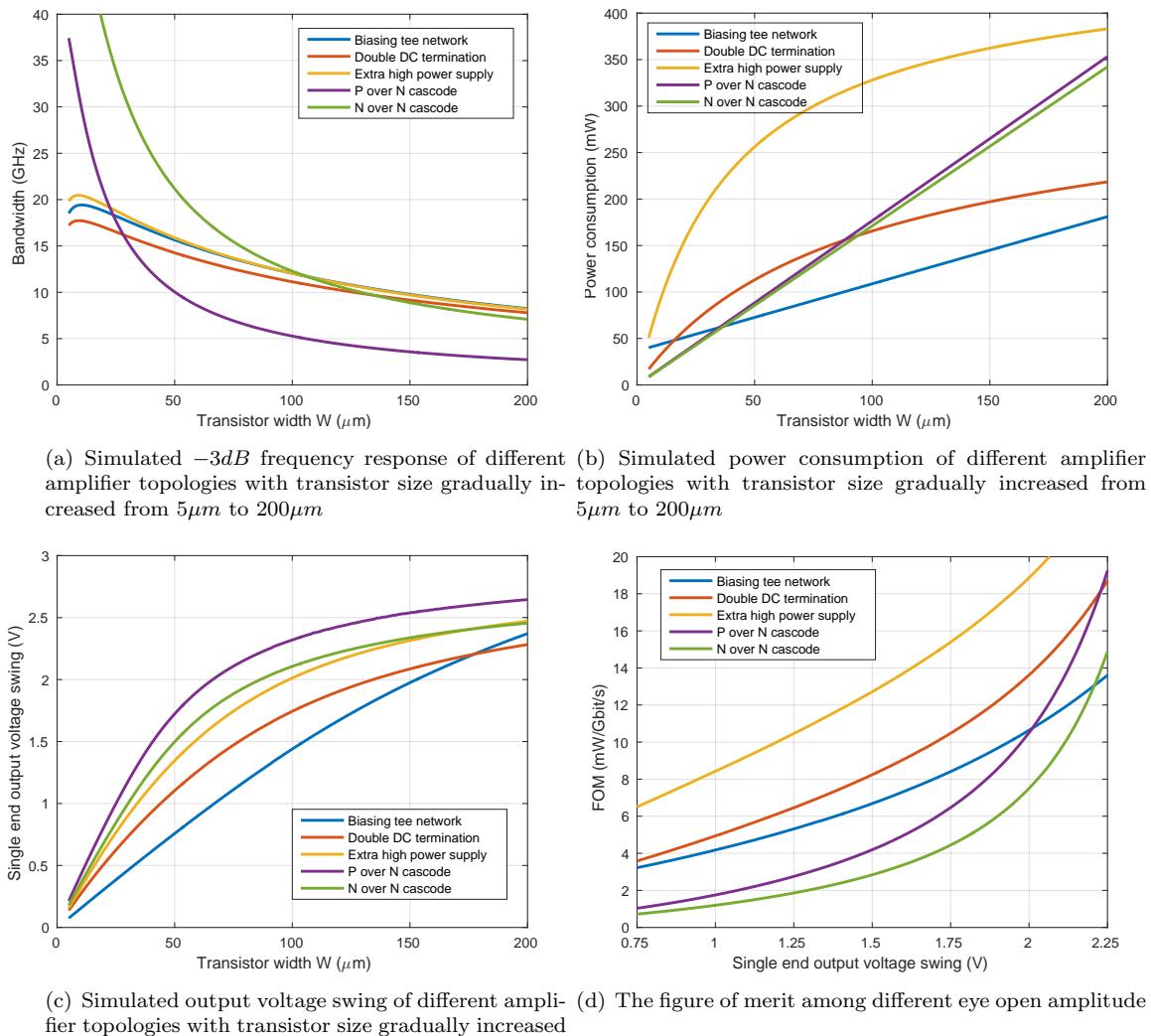


FIGURE 3.9: Simulation comparison result of five different modulator driver (amplifier) circuit topologies

In Fig.3.9 (a-c), in order, the bandwidth ( $-3\text{dB}$  frequency) performance, power consumption and single end output voltage swing are compared while the  $W$  (the width of NMOS, and width of PMOS is  $3 \times W$ ) is gradually increased from 5  $\mu\text{m}$  to 200  $\mu\text{m}$ .

Three topologies based on CML generate similar bandwidth performance while transistor size gradually increases. While  $W > 25\mu\text{m}$ , the bandwidth of P over N cascode is much less than other topologies due to  $f_T$  limitation and the large capacitance load on inputs of PMOS. The proposed circuit generates great bandwidth performance even while  $W > 100\mu\text{m}$ , and the proposed circuit bandwidth performance is not much worse than other CML results.

Due to the biasing tee biases output with a broadband effective inductor, the biasing tee network generates the best power consumption performance and is linear to the transistor size increases (power consumption already includes the power of biasing at

$2V$  for biasing tee). The power consumption of both push pull based topologies are quite linear to transistor size increases. The power consumption of the other two CML based topologies are gradually saturated while transistor size is over  $100\mu m$ .

Apart from the biasing tee network, all the other topologies gradually appear with saturation to experience output voltage swing while  $W > 100\mu m$ . With all of them, push pull based topologies exhibit generally better performance on output swing than CML based topologies.

Base on *data rate (Gbit/s) = BW/0.7*, Fig.3.9(d) presents the FOM (*figure of merit = Power consumption/data rate*) of five driver topologies among output voltage swing. This is a fair comparison for achieving the same output swing, or the efficiency of different drivers. As the results show, with a 40nm process, the two push pull based topologies generate better FOM performance until  $2V$ . Until the  $2.2V$  single end voltage swing, the proposed circuit is always the best choice of all topologies.

As for the simulation of other process nodes, the N over N push pull cascode output stage also generates the best FOM in comparison. In a 130nm CMOS process, the proposed topology is the best FOM until output voltage swing that is larger than  $1.75V$ . In a 65nm CMOS process, the proposed topology is the best FOM until output voltage swing that is larger than  $1.9V$ . Lastly, Table3.1 generally summarizes the performance of five circuit topologies.

TABLE 3.1: Performance comparison of multiple amplifier output stage circuits

Circuit topologies	Bandwidth	Power	Output Vpp	Efficiency
Biasing Tee	Good	Very low	Worse	Worse
Double termination	Good	Good	Worse	Fair
Extra high power supply	Good	Very high	Good	Fair
Conventional P over N	Worse	Good	Best	Good
Proposed N over N	Good	Good	Good	Best

Summarizing the above, the N over N cascode push pull amplifier could generate the best FOM regarding a wide output voltage amplitude requirement. The bandwidth performance of the proposed topology is also as good as other CML based topologies. This proposed circuit requires no external biasing network but only simple terminations while it is compact integrated to MZM or other transmission line based devices. Therefore, for a wide range of output swing and bandwidth requirements, an N over N cascode push pull amplifier as a modulator driver output stage is a great selection.

### 3.6 Improved proposed circuit with inductive peaking

To further improve the overall bandwidth performance of the N over N cascode amplifier, inductive peaking is add to the proposed circuit. Fig.3.10 is the proposed circuit with

inductive peaking bandwidth enhancement. Overall, there are five inductors. Two inductors ( $L_1$  and  $L_4$ ) are located at the gates of input transistors. On the gate of cascode transistors ( $M_2$  and  $M_3$ ), there are two inductors ( $L_3$  and  $L_4$ ) in an RCL network which is biased with voltage reference. Another inductor ( $L_5$ ) is inserted before the output of the proposed circuit.

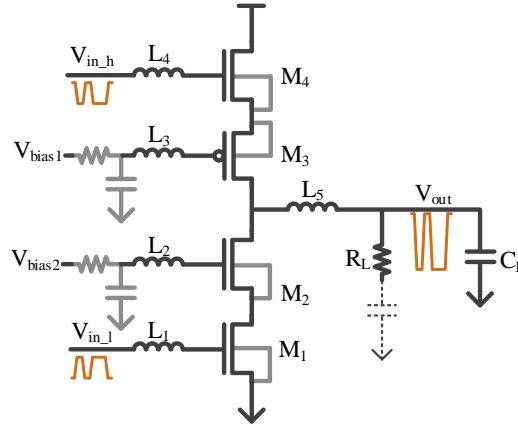


FIGURE 3.10: N over N cascode amplifier with inductor peaking bandwidth enhancement

Fig.3.11 shows the small signal model of the proposed circuit with five inductors. The model is very similar to the previous one but some capacitance has been split to within and without inductive peaking.

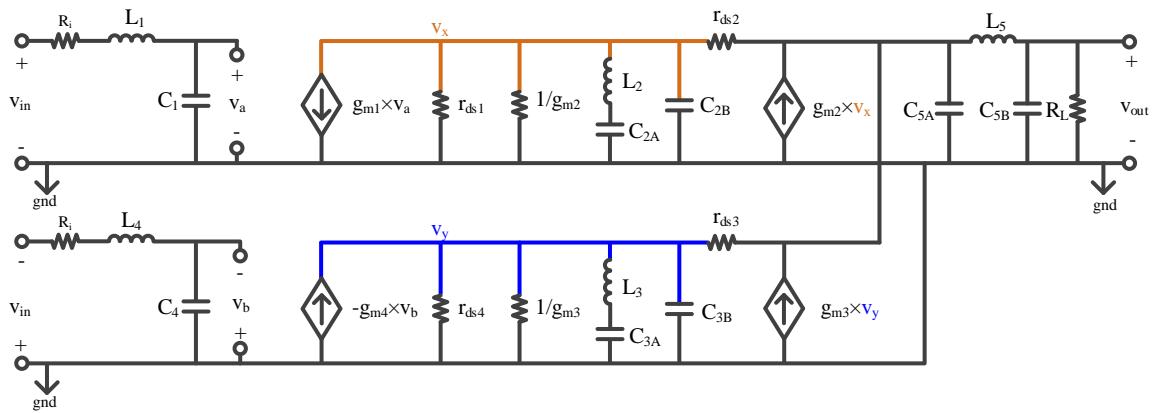


FIGURE 3.11: Small signal model of N over N cascode amplifier with inductive peaking

With inductors the capacitances  $C_2$ ,  $C_3$  and  $C_5$  are split into,

$$C_2 \quad \begin{cases} C_{2A} = C_{gd1} \cdot (1 + \frac{v_x}{v_a}) + C_{gs2} \cong 2 \times C_{gd1} + C_{gs2} \\ C_{2B} = C_{ds1} \end{cases} \quad (3.21)$$

$$C_3 \quad \begin{cases} C_{3A} = C_{gd4} \cdot (1 - \frac{v_x}{v_a}) + C_{gs3} \cong C_{gs3} \\ C_{3B} = C_{ds4} \end{cases} \quad (3.22)$$

$$C_5 \quad \begin{cases} C_{5A} = C_{gd2} + C_{gd3} + C_{ds2} \cdot (\frac{v_{out}}{v_x} - 1) + C_{ds3} \cdot (\frac{v_{out}}{v_y} - 1) \\ \cong C_{gd2} + C_{gd3} + C_{ds2} + C_{ds3} \\ C_{5B} = C_L \end{cases} \quad (3.23)$$

Since the small signal model transfer function is too complex, the transfer function analysis is too difficult to be expanded here. To simplify the inductive peaking bandwidth enhancement analysis, these five inductors could be classified as two types of bandwidth enhancement methods,

$L_1, L_4$  &  $L_5$

Bandwidth enhancement based on serial inductive peaking on loading capacitance.

$L_2$  &  $L_3$

Inductor in a RCL bias network on cascode transistor gate to enhance high frequency performance on common gate amplifier (cascode transistor)

The first type of bandwidth enhancement is presented in Fig.3.12. In case of  $L_1$  and  $L_4$  (inductors on inputs of proposed circuit), the 'Amp' in the figure could be regulated to the pre-amplifier for the output stage. Input resistance (in previous analysis,  $R_i$ ) could be regarded as pre-driver output impedance. And in the case of  $L_5$ , the proposed circuit output impedance can be regulated as  $r_o$  in the figure. Therefore, a simplified model of these three inductive peaking is created as shown in the right part of Fig.3.12.

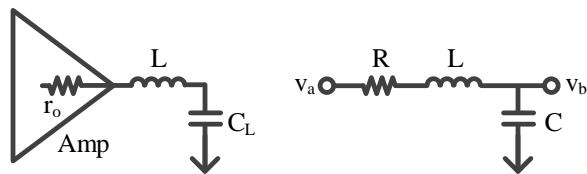


FIGURE 3.12: Bandwidth enhancement based on serial inductive peaking on loading capacitance

For instance, from  $v_a$  to  $v_b$ , the transfer function is yielded as below,

$$\frac{v_b(s)}{v_a(s)} = -\frac{1}{1 + CRs + LCS^2} \quad (3.24)$$

Compared with a similar model without the inductor peaking, the single pole on  $-1/RC$  is transferred to two complex poles. Therefore the bandwidth boost comes entirely from peaking provided by complex poles and there are no zeroes to help things along. For

the sake of bandwidth enhancement, the inductor serial peaking used is given by[114],

$$L = \frac{R^2 C}{m} \quad (3.25)$$

Where  $m=2$  corresponds to the maximum bandwidth enhancement and flat amplitude. And where  $m=3$  leads to a maximum flat group delay and bandwidth boost factor of about 1.36.[114] Generally, to balance the low quality of on-chip integrated custom inductor and maximum bandwidth enhancement, the factor  $m$  may be less than 2. But it should not be too close to 1 or even less than 1. It leads to a large peak on group delay and amplitude shaking.

For a simple example, assume a load of  $C = 200fF$  and  $R = 50\Omega$ , and assume factor  $m = 2$ . It yields the  $L = 250pH$ .

Fig.3.13 presents the result of the assumed example with and without inductive peaking. Compared with the non-inductor model, the bandwidth is enhanced from  $15.9GHz$  to  $22.5GHz$ . And due to the doubled number of poles, phase with inductor ends on  $-180^\circ$  but  $-90^\circ$ (it also shows Pole 1 and 2 are very close). In the Nyquist diagram, it is clear that the curve has invaded the negative half and convergence is back to '0' based on the complex poles system. In the transient analysis, the amplitude peaking of the signal is small which not leads to signal shake. Therefore, with proper parameter of inductors on load capacitance is enhancing the bandwidth.

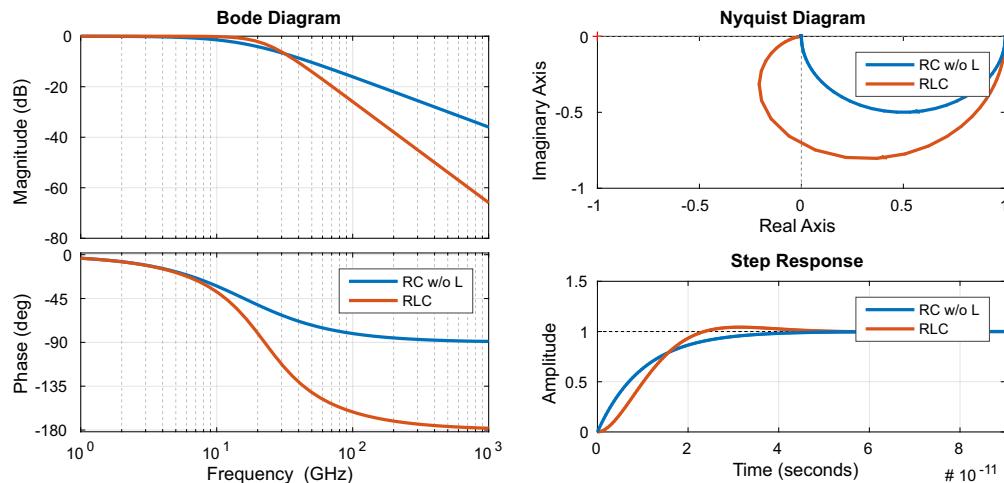


FIGURE 3.13: Bandwidth enhancement based on serial inductive peaking on loading capacitance

In the proposed circuit, the  $L_1$ ,  $L_4$  and  $L_5$  is creating peaks via the complex poles. The complex poles is enabling to move the  $\omega_0$  due to  $C_1$ ,  $C_4$  and  $C_{5B}$  into higher frequency.

The second kind of bandwidth enhancement is the inductor in an RCL bias network on a cascode transistor gate. [50] and [133] also uses a similar method to enhance the bandwidth of common gate amplifiers.

As an example, Fig.3.14 presents the pull down network with an inductor in an RCL network which biases the cascode transistor. The methodology of improvement on the pull up network in the proposed circuit is the same as the pull down one but the cascode transistor is a PMOS.

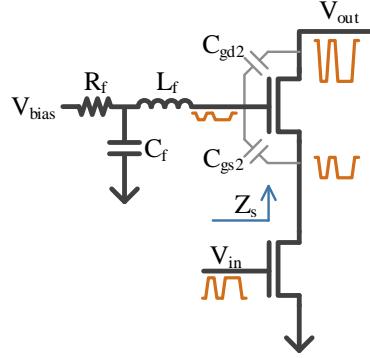


FIGURE 3.14: Cascode transistor is biased by reference voltage through a RCL network

Assuming the cascode transistor is directly biased by  $V_{bias}$  through the inductor, which is the equivalent to the AC ground on gate, and input impedance at the source of the cascode transistor is given by[50],

$$Z_s = \frac{1}{g_m(1 + \frac{sC_{gs}}{g_m})} = \frac{1}{g_m(1 + \frac{s}{\omega_T})} \quad (3.26)$$

Where the  $\omega_T$  is the unit current gain cut off frequency.

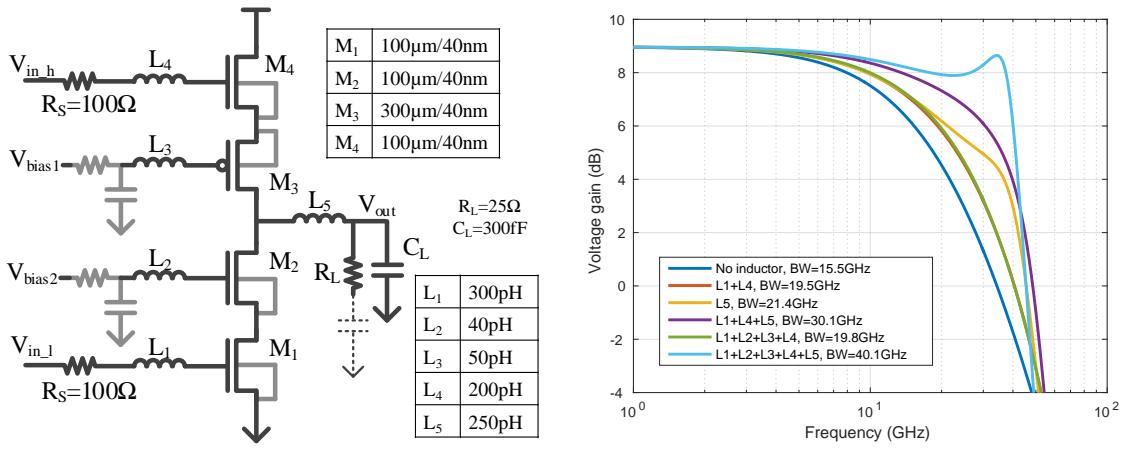
With the insertion of the inductor, an AC coupling from source to the gate of the cascode transistor appeared. The impedance of this network is  $Z_g = R + sL + 1/sC$ . In [50], after insertion of inductor, the input impedance at source of cascode transistor is,

$$Z_s \cong \frac{1}{g_m} \left( \frac{1 + sR(C_{gs2} + C) + s^2L(C_{gs2} + C)}{1 + sLC + s^2RC} \right) \times \left( \frac{1}{1 + \frac{s}{\omega_T}} \right) \quad (3.27)$$

The inductor creates peaking at a high frequency band due to an additional two zeroes. It extends the bandwidth of cascode transistors as common gate amplifiers.

Fig.3.15(a) presents an example of a proposed circuit design case with bandwidth enhancement inductor peaking. This amplifier loads up  $300fF$  and AC  $25\Omega$ . The dual inputs of proposed circuit are individual and load a serial  $100\Omega$  input impedance. With different inductor peaking mechanisms (Fig.3.15(b)), the bandwidth of the proposed circuit bandwidth is enhanced from  $15.5GHz$  (no inductor) to  $40.1GHz$  (five inductors). Overall, with the five inductor version, the inductive peaking bandwidth boost factor is over 2.5.

In this design example, all inductors are ideal devices. Within implementation, the quality (Q factor) of the custom inductor is much worse than them. Thus, in imple-



(a) The proposed circuit parameter and test environment (b) Simulated frequency response of proposed circuit with different inductor peaking mechanism

FIGURE 3.15: An example of inductive peaking bandwidth enhancement on N over N cascode amplifier

mentation, the bandwidth boost factor is going to be much lower than this theoretical analysis case. This design example, strives to enhance the bandwidth as much as possible but meanwhile the group delay is neglected. In the implementation, the bandwidth enhancement with inductor peaking should be used in a limited amount, otherwise, the jitter will lead to shaking on the amplifying signal.

### 3.7 Proposed circuit with a CML pre-stage

In previous sections, the functionality and performance of an N over N cascode amplifier has been analyzed. In this section, Dr. Ke Li creates a CML pre-stage improvement put forward, based on the proposed circuit.

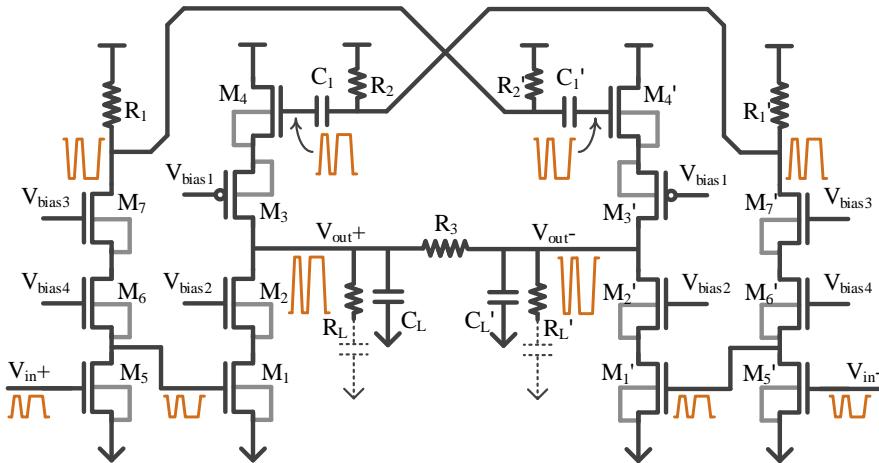


FIGURE 3.16: N over N cascode amplifier with a CML pre-stage

In Fig.3.16, both high and low level of inputs are generated by the CML driver, not two independent pre-drivers. With high voltage swing for  $M4$  and low voltage swing for  $M1$ , the source follower gain is less than 1 could be compensated. Therefore, in the proposed circuit with the CML pre-driver,  $M1$  is not limited by the unbalanced gain from  $M4$  and the output voltage swing could be enhanced.

However the CML pre-stage for the proposed circuit is compromising on power consumption. This approach requires the CML pre-stage to be working under  $V_{Reg}$  which is much higher power consumption than two pre-stage amplifiers which are working under  $V_{dd}$ .

Overall, the proposed circuit with a CML pre-stage benefits on increasing the output voltage swing and compact the design. But the defect of this approach is power consumption. The original topology and this approach should be chosen with different design requirements.

### 3.8 Summary

This chapter illustrates and analyzes the novel output stage of the modulator driver. Some enhancement method and improvements are also applied to N-over-N cascode push-pull amplifier. This circuit topology has an advantage in terms of overall performance regarding a wide application range and it is suitable for compact integration as well.

In Ch.4, three implementations are based on this topology. With 130nm and 40nm CMOS processes, three design in order proved the circuit functionality, bandwidth enhancement method with inductor peaking and CML pre-stage approach.



# Chapter 4

## Implementation of N over N cascode push pull modulator driver

Three implementations demonstrates the modulator driver with N-over-N cascode push-pull as the output stage in this chapter. These three designs are all based on the theoretical analysis in Ch.[3](#).

The 1st implementation is an inductor-less on N-over-N cascode push-pull amplifier design. The 2nd and 3rd design are on order to improved the inductor less proposed circuit with optimization methods in Sec.[3.6](#) and Sec.[3.7](#).

### 4.1 Introduction

In this chapter, there are three modulator driver implementations based on N-over-N cascode push-pull amplifier as the output stage.

The 1st implementation is demonstrated with IBM 130nm CMOS process and the rest two are designed with TSMC 40nm CMOS process.

These three implementations also gradually improve the performance of the modulator driver. The data rate of the modulator driver increases from 20Gb/s to 40Gb/s, and the output stage power efficiency is optimized from 7.75pJ/b to 2.4pJ/b simultaneously.

The implementation 1 and 2 are also integrated with nominal  $50\Omega$  MZM to compose an optical transmitter.

## 4.2 Implementation I

### A basic N-over-N cascode modulator driver

In order to achieve a modulator driver with the proposed N-over-N cascode push-pull output stage, this design is presented with IBM 130nm CMOS process. This modulator driver is adaptable to nominal  $50\Omega$  push pull MZM. Modulator driver power consumption is 296mW, and it is 148mW on output stage. Mid-band AC gain is 44dB and output swing is over 1.7Vpp on the single end. The transmitting data rate is broadband until 20Gb/s.

After electric testing, this design is compact integrated to MZM in [115] to compose the optical transmitter. The optical transmitter is enabling 20Gb/s optical interconnection as well.

#### 4.2.1 Top level schematic of optical transmitter

The top level schematic of this optical transmitter is shown in Fig.4.1. The modulator driver is consists of two pre-amplifier gain stages, four pre-amplifier double fan-out stages and a pair of output stage with on-chip termination network. MZM is integrated with the modulator driver via bonding wires, and there is a pair of off-chip  $50\Omega$  AC termination networks after MZM.

On the modulator driver,  $Vdd$ ,  $Vdd\_Reg$ (regulated  $Vdd$ ) and  $Vss$  are the DC power supply of the chip. In this design, the pre-amplifier gain stage and pre-amplifier double fan-out stage are powered by  $Vdd = 1.6V$ . The output stage is powered by  $Vdd\_Reg = 3.3V$ . MZM shares the  $Vss$  as the reverse bias from the modulator driver. Therefore, the the reverse bias voltage of MZM is equal to the output DC bias of modulator driver to  $Vss$ . In this design it is  $1.65V$ .

#### 4.2.2 Pre-driver system

The pre-driver of the modulator driver consists of two groups of gain stage amplifier and four groups of double fan-out drivers. In Fig.4.2, the abstract and interconnection of the pre-driver is briefly explained.  $Vdd$  of pre-driver is 1.6V. The input of this pre-driver has to be a pair of differential signals, and the outputs are two pairs of amplified differential signals which are feeding into the output stage.

In this pre-driver, the gain stage amplifies the input signals until maximum voltage swing headroom, and the double fan-out stage buffers the amplified signals (nearly 0dB gain but double fan-out) to the output stage. The overall gain stage generates 35dB gain, and power consumption of this pre-driver is  $153mW$  ( $Vdd = 1.6V$ ).

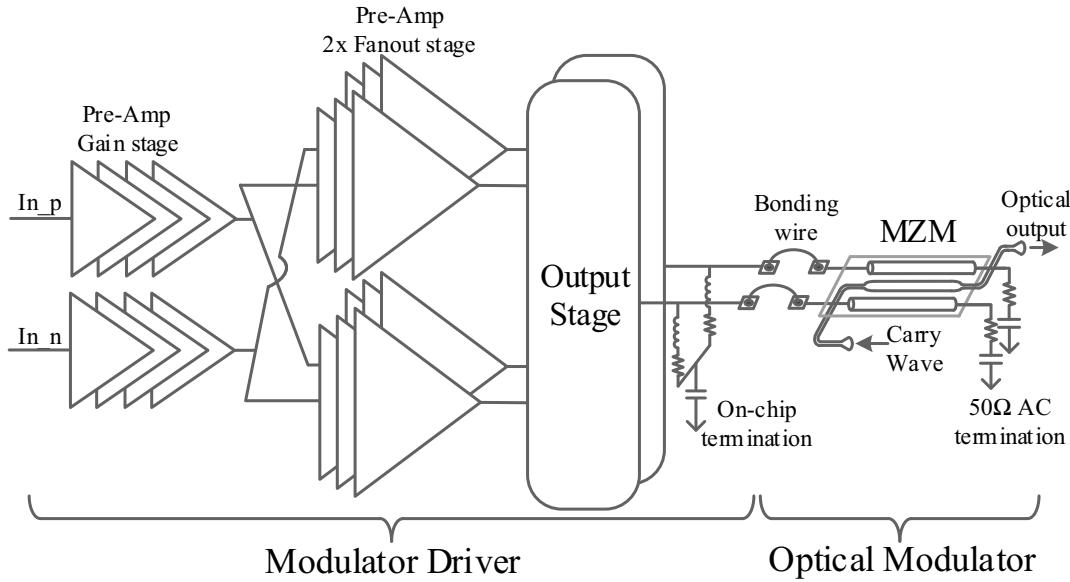


FIGURE 4.1: Top level schematic of optical transmitter

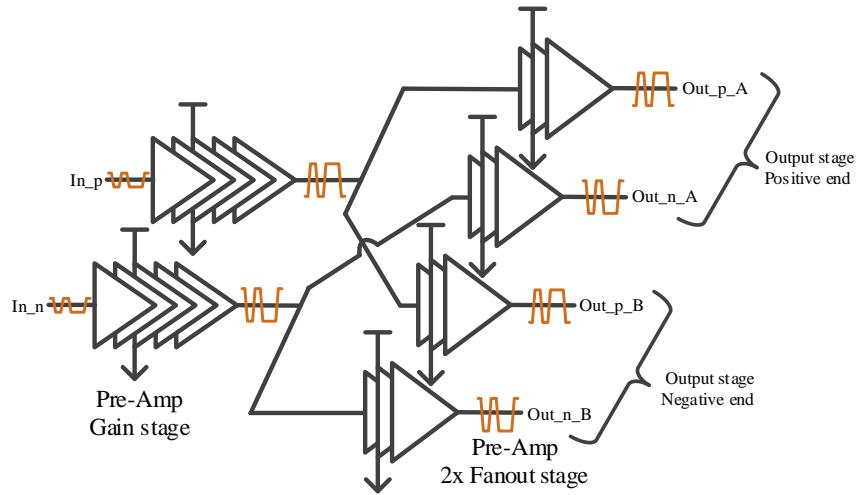


FIGURE 4.2: Pre-driver of modulator driver

### Pre-driver gain stage

The gain stages in the pre-driver are provided by a five stage cascade gain limiting amplifier. Circuit structure is common source amplifier with inductor peaking in Sec.2.5.1.

Fig.4.3 presents the schematic of this limiting amplifier, and its parameters are presented in Table4.1.

In order to archive the input impedance matching, there is a  $50\Omega$  input impedance matching network before the DC block capacitor. An inductor is added into this network. Overall impedance of  $L_{in}$  and  $R_{in}$  is  $50\Omega$  which is covering the pass band until 22GHz.

This amplifier is self DC biased by  $C_{bias}$  and  $R_{bias}$ . The first four stages are standard gain stage. Voltage gain is 2 on each stage, and bandwidth is from DC to 19GHz. DC

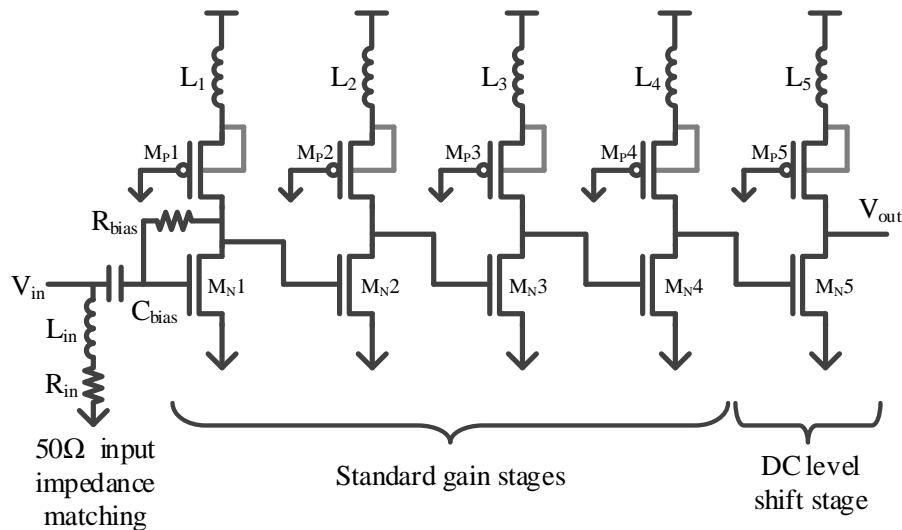


FIGURE 4.3: Schematic of pre-driver gain stage

TABLE 4.1: Parameters of major components in gain stage of pre-driver			
$R_{in}$	47.6Ω	$W/L_{P1} - P4$	$18.3\mu m/0.12\mu m$
$L_{in}$	$L = 225pH(R = 2.7\Omega)$	$W/L_{P5}$	$20.2\mu m/0.12\mu m$
$R_{bias}/C_{bias}$	$61k\Omega/1.82pF$	$W/L_{N1} - N5$	$12\mu m/0.12\mu m$
$L_1 - L_4$	$L = 1.65nH(R = 30.5\Omega)$		
$L_5$	$L = 1.79nH(R = 27.8\Omega)$		

bias of these four stages is 840mV. Power consumption on each stage is 3.9mW at a 20Gb/s data rate. In order to meet the input specification of the double fan-out limiting amplifier, the last stage of cascade gain limiting amplifier shifts the output DC bias from 840mV to 1.05V. Power consumption on this stage is 4.5mW at a 20Gb/s data rate.

The overall gain of the cascade gain limiting amplifier is over 30dB. Power consumption is 20mW at a 20Gb/s data rate. Bandwidth is over 14GHz.

### Pre-driver double fan-out stage

The 2x fan-out stage of pre-driver consists of three stages of NMOS common source amplifiers with doubled the transistor size.

Fig.4.4 presents the schematic of this amplifier and the parameters of the major components are presented in Table4.2.

TABLE 4.2: Parameters of major components in double fan-out stage

$L_6$	$L = 1.05nH(R = 18.1\Omega)$	$W/L_{P6}$	$24\mu m/0.12\mu m$
$L_7$	$L = 380pH(R = 5.3\Omega)$	$W/L_{P7}$	$54\mu m/0.12\mu m$
$L_8$	$L = 225pH(R = 2.7\Omega)$	$W/L_{P8}$	$91.8\mu m/0.12\mu m$
		$W/L_{N6}$	$12\mu m/0.12\mu m$
		$W/L_{N7}$	$24\mu m/0.12\mu m$
		$W/L_{N8}$	$48\mu m/0.12\mu m$

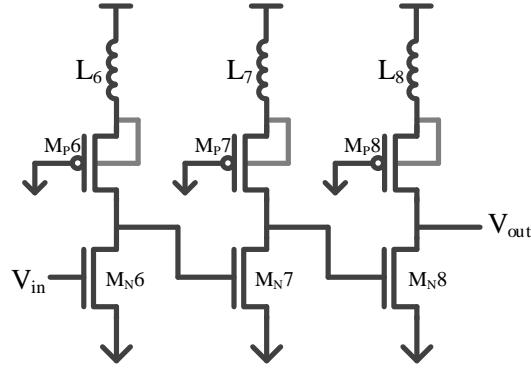


FIGURE 4.4: Schematic of pre-driver double fan-out stage

The input and output DC bias of the first two stages is 1.05V. The last stage output DC bias is moved to 850mV to achieve the maximum voltage swing for the output stage. The power consumption of these three stages, in order, is 4.8mW, 9.2mW and 18.6mw.

The overall power consumption of the 2x fan-out stage in the pre-driver is 31.5mW at a 20Gb/s data rate. The gain of the 2x fan-out stage is 2.1 and bandwidth is 16.5GHz.

#### 4.2.3 Output stage of modulator driver

The modulator output stage is the proposed N-over-N cascode push pull structure. The schematic is shown in Fig.4.5 and the parameters of the circuit is presented in Table4.3.

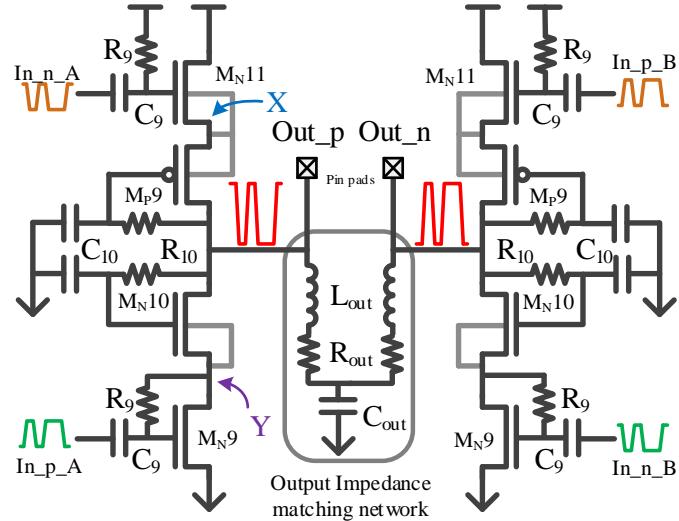


FIGURE 4.5: Schematic of Output stage of modulator driver

DC operating point on gates of  $M_{N9}$  and  $M_{N11}$  are re-biased via  $R_9$  and  $C_9$ .  $M_{N10}$  and  $M_{P9}$  are cascode transistors. The gates of these two transistors are biased by low pass networks which are both composed of  $R_{10}$  and  $C_{10}$ . The DC operating point on gates is the same as the output.

TABLE 4.3: Parameters of major components in output stage			
$L_{out}$	$L = 1.42nH(R = 9.1\Omega)$	$W/L_{N9}$	$90\mu m/0.12\mu m$
$R_{out}/C_{out}$	$82.1\Omega/25pF$	$W/L_{N10}$	$150\mu m/0.12\mu m$
$R_9/C_9$	$95k\Omega/3.2pF$	$W/L_{N11}$	$150\mu m/0.12\mu m$
$R_{10}/C_{10}$	$42k\Omega/0.8pF$	$W/L_{P9}$	$150\mu m/0.12\mu m$

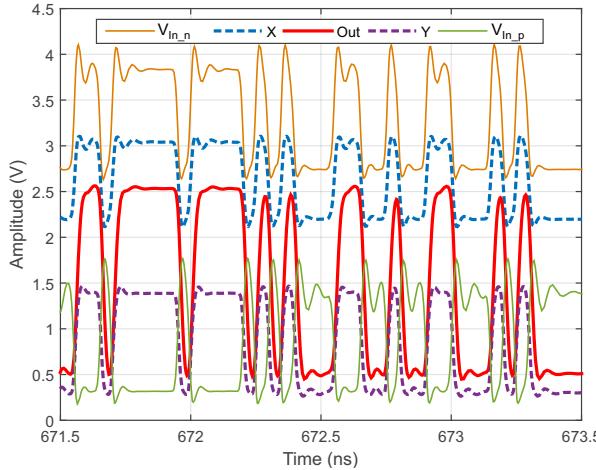


FIGURE 4.6: Transient signal on different nets in output stage

Fig.4.6 is a transient simulation which explains the signals on different nets in the output stage( $V_{In_n}$  and  $V_{In_p}$  are actually the signal past  $C9$ . They are the signal on the gate of  $M_{N9}$  and  $M_{N11}$ ). The regulated power supply ( $Vdd\_reg$ ) is 3.3V at this stage. The voltage  $V_{gd}$  of  $M_{N11}$  varies in the range  $\pm 0.8V$ . The signal on the gate and source (net X) of  $M_{N11}$  are in the same phase.  $V_{gs}$  and  $V_{ds}$  are also less than 1.6V regarding data transmission. Therefore, the voltage differences between the nodes on this transistor ( $M_{N11}$ ) are always less than the break-down voltage ( $V_{break\_down} = 1.6V$  in this CMOS process).

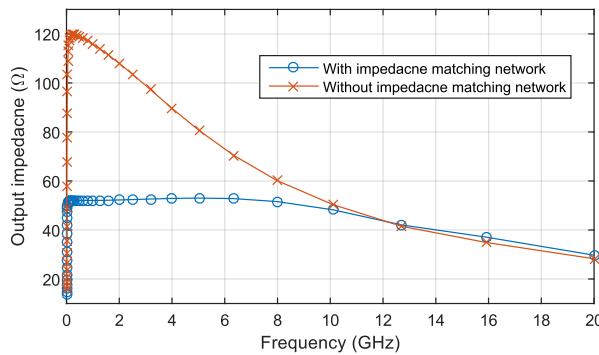


FIGURE 4.7: Output stage impedance matching network

This output stage is an inductor-less design. The  $L_{out}$  is used for output impedance matching. To achieve  $50\Omega$  output impedance matching, a differential impedance matching network is placed between the outputs of the modulator driver. In Fig.4.7, the output impedance with and without impedance matching network on the modulator driver is

compared. With this impedance matching network, the output impedance is reduced from  $120\Omega$  to  $50\Omega$  in the mid-band frequency range. The additional inductor creates a small peak around cut-off frequency. The enhanced output impedance is  $50 \pm 3\Omega$  until 11GHz.

The Bandwidth of the output stage is over 10GHz. The mid-band gain is 7.1dB. The overall power consumption (differential) is 155mW.

#### 4.2.4 Modulator driver layout

In Fig.4.8, it is the layout of this proposed modulator driver design and microscope view of the fabricated chip. DC pads, signal pads and circuit blocks are labeled in the layout. In the layout figure (Fig.4.8(a)), DC pads (Vdd, Vdd\_Reg and Vss) are large pads on the top and bottom. Input signal pads are on the left. Output signal pads are on the right. Signal pads are made in the order of 'gnd!', 'signal+', 'gnd!', 'signal-', 'gnd!'. Pitch of the signal pads are 0.1mm.

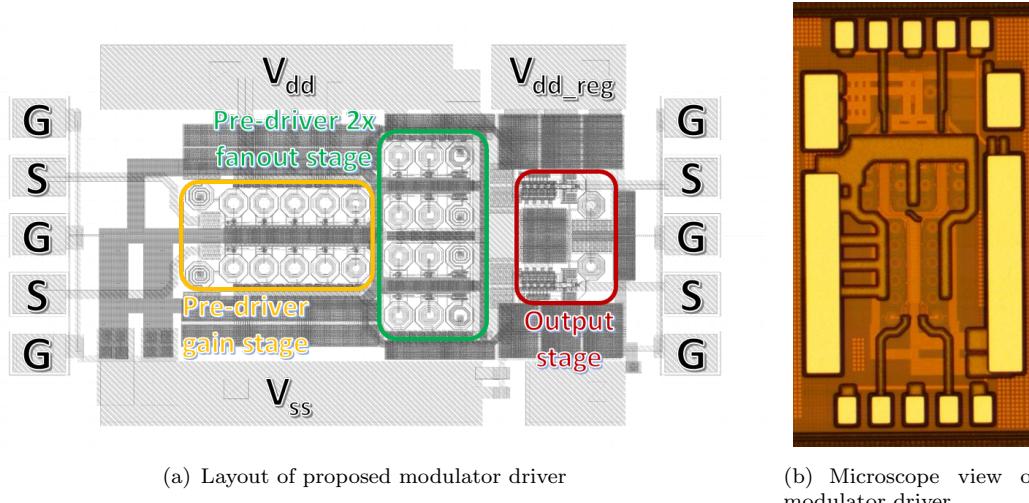


FIGURE 4.8: Layout and microscope view of modulator driver design

Chip size (including all pads) is  $600\mu m \times 1250\mu m = 750000\mu m^2 = 0.75mm^2$ . The active area of the output stage is only  $0.1mm^2$ .

#### 4.2.5 Simulation result

This modulator driver is a differential-in differential-out amplifier and input and output impedance of the driver is single end  $50\Omega$  on the pass band. S-parameter simulation test-bench is shown in Fig.4.9. In this test-bench, two S-parameter ports are connected to the differential input and output. These two ports include  $100\Omega$  impedance on the differential end (equivalent single end  $50\Omega$ ).

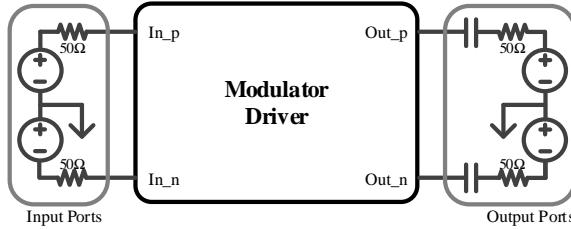


FIGURE 4.9: Modulator driver S-parameter test bench

The group delay from port1 to port2 is plotted in Fig.4.10(a). It is flat in the mid-band and increasing into 30ps while it closes to the cut off frequency. Fig.4.10(b) is the input and output impedance of the modulator driver. Input impedance is  $50 \pm 2.5\Omega$  in the broadband. Output impedance is  $50 \pm 3\Omega$  until 11GHz.

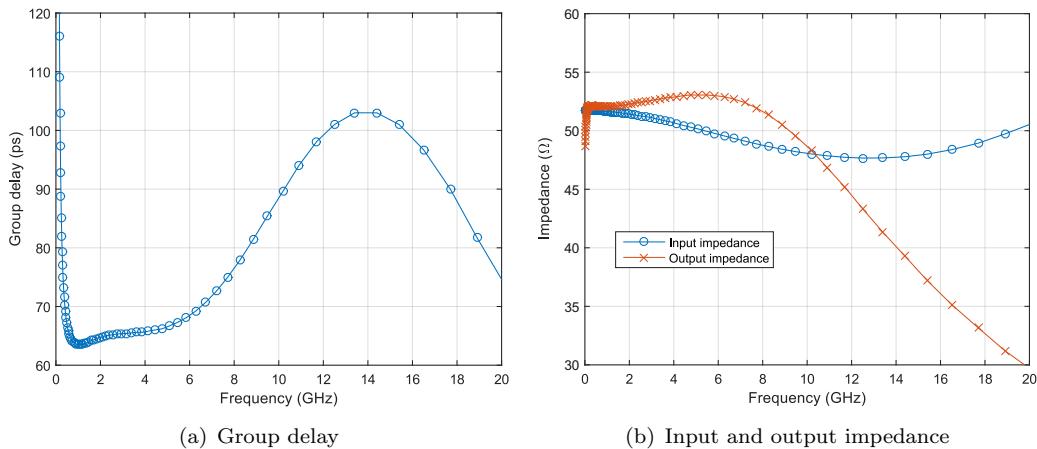


FIGURE 4.10: Group delay and impedance characteristic of modulator driver

The S-parameter characteristic is plotted in Fig.4.11. In the pass band, S11 is less than -20dB and S12 is less than -150dB. S21 demonstrates that the gain of the modulator driver is 44dB in the mid-band and bandwidth is 17GHz. Until the cutoff frequency, S22 of this modulator driver is less than -4dB.

Transient simulation is based on a pair of differential 200mV pseudo random binary sequence(PRBS) NRZ data as input. Output is loading a pair of 50Ω AC termination and 150fF capacitors. The loaded capacitor is similar or equivalent to the electrode attenuation on MZM. Transient simulation results is presented as eye-diagrams in Fig.4.12.

In this simulation, 10Gb/s and 20Gb/s PRBS NRZ are both applied to the modulator driver. Eye-diagrams show both results on differential and positive ends. Differential output voltage swing is over 3.8Vpp, and the single end is 1.9Vpp. Due to group delay increases after 10GHz, the jitter is going to keep increasing while the data rate is over 20Gb/s. Therefore, data rate of this modulator driver is 20Gb/s or below.

The power consumption of  $Vdd = 1.6V$  and  $Vdd\_Reg = 3.3V$  in the 20Gb/s transient

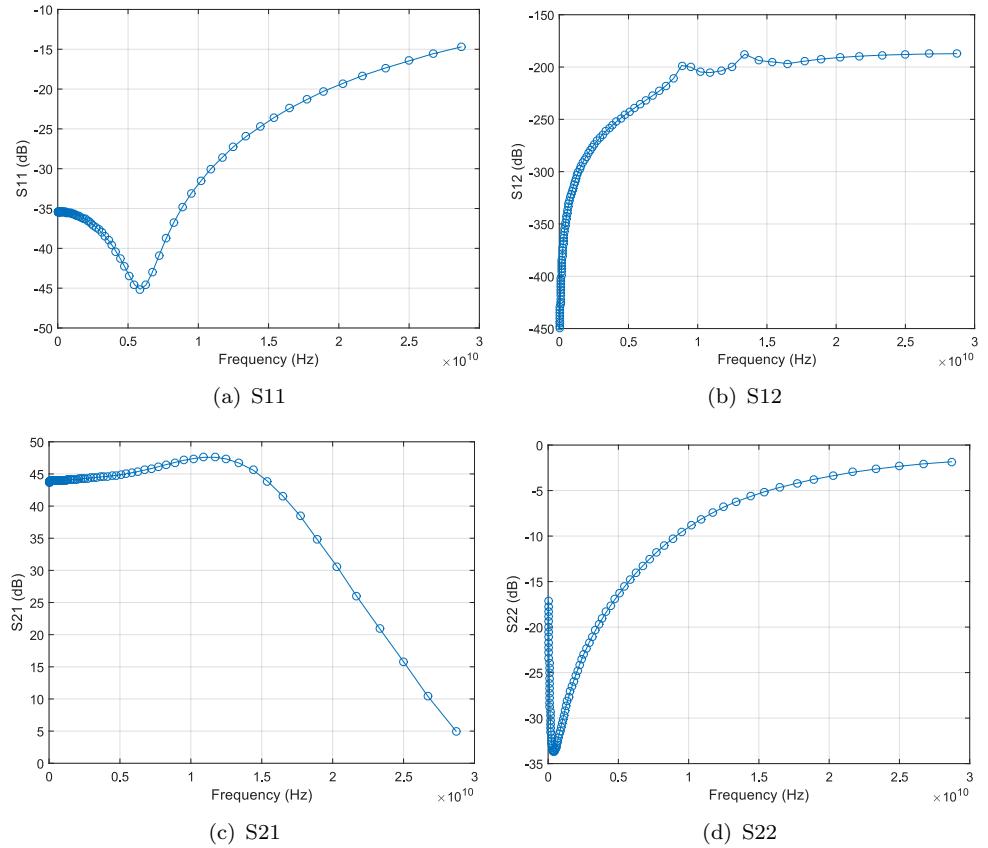


FIGURE 4.11: S-parameter result of modulator driver

simulation is observed,

$$\begin{aligned} Vdd &= 1.6V, \quad Idd_{rms} = 111mA. \\ Vdd\_Reg &= 3.3V, \quad Idd\_Reg_{rms} = 47mA. \end{aligned}$$

Therefore, power consumption of modulator driver with 20Gb/s data rate transmission is,

$$\begin{aligned} P_{full\ chip} &= \overbrace{Vdd \times Idd_{rms}}^{\text{Pre-driver}} + \overbrace{Vdd\_Reg \times Idd\_Reg_{rms}}^{\text{Output stage}} \\ &= 1.6V \times 111mA + 3.3V \times 47mA \\ &= 331mW \quad (20Gb/s\ datarate) \end{aligned}$$

In this simulation result, the full modulator driver

$$\begin{aligned} FOM &= P_{full\ chip}/\text{datarate} \\ &= 331mW/20Gb/s \\ &= 16.55pJ/bit \end{aligned}$$

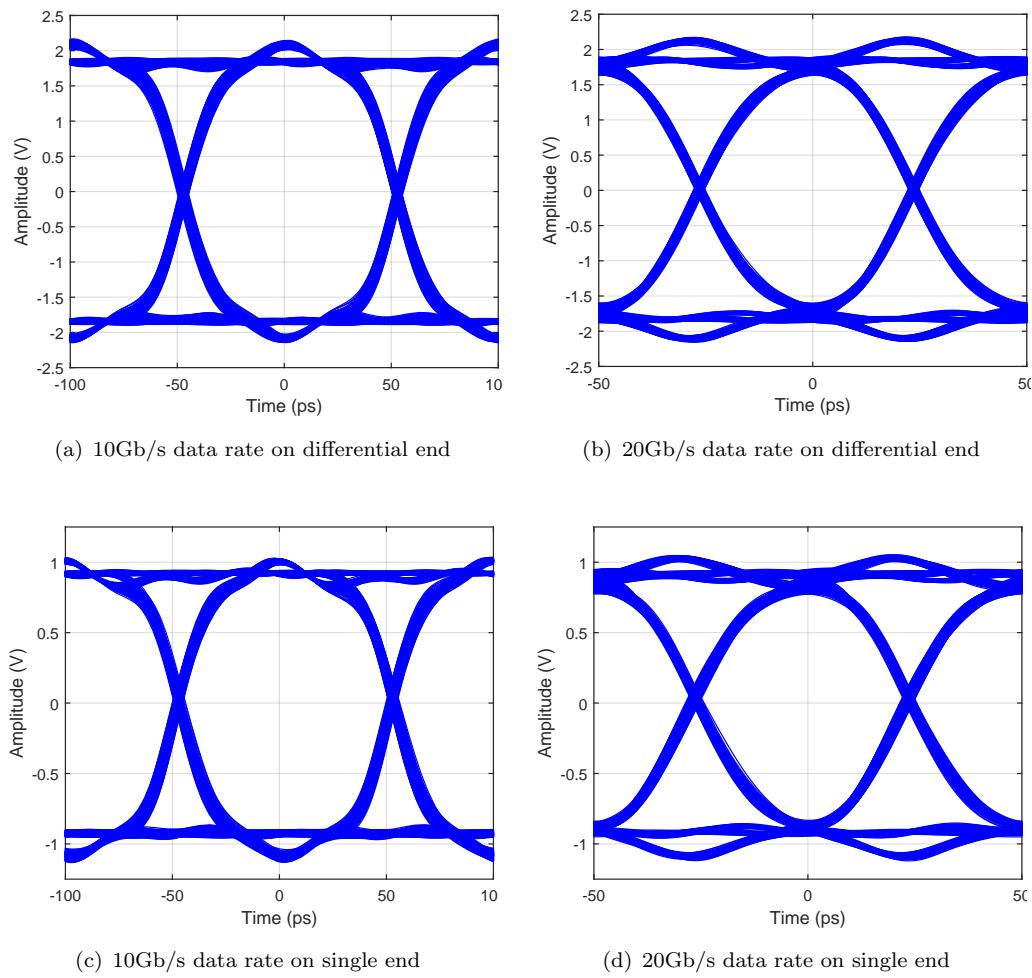


FIGURE 4.12: Transient simulation result of modulator driver

and the output stage of the modulator driver

$$\begin{aligned}
 FOM &= P_{\text{output stage}}/\text{datarate} \\
 &= 155\text{mW}/20\text{Gb/s} \\
 &= 7.75\text{pJ/bit}
 \end{aligned}$$

The previous simulation results are based on tt corner of the process and temperature is set as  $27^\circ\text{C}$ . More specific simulation conditions and an simulation example are presented in App. A.

#### 4.2.6 Testing result

The initial testing results are electrical test of the modulator driver where the input signal is a pair of  $2^{15} - 1$  differential NRZ PRBS signal. The PRBS signal is delivered to the driver via coaxial cables and a RF probe. The modulator driver is blooming

on PCB. DC pads are connected to PCB pads with bonding wires. DC power is also supplied via the custom designed PCB circuit. The output of the driver is fed into a digital communications analyzer (DCA) with  $50\Omega$  input impedance via a RF probe, DC block capacitor and coaxial cable.

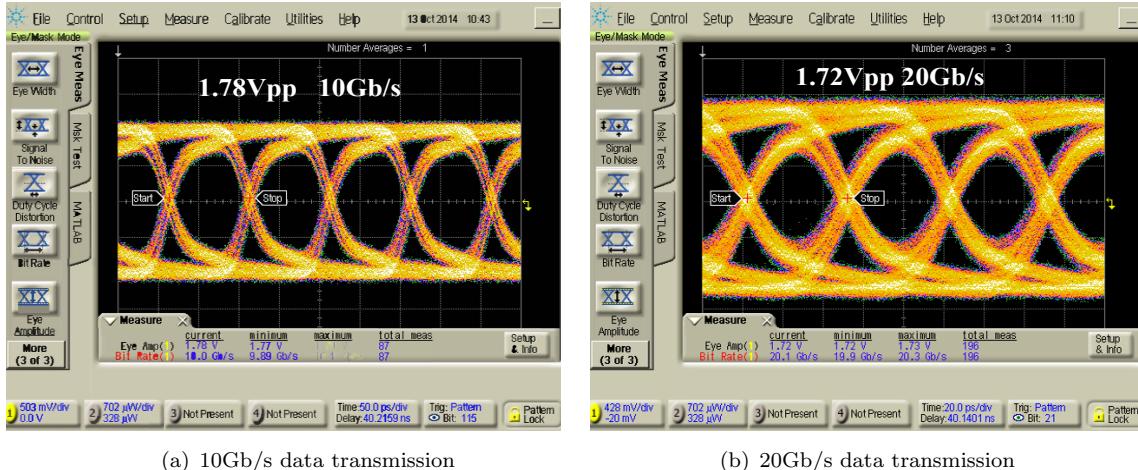


FIGURE 4.13: Modulator driver electric measurement result with  $2^{15-1}$  PRBS

DAC captured eye-diagram of modulator driver is shown in Fig.4.13. It, on the order, presents the modulator driver working on 10Gb/s and 20Gb/s. Single end amplitude is over 1.7V (1.79V at 10Gb/s and 1.72V at 20Gb/s). It can be surmised the differential output voltage swing should be 3.58V at 10Gb/s and 3.44V at 20Gb/s.

The power consumption in testing is

$$Vdd = 1.6V, \quad Idd = 103mA.$$

$$Vdd\_Reg = 3.3V, \quad Idd\_Reg = 45mA.$$

Power consumption (not including laser resource) of full design at 20Gb/s data rate transmission is

$$\begin{aligned} P_{\text{modulator driver}} &= \overbrace{Vdd \times Idd}^{\text{Pre-driver}} + \overbrace{Vdd\_Reg \times Idd\_Reg}^{\text{Output stage}} \\ &= 1.6V \times 103mA + 3.3V \times 45mA \\ &= 312mW \quad (20Gb/s \text{ datarate}) \end{aligned}$$

In the testing results, the

$$\begin{aligned} FOM &= P_{\text{modulator driver}} / \text{datarate} \\ &= 312mW / 20Gb/s \\ &= 15.6pJ/bit \end{aligned}$$

and the output stage of modulator driver

$$\begin{aligned}
 FOM &= P_{\text{output stage}}/\text{datarate} \\
 &= 148\text{mW}/20\text{Gb/s} \\
 &= 7.4\text{pJ/bit}
 \end{aligned}$$

In order to complete the optical transmitter, the modulator driver is integrated with MZM via bonding wires. The MZM is the 1mm long version from [116]. For more modulator efficiency and other specific characteristics, they can be found in the citation. Fig.4.14 presents the microscope view of the optical transmitter.

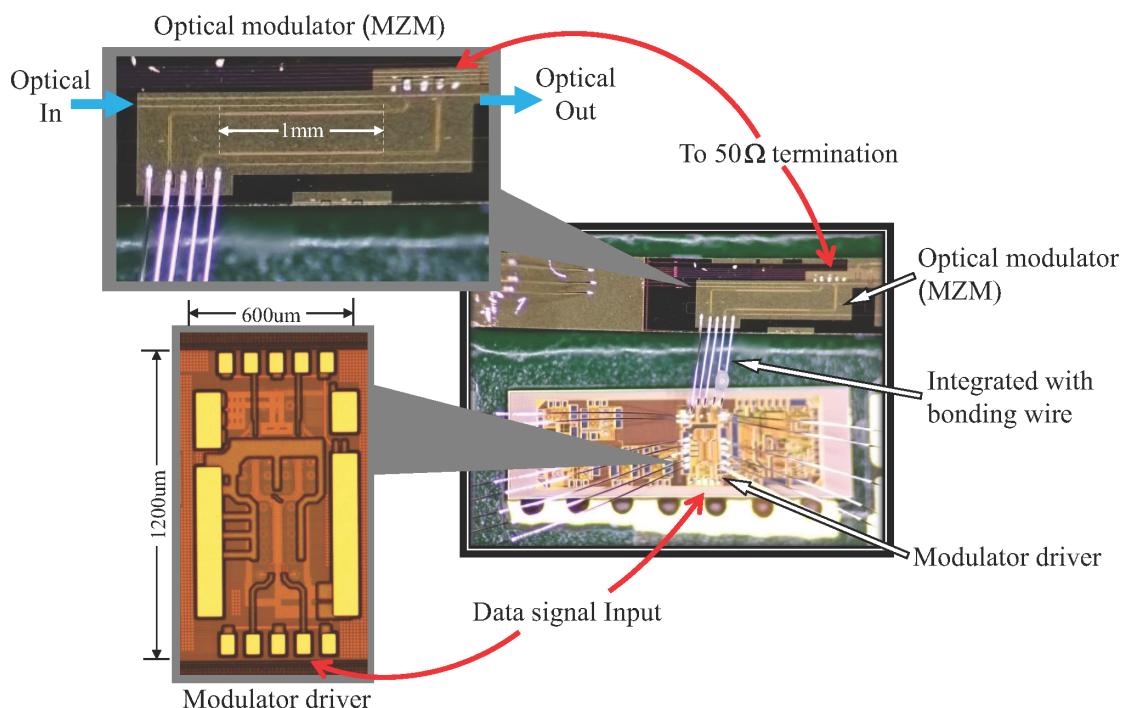


FIGURE 4.14: The optical transmitter

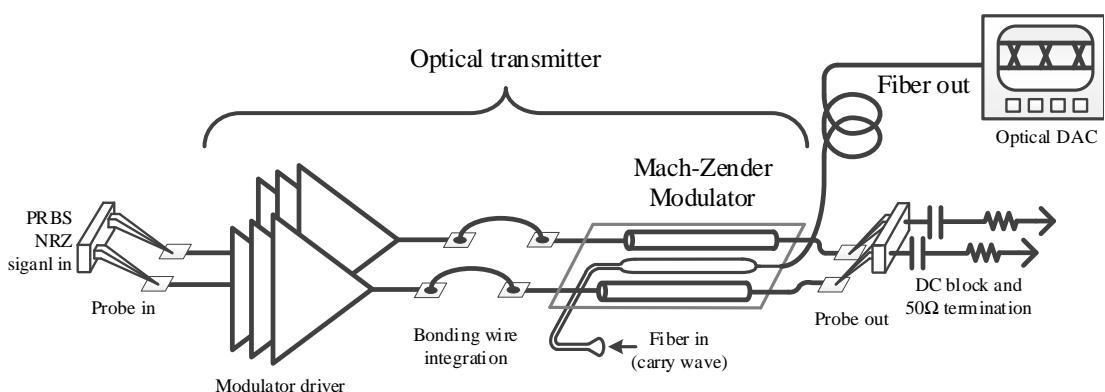


FIGURE 4.15: Testing hierarchy of the integrated optical modulator

An abstract view of the testing environment of this modulator is shown in Fig.4.15. The input signal of the modulator is generated by a  $2^{15-1}$  NRZ PRBS via a coaxial cable and a RF probe. A  $50\Omega$  AC termination after MZM is provided via a RF probe. Light is coupled to and from the MZM by optical fibers. The optical output of the modulator is connected to an optical digital communications analyzer via fiber and an Erbium-Doped Fiber Amplifier (EDFA).

The optical modulator is an unbalanced MZM, and the testing result is based on the -3dB (quadrature point) from the lowest insertion loss band (in this testing case,  $\lambda = 1570nm$  is been selected).

The optical testing result is shown in Fig.4.16. A 20Gb/s NRZ data is transmitted and modulated from the electrical signal to the optical signal. Power on logic "1" level is 2.31mW and logic "0" level is 0.79mW.

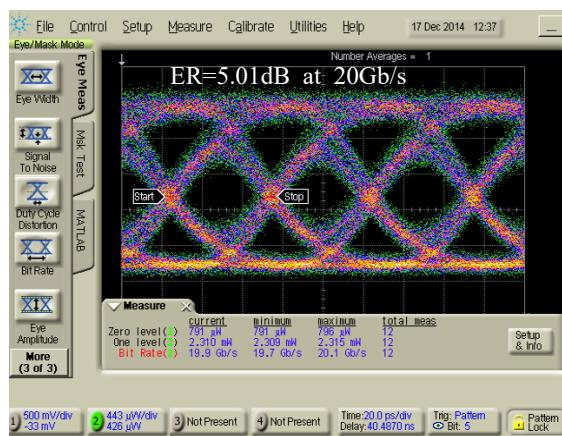


FIGURE 4.16: Optical measurement of optical modulator with  $2^{15-1}$  PRBS at 20Gb/s

The measured noise level of the measurement setup is around  $90\mu W$ . The optical extinction ratio is given by,

$$ER = 10 \log_{10} \frac{P(1) - NL}{P(0) - NL} = \frac{2.31mW - 0.09mW}{0.79W - 0.09mW} = 5.01dB.$$

### 4.3 Implementation II

#### N over N cascode modulator driver with inductor peaking

In this section, a modulator driver with the proposed N-over-N cascode amplifier as the output stage is demonstrated on TSMC 40nm CMOS process. Design in this section is an optimized version with inductive peaking.

This circuit is a differential modulator driver for MZM. Output impedance is differential  $100\Omega$  in the mid-band. The modulator driver power consumption is 143mW (output

stage 95.6mW). Mid-band AC gain is 20dB and the output swing is over 1.5V on the single end. The data rate is broadband until 40Gb/s (V<sub>pp</sub>=1.1V at 40Gb/s).

After the electric testing, two MZM are integrated with the modulator driver. One of them is a 1mm version MZM from [115], and the integrated optical transmitter is functional 30Gb/s optical signal modulating. The other MZM from [55], and it is functional up to 25Gb/s as well.

#### 4.3.1 Top-level schematic of optical transmitter

The top level schematic of the optical transmitter is similar to the previous design. The abstract of the optical transmitter is presented in Fig.4.17.

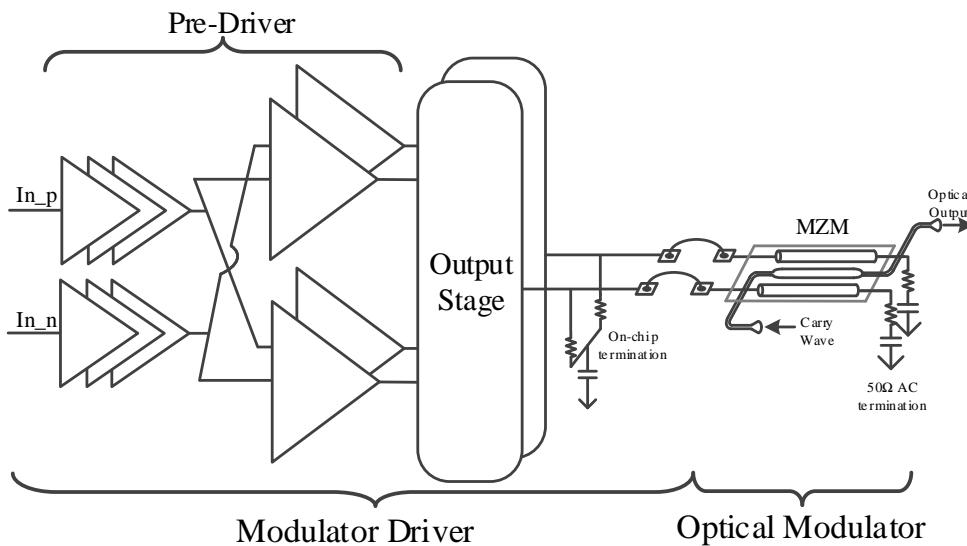


FIGURE 4.17: Top level schematic of optical transmitter

The pre-driver is powered by  $V_{dd} = 1.1V$  and the power supply of the output stage is adjustable from 2.5V to 3.3V (standard operates at 2.8V).

#### 4.3.2 Pre-driver of modulator driver

The pre-driver is designed as two rails of cascode amplifiers. Fig.4.18 is the abstract view of the two rails of the pre-driver and Fig.4.19 presents the schematic of one rail amplifier.

In order to archive the impedance matching, a  $50\Omega$  termination with an inductor peaking is located at the input of pre-driver. This inductor maintains the input impedance and is not declining in the high frequency band. After the termination, the signal is DC blocked and re-biased by self-biasing resistance. The first three limiting amplifier gain stages are an NMOS common source amplifier with PMOS and an inductor as the load.

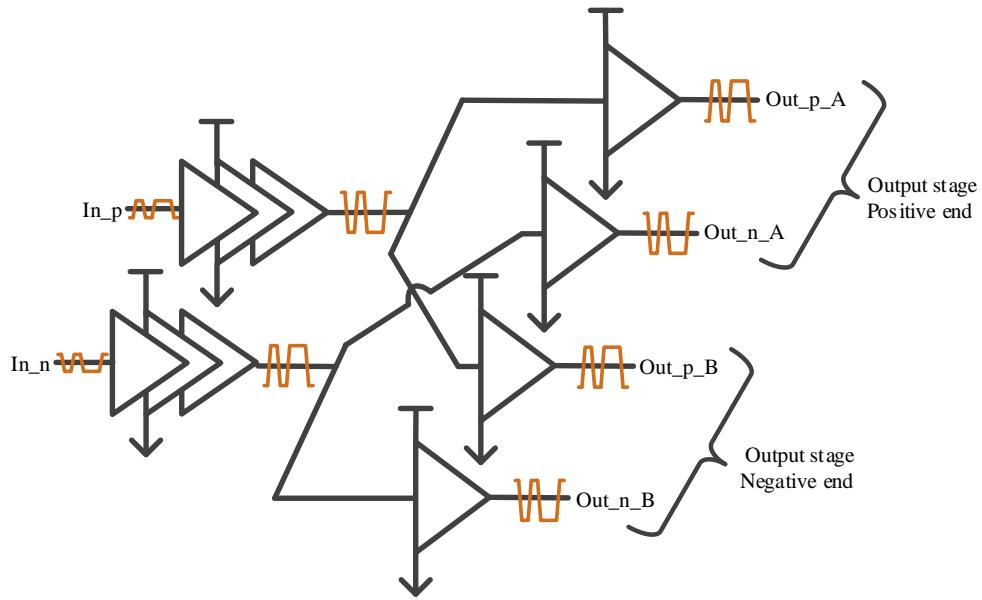


FIGURE 4.18: Abstract of pre-driver in modulator driver

The fourth stage pre-driver is two rails of independent common source amplifier after a serial inductor. Two rails of fourth stage are both unity gain with resistor and inductor loading.

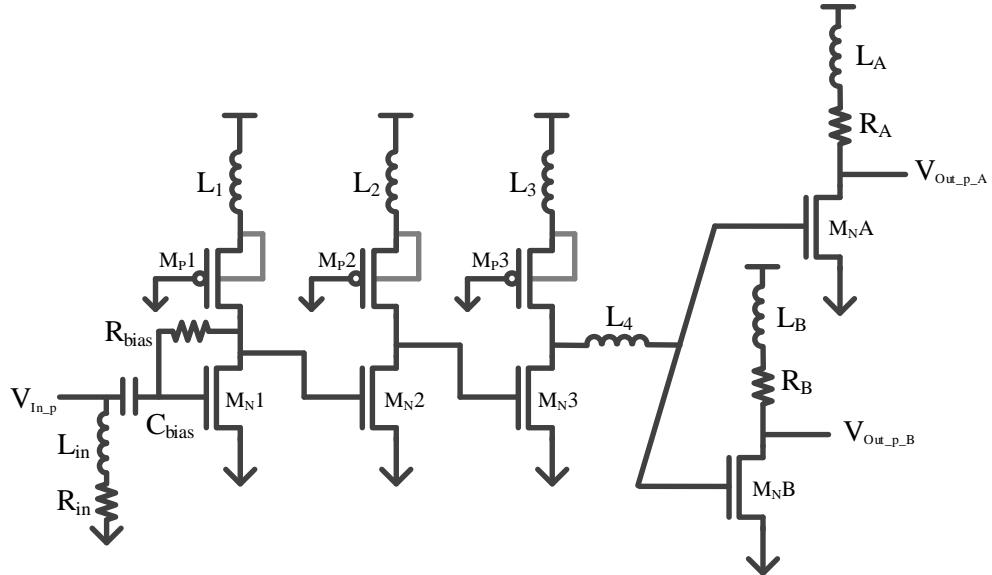


FIGURE 4.19: Schematic of pre-driver in modulator driver

The parameters of major components in pre-driver are listed in Table 4.4. The minor difference between  $L_A$  and  $L_B$  are designed for the the different input loadings of the output stage.

The mid-band gain of the pre-driver is over 20dB with 28GHz bandwidth. The power supply of the pre-driver stages are 1.1V. The power consumption in the simulation is

TABLE 4.4: Parameter of major components in pre-driver

$R_{in}$	$47.6\Omega$	$R_A$ & $R_B$	$42\Omega$
$L_{in}$	$L = 220pH(R = 5.4\Omega)$	$L_A$	$L = 441pH(R = 9.9\Omega)$
$R_{bias}/C_{bias}$	$42k\Omega/2.8pF$	$L_B$	$L = 352pH(R = 8.1\Omega)$
$L_{1-L_2}$	$L = 388pH(R = 8.1\Omega)$	$W/L_P 1 - P 3$	$28\mu m/40nm$
$L_3$	$L = 372pH(R = 10.7\Omega)$	$W/L_N 1 - N 3$	$24\mu m/40nm$
$L_4$	$L = 317pH(R = 7.5\Omega)$	$W/L_N A$ & $W/L_N B$	$36\mu m/40nm$

28mW for each rail, and 56mW of dual rails at a 40Gb/s data rate.

### 4.3.3 Output stage of modulator driver

The output stage schematic and parameters are specified in Fig.4.20 and Table4.5. The proposed circuit is a fully self-biased circuit.

To maintain the output impedance of differential  $100\Omega$ , there is a termination RC network between outputs.

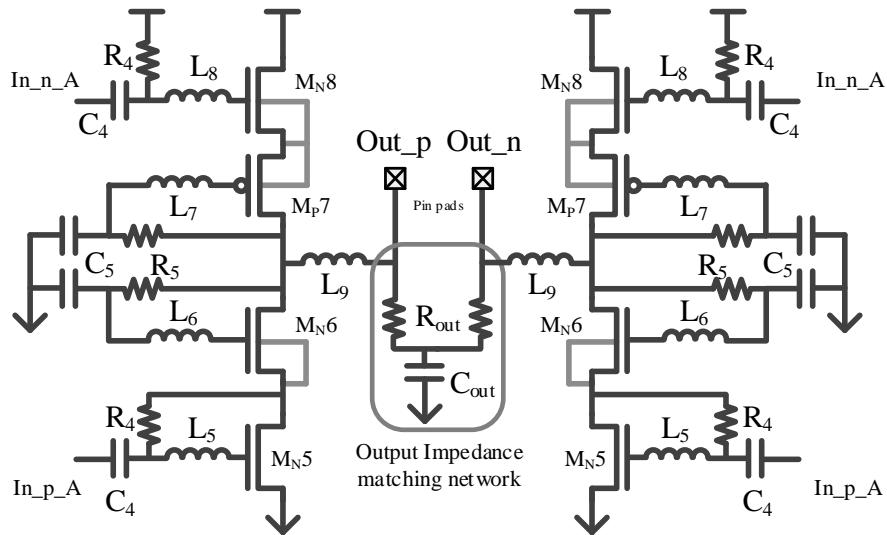


FIGURE 4.20: Schematic of output stage in modulator driver

TABLE 4.5: Parameter of major components in output stage

$R_4/C_4$	$45k\Omega/2.8pF$	$R_5/C_5$	$25k\Omega/1.15pF$
$R_{out}/C_{out}$	$192\Omega/4.3pF$	$L_9$	$L = 205pH(R = 2.3\Omega)$
$L_5$	$L = 317pH(R = 6.8\Omega)$	$W/L_N 5$	$100.8\mu m/40nm$
$L_6$	$L = 103pH(R = 2.0\Omega)$	$W/L_N 6$	$100.8\mu m/40nm$
$L_7$	$L = 69pH(R = 1.6\Omega)$	$W/L_P 7$	$230.4\mu m/40nm$
$L_8$	$L = 220pH(R = 5.4\Omega)$	$W/L_N 8$	$115.2\mu m/40nm$

In the simulation, while the power supply is between 2.5V and 3.3V, the output stage is always functional without any breakdown problem but there exists a minor bandwidth

performance difference. The output voltage swing increases from 1.2V (2.5V power supply) to 1.5V (3.3V power supply) while the power consumption increases from 78mW to 230mW. This adjustment takes advantage of the robustness of the CMOS circuit, retaining some fine-tuning space based on different output swing requirements.

The standard power supply of the output stage is 2.8V and the bandwidth is 25GHz. The power consumption is 101mW with a 2.8V power supply and a 40Gb/s data rate.

#### 4.3.4 Modulator driver layout

Fig.4.21 shows the layout of this modulator driver and microscope view of the fabricated modulator driver. In the layout figure (Fig.4.21(a)), DC pads (Vdd, Vdd\_Reg and Vss) are placed at the left and right of the circuit. The input signal goes through the input pads, pre-driver and output stage, and is then fed into the output pads. The input and output pads are in the order of 'gnd!', 'signal+', 'gnd!', 'signal-', 'gnd!' with a 0.1mm pitch.

Chip area (including all pads) is  $634\mu\text{m} \times 634\mu\text{m} = 401956\mu\text{m}^2 = 0.4\text{mm}^2$ .

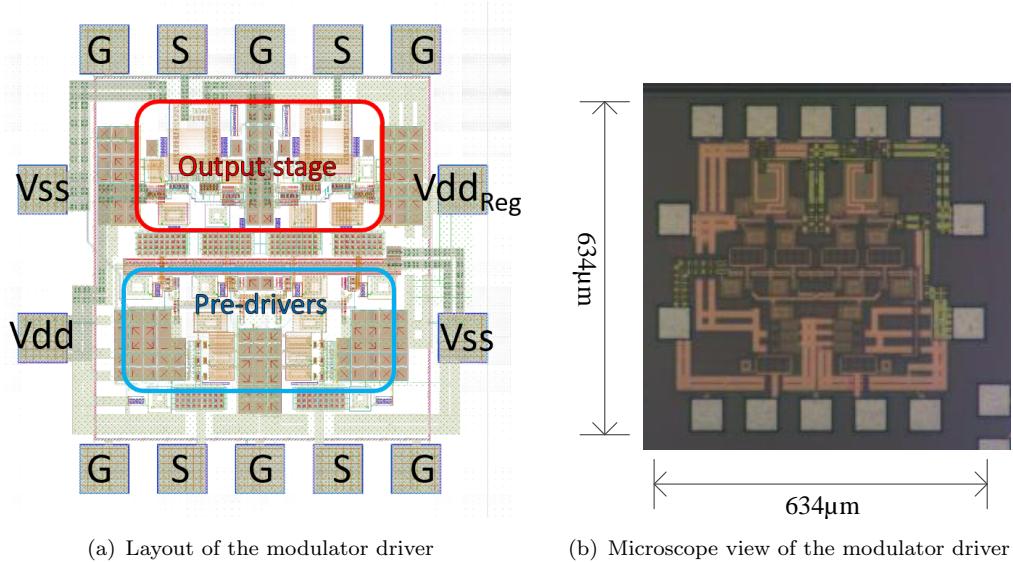


FIGURE 4.21: Layout and microscope view of the modulator driver

#### 4.3.5 Simulation result

This modulator driver is a differential-in differential-out amplifier. The input and output impedance of driver is single end  $50\Omega$  on pass band. An S-parameter simulation test-bench is shown in Fig.4.9.

Group delay from input ports 1 to output ports 2 is plotted in Fig.4.22(a). In the pass band, there is a 12ps ripple. Fig.4.22(b) is the input and output impedance of

the modulator driver. Input impedance is  $50 \pm 8\Omega$  until 28GHz. Output impedance is  $55\Omega$  at mid band, and it is reduced to  $30\Omega$  while it is close to the cut off frequency. Therefore, while the signal frequency is close to the bandwidth limitation, the reflection should presents in voltage swing reduction and jitter increase on the signal.

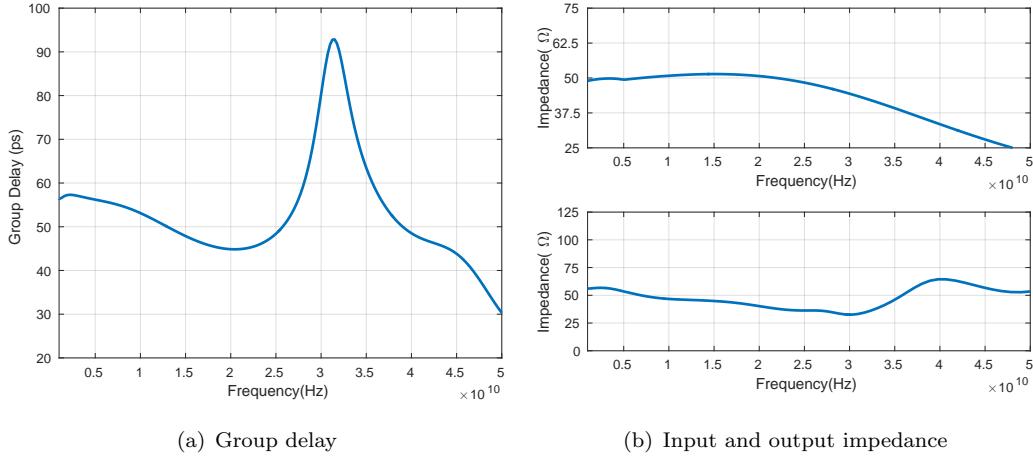


FIGURE 4.22: Group delay and impedance characteristic of modulator driver

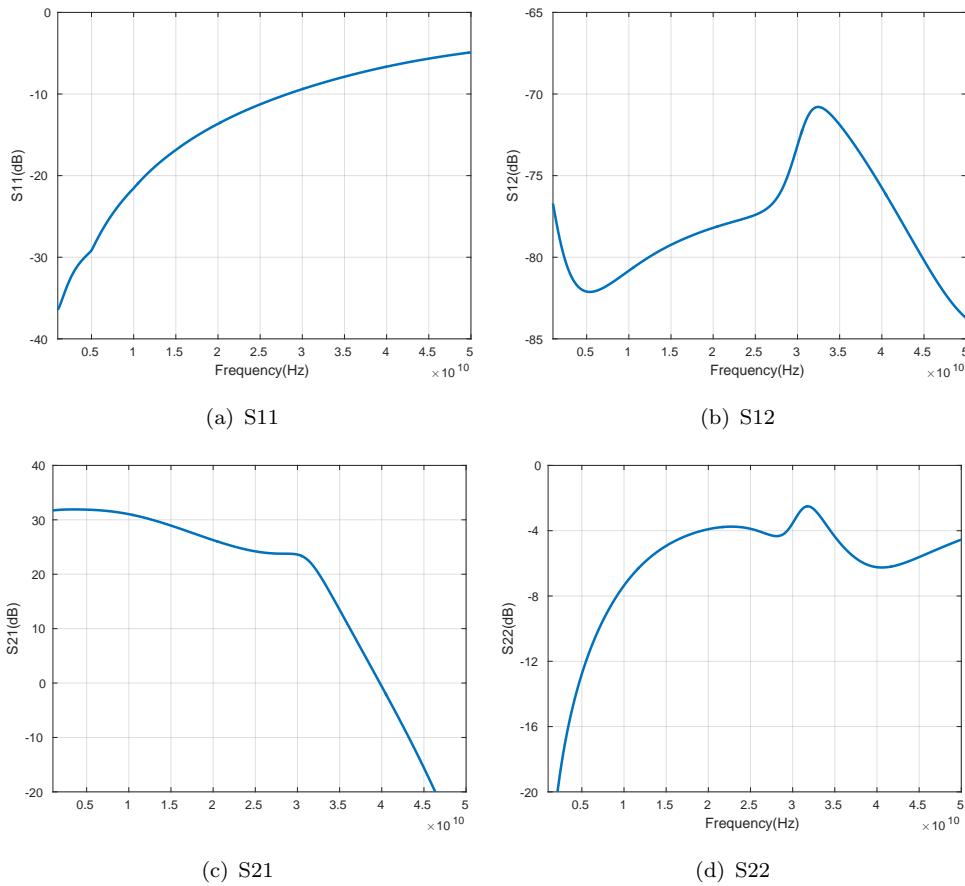


FIGURE 4.23: Schematic of conventional cascode push pull amplifiers

The S-parameter simulation result is plotted in Fig.4.23. The pass band gain of the amplifier can be seen as 23dB even the un-flatness in mid-band. The cutoff frequency

(-3dB) is located at 32GHz. S11 is less than -7dB in the pass band and S22 is greater than -5dB while the frequency is higher than 15GHz.

Transient simulation is based on differential 500mV PRBS NRZ data as input. The output is loading a pair of  $50\Omega$  AC termination and  $150\text{fF}$  capacitors. This capacitor is similar or equivalent to the electrode attenuation on MZM. The transient simulation results is demonstrated as eye-diagrams in Fig.4.24.

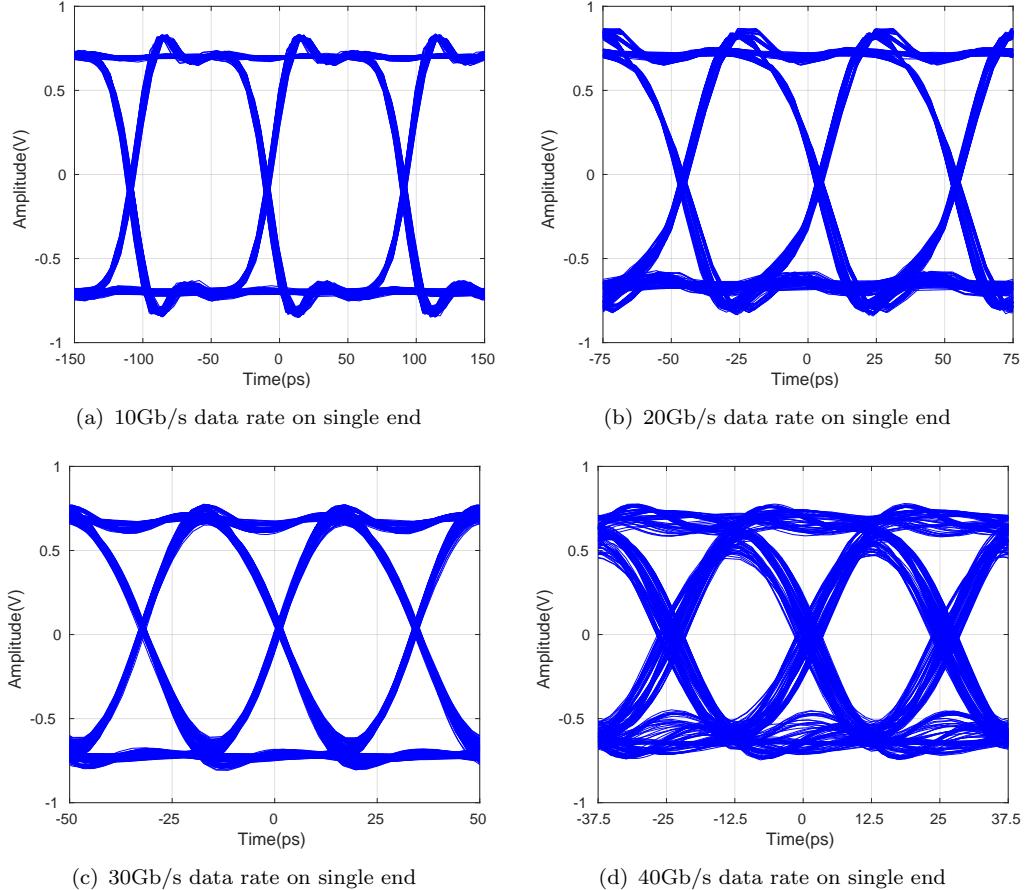


FIGURE 4.24: Transient simulation result of modulator driver

In the transient simulation, 10Gb/s, 20Gb/s, 30Gb/s and 40Gb/s data are applied onto the modulator driver. The output signal swing is over 1.4V. On 30Gb/s and 40Gb/s, the amplitude is minor reduced because of the jitter. This is because of the output impedance reducing on this frequency band. On 40Gb/s the single end voltage swing reduces to around 1.1V.

While 40Gb/s PRBS signal is applied on the modulator driver, power consumptions of  $V_{dd}$  and  $V_{dd\_Reg}$  are observed,

$$V_{dd} = 1.1V, \quad I_{dd\_rms} = 50.9mA.$$

$$V_{dd\_Reg} = 2.8V, \quad I_{dd\_Reg\_rms} = 36.2mA.$$

Power consumption of this modulator driver at 40Gb/s data rate transmission is,

$$\begin{aligned}
 P_{\text{modulator driver}} &= \overbrace{V_{dd} \times I_{dd_{rms}}}^{\text{Pre-driver}} + \overbrace{V_{dd\_Reg} \times I_{dd\_Reg_{rms}}}^{\text{Output stage}} \\
 &= 1.1V \times 50.9mA + 2.8V \times 36.2mA \\
 &= 157mW \quad (40Gb/s \text{ datarate})
 \end{aligned}$$

In the simulation result, the modulator driver

$$\begin{aligned}
 FOM &= P_{\text{modulator driver}} / \text{datarate} \\
 &= 157mW / 40Gb/s \\
 &= 3.9pJ/bit
 \end{aligned}$$

and output stage of modulator driver

$$\begin{aligned}
 FOM &= P_{\text{output stage}} / \text{datarate} \\
 &= 101mW / 40Gb/s \\
 &= 2.5pJ/bit
 \end{aligned}$$

The previous simulation results are based on tt corner of the process and temperature is set as 25°C. More specific simulation conditions and an simulation example are presented in App. A.

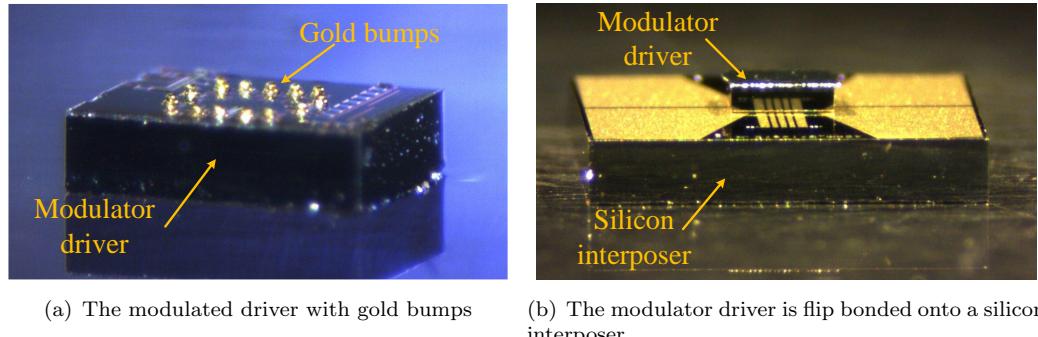
#### 4.3.6 Testing result

The initial test of the modulator driver is electric test.

Fig.4.25 presents the modulator driver with gold bumps and it flip bonded onto a silicon interposer in the electric test. Gold bumps are placed onto the pads of the modulator driver chip. Then, the modulator driver is flipped and mounted onto a silicon interposer. In the electric test, the DC power supply comes from a PCB which connects to the silicon interposer via bonding wire.

A pair of  $2^7 - 1$  differential NRZ PRBS signals is delivered to the modulator driver via a coaxial cable, RF probe and transmission lines on a silicon interposer. The outputs of the modulator driver are fed into the other group of transmission lines on the silicon interposer and RF probe. One output connection is fed into the DCA with  $50\Omega$  input impedance via the coaxial cable and DC block capacitor. And the other output connection of the probe is connected to the DC block capacitor and  $50\Omega$  termination.

Fig.4.26 presents the eye-diagrams of output signal at 10Gb/s, 20Gb/s, 30Gb/s and 40Gb/s. Due to the output reflection increase and attenuation on testing cable, the eye



(a) The modulated driver with gold bumps  
(b) The modulator driver is flip bonded onto a silicon interposer

FIGURE 4.25: The modulator driver flip chip bonding onto silicon interposer

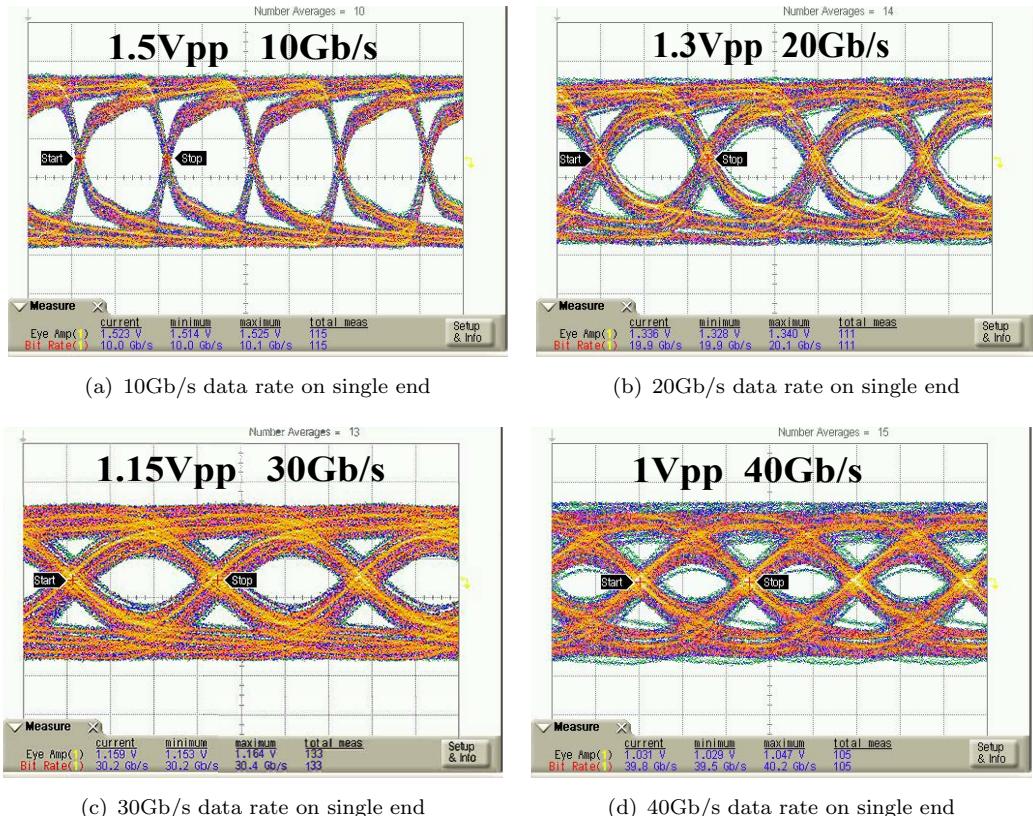


FIGURE 4.26: Electric testing result of modulator driver

amplitude is reduced from 1.5V at 10Gb/s to 1V at 40Gb/s.

Table 4.6 presents the output voltage swing and power consumption on the output stage at 30Gb/s and 40Gb/s input data applied onto the modulator driver when the output stage power supply sweeps from 2.5V to 3.3V.

In this test, on the standard  $Vdd\_Reg = 2.8V$ , while the 40Gb/s data is applied on the

TABLE 4.6: Design detail of output stage

<i>Vdd_Reg</i>	<i>Idd_Reg</i>	Output Amplitude	
		30Gb/s	40Gb/s
2.5V	27mA	1.00V	0.85V
2.8V	34mA	1.15V	1.03V
3.0V	42mA	1.25V	1.10V
3.3V	54mA	1.34V	1.14V

modulator driver, the observed power consumption is,

$$Vdd = 1.1V, \quad Idd_{rms} = 49mA.$$

$$Vdd\_Reg = 2.8V, \quad Idd\_Reg_{rms} = 34mA.$$

Power consumption of full design at 40Gb/s data rate transmission is,

$$\begin{aligned} P_{modulator\ driver} &= \overbrace{Vdd \times Idd_{rms}}^{\text{Pre-driver}} + \overbrace{Vdd\_Reg \times Idd\_Reg_{rms}}^{\text{Output stage}} \\ &= 1.1V \times 49mA + 2.8V \times 34mA \\ &= 149mW \quad (40Gb/s\ datarate) \end{aligned}$$

In the simulation result, the full modulator driver

$$\begin{aligned} FOM &= P_{modulator\ driver}/\text{datarate} \\ &= 149mW/40Gb/s \\ &= 3.7pJ/bit \end{aligned}$$

and output stage of modulator driver

$$\begin{aligned} FOM &= P_{output\ stage}/\text{datarate} \\ &= 95.6mW/40Gb/s \\ &= 2.4pJ/bit \end{aligned}$$

This modulator driver is integrated with two MZM to compose the optical transmitter.

An abstract view of the testing environment of this optical transmitter is shown in Fig.4.15. The input signal of the transmitter is a pair of differential  $2^{7-1}$  NRZ PRBS signals. It is fed into the optical transmitter via a coaxial cable and an RF probe. A  $50\Omega$  AC termination after MZM is provided via an RF probe. The optical signal is coupled to and from the MZM by optical fibres. The optical output of the transmitter is connected to an optical DCA via an optical filter, an EDFA and fibers.

In Fig.4.27, the first integrated modulator is presented. The 1mm length MZM is from [116]. For more modulator efficiency and other specific characteristics, they can be found

in the citation. Unfortunately, there is only one arm of outputs connected to the MZM. The other output arm with wedge pressure pin of bonding is connected to Vss.

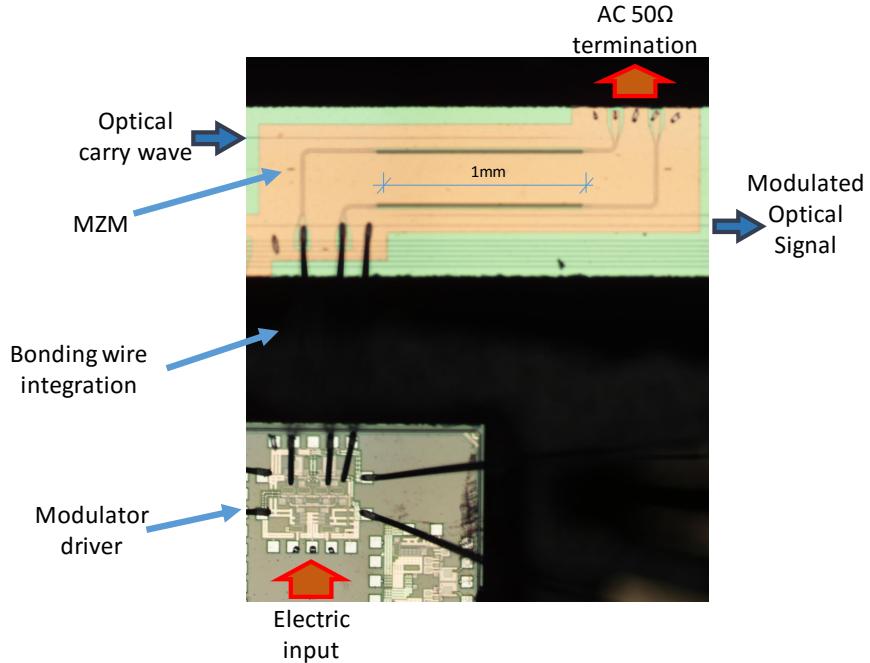


FIGURE 4.27: Modulator driver integrated with MZM from [116]

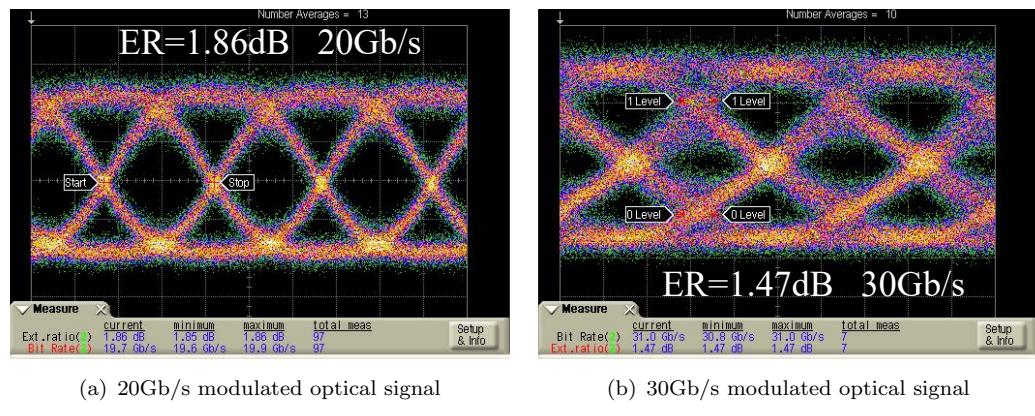


FIGURE 4.28: The modulated optical signals from optical transmitter based on modulator driver and MZM from [116]

The optical modulator is an unbalanced MZM, and the testing result is based on the -3dB (quadrature point) from the lowest insertion loss band.

In this situation, modulated 20Gb/s (Fig.4.28(a)) and 30Gb/s (Fig.4.28(b)) signals are observed on optical DCA. The ER of modulated optical signal is 1.85dB and 1.47dB at 20Gb/s and 30Gb/s.

Unfortunately, by the reason of there is no more MZM samples of [116], the test of integrated optical transmitter base on MZM from [116] stops at this stage.

Fig.4.29 presents the second optical transmitter which is based on MZM from [55]. The modulator driver and the MZM is integrated via bonding wires.

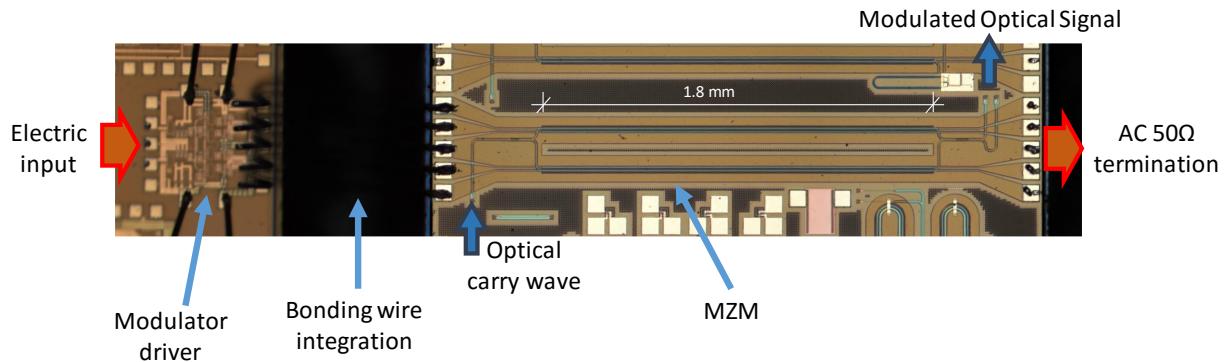


FIGURE 4.29: Modulator driver integrated with MZM2

By measurement, the attenuation on the electrodes of MZM is plotted in Fig.4.30. For more modulator efficiency and other specific characteristics, they can be found in the citation. The -6dB attenuation frequency is 9.76GHz at 0V reverse bias, and it is 20GHz at 3V. In the reason of the reverse bias of the integrated MZM is sharing the VSS of modulator driver, reverse bias voltage is equal to the DC bias of modulator driver which is around 1.65V in 3.3V power supply. The overall bandwidth of the integrated optical transmitter is limited by the electrode attenuation on this MZM.

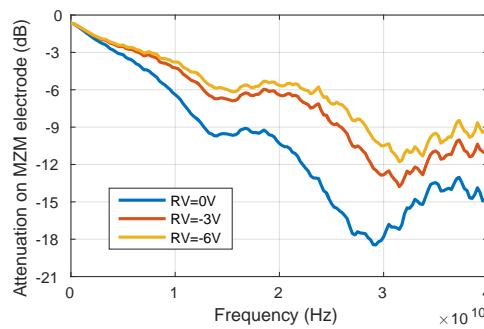


FIGURE 4.30: Attenuation of electrodes on MZM at different reverse bias[55]

The testing result is shown in Fig.4.31. The modulator data rate is up to 25Gb/s with 4.2dB, and 20Gb/s with 6.7dB. In this test, the power supply of the output stage is 3.3V with 51mA.

Both of the previous optical transmitter testing are based on two different unbalanced MZM. And the optical testing result are all on the quadrature point (carry wave from laser are selected the wavelength as -3dB from the minimal insertion loss band of the modulator).

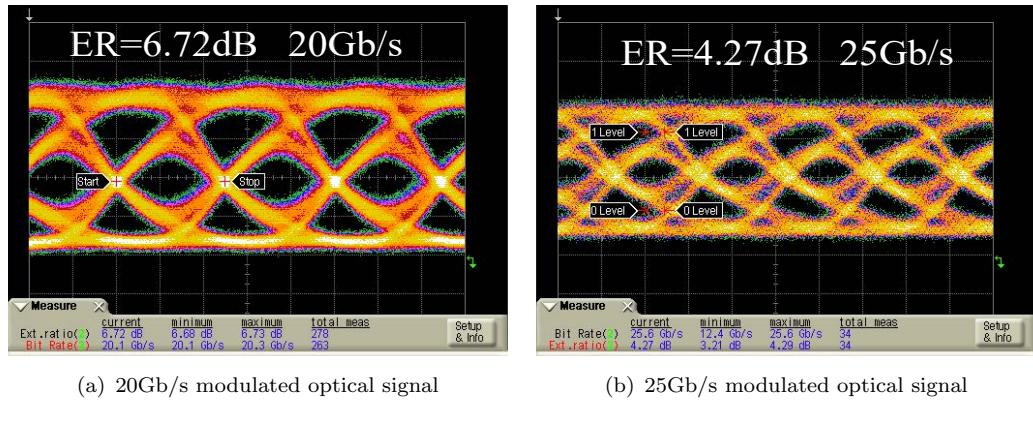


FIGURE 4.31: Electric testing result of modulator driver

## 4.4 Implementation III

### N over N cascode modulator driver with CML pre stage

In this section, a modulator driver is demonstrated in TSMC 40nm CMOS process. Compared with the inductor peaking design in the previous section, this is an optimized design with a CML pre-stage.

This circuit is a fully differential driver for MZM. Output impedance is  $50\Omega$  in the mid-band. Modulator driver power consumption is 228mW (output stage 198mW). Mid-band AC gain is over 20dB and the output voltage swing is over 1.7V on the single end. The data rate is broadband until 40Gb/s ( $V_{pp}=1V$  at 40Gb/s).

#### 4.4.1 Top level schematic of optical transmitter

The top level schematic of the optical transmitter is similar to the previous design. The abstract view of the optical transmitter is presented in Fig.4.32.

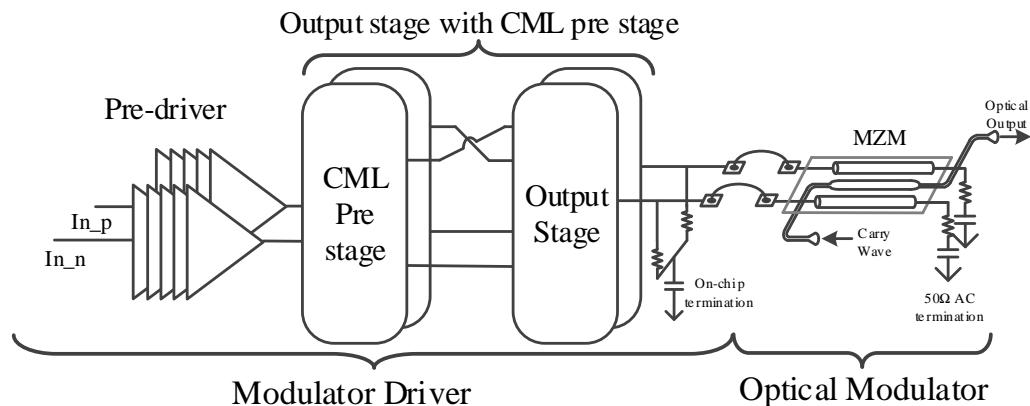


FIGURE 4.32: Top level schematic of the optical transmitter

The power supply of the pre-driver is  $Vdd = 1.1V$  and the output stage including CML pre-stage is powered by  $Vdd_{Reg} = 2.8V$ .

#### 4.4.2 Pre-driver of modulator driver

The pre-driver of the modulator driver is five stages of cascade NMOS common source amplifiers with resistor and inductor loads. Schematic and parameters of circuit are presented in Fig.4.33 and Table 4.7.

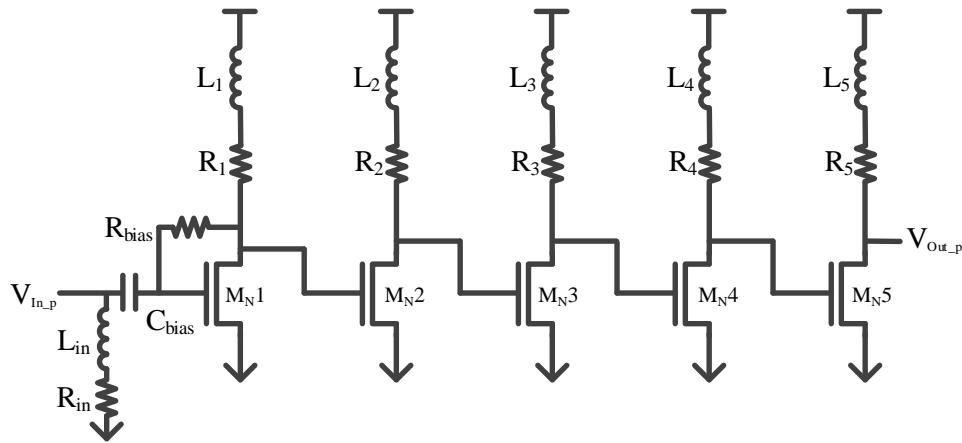


FIGURE 4.33: Schematic of pre-driver in modulator driver

TABLE 4.7: Parameter of major components in pre-driver

$R_{in}$	$46.7\Omega$	$L_{in}$	$L = 168pH(R = 4.9\Omega)$
$R_{bias}/C_{bias}$	$18k\Omega/2.9pF$	$L_1 - L_5$	$L = 297pH(R = 7.6\Omega)$
$R_1 - R_5$	$98\Omega$	$W/L_{N1} - N5$	$16\mu m/40nm$

Input of the pre-driver is a  $50\Omega$  termination with inductor peaking. Through RC network, the signal is re-biased and fed into the five stages of common source amplifiers.

The mid-band gain of the pre-driver is 8dB, and the cut off frequency is 38GHz. Power consumption is 38.6mW with a 1.1V power supply.

#### 4.4.3 Output stage with CML pre-stage

Fig.4.34 and Table4.8 present the design of the output stage of the modulator driver. A CML amplifier with resistance load and inductive peaking is driving up the N-over-N cascode push-pull output stage.

In the CML pre-stage, the cascode transistors are self biased with an RCL network. The gate of  $M_{N11}$  is re-biased from the CML pre-stage; and the gate of  $M_{N11}$  is connected to the drain of  $M_{N5}$  via an inductor. To compose  $50\Omega$  output impedance, an RC network is inserted between outputs.

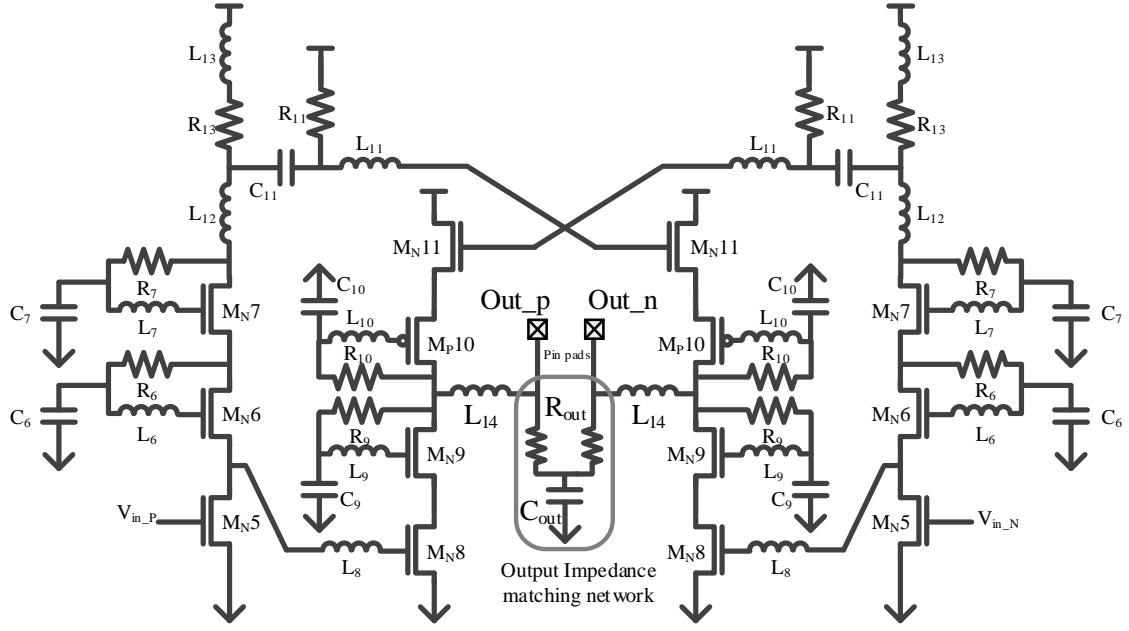


FIGURE 4.34: Schematic of output stage with CML pre-stage in modulator driver

TABLE 4.8: Parameter of major components in output stage with CML pre-stage

$R_6/C_6$	$18k\Omega/1.7pF$	$R_7/C_7$	$18k\Omega/1.7pF$
$R_9/C_9$	$18k\Omega/1.7pF$	$R_{10}/C_{10}$	$18k\Omega/1.7pF$
$R_{11}/C_{11}$	$18k\Omega/2.9pF$	$R_{out}/C_{out}$	$119\Omega/5.4pF$
$L_6-L_7$	$L = 59pH(R = 1.4\Omega)$	$W/L_{N5}$	$48\mu m/40nm$
$L_8$	$L = 269pH(R = 6.1\Omega)$	$W/L_{N6-N7}$	$86.4\mu m/40nm$
$L_9-L_{10}$	$L = 58pH(R = 1.1\Omega)$	$W/L_{N8}$	$126\mu m/40nm$
$L_{11}$	$L = 414pH(R = 8.6\Omega)$	$W/L_{N9}$	$144\mu m/40nm$
$L_{12}$	$L = 269pH(R = 6.1\Omega)$	$W/L_{P10}$	$192\mu m/40nm$
$L_{13}$	$L = 220pH(R = 5.4\Omega)$	$W/L_{N11}$	$156\mu m/40nm$
$L_{14}$	$L = 205pH(R = 2.3\Omega)$		

With the CML as the pre-stage, the voltage swing of the signal fed into  $M_{N11}$  is 1.6 times of the signal fed into  $M_{N8}$ . It compensates for the low gain disadvantage of source follower. Therefore, the output voltage swing of optimized N-over-N cascode push pull amplifier is enhanced.

The output stage including the CML pre-stage is powered by  $Vdd_{Reg} = 2.8V$ ; and the output stage generates over 11.8dB of mid-band gain and the cut-off frequency is around 32GHz.

#### 4.4.4 Modulator driver layout

Fig.4.35 presents the layout and microscope view of this modulator driver. In the layout figure (Fig.4.35(a)), DC pads (Vdd, Vdd\_Reg and Vss) are placed on the left and right

of the circuit. The input signal goes through the input pads, pre-driver, CML pre-driver and output stage, and is then fed into the output pads. The input and output pads are in the order of 'gnd!', 'signal+', 'gnd!', 'signal-', 'gnd!' with 0.1mm pitch.

Chip area (including all pads) is  $613\mu\text{m} \times 620\mu\text{m} = 380060\mu\text{m}^2 = 0.38\text{mm}^2$ .

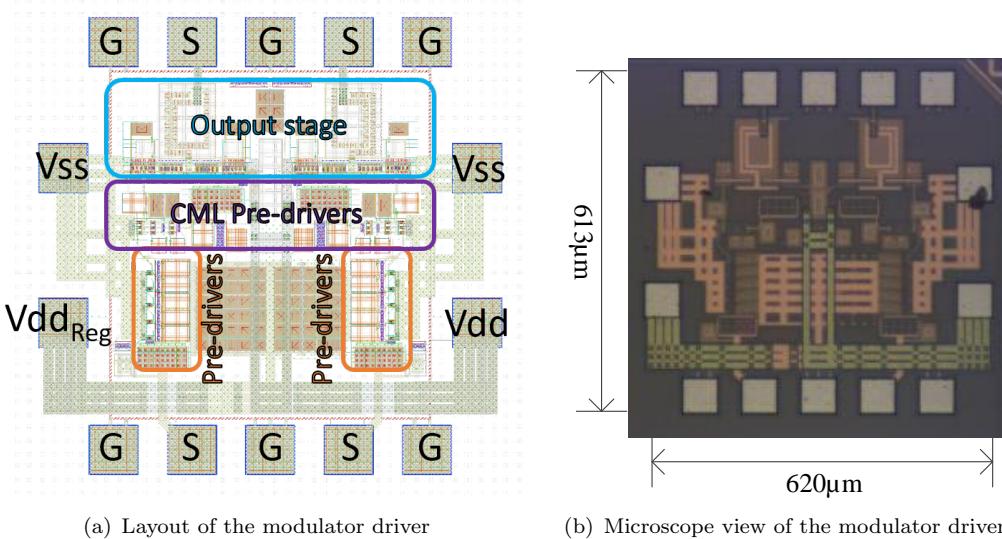


FIGURE 4.35: Layout and photograph of modulator driver

#### 4.4.5 Simulation result

This modulator driver is a differential-in differential-out amplifier where input and output impedance of the driver is  $50\Omega$  on pass band. The S-parameter simulation test-bench is shown in Fig.4.9.

Group delay from input ports 1 to output ports 2 is plotted in Fig.4.36(a). Until 40Gb/s (28GHz), the group delay is  $50\text{ps} \pm 10\text{ps}$ . Fig.4.36(b) is the input and output impedance of the modulator driver. Input impedance is  $50\Omega$  on mid-band and reduced to  $38\Omega$  until 28GHz. In the reason of the inductor L14 in the designed circuit, the output impedance is not flat in the broadband. Output impedance is  $55\Omega$  at mid band, and it is reduced to  $30\Omega$  while it is close to the cut off frequency. Therefore, the reflection will present as jitter and voltage swing reduction while the applied signal is closing to the cut off frequency.

Fig.4.37 presents the S-parameter of the modulator driver. The mid-band gain of the modulator driver is 20dB. In S21, the cut-off frequency is located at 32GHz. The input reflection (S11) is -10dB until 28GHz and the output reflection (S22) is -5dB while the frequency is close to 28GHz. While high speed data (i.e.40Gb/s) is applied onto the modulator driver, there will be apparent jitter appearing on the signal caused by the reflection.

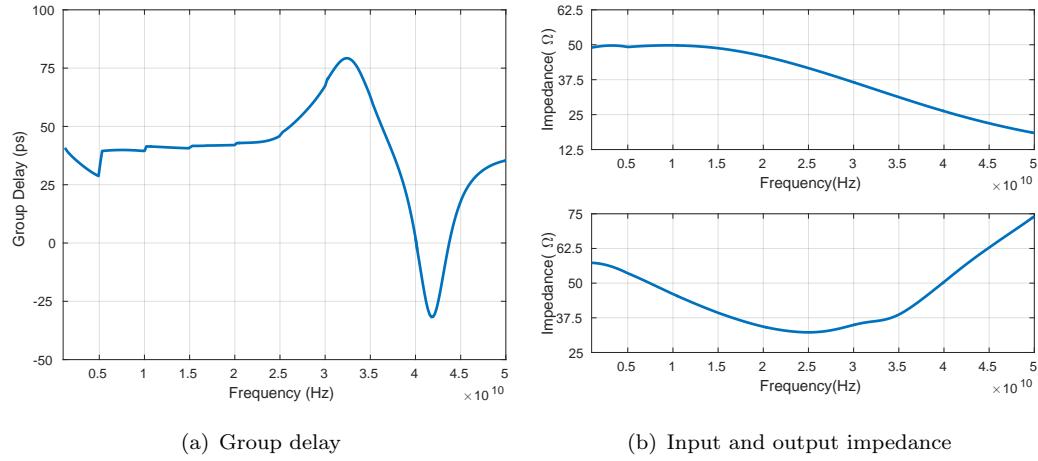


FIGURE 4.36: Group delay and impedance characteristic of modulator driver

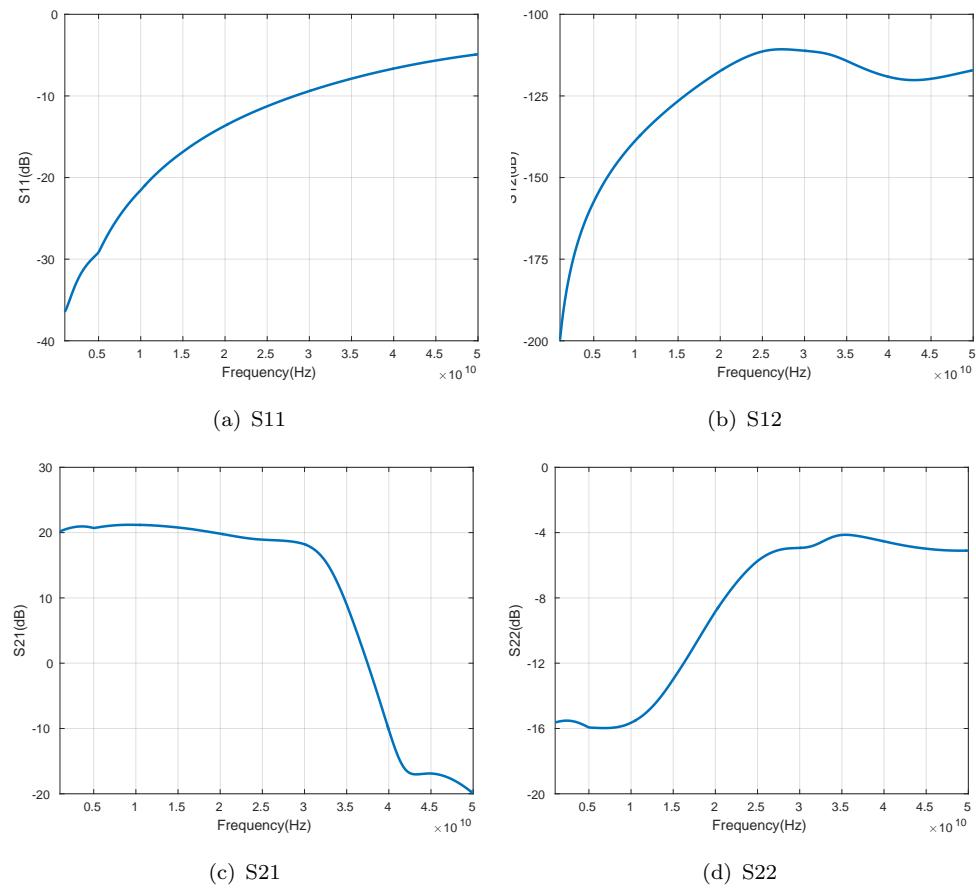


FIGURE 4.37: Schematic of conventional cascode push pull amplifiers

In the transient simulation, 500mVpp PRBS NRZ signals are applied to the modulator driver. The output is loading a pair of  $50\Omega$  AC termination and  $150\text{fF}$  capacitor. This capacitor is similar equivalent to the electrode attenuation on MZM. The transient simulation result is plotted as eye-diagrams in Fig.4.38.

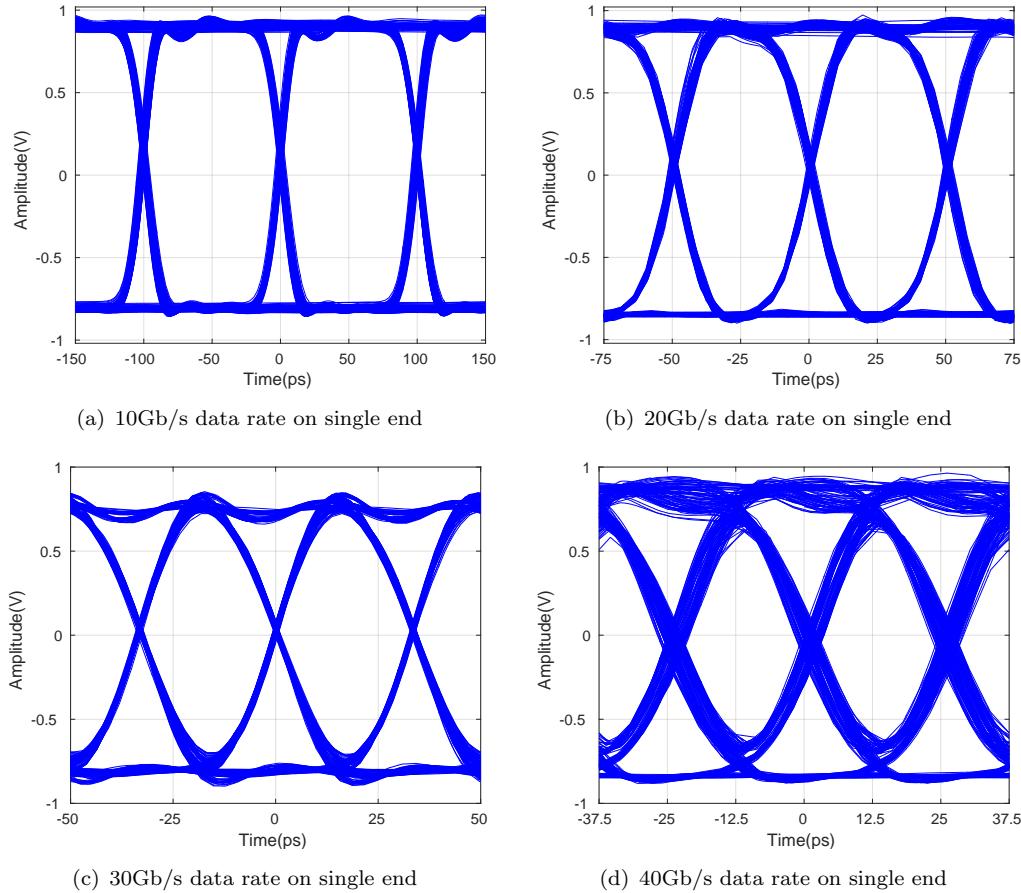


FIGURE 4.38: Transient simulation result of modulator driver

The single end voltage swing of modulator  $V_{pp} = 1.7V$ . While the speed of the data rate increases, the jitter of the signal is rising in the meantime. On 40Gb/s, the output voltage swing reduces to  $1.2V$ . These simulation results are based on the  $V_{dd\_Reg} = 2.8V$ .

In this simulation, the power consumption is observed,

$$V_{dd} = 1.1V, \quad I_{dd_{rms}} = 35.1mA.$$

$$V_{dd\_Reg} = 2.8V, \quad I_{dd\_Reg_{rms}} = 75.6mA.$$

Power consumption of modulator driver at 40Gb/s data rate transmission is,

$$\begin{aligned}
 P_{\text{modulator driver}} &= \overbrace{V_{dd} \times I_{dd_{rms}}}^{\text{Pre-driver}} + \overbrace{V_{dd\_Reg} \times I_{dd\_Reg_{rms}}}^{\text{Output stage}} \\
 &= 1.1V \times 35.1mA + 2.8V \times 75.6mA \\
 &= 250.3mW \quad (40Gb/s \text{ datarate})
 \end{aligned}$$

In the simulation result, the modulator driver

$$\begin{aligned} FOM &= P_{\text{modulator driver}} / \text{datarate} \\ &= 250.3 \text{mW} / 40 \text{Gb/s} \\ &= 6.26 \text{pJ/bit} \end{aligned}$$

and output stage with CML pre-stage of modulator driver

$$\begin{aligned} FOM &= P_{\text{output stage with CML pre-stage}} / \text{datarate} \\ &= 211.7 \text{mW} / 40 \text{Gb/s} \\ &= 5.3 \text{pJ/bit} \end{aligned}$$

The previous simulation results are based on tt corner of the process and temperature is set as 25°C. More specific simulation conditions and an simulation example are presented in App. A.

#### 4.4.6 Testing result

The electric testing of this modulator driver is similar to the previous 40nm design. Gold bumps are mounted onto the pads of the modulator driver. Then the modulator driver is flipped and bonded onto a silicon interposer. The DC power supply comes from the PCB and connects to the silicon interposer via bonding wires.

A pair of  $2^7 - 1$  differential NRZ PRBS signals is delivered to the modulator driver via coaxial cable, RF probe and transmission lines on the silicon interposer. Outputs of the modulator driver are fed into the other group of transmission lines on silicon interposer, and an RF probe. One output connection of RF probe is connected to the DCA with  $50\Omega$  input impedance via coaxial cable and DC block capacitor. And the other output connection of the probe is connected to a DC block capacitor and  $50\Omega$  termination.

Fig.4.39 presents the eye-diagrams of output at 10Gb/s, 25Gb/s, 30Gb/s and 40Gb/s. Single end voltage swing is 1.7V. Due to the output reflection increase in high frequency band and attenuation on testing cable, the Vpp is reduced from 1.73V at 10Gb/s to 1.05V at 40Gb/s. Furthermore, the signal quality of 40Gb/s is obviously reduced causing jitter. This result proofs the simulation result of the output impedance reduction after 20GHz of the output stage. Even with an inductor at the output point which enhances the bandwidth, the group delay as well as the output impedance is compensated. Both the increasing jitter from un-flat group delay and the output impedance discontinued are causing the reduction of signal integrity at 40Gb/s.

Compared with the previous design in Sec.4.3, the output voltage swing in mid-band is optimized with 200mV improvement.

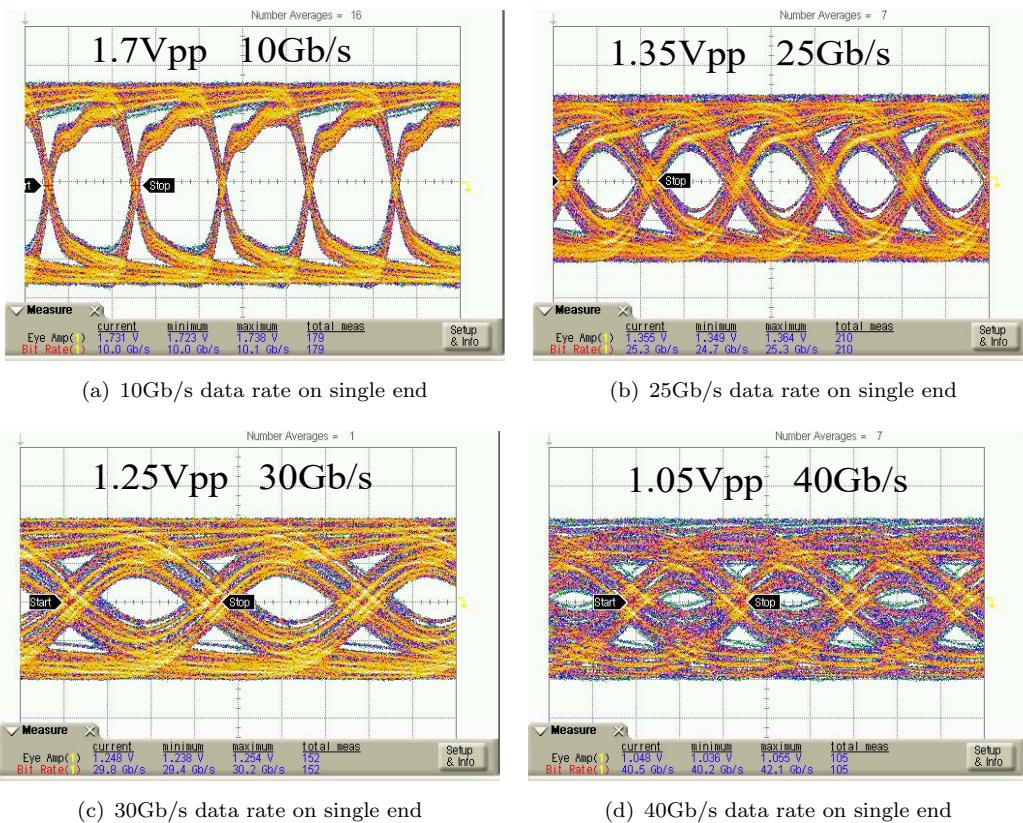


FIGURE 4.39: Electric testing result of modulator driver

On the testing, the power consumption is observed as,

$$Vdd = 1.1V, \quad Idd = 34mA.$$

$$Vdd\_Reg = 2.8V, \quad Idd\_Reg = 71mA.$$

Power consumption of modulator driver at 40Gb/s data rate transmission is,

$$\begin{aligned}
 P_{\text{modulator driver}} &= \overbrace{Vdd \times Idd_{rms}}^{\text{Pre-driver}} + \overbrace{Vdd\_Reg \times Idd\_Reg_{rms}}^{\text{Output stage}} \\
 &= 1.1V \times 34mA + 2.8V \times 71mA \\
 &= 236.2mW \quad (40Gb/s \text{ datarate})
 \end{aligned}$$

In the simulation result, the modulator driver

$$\begin{aligned}
 FOM &= P_{\text{modulator driver}}/\text{datarate} \\
 &= 236.2mW/40Gb/s \\
 &= 5.9pJ/bit
 \end{aligned}$$

and output stage with CML pre-stage of modulator driver

$$\begin{aligned}
 FOM &= P_{\text{output stage with CML pre-stage}} / \text{datarate} \\
 &= 199mW / 40Gb/s \\
 &= 5pJ/bit
 \end{aligned}$$

For the reason of limit numbers of MZM samples, this modulator driver is not integrated to any MZM. Based on the results of electrical tests, it can be inferred that the performance of the integrated optical transmitter is similar to the previous design in Sec.4.3 but ER increases, caused by the output voltage swing optimization.

## 4.5 Analysis

Three implementations have satisfied the design requirements. In three steps, they prove the functionality of the proposed circuit topology and optimize it on bandwidth performance and output voltage swing. These circuit implementations are also verifications of the design methodology in Ch.3.

In the three implementations, there are minor differences between testing results and simulation results. Regarding the example of implementation II, the power consumption of testing result (95.6mW) is 5% lower than the simulation result (101mW). The output voltage swing is lower (around 100mV) in tests and the high-frequency performance of the simulation result is always better than the tests. These differences could be explained by simulated circuit extraction inaccuracies and testing environments.

Table4.5 shows the performance summary of the proposed modulator drivers and their comparison to other related works. The proposed modulator driver is advantageous in overall performance, especially the transmission speed and power consumption. Only one of the related works offers the further advantage of the fabrication process in gaining better speed performance is lacking in terms of power consumption. Power efficiency performance is also optimized in the three implementations. In implementation II, the power efficiency FOM is as low as 3.4pJ/bit including the pre-driver stages. On the N-over-N cascode push-pull output stage only, the FOM in implementation II is as low as 2.4pJ/bit.

In the previous design examples, the output signals present varying output impedance discontinued on the broadband. To further improve these implementations, a possible way is build up an improved, quality output impedance network. Compared with the output impedance matching network in implementation I, the ones in II and III obviously provide worse performance. The group delay of II and III are greater than I, also the jitter on eye diagrams are also increased. In order to optimize that, an additional inductor into the RC network is one solution. In order to further improve the

Process	MWCL 2018 [66]	OFC 2015 [87]	ASSCC 2015 [80]	TCAS 2016 [53]	CICC 2010 [49]	TCAS II 2018 [43]	JSSC 2016 [105]	Imp I	Imp II	Imp III
	90nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	45nm SOI CMOS	65nm FD-SOI CMOS	28nm FD-SOI CMOS	130nm CMOS	40nm CMOS	40nm CMOS
Output stage	DA	DA	CML	CML	Push-Pull	Push-Pull	Proposed	Proposed	Proposed	Proposed
topology			Type 1 1.2/3.3 1.5/2.3/2.6	Type 2 1.5/3.9	3V/5V	1.5/2.7/3.3	6	1.6/3.3	1/2.8	1/2.8
Power Supply (V)	5	4.5								
Data Rate (Gb/s)	40	25	20	25	40	32	60	20	40	40
Power (mW)	650	520	480	348	437	201	318	312		
V <sub>pp</sub> at 10Gb/s	4	6.4	3.3	5	3.8	4.5	4	5	3.4	3
Biassing Tee	X	N/A	O	O	X	X	X	X	X	X
FOM (pJ/bit)	16.25	20.8	19.2	26.7	13.9	10.9	6.28	5.3	15.6	3.4

output impedance, active impedance matching network[35], active inductor network [57] or feed forward equalized [20; 89] output amplifier could be considered to used in the future designs.

## 4.6 Summary

In this chapter, three implementations based on the proposed circuit in Ch.3 are demonstrated in 130nm and 40nm CMOS processes.

Implementation I is a proposed modulator driver design on 130nm CMOS processes. It integrates with MZM via the bonding wires, and composes as a 20Gb/s optical transmitter. With 312mW power consumption, the optical transmitter ER=5dB and output stage FOM=7.4pJ/bit.

The modulator driver in implementation II is functional until 40Gb/s with 149mW power consumption. The FOM is as low as 3.7pJ/bit and output stage power efficient is 2.4pJ/bit. It is compact integrated with two MZM as a 30Gb/s and a 25Gb/s optical transmitter.

Implementation III is an optimized proposed modulator driver with CML pre-stage. It is functional to 40Gb/s with 236mW power consumption, power efficient is 5.9pJ/bit. In this implementation, the output swing is optimized around 200mV compare with implementation II.

These three implementations, in order, to prove the design methodologies and optimizations in Ch.3.



# Chapter 5

## Design methodology of a synergistic designed optical transmitter

Though the conventional MZM is well researched, the most published testing of the MZM is still relying on the commercial devices which are discrete components. In the past years, though our proposed modulator driver is always supporting compact integrations, they still require a far end termination which is consists of off-chip components.

In order to further optimize the compactness of the integrated optical transmitter, a U-shape MZM and a specific designed CMOS modulator driver are proposed. Due to the MZM have to be embedded into the CMOS circuit, the synergistic design method is used in this design as well.

### 5.1 Introduction

In this chapter, a novel synergistic design methodology is developed by our optoelectronic design group. Rely the methodology, MZM could be embedded into the modulator driver circuit as a part of it.

Bases on the synergistic design methodology, an efficiency modulator driver which fits with a specific designed U-shape MZM is designed. The composed optical transmitter is a compact integrated design which avoids the off-chip component.

The designed optical transmitter is also available to demonstrate a efficient PAM4 transmitting. Therefore, the advantage of this efficient PAM4 transmitter and PAM4 linearity adjustment method is investigated as well.

## 5.2 Synergistic design

The synergistic design is a concept that is optical and electronic co-operative design.

A monolithic photonics platform's decisive advantage is the integration of optoelectronic devices in the same design platform, so many unique designs can be realized, but the monolithic photonics platform is rare and expensive. The unique design in monolithic photonics platform is not impossible under other integration methods. Relying on the long-term cooperation between optical engineers and electrical engineers in our design team, and more importantly, our long-standing experience in the integration, unique design can be done on the non-monolithic photonics platform with our close design cooperation.

In this optical transmitter, the synergistic design is used due to the modulator driver cannot work along without MZM. And the MZM is also a unique design which is specially designed for the specific electronic driver circuit.

In the electronic circuit design region, the MZM is modelling as an electric model base on S-parameter, and embedded into the electronic circuit. The optical designer also provides a simulation platform based on the designed MZM on the Interconnect from the Lumerical, which can be used to simulate the modulated optical signal by importing the electrical waveform on the designated circuit node. Simultaneously, the optical engineer is also asked to convert the conventional MZM to be a unique shape which fits the specially designed modulator driver circuit. Regarding the integration, the parasitic of pads and integration (flip chip in this design case) are also considered and embedded into the electronic circuit design platform.

In the later two sections, the optical transmitter design as well as the PAM4 transmitter are designed rely on this synergistic design platform.

## 5.3 An efficient optical transmitter design

In recent years, increasing silicon photonics designs have moved beyond the device level and gradually moved toward onto silicon photonics circuits and even systems. In these silicon photonics circuits or systems, Si MZM is used in because of its stable performance.[4; 71; 131] For silicon photonics circuits, the essential performance of the modulator driver is not only the highest operating speed, but also the power consumption (efficiency) and compact integration. Due to the emergence of WDM and segmented MZM, multiple independent modulator drivers need to be integrated into a limited chip area. Therefore, in some scenarios, compact integration and optimized power efficiency are even more important than the highest operating speed.

In this section, a modulator driver structure is investigated to achieve an efficient design, and a unique MZM is also designed to fit with the modulator driver which optimizes an optical transmitter as a compact integrated design without off-chip components.

The optical transmitter is a cooperative job of our full optoelectronic design team and the author is honored to participate of it. The author's main contribution in the design project is to work with colleagues to establish the novelty of the design, to participate in and build a module-level framework, and to participate in the integration and testing work in the later stage. The electrical circuit design job that should have partially undertaken by the author had to be completed by colleagues during author's suspension due to disease.

### 5.3.1 Open drain modulator driver

The power efficiency of the optical transmitter is one of the significant performance which directly affects the applications. The power efficiency result needs to be built upon the observed power consumption of the modulator drive, and cannot rely on the calculation of the square of the required electrical signal voltage swing divide by termination resistance.

The power consumption of modulator driver is always higher than the square of output  $V_{pp}$  divides termination resistance.[123] Aside all the configurations with bias-tee (they can not compact integrate to modulator), the highest efficient configuration is open drain with a far end termination.

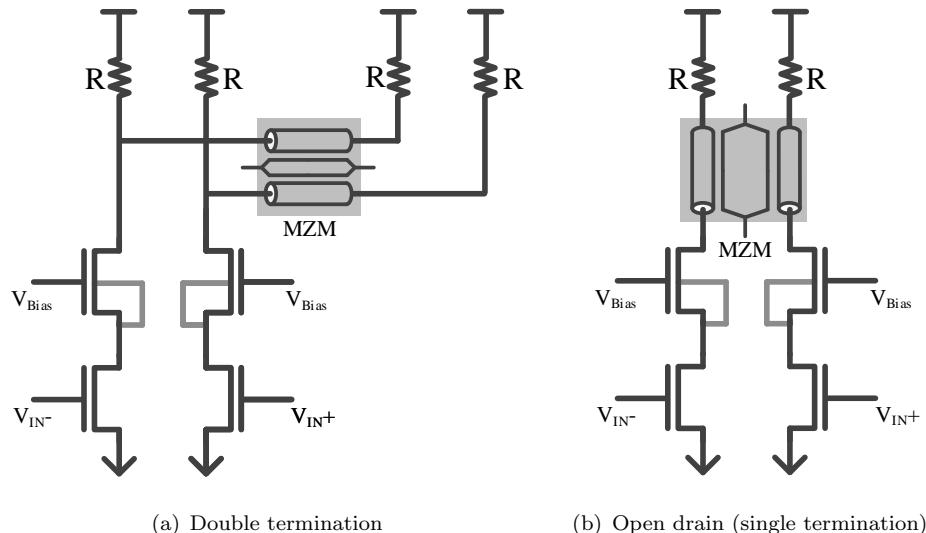


FIGURE 5.1: A modulator driver with two termination configurations

Hereinafter compares a modulator driver with double and single terminations to present the efficient of modulator driver.

The double termination as shown in Fig.5.1(a), is commonly used in the modulator driver designs.[48; 49] One of the advantages of the double termination circuit is that the modulator driver can work alone without the MZM. The other advantage of the double termination circuit is the near-end load resistor guarantee the output impedance of the modulator driver is approx equal or lower at the value of  $R$ . But loading both near and far end terminations, the load impedance of the amplifier is  $R/2$  where the  $R$  equal to Tx line nominal impedance.

To eliminate the power consumption lost due to double terminations, the single termination (Fig.5.1(b)) approach becomes an appropriate selection. In the reason of there is only far end termination load at the end of MZM with power supply, the modulator driver is indeed an open drain amplifier. Without the near end load impedance, the open drain modulator driver can be considered as a controlled current source which amplifies the input signals. The Tx line on MZM and the far end termination impedance with power supply are treated as the load of the amplifier circuit.

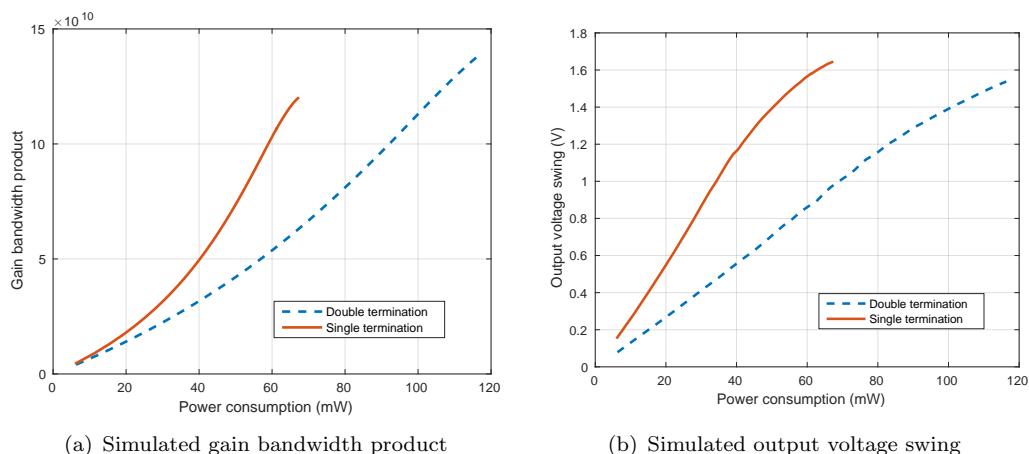


FIGURE 5.2: Two typical modulator driver topologies integrates with a nominal  $50\Omega$  MZM

Fig.5.2 illustrates a comparison of the double termination circuit and open drain (single termination) circuit on a 28nm CMOS process. The width of transistors ( $length = 30nm$  in simulation) in Fig.5.1 grandly increase from  $2\mu m$  to  $180\mu m$ . The power supply of two circuits are both located at  $1.8V$  and  $R = 50\Omega$ . The simulated gain bandwidth product and output voltage swing of these two circuit topologies are plotted with their power consumptions as the x-axis.

To achieve the same gain-bandwidth product, the power consumption of single termination is always lower than double termination. In addition, the comparison of output voltage swing (near end) presents the single termination uses half of the power consumption to achieve the same result in double termination.

Although single termination shows optimized efficiency, there are still a risk in implementation of open drain works with MZM. The electrode on MZM is should be a resistance

less ideal Tx line, but the reality is that the sheet resistance of electrode affects the performance of optical transmitter. The resistance on MZM electrode can be treated as a resistor which also be a part of load. Therefore the output DC bias of open drain increases along the MZM electrode which affects the reverse bias voltage of MZM is increasing along the MZM. The resistance of MZM electrode uses in Ch.6 is approx  $8\Omega$ . Even with a 20mA shunt current, the DC voltage difference between near end and far end of MZM is only 160mV. Both simulation and testing result proves the reverse bias increase on MZM is not significantly affects the optical signal integrity. Therefore in this design case, the DC shift on MZM in design could be neglected.

In the design implementation region, an optimized open drain amplifier is designed in a 28nm CMOS process. Benefit from the synergistic designed platform, the MZM could be embedded into the modulator driver circuit design. More specific circuit information are discussed in Ch.6.

### 5.3.2 U-shape MZM and on CMOS chip termination

To implement future silicon photonics circuits, avoid to use large area cost off-chip component is necessary. In the most of our modulator driver designs, compact integration is one of the additional condition on the performance requirement. Therefore, even if bias tee can maximize efficiency, it still gives up using either commercial or customized on board bias tees [50] in the design. Without bias tee, the most common far end termination is a pair of resistors which locates at Tx line nominal impedance. These resistor could be consisted of wither off-chip components or on optical chip components. In this design, we decide to optimize the compact integration level. Due to open drain amplifier requires a pair of loads with power supply, the far end termination in this design is implemented by on electronic chip components.

To implement the open drain driver and termination network both on the electronic chip, the the cooperative optical device designer has been asked for designing the MZM as a U-shape as shown in Fig.5.3. The electric signal feeds into the MZM and travels through Tx line electrodes, then returns to the electronic chip and connects the far end termination networks with power supply. The U-shape MZM and its modulator driver could be compact integrated together and avoid all the off-chip component.

Fig.5.3 also presents the microscope of the fabricated U-shape MZM. This MZM costs  $1200\mu\text{m} \times 650\mu\text{m}$  area and the phase shifter length is  $2.2\text{mm}$ .

Another advantage of the U-shape MZM is that the electric signal is returned to the electronic chip after it traveled through the electrode on MZM. Therefore, it is possible to capture the returned electric signal and to detect more signal quality information. In future system-level designs, an additional peak detector can detect the returned signal,

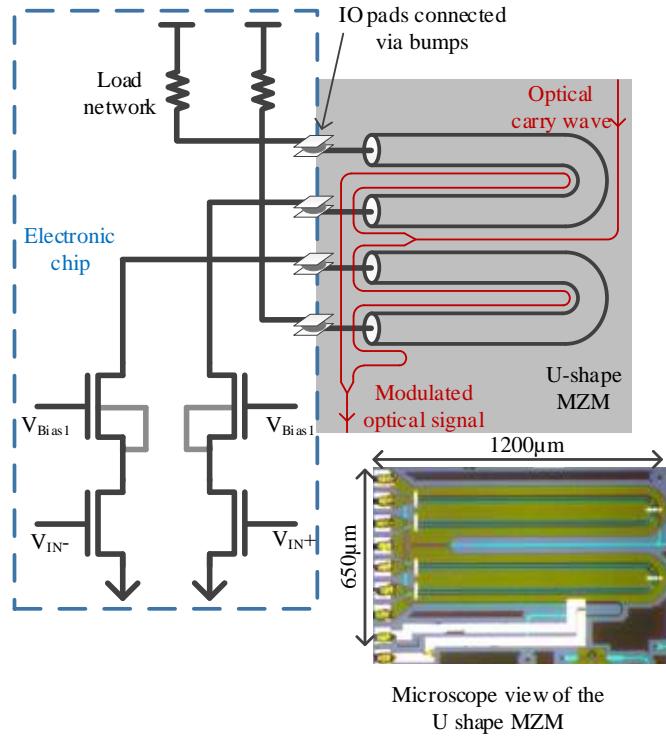


FIGURE 5.3: Abstract view of modulator driver integrated with U-shape MZM and microscope view of the U-shape MZM

then control a pre-emphasis or power system for modulator driver to boost and maintain the signal. This control loop relates to only electronic devices without PD in the conventional control loop[40; 60].

In this optical transmitter, the far end termination load with power supply is consists of on-chip components. Hereinafter illustrates this termination of optical transmitter circuit.

Due to the current density limitation of P+ poly without silicide resistor in the 28nm CMOS process, this resistor is a  $5.4\mu\text{m}$  length,  $32\mu\text{m}$  width con chip component. The parasitic capacitance of the resistor and IO pads can easily reduce the impedance in high frequency region. To enhance the bandwidth of the load impedance is located around  $50\Omega$ , which is the nominal impedance of designed MZM, a customized inductor is added into the load as shown in Fig.5.4(a). And Fig.5.4(b) compares this load impedance with and without the inductor. Assume  $50\Omega \pm 5\Omega$  is acceptable, the observed impedance of load from simulation is enhanced from 20.7GHz to 42.6GHz.

## 5.4 PAM4 optical transmitter

Sec.2.7.2 reviewed the present PAM4 methodology on silicon photonics platform. This section proposes a low cost synergistic designed PAM4 optical transmitter.

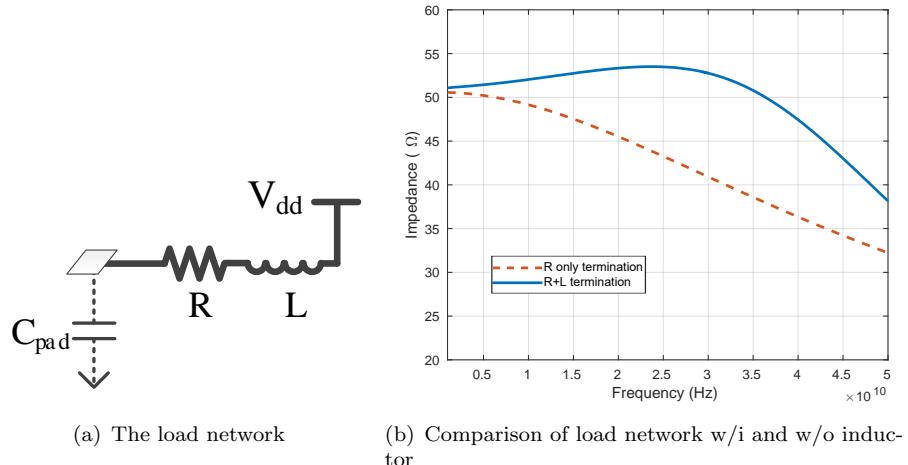


FIGURE 5.4: Two typical modulator driver topologies integrates with a nominal  $50\Omega$  MZM

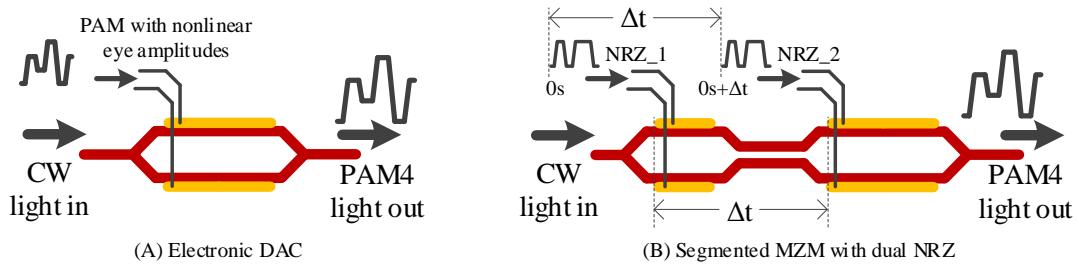


FIGURE 5.5: Conventional PAM4 optical transmitter

Fig.5.5 presents the two conventional PAM4 methodologies. Both of these two requires high performance on the electronic system as below specific,

### Electronic DAC

In the reason of modulated optical signal composes by different phase shifted optical carry waves from two arms of MZM, the relationship of optical ER and electronic amplitude is a  $\pi$  curve but linear. Therefore, the electronic DAC PAM4 requires not only a high speed electronic DAC but the nonlinearity adjustment performance of eye amplitudes. The analysis in Sec.5.4.2 presents equalled optical amplitude PAM4 relationship with electronic amplitudes for different targeting ER. Accurately adjusting the eye amplitude of the electronic signal, high output amplitude and high speed performance significantly increase the performance and cost of the electric DAC.

### Segmented MZM with dual NRZ

On the phase shifter, the electronic signal on electrodes (Tx line) and the optical in the waveguide can be seen as synchronously marching. But the 2nd phase shifter is modulating the optical signal after the 1st phase shifter. Therefore, there must be an initial timing difference between the two electronic inputs. The initial timing

difference ( $\Delta t$ ) is approximately equal to the optical delay from inputs of 1st phase shifter to the inputs of the 2nd one. Therefore, the input two NRZ signals need to be fine-tuned initial timing at ps level. The necessary accurate timing delay circuit before the modulator driver is the reason for the high cost of this method. The other oblivious problem of optical PAM4 on segmented MZM is the unbalanced bandwidth of two segment of electrodes. The demonstration in [131] has measured the S21 of two individual segments on their device. The result clearly indicates that the longer segment, the most significant bit (MSB), bandwidth falls much earlier than the short one, the least significant bit (LSB). And the overall speed of this PAM4 has to accommodate the bandwidth limitation of the MSB.

This section proposes a efficient and economic PAM4 optical transmitter which requires either high performance electronic DAC or accurate timing delay circuit.

#### 5.4.1 An efficient PAM4 optical transmitter

In order to avoid to use high performance electronic DAC and timing delay control on electronic system, the proposed low cost PAM4 optical transmitter is demonstrated in Fig.5.6. In conventional segmented PAM4, the MSB and LSB are composed by two pairs of MZM. In this proposed circuit, the MSB and LSB are the two arms of a push pull MZM with integrated modulator driver.

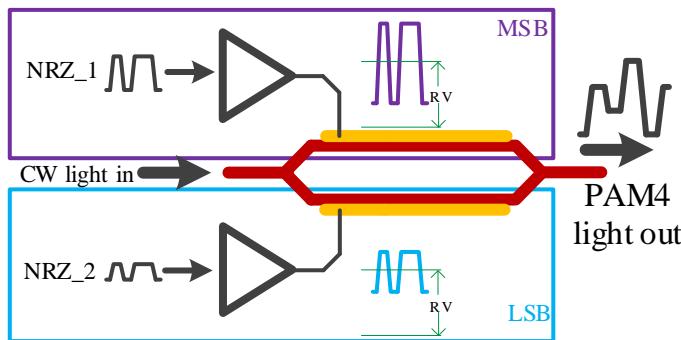


FIGURE 5.6: Low cost PAM4 optical transmitter

With below three assumptions,

- The MSB and LSB in this design are the same as each other but the input signal  $V_{pp}$  are different.
- This push-pull MZM is working at the quadrature point.
- MSB and LSB are sharing the same reverse bias.
- Electric signals after the modulator driver are linearly amplified without distortion.

In the optical transmitter for the NRZ signal, the  $\phi$  difference between the push and pull arm composes the ER. In this PAM4 transmitter, on the individual MSB or LSB, the  $\phi \propto V \times L$  where the V is Vpp of electric signal and L is the length of MZM. Therefore, with fixed L, the adjustable Vpp modifies the phase shifting on MSB and LSB. With the same modulator driver to amplify the input signal,  $\phi \propto Vpp_{Input}$ . Thus, with an appropriate ratio of  $Vpp_{Input}$  of MSB and LSB, the output signal of this MZM is PAM4 modulated.

### 5.4.2 Linearity adjustment of optical PAM4

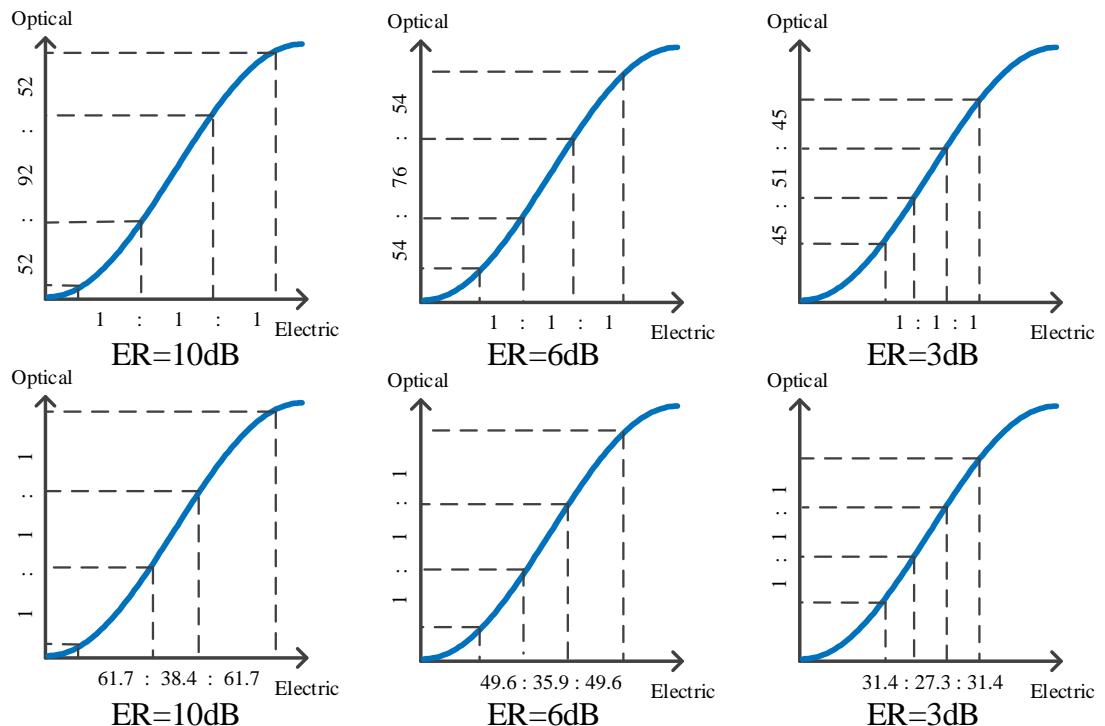


FIGURE 5.7: Linearity of PAM4 optical signal

In this PAM4 optical transmitter, the signal composes by different phase shifting on MSB and LSB. In phase modulation, the relationship of ER and phase shifting is not linearity but a  $\pi$  curve.[104] Therefore, the ratio of  $Vpp_{Input}$  should follow the targeting ER with the relationship on the  $\pi$  curve but not 2:1.

Assume this PAM4 optical transmitter is working at the quadrature point, Fig.5.7 illustrates the relationships of optical signal eye open and electronics at 10dB, 6dB and 3dB.

While Vpp ratio of input electric signals is 2:1 (equivalent to 1:1:1), the resulting optical PAM4 is unbalanced on the eye-amplitude opening. In order to achieve the balanced

optical PAM4, the ratio of electric signal  $V_{pp}$  should be modified as,

$$\frac{V_{ppInputA}}{V_{ppInputB}} = \frac{\pi - \text{acos} \frac{\cos(\frac{\pi}{2 \times 10^{ER*0.1}})}{3} - \frac{\pi}{2 \times 10^{ER*0.1}}}{\text{acos} \frac{\cos(\frac{\pi}{2 \times 10^{ER*0.1}})}{3} - \frac{\pi}{2 \times 10^{ER*0.1}}} \quad (\frac{MSB}{LSB}) \quad (5.1)$$

In Eq.5.1, the targeting ER is unit in dB with limitation of  $ER > 0$ . Fig.5.8 presents this input  $V_{pp}$  ratio in ER from  $0.5dB$  to  $21dB$ . It is around  $2 : 1$  while the targeting ER is near 0 and declining to  $1.62 : 1$  at  $ER \approx 10dB$ , then saturating around over  $1.55 : 1$ .

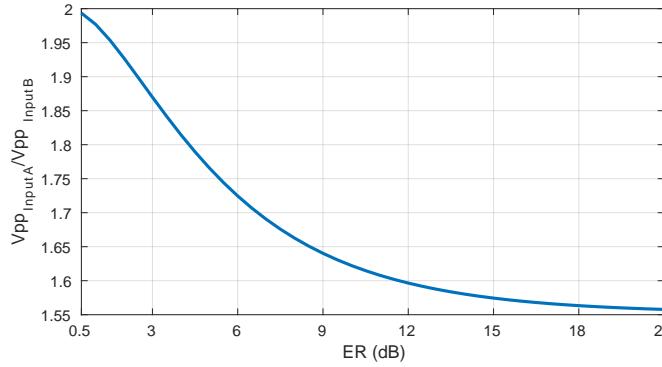


FIGURE 5.8: Input Vpp ratio to targeting ER

A simulation result based on Lumerical is presenting in Fig.5.9. In four different targeting ER, with different input electric  $V_{pp}$  ratios, the optical PAM4 are investigated. The input with modified  $V_{pp}$  ratios generates linear eye amplitude on PAM4.

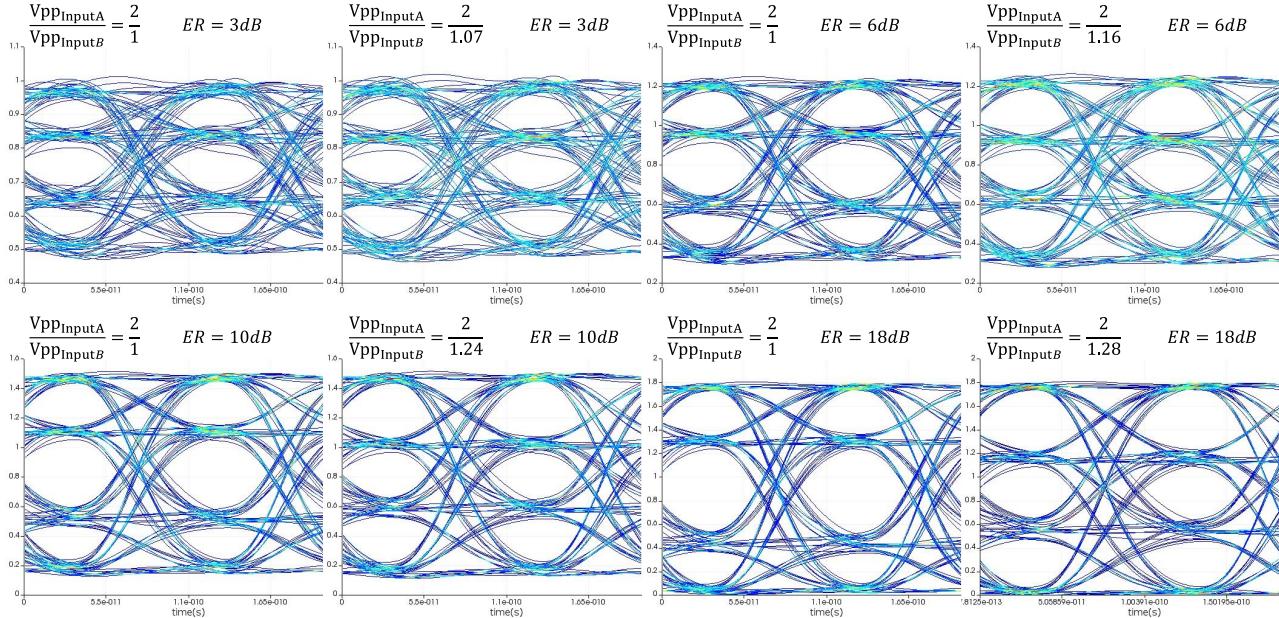


FIGURE 5.9: Input Vpp ratio on different targeting ER

## 5.5 Summary

In this chapter, rely on the experience in the past years of design the optical transmitter, a cooperative optoelectronic design methodology is created and be named as synergistic design method.

With methodology of synergistic optoelectronic design, a specific designed U shape MZM could be embedded into the electric circuit, and compacted integrates with CMOS chip to compose an efficiency optical transmitter which avoids the off-chip component.

In addition, the optical transmitter could be used for demonstrating the efficiency PAM4 optical transmitting. The PAM4 linearity on the MZM bases optical transmitter is also investigated.



# Chapter 6

## Implementation of a synergistic designed optical transmitter

In this chapter, the synergistic designed optical transmitter which is analyzed in Ch.5 is demonstrated. After the description of the proposed optical transmitter, the testing result presents this optical transmitter with NRZ data transmitting, bit error ratio (BER) testing and an efficient PAM4 transmitting.

In this implementation, a combinational packaging which including both flip chip bonding approach and wire bonding approach is demonstrated as well.

### 6.1 Introduction

Based on the analysis in Ch.5, the electronic circuit part of optical transmitter is demonstrated with in TSMC 28nm CMOS process. The optical device is provided by the optical designer in research group.

The electronic chip, optical modulator chip and a specific designed silicon interposer is combinational packaged and connected to PCB. Both wire bonding approach and flip chip bonding approach is used in the integration.

Both simulation and testing result demonstrates the optical transmitter is functional up to 40Gb/s with 1.6pJ/bit power efficiency. A BER test demonstrates a real time back to back NRZ data transceiver system until 30Gb/s.

In addition, the optical transmitter also demonstrates the optical transmitter with PAM4 transmitting. The PAM4 transmitting operating speed is up to 25Gbaud/s (50Gb/s) with 2.94 pJ/bit at 4.3dB (1.43dB per eye).

## 6.2 Optical transmitter

The proposed synergistic designed optical transmitter is shown in Fig.6.1, and Table6.1 presents the parameters of major electric components in circuit.

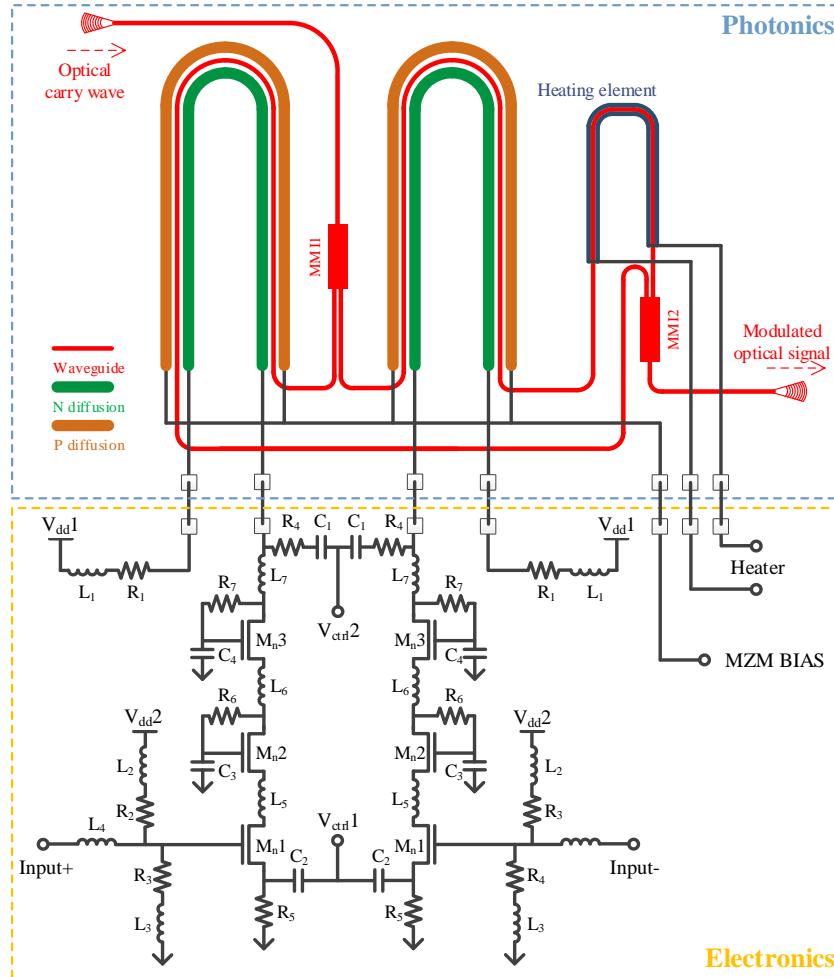


FIGURE 6.1: Schematic of optical transmitter

TABLE 6.1: Parameters of major electric components in optical transmitter

$R_1$	$50\Omega$	$L_1$	$255pH(2.9\Omega)$
$R_2$	$75\Omega$	$L_2$	$113pH(1.2\Omega)$
$R_3$	$150\Omega$	$L_3$	$113pH(1.2\Omega)$
$R_4$	$55\Omega$	$L_4$	$343pH(4.7\Omega)$
$R_5$	$10\Omega$	$L_5$	$255pH(2.9\Omega)$
$C_1$	$16fF - 72fF$	$L_6$	$205pH(2.2\Omega)$
$C_2$	$0.8pF - 2.3pF$	$L_7$	$205pH(2.2\Omega)$
$C_3/R_6$	$1pF/55k\Omega$	$C_4/R_7$	$1pF/55k\Omega$
$M_n1$	$74\mu m/30nm$	$M_n2 - 3$	$84\mu m/30nm$

In the electronic CMOS chip, there is an open drain CML based cascode amplifier and the loading network. The electric model of si MZM could be treated as a transmission line with nominal  $50\Omega$  impedance.

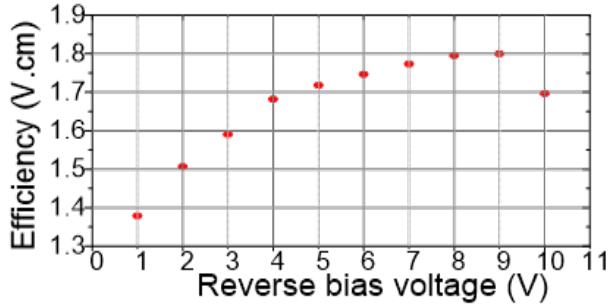


FIGURE 6.2: Measured modulation efficiency under different reverse bias voltage.

The PN junction within the Si MZM is fabricated with doping concentrations of  $3e17cm^{-3}$ ,  $8.5e17cm^{-3}$ ,  $1e20cm^{-3}$ ,  $1e20cm^{-3}$  for n, p, n+, and p+ respectively. As shown in Fig.6.2, the measured DC modulation efficiency is about  $1.4V \times cm$  when reverse biased at 1V and gradually changes to  $1.8V \times cm$  when the reverse bias voltage is 8V. A heating element on si MZM is used to set the quadrature point.

The input network consists of  $L_2$ ,  $L_3$ ,  $L_4$ ,  $R_2$  and  $R_3$  and locates at  $50\Omega$  in the pass band of amplifier.  $V_{dd2} = 0.9V$   $1.1V$  can be slightly varied to optimize the DC bias point of main switching transistor  $M_{n1}$ .  $C_2$  and  $R_5$  is a capacitance degeneration network located at source of  $M_{n1}$ .  $C_2$  is adjustable from  $0.8pF$  to  $2.3pF$  which is controlled by  $V_{ctrl1} = 0V - 1.3V$ . This capacitance degeneration is used for fine tuning the mid-band gain of modulator driver.  $R_4$  and  $C_1$  is a near end termination network. Varying the DC bias voltage  $V_{ctrl2} = 0V - 1.3V$  of an accumulation  $C_1 = 16fF - 72fF$  can fine adjust the near end output impedance above tens of GHz.  $M_{n1}$ ,  $M_{n2}$  and  $M_{n3}$  are three cascode transistors with shunt inductor peaking ( $L_5$ ,  $L_6$  and  $L_7$ ).  $M_{n2}$  and  $M_{n3}$  are self biased by RC networks ( $C_3/R_6$  and  $C_4/R_7$ ). The open drain outputs goes through the U-shape phase shifters and return to the loading network on the CMOS chip and the main power supply  $V_{dd1}$ . The circuit is designed with  $V_{dd1} = 3V$  but it could be varied from  $1.5V$  to  $4.5V$ .

Reverse bias voltage and DC current for heater of MZM is provided via the CMOS chip.

### 6.3 Simulation result

The modulator driver is simulated in the Spectre simulator with an electric model of the electrode (Tx line) on MZM. The MZM electrode model is provided by the optical device designer. The simulation environment is shown in Fig.6.3. The electronic inputs include  $50\Omega$  source impedance. And in the simulation, the  $V_{dd1} = 3V$ ,  $V_{dd2} = 1.05V$ ,  $V_{ctrl1} = 0V$  and  $V_{ctrl2} = 0V$ . The simulation also considers the integration parasitic. At output end and termination end, there are 4 parasitic inductors  $L_{bump} = 25pH$  which estimates the flip chip bonding bumps.

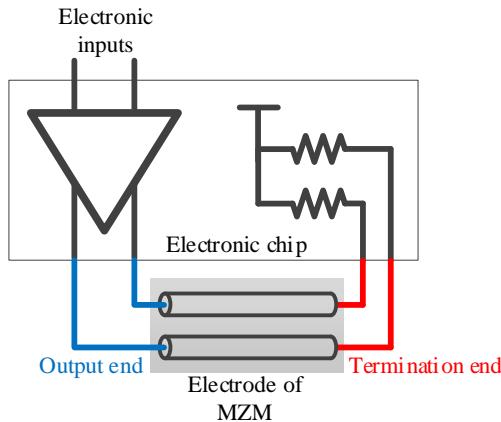


FIGURE 6.3: Electric simulation environment

Fig.6.4 demonstrates the electric AC simulation result of optical transmitter (schematic level). Both AC response at modulator driver output end (before the Tx line on MZM) and termination end (after MZM) is presented. In addition, an estimated equivalent electric-optical (EO) frequency response of optical transmitter which equals to  $(\text{output end} + \text{termination end})/2$  is demonstrated.

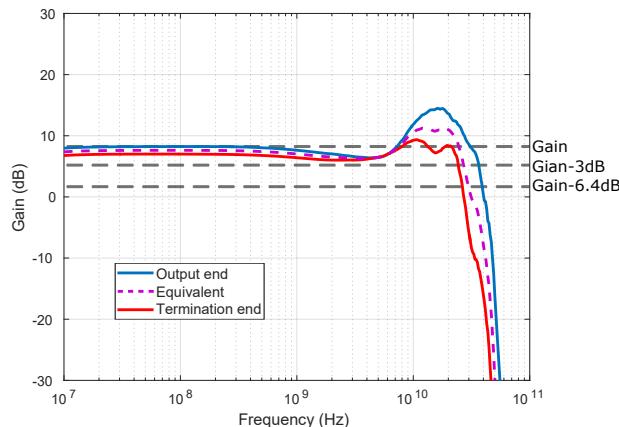


FIGURE 6.4: AC simulation result of U-shape optical transmitter (schematic level)

The mid-band gain of modulator driver is 8.2dB. The bandwidth of the optical transmitter could be treated as  $\text{Gain} - 6.4\text{dB}$  of termination end or  $\text{Gain} - 3\text{dB}$  of the estimated equivalent EO frequency response. In the observed simulation result, the  $\text{Gain} - 6.4\text{dB}$  of termination end is 26.9GHz and  $\text{Gain} - 3\text{dB}$  of the estimated equivalent EO frequency response is 27.5GHz.

Fig.6.5 demonstrates the transient simulation result of the optical transmitter as eye diagrams at 25Gb/s and 40Gb/s. Input amplitude of  $2^{31} - 1$  PRBS signal is 900mVpp. On both data rates, the electric signal preserves the signal integrity after the MZM. Import the observed simulated electric waveform into the optical device model in Interconnection simulator, the optical modulated signal is presented in Fig.6.5(e) and 6.5(f). The optical device model and the simulation environment in Interconnection is provided

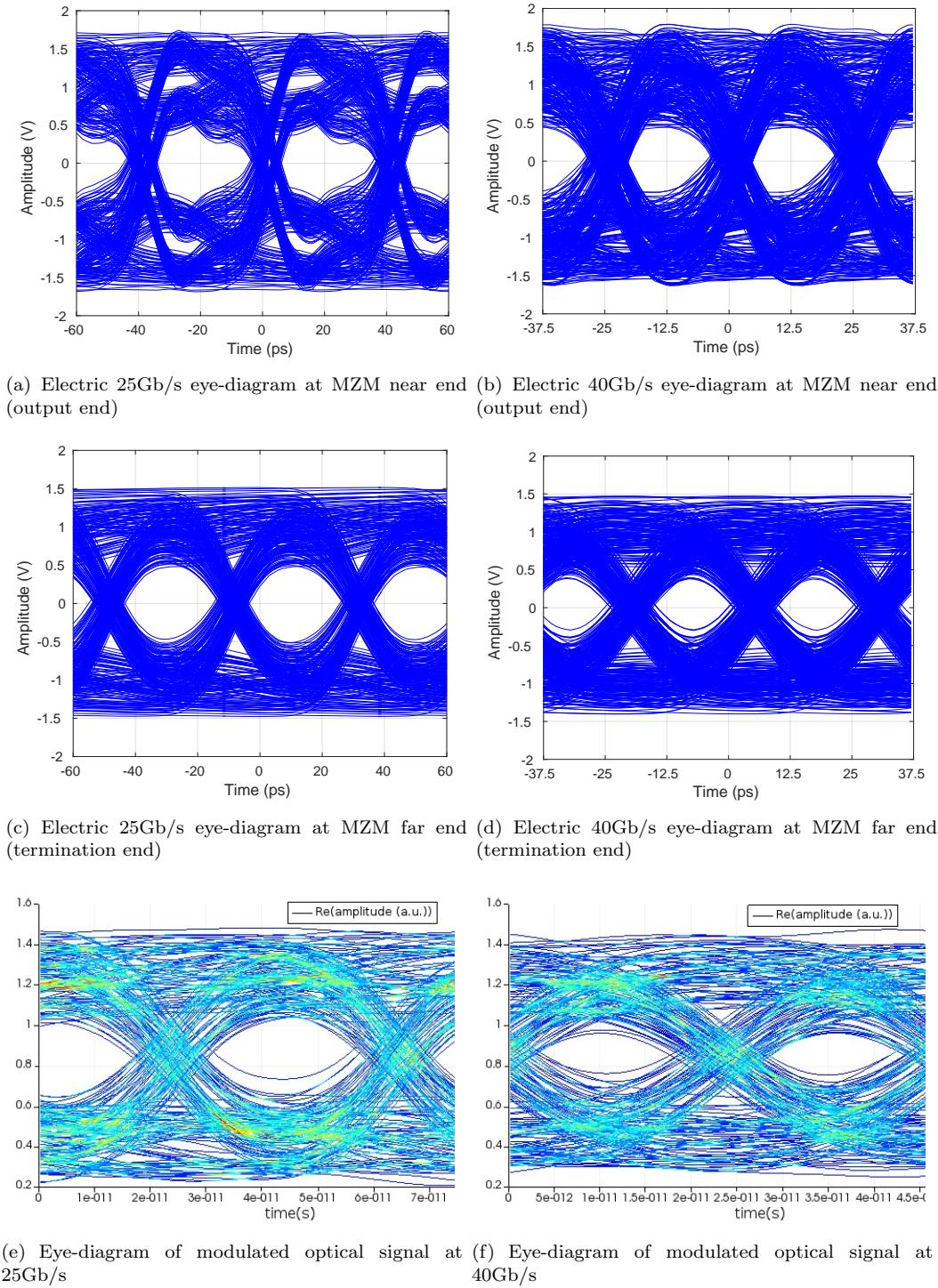


FIGURE 6.5: Transient simulation result of U-shape optical transmitter

by the optical device designer. The observed ER of modulated optical signal in the simulation is  $4.4dB$  at  $25Gb/s$  and  $3.18dB$  at  $40Gb/s$ .

The previous electric simulation results are based on tt corner of the process and temperature is set as  $25^\circ C$ . More specific simulation conditions and an simulation example are presented in App. A. The optical result are based on Lumerical Interconnect simulation software. The input electric signal in Interconnect are extracted from Spectre simulation in Virtuoso.

## 6.4 Package the optical transmitter

The active area cost of CMOS chip is less than  $0.4mm \times 0.8mm = 0.32mm^2$  and the U shape MZM active area cost is less than  $1.2mm \times 0.65mm = 0.78mm^2$ . In order to complete the integrateion of optical transmitter, a additional silicon interposer is designed and fabracated to provide the electric inputs (RF on CPW Tx line and DC from PCB) for modulator driver.

The optical transmitter packaging is combinational multiple platform integration. Gold bump placement, flip chip bonding and wire bonding are all used in the integration process.

### Step 1 Gold bump placement

For later flip chip bonding, gold bumps deposit onto Al pads on CMOS chip. The radius of the gold bumps is approx  $56\mu m$ .

### Step 2 Bottom platform placement

U-shape MZM, silicon interposer and PCB are all mounted onto a flat baseboard. The upper planes of them are on the same height (Solid glue, a high-temperature epoxy, tolerances the height mismatch of them). The interposer's and MZM's PADs are in a horizontal plane, that ensures the modulator driver (CMOS chip with bumps on pads) can be flip bonded.

### Step 3 Flip chip alignment

The CMOS chip is flipped and overlook to the bottom platform. All bumps align to the pads on U-shape MZM and silicon interposer.

### Step 4 Flip chip bonding

Place the CMOS chip onto bottom platform and bonding the CMOS chip onto it. This design uses the thermal compression with ultrasonic approach.

### Step 5 Wire bonding

Connect the power supply and DC control pads on PCB to the silicon interposer. The power supply for PCB are using socket connections at the far end of PCB.

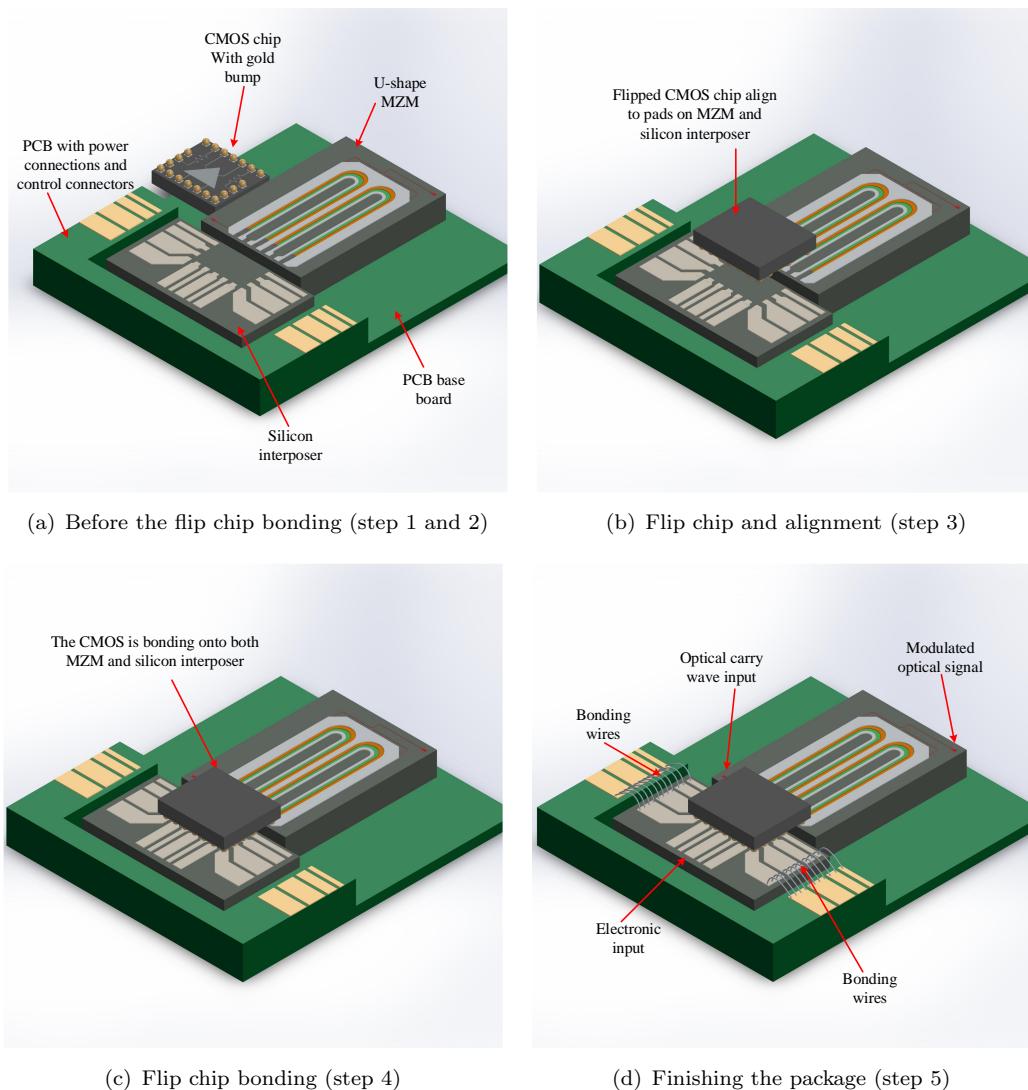


FIGURE 6.6: Combinational integration of the optical transmitter

Fig. 6.7 presents the microscope view of the CMOS chip which has deposited with gold solder bumps, and the packaged optical transmitter. The electronic signal inputs are fed into the optical modulator via transmission lines on the silicon interposer. DC control signals for CMOS chip, reverse bias and heater on MZM provide by PCB. Optical carry wave input and modulated optical signal outputs are fed in and out from MZM via grating couplers.

## 6.5 Testing result

This section includes three parts of testing result on the synergistic designed optical transmitter. On the order of NRZ test, real time BER test on NRZ data and PAM4 transmitting, the optical transmitter is enabling 40Gb/s NRZ and 50Gb/s PAM4 optical transmitting.

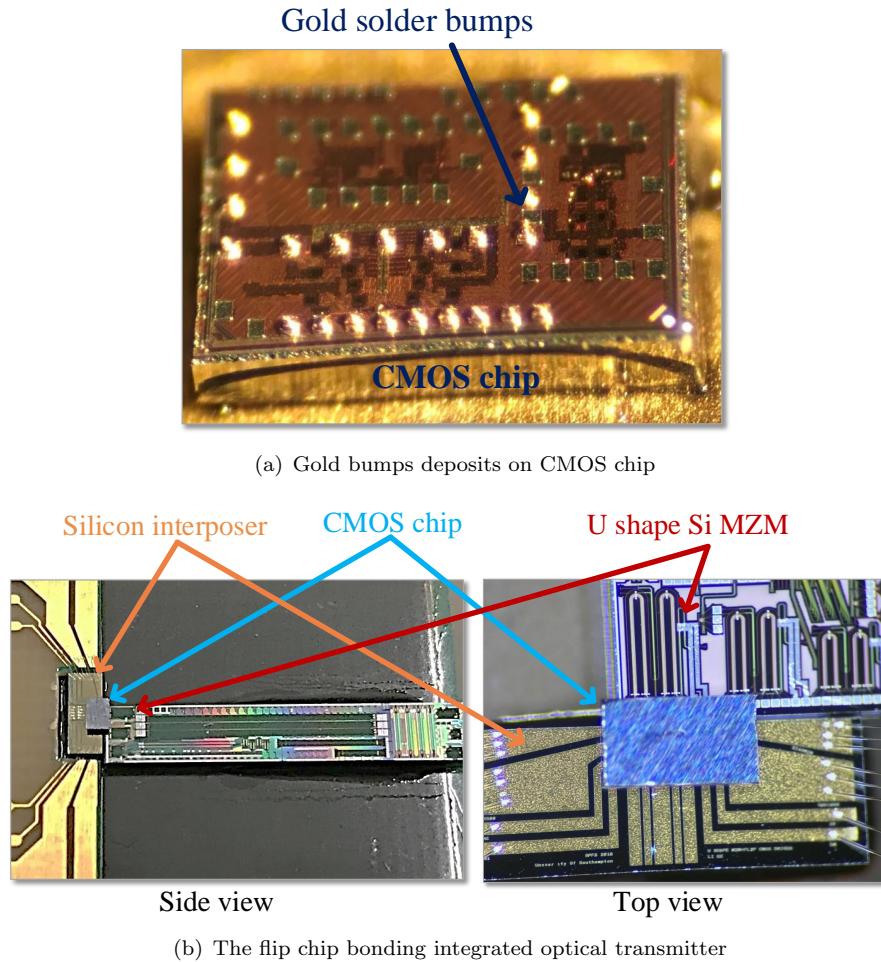


FIGURE 6.7: Transient simulation result of U-shape optical transmitter

### 6.5.1 NRZ transmitter testing

PRBS signal feeds into optical transmitter via RF probe and coaxial cables. The C band optical carry wave is coupled to the optical transmitter as well. Fig.6.8 presents the observed modulated optical signal on DCA via EDFA and fiber.

Within this work, both  $V_{ctrl1} = 0V$  and  $V_{ctrl2} = 0V$ . The reverse bias of MZM is set as  $0V$  meanwhile the reverse bias voltage equals to the modulator driver output DC bias. The heating element is used to set the quadrature point of the Si MZM, which consumes about  $30.6\text{mW}$  power. However, we believe this overhead can be eliminated by applying the trimming process [19] onto the Si MZM in future fabrication runs. Therefore, only the power consumption within the CMOS driver is included in the later power consumption and efficiency calculation.

On the four data rates, only the  $40\text{Gb/s}$  signal integrity is minor compromised due to bandwidth limitation. The observed optical signal is very similar to the simulated result.

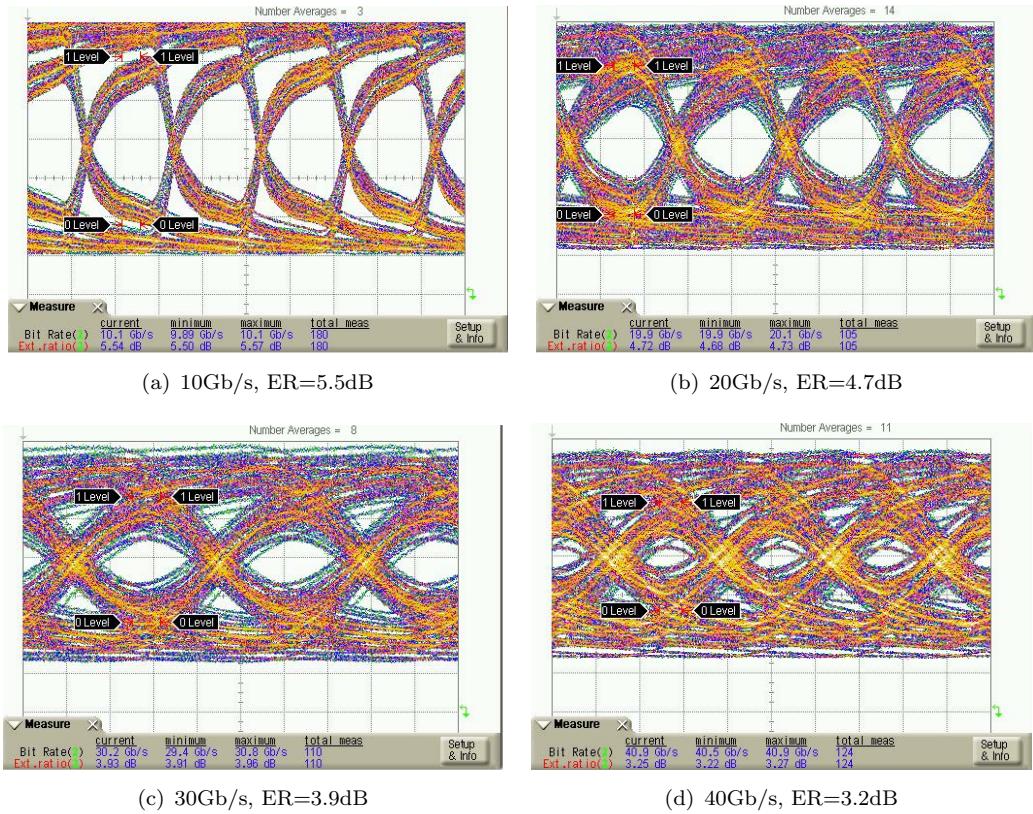


FIGURE 6.8: Transient simulation result of modulator driver

On 40Gb/s, the optical ER=3.2dB and power consumption is,

$$\begin{aligned}
 P &= V_{dd1} \times V_{dd1} + V_{dd2} \times V_{dd2} \\
 &= 3V \times 27mA + 1.05V \times 9mA \\
 &= 90.45mW
 \end{aligned}$$

Due to measurement equipment limitation, the EO bandwidth of the optical transmitter cannot be directly measured. Therefore, in order to describe the EO bandwidth of the optical transmitter, the modulated optical signals on different data rates are recorded and summarized as shown in the Fig.6.9. While the operating data rate is grandly increased (electronic inputs are always 900mVpp), the modulated optical signal ER reduces. After 40Gb/s, the signal integrity is compromised due to bandwidth limitation. In this work, the DC power supply  $V_{dd1} = 3V$ , and  $V_{dd2} = 1.05V$ .

The modulator driver also supports to adjust the main power supply ( $V_{dd1}$ ) from 1.5V to 4.5V. Fig.6.10 presents the observed ER of the modulated optical signal at 25Gb/s with different power supply. To note, Fig.6.10, the x-axis of power consumption and efficiency is not linear increasing but just a record corresponding the increasing power supply. The increasing ER is saturated after  $V_{dd1} = 3.5V$  due to the output amplitude is saturated and the reverse bias voltage is increasing which compromises the output

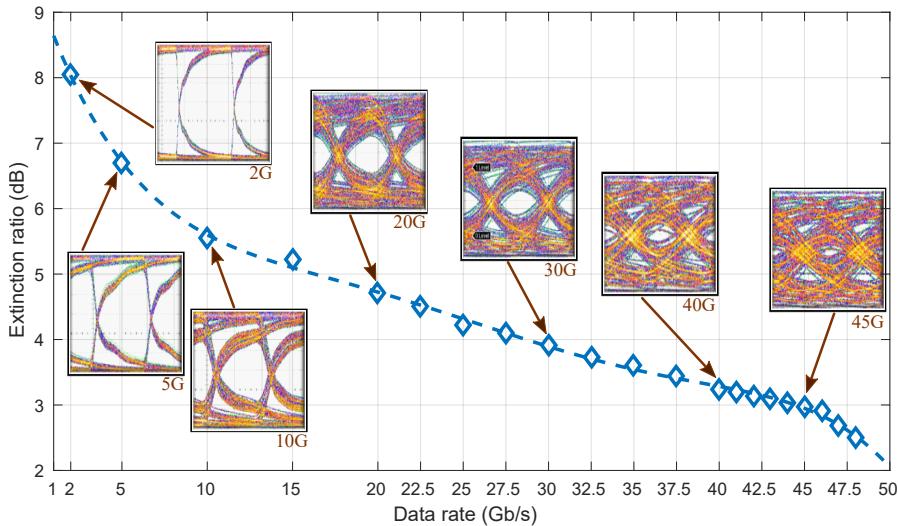
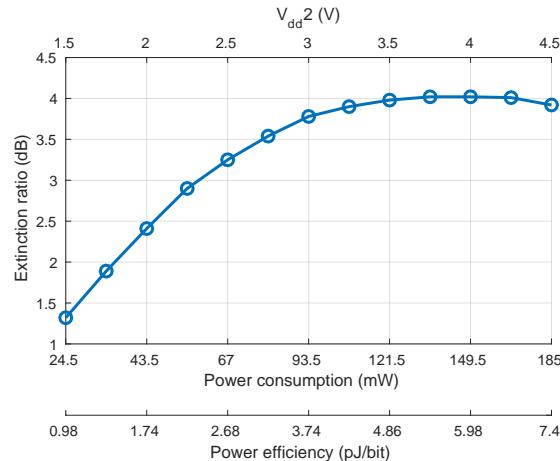


FIGURE 6.9: ER of optical transmitter under different operating data rate

ER.


 FIGURE 6.10: ER at 25Gb/s with  $V_{dd}2$  gradually increase from 1.5V to 4.5V

In the test, varying the main power supply  $V_{dd}1 = 2.5V$  with  $40Gb/s$  input PRBS signals, the observed modulated optical signal  $ER = 3dB$  which satisfies the ER requirement of the NRZ interconnection. The recorded power of this test is,

$$\begin{aligned}
 P &= V_{dd}1 \times I_{dd}1 + V_{dd}2 \times I_{dd}2 \\
 &= 2.5V \times 22mA + 1.05V \times 9mA \\
 &= 64mW
 \end{aligned}$$

and the power efficiency of the optical transmitter at 40Gb/s data rate is,

$$\begin{aligned}
 FOM &= P/\text{data rate} \\
 &= 64\text{mW}/40\text{Gb/s} \\
 &= 1.6\text{pJ/bit}
 \end{aligned}$$

And in Fig.6.11, it is the DCA observed eye diagram of modulated output signal at this operating point.

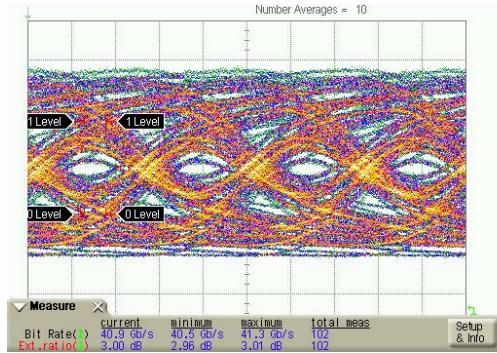


FIGURE 6.11: Optical transmitter outputs 40Gb/s with 1.6pJ/bit

### 6.5.2 BER testing

The bit error ratio (BER) testing is applied onto this optical transmitter. Fig.6.12 illustrates the BER testing environment. This BER test is a real time BER test, not a off-line equalized result. Therefore, this BER test result can be seen as a reliable back to back Connection without DSP equalizations. Fig.6.12 illustrates the BER test setup.

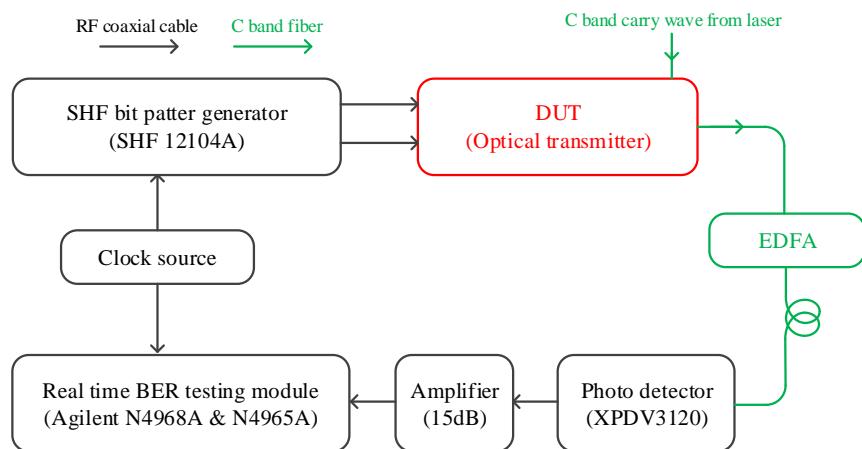


FIGURE 6.12: The BER testing setup

PRBS data is generated in SHF bit patter generator and fed into design under test (DUT) and modulated onto the optical carrier. The modulated optical signal amplifies in EDFA and demodulates by PD. An electronic amplifier amplifies the output of PD

to appropriate amplitude to fit the input requirement of the BER testing module. The real time BER testing module and PRBS source data generator is drove by the same clock source.

Because of the limitation of clock jitter of BER testing module, the BER testing is running up to 30Gb/s. Fig.6.13 is the BER result of this optical transmitter on 20Gb/s, 24.8Gb/s and 30Gb/s.

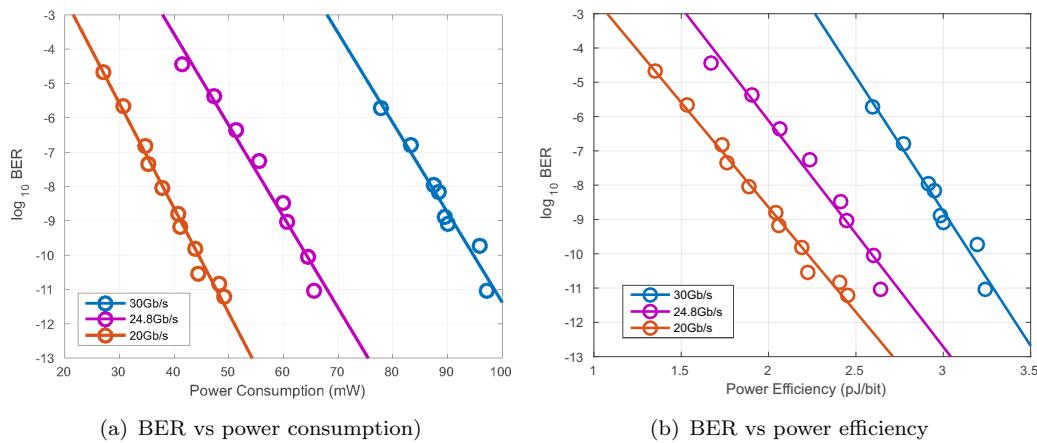


FIGURE 6.13: BER result of the optical transmitter

Due to the pre-FEC BER of the optical transmitter at 25Gb/s could being lower  $10^{-12}$ . The optical transmitter could satisfy and be a part of the 25 Gigabit Ethernet communication which fits the 802.3by standard.

In the BER test, the transceiver system without equalizer and additional DSP systems (pre-FEC), the error free transmitting requires the BER lower or close to  $10^{-12}$ . But in a commercial communication links with equalizer and additional DSP systems, a BER lower than  $2.3e-4$  will be acceptable. The BER of the proposed optical transmitter is related to the power consumption of the modulator driver (via adjust the power supply). In the usual BER testing of optical transmission, the X-axis unit is optical modulation amplitude (OMA). But this is a low power design which needs to prove the relationship between BER and power consumption (Fig.6.13(a)) in the interconnection environment. In the testing, the optical transmitter works with the fixed power of the laser carrier, fixed transmission channel and fixed receiver. In different transmission data rate, the  $V_{dd2}$  is grandly reduced to detect the BER under different power consumption. Therefore, the X-axis unit of the BER result is power consumption of the optical transmitter and its power efficiency. The BER increases within the same slope at the different speeds while the power consumption of the optical transmitter is reducing. In order to investigate the relationship between the BER and power efficiency of the optical transmitter, Fig.6.13(b) also transforms the x-axis as the power efficiency.

Table6.2 summarizes the power efficiency improvement leads to a penalty of orders of BER level in different speed.  $\frac{\text{Power increase ratio}}{\text{BER order improve}}$  in table and slopes of three curve in

TABLE 6.2: Power efficiency increase leads BER improve

Data rate	20Gb/s		24.8Gb/s		30Gb/s	
	Worst	Best	Worst	Best	Worst	Best
BER (log10)	-4.66	-11.20	-4.44	-11.04	-5.70	-11.05
FOM(pJ/bit)	1.35	2.45	1.67	2.64	2.60	3.24
BER order improve	6.54		6.6		5.35	
Power increase ratio	44.9%		36.7%		19.7%	
<i>Power increase ratio</i> <i>BER order improve</i>	6.87%		5.56%		3.68%	

Fig.6.13(b) illustrates BER improve costs less power efficiency with higher transmission data rate.

### 6.5.3 PAM4 testing

According to the efficient PAM4 optical transmitter analysis in Sec.5.4, the proposed optical transmitter could use the independent arms of phase shifters and modulator drivers to demonstrate the PAM4 transmission. The abstract of this PAM4 optical transmitter is presented in Fig.6.14.

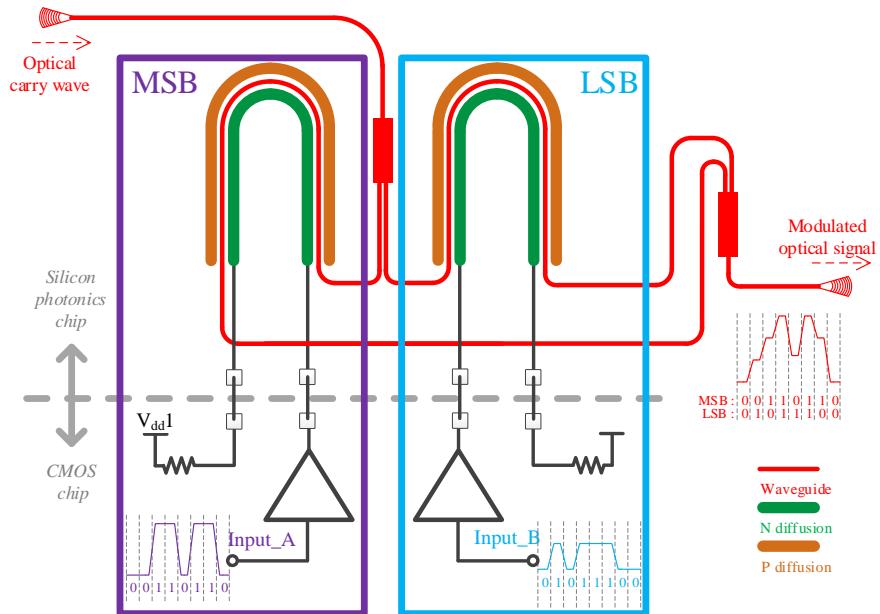


FIGURE 6.14: The PAM4 transmission on the synergistic designed optical transmitter

The independent two arms of input NRZ signals are provided from the BPG with programmable voltage swings. The other measurement setup is the same as the NRZ test. Main power of the PAM4 test is located at 4V.

DCA observed PAM4 testing result are plotted in Fig.6.15. The modulated PAM4 requires two independent data inputs with appropriate amplitude. The input amplitudes and optical ER are clearly labeled aside of the PAM4 eye-diagram. This PAM4 optical

transmitter is error less until 50Gb/s without DSP. The ER of PAM4 result could arrive 4.3dB (1.43dB per eye).

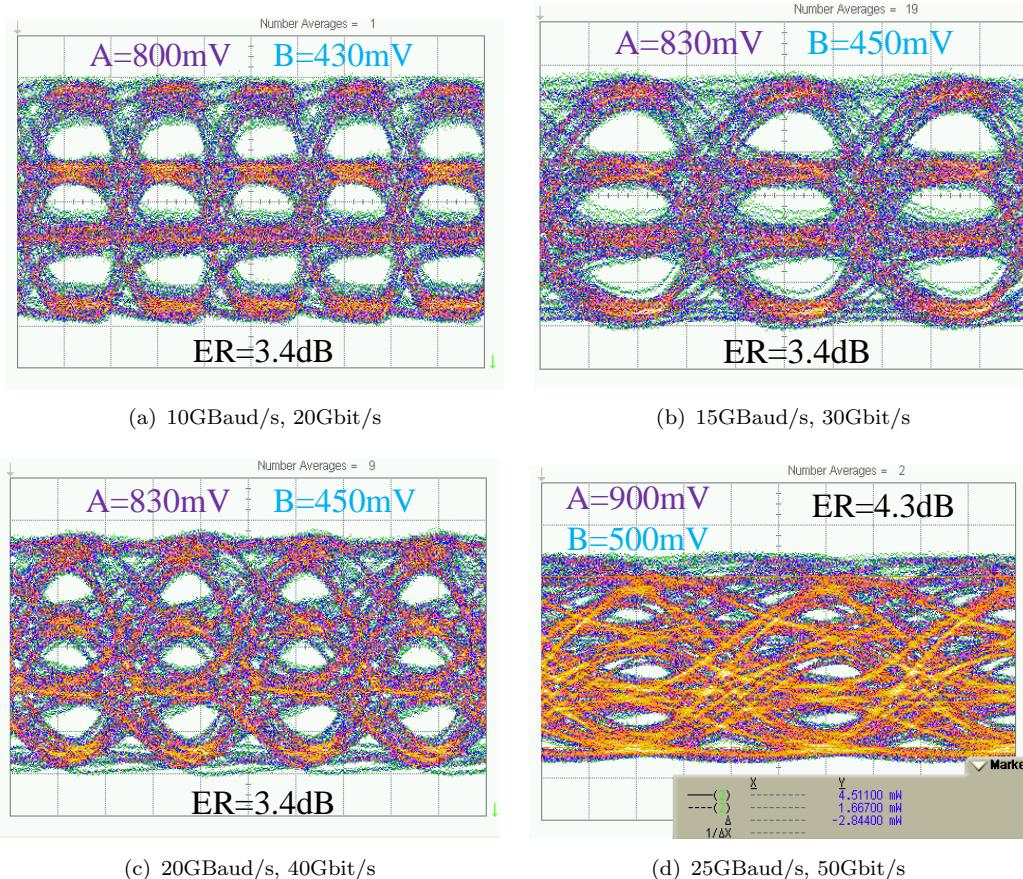


FIGURE 6.15: PAM4 result of the optical transmitter

The power supply of the PAM4 testing on 50Gb/s is  $V_{dd2} = 4V$  at  $I_{dd2} = 34mA$  and  $V_{dd1} = 1.1V$  at  $I_{dd1} = 10mA$ . The power consumption is,

$$\begin{aligned} P &= V_{dd2} \times I_{dd2} + V_{dd1} \times I_{dd1} \\ &= 147mW \end{aligned}$$

And the power efficiency of this PAM4 optical transmitter is,

$$\begin{aligned} FOM &= P/\text{data rate} \\ &= 147mW/50Gb/s \\ &= 2.94pJ/bit \end{aligned}$$

## 6.6 Analysis

Due to the synergistic design method, the MZM is embedded into the CMOS circuit in this design. Based on the optical device simulation platform which is provided by the optical device designer, both electric and optical simulation results are presented. The test result and the simulation result are very close which proves the correctness of the synergistic design method.

As Sec.5.3.1 has mentioned, though the output DC bias of modulator driver is increasing along the MZM until the termination end, in both simulation and the test result, the signal integrate is not affected due to the DC shift is less than 160mW.

The other issue is that during the real-time BER testing, the reliability of the test bench is quite essential. Especially while we tested the errorless results, each testing sample result takes tens of minutes, any unreliable like shaking on fiber which is coupled to the optical transmitter could ruin the current test. In the future, optimize the reliability of the packaging for the real-time test may should be increasing considered.

## 6.7 Summary

The modulator driver is designed in a 28nm CMOS process and integrated to the special designed U-shape MZM to compose the optical transmitter. The packaging of the proposed optical transmitter which avoids all of the off-chip components is combinational of wire bonding, gold bump placement and flip chip bonding.

The efficiency of the optical transmitter with NRZ is as low as 1.6pJ/bit at 40Gb/s. The output optical ER can be adjusted in a wide range with turning the power supply of the modulator driver. A BER test of back to back transcending is demonstrated as well.

An efficient PAM4 optical transmitting experiment is also presented in this chapter as well. The efficiency of the PAM4 signal at 25Gbaud/s (50Gb/s) is 2.94pJ/bit.



## Chapter 7

# Theoretical Analysis of Temperature Variation Tolerance Modulator Driver

This part of research work was indeed conducted at the very earlier period of this PhD project. At the time we opened this research project, the initial challenge is that we cannot find a comprehensive electrical model for the silicon modulator that the driver needs to be coupled with. Therefore, rather than design a general purpose CMOS driver, we, therefore, chose the temperature compensation technique as the starting point of this PhD project.

Temperature performance is such an important characteristic that almost all the semiconductor devices must be characterized within the relatively wide temperature range. The temperature variation issue of optical device has been widely analyzed in the many research works[83], whereas not so many works have ever focused on the electrical components that coupled to the optical devices. In this part of work, a relatively old CMOS process(IBM 130nm CMOS) was chosen. This is mainly because of the affordable fabrication cost and the fact that mature temperature models have been integrated with all the device types(transistors, resistors, capacitors) in this process.

### 7.1 Introduction

Compared with silicon ring modulator, silicon Mach-Zehnder Modulators (MZM) is much more tolerant to the temperature variation, although it is always criticized for the relatively large power consumption (hundreds mW) associated with the driver circuit that MZM couple with. However, temperature variation will become a notable issue when the power density increases. Even if we may exaggerate assume that per-

formance of silicon MZM is stable within a wide temperature range, the fact is that overall performance of the optoelectronic transmitter may still significantly affected by the performance drop of the electrical driver only.

An example schematic diagram of modulator driver integrated with an MZM is given in Fig.7.1. The modulator driver is composed of a pre-driver and output buffer. The overall gain of the modulator driver is accumulated in the stages of the pre-driver, and the modulated optical signal of MZM is determined by the voltage swing of the output stage.

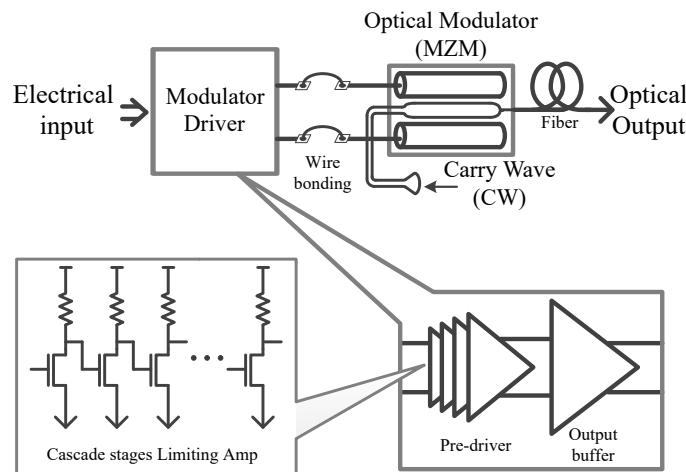


FIGURE 7.1: Modulator driver integrated with optical modulator

The conventional solution for a temperature tolerance driver is dual-loop automatic power control. [62] uses a PD on the transmission side to provide a feedback network. This not only creates more cost regarding the optical device, the feedback is of high complexity. [59] provides another solution without PD, however this is high cost and requires a high level of power due to the peak detector in the electrical design.

In this chapter, a method for creating a low cost temperature tolerance modulator driver is introduced with theoretical analysis. The performance of the amplifier is directly related to temperature without PD or a peak detector.

## 7.2 Temperature analysis of device and circuit

Successfully implementing a temperature variation tolerant amplifier rely on the deep understanding of temperature properties of all the components that are used within the circuit. The temperature model provided by the IBM 130nm CMOS process has an upper limitation at  $150^{\circ}\text{C}$ . Therefore, the characteristic of all the devices(resistors transistor, etc) were analyzed by running the DC operating point analysis from the nominal room temperature  $27^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ . It is found that the resistance of a ploy based resistor is increased only 2.5% within this temperature range, whereas the characteristic of active

devices(CMOS transistors) varies considerably that must be carefully quantified with following design example.

### 7.2.1 Temperature analysis of CMOS transistors

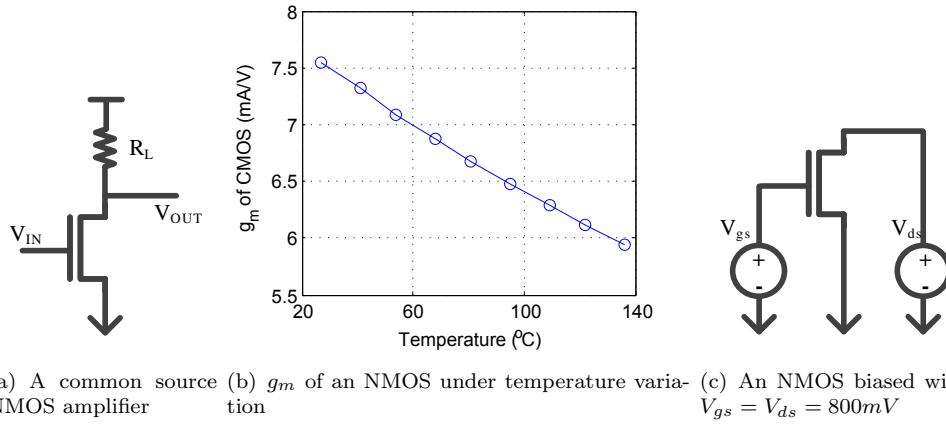
The temperature effects on CMOS transistors have been deeply analyzed in [83; 94]. The physical mechanism behind this is out of scope of this thesis. As a circuit designer, the most straightforward approach is simulation devices under different temperatures.

In an amplifier, the pass-band gain is given by,

$$A_v = G_m \cdot Z_{out} \quad (7.1)$$

In a common source NMOS amplifier with a resistance load as shown in Fig.7.2(a), the  $G_m$  is the transconductance,  $g_m$ , of the transistor and  $Z_{out} = R_L \parallel r_o \approx R_L$ . It has been mentioned the passive component under temperature variation is tolerant; hence the  $g_m$  is researching object.

Fig.7.2(b) is the  $g_m$  of an NMOS ( $W=10\mu m$ ,  $L=120nm$ ), in which  $V_{gs}$  and  $V_{ds}$  are biased at  $800mV$  (Fig.7.2(c)), while temperature grandly increases from  $27^\circ C$  to  $135^\circ C$ .



(a) A common source NMOS amplifier (b)  $g_m$  of an NMOS under temperature variation (c) An NMOS biased with  $V_{gs} = V_{ds} = 800mV$

FIGURE 7.2: Schematic of two individual stage of example limiting amplifiers

From  $27^\circ C$  to  $135^\circ C$ , the  $g_m$  reduction is more than 20%. Assuming this NMOS is used in a common source amplifier, the DC gain loss of the amplifier is approximately equal to the  $g_m$  reduction. In this condition, to provide 5 stage cascade gain limiting amplifier under temperature variation, there will be over 70% (almost 5dB) of loss in overall gain.

$f_T$  (the transistor transitions from an amplifier to an attenuator) to current density ( $I_{ds}$ ) characteristic of transistor is a general method used to describe the frequency response ability of transistors.[92]

$f_T$  curve presents the frequency performance of the transistor while frequency response of  $|i_d/i_g|$  is located at 0dB.  $|i_d/i_g|$  response to frequency curve also decides amplifier

frequency response after the first pole and it is given by,[92]

$$v_{gs} = \frac{i_g}{j\omega \cdot (C_{gs} + C_{gd})}$$

$$i_d = g_m \cdot v_{gs}$$

$$\left| \frac{i_d}{i_g} \right| = \frac{g_m}{2\pi f \cdot (C_{gs} + C_{gd})} \quad (7.2)$$

$f_T$  is the frequency while  $|i_d/i_g| = 1$  in Eq.7.2. Due to  $C_{gs} \gg C_{gd}$ , while gain locates at 1,

$$\left| \frac{i_d}{i_g} \right| \approx \frac{g_m}{2\pi f \cdot C_{gs}} \propto \frac{\beta_{eff} \cdot V_{DS,sat}}{L^2} \quad (7.3)$$

Fig.7.2(b) presents the  $g_m$  of an NMOS under temperature variation. It could be conjecture,  $f_T$  will reduce due to  $g_m$  reduction in high temperature.

Fig.7.3 is the  $f_T$  to current density characteristic of an NMOS ( $W = 10\mu m$ ,  $L = 120nm$ ).

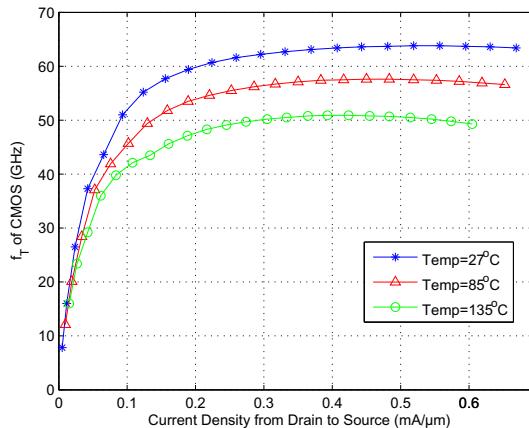


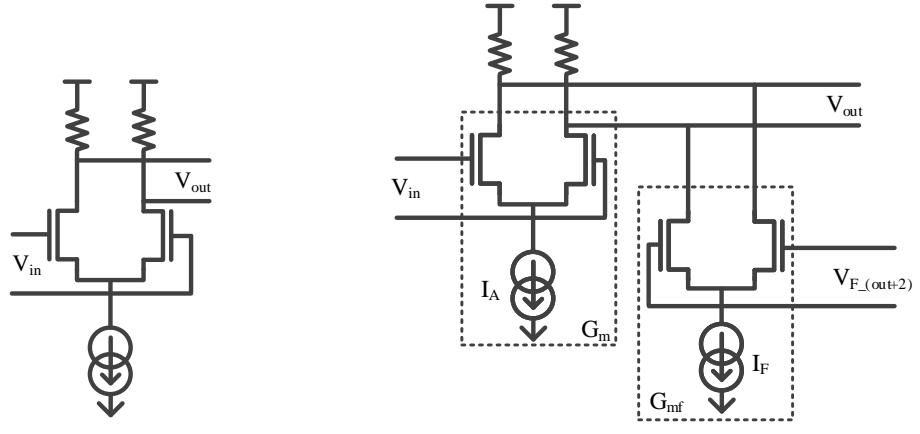
FIGURE 7.3:  $f_T$  of a NMOS in temperature variation

This NMOS is biasing at  $V_{ds} = 800mV$  and loading an NMOS as the same size of the NMOS under research. In three temperature conditions, while current density is  $0.4 \pm 0.2mA/\mu m$ ,  $f_T$  is saturated. But, while temperature is increasing, the peaking  $f_T$  is reducing. This reduction is directly related to  $g_m$  loss under high temperature. In this process, it is close to 20% which meets the DC operant analysis of  $g_m$ .

### 7.2.2 Temperature analysis of limiting amplifiers

This section explains the performance loss of cascade amplifiers (limiting amplifiers) under temperature variation.

The first example is a five stage limiting amplifier with NMOS common source amplifier with resistance load. Fig.7.4(a) is one stage of the limiting amplifier. Under the room



(a) Standard differential common gate amplifier (b) A differential amplifier with 2nd order active feedback

FIGURE 7.4: Schematic of two individual stage of example limiting amplifiers

temperature,  $27^\circ C$ , input and output DC bias is set the same as 900mV, the current density of NMOS is  $0.22mA/\mu m$ , and the DC gain of each stage is 2 ( $6dB$ ). The last stage output load is a capacitance load which is equal to  $C_{gs}$  of NMOS in used.

Fig.7.4(a) presents the frequency response under temperature variation of first example. Clearly, due to  $g_m$  of NMOS losses in high temperature,, and overall DC gain simultaneously reduces. In this five stage amplifier, overall DC gain is reduced from  $28.7dB$  to  $20.7dB$ . The slope of the frequency band after  $\omega_0$  is similar under increasing temperature.

The second example is another five stage limiting amplifier with amplifier cell as shown in Fig.7.4(b). In this amplifier, an active feedback  $G_{mf}$  is  $1/10$  of amplify  $G_m$  ( $I_A = 10 \cdot I_F$ , width of amplify NMOS and feedback NMOS is also 10:1) is inserting into the amplifier. Under room temperature ( $27^\circ C$ ), input and output DC bias is set the same as 742mV, and the mid-band gain of each stage is 1.35 ( $2.6dB$ , active feedback limits the voltage gain but optimizes bandwidth). The last stage output load is a capacitance load which is equal to  $C_{gs}$  of the common source amplifier NMOS in use.

Fig.7.4(b) presents the frequency response of this limiting amplifier with active feedback. The bandwidth has been enhanced to 20GHz and above. In the reason of  $G_m$  and  $G_{mf}$  are both reduced under high temperature, DC gain lost in five stage is  $4.5dB$ , and bandwidth lost is over  $7GHz$ .

Summarizing all the above, in high temperatures, both performance on bandwidth and gain of cascode amplifier reduce which causes by  $g_m$  lost. In the cascade amplifier, the lost effect is the exponential growing because of multiple stages.

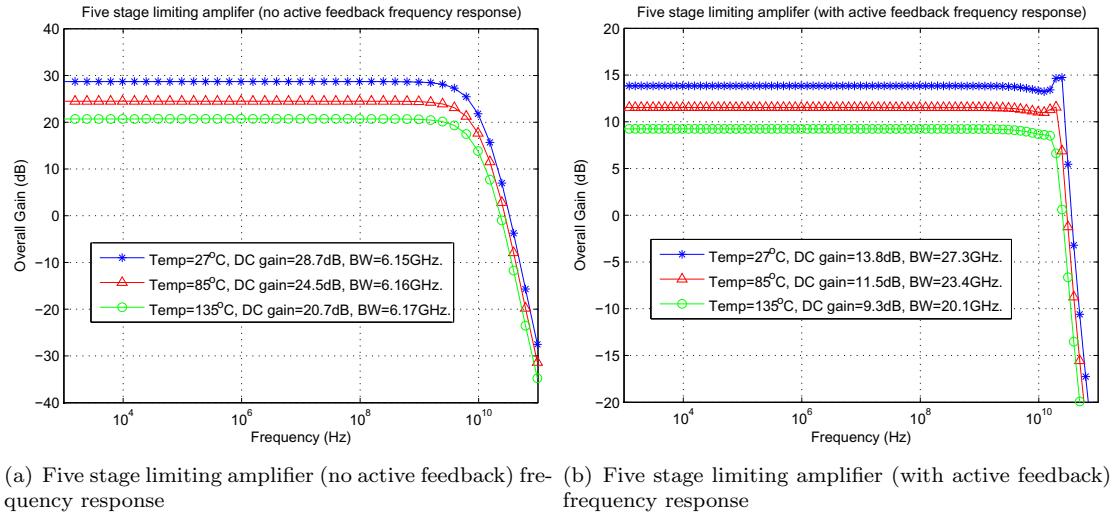


FIGURE 7.5: Frequency response plot of example limiting amplifiers

### 7.3 Temperature variation tolerance limiting amplifier

In high temperatures, both gain and bandwidth of CMOS amplifier reduces due to  $g_m$  lost. Thus, a classic amplifier circuit with a temperature variation tolerance system is developed. It is shown in Fig.7.7 as a limiting amplifier cell with second order active feedback.

Transfer function [11] is given by,

$$H(s) = \frac{A_0^3}{(1 + \frac{s}{\omega_0})^3 + A_0^2\beta} = \frac{G_m^3 \cdot R_L^3}{(1 + sR_L C)^3 + G_m^2 G_{mf} R_L^3} \quad (7.4)$$

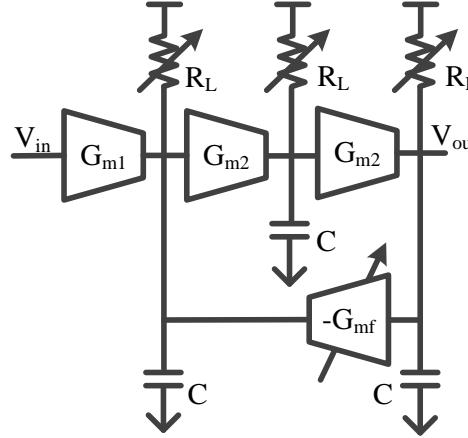


FIGURE 7.6: Topology level analysis of temperature variation tolerance system on a second order active feedback amplifier

Assume the characteristics of all components are adjustable while temperature increases, in order to repair the mid-band gain, the increasing  $R_L$  will compensate the lost of  $G_m$

$(g_m)$ .

The active feedback creates one more pole in the denominator. Increasing  $G_{mf}$  while temperature increases could move the pole and optimize the effect which could repair the bandwidth of limiting amplifier.

The disadvantage of the adjustment  $G_{mf}$  to repair the bandwidth is the increased jitter on the signal.  $G_{mf}$  is directly affecting the additional pole which generates a frequency response peaking around  $\omega_0$ . In high temperature, the increasing  $G_{mf}$  intensifies the peak on frequency response which may be causing extra jitter on the transmission signal.

To implement this topology in Fig.7.6 onto CMOS circuit, see Fig.7.7.

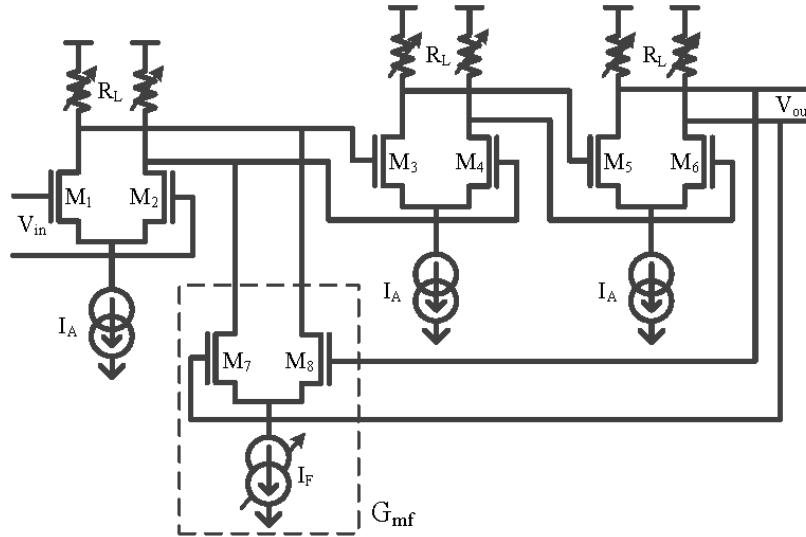


FIGURE 7.7: Temperature variation tolerance system on second order limiting amplifier

With this example circuit,  $M_{7-8}$  and a controlled current source  $I_F$  compose the  $G_{mf}$ .  $M_{1-6}$  are biased with a fixed current source  $I_A = 3.7mA$ . And loading of the amplifier is the adjustable resistance load  $R_L$ . In this example, two adjustable part in the circuit,  $R_L$  and  $I_F$  are linear to temperature variation,

$$R_L = 300\Omega + k_1 \cdot (\text{temperature} - 27^\circ C), \quad k_1 = 1\Omega/\text{ }^\circ C; \quad (7.5)$$

$$I_F = 0.18mA + k_2 \cdot (\text{temperature} - 27^\circ C), \quad k_2 = 0.8\mu A/\text{ }^\circ C \quad (7.6)$$

The compensation of  $I_F$  increment from  $27^\circ C$  to  $135^\circ C$  is 47%. Simultaneously,  $R_L$  increment is around 30% which includes the compensation of  $g_m$  reduction and further gain loss causing by increasing  $I_F$  in high temperature.

This temperature variation tolerance system example is based on a 130nm CMOS process. In another CMOS process, the topology of the circuit could be the same but the coefficient and constant should be different.

In three temperatures, details of this circuit are shown in Table 7.1. While temperature increases, the ratio of  $I_A/I_F$  increases from 20.7 : 1 to 13.8 : 1. It increases the peak created by the additional pole in the transfer function, which will also generate more jitter on the signal.

TABLE 7.1: Detail of temperature variation tolerance system example  
 Constant with temperature variation

$I_A$	3.7mA		
$M_1 - M_6$	LvtNMOS, $W = 10\mu m$ , $L = 120nm$		
$M_7 - M_8$	LvtNMOS, $W = 2\mu m$ , $L = 120nm$		
$C_L$	$11.25fF (\approx C_{gs} \text{ of } M_1)$		
Adjustable with temperature variation			
Temperature	27°C	85°C	135°C
$R_L$	308Ω	349Ω	402Ω
$I_F$	178μA	222μA	268μA
$I_A/I_F$	20.7 : 1	16.7 : 1	13.8 : 1

Fig. 7.8(b) presents the frequency response of the limiting amplifier with temperature variation tolerance system. Fig. 7.8(a) presents the same circuit but  $R_L = 308\Omega$  and  $I_F = 178\mu A$  fixed at all temperature conditions.

Clearly, with temperature variation tolerance system, there is no loss of DC gain. And bandwidth loss of amplifier is optimized than the previous example. But, with higher temperature, the peak in frequency response close to  $\omega_0$  increases from the lower temperature. It generates a peak on group delay, and increases it in high temperature. This peak both repairs the bandwidth of amplifier and creates more jitter on signal.

In summary, with the proposed temperature variation tolerance system in a limiting amplifier, the performance of amplifier can be maintained. In the implementation, limiting the feedback to limit the jitter on the signal is important.

## 7.4 Temperature variation tolerance output stage

In the previous section, a temperature variation tolerance limiting amplifier is presented. As mentioned at the beginning, the modulator driver is composed of a limiting amplifier as pre-driver stage and output driver as the final stage. This section compares two output stage circuit topologies to provide a better temperature tolerance selection.

To assess the impact of temperature comparisons are made between a current mode logic amplifier and a cascode push pull amplifier (which can achieve  $4V_{pp}$  differential voltage swing). The current mode logic amplifier in Fig. 7.9(a) is driving a  $50\Omega$  termination with biasing. In Fig. 7.9(b), there are two inputs in a cascode push pull with a  $50\Omega$  AC termination. Both topologies are tested with the same input voltage swing ( $V_{in} = 1V_{pp}$ ), and output swing (single rail) is observed to be higher than  $2V_{pp}$  at room temperature.

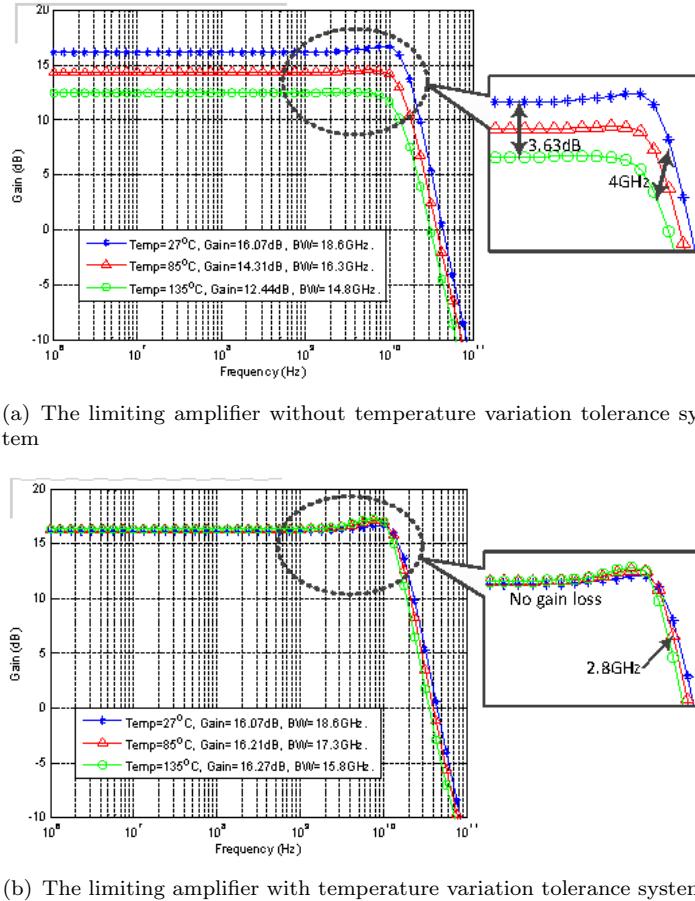


FIGURE 7.8: Frequency response of limiting amplifier with and without temperature variation tolerance adjustment

Fig. 7.10 presents the electrical voltage swing of both topologies under a wide temperature range. At a high temperature, the gain loss of the current mode logic circuits result in a reduction of  $g_m$  in the NMOS device. At 135°C, the output voltage swing is reduced to 1.6V (25% loss). In contrast, the cascode push pull architecture suggests much higher gain should be achieved but behaves as a buffer in this case. Most of the output voltage swing loss in a cascode push pull circuit is headroom limitation which is around 5% (150mV) in this comparison. Though optical devices are not included in this comparison, MZM are also independent of temperature variations, therefore, the extinction ratio of integrated optical transmitter could be related to the electric device output swing.

At a high temperature, the bandwidth of both topologies is reduced. To maintain the bandwidth on output stage requests feedback or control loop which is complex and increases the parasitic on the output stage. In order to achieve a low cost design, the output stage should be kept as simple as possible. Therefore, the cascode push pull provides enough tolerance on temperature variation as a modulator driver output stage.

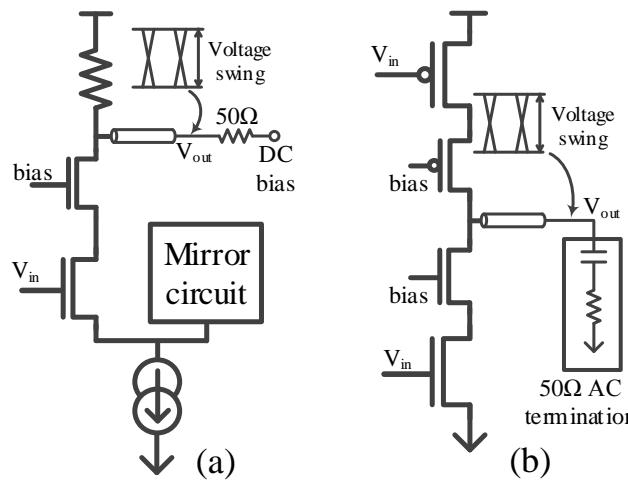


FIGURE 7.9: Output stage of (a) current mode logic and (b) cascode push pull

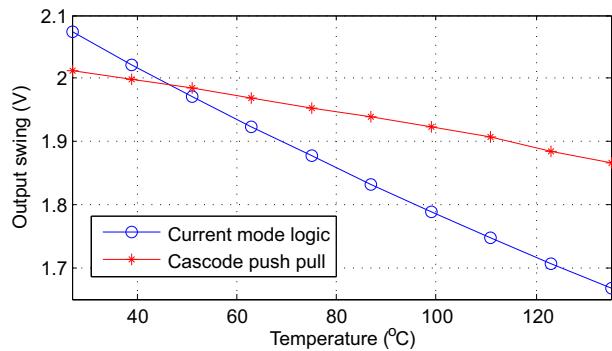


FIGURE 7.10: Voltage swing of output stage

## 7.5 Summary

Though the methodology provided in this chapter is not completely lossless on performance when compared with [59; 62], the tolerance under temperature variation of modulator driver is improved. Consider about the cost of implementable circuit, the methodology provided in this chapter is more efficient than the reviewed solutions.

With a temperature variation tolerance limiting amplifier and cascode push-pull output stage, in Ch.8, a modulator driver driver is demonstrated in IBM 130nm CMOS process.

# Chapter 8

## Implementation of Temperature Variation Tolerance Modulator Driver

Theoretical analysis in Ch<sup>7</sup> proposes a efficient temperature variation tolerance method for modulator driver design. In this chapter, a modulator driver design includes the temperature variation tolerance system is demonstrated in a 130nm CMOS process. With an on-chip temperature sensor with its control loop, the temperature variation tolerance system is related to temperature without PD or general power control system.

### 8.1 Introduction

This modulator driver is designed for a nominal  $50\Omega$  push-pull MZM. It includes a temperature tolerance pre-driver and push pull output stage. To complete a temperature tolerance system with automatic control loop without general power control system, an on-chip temperature sensor with control loop are designed as well.

This modulator driver is demonstrated on IBM 130nm CMOS process.

In the simulation, the modulator is functional up to 12.5Gb/s with 4Vpp output swing. In the testing, 8Gb/s data transmission is observed. Power consumption of this modulator driver is 377mW.

#### 8.1.1 Top level design

The top level schematic of this modulator driver is shown in Fig.8.1.

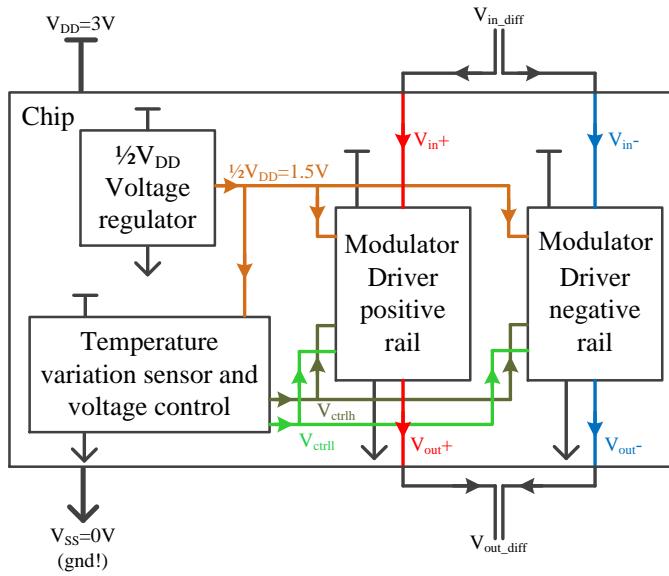


FIGURE 8.1: Top level of temperature variation tolerance modulator driver system

$V_{DD}$  of this system is a 3V DC power supply. The descriptions of these sub-modules are,

**Modulator drivers** This module is built with two layers of pre-driver and output stage. It requires  $V_{DD} = 3V$ ,  $V_{SS} = 0V$  and  $1/2V_{DD} = 1.5V$  as DC power supply. The pre-driver needs to be controlled by  $V_{ctrlh}$  and  $V_{ctrll}$  to adjust temperature variation tolerance system. In each of the modulator drivers, two groups of the pre-server works from  $V_{SS} = 3V$  to  $1/2V_{DD}$  and from  $1/2V_{DD}$  to  $V_{DD}$ . A improved push pull output stage combine outputs from these two groups of pre-driver as a output signal and fed into the output pads of chip.

**Temperature variation sensor and voltage control** This module is used for testing chip temperature and generating temperature variation control voltages ( $V_{ctrll}$  for low layer of pre-driver and  $V_{ctrlh}$  for high layer of pre-driver) to adjust the temperature variation tolerance system.

**$1/2V_{DD}$  regulator** This module generates a  $1/2V_{DD} = 1.5V$  for drivers, temperature variation sensor and voltage control module. This  $1/2V_{DD}$  generates very high fan-out as high as a global DC point.

Aside from these modules, to provide the temperature independent current source and bias voltages, a conventional band gap reference (BGR) circuit is also placed in the circuit. The design methodology of this BGR is following the [92]. From  $27^{\circ}C$  to the CMOS process limitation, and in the range of power supply is  $3V \pm 1V$ , this BGR circuit could provide the reference current and voltage which could ignore the variation.

### 8.1.2 Modulator driver

The modulator driver consists of temperature variation tolerance pre-drivers and output stage composes.

The modulator driver is presented in Fig.8.2. The parameters of the output stage is listed in Table8.1.

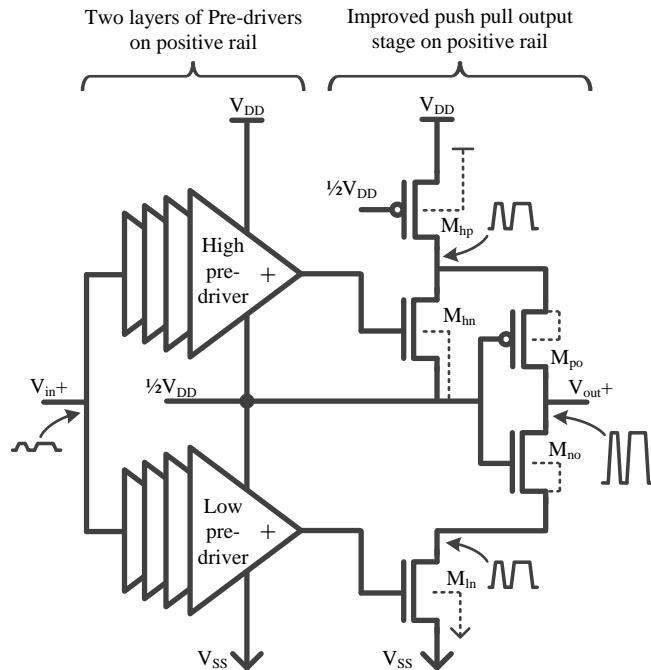


FIGURE 8.2: Modulator driver

TABLE 8.1: Parameters of major components in the improved push pull output stage

Parameter	Value
$W/L_{hp}$	$240\mu m/0.12\mu m$
$W/L_{hn}$	$45\mu m/0.12\mu m$
$W/L_{ln}$	$128\mu m/0.12\mu m$
$W/L_{po}$	$300\mu m/0.12\mu m$
$W/L_{no}$	$300\mu m/0.12\mu m$

An optimized push pull driver is used as the output stage of this modulator driver. Five transistors at the output stage are powered by  $V_{dd} = 3V$ .  $W/L_{hn}$  and  $W/L_{no}$  which are deep N-well NMOS in triple well isolation, bulk connects to the source of the transistor. The gates of  $W/L_{hp}$ ,  $W/L_{no}$  and  $W/L_{po}$  are biased at  $1/2V_{DD} = 1.5V$  which are generated from  $1/2V_{DD}$  regulator.

In the modulator driver, there are two groups of pre-drivers for each output stage. One pre-driver group (high) is powered by  $V_{dd} = 3V$  with  $V_{ss}$  as  $1/2V_{DD} = 1.5V$ . The other group of pre-driver (low) is powered by  $1/2V_{DD} = 1.5V$  with  $V_{ss}$  as the global *gnd* on chip. The high pre-driver is placed in a triple well isolation area. Aside from the

triple well isolation, the high and low pre-driver are the same design. These two pre-driver both requires control voltage ( $V_{ctrlL}$  and  $V_{ctrlH}$ ) which generates from temperature variation sensor and voltage control.

Before the pre-drivers, there is a  $50\Omega$  resistance to provide as termination.

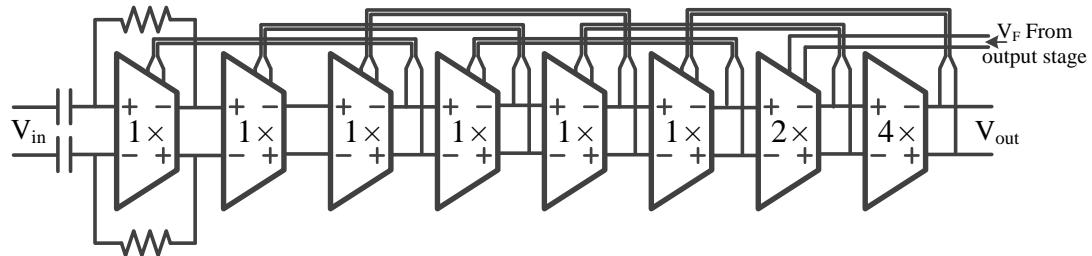


FIGURE 8.3: Temperature variation tolerance limiting amplifier

Fig.8.3 is the schematic of the pre-driver in the modulator driver. It is an 8 stage cascade limiting amplifier composed of temperature variation tolerance limiting amplifier cells. The first 6 stages are standard cells. The last 2 stages are designed as 2 times and 4 times of transistor width in standard cell. In these 8 stages, excluding the last stage, there are seven 2nd order interleaving active feedbacks. The input signal of the pre-driver is re-biased by an on-chip RC network.

The temperature variation tolerance limiting amplifier cell is presented in Fig.8.4 and Table8.2.

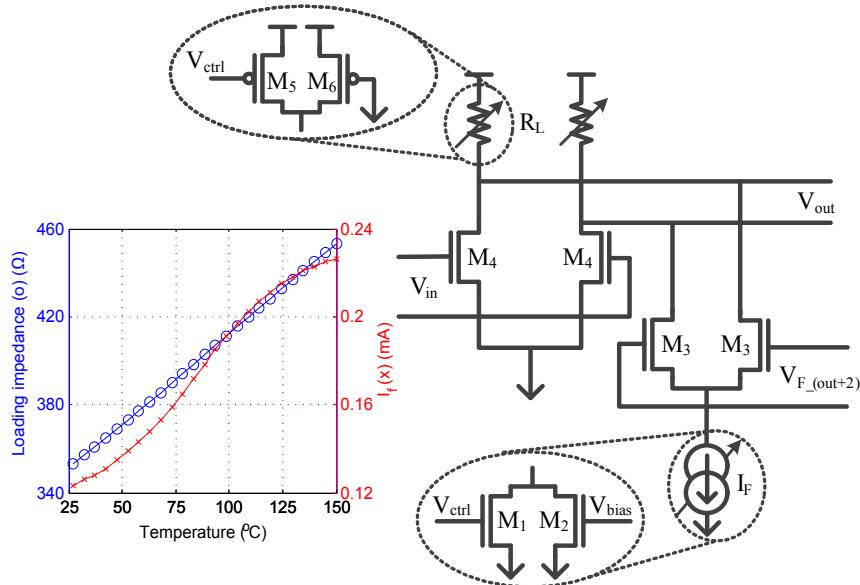


FIGURE 8.4: Temperature variation tolerance limiting amplifier cell

The adjustable load resistance and current source are composed of a transistor with a fixed bias and a transistor which is biased as a control voltage. For high and low groups of pre-drivers, the  $V_{ctrlH} = V_{ctrlL} + 1.5V$ . While the temperature increases,  $R_L$  and  $I_F$

TABLE 8.2: Design detail of temperature variation tolerance limiting amplifier cell

Parameter	Value
$W/L_1$	$2\mu m/0.12\mu m$
$W/L_2$	$2.6\mu m/0.12\mu m$
$W/L_3$	$0.5\mu m/0.12\mu m$
$W/L_4$	$8\mu m/0.12\mu m$
$W/L_5$	$2.4\mu m/0.12\mu m$
$W/L_6$	$6\mu m/0.12\mu m$

almost linearly increase to the trend in Eq.7.5 and Eq.7.6. In this implementation, the  $V_{bias} = 550mV$  which directly generates from the BGR circuit.

### 8.1.3 Temperature variation sensor and voltage control

The modulator driver requires the function of adjusting the automatically with the on-chip circuit. Therefore, an on-chip circuit which detects the temperate of the modulator driver and generates the control voltages for the modulator driver circuit with a control loop is necessary.

To provide a efficient temperature sensitive control voltage on chip, the self biased PMOS with a current source composes the temperature sensor in Fig.8.5. All current sources are based on a band-gap reference circuit which is tolerance in temperature variation. [120] illustrates the threshold voltage of MOSFAT is similar linear to the temperature variation. In this circuit,  $V_{temp}$  is grandly increasing with temperature as well.  $V_{temp}$  is recalculated via an OPAMP based subtract circuit to create  $V_{ctrl}$  to adjust the temperature variation tolerance driver.

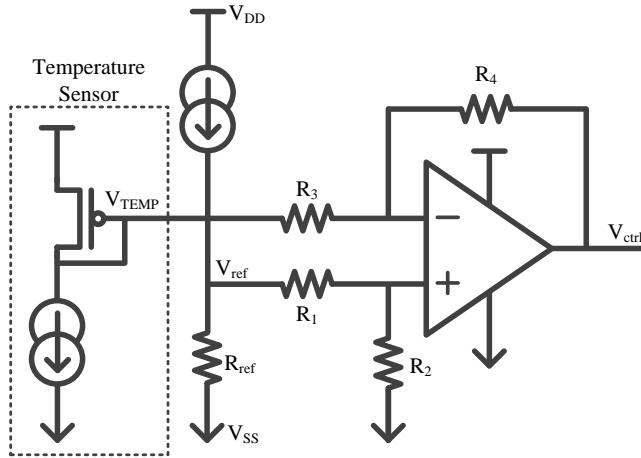


FIGURE 8.5: Temperature variation sensor and voltage control

In this design case, sensor PMOS is  $W/L = 64\mu m/0.12\mu m$ .  $I_T$  and  $I_S$  are both  $20\mu A$ .  $R_{ref}$  is  $67.8k\Omega$ , and  $V_{ref}$  is  $135.5mV$ .  $R_2/R_1 = 240.9k\Omega/60.2k\Omega = 4/1$ , and  $R_4/R_3$  are

same values and ratio. In this case,  $V_{ctrl}$  is given by,

$$V_{ctrl} = 4 \times V_{temp} - 4 \times V_{ref} \approx 4 \times V_{temp} - 540mV$$

The simulation result shows, while the temperature increases from  $27^{\circ}C$  to  $135^{\circ}C$ ,  $V_{TEMP}$  increases from  $198mV$  to  $299mV$ . Meanwhile the  $V_{ctrl}$  increases from  $252mV$  to  $656mV$ .

In this design, OPAMP is a rail to rail input rail to rail output differential to single OPAMP. With  $10pF$  capacitance load, GBW of OPMAP is  $20MHz$ , and the phase margin is  $85.6^{\circ}$ .

To compose control voltage for both high and low pre-driver, two temperature variation sensors and voltage control modules are independently working between  $V_{ss}$  to  $1/2V_{DD}$  and  $1/2V_{DD}$  to  $V_{dd}$ . The module works between  $1/2V_{DD}$  and  $V_{dd}$  is located in a triple well isolation.

#### 8.1.4 Half $V_{DD}$ generator

In the reason of a  $1/2V_{DD}$  being required in this design, an on chip half  $V_{DD}$  regulator is also necessary.

As Fig.8.6 presents, it is a typical regulator.  $V_{ref}$  is generated by a middle voltage point with two resistors ( $R_{shunt} = R_{tail}$ ). OPAMP is a very large fan-out regulator use rail to rail differential in single output OPMAP which is designed with high voltage transistors (available until  $3.6V$ , minimal length is  $0.4\mu m$ ) in this  $0.13\mu m$  CMOS process. This regulator could drive up  $R_L = 10\Omega$  and  $C_L = 300pF$  with  $GBW = 3.5MHz$  and  $Phase\ margin = 85^{\circ}$ .

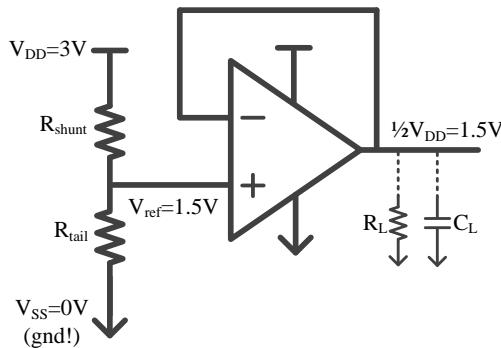


FIGURE 8.6:  $1/2V_{DD}$  regulator

### 8.1.5 Modulator driver layout

Fig.8.7 is the layout of this modulator driver. DC pads (vdd and vss) are located at the top and bottom of the layout area. Input and output signal pads are on the order of 'gnd!', 'signal+', 'gnd!', 'signal-', 'gnd!'. The placed signal pads are of  $0.15\text{mm}$  pitch.

On the layout view of this design, all modules are clearly labeled.

This is an inductor-less design. Including all of the IO pads, the layout area is  $950\mu\text{m} \times 1050\mu\text{m} = 997500\mu\text{m}^2 \approx 1\text{mm}^2$ . Layout area cost of two rails of modulator drivers are only  $0.11\text{mm}^2$ .

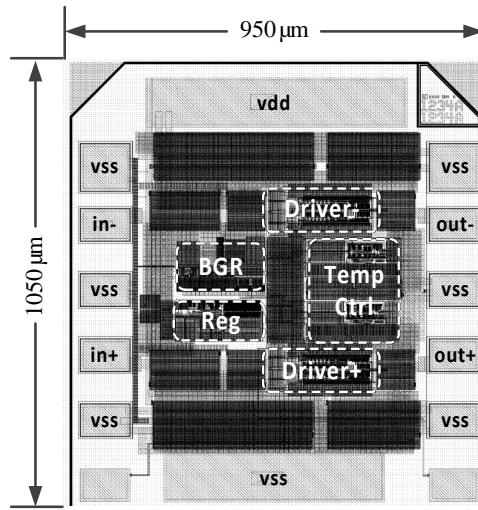


FIGURE 8.7: Layout of temperature tolerance modulator driver

## 8.2 Simulation result

The simulation environment of the temperature tolerance modulator is plotted in Fig.8.8.

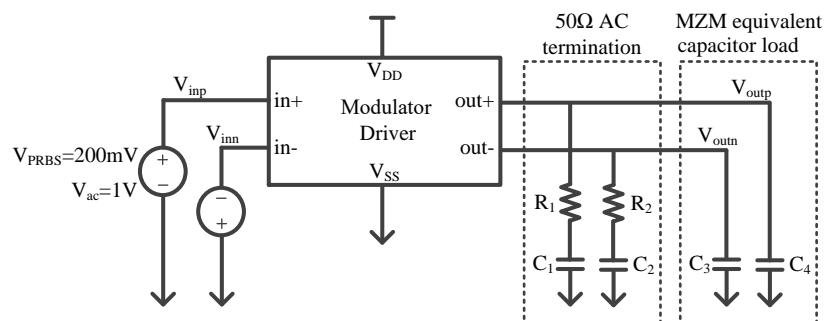


FIGURE 8.8: Testing environment of temperature variation tolerance modulator driver

The power supply of the modulator driver is  $Vdd = 3V$ . The transient input is a pair of differential  $2^7 - 1$  pseudo-random bit sequence (PRBS) with 200mV amplitude. Outputs are AC  $50\Omega$  terminated with  $R_1 = R_2 = 50\Omega, C_1 = C_2 = 10\mu F$ . A pair of MZM attenuation equivalent capacitor  $C_3 = C_4 = 150fF$  are connected to the output as well.

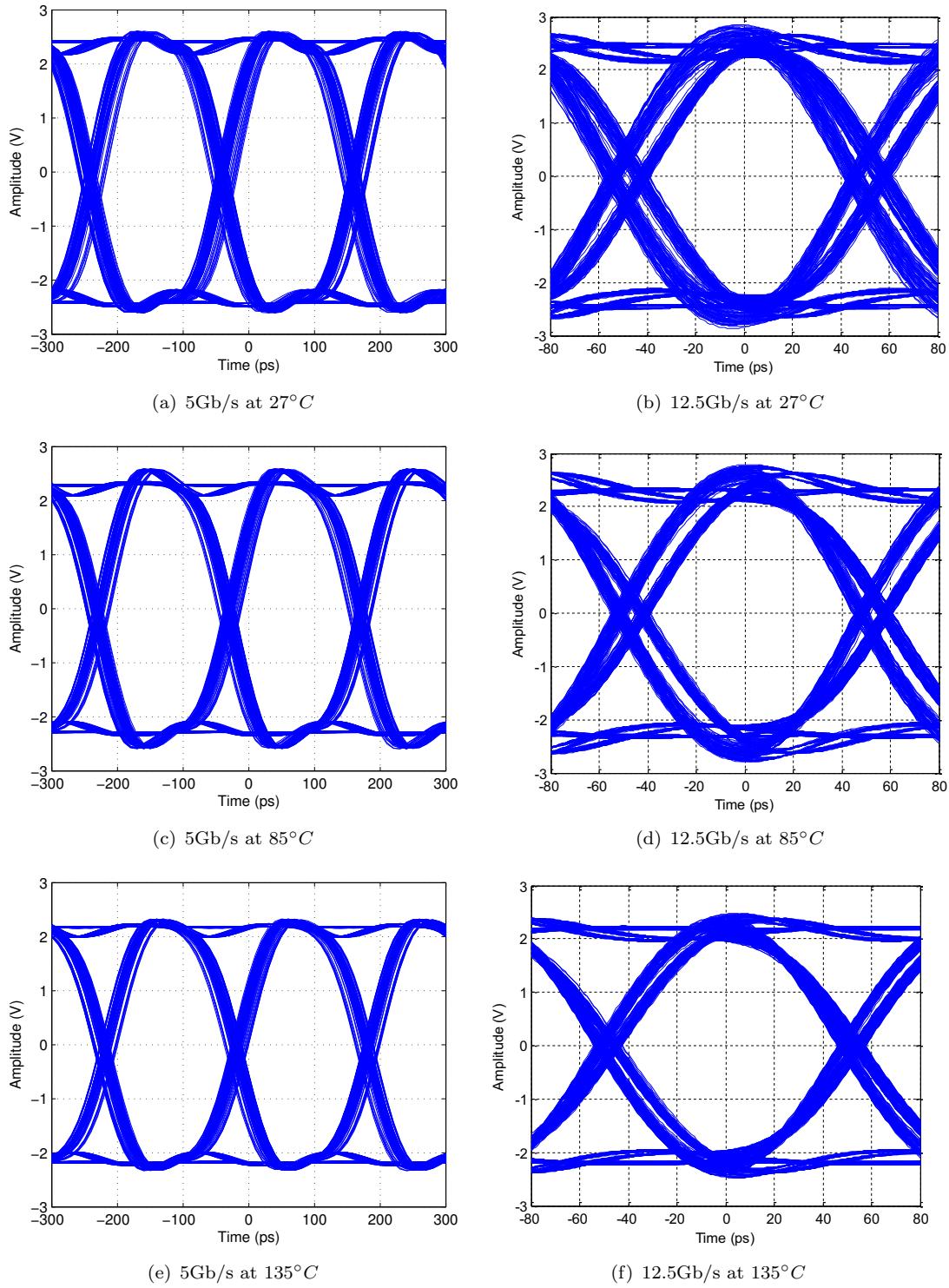


FIGURE 8.9: Modulator driver outputs under temperature variation

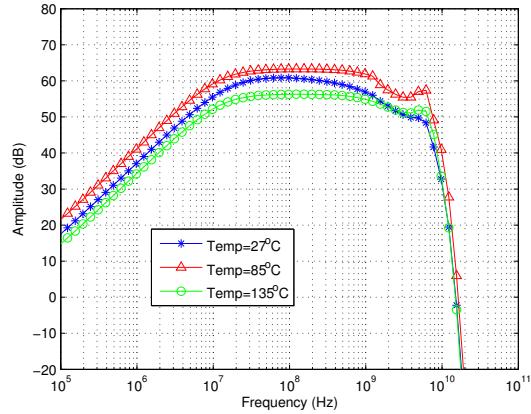


FIGURE 8.10: AC response of modulator driver under temperature variation

Fig.8.10 presents the AC response of the modulator driver under different temperatures. The gain of modulator driver is always over 50dB and the cut off frequency is close to 7GHz. Compare with result on  $27^{\circ}\text{C}$ , while the temperature increases to  $85^{\circ}\text{C}$  and  $135^{\circ}\text{C}$ , most performance of the modulator driver are maintained.

Fig.8.9 presents the modulator driver outputs as eye-diagrams under three temperatures at 5Gb/s and 12.5Gb/s. The differential output voltage swing is 4.3Vpp at  $27^{\circ}\text{C}$ . With temperature increases, it is reduced to 4Vpp at  $135^{\circ}\text{C}$ .

The observed  $Idd = 125.7\text{mA}$  at  $27^{\circ}\text{C}$  with 12.5Gb/s data transmission. In all temperature conditions, it is the highest power consumption. While temperature increases, the power consumption of the modulator driver is minor reduces. Until  $135^{\circ}\text{C}$ , there are  $5\text{mA}$  reduction. Therefore, the power consumption of the modulator driver is  $Idd \times Vdd = 125.7\text{mA} \times 3\text{V} = 377.1\text{mW}$  or less.

A significant backward of the design is the jitter of the signal which is causing by the active feedback circuit creates a peaking around the cut off frequency. In the varied temperature, though the active feedback compensates the bandwidth loss, it also compromised with the extra peak which leads to the higher jitter on the output.

The previous simulation results are based on tt corner of the process. More specific simulation conditions and an simulation example are presented in App. A.

### 8.3 Testing result

In order to test the modulator driver in different temperature environment, a thermal test platform is built.

To avoid high temperature damage on PCB, in this test is made by Rogers<sup>1</sup>, not FR4. In the reason either super glue (functional up to  $120^{\circ}\text{C}$ ) or general conductive epoxy (melt

<sup>1</sup>Rogers 4003, heatproof  $280^{\circ}\text{C}$

at less  $150^{\circ}\text{C}$ ) are less or too close to the target test temperature, a high temperature epoxy<sup>2</sup> is used in this test to mount the chip on PCB. DC power of the modulator driver is suggested by PCB via bonding wires (DC sockets on PCB is at the far end on PCB).

Input signals of the modulator driver are provided by 200mV  $2^7 - 1$  PRBS via coaxial cable and RF probes. The out+ is fed into digital communications analyzer (DCA) via RF probe and coaxial cable. The out- is connected to a AC  $50\Omega$  termination via RF probe.

Fig.8.11 presents the microscope viewed modulator driver.

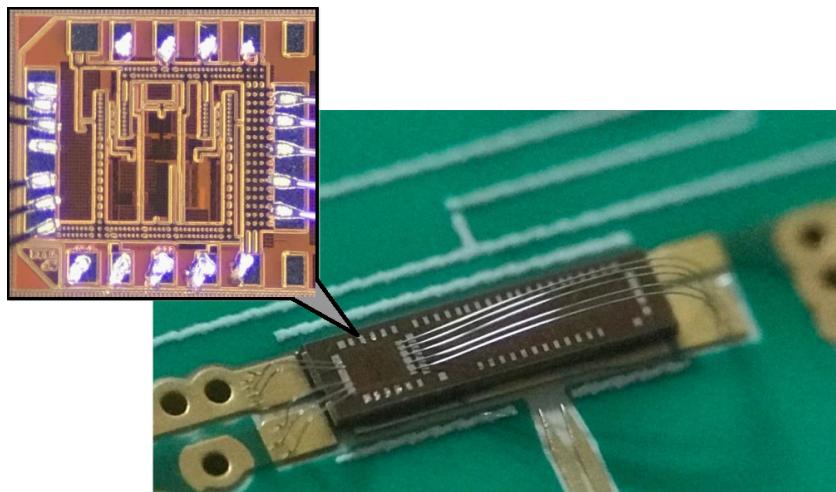


FIGURE 8.11: Microscope view of the modulator driver

In order to provide the adjustable thermal environment for the modulator driver, a heating air gun which is available to adjust the heating temperature is placed on the top of the chip. While the high temperature is needed, the air flow keeps shooting on the design under test to provide thermal environment which is same as the air gun displayed. A disadvantage of this adjustable temperature test bench is due to area limitation of the original RF test bench, the thermal camera cannot located close to the chip for further accurate temperature measurements. To note, in the test, the temperature of the chip should be close to the display on heating air gun, but there might be a tolerance of several degrees. In order to ensure that the established high temperature environment is effective, each high temperature test is started after the air gun building the thermal environment is stable (at least 3 mins before test).

Fig.8.12 presents the eye-diagram of modulator driver output at room temperatures. The 2Gb/s, 5Gb/s and 10Gb/s are tested with 3V power supply and the power consumptions at these three tests are on the order of 345mW, 351mW and 372mW. While increases the power supply until 3.3V, the modulator driver is also functional at 12.5Gb/s data transmission with 468mW power consumption.

<sup>2</sup>High temperature epoxy from HG chemicals, heatproof  $250^{\circ}\text{C}$  after solid

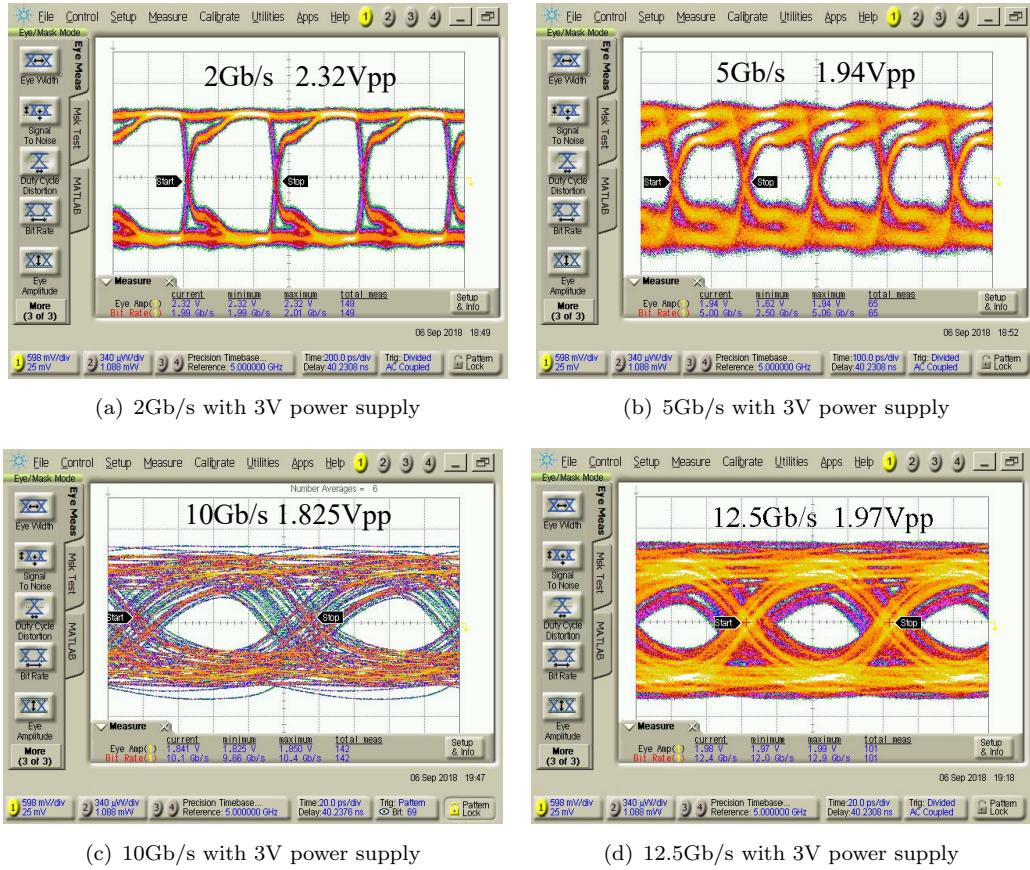


FIGURE 8.12: Measurement of modulator driver at room temperature

The modulator driver under different temperature are also investigated. Fig.8.13 presents the outputs of modulator driver with 10Gb/s data at  $27^{\circ}\text{C}$ ,  $85^{\circ}\text{C}$ ,  $105^{\circ}\text{C}$  and  $135^{\circ}\text{C}$ . In the thermal test, the power supply of modulator driver is 3V. While temperature increases, the power consumption reduces from  $372\text{mW}$  at  $27^{\circ}\text{C}$  to  $361\text{mW}$  at  $135^{\circ}\text{C}$ .

A significant drawback of the design is the jitter of the signal, which is caused by the active feedback circuit that creates a peaking around the cut off frequency. With varied temperature, though the active feedback compensates the bandwidth loss, it also compromised with the new peak, which leads to the higher jitter on the output.

The output voltage swing of the modulator driver reduces along with the increasing temperature. Until  $105^{\circ}\text{C}$ , there is the  $54\text{mV}$  reduction, and in the further  $30^{\circ}\text{C}$  increases, the extra  $123\text{mW}$  reduction is observed.

## 8.4 Analysis

Compare with the simulation result, the performance of the modulator driver in the test is reduced. The transmission speed with standard power supply  $Vdd = 3\text{V}$  is limited at 10Gb/s. To achieve the 12.5Gb/s transmission, the modulator driver needs

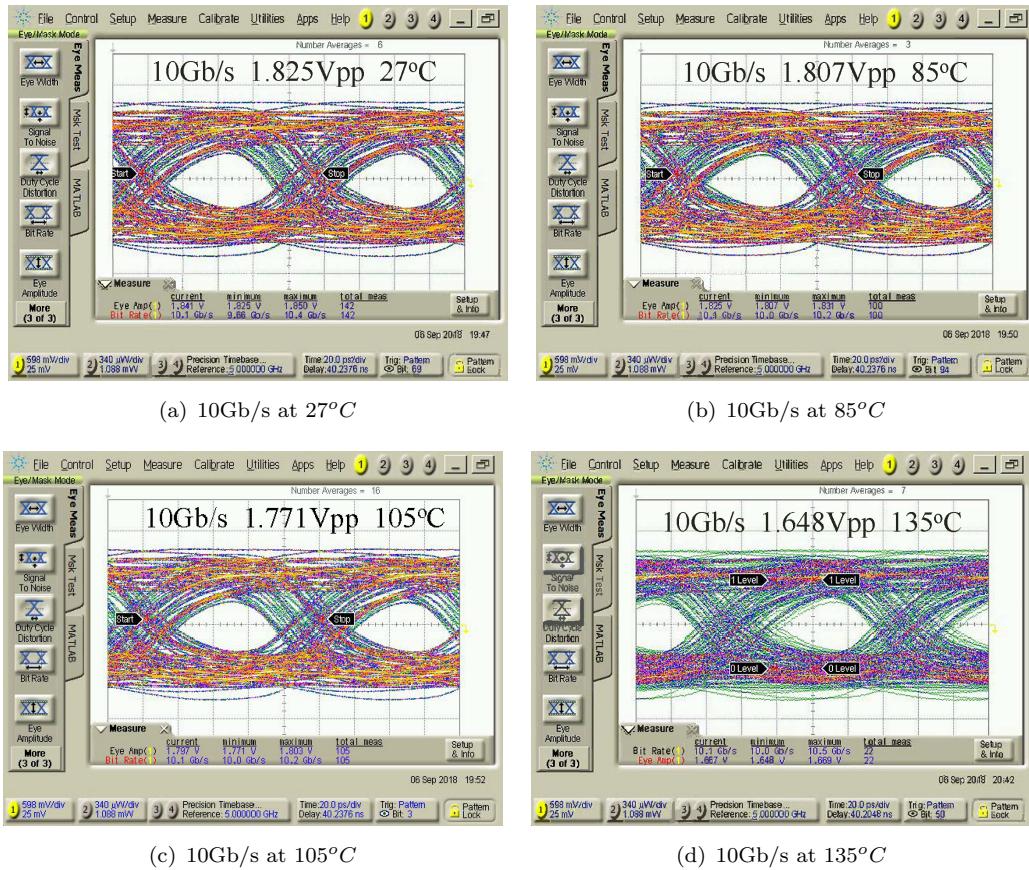


FIGURE 8.13: Measurement of modulator driver in thermal environment

to increase the power supply to 3.3V. On the other hand, compared with simulation, there is almost 200mV output voltage swing reduction on the single end in the test. However, the high-temperature trend of reduction in output voltage swing is the same as the simulation.

The bandwidth and output voltage swing reduction in the test could be explained as the design mistake on the output impedance of the modulator driver is not  $50\Omega$ . This mistake could be optimized in the future designs with a near-end on-chip termination network as shown in the Ch.4.

Though there is some variation between the simulation and test, the temperature variation tolerance system maintains the most performance of the modulator driver in both results. In case to neglect the absolute value of performance, the trend of simulation and test in temperature variation are the same.

Until  $105^\circ\text{C}$ , the output voltage swing reduction is only 54mV on the single end. Consider about most RF device is only support working environment up to  $85^\circ\text{C}$  with significant performance variation, this modulator driver for MZM could increase the system level reliability on temperature variation.

In addition, the automatic control loop for the temperature variation tolerance system

in this implementation consists of all on-chip circuit. In the system level, it avoids using the PD as a sensor. This control loop simplifies system complexity and avoids additional integrations. Furthermore, compares with the conventional power control loop solution, this automatic control loop cooperates with the novel temperature variation tolerance system is an optimized efficient solution for modulator drivers.

## 8.5 Summary

In this chapter, a modulator driver is demonstrated in IBM 130nm CMOS process. The modulator driver which includes the automatic control loop for temperature variation, consists of on chip circuit. From room temperature to CMOS process limitation, it generates over 50dB gain and 7GHz bandwidth with less than 377mW power consumption. In a wide temperature variation range, the performance of this modulator driver is maintained.

This implementation could optimize the system level reliability on temperature variation. In both simulation and test, this design confirms that the methodology of the temperature variation tolerance system in Ch.7 is functional.



# Chapter 9

## Conclusions and future work

### 9.1 Conclusions

In recent years, silicon photonics has become one of the long term solutions to the interconnect bottleneck. However, the si MZM, which appears in most literature is still driven by commercial amplifiers. In the future, the silicon photonics for interconnection may need to replace the interconnections between modules even inner of a chip. Also, integrating a commercial amplifier with a silicon chip is nearly impossible. Therefore, optical modulators need to build up modulator drivers and related circuits based on a typical CMOS process. In this scenario, multiple additional requirements, such as power efficiency, reliability and compact integration must be added into the performance list together with operating speed. This research project has investigated, and presented the results, of CMOS modulator driver design methods for thermal reliability, efficiency and compact integration of si MZM. The investigation and research appear in three parts and implements on multiple times of tape-out and experiments.

The first sub-topic investigated the thermal reliability of CMOS modulator drivers of the CMOS circuits under thermal environments, which was followed with a proposal for a novel method to maintain circuit performance. The research involved the integration into a CMOS process of an efficient on-chip feedback loop which avoided the off CMOS chip optical devices and complex peak detection circuits. The experimental result shows that the implementation of this research provides relative tolerance to a wide range of temperatures.

In order to optimize both states of the art modulator drivers on operating speed and power efficiency, a conventional push pull modulator driver is optimized as a novel N-over-N cascode push pull amplifier. An analysis of the proposed circuit shows that it provides the same bandwidth with lower power consumption in comparison to other popular modulator driver models. The proposed circuit is also further optimized on both bandwidth enhancement with inductors and boost on output voltage swing. Three

CMOS circuit implementations present the circuit performance is outstanding in comparisons to the implements in similar applications. In addition, these modulator drivers are also compactly integrated to si MZMs in order to demonstrate the optical transmitters.

The last part of the research depended on to a great extent on cooperating with the optoelectronic design team. Due to the synergistic design method, the optoelectronic design has been redirected on to a new level. The MZM could be embedded in the electronic circuit as a part of it. Based on this scenario, a more efficient modulator driver structure is implemented. Our creative attempt to bend the traditional MZM into a U shape which also creates a possibility to implement the termination as an on-chip circuit. The proposed and implemented optical transmitter is compactly integrated with only CMOS chip and the optical modulator without off-chip components. In the experiment, the optical transmitter demonstrates the 40Gb/s NRZ data transmission with 1.6pJ/bit. This optical transmitter is also available to achieve an efficient PAM4 transmitter as well. Compares to the latest publishes, this result could be a milestone in the states of the art.

In addition, while implementing these designs, the compact integration solution was defined as being a basic requirement. All these drivers can be used to replace commercial amplifiers in the general si MZM test, and are easily connected to, or even merged with any CMOS based The front-end computing unit into the same die. Most of these designs require only far end terminations after MZM thus avoiding commercial components, or onboard bias tee. In the most recent design, the compact integration is more thorough as it implements the far end termination with an on-chip circuit network that shares the CMOS chip with the modulator driver.

In recent years, silicon photonics research at the device level has become complete, therefore the next phase of development stage will be the silicon photonics circuits and commercial applications. The modulator drivers of typical CMOS processes perform the critical role of connecting optical modulators with CMOS-based computing units. The researches into reliability and efficiency have also brought the integrated silicon photonics closer to the applications in the silicon photonics circuits together with multiple modulators be an essential part for the photonics circuit.

The investigation, design and results described in this thesis bring this PhD project to a conclusion, and it is hoped that they may advance to another stage the design and application of drivers for si modulators.

## 9.2 Future work

The next steps for the project will involve continuing with the development of the modulator and related circuits in order to pursue further performance optimization.

Two practical plans, a U-shape optical transmitter based silicon photonics circuits, and an optical transmitter on bifilar MZM, will be undertaken in the next phase of this research.

- U-shape optical transmitter based silicon photonics circuits

The optical transmitter demonstrated in Ch.6 is a compact integrated device. It avoids all of the off-chip component, and the power efficiency of the optical transmitter is excellent. Hence, this approach could be extended to use into the silicon photonics circuits which require multiple modulator drivers in single device.

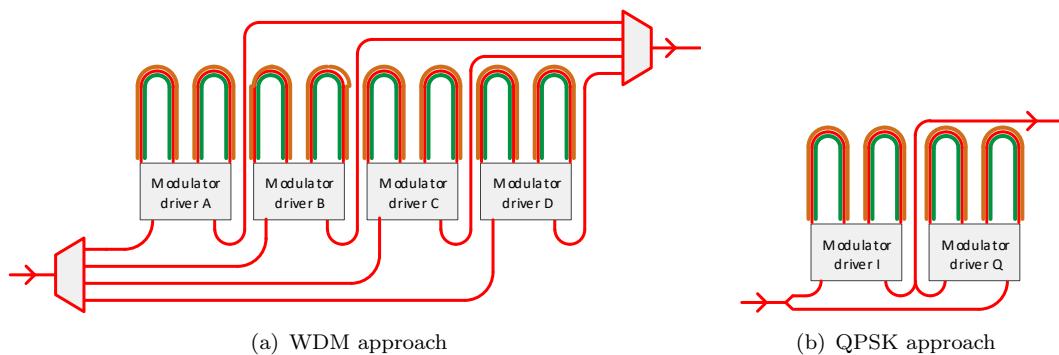


FIGURE 9.1: U-shape optical transmitter using in the silicon photonics circuit

The next step of the research is embedded the U-shape design into complex modulating optical transmitters with WDM or QPSK approaches. Fig.9.1(a) demonstrates an abstract view of a 4 channel optical WDM and a optical QPSK is presented in Fig.9.1(b). The challenge in these silicon photonics circuit is not only about the modulator driver design but also on the integrations and system control.

- Optical transmitter on bifilar MZM

Along with the developing of the CMOS technology developing, the breakdown voltage of CMOS transistor is keeping reduce. Therefore, complete the CMOS based modulator driver which still provides a high volume output swing is increasing challenge. Inspired by [113], the low power CMOS circuits integrated with the bifilar MZM may contribute to a excellent result.

The phase shifter in conventional MZM is traveling the signal on one type of doping and connect the another type of doping as reverse bias which is a AC ground. Fig.9.2 presents an abstract view of CMOS circuit driving a bifilar MZM. 4 modulator drivers can drive the 4 electrodes on bifilar MZM. Under the premise of

specific designed the power supply within deep N well technology, the modulator drivers still provide over 2V reverse bias voltages on the MZM.

In CMOS driver design, a high volume output voltage swing requirement is not

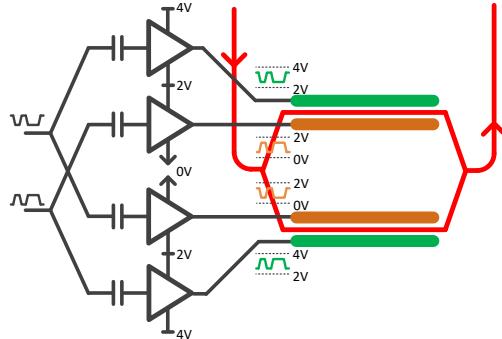


FIGURE 9.2: Optical transmitter consists of 4 modulator drivers and bifilar MZM

only limiting the bandwidth performance, but also resulting in a relatively high power consumption. 4 drivers on bifilar MZM could relieve the backwards which leads the MZM more close to the states of the art low power CMOS processes.

In addition, provide individual signals for the drivers is also a solution to provide an efficiency PAM modulation.

In future developments, increasing challenges will shift from the general electrical circuit design to method for integration and electrical modelling of the optical devices. Future research over the next few years, therefore, will involve these areas alongside further development and application of CMOS technology, which should bring about improvements in silicon photonics applications. It is hoped that the research undertaken in this PhD thesis proves to have a positive effect by enabling future investigations and developments in the silicon photonics field.

## Appendix A

# General circuit design process

This chapter briefly describes the general design process on Virtuoso<sup>1</sup>. It also includes the custom inductor design method which bases on Advanced Design System (ADS)<sup>2</sup> for circuit design. A part of limiting amplifier design from Sec.4.3.2 illustrates this process as an example.

Three CMOS processes have been used for electronic chip design in this thesis. They are IBM 130nm CMOS, TSMC 40nm CMOS and TSMC 28nm CMOS processes. The design platform is Virtuoso from Cadence, and simulation environment is based on Spectre model in Analog Design Environment L in Virtuoso as well.

The general design process is shown in Fig.A.1, and TableA.1 presents the specific software for different design processes.

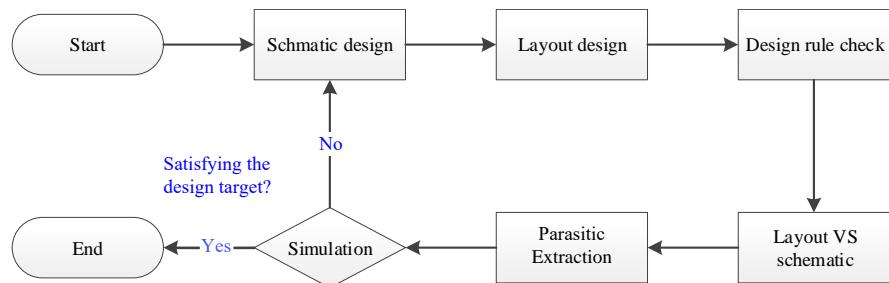


FIGURE A.1: General design process

The design goes through Design Rule Check (DRC), Layout VS Schematic (LVS) and parasitic extraction to be a net-list for post-layout simulation. For IBM 130nm CMOS

<sup>1</sup>Virtuoso, the Cadence Virtuoso System Design Platform is a tool for designing full-custom integrated circuits. It includes schematic entry, behavioral modeling, circuit simulation, custom layout, physical verification, extraction and back-annotation. Used mainly for analog, mixed-signal, RF, and standard-cell designs, but also memory and FPGA designs.

<sup>2</sup>ADS is an electronic design automation software system produced by Keysight EEs of EDA, a division of Keysight Technologies. It provides an integrated design environment to designers of RF electronic products such as mobile phones, pagers, wireless networks, satellite communications, radar systems, and high-speed data links.

TABLE A.1: DRC, LVS and parasitic extraction for different processes

Process	IBM 130nm	TSMC 40nm	TSMC 28nm
DRC	Assura-DRC	Calibre-DRC	Calibre-DRC
LVS	Assura-LVS	Calibre-DRC	Calibre-DRC
Extraction	Assura-QRC	Calibre-PEX	Calibre-PEX

process, the extraction used for post layout simulation is  $RLC$  with coupled capacitor in Assura-QRC.  $RC + CC$  in Calibre-PEX is used for both TSMC processes.

If the design target can not be satisfied, it needs to adjust the circuit parameters from the schematic level and go through the process again. Usually, the design requires to undergo several iterations of adjustment to achieve the design requirements.

Fig. A.2 presents the example of a limiting amplifier on TSMC 40nm CMOS process. It is a 3 stages limiting amplifier with shunt and serial inductors.

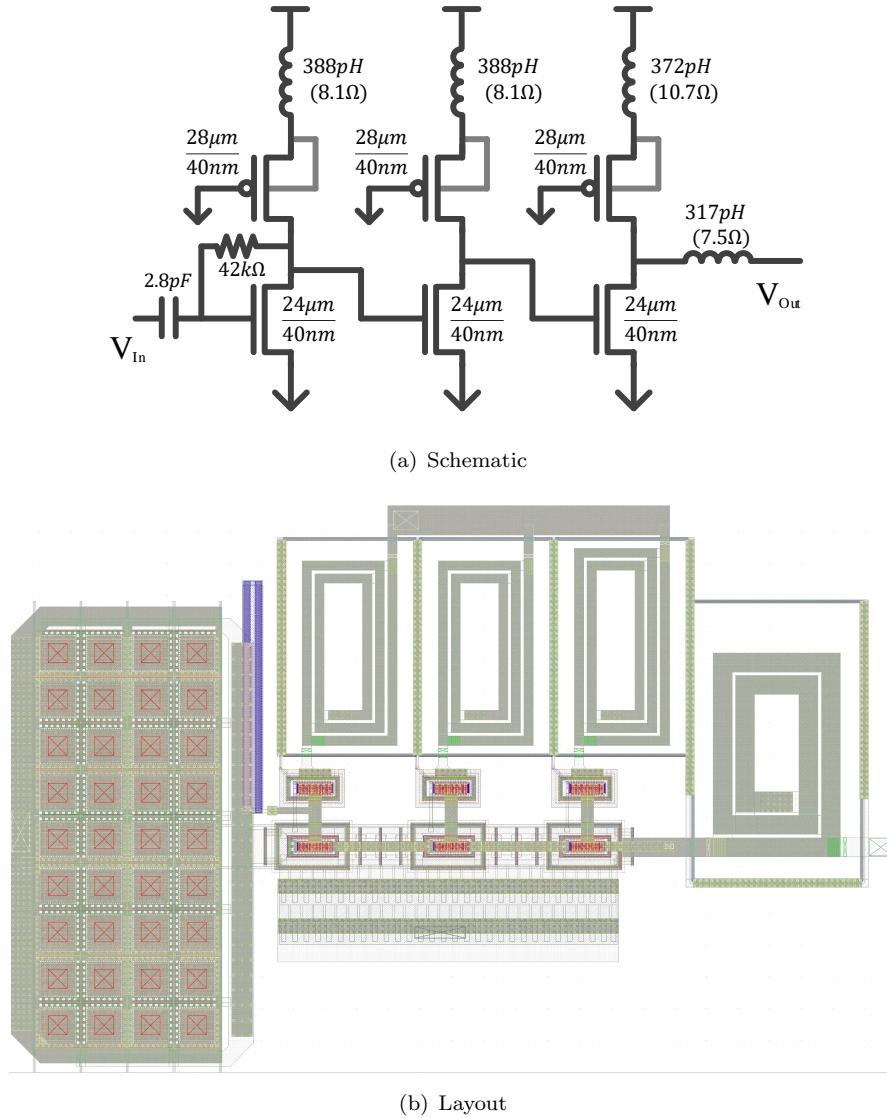


FIGURE A.2: The example limiting amplifier

In this CMOS process, the top two metal layers are thicker than others, hence they have fewer sheet resistance. Also, the parasitic capacitance of the top layers of metal is less, the inductor is designed among the top two layers of metal to minimize the parasitic.

In this example, the custom inductors are designed and modeled with ADS. The layout of inductor and the corresponding layer map are imported into ADS. The inductor is realized with M7, M8 and the Via between these two metal layers. The substrate data utilized in ADS modelling is presenting in Fig.A.3.

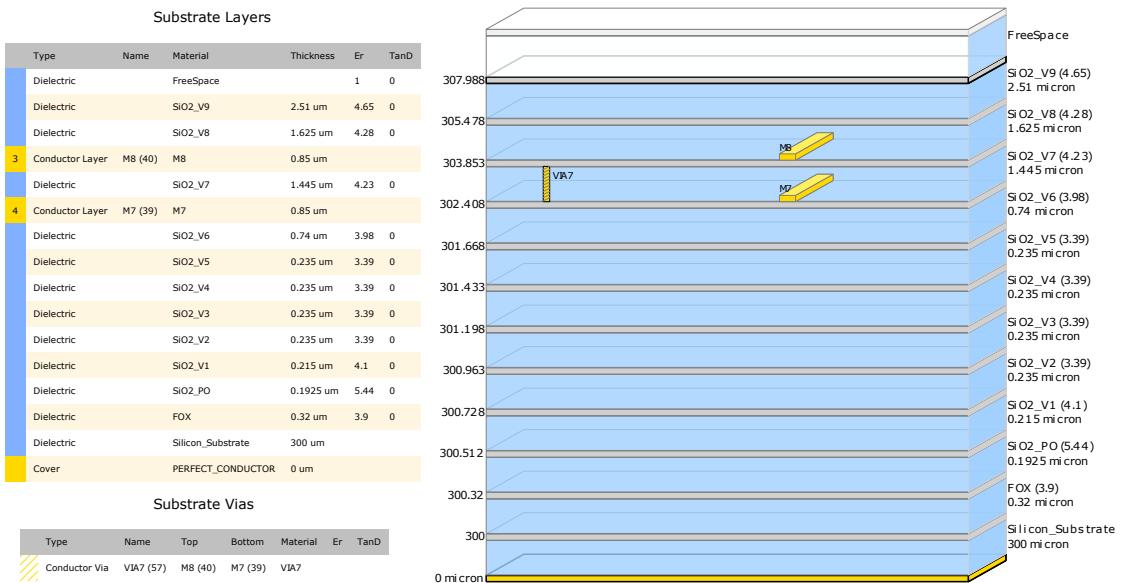


FIGURE A.3: Substrate data utilized in ADS for example custom inductor

Fig.A.4 illustrates the modeling result of the 3rd stage shunt inductor. While the ADS simulation, a guard ring which connects to the *Gnd!* is surrounding the inductor. In Virtuoso layout design, corresponding guard ring area with dummy fill free mask is placed in the design as well.

$Q = \frac{L_{eff}}{R_{eff}}$  defines the quality of inductors. The most efficient way to increase the Q factor is to increase the diameter of the inductor. It is a compromise between the quality of custom inductor and the layout area cost.

The extracted layout eliminates the inductors and replaces the connections to inductor as a pair of IO. The inductor is placed into the top-level layout with additional dummy metal resistor to avoid the LVS error. In Spectre simulation, the ADS simulated custom inductor is transferred to an S-parameter model and embedded into the circuit as an N-port model (s2p for inductors).

Fig.A.5 presents the simulated AC response of schematic level and extracted layout circuit. In the simulation, the example circuit is loading a  $50fF$  capacitor. For both schematic and extracted layout, the custom inductors are the same model from ADS.

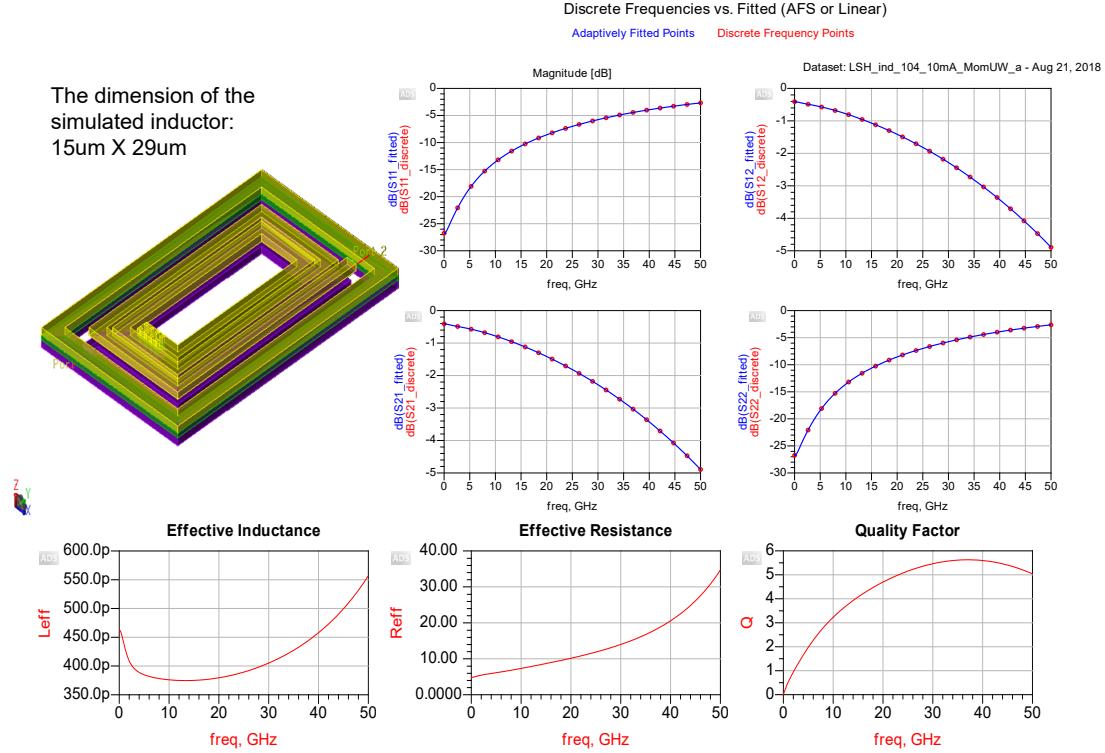


FIGURE A.4: Modeling the custom inductor in ADS

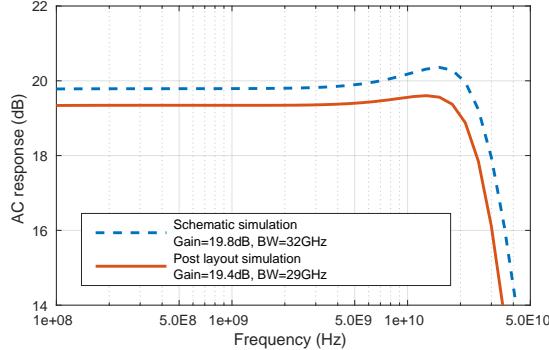


FIGURE A.5: Comparison of simulated AC response on schematic and extracted layout

Both mid-band gain and the bandwidth of the amplifier reduce in the extracted layout simulation due to parasitics.

The Spectre is supporting to simulate all of the process corners. Fig.A.6(a) presents a general CMOS process corner plot. The standard process corner of fabrication is TT corner.

Fig.A.6(b) presents the AC response of the example circuit on FF, SS and TT process corners. Clearly, both of the mid-band gain and bandwidth of this limiting amplifier reduce on the order of SS, TT and FF. In addition, the power consumption also increases from 13.4mW at SS to at 15.5mW and 18.7mW at FF.

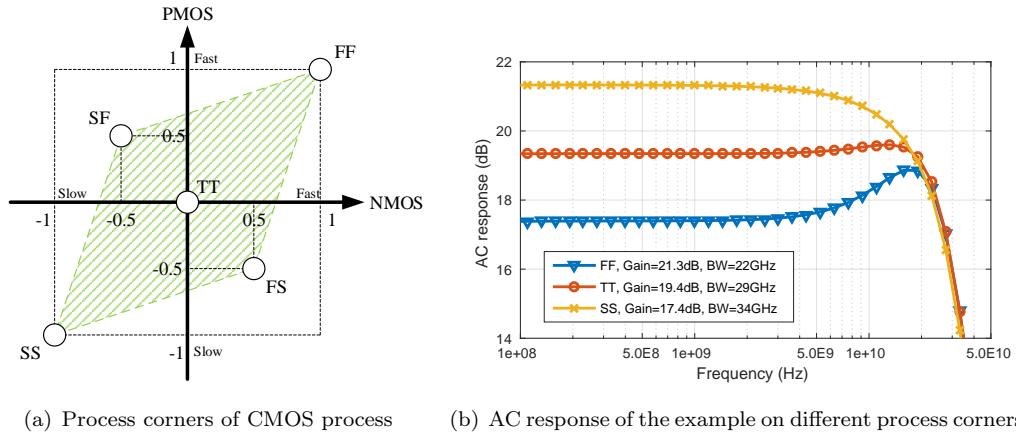


FIGURE A.6: Process corners of CMOS process and the AC response of example circuit on different process corners

All presented simulation results in the thesis are on the process corner TT. And all the designs are simulated under corner FF and SS for functionality check before the submission to manufacturing.



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